Design and Implementation of a Converter with Wide Operating Range Using a Variable-Inverter-Rectifier-Transformer Structure

by

Intae Moon

B.S., Electrical Engineering, University of Illinois Urbana-Champaign (2016)

Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering and Computer Science at the MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 2018

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Abstract

Power supplies for portable electronics such as cell phones, tablets, and laptops characterized by the low-voltage load are supplied by a single-phase grid-tied ac-dc converter. Achieving miniaturization and high efficiency of power supplies in this application is challenging due to the large voltage conversion ratios and the large variations in conversion ratios. The fact that low-output-voltage, large step-down transformers are often constrained by a minimum single-turn secondary also exacerbates loss and size constraints in such applications. To address this, a new hybrid magnetic-electronic structure is explored - the Variable-Inverter-Rectifier-Transformer (VIRT). This new approach enables voltage conversion in which the transformer provides fractional and reconfigurable effective turns. This new VIRT approach is developed, and multiple implementation approaches are explored, designed and implemented. This design is further augmented with a rectifier topology which allows for a full utilization of the effective core area in all modes of operation and hence improvement in a core loss. Moreover, a hybrid Litz-PCB construction of VIRT transformer is explored. This approach reduces copper loss and easily satisfies the voltage insulation requirements in such "off-line" applications (2.5 kV in this case [1]) through use of a triple insulated litz wire.

Thesis Supervisor: David J. Perreault
Title: Professor of Electrical Engineering and Computer Science
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Chapter 1

Introduction

In the consumer electronic market, there has been a great interest in miniaturizing chargers that power portable electronics such as smartphones, tablets, and laptops. In parallel with this trend, advances in power semiconductors such as Gallium Nitride FETs have opened up opportunities for miniaturization and efficiency of these converters. However, advancement in passive components such as inductors and capacitors have not kept pace with that of power semiconductor technology. Consequently, the performance of many power converters, including size and efficiency, are largely determined by passive components, especially magnetic components due to their major contribution to the power transfer mechanism of the converter [5].

In “off-line” (grid-tied) charger applications, a transformer with a large turns ratio is often implemented to provide the large step-down conversion from the high (and variable) grid voltage to the low-voltage levels needed for the output. This transformer must meet the safety isolation requirement and - for many designs - widely varying voltage conversion ratios [6]. This type of large step-down, low-voltage-output design often leads to the situation where the secondary comprises a (minimum) single turn, and the copper loss of the transformer greatly exceeds the core loss. This imbalance of the loss mechanisms (driven by the inability to further reduce secondary turns) compromises the efficiency of the transformer. The ability to minimize loss is fundamentally limited since a full single turn is required for a conventional transformer. In other words, if the transformer losses are not balanced and optimized after either
winding reaches a single turn, one either has to accept the losses as they are or find another means to optimize transformer losses such as using a larger transformer core or changing the turns ratio.

Therefore, transformers that can – in some true sense - achieve fractional turns are extremely valuable in applications requiring low voltage outputs where the ideal secondary would have less than one turn. While previous research has touched upon "flux-division" approaches towards fractional turns [7], [8], these previous approaches do not fully help reduce the copper-loss concerns of low-voltage transformer design. In addition, the converters with these large step-down transformers are often required to accommodate wide operating ranges. As a notable example, a Universal Serial Bus – Power Delivery (USB-PD) wall charger needs to be designed such a way that it can accommodate the universal ac voltage (85 – 265 Vac) from the grid as an input and provide a regulated output voltage between 5 V_{dc} and 20 V_{dc} [6]. This design requirement imposes a great challenge to implementing the compact, efficient converter design due to the large step-down ratios and large variations in operating voltages.

This thesis explores the development, design and application of a hybrid electronic-magnetic transformer structure, the Variable-Inverter-Rectifier-Transformer (VIRT), that addresses these challenges [2]. In Chapter 2, the magnetic circuit and electrical model of the proposed structure are developed and the prototype is designed and implemented to verify the model and its benefits in the wide operating condition. In Chapter 3, the VIRT rectifier topology augmented with the "bypass" switch which enables an utilization of the full core area across all VIRT modes of operation is introduced. In addition, a hybrid transformer where its primary-side winding consists of a Litz wire and the fractional secondary turns are built with the PCB traces is introduced and designed in order to further optimize the transformer loss. In Chapter 4, the optimal VIRT DC-DC design with the bypass switch and hybrid transformer carefully chosen in Chapter3 is simulated, implemented, and tested. Its performance with the bypass switch is compared to the conventional VIRT mode of operation. Finally, other rectifier implementation approaches for the VIRT structure
are introduced and future work including designing a full ac-dc system is explored.
Chapter 2

Variable-Inverter-Rectifier-Transformer
(VIRT)

In order to address the design challenge with a high-turns ratio transformers limited by a single-turn winding, we have recently proposed a new hybrid electronic and magnetic structure named a Variable-Inverter-Rectifier-Transformer (VIRT) that achieves a transformer with a fractional and reconfigurable effective turns ratio [2]. The proposed structure is named this way because it realizes the hybridization between an electronic structure, an inverter or rectifier, and a magnetic structure of the transformer, which provides a variable conversion ratio and effective fractional turns. The effective fractional turn enabled by the proposed structure enables a reduced copper loss and miniaturization by providing a designer with a means to further scale down the absolute number of turns for the transformer, enabling overall loss minimization. In addition, the variable effective conversion ratio enables the proposed structure to better accommodate wide operating voltages without compromising efficiency and overall size of the system.
2.1 Principle of Operation

Shown in Fig. 2-1 is an example of the proposed VIRT structure. A primary winding around the core center post (not shown) generates flux though the center post of the core. The two full-bridge rectifiers named A and B, respectively, are distributed around the magnetic core and connected through two secondary half-turns around the center post. Rectifier A consists of two half-bridge cells labelled A1 and A2, and Rectifier B consists of cells B1 and B2. Finally, each cell is connected to the output bus terminals, \( V_{\text{out}} \) and GND through power and ground planes that are routed outside the magnetic core.

Each rectifier can be operated as a full-bridge (FB), half-bridge (HB), or "zero" mode. When a rectifier is operated in a FB mode, both half-bridge cells (e.g. A1 and A2) are active, switching as a full-bridge structure. In a HB mode, only one half-bridge cell is active while the other cell is shorted to the ground. In a zero mode, both cells are shorted to the ground, effectively creating an ac short path for the current to flow for that section of the secondary winding. By combining these two rectifiers, 5 different modes of VIRT can be configured: FB/FB mode, FB/HB mode,
HB/HB mode, FB/0 mode, and finally HB/0 mode [2]. These different modes can be used to support wide output voltage range. For example, in a USB-PD application where the output voltage may be regulated to any of 5 V, 9 V, 15 V, or 20 V, one can select among FB/FB, HB/HB, and HB/0 modes to support the different output voltages while preserving low transformer loss.

![Diagram of induced current flow on the secondary side in each operating mode.](image)

Figure 2-2: Induced current flow on the secondary side in each operating mode.

An effective turns ratio provided by each mode can be intuitively figured out by looking at the induced current through the secondary winding and the output voltage insertion into the secondary winding through the two rectifiers. For example, in a FB/FB mode (Fig. 2-2a) where both rectifiers A and B are in a FB mode and A1 and B1 cells are switching in phase, the induced current around the secondary loop flows in a way that the output voltage $V_{out}$ is inserted twice into the loop. Given that the flux through the core is generated by applying an ac voltage with peak $V_p$ onto the primary winding with $N_p$ turns, it yields $\frac{V_p}{N_p} = 2V_{out} = \frac{V_{out}}{0.5}$ using Faraday’s law and equating the generated flux. Note that this voltage conversion ratio is effectively equivalent to that of a $N_p : 0.5$ transformer, where $N_p$ is the number of primary turns. Similarly, in HB/HB mode (Fig. 2-2b) the output voltage $V_{out}$ is inserted once into the loop due to the voltage-halving action of the half bridges. This results
in \( V_p/N_p = V_{out} \), which is equivalent to the voltage conversion ratio of a \( N_p : 1 \) transformer. Finally, in HB/0 mode (Fig. 2-2c) one can achieve the effective voltage conversion ratio of a \( N_p : 2 \) transformer since only the half of \( V_{out} \) is inserted into the loop. However, in a HB/zero mode an ac short is effectively created around one leg of the core ideally rejecting the ac flux though that section of the core, which increases the peak flux density of the given core due to the reduced effective core area and hence core loss. This poor utilization of the core area can be resolved by utilizing the bypass switch introduced in Chapter 3.

### 2.2 Electrical Model

In order to derive the electrical model of the VIRT structure, one has to come up with a magnetic circuit model based on the current flows around the transformer and induced flux as shown in Fig. 2-3. \( \dot{I}_A \) and \( \dot{I}_B \) represent the current flows between the half-bridge cells in full-bridge rectifiers A and B, respectively. The current components of \( \dot{I}_A \) and \( \dot{I}_B \) inside the core are expected to be equal since two half-turns and rectifiers A and B shown in Fig. 2-1 are identical and symmetric and effectively form a single loop around the center post which the primary-side induced flux passes through. Therefore, the current components of \( \dot{I}_A \) and \( \dot{I}_B \) outside the core, represented as dotte lines in Fig. 2-3a, are virtual and invoked for the modeling purpose along with the another virtual current component \( \dot{I}_G \) serving to cancel out virtual components of \( \dot{I}_A \) and \( \dot{I}_B \) such that the net current flow in this model is equivalent to the flow of the physical current inside the core as shown in Fig. 2-2a [2].

Fig. 2-3b shows the resulting magnetic circuit with a transference element, \( L \), associated with the small resistance \( R_{SH} \) of the ground plane around the core in a magnetic circuit [9]. Due to the small resistance associated with the ground plane, it is safe to assume \( R_{SH} \) is close to zero and the resulting magnetic circuit simplifies to a standard three-winding transformer as shown in Fig. 2-3c [2]. Due to the geometry of the EQ type core, one can assume \( R_{CA} = R_{CB} \) and \( \Phi_A = \Phi_B \). Finally, an electrical model shown in Fig. 2-4 can be derived based on the simplified magnetic circuit in
Figure 2-3: Magnetic circuit derivation of VIRT model. Solid lines correspond to real components of currents, while dotted components correspond to virtual components of currents invoked for modeling purpose [2].

Figure 2-4: The electrical model of the proposed VIRT Structure [2].

Fig. 2-3c.

With the derived electrical model in Fig. 2-4, one can compute magnetizing inductance in each mode of VIRT operations. In a symmetric operation such as
Table 2.1: Summary of VIRT operations. Detailed derivations for FB/FB, HB/HB, and HB/0 modes are covered in [2]. Note that "net" magnetizing inductance is calculated assuming a fixed gap across all three core legs.

<table>
<thead>
<tr>
<th>VIRT mode</th>
<th>Description</th>
<th>Effective Turns Ratio</th>
<th>Mode Type</th>
<th>&quot;Net&quot; Magnetizing Inductance*</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB/FB (Fig. 2-2a)</td>
<td>All switches active</td>
<td>Np : 1/2</td>
<td>Symmetric</td>
<td>( L_M = \frac{N_p^2}{2R_{cc}} )</td>
</tr>
<tr>
<td>HB/HB (Fig. 2-2b)</td>
<td>A2, B2 active A1, B1 short to GND</td>
<td>Np : 1</td>
<td>Symmetric</td>
<td>( L_M )</td>
</tr>
<tr>
<td>HB/0 (Fig. 2-2c)</td>
<td>B2 active A1, A2, B1 short to GND</td>
<td>Np : 2</td>
<td>Asymmetric</td>
<td>( \frac{2}{3}L_M )</td>
</tr>
</tbody>
</table>

* "Net" magnetizing inductance means \( L_A + L_B \) in Fig. 2-4.

FB/FB and HB/HB mode, it is straightforward to derive \( L_A = L_B = \frac{N_p^2}{2R_{cc} + R_{ca}} \) assuming \( R_{ca} = R_{cb} \) and \( \Phi_P = \Phi_A + \Phi_B \) where \( \Phi_A = \Phi_B \). Note that \( R_{ca} = R_{cb} = 2R_{cc} \) since the cross section of each side leg of the core is twice larger than that of the center post. In an asymmetric operation such as HB/0 mode, an ac-short is effectively created around one leg of the core ideally rejecting the flux through that section of the core as mentioned before. In a case where half-bridge cells A1, B1, and B2 are shorted to the ground, the overall magnetizing inductance is solely decided by \( L_A \) given that on-resistances of the bypassed switches and resistance of the ground plane around the core are negligible. Therefore, \( L_M = L_A = \frac{N_p^2}{R_{cc} + R_{ca}} \) [2]. A magnetizing inductance in each VIRT mode is listed in Table 3.1.

2.3 Experimental Design

In order to demonstrate the proposed VIRT structure and its benefits in a wide input and output range operation, an experimental prototype, which handles the input voltage range of 120 - 380 \( V_{dc} \) and regulates the output voltage to any of 5 V, 9 V, and 12 V at 5 A, 4 A, and 3 A, respectively, has been designed and built. These operating points which require widely varying, high conversion ratios are particularly suitable for the VIRT application. Furthermore, a stacked half-bridge inverter which compresses the widely varying input voltage is implemented with a LLC resonant tank and VIRT implemented on the rectifier side as shown in Fig. 2-5.

Designing a LLC resonant tank with VIRT requires special considerations since
an effective load resistance \( R_{eff} \) and voltage gain \( M_g \) are different for each VIRT operating mode. In addition, one needs to ensure the primary-side ZVS and voltage gain requirements in all operating modes are met in order to design high performance DC-DC VIRT system. Details on designing a LLC resonant tank with the VIRT are covered later in Chapter 3.3. The chosen LLC design parameters and list of components for this prototype are shown in Table 2.2.

![VIRT structure with \( N_p = 12 \)](image)

Figure 2-5: The electrical model of the stacked half-bridge interfaced with VIRT [2].

### 2.3.1 Stacked Half-bridge Inverter

A stacked half-bridge structure uses two different modes to compress the input voltage range, through use of the Variable-Frequency Multiplier ("VFX") technique by yielding an ac square waveform at the inverter output with an amplitude that is half (Mode 1) or quarter (Mode 2, "VFX") of the input voltage \( V_{IN} \) in the low-line (120 - 190 V) or high-line (190 - 380 V) range, respectively, as shown in Fig. 2-6 and Fig. 2-7 [10]. Due to this input voltage compression, for a range of \( V_n \) of 120 - 380 V, the peak voltage range of the square waveform that a LLC resonant tank has to handle is only 47.5 - 95 V. Furthermore, a stacked half-bridge inverter structure makes it easier to achieve the primary side zero voltage switching (ZVS). Disregarding energy conversion effects of larger capacitances such as \( C_r \) and \( C_{in} \), it aligns the device capacitors \( C_{ds} \) of two switches in series, effectively halving the capacitive energy associated with
Table 2.2: List of main components and LLC resonant tank design [2]

<table>
<thead>
<tr>
<th>Inverter</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>GS66504B (650 V / 15 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Signal isolators</td>
<td>SI8610</td>
</tr>
<tr>
<td>Isolated power</td>
<td>ADUM5010</td>
</tr>
<tr>
<td>Balancer diodes</td>
<td>MMBD3004BRM</td>
</tr>
<tr>
<td>Balancer capacitors</td>
<td>10 uF (1812) / 450 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIRT Rectifier</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>EPC2023 (30 V / 60 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Blocking capacitors</td>
<td>22 uF (0805) / 16 V</td>
</tr>
<tr>
<td>Decoupling capacitors</td>
<td>10 uF (0508) / 16 V per half-bridge</td>
</tr>
<tr>
<td>Output capacitors</td>
<td>22 uF (1210) / 16 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LLC Resonant Tank</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Frequency</td>
<td>1.2 MHz</td>
</tr>
<tr>
<td>Operating frequency range</td>
<td>470 - 910 kHz</td>
</tr>
<tr>
<td>Number of primary turns (Np)</td>
<td>12</td>
</tr>
<tr>
<td>Magnetizing Inductance</td>
<td>38 µH</td>
</tr>
<tr>
<td>Resonant capacitor (split)</td>
<td>2 x 3.47 nF in series</td>
</tr>
<tr>
<td>Resonant inductors (split)</td>
<td>2 x 1.79 uH in series; ea. RM5I / 3F36, 3 turns 46 AWG / 180 Litz wire</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIRT Transformer</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>EQ20 + PLT/3F36, 0.006” gap on all legs</td>
</tr>
<tr>
<td>Primary windings</td>
<td>Six turns on Layer 3 and 4 connected in series, 0.019” trace width, 0.008” trace-to-trace spacing</td>
</tr>
<tr>
<td>Secondary windings</td>
<td>Two sets of half turns (one set each on layers 1 and 2) connected in parallel</td>
</tr>
<tr>
<td>PCB</td>
<td>2 oz, 4 layers, 0.063”, FR4, 0.025” separation between layers 2 and 3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Control</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller</td>
<td>TI TMS320F28379D</td>
</tr>
</tbody>
</table>
the device capacitors compared to a conventional half-bridge structure with the same input voltage $V_{IN}$. More details on achieving the primary side ZVS are covered later in Chapter 3.3. Finally, a balancing circuitry which consists of an array of diodes and capacitors is implemented to ensure input capacitors hold half the DC input voltage.

![Diagram of stacked half-bridge structure](image)

Figure 2-6: Operations of the stacked half-bridge structure. Note that each $C_{in}$ holds $\frac{1}{2}V_{IN}$.

![Waveforms of stacked half-bridge structure](image)

Figure 2-7: Operations of the stacked half-bridge structure in waveforms.

### 2.3.2 VIRT Transformer Design and Layout

Planar magnetics have gained increasing popularity owing to miniaturization and ease of fabrication [11], [12]. In order to properly exploit the benefits of the VIRT structure and demonstrate its great promise for miniaturization and loss reduction, a planar transformer where both primary and secondary windings consist of PCB traces has been implemented. Transformer parameters such as a core shape, the number of
primary-side turns \( (N_p) \), and the number of PCB layers for each winding need to be carefully chosen to ensure high performance operations of VIRT.

The number of the primary-side turns with the single secondary-side turn for a wide operating condition can be computed in Equation (2.1).

\[
N_p = M_{g,\text{mean}} \frac{k_{\text{inv}} V_{\text{in,mean}}}{V_{\text{out,mean}}} \approx 12.58, \tag{2.1}
\]

where \( M_{g,\text{mean}} \), the mean gain of the LLC resonant tank, is 1.38 (\( M_{g,\text{max}} = 2.53 \) and \( M_{g,\text{min}} = 0.76 \)), \( k_{\text{inv}} \), the voltage gain of the stacked half-bridge inverter stage, is \( \frac{1}{2} \), \( V_{\text{in,mean}} = 155 \text{ V} \) (\( V_{\text{in,max}} = 190 \text{ V} \) and \( V_{\text{in,min}} = 120 \text{ V} \)), and finally \( V_{\text{out,mean}} = 8.5 \text{ V} \) (\( V_{\text{out,max}} = 12 \text{ V} \) and \( V_{\text{out,min}} = 5 \text{ V} \)). In order to make the planar transformer simple and symmetric, an even number 12 has been chosen as the number of the primary-side turns \( N_p \). Note that in FB/FB mode the VIRT transformer effectively achieved 12 : 0.5 turns ratio whereas a conventional transformer achieves same step-down ratio with 24 turns on the primary-side winding.

In order to quantitatively analyze the improved performance of the VIRT transformer, it is worthwhile to compare \( R_{ac} \) of the VIRT transformer to that of a conventional transformer in both interleaved and non-interleaved windings. Since the
secondary-side voltages applied on the transformer ports are the same for the VIRT transformer and conventional transformer with a full-bridge rectifier, the core losses of the both cases are expected to be the same. Therefore, it is the copper loss that makes a difference in terms of transformer performance. M2Spice, a software tool designed to accurately capture skin and proximity effects in multi-layer planar magnetics, is used to generate the circuit netlist for each transformer configuration and compute $R_{\text{ac}}$ [13]. Shown in Fig. 2-8 are $R_{\text{ac}}$ of the chosen layer configurations over frequency. Note that all primary-side layers are connected in series and all secondary-side layers are connected in parallel. As expected, the VIRT transformer shows improved performance in both non-interleaved and interleaved cases. For the prototype, Configuration 3, where the planar transformer is built in a non-interleaved fashion with two layers of the primary-side in series comprising the total of 12 turns and another two layers of the secondary-side in parallel comprising a single physical turn, has been chosen due to its performance and cost-effectiveness. An interleaved design such as Configuration 4 would require buried VIAs and substantially increase the cost and complexity of building the PCB with such configuration. In addition, large inner-layer cores need to be used to meet the voltage insulation requirement between the primary and secondary windings (2.5 kV in this application [1]) and increase the volume of a PCB.

It is important to minimize the current excursions around the core in order to minimize a copper loss contributed by the extended current path and ensure the optimal operation of VIRT. To this end, a layout of the VIRT transformer and rectifiers needs to be carefully designed while minimizing ac current path as much as possible. Shown in Fig. 2-9 and Fig. 2-10 are the proposed layout of the VIRT rectifier and "bad" layout example for comparison. Note that only top side half-bridge cells along with the VIRT transformer are shown for the sake of simplicity. Nonetheless, the example current paths shown in the figure cover all possible current paths for different VIRT modes. Note that all switches are placed on the same side of the board since they would have placed substantially far from the transformer due to the voltage insulation requirement if placed on the other side of the board where the primary-side
Figure 2-9: The proposed layout for an optimized current path showing all possible current paths for VIRT modes.

winding layers are. Finally, blocking capacitors are placed partially inside the core in order to further reduce the current excursion. As Fig. 2-9 and Fig. 2-10 show, the placement of decoupling capacitors and bus voltage connections (i.e. $V_{out}$ and $GND$) can make a huge difference in terms of the length of a current excursion. Table 2.3 approximately quantifies current paths for both cases using the number of resistance squares normalized by the estimated trace width, proving the proposed layout offers more optimal current paths.

2.4 Experimental Results

In order to experimentally verify the electrical model of VIRT derived in Section 2.2 designed with an LLC resonant tank and stacked half-bridge inverter, the prototype
has been built as shown in Fig. 2-11 with the main components listed in Table 2.2.

Full schematics, a bill of material and pcb layout files are presented in Appendix B.1.

As shown in Fig. 2-12, the voltage gain curves versus operating frequency from the experiments are compared to the ones from the circuit simulation and fundamental harmonic approximation (FHA) analysis. The experimental gain curves show a good
Figure 2-11: Experimental prototype with close-ups of the VIRT layout [3]. The simplified schematic is shown in Fig. 2-5, and the main components are indicated in Table 2.2. Full schematics, bill of materials and layout files are presented in Appendix B.1.

resemblance to the ones from the simulation and FHA analysis. MATLAB script for making the gain curves may be found in Appendix A. Toward higher operating frequencies, the matching becomes more accurate as expected since the FHA analysis can better model the LLC gain characteristic in the vicinity of the resonant frequency, 1.2 MHz in this case, which proves validity of the derived electrical model of VIRT and the LLC resonant tank design.

Shown in Fig. 2-13 are the waveforms demonstrating the symmetric operation of the VIRT. Note that $V_{A1}$ and $V_{B1}$ are the voltages across the low-side switches of A1 and B1, respectively, as labeled in Fig. 2-5. These two waveforms collected at $V_{in} = 120$ V, $V_{out} = 9$ V, $P_{out} = 36$ W, and $f_{sw} = 558.5$ kHz show excellent symmetry, which suggests two rectifiers placed on each side of the VIRT transformer see the same secondary-side induced current as depicted in Fig. 2-2. Note that oscillations in the rectifier waveforms are associated with the device capacitors charging and discharging when the secondary-side switches are not conducting and the power transfer from the primary-side is effectively ceased during the LLC operation below the resonance. In addition to the well-matching voltage gain curves shown in Fig. 2-12, the
Figure 2-12: Voltage gain curves versus operating frequency for each inverter mode [3].

great symmetry shown by these two rectifier waveforms further validates the derived electrical model of the VIRT.

Shown in Fig. 2-14 is the efficiency of the prototype converter versus input voltage at full load. Note that FB/FB mode is used for 5 V output, HB/HB mode for 9 V, and
Figure 2-13: Voltage waveforms validating expected symmetric operation of the A1 and B1 rectifiers: HB/HB mode, $V_{in} = 120$ V, $V_{out} = 9$ V, $P_{out} = 36$ W, $f_{sw} = 558.5$ kHz [3].

Figure 2-14: Power stage efficiency at full load [3].

Finally HB/0 mode for 12 V. Two different modes of the stacked half-bridge inverter are used; Inverter Mode 1 effectively halves the input voltage $V_{IN}$ ranging from 120 - 190 V and Inverter Mode 2 effectively quarters the input voltage $V_{IN}$ ranging from
190 - 380 V. The efficiency ranges from 94.4 - 95.7 % in Inverter Mode 1 and 93.4 - 95.2 % in Inverter Mode 2, which shows a great potential of the VIRT structure for wide input and output range applications, especially when combined with techniques such as variable-frequency multiplication (VFX).

Note that the efficiency for each output shows an increasing trend as the input voltage increases. This is because with the fixed voltage gains from the stacked half-bridge inverter and VIRT rectifier for a certain mode of VIRT operation, a higher input voltage for the fixed output voltage and power results in a higher operation frequency in order to meet the required voltage gain through the LLC resonant tank. As the operation frequency increases toward and beyond the resonant frequency, the circulating current through the LLC resonant tank becomes smaller. This results in the improved performance due to the reduced conduction losses of the inverter and rectifier switches as well as reduced copper loss of the transformer given that the primary-side ZVS is achieved over the entire operating frequency. Finally, the reduced efficiency in Inverter Mode 2 compared to Inverter Mode 1 can be attributed to the additional loss from the inverter mode shift since it has been experimentally verified that 380 V Mode 2 generates the identical square waveform $V_{inv}$ exciting the LLC resonant tank as 190 V Mode 1 does [2]. Despite the ZVS operation of the primary-side inverter, the fact that each device capacitor in Inverter Mode 2 sees twice the voltage for the same square waveform $V_{inv}$ compared to Inverter Mode 1 causes an additional parasitic loss in practice.
Chapter 3

Design Analysis: VIRT with Bypass Switch

3.1 Motivation

The proposed Variable-Inverter-Rectifier-Transformer (VIRT) structure in Chapter 2 has shown high performance across wide operating conditions ($V_{in} = 120 - 380$ V DC, $V_{out} = 5 - 12$ V DC, and $P_{out} = 25 - 36$ W) owing to its effective fractional and reconfigurable turns ratio. This allows a designer to further optimize the overall transformer loss and meet the widely varying operating conditions with a compact, efficient converter design. However, the proposed structure has shown a reduced performance in HB/0 mode which generates an upper-end of the output voltage and power ranges (12 V and 36 W in the proposed design from Chapter 2) due to the poor utilization of the effective core area.

In this chapter, we introduced an improved rectifier topology that utilizes a “bypass switch”. This rectifier topology enables much better utilization of the core area and improves the VIRT performance associated with an asymmetric mode such as HB/0 mode. This technique is especially valuable since HB/0 mode is utilized for a high output voltage and power operation which is often the bottleneck for an acceptable temperature raise of the converter. Furthermore, we introduce a hybrid construction of the VIRT transformer in which the primary-side winding is built...
with litz wire and the fractional-turn secondary is constructed with printed windings in a PCB. This structure is implemented to improve the copper loss of the VIRT transformer and benefits from the high window utilization of the primary, the use of the printed circuit board for galvanic isolation, and the controlled geometry and low interconnect loss of the fractional-turn secondary winding. Finally, this chapter introduces a systematic design and analysis method for a DC-DC VIRT system implemented with a bypass switch rectifier and a hybrid transformer.

3.2 Principle of Operation

Shown in Fig. 3-1a is the proposed VIRT structure with a bypass switch implemented with an EQ type core. Fig. 3-2 shows electrical models of the proposed structure for operation with the bypass switch open and closed. Details on deriving the VIRT electrical model are covered in Chapter 2.2. A primary winding around the center post of the core (not shown) generates flux though the center post. The two full-bridge rectifiers named A and B, respectively, are distributed around the magnetic core and connected through two secondary half-turns around the center post. Rectifier A consists of two half-bridge cells labelled A1 and A2, and Rectifier B, cells B1 and B2. Finally, each cell is connected to the output bus terminals, $V_{OUT}$ and GND through power and ground planes that are routed outside the magnetic core [2].

Each rectifier can be operated as a full-bridge (FB), half-bridge (HB), or “zero” mode. When a rectifier is operated in FB mode, both half-bridge cells (e.g. A1 and A2) are active, switching as a full-bridge. In HB mode, only one half-bridge cell is active while the other cell is shorted to ground. In zero mode, both cells are shorted to ground (or to the output bus), effectively creating an ac short-circuit path for the induced current around the associated outer core leg; this has the effect of rejecting ac flux through that core leg.

In a USB-PD application where the output voltage may be regulated to any of 5 V, 9 V, 15 V, or 20 V, one can select among the various VIRT modes in Fig. 3-1b - 3-1f to support the different output voltages. A summary of all VIRT modes
including the bypass modes is shown in Table 3.1. Note, for example, that the HB/0 and HB/bypass modes offer four times larger voltage gain than the FB/FB mode. Thus, it is sensible to utilize HB/0 or HB/bypass to achieve the 20 V operating point,
and FB/FB to achieve the 5 V point.

Table 3.1: Summary of VIRT operations. Detailed derivations for FB/FB, HB/HB, and HB/O modes are covered in [2]. Note that "net" magnetizing inductance is calculated assuming an identical gap on all three core legs. A design with a gap only in the center post would have different values for magnetizing inductances.

<table>
<thead>
<tr>
<th>VIRT mode</th>
<th>Description</th>
<th>Effective Turns Ratio</th>
<th>Mode Type</th>
<th>&quot;Net&quot; Magnetizing Inductance*</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB/FB (Fig. 3-1b)</td>
<td>All switches active</td>
<td>Np : 1/2</td>
<td>Symmetric</td>
<td>$L_M = \frac{N_p^2}{2R_{cc}}$</td>
</tr>
<tr>
<td>HB/HB (Fig. 3-1d)</td>
<td>A2, B2 active A1, B1 short to GND</td>
<td>Np : 1</td>
<td>Symmetric</td>
<td>$L_M$</td>
</tr>
<tr>
<td>FB/byp (Fig. 3-1c)</td>
<td>A1, B2 active Bypass switch on</td>
<td>Np : 1</td>
<td>Bypass</td>
<td>$L_M$</td>
</tr>
<tr>
<td>HB/O (Fig. 3-1f)</td>
<td>B2 active A1, A2, B1 short to GND</td>
<td>Np : 2</td>
<td>Asymmetric</td>
<td>$\frac{2}{3}L_M$</td>
</tr>
<tr>
<td>HB/byp (Fig. 3-1e)</td>
<td>B2 active, A1 short to GND Bypass switch on</td>
<td>Np : 2</td>
<td>Bypass</td>
<td>$L_M$</td>
</tr>
</tbody>
</table>

* "Net" magnetizing inductance means $L_A + L_B$ in Fig. 3-2a and is derived through modeling magnetic circuit as shown in Fig. 3-3.

While both HB/O and HB/bypass modes offer the same effective transformer turns ratio (i.e. same voltage gain), HB/bypass mode can achieve lower losses for the same conversion requirement. In HB/O mode an ac short is effectively created around one leg of the core, ideally rejecting the ac flux though that section of the core as illustrated in Fig. 3-3a. This causes the flux through the center post to be routed through only one of the outer core legs as shown in Fig. 3-3c, increasing the peak flux density through that leg and increasing core loss [2]. The proposed VIRT structure with the bypass switch in Fig. 3-1a eliminates this issue, enabling the same gain characteristic to be achieved while maintaining full utilization of the core material.
Figure 3-3: Magnetic circuit derivation of the VIRT model. Solid lines correspond to real components of currents, while dotted components correspond to virtual components of currents invoked for modeling purpose [2].

Note that S\textsubscript{BYP} carries bidirectional current and blocks bidirectional voltage and can be implemented by two "back-to-back" MOSFETs. The "bypass" modes enabled by this switch redirect the current path such that it bypasses the entire rectifier structure on one side of the VIRT and configures the un-bypassed rectifier as a FB or HB as shown in Fig. 3-1c and 3-1e, respectively. HB/bypass mode in Fig. 3-1e utilizes the entire effective core area of the transformer as opposed to HB/0 mode by allowing the flux generated by the primary side current to be routed through both legs of the core as shown in Fig. 3-3e, which in turn avoids unequal flux densities in the outer core legs and hence reduces core loss. Therefore, the bypass switch provides a means to achieve improved system efficiency in the higher output voltage regime while adding little complexity to the system.
3.3 Experimental Design

![Stacked half-bridge inverter](image)

**Figure 3-4:** Schematics of the DC-DC VIRT system with the bypass switch.

In order to verify the benefits of the bypass modes, a VIRT system with bypass switch has been designed and built with a LLC resonant tank and stacked half-bridge inverter as shown in Fig. 3-4; complete schematics, bill of materials, and pcb layout files may be found in Appendix B.2. The input voltage is defined by two ranges: 120 - 170 V\(_{dc}\) and 310 - 380 V\(_{dc}\). These correspond to the peak of ac line for low-line (85 - 120 V\(_{ac}\)) operation and high-line (220 - 268 V\(_{ac}\)) operation, respectively. A stacked half-bridge structure uses two different modes to compress the input voltage range by halving (Mode 1) or quartering (Mode 2, “VFX”) \(V_{IN}\) in the low-voltage range or high-voltage range, respectively [10]. The VIRT and LLC work interactively to regulate the output voltage, \(V_{OUT}\), to 5 V (25 W rating), 9 V (36 W rating), 15 V (45 W rating), and 20 V (50 W rating), respectively. These specifications correspond to those for a USB-PD charger [6]. Due to these wide input and output voltage ranges regulated at different maximum power levels, an LLC stage interfaced with the VIRT
needs special design considerations to meet voltage gains and ensure primary-side ZVS across all modes of operation.

3.3.1 VIRT Rectifier with Bypass Switch

As illustrated in Section 3.2, two synchronous full-bridge rectifiers are implemented along with the bi-directional bypass switch. The bypass modes enabled by this switch redirect the current path such that it bypasses the entire rectifier structure on one side of the VIRT and configures the un-bypassed rectifier as a full-bridge or half-bridge. The re-configurable voltage gain from the LLC rectifier input to the dc output voltage achieved by the VIRT rectifier puts a lower stress on the LLC resonant tank. This results in an efficient LLC performance due to the compressed output voltage range that needs to be regulated by the LLC converter.

The DC-DC VIRT system shown in Fig. 3-4 is designed to regulate the output voltage in ranges between 5 - 20 V. Since HB/bypass mode offers four times larger voltage gain than FB/FB mode and twice larger voltage gain than FB/bypass mode, it makes sense to utilize HB/bypass mode to achieve 15 V and 20 V, FB/bypass mode to achieve 9 V, and finally FB/FB mode to achieve 5 V. Therefore, the output voltage range the LLC converter must regulate to is reduced from 5 - 20 V to 3.75 - 5 V owing to the output voltage compression capability of the VIRT rectifier with bypass switch.

3.3.2 LLC Resonant Tank Design

In order to design a LLC resonant tank in the proposed DC-DC VIRT system, additional voltage gains from the stacked half-bridge inverter and VIRT rectifier need to be taken into account. The voltage gain of the DC-DC VIRT system can be expressed as shown in Equation (3.1).

\[
\frac{V_{out}}{V_{in}} = M_{g, LLC} M_{inv} \frac{k}{n},
\]

(3.1)
Table 3.2: Minimum and maximum LLC voltage gains ($M_{g, LLC}$), effective load resistances ($R_{eff}$), and quality factors ($Q_e$) for all operation modes of the VIRT with the bypass switch

<table>
<thead>
<tr>
<th>Mode</th>
<th>FB/FB</th>
<th>FB/bypass</th>
<th>HB/bypass I</th>
<th>HB/bypass II</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{load}$ (Ω)</td>
<td>1</td>
<td>2.25</td>
<td>5</td>
<td>8</td>
</tr>
<tr>
<td>$V_{OUT}$ (V)</td>
<td>5</td>
<td>9</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>$P_{OUT}$ (W)</td>
<td>25</td>
<td>36</td>
<td>45</td>
<td>50</td>
</tr>
<tr>
<td>Minimum $M_{g, LLC}$ (V/V)</td>
<td>1.26</td>
<td>1.14</td>
<td>0.95</td>
<td>1.26</td>
</tr>
<tr>
<td>Maximum $M_{g, LLC}$ (V/V)</td>
<td>2.00</td>
<td>1.80</td>
<td>1.50</td>
<td>2.00</td>
</tr>
<tr>
<td>$R_{eff}$ (Ω)</td>
<td>467</td>
<td>263</td>
<td>146</td>
<td>233</td>
</tr>
<tr>
<td>$Q_e$</td>
<td>0.10</td>
<td>0.17</td>
<td>0.31</td>
<td>0.19</td>
</tr>
</tbody>
</table>

Table 3.3: LLC resonant tank design

<table>
<thead>
<tr>
<th>Resonant Frequency ($f_{res}$) MHz</th>
<th>f_max range (kHz) FHA analysis</th>
<th>Number of primary-side turns ($N_p$)</th>
<th>Magnetizing Inductance $L_m$ (μH)</th>
<th>Resonant Inductance $L_{res}$ (μH)</th>
<th>Resonant Capacitance $C_{res}$ (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.15</td>
<td>680 - 1300</td>
<td>12</td>
<td>20.2</td>
<td>5.50</td>
<td>3.47</td>
</tr>
</tbody>
</table>

where $M_{g, LLC}$ is the voltage gain of the LLC resonant tank, $M_{inv}$ is the voltage gain of the stacked half-bridge inverter, $n$ is the physical turns ratio of the transformer, and $k$ is the voltage gain of VIRT rectifier stage, respectively.

$M_{inv}$ is $\frac{1}{2}$ in VFX Mode 1 and $\frac{1}{4}$ in VFX Mode 2 [10]. Note that Mode 1 is utilized for the low-range $V_{IN}$ associated with U.S. and Japan ac voltages (120 - 170 V) and Mode 2 for the high-range $V_{IN}$ (310 - 380 V) associated with European ac voltages. $n$, the physical turns ratio of the transformer, is chosen to be 12 following the guideline introduced in Section 2.3.2. Finally, $k$ is $\frac{1}{2}$ for FB/FB mode, 1 for FB/bypass mode, and 2 for HB/bypass mode.

Shown in Table 3.2 are minimum and maximum LLC voltage gains ($M_{g, LLC}$), effective load resistances ($R_{eff}$), and quality factors ($Q_e$) for all the operation modes of the VIRT with the bypass switch. $R_{eff}$ can be calculated as

$$R_{eff} = \frac{8}{\pi^2} \left(\frac{n}{k}\right)^2 R_{load},$$

(3.2)

where $k$, the voltage gain of the VIRT rectifier, is $\frac{1}{2}$ for FB/FB mode, 1 for FB/bypass mode, and 2 for HB/bypass mode (See [14] for derivation of this ac-recitifier equivalent
resistance formulation). Finally, a quality factor \( Q_e \) is [14]

\[
Q_e = \frac{\sqrt{L_r/C_r}}{R_{\text{load}}},
\]

(3.3)

Note that the range of \( M_{g,\text{LLC}} \) is from 0.95 to 2 across all the operation modes owing to the input and output voltage compression from the stacked half-bridge inverter and VIRT rectifier, respectively. This results in a max-to-min gain ratio \( \frac{M_{g,\text{LLC,\max}}}{M_{g,\text{LLC,\min}}} = 2.11 \). If one instead were to use a conventional LLC converter with a half-bridge inverter and single full-bridge rectifier, the max-to-min gain ratio \( \frac{M_{g,\text{LLC,\max}}}{M_{g,\text{LLC,\min}}} \) would have been 12.7, placing an unacceptable stress on the LLC resonant tank to reach all operating points. This reduced range of the LLC voltage gain ensures efficient performance of the LLC converter.

Based on the design guidelines available in [14], the LLC resonant tank design parameters have been set as shown in Table 3.3. Note that these design values have been further tuned in order to ensure a zero-volt-switching (ZVS) on the primary-side inverter. Shown in Fig. 3-5 are the voltage gain and ZVS curves for FB/FB mode \((V_{\text{out}} = 5 \text{ V and } P_{\text{out}} = 25 \text{ W})\) and HB/bypass mode \((V_{\text{out}} = 15 \text{ V and } P_{\text{out}} = 45 \text{ W})\); MATLAB script for generating these curves is provided in Appendix A. The curves for the other modes are also included in Appendix A. In each plot, \( V_{\text{out}} \) vs \( f_{\text{sw}} \) for each \( V_{\text{in}} \) from a low-range voltage \((120 - 170 \text{ V})\) and high-range voltage \((310 - 380 \text{ V})\) is plotted along with a desired output voltage since \( V_{\text{out}} = V_{\text{in}}M_{g,\text{LLC}}(f_{\text{sw}}, Q_e, L_n)M_{\text{inv}}\), where \( L_n = \frac{L_m}{L_r} \). Note that a fundamental harmonic approximation (FHA) for the square waveform onto the LLC resonant tank has been made. Nonetheless, these voltage gain curves show reasonable accuracy for operations in the vicinity of the resonant frequency \( f_{\text{res}} \).

In order to ensure ZVS on the primary-side inverter in a LLC converter, one needs to ensure that the input impedance \( Z_{\text{in}} \) looking into the resonant tank is inductive such that the resonant current \( I_{\text{res}} \) lags behind the applied voltage \( V_{\text{INV}} \) in this case [14].

\[
Z_{\text{in}} = |Z_{\text{in}}|e^{j\phi},
\]

(3.4)
(a) Voltage gain and ZVS curves for FB/FB mode ($V_{out} = 5$ V and $P_{out} = 25$ W).

(b) Voltage gain and ZVS curves for HB/bypass mode ($V_{out} = 15$ V and $P_{out} = 45$ W).

Figure 3-5: Voltage gain and ZVS curves generated through MATLAB.
where $-\pi/2 \leq \Phi_z \leq \pi/2$ and $Z_{in}$ is inductive for $\Phi_z > 0$, capacitive for $\Phi_z < 0$, and resistive for $\Phi_z = 0$. Note that $\Phi_z$ is a function of the switching frequency $f_{sw}$. In Fig. 3-5, ZVS I curve serves as a border between the capacitive and inductive regions such that the region above the ZVS I curve is the inductive region of $Z_{in}$ and the region below it is the capacitive region. Finally, for operation above the series resonance point it is guaranteed that $Z_{in}$ is always inductive. As shown in Fig. 3-5, the DC-DC VIRT system is designed to operate in an inductive region for any output voltage it regulates to.

Figure 3-6: Schematics of the DC-DC VIRT system.

Figure 3-7: Operations of the stacked half-bridge structure. Note that each $C_{in}$ holds $\frac{1}{2}V_{in}$. 

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In addition to making sure $Z_{in}$ is always in an inductive region for ZVS, one needs to ensure there is a sufficient inductive energy associated with the current through the magnetizing inductance $I_m$ during the deadtime such that in Inverter mode 1, it can charge up the $C_{ds}$ of $S_1$ and $S_4$ and discharge the $C_{ds}$ of $S_2$ and $S_3$ before the body diode conduction of $S_2$ and $S_3$. In Inverter Mode 2, $I_m$ needs to charge up the $C_{ds}$ of $S_1$ and discharge the $C_{ds}$ of $S_2$ before the body diode conduction of $S_2$ in one cycle. In the other cycle of Inverter Mode 2, $I_m$ needs to charge up the $C_{ds}$ of $S_4$ and discharge the $C_{ds}$ of $S_3$ before the body diode conduction of $S_3$. The schematic of the DC-DC VIRT system and operation of the stacked half-bridge structure are shown again in Fig. 3-6 and Fig. 3-7, respectively, for convenience. Therefore, Equation (3.5) must be met in order to achieve ZVS on the primary-side inverter.

$$\frac{1}{2}(L_m + L_r)I_{m,\text{peak}}^2 \geq \frac{1}{2} n_{\text{cap}} C_{eq}(k_{inv} V_{in})^2,$$

where $I_{m,\text{peak}} = \frac{2n V_{out}}{k \pi^2 f_{sw} L_m}$ (FHA), $C_{eq} = C_{ds} + C_{par}$, $n_{\text{cap}} = 4$ for Inverter mode 1 and 2 for Inverter mode 2 and $k_{inv} = \frac{1}{2}$. In order to plot a ZVS II boundary as shown in Fig. 3-5 Equation (3.5) can be further transformed as follow;

$$V_{out} \geq \sqrt{\frac{n_{\text{cap}} C_{eq}(k_{inv} V_{in})^2 k \pi^2 f_{sw} L_m}{2n}}$$

where $k$ is the gain of the VIRT rectifier defined in Equation (3.1). This ZVS II boundary, which is based on the energy requirement for sufficient charge and discharge, sets the minimum output voltage the DC-DC VIRT system can achieve at certain switching frequency $f_{sw}$ with the given LLC parameters in order to achieve ZVS on the primary-side inverter. Note that this energy requirement is met in all VIRT operations of the proposed design as shown in Fig. 3-5.

Note that both $C_r$ and $C_{in}$ can be ignored in an energy conversion analysis since they are much larger than the device capacitances $C_{ds}$. $C_{eq}$ includes parasitic capacitances $C_{par}$ in addition to $C_{ds}$. $n_{\text{cap}}$ is 4 for Inverter mode 1 and 2 for Inverter mode 2 due to the fact that 2 device capacitors are charged up and 2 other device
capacitors are discharged in one cycle of Inverter mode 1 whereas only one device capacitor is charged and one other capacitor is discharged in one cycle of Inverter mode 2 as illustrated in Fig. 3-7. Therefore, for the same square waveform $V_{INV}$ onto the LLC resonant tank, a capacitive energy in Inverter mode 2 is twice larger than that in Inverter mode 1 due to the square dependence of the capacitive energy on the input voltage $V_{in}$ which in this case is twice larger in Inverter mode 2 than in Inverter mode 1 for the same $V_{INV}$. This capacitive energy difference between Inverter mode 1 and mode 2 is reflected in Fig. 3-5 as the Inverter mode 2 imposes a more strict minimum $V_{out}$ set by ZVS II curves than Inverter mode 1 does, despite the relatively similar resulting $V_{INV}$.

Finally, $k_{inv}$ is $\frac{1}{2}$ for both mode 1 and 2 of the inverter due to half the input voltage across each device capacitor $C_{ds}$ that needs to be charged and discharged in one cycle for the both modes of operation. Despite twice the number of device capacitors in the stacked half-bridge structure compared to the number of device capacitors in a conventional half-bridge structure, the stacked half-bridge structure has half the capacitive energy due to the square dependence of the capacitive energy on the voltage across each device capacitor. In other words, each device capacitor in the stacked half-bridge structure sees half the input voltage whereas it sees the full input voltage in a conventional half-bridge structure. In addition to the input voltage compression capability, this reduced capacitive energy of the stacked half-bridge structure satisfies the ZVS condition with a less circulating current $I_m$ compared to a conventional half-bridge structure, which results in reduced conduction losses of the switches on both primary and secondary sides and copper loss of the transformer.

### 3.4 Hybrid VIRT Transformer

Planar transformers, in which the windings are formed as part of the printed circuit board (PCB), are often desirable for low-output-voltage systems for a variety of reasons. This includes the fact that planar construction helps minimize additional interconnect losses in the high-current secondary, promotes reduced height, and en-
ables sophisticated winding patterns among other benefits [13], [12] and has a great potential for promoting miniaturization. Planar construction is particularly advantageous for the VIRT technique, since the secondary can be printed in the circuit board and directly connected locally to the distributed rectifiers. However, implementation of transformers with large turns ratios becomes challenging, especially if planar construction is desired. A planar transformer has its windings routed on a printed circuit board (PCB) and geometries of these winding traces are subject to the PCB fabrication requirements such as a trace width and trace-to-trace spacing as well as current and voltage requirements. These manufacturing constraints could potentially increase the copper loss for a transformer that has a large turns ratio or simply render the implementation of such a transformer unfeasible. Thus, for high step-down designs it would be valuable to explore alternative transformer constructions that give the benefit of planar secondaries (especially in the VIRT configuration) but do not suffer the spacing and voltage constraints on the high-voltage primary.

To this end, this thesis explores the design of a “hybrid” transformer built as a hybrid construction where the primary side winding is built with litz wire and the fractional-turn secondary is constructed in a planar fashion with printed windings. This approach can both address copper packing/utilization issues on the primary side and directly provide high-voltage insulation between primary and secondary windings without requiring large printed-circuit-board core spacings, if a triple-insulted litz wire is used. In an application which requires a high step-down ratio, the VIRT structure enables an effective fractional turns ratio (e.g. 12:0.5) which significantly reduces the number of turns on the primary side for the equivalent effective conversion ratio. A hybrid construction of the transformer provides a means to further reduce this copper loss by replacing PCB primary winding traces whose width and thickness are strictly subject to the PCB fabrication requirements with litz wire, achieving a higher window fill factor and enabling mitigation of skin and proximity effects through careful selection of the litz wire design. In addition, triple-insulted litz wire can be used to directly meet the voltage insulation requirement of the transformer, about 2.5 kV [1], which is in a fully planar transformer must be met by having a large isolation barrier.
between the primary and secondary windings, which increases space and circuit board cost if interleaving of the transformer is desired. Therefore, the hybrid transformer structure with litz wire has a great potential for reducing a copper loss and achieving further miniaturization.

### 3.4.1 Litz Wire Selection

A software tool called LitzOpt, which allows an user to choose an optimal litz wire design and optimize copper loss in transformers with multiple windings for any arbitrary current waveforms [4], has been used to determine the number of strands and diameter of each strand for the given geometry and number of primary-side turns. Fig. 3-8 shows the user-interface page of LitzOpt, where an user can enter core geometry information such as an available window area and gap length and type. Furthermore, it allows an user to input a current waveform through each winding, the number of each
winding, and winding cross section data to perform a comprehensive analysis on the winding loss based on one-dimensional or two-dimensional field calculation depending on an user’s choice [4]. The input data is based on the LLC design interfaced with VIRT with the bypass switch introduced in Chapter 3.3.2. Note that a back-to-back EE shape (EQ20 core) has been used to minimize inter-winding capacitance and gap fringing effects by exploiting the large available window area and placing windings sufficiently away from the gap and each other. Table 3.4 shows the reference VIRT design for selecting an optimal litz wire design. Note that two different currents obtained through a circuit simulation at two different extreme conditions have been used for this analysis. One is the largest current value across all VIRT modes, 1.303 A\text{rms}, which happens at \(V_{in} = 120 \text{ V}, \ V_{out} = 20 \text{ V} \) and \(P_{out} = 50 \text{ W} \) in HB/bypass mode. The other is the current at the highest \(f_{sw}\), 0.769 A, which happens at \(V_{in} = 380 \text{ V}, \ V_{out} = 15 \text{ V}, \) and \(P_{out} = 45 \text{ W} \) in HB/bypass mode.

Shown in Table 3.5 and 3.6 are the buildable design tables generated through LitzOpt in the worst current case (\(I_{winding} = 1.303 \ A_{rms} \) at \(f_{sw} = 713 \text{ kHz}\)) and worst frequency case (\(I_{winding} = 0.768 \ A_{rms} \) at \(f_{sw} = 1.3 \text{ MHz}\)), respectively. In each table, design alternatives ranging from high-cost, low-loss designs to low-cost, high-loss designs are listed in the order of increasing winding loss. \(R_{dc}\) for each design has been calculated using winding loss and current. Design number d11 in each table corresponds to the most loss-optimized design. Design d11 in Table 3.5 is added to Table 3.6 as a reference design ref2, and d11 in Table 3.6 is added to Table 3.5 as ref2 in order to analyze performance of the most optimized litz design in one extreme case (e.g. worst frequency case) put into the other extreme case (e.g. worst current case) and decide most suitable litz wire design overall. Finally, design ref1 in each table, 48 AWG and 180 strands corresponds to an intermediate design between d11 and ref2.
Table 3.5: Buildable design table generated through LitzOpt in the worst current case ($I_{winding} = 1.303$ $A_{rms}$ at $f_{sw} = 713$ kHz)

<table>
<thead>
<tr>
<th>Design Number</th>
<th>Gauge (AWG)</th>
<th>Relative Cost</th>
<th>Loss (W)</th>
<th>Number of Strands</th>
<th>$R_{ac}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>d1</td>
<td>28</td>
<td>0.275</td>
<td>1.961</td>
<td>1</td>
<td>1.155</td>
</tr>
<tr>
<td>d2</td>
<td>30</td>
<td>0.175</td>
<td>0.993</td>
<td>1</td>
<td>0.585</td>
</tr>
<tr>
<td>d3</td>
<td>32</td>
<td>0.112</td>
<td>0.739</td>
<td>1</td>
<td>0.435</td>
</tr>
<tr>
<td>d4</td>
<td>34</td>
<td>0.072</td>
<td>0.842</td>
<td>1</td>
<td>0.496</td>
</tr>
<tr>
<td>d5</td>
<td>36</td>
<td>0.095</td>
<td>0.669</td>
<td>2</td>
<td>0.394</td>
</tr>
<tr>
<td>d6</td>
<td>38</td>
<td>0.128</td>
<td>0.531</td>
<td>4</td>
<td>0.313</td>
</tr>
<tr>
<td>d7</td>
<td>40</td>
<td>0.227</td>
<td>0.362</td>
<td>10</td>
<td>0.213</td>
</tr>
<tr>
<td>d8</td>
<td>42</td>
<td>0.438</td>
<td>0.254</td>
<td>25</td>
<td>0.150</td>
</tr>
<tr>
<td>d9</td>
<td>44</td>
<td>0.999</td>
<td>0.187</td>
<td>61</td>
<td>0.110</td>
</tr>
<tr>
<td>d10</td>
<td>46</td>
<td>2.810</td>
<td>0.145</td>
<td>135</td>
<td>0.085</td>
</tr>
<tr>
<td>d11</td>
<td>48</td>
<td>10.400</td>
<td>0.114</td>
<td>284</td>
<td>0.067</td>
</tr>
<tr>
<td>ref1</td>
<td>48</td>
<td>6.619</td>
<td>0.134</td>
<td>180</td>
<td>0.079</td>
</tr>
<tr>
<td>ref2</td>
<td>48</td>
<td>5.700</td>
<td>0.147</td>
<td>155</td>
<td>0.087</td>
</tr>
</tbody>
</table>

Table 3.6: Buildable design table generated through LitzOpt in the worst frequency case ($I_{winding} = 0.768$ $A_{rms}$ at $f_{sw} = 1.3$ MHz)

<table>
<thead>
<tr>
<th>Design Number</th>
<th>Gauge (AWG)</th>
<th>Relative Cost</th>
<th>Loss (W)</th>
<th>Number of Strands</th>
<th>$R_{ac}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>d1</td>
<td>28</td>
<td>0.503</td>
<td>2.129</td>
<td>1</td>
<td>3.601</td>
</tr>
<tr>
<td>d2</td>
<td>30</td>
<td>0.320</td>
<td>0.918</td>
<td>1</td>
<td>1.552</td>
</tr>
<tr>
<td>d3</td>
<td>32</td>
<td>0.205</td>
<td>0.483</td>
<td>1</td>
<td>0.818</td>
</tr>
<tr>
<td>d4</td>
<td>34</td>
<td>0.132</td>
<td>0.383</td>
<td>1</td>
<td>0.647</td>
</tr>
<tr>
<td>d5</td>
<td>36</td>
<td>0.087</td>
<td>0.456</td>
<td>1</td>
<td>0.771</td>
</tr>
<tr>
<td>d6</td>
<td>38</td>
<td>0.117</td>
<td>0.362</td>
<td>2</td>
<td>0.612</td>
</tr>
<tr>
<td>d7</td>
<td>40</td>
<td>0.248</td>
<td>0.218</td>
<td>6</td>
<td>0.369</td>
</tr>
<tr>
<td>d8</td>
<td>42</td>
<td>0.448</td>
<td>0.160</td>
<td>14</td>
<td>0.271</td>
</tr>
<tr>
<td>d9</td>
<td>44</td>
<td>0.986</td>
<td>0.119</td>
<td>33</td>
<td>0.202</td>
</tr>
<tr>
<td>d10</td>
<td>46</td>
<td>2.810</td>
<td>0.092</td>
<td>74</td>
<td>0.155</td>
</tr>
<tr>
<td>d11</td>
<td>48</td>
<td>10.400</td>
<td>0.072</td>
<td>155</td>
<td>0.122</td>
</tr>
<tr>
<td>ref1</td>
<td>48</td>
<td>12.086</td>
<td>0.071</td>
<td>180</td>
<td>0.120</td>
</tr>
<tr>
<td>ref2</td>
<td>48</td>
<td>19.069</td>
<td>0.078</td>
<td>284</td>
<td>0.132</td>
</tr>
</tbody>
</table>
in terms of both winding loss and cost and is added to see if the intermediate design could be more suitable design choice overall.

![Graph](image)

Figure 3-9: $R_{ac}$ vs $f_{sw}$ for three different litz wire designs chosen from Table 3.5 and 3.6.

Shown in Fig. 3-9 is the plot of $R_{ac}$ vs $f_{sw}$ for three different litz wire designs. These designs are chosen from Table 3.5 and 3.6 for this analysis in order to find the best design over the operating frequency range of the reference design in Table 3.4. Although Design 3 shows the lowest $R_{ac}$ in the lower frequency range due to having the lowest dc resistance, its performance becomes gradually compromised by the eddy current loss toward the higher operating frequency range. Considering the cost and winding loss, it is clear that Design 2, which comprises 180 strands of AWG 48 wire, is the best litz wire choice for the reference design. Note that this ac loss analysis on litz wire accounts for only strand-level effects due to eddy currents circulating within individual strands and ignores bundle-level effects due to eddy currents circulating between strands, assuming that bundle-level effects are negligible with the proper bundle construction.
3.4.2 Winding Configuration

In order to analyze the winding loss contribution from the secondary-side planar traces, M2Spice [13] and LTspice are utilized to compute $R_{ac}$ of secondary-side PCB traces. Shown in Fig. 3-10 are the possible winding configurations of the hybrid transformer: non-interleaved design and partially-interleaved design. The number of secondary-side PCB layers connected in parallel can be chosen from 4 - 8 layer which can be built with 1 oz or 2 oz copper. Each combination of the number of layers and amount of copper has been evaluated in order to choose the most practical and efficient combination for the secondary-side planar design as shown in Fig. 3-12. $R_{ac}$ of the chosen litz wire (48 AWG/180 strands) on the primary-side computed through LitzOpt in Section 3.4.1 and plotted in Fig. 3-9 is added to the ac resistance of the secondary-side PCB layers $R_{ac,sec}$ plotted in Fig. 3-11 for each combination at every operating frequency (680 kHz - 1.3 MHz in Table 3.4) through curve-fitting in order to compute $R_{ac,total}$ of the transformer and perform more meaningful comparison among the design choices. Note that the ac resistances of the primary-side litz are computed through LitzOpt and the ac resistance of the secondary-side PCB traces are computed through M2Spice and LTspice simulations as explained before. Then, these two ac-resistances computed independently are added together to figure out the total ac resistance of the hybrid transformer over the operating frequency. This process does not fully capture the possible conduction losses due to the mutual resistance components associated with the details of the primary and secondary winding conductor interactions [15], but it is anticipated to be quite close, especially in the case where
there is significant physical separation between primary and secondary windings as required for meeting galvanic isolation requirements.

(a) Secondary-side ac resistance $R_{ac,sec}$ of the non-interleaved configurations with 4, 6, and 8 layers built with 1 oz and 2 oz copper.

(b) Secondary-side ac resistance $R_{ac,sec}$ of the interleaved configurations with 6 and 8 layers built with 1 oz and 2 oz copper.

Figure 3-11: Secondary-side ac resistance $R_{ac,sec}$ for possible transformer winding configurations

For non-interleaved designs shown in Fig. 3-12a, it is straightforward to choose the secondary-side design with a 8-layer and 2 oz copper and the design with a 8-layer and 1 oz copper as the two best designs. Note that the design with a 8-layer and 1 oz copper shows better performance than the design with a 6-layer and 2 oz copper does toward high frequencies beyond 1 MHz due to the skin and proximity...
Figure 3-12: $R_{ac, total}$ vs $f_{sw}$ for possible transformer winding configurations

effects compromising the performance of the more copper-heavy design. $R_{ac, total}$ of these two best non-interleaved designs are then compared to the interleaved designs as shown in Fig. 3-12b. In terms of $R_{ac, total}$, the majority of the interleaved designs outperform the best non-interleaved designs as the non-interleaved designs are more susceptible to the eddy current losses. Based on the analysis, the interleaved design with a 8-layer built with 2 oz copper shows the best performance.

However, varying degrees of mismatch between the analysis results and experimental results in this analysis may come from the gap fringing effects and parasitics.
inter-winding capacitances that may compromise the transformer performance toward high frequencies. Shown in Fig. 3-13 are the drawings of non-interleaved and partially-interleaved hybrid transformers with scale. In order to prevent the fringing field effects (e.g., from the gap) and undesirable changes in current distribution across the PCB layers, a gap-to-winding clearance is recommended to be at least 25% of the total window width corresponding to h in Fig. 3-13 [16]. Furthermore, a clearance of approximately 0.5 mm between the primary-side litz wire and secondary-side PCB layers in Fig. 3-13b is set to respect IPC-2221B trace spacing requirement and minimize the inter-winding parasitic capacitances. Note that a teflon material with a low-permittivity can be used as a spacer between windings to meet the requirement and reduce the interwinding capacitances. In practice, the voltage insulation requirement between the primary and secondary windings of a transformer is 2.5 kV [1] and can be effectively met by using a triple insulated litz wire made up of three insulating layers that eliminates the needs for interlayer tapes and/or insulating tubes [17].

![Diagrams with scale of non-interleaved and partially-interleaved hybrid transformers. (The drawings are not to scale.)](image)

With the given core geometry of EQ20 EE and optimal litz wire design (48 AWG / 180 strands, 12 turns), a PCB height is set to 1 mm in order to meet the gap-to-winding (2.05 mm) and winding-to-winding (0.5 mm) clearances. Although the 2 oz copper interleaved designs with a 6-layer and 8-layer show the best performances in

---

1[16] treats the E-I core case, instead of the E-E core case, but it is estimated that the difference in the result would not be severe, especially as h is significantly larger than w.
terms of $R_{ac, total}$ as shown in Fig. 3-12b, building a 1-mm PCB with such configurations is costly since these configurations leave little room for pre-pregs and inner-layer cores with the given PCB height, such that exotic prepreg materials and PCB manufacturing method would need to be used to meet the voltage insulation requirement between layers. For this reason, the design with a 8-layer built with 1 oz copper is chosen due to its combination of reasonable performance and cost-effectiveness. As mentioned before, due to the fringing field effects and parasitic capacitances that may cause a mismatch between the analysis predictions and experimental results, an experimental evaluation of both non-interleaved and partially-interleaved transformers with the chosen winding design is performed in Section 4.2 and the final design for the hybrid transformer is chosen. As will be seen there, a non-interleaved design is preferred for multiple reasons.

### 3.5 System Loss Analysis

In order to predict the performance of the chosen design with a reasonable accuracy, an intuitive design tool and loss analysis are introduced in this section. A majority of the power loss of the DC-DC VIRT system is contributed by the transformer and switches from the inverter and VIRT rectifiers. Therefore, it is important to keep those losses in check in order to build the high-performance converter. To this end, the plots shown in Fig. 3-14 can serve as a useful design tool as a designer can intuitively see the amounts of resonant current ($I_{res}$) and magnetizing inductance current ($I_m$) in Fig. 3-14a and resulting conduction loss ($P_{cond}$), transformer loss ($P_{former}$), and total loss ($P_{total}$) at the selected input voltage ($V_{in} = 380$ V in this case) computed over the switching frequency ($f_{sw}$) in Fig. 3-14b. $P_{total}$ includes the energy loss of the capacitors in the VIRT rectifiers in addition to $P_{cond}$ and $P_{total}$. The plots shown in Fig. 3-14 are based on HB/bypass mode where $V_{in} = 380$ V, $V_{out} = 15$ V, and $P_{out}$ is 45 W. Note this operating condition is the bottleneck for achieving the voltage gain and ZVS requirements due to its lowest effective load resistance $R_{eff}$ as shown in Table 3.2.
The voltage gain and ZVS II curves are also included in Fig. 3-14b so that a designer can find an optimal operating point to meet the voltage gain and ZVS requirements and ensure the most optimal operation with the given LLC resonant design for the bottleneck mode (HB/bypass mode in this case) in an intuitive manner. Note that the fundamental harmonic approximation (FHA) is used for this analysis. Therefore,

\[ I_{m-rms} = \frac{\sqrt{2} n V_{out}}{k \pi^2 f_{sw} L_m}, \]  

(3.7)
\[
I_{oe-\text{rms}} = \frac{k \pi P_{out}}{2 \sqrt{2} n V_{out}},
\]

\[
I_{res-\text{rms}} = \sqrt{I_{m-\text{rms}}^2 + I_{oe-\text{rms}}^2},
\]

where \(k\) is the gain of the VIRT rectifier stage for each VIRT mode and defined in Equation (3.1) and \(I_{oe-\text{rms}}\) is the primary-side RMS current. \(P_{\text{cond}}\), total conduction loss from the inverter switches and active bypass and rectifier switches, are computed based on the resonant current \(I_{res-\text{rms}}\) and \(I_{oe-\text{rms}}\). A copper loss portion of \(P_{\text{transformer}}\) is computed using a curve-fitting method to define \(R_{ac}\) at every operating frequency based on the analysis in Section 3.4.2. Finally, a core loss portion is computed based on the square wave excitation of the transformer and chosen geometry and material of the core (EQ20 EE / N49). Due to the nature of the FHA, the power loss analysis is expected to show a better accuracy in the vicinity of the resonant frequency. Note that the power losses associated with the passive components such as resonant capacitors, blocking capacitors, and input and output capacitors are negligible and therefore not included in the analysis. Finally, the MATLAB script for the loss analysis is included in Appendix A so that one can generate the plots shown in Fig. 3-14 for any VIRT mode and input voltage \(V_{in}\).
Chapter 4

Implementation : VIRT with Bypass Switch

Based on the chosen design through the detailed analysis in Chapter 3, a complete DC-DC VIRT system with the bypass switch and hybrid transformer has been built and tested. The simulation and experimental results of the system are performed and analyzed to verify the electrical modeling of the VIRT and LLC resonant tank design. Furthermore, the performance of the newly proposed bypass mode operation (FB/bypss and HB/bypass) is compared to the performance achieved with the conventional VIRT operation (HB/HB and HB/0). Finally, other implementations of the VIRT rectifier to expand the number of possible operating modes are briefly explored; these approaches - while more complicated in terms of numbers of components - provide the opportunity to achieve different voltage gain characteristics and further optimization of the transformer loss.

4.1 Simulation

The operation of the DC-DC VIRT system is simulated using the LTspice circuit simulation tool as shown in Fig. 4-1. Note that the small resistors (e.g. R3, R4, and so on) included in the schematics serve to measure currents without affecting operation of the system. Simulation waveforms for three key VIRT operating modes:
FB/FB, FB/bypass, and HB/bypass modes are shown in Fig. 4-2, Fig. 4-3, and Fig. 4-4, respectively. The simulation further verifies the electrical model of the VIRT and LLC resonant tank design performed in Section 3.3 as there is a small overall $f_{sw}$ difference between the FHA analysis and simulation for each VIRT operating mode.
which becomes even closer towards the resonant frequency $f_{res}$ of 1.15 MHz. In order to experimentally evaluate the electrical model and LLC resonant tank design, these simulation waveforms will also be compared to the experimental waveforms in Section 4.3. Note that in order to ensure synchronous operation of the VIRT rectifier and prevent a body-diode conduction, a turn-on timing and duration of each rectifier switch need to be fine-tuned. As the waveforms in Fig. 4-5 suggest, a poor tuning of the rectifier switches results in body diode (or equivalent) conduction and
compromises the performance of the VIRT rectifier.

(a) An ideal synchronous rectifier operation as a result of good tuning. FB/bypass mode ($V_{OUT} = 9$ V at 36 W).

(b) Body diode conduction as a result of poor tuning. FB/bypass mode ($V_{OUT} = 9$ V at 36 W)

Figure 4-5: Good tuning vs poor tuning of the rectifier switches.
4.2 VIRT Transformer Evaluation

![Ideal simulated VIRT rectifier waveforms for FB/FB mode](image1)

Figure 4-6: Ideal simulated VIRT rectifier waveforms for FB/FB mode ($V_{in} = 120$ V (Inverter mode 1) and $V_{out} = 5$ V at 25 W).

![VIRT waveforms from the non-interleaved transformer](image2)

Figure 4-7: VIRT waveforms from the non-interleaved transformer for FB/FB mode ($V_{in} = 170$ V (Inverter mode 1) and $V_{out} = 5$ V at 25 W. 95.3 % power stage efficiency. $L_m = 36.3 \mu H$, $L_r = L_{\text{Leak}} = 5.5 \mu H$, and $C_r = 3.47 nF$).

In Section 3.4.2, a litz wire with 48 AWG / 180 strands and a 8-layer PCB built with 1 oz copper are chosen for the primary-side winding and secondary-side winding, respectively, based on their performance and cost-effectiveness. With the given winding designs, the performances with a non-interleaved (Fig. 3-13a) and partially
Figure 4-8: VIRT waveforms from the partially-interleaved transformer for FB/FB mode ($V_{in} = 120$ V (Inverter mode 1) and $V_{out} = 5$ V at 25 W. 92.0 % power stage efficiency. $L_m = 27.8$ $\mu$H, $L_r = 4$ $\mu$H ($L_{leak} = 2.5$ $\mu$H and $L_{r,ext} = 1.5$ $\mu$H), and $C_r = 3.47nF$).

interleaved (Fig. 3-13b) transformer are experimentally evaluated. Both transformer configurations were tested with the DC-DC VIRT system whose schematic is shown in Fig. 4-10a. Full design information including schematics, BOM, and layout for one of the design configurations can be found in Appendix B.2. The different experiments vary by transformer configuration only. Despite the slight difference in their resonant tanks and operating frequencies, they are expected to have comparable power stage efficiencies and symmetrical VIRT rectifier waveforms. Any substantial drop in a power stage efficiency and asymmetry of VIRT waveforms can be attributed to the parasitic effects from the transformer.

The rectifier waveforms from the non-interleaved design in Fig. 4-7 show a good symmetry and resemblance to the ideal simulated waveforms in Fig. 4-6, whereas the rectifier waveforms from the interleaved design in Fig. 4-8 are affected with the parasitic effects from gap fringing fields and inter-winding capacitances which result in undesirable current flows through the layers of the VIRT transformer and distorted rectifier waveforms with spikes and poor symmetry. In the non-interleaved version of the transformer, a gap-to-winding clearance (2 mm) is satisfied and primary-to-secondary inter-winding capacitances are insignificant since the windings are placed
Figure 4-9: Diagram and Picture of Hybrid litz-PCB construction of VIRT transformer. The litz wire used for the winding is 48 AWG / 180 strands (5 bundles where each bundle contains 36 strands).

at each end of the window area as shown in Fig. 3-13a. On the other hand, in the partially-interleaved version of the transformer shown in Fig. 3-13b, some secondary-side layers of the PCB toward the gap are inevitably susceptible to the fringing field effects. In addition, the parasitic inter-winding capacitances come into play due to a relatively small spacing between the windings. One may choose to utilize a larger core to minimize the parasitic effects, which, however, makes the miniaturization of the converter harder to achieve. Consequently, in experimental evaluation the VIRT system with the non-interleaved hybrid transformer achieves a high power stage efficiency of 95.3 % whereas the VIRT system suffers from a poor power stage efficiency and undesirable parasitic effects when implemented with the partially interleaved transformer. Furthermore, the placement of windings in the non-interleaved hybrid transformer results in a large leakage inductance (5.5 μH in this case). In a LLC resonant tank design, this eliminates the need for an additional physical inductor, which is very promising for achieving a high power density design.

Therefore, the non-interleaved hybrid transformer design shown in Fig. 4-9a is chosen to be implemented with the VIRT system due to its superior capability to minimize the parasitic effects and potential for a high power density design. The transformer is implemented with an EQ20 EE/N49 core, 10-mil gap across all legs where the primary-side winding has 12 turns routed with a 48 AWG/180 strands (5 bundles where each bundle contains 36 strands) litz wire and the secondary-side winding consists of 8 layers of 1 oz copper PCB trace connected in parallel.
Table 4.1: List of main components in the DC-DC VIRT with the bypass switch

<table>
<thead>
<tr>
<th>Stacked Half-Bridge Inverter</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>EPC2050 (350 V / 25 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Signal isolators</td>
<td>SI8610</td>
</tr>
<tr>
<td>Isolated power</td>
<td>ADUM5010</td>
</tr>
<tr>
<td>Balancer diodes</td>
<td>MMBD3004BRM</td>
</tr>
<tr>
<td>Balancer capacitors</td>
<td>10 uF (1812) / 450 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIRT Rectifier</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectifier switches</td>
<td>TPN2R703NL (30 V / 45 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Bypass switches</td>
<td>EPC2023 (30 V / 90 A)</td>
</tr>
<tr>
<td>Gate driver (bypass)</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Isolated power and digital signals (bypass)</td>
<td>ADUM5210</td>
</tr>
<tr>
<td>Blocking capacitors</td>
<td>22 uF (0805) / 25 V</td>
</tr>
<tr>
<td>Decoupling capacitors</td>
<td>25 uF (0508) / 25 V per half-bridge</td>
</tr>
<tr>
<td>Output capacitors</td>
<td>22 uF (1210) / 25V</td>
</tr>
</tbody>
</table>

4.3 Experimental Results

Shown in Table 4.1 and Fig. 4-10 are the list of main components in the DC-DC VIRT with the bypass switch and schematic and prototype pictures of the DC-DC VIRT system with the bypass switch, respectively. As mentioned before, the bypass switch is implemented with two “back-to-back” MOSFETs (EPC2023 GaN FETs in this case) such that it can carry bidirectional current and block bidirectional voltage. A layout showing how these “back-to-back” GaN FETs are placed with respect to the transformer and VIRT rectifier switches is shown in Fig. 4-11. The rectifier switches outlined with blue are placed on the bottoms-side of the PCB along with the blocking capacitors whereas the bypass switches and their gate driver are placed on the top-side. Note ADUM5210 (not shown in the figure) from Analog Devices is used to provide an isolated power and bypass switch driving signal to the gate driver (UCC27611), which drives two GaN FETs (EPC2023) with its reference to the source (S) of these two back-to-back FETs. Owing to the hybrid litz-PCB construction of the VIRT transformer which satisfies the voltage insulation requirement due to the placement of its windings sufficiently away from each other, the bypass switches can be
Figure 4-10: Schematic and prototype pictures of the DC-DC VIRT system with the bypass switch.
placed on the top-side area of the PCB in close vicinity of the core, optimizing the path of the secondary-side induced current when the bypass modes are activated. With a fully planar construction of the VIRT transformer where a top-side of the board has to be used as the primary-side PCB winding for the several practical reasons mentioned in Section 3.4.2, the bypass switches would have had to be placed substantially away from the primary-side winding to meet the voltage insulation requirement, incurring additional copper loss associated with the extended current path and compromising the performance of the VIRT system.

Experimental results show three key VIRT operations: FB/FB (Fig. 4-12), FB/bypass (Fig. 4-13), and HB/bypass (Fig. 4-14) modes, which validates the DC-DC VIRT system modeling and design. These experimental waveforms and operating switching frequencies $f_{sw}$ show a close resemblance to the simulation waveforms and switching frequencies $f_{sw}$ in Section 4.1 (Fig. 4-2 for FB/FB, Fig. 4-3 for FB/bypass, and Fig. 4-4 for HB/bypass) obtained at the same operating points. As shown in Fig. 4-15a, the bypass modes described in Fig. 3-1c and 3-1e result in much more efficient operation compared to the conventional VIRT modes of operation in Fig. 3-1d and 3-1f.
The efficiency improvement is substantial in HB/bypass mode compared to HB/0 mode is due to full utilization of the core area which results in reduced transformer loss as shown in Fig. 4-15b. A part of the efficiency improvement is also attributable to reduced circulating currents in HB/bypass mode. This reduction is due to HB/bypass mode having a larger "net" magnetizing inductance compared to HB/0 mode as shown in Table 3.1, due to the transformers being constructed with a gap across all three core legs. Note that the number of active switches and the number of always-on switches
are the same for both zero and bypass modes. However, the bypass switches can be optimized for smallest $R_{on}$ as their switching characteristics are irrelevant. Therefore, in HB/bypass mode, a small portion of an efficiency improvement comes from the fact lower resistance always-on switches (i.e. bypass switches) are utilized. On the other hand, in FB/bypass mode, an efficiency improvement compared to HB/HB mode is associated with these always-on switches.

As shown in Fig. 4-16, the power losses associated with a conventional HB/0 mode range from 3 W to 6.5 W and are disproportionately high compared to the power losses from the rest of the VIRT modes. This can result in an unacceptable temperature raise of the converter, making it unsuitable as a consumer electronics product. With the bypass modes, the power losses in HB/0 mode are dramatically reduced below 3 W, compressing the range of power losses across all the modes of VIRT operation and keeping temperature raise of the converter in check.

### 4.4 Other Implementations of the VIRT rectifier

We introduced the VIRT structure implemented with full-bridge rectifiers in Chapter 2 and the improved VIRT structure with the bypass switch in this chapter. A
full-bridge rectifier can be configured as a full-bridge, half-bridge, or zero in order to achieve a re-configurable transformer turns-ratio. To this end, a different rectifier topology (e.g. switched-capacitor step-down rectifier) and/or number of core sections (e.g. 5-legged core) could be utilized to provide different ranges of effective trans-
former turns ratio and offer further scaling down of the copper loss associated with physical transformer windings.

4.4.1 Switched-capacitor Step-down Rectifier

Shown in Fig. 4-17 are the VIRT structure implemented with the switched-capacitor step-down rectifier [18] and schematics of the single and multi-level rectifier. Note that the primary-side winding is not shown for the simplicity and the capacitors in blue correspond to dc blocking capacitors. One rectifier is placed on the top side and the other rectifier symmetrical across the core is placed on the bottom. One end of each half-turn is connected to the input of the rectifier and the other end is connected to the ground such that an ac voltage across each half-turn (e.g. $V_{AC1}$) is applied as an input to the rectifier as shown in Fig. 4-17b. Note that the bypass switch $S_{BYP}$ enables the “bypass” mode where the induced secondary-side current path is redirected such that it bypasses the entire rectifier structure on one side (top side in this case) of the VIRT transformer in order to fully utilize the given core area as explained in Chapter 3.2. Finally, $S_1$ and $S'_1$ are implemented with P-Channel MOSFETs and $S_2$ and $S'_2$ are implemented with N-Channel MOSFETs, where each switch needs to be rated for $V_{out}$.
The operation of the switched-capacitor capacitor is well illustrated in [18]. In addition to Mode 1 in [18], Mode 2 and Mode 3 are introduced to achieve re-configurable conversion ratio. Details on the modes of operation are shown in Table 4.2. In Mode 1 where a rectifier is implemented with the multi-level switched-capacitor step-down rectifier as shown in Fig. 4-17c, one can achieve a higher step-down ratio of the transformer with a higher level rectifier (i.e. \( N_p : \frac{1}{2N} \) for a N-level rectifier). Furthermore, one can decide to bypass intermediate rectifier(s) to achieve multiple different turns ratios. For example, with a 2-level switched-capacitor step-down rectifier, it is possi-
ble to achieve not only $N_p : \frac{1}{4}$ but also $N_p : \frac{1}{2}$ by bypassing an intermediate rectifier. Finally, despite the complexity of driving the switches and larger area compared to a full-bridge rectifier, its integrated version has a strong potential to overcome those setbacks and still achieve a compact VIRT design with a greater flexibility in an effective conversion ratio.

Table 4.2: Modes of operation for the VIRT with a switched-capacitor step-down rectifier.

| Mode   | $\Phi 1$ | $\Phi 2$ | $|\Delta V_{AC}|$ | Effective turns ratio ($n$) | Notes                                                                 |
|--------|----------|----------|-------------------|-----------------------------|----------------------------------------------------------------------|
| Mode 1 [18] | $S_1, S'_1$ | $S_2, S'_2$ | $2N \cdot V_{out}$ | $N_p : \frac{1}{2N}$ | n equivalent to FB/FB mode when $N = 1$ |
| Mode 2 | $S_1, S'_2$ | $S_2, S'_1$ | $V_{out}$ | $N_p : 1$ | n equivalent to HB/HB (FB/bypass) mode |
| Mode 3 | $S_1, S'_2, S_{BYP}$ | $S_2, S'_1, S_{BYP}$ | $V_{out}$ | $N_p : 2$ | The other rectifier is shorted to GND. n equivalent to HB/0 (HB/bypass) mode |

4.4.2 VIRT with a 5-legged Core and Bypass Switches

![Figure 4-18: The VIRT structure with a 5-legged core and bypass switches.](image)

Shown in Fig. 4-18 is the VIRT structure with a 5-legged core and bypass switches. Four full-bridge rectifiers are connected through quarter-turns around a 5-legged core. When all the rectifiers are operating as full-bridges, this structure can achieve the effective turns ratio of $N_p : \frac{1}{4}$, which provides a designer with a means to further...
scale down the number of transformer primary-side turns, reducing copper loss when the transformer loss is still not optimized with an effective turns ratio of $N_p : \frac{1}{2}$. As for the case for the VIRT with a switched-cap step-down rectifier, each full-bridge rectifier can be “bypassed” through the bypass switch in order to achieve additional effective turns ratios as shown in Table 4.3 and ensure a full utilization of the effective core area across all modes of operations. While these design approaches have not yet been implemented (as the one utilized led to good performance) they are promising for future designs having specifications which motivate more operating modes and/or a greater degree of re-scaling between core and copper loss.
Chapter 5

Conclusion

5.1 Summary

In order to build a high-performance DC-DC converter for portable charger applications which require the large step-down ratios and variations in operating voltage (e.g. universal ac input voltage 85 - 265 V<sub>ac</sub> and regulated dc output 5 - 20 V), a new hybrid magnetic-electronic structure, the Variable-Inverter-Rectifier-Transformer (VIRT), has been proposed. The electrical model of the VIRT structure and different modes of operation are derived and explored in Chapter 2. The prototype, designed to handle dc input voltage between 120 and 380 V, which corresponds to ac peak of 85 V<sub>rms</sub> and 264 V<sub>rms</sub>, respectively, and regulate the dc output voltage to any of 5 V, 9 V, and 12 V, are built and tested to validate the derived electrical model. Furthermore, the fractional and reconfigurable conversion ratios made possibly by the VIRT structure enable high-performance of the system across wide range of operating conditions.

In Chapter 3, a comprehensive design analysis is performed on the DC-DC VIRT system with the bypass switch and hybrid transformer. The VIRT rectifier topology augmented by the "bypass" switch enables a full utilization of the given core area and dramatically improves the transformer loss compared to a conventional VIRT asymmetric mode (HB/0). A systematic design method for the LLC resonant tank interfaced with the VIRT structure is thoroughly explained. Furthermore, a hybrid
VIRT transformer where the primary-side winding consists of a carefully selected litz wire winding and the secondary-side is constructed with PCB traces in a planar fashion has been designed and implemented with the VIRT structure in order to further reduce the copper loss of the transformer by better utilizing the window area of the core and mitigating skin and proximity effects. Finally, an intuitive design tool generated through a MATLAB script for the power loss analysis of the DC-DC VIRT system is developed.

The optimal design of the DC-DC VIRT system carefully chosen and analyzed in Chapter 3 is simulated, implemented, and tested in Chapter 4. Furthermore, a non-interleaved winding configuration of the hybrid transformer is selected since it is found experimentally that the non-interleaved winding configuration minimizes parasitic effects and enables a further miniaturization of the system by fully replacing the external resonant inductor with transformer leakage inductance. With the proposed hybrid transformer design and bypass switch, the DC-DC VIRT system has shown much improved performance especially in high output voltage and power operations (e.g. 15 V at 45 W and 20 V at 50 W) compared to the conventional VIRT mode (HB/0), dramatically reducing the temperature raise of the converter at the rated power. Finally, other implementation options for the VIRT rectifier are introduced to achieve wider range of the output voltage compression.

5.2 Future Work

Figure 5-1: Board picture of the area-optimized DC-DC VIRT system with the bypass switch and planar windings (secondary-side) of the hybrid transformer.
Figure 5-2: Simplified diagram of the full ac-dc system with the DC-DC VIRT stage.

Shown in Fig. 5-1 is the picture of the area-optimized version of the DC-DC VIRT system. Board I and Board II in 4-10b are integrated into one single board with a dramatic area reduction owing to the reduced size of the LLC resonant tank, small form factor switches and gate drivers, and PCB layout techniques. Future work involves designing and building a full ac-dc system which consists of the ac-dc rectifier and DC-DC VIRT stages as shown in Fig. 5-2. The DC-DC VIRT stage shown in Fig. 5-1 sets the area of the full ac-dc system and other essential parts of the system such as an ac-dc rectifier stage with a bus capacitor and EMI filter will be designed and integrated with the VIRT stage. In the following section, we outline the sizing of a bus capacitor for an ac-dc converter, which is one of the considerations for an ac-dc converter system beyond that required for the dc-dc converter block itself. It is further described how sizing this bus capacitor influences further optimization of the dc-dc converter stage.

5.2.1 Bus Capacitor Volume Analysis

In an grid-tied ac-dc converter for portable charger applications, an energy storage device, often implemented with capacitors, is required in order to handle instantaneous power difference at twice-line frequency between the time-varying power drawn from the ac source and the constant power delivered to the dc output bus. Typically, this bus capacitor is a group of large electrolytic capacitors that make a miniaturization of the converter especially challenging. Therefore, in order to build a high-performance, miniaturized ac-dc system, one needs to come up with a means to reduce the volume of the bus capacitor. Multiple "exotic" means are available, including more sophisticated circuit blocks that replace simple capacitors with switched-mode circuits to
buffer energy (e.g., [19], [20], and [21]), or by using power-factor correction circuitry to draw carefully-selected line currents to minimize energy storage (e.g., [22]). Here we consider some basic considerations in selecting capacitor size for the proposed charger application when interfacing the line via a simple line-frequency rectifier.

Figure 5-4: Plot of $C_{bus}$ over $V_{min}$ at $V_{in} = 85 V_{rms}$ ($V_{max} = 120 V$), $f_{line} = 50$ Hz, and $P_{out} = 50$ W.

Shown in Fig. 5-3 are a simple representation of the full-bridge rectifier output voltage waveform across the bus capacitor $V_{bus}$ and idealized full-bridge rectified waveform $V_{rec}$. The energy stored in the capacitor (C) with the charged voltage ($V_{bus}$) is

$$E = \frac{CV_{bus}^2}{2},$$

(5.1)
Therefore, the energy discharged by the bus capacitor in each cycle is

\[ E_{\text{discharged}} = \frac{C_{\text{bus}}(V_{\text{max}}^2 - V_{\text{min}}^2)}{2} = P_{\text{avg}}\Delta t, \quad (5.2) \]

where \( P_{\text{avg}} \) is the average power and \( \Delta t \), the discharging interval in each cycle, is \( \frac{\pi - \Theta}{2\pi f_{\text{line}}} \). Using a trigonometric approximation, the charging angle \( \Theta = \cos^{-1}(V_{\text{min}}/V_{\text{max}}) \).

Finally, re-arranging Equation (5.2),

\[ C_{\text{bus}} = \frac{2P_{\text{avg}}(\pi - \cos^{-1}(V_{\text{min}}/V_{\text{max}}))}{2\pi f_{\text{line}}(V_{\text{max}}^2 - V_{\text{min}}^2)}, \quad (5.3) \]

It is intuitively clear from Equation (5.3) that one can reduce \( C_{\text{bus}} \) by making \( V_{\text{min}} \) smaller with the given peak voltage of the ac line \( V_{\text{max}} \) and therefore making the ripple voltage across \( C_{\text{bus}} \) larger. Shown in Fig. 5-4 is the plot of \( C_{\text{bus}} \) over \( V_{\text{min}} \) at \( V_{\text{in}} = 85 \) V\(_{\text{rms}} \) (i.e. \( V_{\text{max}} = 120 \) V), \( f_{\text{line}} = 50 \) kHz, and \( P_{\text{out}} = 50 \) W. Note that this operating condition is the worst-case scenario that maximizes \( C_{\text{bus}} \). Therefore, with the same \( C_{\text{bus}} \) chosen for this operating condition, \( V_{\text{min}} \) in all other operating conditions that the DC-DC VIRT stage has to handle is higher than \( V_{\text{min}} \) in the operating condition shown in Fig. 5-4.

If \( V_{\text{min}} \), for example, is allowed to go as low as 85 V, the required \( C_{\text{bus}} \) is only 105 \( \mu \)F which can be implemented with relatively small electrolytic capacitors. This is very promising for building a miniaturized ac-dc converter. In order to achieve the volume miniaturization through this method, the DC-DC VIRT system needs to be designed such that it can handle \( V_{\text{min}} \) (e.g. 85 V) and still generate the required output voltage. Future work, therefore, involves tuning the LLC resonant tank in the DC-DC VIRT stage to accommodate such a range, and implementing a closed-loop control to regulate the output voltage of the DC-DC stage to a constant level with the varying input voltage.
Appendix A

MATLAB scripts

This appendix includes MATLAB scripts used to generate voltage gain curves, ZVS boundaries, and power losses of the DC-DC VIRT system computed over the operating frequency. These generated plots serve as an intuitive design tool for those who would like to design the VIRT system with wide range of operating conditions.
(a) Voltage gain and ZVS curves for FB/FB mode ($V_{out} = 9$ V and $P_{out} = 36$ W).

(b) Voltage gain and ZVS curves for HB/bypass mode ($V_{out} = 20$ V and $P_{out} = 50$ W).

Figure A-1: Voltage gain and ZVS curves generated through MATLAB scripts ($VIRTS\text{ystemGainZVS.m}$ and $VIRTvoltageGainPlotter.m$).
Listings

A.1 Output voltage gain and ZVS boundaries .................................. 89
A.2 VIRT system currents and losses .............................................. 96
A.3 Output voltage gain plotter ...................................................... 114

Listing A.1: Output voltage gain and ZVS boundaries

1  % Author: Intae Moon
2  % Last modified: July. 15, 2018
3  %
4  % filename: VIRTSystemGainZVS.m
5  %
6  % This code generates voltage gain curves for any VIRT operating modes
7  % (FB/FB, FB/bypass, and HB/bypass modes) at Vin = 120 V, 140 V, 170 V
8  %, 310
9  % V, 340 V, and 380 V. Furthermore, two ZVS boundary curves are
generated.
10  % ZVS I is a dividing line between the inductive Zin and capacitive
Zin.
11  % ZVS II boundary, which is based on the energy requirement for
sufficient
12  % charge and discharge, sets the minimum output voltage the DC-DC VIRT
system
13  % can achieve at certain switching frequency with the given LLC
parameters
% in order to achieve ZVS on the primary-side inverter.
clear all;
close all;
clc;

%% User inputs
% I. LLC resonant tank parameters
Cr = 3.47e-9;
Lr = 5.5e-6;
Ln = 20.169e-6/Lr;
Lm = Lr*Ln;
Np = 12;

% II. VIRT operating mode
% VIRTmode 0 -> FBFB 5V
% VIRTmode 1 -> FB/bypass 9V
% VIRTmode 2 -> HB/bypass 15V
% VIRTmode 3 -> HB/bypass 20V
VIRTmode = 2;

loop_count = 6;
for i = 1:1:loop_count
% Ceq chosen based on EPC2050 datasheet at each Vin
if i == 1
    Vin = 120;
    invMode = 0;
    Ceq = 186e-12; % two in series for a VFX inverter
elseif i == 2
    Vin = 140;
invMode = 0;
Ceq = 176e-12;

elseif i == 3
Vin = 170;
invMode = 0;
Ceq = 152e-12;

elseif i == 4
Vin = 310; % for calculating ZVS boundary II
invMode = 1;
Ceq = 159e-12; % at 155 V

elseif i == 5
Vin = 340;
invMode = 1;
Ceq = 155e-12; % at 325/2 V

elseif i == 6
Vin = 380;
invMode = 1;
Ceq = 140.5e-12; % find out the best scaling factor at 380/2 V
end

% Computing the effective voltage onto the LLC resonant tank
% using a stacked half-bridge inverter gain for Mode 1 and 2
if (invMode == 0) % Inverter Mode 1;
    Minv = 0.5;
    V_LLCEff = Vin*Minv;
    ncap = 4; % # of device cap charged/discharged in each cycle.
    To be used for ZVS II curve
else % Inverter Mode 2;
    Minv = 0.25;
    V_LLCEff = Vin*Minv;
end
ncap = 2;

end

if VIRTmode == 0 % 5 V (FB/FB) operation
    Rload = 1;
    Vout_desired = 5;
    Re = 32*Np^2/pi^2*Rload;
    k_rec = 1/2;
elseif VIRTmode == 1 % 9 V (FB/bypass) operation
    Rload = 2.25;
    Vout_desired = 9;
    Re = 8*Np^2/pi^2*Rload;
    k_rec = 1;
elseif VIRTmode == 2 % 15 V (HB/bypass) operation
    Rload = 5;
    Vout_desired = 15;
    Re = 2*Np^2/pi^2*Rload;
    k_rec = 2;
elseif VIRTmode == 3 % 20 V (HB/bypass) operation
    Rload = 8;
    Vout_desired = 20;
    Re = 2*Np^2/pi^2*Rload;
    k_rec = 2;
end

% Series resonant frequency
fo = 1/(2*pi*sqrt(Lr*Cr));
f_min = 100e3;
f_max = 3600e3;
\[ L_m = \frac{L_m}{L_r}; \]
\[ Q_e = \frac{\sqrt{L_r/C_r}}{R_e}; \]

% Plot voltage gain curves and Mz1 (for computing ZVS I boundary, a
% dividing line between the inductive Zin and capacitive Zin)
[Mz1, fn, Mg, fsw, Vo] = VIRTvoltageGainPlotter(fo,f_min,f_max,Ln,
    Qe, V_{LLC\_eff}, i, Np, Lr, Lm, Cr, Re, VIRTmode, loop_count,
    k_{rec});

% ZVS I boundary : dividing line between the inductive Zin and capacitive Zin
netVo = Vo./Mg;
outZVSI = netVo.*Mz1;
outZVSI(1:6995) = -5;

% Plot ZVS II boundary (ensuring sufficient inductive energy in
% the system to charge/discharge Cds)
\[ k_{inv} = \frac{1}{2}; \] % A scaling factor to calculate the actual voltage
across the device capacitance
outZVSII = sqrt(ncap*Ceq*(k_{inv}*Vin)^2/(L_m + L_r))*2*pi^2*fsw.*
L_m*k_{rec}/(4*Np)*1000;

%% Plot ZVS boundary I and II
if (i == 1)
    plot(fsw, outZVSI, 'DisplayName', 'V_{in} = 120 V ZVS I','
        Color','k', 'LineStyle','--');
    plot(fsw, outZVSII,'DisplayName', 'V_{in} = 120 V ZVS II','
        Color','k', 'LineStyle',':');
elseif (i == 2)
plot(fsw, outZVI, 'DisplayName', 'V_{in} = 140 V ZVS I', 'Color', 'b', 'LineStyle', '-.');
plot(fsw, outZVII, 'DisplayName', 'V_{in} = 140 V ZVS II', 'Color', 'b', 'LineStyle', ':');

elseif (i == 3)
    plot(fsw, outZVI, 'DisplayName', 'V_{in} = 170 V ZVS I', 'Color', 'c', 'LineStyle', '-.');
    plot(fsw, outZVII, 'DisplayName', 'V_{in} = 170 V ZVS II', 'Color', 'c', 'LineStyle', ':');

elseif (i == 4)
    plot(fsw, outZVI, 'DisplayName', 'V_{in} = 310 V ZVS I', 'Color', 'g', 'LineStyle', '-.');
    plot(fsw, outZVII, 'DisplayName', 'V_{in} = 310 V ZVS II', 'Color', 'g', 'LineStyle', ':');

elseif (i == 5)
    plot(fsw, outZVI, 'DisplayName', 'V_{in} = 340 V ZVS I', 'Color', 'm', 'LineStyle', '-.');
    plot(fsw, outZVII, 'DisplayName', 'V_{in} = 340 V ZVS II', 'Color', 'm', 'LineStyle', ':');

elseif (i == 6)
    plot(fsw, outZVI, 'DisplayName', 'V_{in} = 380 V ZVS I', 'Color', 'r', 'LineStyle', '-.');
    plot(fsw, outZVII, 'DisplayName', 'V_{in} = 380 V ZVS II', 'Color', 'r', 'LineStyle', ':');
end

legend('Location', 'bestoutside')
set(gca, 'FontSize', 28);
end
%% Plotting the horizontal line for the desired output voltage
grid on;
grid minor;

lgd = legend('show');
lgd.FontSize = 15;
ylim([0 ceil(max(Vo))+2])

if VIRTmode == 0 % 5 V (FB/FB) operation
    hline = refline([0 5]);
elseif VIRTmode == 1 % 9 V (FB/bypass) operation
    hline = refline([0 9]);
elseif VIRTmode == 2 % 15 V (HB/bypass) operation
    hline = refline([0 15]);
elseif VIRTmode == 3 % 20 V (HB/bypass) operation
    hline = refline([0 20]);
end

hline.Color = 'k';
hline.LineStyle = '-';
hline.DisplayName = 'V_{out} desired';
tlt = title(['Q_{e} = ' num2str(round(Qe,4)) ' L_{m} = ' num2str(round(Lm*1e6,2)) ' uH, L_{r} = ' num2str(round(Lr*1e6, 3))...
    ' uH, C_{r} = ' num2str(round(Cr*1e9, 3)) ' nF, f_{res} = ' num2str(round(fo/1000)) ' kHz, N_{p} = ' num2str(Np) ' turns, V_{out} = ' num2str(Vout_desired) ' V']);
tlt.FontSize = 15;

set(gca, 'FontSize', 28);
set(findall(gca, 'Type', 'Line'),'LineWidth',1.5);
% Author: Intae Moon
% Last modified: Aug. 1, 2018
% filename: VIRTSystemLoss.m
%
% This code generates magnetizing current (Im) and resonant current (Ires)
% based on the fundamental harmonic approximation (FHA) for any VIRT
% operating mode (FB/FB, FB/bypass, and HB/bypass mode)
% Furthermore, based on the computed currents in the system, this code
% plots conduction loss of the inverter and rectifier switches (P_cond),
% transformer loss (P_xformer), secondary-side rectifier capacitor
% losses (P_coss), and resulting total loss of the system (P_total) for any
% Vin
% (120 V, 140 V, 170 V, 310 V, 340 V, 380 V)
% and VIRT operating modes.
%
% Outputs: VIRT_current_curves.pdf, VIRT_system_losses.pdf
%
clc;
close all;
clear all;

%% User inputs
% I. LLC resonant tank parameters
Cr = 3.47e-9;
Lr = 5.5e-6;
Ln = 20.169e-6/Lr;
Lm = Lr*Ln;
Np = 12;

% II. VIRT operating mode
VIRTmode 0 -> FBFB 5V
VIRTmode 1 -> FB/bypass 9V
VIRTmode 2 -> HB/bypass 15V
VIRTmode 3 -> HB/bypass 20V
VIRTmode = 2;

% III. Select Vin for the system loss calculation for the chosen VIRT mode
sel 1 -> 120 V, sel 2 -> 140 V, sel 3 -> 170 V, sel 4 -> 310 V, sel 5 ->
% 340 V, sel 6 -> 380 V
sel = 6;

% On-resistances of the inverter switch (EPC2050), rectifier switch
% (TPN2R703NL), and bypass switch (EPC2033)
Rds_pri = 120e-3; % EPC2050
Rds_sec = 4e-3; % TPN2R703NL
Rds_gan = 1.6e-3; % EPC2023

% Device capacitance (TPN2R703NL) selected based on the desired output
% voltage
if VIRTmode == 0
    Cross = 1.8e-9;
elseif VIRTmode == 1
    Cross = 1.3e-9;
elseif VIRTmode == 2
    Cross = 0.85e-9;
else
    Cross = 0.7e-9;
end

loop_count = 6;
for i = 1:1:loop_count
    if i == 1
        Vin = 120;
        invMode = 0;
    elseif i == 2
        Vin = 140;
        invMode = 0;
    elseif i == 3
        Vin = 170;
        invMode = 0;
    elseif i == 4
        Vin = 310;
        invMode = 1;
    elseif i == 5
        Vin = 340;
        invMode = 1;
    elseif i == 6
        Vin = 380;
 invMode = 1;
end

% Computing the effective voltage onto the LLC resonant tank
% using a stacked half-bridge inverter gain for Mode 1 and 2
if (invMode == 0) % For Inverter mode 1;
    Minv = 0.5;
    V_LLCEff = Vin*Minv;
    ncap = 4; % # of device cap charged/discharged in each cycle.
    To be used for ZVS II curve
else % For Inverter mode 2;
    Minv = 0.25;
    V_LLCEff = Vin*Minv;
    ncap = 2;
end

if VIRTmode == 0 % 5 V (FB/FB) operation at 25 W
    Rload = 1;
    Vout_desired = 5;
    Re = 32*Np^2/pi^2*Rload;
    k_rec= 1/2; % VIRT rectifier gain
elseif VIRTmode == 1 % 9 V (FB/bypass) operation at 36 W
    Rload = 2.25;
    Vout_desired = 9;
    Re = 8*Np^2/pi^2*Rload;
    k_rec= 1;
elseif VIRTmode == 2 % 15 V (HB/bypass) operation at 45 W
    Rload = 5;
    Vout_desired = 15;
    Re = 2*Np^2/pi^2*Rload;
elseif VIRTmode == 3 % 20 V (HB/bypass) operation at 50 W
    Rload = 8;
    Vout_desired = 20;
    Re = 2*Np^2/pi^2*Rload;
    k_rec = 2;
end

fo = 1/(2*pi*sqrt(Lr*Cr)); % series resonant frequency
f_min = 100e3;
f_max = 3600e3;

Ln = Lm/Lr;
Qe = sqrt(Lr/Cr)/Re;

% Plot voltage gain curves
[Mz1, fn, Mg, fsw, Vo] = VIRTvoltageGainPlotter(fo,f_min,f_max,Ln,
    Qe, V_LLCEff, i, Np, Lr, Lm, Cr, Re, VIRTmode, loop_count,
    k_rec);

fsw = linspace(f_max,f_min,10000);

% Based on the selected voltage input (Vin), a corresponding
% output voltage
% gain curve is chosen.
if sel == 1 && i == 1
    Vo_sel = Vo;
elseif sel == 2 && i == 2
    Vo_sel = Vo;
elseif sel == 3 && i == 3
    Vo_sel = Vo;

100
elseif sel == 4 && i == 4
    Vo_sel = Vo;
elseif sel == 5 && i == 5
    Vo_sel = Vo;
elseif sel == 6 && i == 6
    Vo_sel = Vo;
end

if (i == loop_count) % ensuring the loss computation at the
    last iteration
% Compute the currents in the DC–DC VIRT system based on FHA for
% selected input voltage (Vin)
    Im_rms = 2*sqrt(2)/pi*Np*Vo_sel./(fsw*2*pi*Lm*k_rec);
    Ioe = k_rec*pi*(Vo_sel)/Rload/(sqrt(8)*Np);
    Ir = sqrt(Im_rms.^2 + Ioe.^2);
    Ioe_prime = Ioe*Np;

% Plot the computed currents for the selected input voltage (Vin)
    yyaxis right
    if sel == 1
        plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 120 V)', 'LineStyle','-');
        plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 120 V)', 'LineStyle','-');
    elseif sel == 2
        plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 140 V)', 'LineStyle','-');
        plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 140 V)', 'LineStyle','-');
elseif sel == 3
    plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 170 V)', 'LineStyle', '-');
    plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 170 V)', 'LineStyle', '-');
elseif sel == 4
    plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 310 V)', 'LineStyle', '-');
    plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 310 V)', 'LineStyle', '-');
elseif sel == 5
    plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 340 V)', 'LineStyle', '-');
    plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 340 V)', 'LineStyle', '-');
elseif sel == 6
    plot(fsw/1000, Im_rms, 'DisplayName', 'I_{m-rms} (V_{in} = 380 V)', 'LineStyle', '-');
    plot(fsw/1000, Ir, 'DisplayName', 'I_{r-rms} (V_{in} = 380 V)', 'LineStyle', '-');
end

ylabel('Current [A]');
grid on;
grid minor;
end
% Setting the parameters for the plot with the voltage gain and currents curves
xlabel('Switching frequency, f_{sw} (kHz)')
legend('Location','bestoutside')
tlt = title(['Q_{e} = ' num2str(round(Qe,4)) ' L_{m} = ' num2str(round(Lm*1e6, 2)) ' uH, L_{r} = ' num2str(round(Lr*1e6, 3)) ' uH, C_{r} = ' num2str(round(Cr*1e9, 3)) ' nF, f_{res} = ' num2str(round(fo/1000)) ' kHz, N_{p} = ' num2str(Np) ' turns, V_{out} = ' num2str(Vout_desired) ' V'])
tlt.FontSize = 15;
set(gca, 'FontSize', 28);
set(findall(gca, 'Type', 'Line'),'LineWidth',1.5);
set(gca, 'FontName', 'Times New Roman');
hold off;
fig1=figure(1);
fig1.Renderer='Painters';

% save the plot as a pdf
set(gcf, 'PaperPosition', [0 0 25 10]);
set(gcf, 'PaperSize', [25 10]);
print('VIRT_current_curves','-dpdf','-fillpage')

% Plotting the system losses on an additional figure
figure;
for i = 1:1:loop_count
% Ceq chosen based on EPC2050 datasheet at each Vin
if i == 1
    Vin = 120;
end
invMode = 0;
Ceq = 186e-12;

elseif i == 2
Vin = 140;
invMode = 0;
Ceq = 176e-12;

elseif i == 3
Vin = 170;
invMode = 0;
Ceq = 152e-12;

elseif i == 4
Vin = 310;
invMode = 1;
Ceq = 159e-12;

elseif i == 5
Vin = 340;
invMode = 1;
Ceq = 155e-12;

elseif i == 6
Vin = 380;
invMode = 1;
Ceq = 140.5e-12;

end

V_{LLC\_eff} = Vin\times Minv;
ncap = 4; \# of device cap charged/discharged in each cycle.
To be used for ZVS II curve

```matlab
else
    
    Minv = 0.25;
    V_LLC_eff = Vin*Minv;
    ncap = 2;

    if VIRTmode == 0
        Rload = 1;
        Vout_desired = 5;
        Re = 32*Np^2/pi^2*Rload;
        k_rec = 1/2;
    elseif VIRTmode == 1
        Rload = 2.25;
        Vout_desired = 9;
        Re = 8*Np^2/pi^2*Rload;
        k_rec = 1;
    elseif VIRTmode == 2
        Rload = 5;
        Vout_desired = 15;
        Re = 2*Np^2/pi^2*Rload;
        k_rec = 2;
    elseif VIRTmode == 3
        Rload = 8;
        Vout_desired = 20;
        Re = 2*Np^2/pi^2*Rload;
        k_rec = 2;
    end

    % Series resonant frequency
```
% Based on the selected voltage input (Vin), corresponding output voltage

% Plot voltage gain curves
[Mz1, fn, Mg, fsw, Vo] = VIRTvoltageGainPlotter(fo, f_min, f_max, Ln, Qe, V_LL eff, i, Np, Lr, Lm, Cr, Re, VIRTmode, loop_count, k_rec);

fsw = linspace(f_max, f_min, 10000);

% Based on the selected voltage input (Vin), corresponding output voltage
% gain curve is chosen.
if sel == 1 && i == 1
    Vo_sel = Vo;
elseif sel == 2 && i == 2
    Vo_sel = Vo;
elseif sel == 3 && i == 3
    Vo_sel = Vo;
elseif sel == 4 && i == 4
    Vo_sel = Vo;
elseif sel == 5 && i == 5
    Vo_sel = Vo;
elseif sel == 6 && i == 6
    Vo_sel = Vo;
end
Plot ZVS II boundary (ensuring sufficient inductive energy in the system to charge/discharge Cds)

\[ \text{kinv} = 1/2; \quad \% \text{A scaling factor to calculate the actual voltage across the device capacitance} \]

\[ \text{outZVS} = \sqrt{\text{ncap} \times \text{Ceq} \times (\text{kinv} \times \text{Vin})^2 / (\text{Lm} + \text{Lr})} \times 2 \times \pi \times (2) \times \text{fsw} \times \text{Lm} \times \text{k_rec} / (4 \times \text{Np}); \]

if \( i = 1 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 120 V ZVS II','Color','k', 'LineStyle',':')}; \]

elseif \( i = 2 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 140 V ZVS II','Color','b', 'LineStyle',':')}; \]

elseif \( i = 3 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 170 V ZVS II','Color','c', 'LineStyle',':')}; \]

elseif \( i = 4 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 310 V ZVS II','Color','g', 'LineStyle',':')}; \]

elseif \( i = 5 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 340 V ZVS II','Color','m', 'LineStyle',':')}; \]

elseif \( i = 6 \)

\[ \text{plot(fsw/1000, outZVS,'DisplayName', 'V_{in} = 380 V ZVS II','Color','r', 'LineStyle',':')}; \]

end

if \( i == \text{loop_count} \) \% ensuring the loss computation at the last iteration

\% Compute the currents in the DC–DC VIRT system based on FHA for the
% selected input voltage (Vin)
\[
\text{Im}_{\text{rms}} = \frac{2\sqrt{2}}{\pi N_p} \frac{V_{\text{sel}}}{f_{\text{sw}} (2\pi L_m k_{\text{rec}})};
\]
\[
I_{\text{oe}} = k_{\text{rec}} \pi \frac{V_{\text{sel}}}{R_{\text{load}} (\sqrt{8} N_p)};
\]
\[
I_{r} = \sqrt{\text{Im}_{\text{rms}}^{\cdot2} + I_{\text{oe}}^{\cdot2}};
\]
\[
I_{\text{oe}}' = I_{\text{oe}} N_p;
\]

%% Loss calculation

% Conduction/capacitor loss
\[
P_{\text{cond pri}} = 2 R_{d_{s pri}} I_{r}^{\cdot2};
\]
\[
\text{if } \text{VIRTmode} == 0 \% FB/FB mode
\]
\[
P_{\text{cond sec}} = 4 R_{d_{s sec}} I_{\text{oe}}'^{\cdot2};
\]
\[
P_{\text{sec coss}} = 0.5 f_{\text{sw}} \text{Cross}^{\cdot}(V_{\text{sel}}^{\cdot2})^{\cdot8};
\]
\[
\text{elseif } \text{VIRTmode} == 1 \% FB/bypass mode
\]
\[
P_{\text{cond sec}} = 2 R_{d_{s sec}} I_{\text{oe}}'^{\cdot2} + 2 R_{d_{s gan}} I_{\text{oe}}'^{\cdot2};
\]
\[
P_{\text{sec coss}} = 0.5 f_{\text{sw}} \text{Cross}^{\cdot}(V_{\text{sel}}^{\cdot2})^{\cdot4};
\]
\[
\text{else } \% HB/bypass mode
\]
\[
P_{\text{cond sec}} = 2 R_{d_{s sec}} I_{\text{oe}}'^{\cdot2} + 2 R_{d_{s gan}} I_{\text{oe}}'^{\cdot2};
\]
\[
P_{\text{sec coss}} = 0.5 f_{\text{sw}} \text{Cross}^{\cdot}(V_{\text{sel}}^{\cdot2})^{\cdot2};
\]
end

% Copper loss
% Rac_primary (LitzOpt) and Rac_secondary (M2Spice) are
% computed at three different frequencies within the
% operating
% range and added together using a linear curve-fitting method
% at every
% frequency over the operating frequency range
% Primary side : Litz (48 AWG / 180 strands, 12 turns)
% Secondary side: 1 oz, 8 layers of PCB trace connected in parallel
fsw1 = fsw(1:7829); % 3.6 MHz ~ 860 kHz
fsw2 = fsw(7830:10000); % 860 kHz ~ 100 kHz
Ir1 = Ir(1:7829); Ir2 = Ir(7830:10000);

% Rac primary and Rac secondary at 680 kHz (1), 990 kHz (2), and 1.3 MHz (3)
f1 = 680e3; f2 = 990e3; f3 = 1300e3;
Rp1 = 0.130838634*Np/22*1.10; Rp2 = 0.130838634*Np/22*1.296;
Rp3 = 0.130838634*Np/22*2;
Rs1 = 0.21868; Rs2 = 0.262416; Rs3 = 0.37488;

% Linear curve-fitting method
slopel = (Rp3 - Rp2)/(f3 - f2);
Rac_pril = slopel*fsw1 + (Rp3 - slopel*f3);
slope2 = (Rp2 - Rp1)/(f2 - f1);
Rac_pri2 = slope2*fsw2 + (Rp2 - slope2*f2);

slopes = (Rs3 - Rs2)/(f3 - f2);
Rac_secl = slopes*fsw1 + (Rs3 - slopes*f3);
slope2s = (Rs2 - Rs1)/(f2 - f1);
Rac_sec2 = slope2s*fsw2 + (Rs2 - slope2s*f2);

Rac1 = Rac_pril + Rac_secl;
Rac2 = Rac_pri2 + Rac_sec2;

Pcopper1 = (Ir1.^2).*Rac1; Pcopper2 = (Ir2.^2).*Rac2;
Pcopper = [Pcopper1 Pcopper2];
Core loss calculation (square-wave excitation assumption)

MAGNETICS OPTIONS

CORE SETS

% [Ae(mm^2), Ve(mm^3), inner_post_diameter(mm), outer_diameter
(mm), Rth (degC/W) ]

% All linear dimensions in mm, mm^2, mm^3. Rth in degC/W

EQ13_PLT = [19.8, 315, 5, 11.2, 116];
EQ20_PLT = [59.8, 1500, 8.8, 18, 61];
EQ25_PLT = [89.7, 2370, 11, 22, 33];
EQ30_PLT = [108, 3910, 11, 26, 26];
EQ38_PLT = [148, 6190, 14, 33.1, 20];
EILP43_14_28 = [229, 11500, 8.1, 35.4, 17]; % Crudely
estimating it as having circular winding window

%CORE_MATERIAL = [k, alpha, beta] @ 100 degC
FERROXCUBE_3F35 = [1.12e-7, 2.1952, 2.7199];
FERROXCUBE_3F36 = [1.12e-7, 2.1952, 2.7199];
FERROXCUBE_3F45 = [2e-2, 1.29, 2.75];
EPCOS_N49 = [5.9899e-3, 1.3813, 2.7746];

CORESET_CHOICE = EQ20_PLT;
CORE_MATERIAL = FERROXCUBE_3F36;

desiredCoreMaterial = num2cell(CORE_MATERIAL);
[k, alpha, beta] = deal(desiredCoreMaterial{:});

desiredCoreSet = num2cell(CORESET_CHOICE);
[Ae, Ve, inner_post_diam, outer_diam, Rth] = deal(
    desiredCoreSet{:});
% Scaling factor for the effective voltage across the secondary-side transformer ports
Vo_eff_xfmr = Vo_sel/k_rec;

Core_Area_factor = 1; % 1 for effectively utilizing full area of the core
Core_Volume_factor = 2; % 2 for a EE core shape
Bpk = Vo_eff_xfmr./(4.*fsw.*Core_Area_factor*Ae*1e-6); % [T], assumes square wave excitation
A = 4.*fsw.*Core_Area_factor;
Pcore_density = k * fsw.^alpha .* Bpk.^beta;
Pcore = Pcore_density.*Core_Volume_factor*10^-6.*Ve;

% Configuring the system losses
Pxformer = Pcore + Pcopper;
Pcond = Pcond_pri + Pcond_sec;
Ptotal = Pcond + Pxformer + Psec_coss;

% Plot the system losses
yyaxis right
if sel == 1
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 120 V)','LineStyle','-');
    plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 120 V)','LineStyle','-.');
    plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 120 V)','LineStyle','-');
elseif sel == 2
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 140 V)','LineStyle','-');
plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 140 V)','LineStyle','-.');
plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 140 V)','LineStyle','-');

elseif sel == 3
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 170 V)','LineStyle','--');
    plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 170 V)','LineStyle','-.');
    plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 170 V)','LineStyle','-');
elseif sel == 4
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 310 V)','LineStyle','--');
    plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 310 V)','LineStyle','-.');
    plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 310 V)','LineStyle','-');
elseif sel == 5
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 340 V)','LineStyle','--');
    plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 340 V)','LineStyle','-.');
    plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 340 V)','LineStyle','-');
elseif sel == 6
    plot(fsw/1000, Pxformer, 'DisplayName', 'P_{xformer} (V_{in} = 380 V)','LineStyle','--');
    plot(fsw/1000, Pcond,'DisplayName', 'P_{cond} (V_{in} = 380 V)','LineStyle','-.');
plot(fsw/1000, Psec_coss,'DisplayName', 'P_{coss}(sec) (V_{in} = 380 V)', 'LineStyle', ':');
plot(fsw/1000, Ptotal,'DisplayName', 'P_{total} (V_{in} = 380 V)', 'LineStyle', '-');

end

ylabel('Power Loss [W]');
grid on;
grid minor;
end

%% Setting the parameters for the plot with the voltage gain and currents curves
xlabel('Switching frequency, f_{sw} (kHz)')
legend('Location','bestoutside')
tlt = title(['Q_e' = num2str(round(Qe,4)) ' L_{m}' = num2str(round(Lm*1e6,2)) ' uH, L_{r}' = num2str(round(Lr*1e6, 3))...
' uH, C_{r}' = num2str(round(Cr*1e9, 3)) ' nF, f_{res}' = '
num2str(round(fo/1000)) ' kHz, N_{p}' = num2str(Np) ' turns,
V_{out}' = num2str(Vout_desired) ' V'])
tlt.FontSize = 15;

set(gca, 'FontSize', 28);
set(findall(gca, 'Type', 'Line'),'LineWidth',1.5);
set(gca, 'FontName', 'Times New Roman');
hold off;

fig1=figure(2);
fig1.Renderer='Painters';
Listing A.3: Output voltage gain plotter

function [Mz, fn, Mg, fsw_2, Vo ] = VIRTvoltageGainPlotter( fr, f_min, f_max, Ln, Qe, V_LLCEff, i, Np, Lr, Lm, Cr, Re, VIRTmode, loop_count, k_rec)

% This function plots the voltage gain curves of the DC-DC VIRT system
% built with a LLC resonant tank
% See (Designing a resonant LLC half-bridge power converter by Huang)
% Huang for more detailed explanations

% filename: VIRTvoltageGainPlotter.m
% Called by VIRT_SystemGain_ZVS.m and VIRT_system_loss.m

% Computing Mg (LLC gain) using Ln, fsw (normalized), and Qe
fsw = linspace(f_max,f_min,10000);
fn = fsw/fr;

A = (Ln+1).*fn.^2 - 1;
B = (fn.^2 - 1).*fn*Qe*Ln;
C = complex(A,B);
Mg = abs(Ln.*fn.^2./C);
% Compute Mz associated with ZVS Boundary I: a dividing line between
% the inductive Zin and capacitive Zin
lambda = 1/Ln;
Mz = fn./sqrt(fn.^2*(1+lambda)-lambda);
[val, ind] = max(Mz); % Put irrelevant Mz values at lower frequency range out of the plot window
Mz(ind:length(Mz)) = 200;

fsw_2 = fsw/1000; % Scale fsw by 1000 for simplifying xaxis unit (kHz)
Vo = Mg*V_LLC_eff*k_rec/Np;

% Plot output voltage gain curve at each input (Vin)
if (i == 1)
    plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 120 V','Color','k', 'LineStyle','-');
elseif (i == 2)
    plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 140 V','Color','b', 'LineStyle','-');
elseif (i == 3)
    plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 170 V','Color','c', 'LineStyle','-');
elseif (i == 4)
    plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 310 V','Color','g', 'LineStyle','-');
elseif (i == 5)
    plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 340 V','Color','m', 'LineStyle','-');
elseif (i == 6)
plot(fsw_2,Vo, 'DisplayName', 'V_{in} = 380 V', 'Color', 'r', 'LineStyle', '-');

end

hold on;
xlim([300 2600]); ylim([0 ceil(max(Vo))+2])
ylabel('Output Voltage, V_{out} (V)');
xlabel('Switching Frequency, f_{sw} (kHz)');

% Plotting the horizontal line for the desired output voltage
if i == loop_count
    if VIRTmode == 0 % 5 V (FB/FB) operation
        hline = refline([0 5]);
    elseif VIRTmode == 1 % 9 V (FB/bypass) operation
        hline = refline([0 9]);
    elseif VIRTmode == 2 % 15 V (HB/bypass) operation
        hline = refline([0 15]);
    elseif VIRTmode == 3 % 20 V (HB/bypass) operation
        hline = refline([0 20]);
    end

    hline.Color = 'k';
    hline.LineStyle = '-';
    hline.DisplayName = 'Vo desired';
end

end
Appendix B

Prototype Converter: Schematics, Layout, and Bill-of-Materials

B.1 VIRT prototype version 1

This prototype version includes the DC-DC VIRT system mainly covered in Chapter 2. The prototype is designed to handle dc input voltage between 120 and 380 V, which corresponds to ac peak of 85 $V_{rms}$ and 264 $V_{rms}$, respectively, and regulate the dc output voltage to any of 5 V (25 W rating), 9 V (35 W rating), and 12 V (36 W rating).
B.2 VIRT prototype version 2: Bypass Switch and Hybrid Transformer

This prototype version includes the DC-DC VIRT system with bypass switch and hybrid transformer mainly covered in Chapter 3 and 4. In this prototype, the DC-DC VIRT system consists of two boards: Board I (stacked half-bridge inverter) and Board II (LLC resonant tank and VIRT rectifier) The dedicated inverter board which contains a stacked half-bridge structure in Fig. B-8 - B-12 has been designed by Mike K. Ranjram (mranjram@mit.edu). Note that a half-bridge structure part of Board II is not utilized. In this prototype, the DC-DC VIRT system is designed to handle two ranges of the input voltage (120 - 170 V and 310 - 380 V) and regulate the output voltage, $V_{OUT}$, to 5 V (25 W rating), 9 V (36 W rating), 15 V (45 W rating), and 20 V (50 W rating), respectively.
Figure B-1: VIRT prototype v1: schematic sheet 1.
Figure B-2: VIRT prototype v1: schematic sheet 2.
Figure B-3: VIRT prototype v1: schematic sheet 3.
Figure B-4: VIRT prototype v1: layout layer 1 (115 mm x 70 mm).
Figure B-5: VIRT prototype v1: layout layer 2 (115 mm x 70 mm).
Figure B-6: VIRT prototype v1: layout layer 3 (115 mm x 70 mm).
Figure B-7: VIRT prototype v1: layout layer 4 (115 mm x 70 mm).
Table B.1: Bill of materials for the main components in VIRT prototype v1

<table>
<thead>
<tr>
<th><strong>Inverter</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>GS66504B (650 V / 15 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Resistors (Gate drivers)</td>
<td>High: 3 OHM 5% 1/16W 0402 Low: 1 OHM 5% 1/16W 0402</td>
</tr>
<tr>
<td>Bypass capacitors (Gate drivers)</td>
<td>1Uf 10V X6S 0402</td>
</tr>
<tr>
<td>Bootstrap capacitors (Gate drivers)</td>
<td>10UF 6.3V X6S 0402</td>
</tr>
<tr>
<td>Signal isolators</td>
<td>SI8610</td>
</tr>
<tr>
<td>Isolated power</td>
<td>ADUM5010</td>
</tr>
<tr>
<td>Balancer diodes</td>
<td>MMBD3004BRM</td>
</tr>
<tr>
<td>Balancer capacitors</td>
<td>10 uF (1812) / 450 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>VIRT Rectifier</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>EPC2023 (30 V / 60 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Resistors (Gate drivers)</td>
<td>0 OHM JUMPER 1/16W 0402</td>
</tr>
<tr>
<td>Bypass capacitors (Gate drivers)</td>
<td>1 uF 6.3 V X6S 0402</td>
</tr>
<tr>
<td>Bootstrap capacitors (Gate drivers)</td>
<td>1 uF 6.3 V X6S 0402</td>
</tr>
<tr>
<td>Blocking capacitors</td>
<td>22 uF (0805) / 16 V JB</td>
</tr>
<tr>
<td>Decoupling capacitors</td>
<td>10 uF (0508) / 16 V X5R per half-bridge</td>
</tr>
<tr>
<td>Output capacitors</td>
<td>22 uF (1210) / 16V X6S</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>LLC Resonant Tank</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant capacitor (split)</td>
<td>2 x 3.47 nF in series (1500 pF 630 V COG 0805 x 4 and 470 pF 450 V COG 0805 x 2)</td>
</tr>
<tr>
<td>Resonant inductors (split)</td>
<td>2 x 1.79 uH in series; ea. RM5I / 3F36, 3 turns 46 AWG / 180 Litz wire</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>VIRT Transformer</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>EQ20 + PLT/3F36, 0.006” gap on all legs</td>
</tr>
<tr>
<td>Primary windings</td>
<td>Six turns on Layer 3 and 4 connected in series, 0.019” trace width, 0.008” trace-to-trace spacing</td>
</tr>
<tr>
<td>Secondary windings</td>
<td>Two sets of half turns (one set each on layers 1 and 2) connected in parallel</td>
</tr>
<tr>
<td>PCB</td>
<td>2 oz, 4 layers, 0.063”, FR4, 0.025” separation between layers 2 and 3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>Control</strong></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller</td>
<td>TI TMS320F28379D</td>
</tr>
</tbody>
</table>
Figure B-8: VIRT prototype v2 Inverter Board: schematic sheet 1.
Figure B-9: VIRT prototype v2 Inverter Board: layout layer 1 (67 mm x 36 mm).
Figure B-10: VIRT prototype v2 Inverter Board: layout layer 2 (67 mm x 36 mm).
Figure B-11: VIRT prototype v2 Inverter Board: layout layer 3 (67 mm x 36 mm).
Figure B-12: VIRT prototype v2 Inverter Board: layout layer 4 (67 mm x 36 mm).
Figure B-13: VIRT prototype v2 LLC resonant tank and VIRT rectifier: schematic sheet 1.
Figure B-14: VIRT prototype v2 LLC resonant tank and VIRT rectifier: schematic sheet 2.
Figure B-15: VIRT prototype v2 LLC resonant tank and VIRT rectifier: schematic sheet 3.
Figure B-16: VIRT prototype v2 Inverter Board: layout layer 1 (107 mm x 47 mm).
Figure B-17: VIRT prototype v2 Inverter Board: layout layer 2 (107 mm x 47 mm).
Figure B-18: VIRT prototype v2 Inverter Board: layout layer 3 (107 mm x 47 mm).
Figure B-19: VIRT prototype v2 Inverter Board: layout layer 4 (107 mm x 47 mm).
Figure B-20: VIRT prototype v2 Inverter Board: layout layer 5 (107 mm x 47 mm).
Figure B-21: VIRT prototype v2 Inverter Board: layout layer 6 (107 mm x 47 mm).
Figure B-22: VIRT prototype v2 Inverter Board: layout layer 7 (107 mm x 47 mm).
Figure B-23: VIRT prototype v2 Inverter Board: layout layer 8 (107 mm x 47 mm).
Table B.2: Bill of materials for the main components in VIRT prototype v2.

<table>
<thead>
<tr>
<th>Stacked Half-Bridge Inverter</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN FETs</td>
<td>EPC2050 (350 V / 25 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Resitors (Gate drivers)</td>
<td>High: 3 OHM 5% 1/16W 0402</td>
</tr>
<tr>
<td></td>
<td>Low: 1 OHM 5% 1/16W 0402</td>
</tr>
<tr>
<td>Bypass capacitors (Gate drivers)</td>
<td>1UF 10V X6S 0402</td>
</tr>
<tr>
<td>Bootstrap capacitors (Gate drivers)</td>
<td>10UF 6.3V X6S 0402</td>
</tr>
<tr>
<td>Signal isolators</td>
<td>SI8610</td>
</tr>
<tr>
<td>Isolated power</td>
<td>ADUM5010</td>
</tr>
<tr>
<td>Balancer diodes</td>
<td>MMBD3004BRM</td>
</tr>
<tr>
<td>Balancer capacitors</td>
<td>10 uF (1812) / 450 V</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LLC Resonant Tank</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Resonant Capacitor</td>
<td>3.47 uF</td>
</tr>
<tr>
<td></td>
<td>(1500 pF 630 V COG 0805 x 2 and 470 pF 450 V COG 0805)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIRT Rectifier</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Rectifier switches</td>
<td>TPN2R703NL (30 V / 45 A)</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>LM5113</td>
</tr>
<tr>
<td>Resistors (Gate drivers)</td>
<td>0 OHM JUMPER 1/16W 0402</td>
</tr>
<tr>
<td>Bypass capacitors (Gate drivers)</td>
<td>1 uF 6.3 V X6S 0402</td>
</tr>
<tr>
<td>Bootstrap capacitors (Gate drivers)</td>
<td>1 uF 6.3 V X6S 0402</td>
</tr>
<tr>
<td>Bypass switches</td>
<td>EPC2023 (30 V / 90 A)</td>
</tr>
<tr>
<td>Gate driver (bypass)</td>
<td>UCC27611</td>
</tr>
<tr>
<td>Isolated power and digital signals (bypass)</td>
<td>ADUM5210</td>
</tr>
<tr>
<td>Blocking capacitors</td>
<td>22 uF (0805) / 35 V JB</td>
</tr>
<tr>
<td>Decoupling capacitors</td>
<td>25 uF (0508) / 25 V X5R per half-bridge</td>
</tr>
<tr>
<td>Output capacitors</td>
<td>22 uF (1210) / 25V X7R</td>
</tr>
</tbody>
</table>
Bibliography


[10] W. Inam, K. K. Afridi, and D. J. Perreault, “Variable frequency multiplier tech-


