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Video Article

Scanning-probe Single-electron Capacitance Spectroscopy

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Abstract

The integration of low-temperature scanning-probe techniques and single-electron capacitance spectroscopy represents a powerful tool to study the electronic quantum structure of small systems - including individual atomic dopants in semiconductors. Here we present a capacitance-based method, known as Subsurface Charge Accumulation (SCA) imaging, which is capable of resolving single-electron charging while achieving sufficient spatial resolution to image individual atomic dopants. The use of a capacitance technique enables observation of subsurface features, such as dopants buried many nanometers beneath the surface of a semiconductor material^{1,2,3}. In principle, this technique can be applied to any system to resolve electron motion below an insulating surface.

As in other electric-field-sensitive scanned-probe techniques⁴, the lateral spatial resolution of the measurement depends in part on the radius of curvature of the probe tip. Using tips with a small radius of curvature can enable spatial resolution of a few tens of nanometers. This fine spatial resolution allows investigations of small numbers (down to one) of subsurface dopants^{1,2}. The charge resolution depends greatly on the sensitivity of the charge detection circuitry; using high electron mobility transistors (HEMT) in such circuits at cryogenic temperatures enables a sensitivity of approximately 0.01 electrons/Hz^{1/2} at 0.3 K⁵.

Video Link

The video component of this article can be found at <https://www.jove.com/video/50676/>

Introduction

Subsurface Charge Accumulation (SCA) imaging is a low-temperature method capable of resolving single-electron charging events. When applied to the study of dopant atoms in semiconductors, the method can detect individual electrons entering donor or acceptor atoms, permitting characterization of the quantum structure of these minute systems. At its heart, SCA imaging is a local capacitance measurement⁶ well-suited for cryogenic operation. Because capacitance is based on electric field, it is a long-range effect that can resolve charging beneath insulating surfaces⁵. Cryogenic operation permits investigation of single-electron motion and quantum level spacing that would be unresolvable at room temperature^{1,2}. The technique can be applied to any system in which electron motion below an insulating surface is important, including the charging dynamics in two-dimensional electron systems at buried interfaces⁷; for brevity, the focus here will be on studies of semiconductor dopants.

At the most schematic level, this technique treats the scanned tip as one plate of a parallel-plate capacitor, although realistic analysis requires a more detailed description to account for the curvature of the tip^{8,9}. The other plate in this model is a nanoscale region of the underlying conducting layer, as shown in **Figure 1**. Essentially, as a charge enters a dopant in response to a periodic excitation voltage, it gets closer to the tip; this movement induces more image charge on the tip, which is detected with the sensor circuit⁵. Similarly, as the charge exits the dopant, the image charge on the tip is decreased. Hence the periodic charging signal in response to the excitation voltage is the detected signal - essentially it is capacitance; thus this measurement is often referred to as determining the C-V characteristics of the system.

During the capacitance measurement, the only net tunneling is between the underlying conductive layer and the dopant layer - charge never tunnels directly onto the tip. The lack of direct tunneling to or from the tip during the measurement is an important difference between this technique and the more familiar scanning tunneling microscopy, although much of the hardware for this system is essentially identical to that of a scanning tunneling microscope. It is also important to note that SCA imaging is not directly sensitive to static charges. For investigations of static charge distributions, scanning Kelvin probe microscopy or electrostatic force microscopy is appropriate. Additional cryogenic methods for examining local electronic behavior exist which also have good electronic and spatial resolution; for example, scanning single-electron transistor microscopy is another scanning probe method capable of detecting minute charging effects^{4,10}. SCA imaging was originally developed at MIT

by Tessmer, Glicofridis, Ashoori, and co-workers⁷; moreover, the method described here can be considered as a scanning probe version of the Single-Electron Capacitance Spectroscopy method developed by Ashoori and co-workers¹¹. A key element of the measurement is an exquisitely sensitive charge-detection circuit^{5,12} using high electron mobility transistors (HEMT); it can achieve a noise level as low as $0.01 \text{ electrons/Hz}^{1/2}$ at 0.3 K, the base temperature of the cryostat in Reference 5. Such a high sensitivity allows observation of single-electron charging in subsurface systems. This method is suited for the study of electron or hole dynamics of individual or small groups of dopants in semiconductors, with typical dopant areal densities on the order of 10^{15} m^{-2} in a plane geometry². An example of a typical sample configuration for this type of experiment is shown in **Figure 1**. The dopant layer is typically positioned a few tens of nanometers beneath the surface; it is important to know the precise distances between the underlying conducting layer and the dopant layer and between the dopant layer and the sample surface. In contrast to tunneling, capacitance does not fall off exponentially but instead essentially decreases in inverse proportion to the distance. Hence, the dopant depth could in principle be even deeper than tens of nanometers beneath the surface, as long as some reasonable fraction of electric field lands on the tip. For all of the aforementioned cryogenic local probes of electronic behavior, including the technique described here, spatial resolution is limited by the geometric size of the tip and by the distance between the subsurface feature of interest and the scanning probe tip.

Protocol

1. Protocol

1. Initial setup of microscope and electronics.
 1. Begin with a cryogenic-capable scanning probe microscope with associated control electronics. The microscopes used for the research described here use inertial translation to "walk" the sample towards and away from the tip along ramps¹³ (made from a conducting material such as copper, brass, or stainless steel to enable them to transmit bias voltage to the sample) as part of a Besocke design STM¹⁴, schematically shown in **Figure 2**.
 2. In addition to the bias voltage and tunneling current coaxial wires, provide at least two other coaxial wires and a ground wire which extend from the electronics rack to near the tip area of the microscope in order to operate the cryogenic amplifier circuit for sensitive charge detection. Assemble the elements of the amplifier circuit, described in detail in References 5, 12, and 15, that are housed on the electronics rack; this is the portion of the circuit outside the shaded box in **Figure 2**. This part of the circuit will remain at room temperature throughout the experiment.
2. Assemble the mounting chip for the tip and HEMT circuit (shaded box in **Figure 2**); the HEMT circuit will be lowered to cryogenic temperature to obtain optimal energy resolution.
 1. Cleave a square chip sized approximately 1 cm x 1 cm from a GaAs wafer using a scribe; the sensor circuit and tip will be mounted on this chip. Deposit approximately 100 nm of gold atop a titanium sticking layer through a shadowmask onto the GaAs chip to form several gold pads, each sized approximately 1 mm x 1 mm, to which wires from the HEMT and biasing resistor will be bonded. The dimensions of the pads are not critical.
 2. Prepare a sharp STM tip by mechanically cutting an 80:20 Pt:Ir wire using diagonal cutters. The tip can also be prepared by chemical etching or another method or can be purchased commercially. Determine the radius of curvature of the tip via scanning electron microscopy; the radius of curvature should be on the order of the spatial resolution needed for the experiment.
 3. Epoxy a gold wire onto each of the gold pads using conductive epoxy capable of withstanding cryogenic temperatures; these wires will connect the elements of the circuit on the mounting chip to the coaxial wires on the microscope. Since the gold wires can be easily removed after the next step if they are not needed, epoxy a few redundant gold wires onto the pads. Epoxy the HEMT, the biasing resistor, and the STM tip onto the GaAs mounting chip. Cure the epoxy as indicated on its product information sheet. (See the table of materials below for details.)
 4. Using a wire bonder loaded with gold wire, bond the source, drain, and gate elements of the HEMT to separate gold pads on the GaAs chip. Bond temporary wires connecting the gate and source or drain pads to ensure the gate does not become charged with respect to the source-drain channel. Use a grounding strap for added safety while manipulating the HEMT; it is important to take precautions to avoid introducing stray static charges that could destroy the HEMT.
 5. Store the prepared mounting chip with the wires attached to the gate and to the source-drain channel of the HEMT electrically connected to each other to avoid shorting the HEMT. If the temporary wires mentioned in the previous step have been removed, gently twist the wires together. It is simplest to connect all the wires to one another.
3. Attach the mounting chip to the microscope.
 1. Ensure that the gate and source-drain channels are never floating; this is to prevent destructive shorts between the gate and source-drain channels of the HEMT. Ground the coaxial wires on the microscope to which the wires from the chip will be soldered.
 2. Affix the mounting chip atop the scanning piezotube, as shown in **Figure 2**.
 3. Solder the gold wires extending from the mounting chip to the pertinent coaxial wires using indium solder.
4. Check the integrity of the HEMT using a curve tracer connected to the coaxial wires at the electronics rack. Essentially, the curve tracer shows the source-drain current-voltage characteristics. The most common failure mode is a short between the HEMT gate and its source-drain channel, which results in source-drain characteristics which are insensitive to gate voltage.
5. Mount the sample. Walk into range with the microscope configured in STM mode to ensure that the sample will successfully approach the tip.
 1. Connect wire T to the preamplifier used for STM tunneling current measurements, and attach DC bias voltage V_{DC} to wire B. (All connections are made at the electronics rack.)
 2. Walk in until the sample and tip are in tunneling range. When in range, the scanning piezotube should remain extended slightly from its equilibrium position so that grounding the scanning piezotube will cause the tip to retract from its in-range extension. This verifies that the sample can successfully approach the tip. Walk out of range after doing this, to protect the tip during the next actions.
 3. Transfer the microscope from the laboratory benchtop to the dewar for eventual low-temperature operation. At this point, the testing phase is complete and the experimental phase can begin.

6. Pump out the microscope to a vacuum of a few microtorr. Cool the microscope to 4.2 K or below for optimum energy resolution, following the procedure outlined in the manual for the cryostat.
 1. After cooling the microscope to its base temperature, allow the microscope sufficient time to reach thermal equilibrium; since repeated, lengthy scans of the same area will be performed, it is important to minimize thermal drift. (Drift is a shift in the equilibrium position of the tip with respect to the sample.)
 2. Suspend the dewar to isolate the microscope as much as possible from vibrations due to mechanical coupling to the building and to vacuum pumps and other devices attached to the microscope and dewar. This can be done using a bungee cord suspension system, as in Reference 15, or by using air springs or a similar method.
7. After cooling the microscope and before attempting data collection, verify the integrity of the HEMT again using the curve tracer.
8. Scan the sample in tunneling (STM) mode.
 1. Walk into range. Locate a region of the sample surface which is free from debris and from substantial height or conductivity variations, and ensure the tip is stable.
 2. Correct for any tilt of the sample; this is especially important because capacitance scans will be performed with the feedback loop disabled, thus the tip could crash into the surface if the scanning plane is not parallel to the surface of the sample. In principle, one could use the capacitance signal with feedback to maintain a constant capacitance while scanning the tip; however, in practice, the signal is not sufficiently robust to prevent a crash if feedback is used.
 3. Observe any thermal drift so that it can be compensated for by repositioning the tip offset. Note the amount of extension of the tip while in range in tunneling mode, referred to in this protocol as the touch point.
9. Move to an unperturbed area of the sample, one which was not scanned in STM mode.
 1. Disable the feedback loop in the STM controller. Recall that when the feedback loop is disabled, manual motions of the tip could inadvertently cause a crash. Great care should therefore be taken while moving the tip.
 2. Retract the tip a few tens of nanometers from the touch point.
 3. Offset the lateral position of the tip to a nearby area of the sample which has not recently been scanned, to avoid any perturbations (such as charging of semiconductor dopant sites) the bias voltage required to enable tunneling through the semiconducting sample for STM scanning may have induced.
 4. Cautiously extend the tip toward the surface until the tip displacement from equilibrium extension is close in magnitude to the touch point.
10. Switch wiring configuration to capacitance mode.
 1. Ground all coaxial wires to protect the HEMT.
 2. Connect the coaxial wires to the relevant voltage sources and resistors and to the lock-in amplifier and the function generator, as shown in **Figure 2**.
 3. Turn on all voltage sources. To avoid shocking the HEMT, begin with voltage source outputs at 0 V.
 4. Unground the coaxial wires, remembering to keep the gate and the source-drain channel of the HEMT connected to each other as long as possible in order to protect the HEMT.
 5. Set the voltage source on the voltage divider resistor (wire D).
 6. Tune the HEMT to its most sensitive region by monitoring the voltage across wire L with a multimeter while adjusting V_{tune} . Reattach wire L to the lock-in amplifier afterwards.
 7. Increase V_{tune} until the in-phase signal on the lock-in amplifier increases and begins to plateau; record this value of V_{tune} , which is the voltage applied to the tip. This enables all charge from the measurement to go to the HEMT instead of leaking through wire L.
 8. Optimize the internal phase of the lock-in amplifier using its autophase ability and record the phase value.
 9. Wait for the HEMT to stabilize to ensure there are no significant thermal effects (this often takes up to two hours).
11. Balance the HEMT by adjusting the signal on the standard capacitor to ensure that only the signal of interest goes to the lock-in amplifier. Adjustments of the signal on the standard capacitor can be done either to the amplitude of V_{balance} or to the relative phase between V_{balance} and $V_{\text{excitation}}$. The HEMT is considered balanced when the in-phase signal on the lock-in amplifier is minimized at this step of the procedure.
12. Perform scanning charge accumulation imaging.
 1. Set the DC bias voltage V_{DC} on the sample.
 2. Extend the tip to within 1 nm of the surface, using the touch point as reference.
 3. Record the output of the lock-in amplifier using the data acquisition software; this is the signal of interest.
 4. Scan the sample. To obtain good resolution, the scans may need to be acquired at the rate of several hours per scan to allow sufficient signal averaging for each pixel and to prevent smearing of the signal across adjoining pixels of the image. Perform several scans over the same area, and average these scans together to improve the signal-to-noise ratio.
13. Perform capacitance (C-V) spectroscopy with the tip stationary above a subsurface feature of interest in the charge accumulation image acquired during the previous step.
 1. Ramp V_{DC} and record the output of the lock-in amplifier using the data acquisition software.
 2. Take several capacitance vs. voltage (C-V) curves in the same location, and average these curves together to improve the signal-to-noise ratio. Typically, a few curves are averaged together. While averaging curves improves the signal-to-noise ratio, because of the potential for drift during scans, only a handful of successive scans should be averaged together.
14. Return to tunneling (STM) mode.
 1. Retract the tip to its equilibrium extension and reconfigure the electronics for STM. Re-enable the feedback loop and record the present in-range extension of the tip (touch point).
 2. Scan the area in tunneling mode to look for features in the topography which may have generated artifacts in the capacitance imaging and capacitance spectroscopy.
15. Analyze and interpret data, following Reference 9 and the supporting information in Reference ¹.

Representative Results

The chief indicator of a successful measurement is reproducibility, much as in other scanning probe methods. Repeated measurements are very important for this reason. For point capacitance spectroscopy, taking many measurements in succession at the same location helps to increase the signal-to-noise ratio and identify spurious signals.

Once a feature of interest has been identified within the charge accumulation image and capacitance spectroscopy has been performed, interpretation of the C-V data begins by determining the voltage lever arm. The voltage lever arm is the scale factor relating the actual potential at the location of the dopant to the applied V_{DC} . It essentially accounts for the nonzero distance of the tip from the dopant layer and for any lateral offset of the dopant from the position directly beneath the tip. The voltage lever arm is found by fitting a Lorentzian function to the C-V spectroscopy data^{1,8}. If an absolute voltage scale is desired, the contact potential (voltage at which no electric field lines from the sample terminate at the tip) should be determined via a Kelvin probe measurement^{1,2,3,7}.

Figure 3(a) shows an example of a charge accumulation image with C-V spectroscopy acquired at the indicated point. The sample was silicon, doped with boron acceptors with an areal density of $1.7 \times 10^{15} \text{ m}^{-2}$ in a delta-doped layer 15 nm below the surface. Brighter colors indicate increased charging. The bright spots are interpreted as marking the location of individual subsurface boron atoms. The blue dot indicates a particular bright spot where point C-V spectroscopy was performed¹, as shown in **Figure 3(b)**. The largest peak is interpreted to be charge entering the dopant directly below the tip. Nearby peaks are due to nearby dopants. Their centers are shifted and amplitudes decreased with respect to the main peak because the increased distance of these dopants from the tip changes their lever arm parameters. The peaks are broadened along the voltage axis by essentially four effects: (1) the lever arm, (2) thermal broadening, (3) the amplitude of the excitation voltage, and (4) the output filter of the lock-in amplifier. These effects are accounted for in the model, as shown by the good agreement between the overlaid model curve¹ and the data.

Figure 4(a) shows a series of charging peaks, similar to **Figure 3(b)**. In this case, the sample was GaAs, doped with silicon donors with an areal density of $1.25 \times 10^{16} \text{ m}^{-2}$ in a delta-doped layer 60 nm below the surface. Due to the high dopant density, most of the spectroscopic features in this experiment reflect groups of many electrons. Peaks are identified by fitting; interpretation of a peak as being attributable to a single electron comes from its consistency in shape and magnitude with the expected form of a single-electron peak. A handful of single-electron peaks were resolved in this experiment², one of which is indicated by the red arrow. **Figure 4(b)** and **4(c)** focus on this peak, showing that it has the expected shape for a single-electron effect. The fit in **Figure 4(c)** is a half-ellipse¹⁶ convolved with functions accounting for the peak-broadening effects described above. This fit has two free parameters: the center of the peak and the lever arm. The three C-V curves in **Figure 4(b)** are sequential spectroscopy measurements on the same feature. The amount of scatter in the data in **Figure 4(b)** is typical; averaging several curves together, as is done in **Figure 4(a)**, results in more easily-identifiable peak structure, which is why doing multiple C-V curves on the same feature is very important for improving the signal-to-noise ratio.

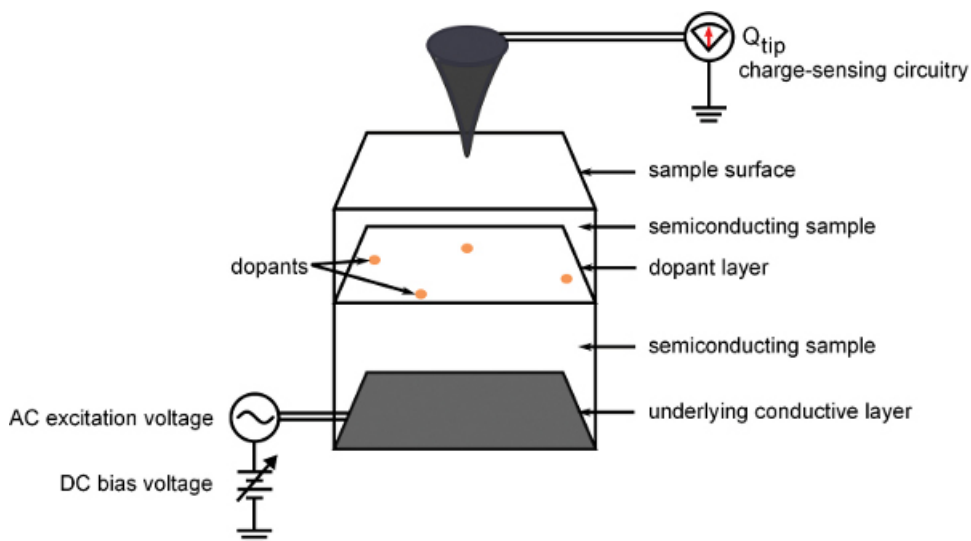


Figure 1. Schematic of a Typical Sample. Schematic of a typical sample for scanning-probe single-electron capacitance experiments. The sample is a semiconductor with an underlying conducting layer at a known depth from the surface to which the bias and excitation voltages are applied. A two-dimensional layer of dopants is embedded, also at a known depth from the surface. Electrons tunnel between the conducting layer and the dopant layer, changing the capacitance of the system and inducing an image charge in the tip which is measured by the charge-sensitive apparatus. A sufficiently high bias voltage will enable electrons to tunnel between the dopant layer and a surface state as well, enabling their detection at the surface by STM.

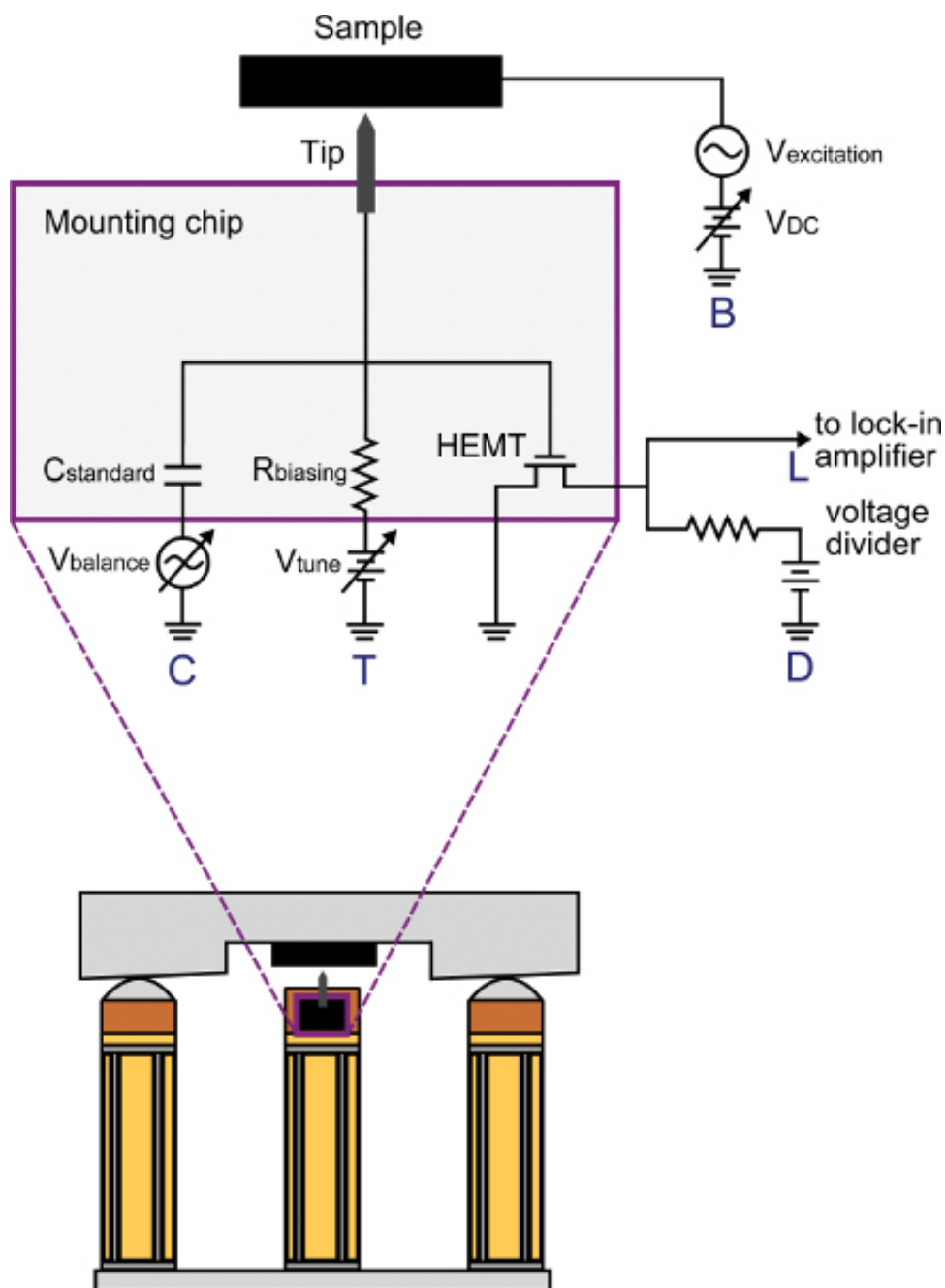


Figure 2. Schematic of Microscope and Charge-sensing Apparatus. Circuit diagram for the amplifier described in Reference 5 and based on Reference 12. Mounting chip is shown in place on a schematic of a Besocke-design¹⁴ scanning probe microscope with ramps¹³ and sample (not to scale). Wire B provides the sample bias voltage, including the AC excitation voltage used to incite tunneling to and from subsurface dopants. Wire C is connected to the standard capacitor and the tunable AC voltage source that permits balancing of the HEMT. Wire L connects to the lock-in amplifier from which the capacitance signal is recorded, and wire D connects to a voltage source through a resistance to create a voltage divider; the output of the voltage divider is the signal sent to the lock-in amplifier. During capacitance measurements, wire T is connected to an adjustable voltage source through a large resistor to prevent AC charge on the tip from leaking down this pathway. In tunneling (STM) mode, wire T becomes the tunneling current wire (with its voltage source disconnected), wire B remains connected to a DC voltage source, and all other wires are grounded. A typical choice for the voltage divider resistance on wire D is 100 k Ω with a voltage on wire D of +1.25 V. The choice of standard capacitance should counteract the background tip-sample mutual capacitance, which is approximately 20 fF. The biasing resistor on wire T should be in the neighborhood of 20 M Ω . These choices aim to tune the resistance of the HEMT source-drain channel to its most sensitive regime.

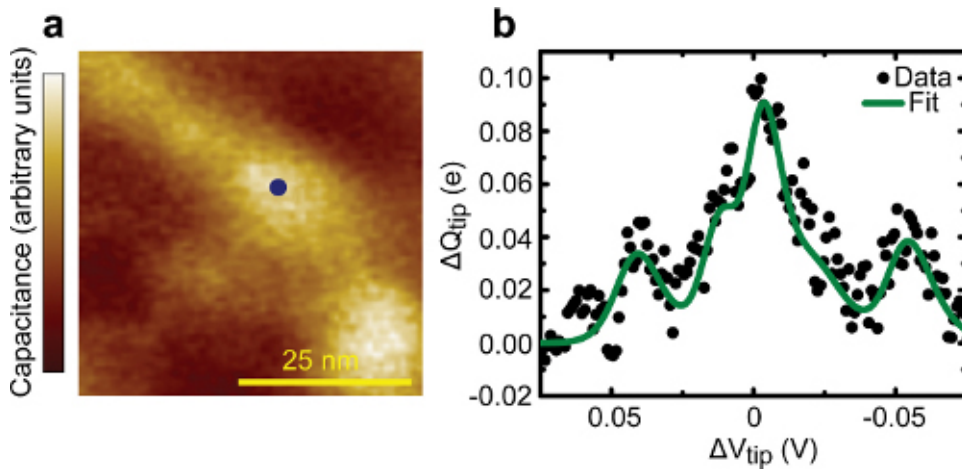


Figure 3. SCA Image and C-V Spectroscopy on Acceptor-doped Si. (a) Scanning charge accumulation image of a silicon sample doped with a layer of boron acceptors of areal density $1.7 \times 10^{15} \text{ m}^{-2}$ located 15 nm below the surface¹; $V_{\text{DC}} = 75 \text{ mV}$, $V_{\text{excitation}} = 3.7 \text{ mV}$; the temperature was 4.2 K. (b) C-V spectroscopy acquired at the point in (a) indicated by the blue dot. To focus on the peak structure, a background line was subtracted. The voltage scale has been shifted so that zero is the center of the largest peak; since no Kelvin probe measurement was done during this experiment to determine the absolute voltage scale, this offset is a matter of convenience.

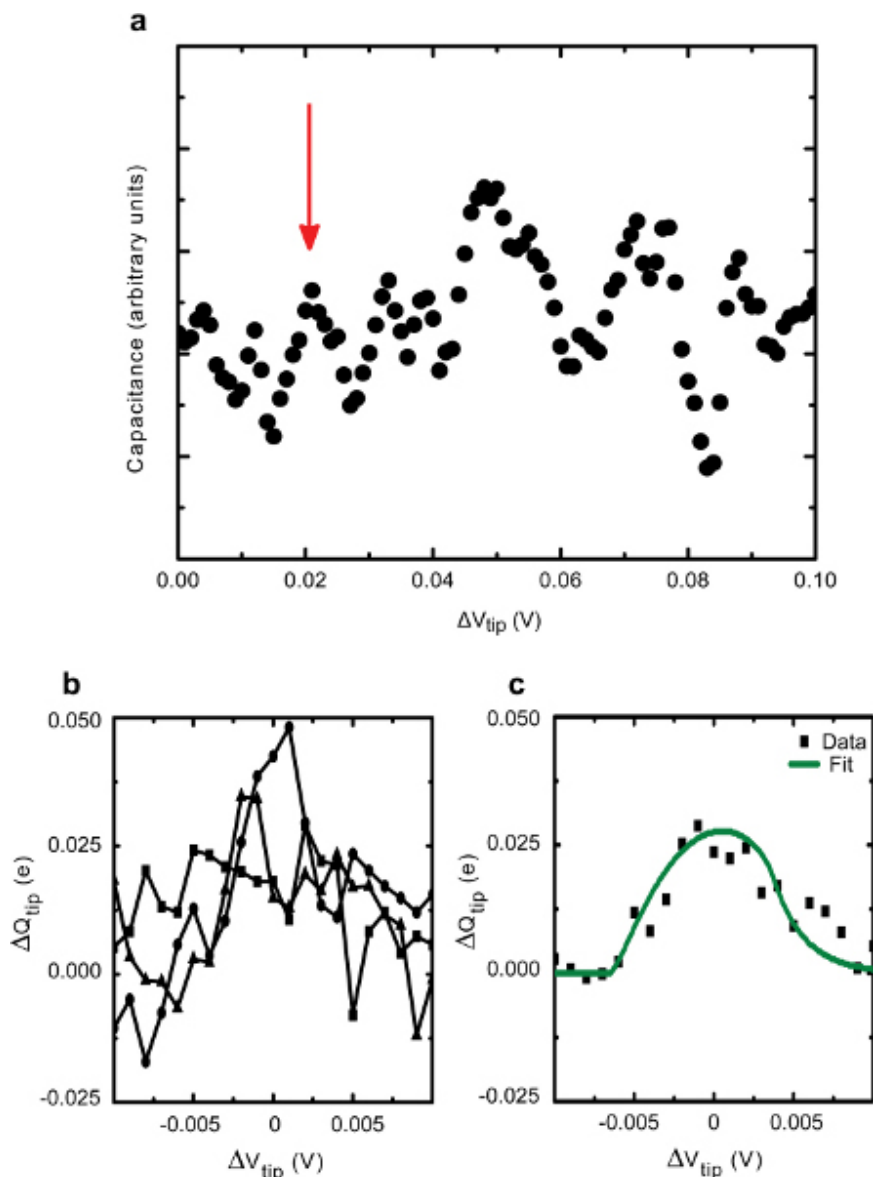


Figure 4. C-V Spectroscopy Analysis on Donor-doped GaAs. (a) C-V spectroscopy acquired on GaAs, doped with a layer of silicon donors of areal density $1.25 \times 10^{16} \text{ m}^{-2}$ located 60 nm below the surface²; $V_{\text{excitation}} = 15 \text{ mV}$; the temperature was 0.3 K. The red arrow marks a peak which was further investigated. (b) More detailed individual C-V spectroscopy measurements of the indicated peak in (a) with the voltage centered on the peak; $V_{\text{excitation}} = 3.8 \text{ mV}$. (c) Averaged data of the multiple curves shown in (b). The fit, shown in green, accounts for four effects that broaden the peak: the lever arm, thermal broadening, the amplitude of the excitation voltage, and the output filter of the lock-in amplifier. In (b) and (c), the charging signal detected on the tip is plotted on the ordinate axis; unlike in (a), the conversion to a capacitance value via $C = \Delta Q_{\text{tip}}/V_{\text{excitation}}$ has not been made.

Discussion

A detailed explanation of the theoretical basis for this experimental method is given in References 8 and 9 and discussed with respect to the scenario of subsurface dopants in Reference 2; the overview presented here will therefore be brief and conceptual. The tip is treated as one plate of a capacitor, and the conducting layer underlying the sample comprises the other plate. If the DC voltage is applied such that electrons are pulled toward the tip, and if there is a dopant atom situated between the underlying conducting layer and the tip that can accommodate an additional charge, then the electron will enter the dopant and hence get closer to the tip. From electrostatics, the movement of this electron must induce an image charge of the opposite sign on the tip. The sinusoidal excitation voltage ($V_{\text{excitation}}$) that is summed into the DC voltage will cause the electron to resonate between the substrate layer and the dopant. In turn, the image charges will also resonate, giving an AC signal which is detected by the sensitive charge-detection circuitry utilizing the HEMT and further amplified with a lock-in amplifier. This charging signal can then be converted into a capacitance.

The most common failure mode of this experiment involves damage to the HEMT circuit that enables the sensitive charge detection. Since the HEMT gate is so small, even a small static charge buildup can cause a failure of the HEMT, usually in the form of a short between the source-drain channel and the gate. If a HEMT is shorted, the single-electron capacitance measurement cannot continue without replacing it. Since an

appreciable amount of time is generally spent in preparing the experiment, particularly in cooling the microscope down to its base temperature, HEMTs used for these experiments should be protected by ensuring that the gate and source-drain channels are never floating, either by connecting these leads to each other (when working with the small gold wires on the chip) or by grounding them (when working with the coaxial wire connections). Extra precautions can be taken by wearing a grounding strap while handling the mounting chip or the microscope hardware, particularly in dry weather, as even mild static charge from the experimenter's person can ruin a HEMT either by outright shorting it or by causing it to trap charges in such a way that it never quite stabilizes. If in doubt about the health of the HEMT, one should use a curve tracer to look for the expected variations in the source-drain characteristics with applied gate voltage (often called the "fan").

The dimensions of the gold pads on the mounting chip are not of great importance, provided that they are large enough to permit successful wire bonding, yet much smaller than a millimeter to avoid coupling excess capacitance to the circuit. Before attaching the HEMT or tip, it may be useful to do a test bond elsewhere on the mounting chip to test how well bonding can be expected to work on that chip. Including a few extra gold pads on the mounting chip can also be useful in case part of the chip is more amenable to bonding than other regions on the chip. If the bonding process appears to be pulling swatches of gold off of the pad, the GaAs chip may not have been sufficiently clean before the metal layers were laid down or the gold may have deteriorated with age. Decreasing the ultrasonic power used on the wire bonder may be helpful in this case.

Indium solder is used to attach the gold leads to the coaxial wires because of its good properties at cryogenic temperatures. Similarly, GaAs is used as the material for the mounting chip to avoid causing a thermal-contraction-induced strain in the HEMT, which is itself fabricated on a GaAs substrate. Since GaAs is a piezoelectric material, a mechanical strain on the substrate could cause a short and consequent failure of the HEMT.

For the semiconductors used in the experiments in References 1 and 2, the sample surface could be imaged by using the system as an STM. That is to say, electrons could indeed tunnel directly onto the tip when the apparatus was configured in STM mode. This is very useful as it provides a way to bring the tip close to the sample without crashing the tip into the surface. A bias voltage on the order of a few to several volts is needed to establish a stable tunneling current. With a sufficiently high bias voltage, charges will be pulled from the underlying conducting layer across the insulating regions of the sample to form a conducting puddle of charge at the surface; this puddle will follow the tip as the tip is scanned. Hence the surface can be imaged just as in standard STM. Tunneling mode can cause electronic damage for subsequent measurements. For example, the potential exists for the sample to be affected by the large bias voltages required to image a semiconducting sample in tunneling mode, possibly inducing transient charging of near-surface defects. To solve this, one can remove the large voltage and offset the tip to a region several hundred nanometers away (typically without the use of feedback), as described in the protocol. Alternatively, the presence of damage to the sample can be detected by performing C-V spectroscopy or by doing a Kelvin probe measurement².

The geometry of the experiment implies certain characteristics should be aimed for in development of the sample. Localization of the dopant layer along the direction of tunneling is important, as an overly thick dopant layer will add ambiguity to the determination of the lever arm. In other words, the thickness of the dopant layer should be as close as possible to a single atomic plane. This arrangement is referred to as "delta doping." For example, in the experiment in Reference 1, the dopant layer was approximately 2 nanometers thick.

Successful charge accumulation imaging scans done to locate capacitive features of interest can take a substantial amount of time, sometimes on the order of several hours. With regard to scan speed, each pixel of the image should take an amount of time comparable to several periods of $V_{\text{excitation}}$, and the output filter of the lock-in amplifier should be set to approximately the same value as the time per pixel. Drift in the microscope which was not noticeable over the course of a few-minute STM scan can contribute to smearing of the substantially-longer-duration charge accumulation images.

The same tip used for tunneling and for capacitance experiments will have a different effective shape due to the distance dependence of the respective measurement mechanisms. Since tunneling is exponentially dependent upon distance, to a good approximation, only a single tip atom will receive most of the current. Hence the shape of the tip on the nanometer scale is mostly irrelevant, as long as the apex is mechanically stable. In SCA imaging, by contrast, the charge detected on the tip is due to capacitance; roughly speaking, it is inversely proportional to distance and higher portions of the tip can indeed receive a significant fraction of the signal. This means the nanometer-scale radius of curvature of the tip is relevant for capacitance measurement techniques. To maximize the amplitude of the signal without compromising spatial resolution, the tip radius should be approximately equal to the depth of the dopant layer beneath the surface^{8,9}.

Disclosures

The authors declare that they have no competing financial interests.

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