A Switched-Capacitor Pipelined BiCMOS Analog-to-Digital Converter

by

Andrew Nicholas Karanicolas

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Signature of Author ________________

Department of Electrical Engineering and Computer Science
September 1990

Certified By ________________

Hae-Seung Lee, Thesis Supervisor

Accepted By ________________

Chairman, Departmental Committee on Graduate Students

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Abstract

There is an increasing interest in high-performance analog-to-digital converters for use in integrated analog and digital mixed processing systems. Pipelined A/D converter architectures coupled with BiCMOS process technology have the potential for realizing monolithic high-speed and high-accuracy A/D converters.

In this thesis, the design of a switched-capacitor pipelined BiCMOS A/D converter is presented. The reference restoring and reference non-restoring algorithms for pipeline A/D conversion are discussed and compared. A BiCMOS operational amplifier and comparator suitable for use in the pipeline A/D converter, or other high-performance switched-capacitor applications, are described. Simulation results of the circuit blocks and the converter system are presented. A high frequency, fully differential BiCMOS operational amplifier been designed, fabricated and tested. The op-amp is integrated in a 3.0 GHz, 2 μm BiCMOS process with an active die area of 1.0 mm x 1.2 mm. This BiCMOS op-amp offers an infinite input resistance, a d-c gain of 100 dB, a unity-gain frequency of 90 MHz with 45° phase margin and a slew rate of 150 V/μs. The differential output range is 12 V. The circuit is operated from a ±5 V power supply and dissipates 125 mW. The op-amp is unity-gain stable with 7 pF of capacitive loading at each output. These performance measures indicate that the BiCMOS op-amp is suitable for use in high-performance switched capacitor applications.

Thesis Supervisor: Prof. Hae-Seung Lee
Title: Associate Professor of Electrical Engineering and Computer Science
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This work would not have been possible without the continuous love and support from my mother, father and sister. I owe any success I can claim today to them.
Dedication

This work is dedicated to the memory of my grandfather, Efthemios Katsapis.
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Chapter 1

Introduction

1.1 Background

There is an increasing interest in high-performance analog-to-digital converters for use in integrated analog and digital mixed processing systems. The realization of high-performance A/D converters typically has been limited to hybrid circuit technique. Insufficient matching accuracy of passive components and gain-bandwidth limitations of CMOS analog circuits has challenged implementation of high-performance A/D converters in low cost digital CMOS processes.

This thesis is concerned with the design of a pipelined BiCMOS A/D converter using a switched-capacitor, fully differential architecture. The pipeline architecture offers the potential of high throughput rate at moderate circuit complexity and cost [1]. Flash converters generally offer the highest possible speed but the circuit complexity for this case is an exponential function of the converter resolution. To contrast this, the circuit complexity of the pipeline converter is a linear function of the converter resolution. As a result, the pipeline converter is relatively easier to integrate monolithically because of fewer required components [2]. Currently, A/D converters with resolutions of more than 12-bits tend to use successive-approximation or oversampled architectures. Using these techniques, relatively small and low power converters have been constructed but require many clock cycles to complete a conversion and are thus relatively slow [3]. By taking advantage of the concurrent operation of the pipeline stages, the throughput of the pipeline converter can be significantly higher than successive approximation or oversampled converters.

Sampled data systems using switched-capacitor architectures are amenable to CMOS monolithic integration. CMOS process technology permits switched-capacitor architectures in addition to dense logic circuitry needed in many mixed signal processors. For analog circuits, bipolar devices offer a transconductance that is generally higher compared to MOS devices leading to, for a given area and power, higher speed and higher gain. The use of a switched-capacitor, fully differential pipelined architecture and BiCMOS process technology provides a basis for constructing monolithically integrated high-accuracy and high-speed A/D converters.
The success of monolithically integrated pipeline A/D architectures has been recently demonstrated. In [1, 4], a pipelined 5-Msample/s, 9-bit A/D converter with digital error correction was demonstrated. This converter uses a fully differential architecture and is implemented in 3μm CMOS technology. The chip uses 8500 mil² of area and 180 mW of power. In [3, 5], a pipelined 13-bit, 250-ksample/s A/D converter uses a reference-feedforward correction technique. A fully differential architecture is used and the converter is implemented in 3μm CMOS technology. The prototype requires 3400 mil² of area and 15 mW of power. A 12-bit, 1-Msample/s A/D converter using a capacitor error averaging technique is demonstrated by [2]. A fully differential architecture is used and the converter is implemented in 1.75μm CMOS technology. The prototype requires 14 mm² or 21,700 mil² and 400 mW of power. Most recently, a 13-bit, 2.5MHz A/D self-calibrated A/D converter is demonstrated by [6]. A fully differential architecture is used and the converter is implemented in 3μm CMOS technology. The chip uses 40,000 mil² and consumes 100mW. In this thesis, the target performance is set to be at 14-bit resolution at 10 MHz conversion rate. Typically, such high performance was achieved using expensive hybrid components. This thesis presents the analysis, design and simulation of major building blocks consistent with the target performance.

1.2 Design Strategy

Ideally, the design of complex systems should follow from an a priori list of specifications. In practical scenarios, because of the large number of parameters that can be varied in complex systems, it is important to have a design strategy to accomplish the design. From the outset, this strategy should be consistent with the design goals. This strategy should provide a guide as to how design decisions should be made as the design evolves. For A/D converters, it is desirable to achieve the highest possible accuracy and throughput. Although accuracy and throughput are important, cost, power dissipation, area and immunity to noise are examples of other parameters that also may be important. In this thesis, the primary design goal will be to design monolithic circuits and systems that can be used to synthesize high-performance pipeline A/D converters and other switched-capacitor circuits. The use of BiCMOS technology facilitates reaching this goal.

The primary design strategy is to first achieve a certain level of throughput and accuracy before imposing limits on critical parameters, within reasonable limits. For instance, power dissipation and area will be of concern but they will not be strictly defined. As is common in analog circuit design, dependencies are frequently more important than strict limits. The dependence of the throughput and accuracy on certain critical parameters will be of interest. Knowledge of such dependencies can be used to improve a design or identify a system limitation. In addition, knowledge of such dependencies may allow trade-off of performance parameters. In order that these trade-offs can occur, a useful strategy is to design circuits that permit flexibility in critical parameters, when possible. Robustness is another important design strategy
for designing complex systems in the presence of uncertainty. This particular strategy decouples otherwise potentially critical parameters.

1.3 Thesis Organization

This thesis is organized as follows. Chapter 2 will present a system level description of the reference restoring and reference non-restoring pipeline algorithms. Chapter 3 introduce the switched-capacitor circuit blocks used to implement the reference non-restoring algorithm. The switched-capacitor multiply-by-two and comparator will be analyzed from a system level viewpoint. Chapter 4 will present the design and analysis of the BiCMOS operational amplifier, comparator pre-amplifier and latch. Since the op-amp dynamic performance primarily dictates the throughput of the converter, focus will be placed on the op-amp dynamic performance parameters. Chapter 5 will show the circuit simulation results of the BiCMOS operational amplifier and comparator. The simulation results of the BiCMOS pipeline A/D converter is then presented. Chapter 6 will present the test results of a BiCMOS operational amplifier suitable for high performance switched-capacitor circuits. Finally, the conclusion including future work is given in Chapter 7.
Chapter 2

Pipelined A/D Converter

2.1 Architecture

In this thesis, radix-2 pipeline A/D converter architecture will be of prime interest. The basic architecture of such pipeline A/D converters is a cascade of 1-bit A/D converter stages, as shown in Fig. 2.1. The input is denoted as $V_{in}$ and the outputs are denoted as $[x_{N-1}x_{N-2} \cdots x_2x_1]$. Basically, for N-bit resolution, N stages are required. The input signal is presented to the leftmost stage, Stage $N$, resulting in the MSB decision. A residue is then passed to Stage $N-1$ and so forth until Stage 1, which decides the LSB. A more detailed description of pipeline algorithms is described later in this chapter. The pipelined A/D converter is inherently a sampled data system. Thus, each of the blocks in Fig. 2.1 performs a sample and hold function. The A/D conversion associated with this pipeline structure is a serial process. As a result, there is latency in the pipeline converter. For N stages, the latency of the converter $T_{latency}$ is,

$$T_{latency} = NT_{delay}$$  \hspace{1cm} (2.1)

where $T_{delay}$ is the processing delay of a single stage. A conversion latency is not an issue in most telecommunication and instrumentation applications. However, the latency can become important in control system applications. The concurrency of radix-2 pipeline converters permits the throughput of the converter to be that of a

![Figure 2.1: Basic architecture of a pipelined A/D converter.](image-url)
Figure 2.2: Signal flow graph of the \( k \)-th stage for the reference restoring algorithm.

A single stage,

\[ T_{\text{throughput}} = T_{\text{delay}}. \tag{2.2} \]

This throughput refers to a pipeline that is full with valid data. This condition is reached after waiting a full pipeline latency period beyond initial power-up or full reset.

## 2.2 Reference Restoring Algorithm

This section considers the system level description of an ideal pipelined A/D converter utilizing the reference restoring algorithm. Each of the stages in the pipeline independently follows the reference restoring algorithm. Signal flow graphs will be used to describe discrete-time systems. A signal flow graph description of the \( k \)-th stage in the pipeline is shown in Fig. 2.2. The nodes of the signal flow graph are indicated by open boxes. Nodes are connected by branches and the direction of the signal at each branch is indicated by the arrowhead. Each branch has associated with it a branch input, a branch transmittance and a branch output. The branch transmittance is indicated next to the respective arrowhead and is assumed to be unity when no label is indicated. A source node has no entering branches and a sink node has only entering branches. The value of any node is the sum of all entering branch outputs. The reader is referred to [7, 8] for further discussion of signal flow graphs.

In Fig. 2.2, the discrete time input signal is \( v_k(n) \). The subscript \( k \) indicates that the signal is an input to stage \( k \). The input \( v_k(n) \) is delayed by the first branch transmittance labeled as \( z^{-1} \). The delayed version of the input is then multiplied by 2 and a reference voltage \( V_{\text{ref}} \) is subtracted. The result, \( 2v_k(n) - V_{\text{ref}} \), is compared to zero and delayed again. The binary result of the comparison is made, namely \( x_{k-1}(n-2) \). If \( 2v_k(n) - V_{\text{ref}} \geq 0 \) then \( x_{k-1}(n-2) = 1 \). If \( 2v_k(n) - V_{\text{ref}} < 0 \) then \( x_{k-1}(n-2) = 0 \). The binary output of the comparator dictates whether the signal
2v_k(n) - V_{ref} will be routed to the upper or lower part of the flow graph, depending on whether x_{k-1}(n - 2) is 1 or 0, respectively. If the comparison selects the upper branch, then the signal 2v_k(n) - V_{ref} will be delayed once more resulting in the output v_{k-1}(n - 3) = 2v_k(n) - V_{ref}. If the comparison selects the lower branch, then the reference is added back, or restored, and the final output is then v_{k-1}(n - 3) = 2v_k(n). Notice that the latency for the k-th stage is 3 clock periods. The reference restoring algorithm for the k-th stage can now be summarized,

Algorithm 2.1 Reference restoring method for k-th Stage.

1. If $2v_k(n) - V_{ref} \geq 0$ then
   \[ x_{k-1}(n - 2) = 1 \text{ and } v_{k-1}(n - 3) = 2v_k(n) - V_{ref} \]

2. If $2v_k(n) - V_{ref} < 0$ then
   \[ x_{k-1}(n - 2) = 0 \text{ and } v_{k-1}(n - 3) = 2v_k(n) \]

2.3 Reference Non-Restoring Algorithm

The reference non-restoring algorithm is derived by observing the logical timing of the reference restoring algorithm. Consider v_k at the input of stage k. In the reference restoring algorithm, one clock period is used to add the reference back if the quantity $2v_k - V_{ref} < 0$. This reference restoring wastes a clock period because the knowledge of how v_k compares to $V_{ref}/2$ is already known at the time v_k is available at the input of stage k. The state of the output bit at the previous stage k + 1 reflects how v_k compares to $V_{ref}/2$. Thus, the principle of the reference non-restoring algorithm becomes clear. The input to stage k includes v_k and the state of the output bit at stage k + 1. The leading stage is different as it only needs to perform a sample-and-hold function of the pipeline input and determine how the pipeline input compares to $V_{ref}/2$ thus determining the MSB. The consequence of one less clock cycle not only increases the throughput of the system but also results in less manipulation of the analog signal as it progresses in the pipeline. Thus, there are fewer opportunities for the signal to be corrupted.

This section considers the system level description of an ideal pipelined A/D converter utilizing the reference non-restoring algorithm. Each stage in the pipeline independently follows the reference non-restoring algorithm but the leading stage N follows a simpler algorithm. A signal flow graph of the N-th stage is shown in Fig. 2.3 A signal flow graph of the k-th stage, k ≠ N is shown in Fig. 2.4.

In Fig. 2.3, the discrete time input signal is $v_N(n)$. The subscript N indicates that the signal is an input to stage N. The input $v_N(n)$ is delayed by the first branch transmittance labeled as $z^{-1}$. At this point, a comparison to $V_{ref}/2$ is performed and the binary result is $x_{N-1}(n - 2)$. The delayed input is delayed yet another clock

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Figure 2.3: Signal flow graph of the N-th stage for the reference non-restoring algorithm.

Figure 2.4: Signal flow graph of the k-th stage, \( k \neq N \), for the reference non-restoring algorithm.
period to the output \( v_{N-1}(n-2) \). Notice that the latency of the \( N \)-th stage is 2 clock periods.

In Fig. 2.4, the discrete time input \( v_k(n) \) is delayed by the first branch transmittance labeled as \( z^{-1} \). The binary input \( x_k(n) \) controls whether the input \( v_k(n) \) will be routed to the upper or lower part of the flow graph depending on whether \( x_k(n) \) is 1 or 0, respectively. If the upper branch is selected, then the delayed input signal is multiplied by 2 and the reference \( V_{ref} \) is subtracted resulting in \( 2v_k(n) - V_{ref} \). This result is delayed once more to the output \( v_{k-1}(n-2) \). If the lower branch is selected, then the delayed input signal is multiplied by 2 resulting in \( 2v_k(n) \). This result is delayed to the output \( v_{k-1}(n-2) \). Before the signal \( 2v_k(n) - V_{ref} \) or \( 2v_k(n) \) is delayed to the output, it is compared to \( V_{ref}/2 \) and the result is the binary output \( x_{k-1}(n-2) \). Notice that the latency for the \( k \)-th stage is 2 clock periods. The reference non-restoring algorithm can now be summarized:

Algorithm 2.2 Reference non-restoring method for \( N \)-th stage.

1. \( v_{N-1}(n-2) = v_N(n) \).
2. If \( v_{N-1}(n-2) \geq V_{ref}/2 \) then \( x_{N-1}(n-2) = 1 \).
3. If \( v_{N-1}(n-2) < V_{ref}/2 \) then \( x_{N-1}(n-2) = 0 \).

Algorithm 2.3 Reference non-restoring method for \( k \)-th stage, \( k \neq N \).

1. If \( x_k(n) = 1 \) then \( v_{k-1}(n-2) = 2v_k(n) - V_{ref} \).
2. If \( x_k(n) = 0 \) then \( v_{k-1}(n-2) = 2v_k(n) \).
3. If \( v_{k-1}(n-2) \geq V_{ref}/2 \) then \( x_{k-1}(n-2) = 1 \).
4. If \( v_{k-1}(n-2) < V_{ref}/2 \) then \( x_{k-1}(n-2) = 0 \).

As discussed above, the reference non-restoring algorithm has a higher throughput and manipulates the analog signal fewer times, compared to the reference restoring algorithm, since the reference restoring operation is not performed. The pipeline A/D converter in this thesis utilizes the reference non-restoring algorithm. For completeness, both algorithms will be summarized in the context of fully differential signal schemes.

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2.4 Fully Differential Signal Scheme

In fully differential systems, the maximum dynamic range is obtained when the common mode level is between the two power supply voltages for split supplies or half way in between a single supply. Regardless, a differential value of zero is assigned when both outputs of the differential system are at the common mode level. The voltage assignment for this condition is arbitrary but the choice of zero is convenient. Fig. 2.5 shows voltage assignments for single ended and fully differential systems. From this figure, the relation between voltages assigned to single and differential systems is:

\[ v_k = v_k' + \frac{V_{\text{ref}}}{2} \]  

(2.3)

where \( v_k' \) is the fully differential signal and \( v_k \) is the single ended signal. Since the choice of differential analog ground is completely arbitrary, the pipelined A/D algorithms and signal flow graphs remain logically unchanged. By using equation 2.3, the signal flow graphs and algorithms will be restated for fully differential signal schemes. Note that in a fully differential system, two voltage references are needed, namely \( V_{\text{ref}}/4 \) and \( -V_{\text{ref}}/4 \), in order to define a zero common mode level for the system references. Since switch networks are readily constructed in MOS circuit implemen-
Algorithm 2.4 Reference restoring method for $k$-th stage using a fully differential signal scheme.

1. If $2v'_k(n) \geq 0$ then
   
   \[ x_{k-1}(n-2) = 1 \text{ and } v'_{k-1}(n-3) = 2v'_k(n) - V_{ref}/2. \]

2. If $2v'_k(n) < 0$ then
   
   \[ x_{k-1}(n-2) = 0 \text{ and } v'_{k-1}(n-3) = 2v'_k(n) + V_{ref}/2. \]

Algorithm 2.5 Reference non-restoring method for $N$-th stage using a fully differential signal scheme.

1. $v'_{N-1}(n-2) = v'_N(n)$.

2. If $v'_{N-1}(n-2) \geq 0$ then $x_{N-1}(n-2) = 1$.

3. If $v'_{N-1}(n-2) < 0$ then $x_{N-1}(n-2) = 0$.

Algorithm 2.6 Reference non-restoring method for $k$-th stage, $k \neq N$, using a fully differential signal scheme.

1. If $x_k(n) = 1$ then $v'_{k-1}(n-2) = 2v'_k(n) - V_{ref}/2$.

2. If $x_k(n) = 0$ then $v'_{k-1}(n-2) = 2v'_k(n) + V_{ref}/2$.

3. If $v'_{k-1}(n-2) \geq 0$ then $x_{k-1}(n-2) = 1$.

4. If $v'_{k-1}(n-2) < 0$ then $x_{k-1}(n-2) = 0$. 

Figure 2.6: Signal flow graph of the k-th stage for the reference restoring algorithm using a fully differential signal scheme.

Figure 2.7: Signal flow graph of the N-th stage for the reference non-restoring algorithm using a fully differential signal scheme.
Figure 2.8: Signal flow graph of the k-th stage, $k \neq N$, for the reference non-restoring algorithm using a fully differential signal scheme.
Chapter 3

Switched-Capacitor Systems

The switched-capacitor system design for the sample-and-hold, multiply-by-two and the comparator is presented in this chapter. The N-th stage in the pipeline uses a sample-and-hold amplifier and a comparator. The structure for the N-th stage is shown in Fig. 3.1. The k-th stage, $k \neq N$, uses a multiply-by-two amplifier and comparator. The structure for the k-th stage is shown in Fig. 3.2

3.1 Amplifier Systems

The sample-and-hold and multiply-by-two amplifiers are basic building blocks of the reference non-restoring pipeline A/D converter. The sample-and-hold amplifier function is a subset of the multiply-by-two amplifier function so the multiply-by-two will be first discussed.

3.1.1 Multiply-by-Two Amplifier

The multiply-by-two system is shown in Fig. 3.3. The multiply-by-two architecture shown in Fig. 3.3 has an important advantage over a conventional approach. Typically, the multiply-by-two for a pipeline A/D converter uses a sampling capacitor of $2C$ and a feedback capacitor of $C$. The loop transmission for this structure is basically $1/3$ of the op-amp forward transmission when op-amp input capacitance is not included. For the multiply-by-two structure in Fig. 3.3, the input and feedback capacitors are the same value so the loop transmission is $1/2$ of the op-amp forward transmission when op-amp input capacitance is not included. A direct result of the increased loop transmission is a higher closed-loop frequency and thus an improved settling time. The architecture of the multiply-by-two is derived from [2].

For understanding the operation of the system, it is assumed that the capacitor values are nominally equal so as a result $C_m \equiv C_{m1} = C_{m2} = C_{m3} = C_{m4}$. In addition, balanced op-amp halves are assumed. A common mode feedback scheme will be assumed so that the output common mode level is set to zero. Consider a differential signal with zero common mode level applied at the inputs $V_{i1}$ and $V_{i2}$ so
Figure 3.1: Structure of N-th switched-capacitor stage of the pipelined A/D converter.

Figure 3.2: Structure of k-th switched-capacitor stage, $k \neq N$, of the pipelined A/D converter.
NOTE:

Phi1 controls: SM5, SM10

Phi2 controls: SM1, SM2, SM6, SM7

Phi3 controls: SM3, SM4, SM8, SM9

Previous state bit controls: SM11, SM12, SM13, SM14

Figure 3.3: Switched-capacitor multiply-by-two amplifier.
that \( V_{id} = V_{i1} - V_{i2} \). Assume that \( V_{ref1} = V_{ref}/4 \) and that \( V_{ref2} = -V_{ref}/4 \). The top half of the system is now used to analyze the system operation.

With \( \phi_1 = 1 \), \( \phi_2 = 1 \), \( \phi_3 = 0 \) the multiply-by-two system is performing the sample function. Consider the charge on capacitors \( C_{m1} \) and \( C_{m2} \) after the op-amp has settled:

\[
q_1(n-1) = (C_{m1} + C_{m2}) \left[ V_{i1}(n-2) - \frac{1}{2} V_{N}(n-1) \right] \tag{3.1}
\]

where \( V_{N}(n) \) is the op-amp differential input referred noise which includes d-c noise, or offset, 1/f noise and thermal noise. The timing of the system requires that \( \phi_1 \) is set to 0 before \( \phi_2 \) or \( \phi_3 \) change state. Once this condition is met, \( \phi_1 = 0 \), \( \phi_2 = 0 \), \( \phi_3 = 1 \) and the multiply-by-two is then in the amplification mode. The charge on capacitors \( C_{m1} \) and \( C_{m2} \) after the op-amp has settled is:

\[
q_2(n) = C_{m2} \left[ \frac{1}{4} x V_{ref}(n) - \frac{1}{2} V_{N}(n) \right] + C_{m1} \left[ V_{o1}(n) - \frac{1}{2} V_{N}(n) \right] \tag{3.2}
\]

where \( x \) represents the sign of the input \( V_{id}(n) \), as prescribed by the reference non-restoring algorithm. Thus, if \( V_{id}(n) \geq 0 \) then \( x = 1 \), otherwise \( x = -1 \). Notice that switch network \( S_{m11}, S_{m12}, S_{m13} \) and \( S_{m14} \) is used to derive the differential reference \( \pm V_{ref}/2 \) as a function of \( x \). If the charge on capacitors \( C_{m1} \) has not been corrupted by charge injection then charge conservation requires that \( q_1(n-1) = q_2(n) \). With \( C_m = C_{m1} = C_{m2} \), the difference equation for \( V_{o1}(n) \) is:

\[
V_{o1}(n) = 2V_{i1}(n-2) - \frac{x V_{ref}(n)}{4} + V_{N}(n) - V_{N}(n-1) \tag{3.3}
\]

It can be shown that the difference equation for \( V_{o2}(n) \) is:

\[
V_{o2}(n) = 2V_{i2}(n-2) + \frac{x V_{ref}(n)}{4} + V_{N}(n-1) - V_{N}(n) \tag{3.4}
\]

Subtracting equation 3.4 from 3.3 results in:

\[
V_{od}(n) = 2V_{id}(n-2) - \frac{x V_{ref}(n)}{2} + 2 [V_{N}(n) - V_{N}(n-1)] \tag{3.5}
\]

Thus, it is seen that the input is multiplied by two and the reference voltage is either subtracted or added, depending on the sign of the input. The \( z \)-transform of equation 3.5 produces:

\[
V_{od}(z) = 2V_{id}(z)z^{-2} - \frac{x V_{ref}(z)}{2} + 2V_{N}(z)(1 - z^{-1}) \tag{3.6}
\]

The CDS (Correlated Double Sampling) transfer function \( H_{CDS}(z) \) is \([9, 10, 11]\):

\[
H_{CDS}(z) = 2(1 - z^{-1}) \tag{3.7}
\]
The squared frequency response magnitude of equation 3.7 is expressed as:

\[ |H_{CDS}(\omega)|^2 = 4 \left| 1 - e^{-j\omega} \right|^2 \]  \hspace{1cm} (3.8)

\[ = 16 \sin^2 \frac{\omega}{2} \]  \hspace{1cm} (3.9)

Since a delay in this switched capacitor system represents only one half of the sample period,

\[ \omega = \frac{\Omega T}{2} \]  \hspace{1cm} (3.10)

where \( \Omega \) is the continuous time frequency. Thus, equation 3.9 becomes:

\[ \left| H_{CDS} \left( \frac{\Omega T}{2} \right) \right|^2 = 16 \sin^2 \frac{\Omega T}{4} \]  \hspace{1cm} (3.11)

Thus, at frequencies \( \Omega = 4k\pi/T \), where \( k \) is an integer, the magnitude of the system function is 0. Thus, d-c noise is eliminated. It can be shown that 1/f noise is effectively canceled if the corner frequency of the 1/f noise process is less than 1/4 the sample frequency [12]. The corner frequency of 1/f noise in MOS devices is typically less than 100 kHz [13, 14, 15] while the intended sampling frequency is greater than 1 MHz. As a result, the 1/f noise is effectively canceled. Since the thermal noise PSD has high frequency components, the CDS does not cancel thermal noise.

A primary source of differential error occurs from MOS device charge injection. If the MOS switches, and the impedances that they are connected to, could be matched then the charge injection would balance on both halves of the fully differential system resulting in a zero differential error. Since mismatches are inevitable in an actual implementation, the charge injection from switches is important. The op-amp inputs are capacitive nodes except when \( \phi_1 = 1 \). As a result, the only significant d-c path from the op-amp inputs to ground is by switches \( S_{m5} \) and \( S_{m10} \). It is important that these switches are turned off before the state of the other switches changes. The reason for this is that once switches \( S_{m5} \) and \( S_{m10} \) are turned off, the charge injection from the other switches cannot affect the sampled charge. Thus, with this timing scheme, a primary source of differential error occurs when switches \( S_{m5} \) and \( S_{m10} \) turn off because of charge injection corrupting the sampled charge on the capacitors. It has been shown that transmission gates do not cancel charge injection, even when the geometry of the respective NMOS and PMOS device are scaled by the ratio of the mobilities [16]. Furthermore, the use of transmission gates at critical locations can cause problems resulting from the clock timing and skew of the complementary clocks. Thus, clock jitter can be translated into amplitude noise, unless proper precautions are taken. As a result, the switches \( S_{m5} \) and \( S_{m10} \) should be implemented with a single MOS device using the minimum possible geometry to minimize the charge injection. A minimum geometry for these switches may conflict with the need of low resistance switches for facilitating the reset mode when \( \phi_1 = 1 \). Also, a low resistance switch is desired for these switches so that the phase margin of the unity-gain connection is not
degraded because of a pole introduced by the switch resistance and the op-amp input capacitance. It is important to use the minimum channel length for the switches. This is because reducing the channel length reduces charge injection and decreases the switch resistance.

It is important to realize that charge injection depends on the impedances connected to the source and drain terminals of the MOS device in question [16]. Consider a case where the capacitors are of equal value. When switches \(S_{s_m5}\) and \(S_{s_m10}\) are turned off, switches \(S_{s_m1}, S_{s_m2}, S_{s_m6}\) and \(S_{s_m7}\) are still on as the multiply-by-two was in the sample mode. A large differential error can result from the charge injection of \(S_{s_m5}\) and \(S_{s_m10}\) because of resistance mismatch in the four input switches. Even with symmetrically scaled geometries between differential halves, this mismatch can still occur because the transmission gate resistance is typically not an even function of the voltage across the transmission gate. This occurs partly because of differences in the mobilities and back-gate effect between NMOS and PMOS devices. Thus, when a differential input signal is applied across \(V_{i1}\) and \(V_{i2}\), a signal dependent charge injection results. By simply scaling the geometries of the transmission gate devices by the ratio of the NMOS and PMOS mobilities, the switch resistance is close to an even function of the voltage applied across the transmission gate. As a result, the this differential error component can be substantially reduced. Another approach for reducing the differential error is to minimize the input switch resistance [17]. By reducing the absolute resistance of the input switches, the differential error is then scaled down. The best approach for designing the input transmission gates is to scale the device geometries by the mobilities and to minimize the switch resistance as much as possible.

### 3.1.2 Sample-and-Hold Amplifier

The sample-and-hold amplifier is shown in Fig. 3.4. This structure is similar to the multiply-by-two with \(C_{m2} = 0\) and \(C_{m3} = 0\). To simplify the analysis, assumptions similar to the multiply-by-two concerning symmetry are used so that \(C_h \equiv C_{h1} = C_{h2}\). In addition, balanced op-amp halves are assumed. In a manner similar to the multiply-by-two, it can be shown that the governing difference equation is:

\[
V_{od}(n) = V_{id}(n - 2) + V_N(n) - V_N(n - 1)
\]  
(3.12)

Thus, it is seen that the input is multiplied by one, as is desired for this sample-and-hold. The z-transform of equation 3.12 produces:

\[
V_{od}(z) = V_{id}(z)z^{-2} + V_N(z)\left(1 - z^{-1}\right)
\]  
(3.13)

Thus, CDS is performed with the same results as the multiply-by-two. The clock timing and charge injection issues for the sample-and-hold are analogous to the multiply-by-two.
Figure 3.4: Switched-capacitor sample-and-hold amplifier.

NOTE:

PHI1 controls: SH3, SH6

PHI2 controls: SH1, SH4

PHI3 controls: SH2, SH5
3.2 Comparator System

The basic element of the comparator system is the regenerative latch. A difficulty with regenerative circuits for use in high accuracy A/D converters is that they exhibit relatively large input referred offsets. As a result, a pre-amplifier system is needed to overcome the offset when the smallest anticipated input is to be compared. However, a drawback of this approach is that the pre-amplifier circuits also have input referred offset that must be canceled for a high accuracy converter. Thus, an offset cancellation scheme is needed for the pre-amplifier system.

In order to satisfy the high accuracy and high throughput requirements, an open loop offset cancellation scheme is chosen. However, open loop schemes can have difficulties related to dynamic range. In general, multi-stage amplifiers achieve the highest gain-bandwidth products. It can be shown that multi-stage amplifiers are optimum for minimizing power, area and response time for high accuracy pre-amplifier systems [18]. As a result, two pre-amplifier stages are chosen to construct the pre-amplifier system. The comparator system is shown in Fig. 3.5. In order to understand the operation of the pre-amplifier system, one stage will first be considered, as shown in Fig. 3.6. For understanding the operation of one stage, it is assumed that the capacitor values are equal so as a result \( C_p = C_{p1} = C_{p2} = C_{p3} = C_{p4} \). The capacitors \( C_{z1} \) and \( C_{z2} \) model the input capacitance of the succeeding stage. It will be assumed that \( C_z = C_{z1} = C_{z2} \). The voltages \( V_{z1} \) and \( V_{z2} \) are the effective outputs. Consider a differential signal with zero common mode level applied across the inputs \( V_{11} \) and \( V_{21} \) so that \( V_{id} = V_{11} - V_{21} \). The top-half of the system is now used to analyze the operation of the circuit.

With \( \phi_1 = 0, \phi_2 = 1 \) the pre-amplifier system is in the offset cancel mode. Consider the output voltage of the pre-amplifier circuit after settling:

\[
V_{op1}(n - 1) = -a_0 \frac{1}{2} V_N(n - 1) \tag{3.14}
\]

where \( a_0 \) is the d-c gain and \( V_N(n) \) is the input referred noise of the pre-amplifier circuit. The charge held on \( C_{p1} \) is:

\[
q_1(n - 1) = C_p a_0 \frac{1}{2} V_N(n - 1) \tag{3.15}
\]

With \( \phi_1 = 1, \phi_2 = 0 \), the pre-amplifier system is in the amplification mode. The output voltage of the pre-amplifier circuit after settling is:

\[
V_{op1}(n) = a_0 \left[ V_{11}(n) - \frac{1}{2} V_N(n) \right] \tag{3.16}
\]

At this point, the charge on the capacitive circuit can be expressed as:

\[
q_2(n) = C_p [V_{z1}(n) - V_{op}(n)] + V_{z1}(n) C_z \tag{3.17}
\]
Figure 3.5: Switched-capacitor comparator system.
Figure 3.6: One pre-amplifier stage of a switched-capacitor comparator system.

Assuming that charge on $C_p$ was not corrupted by charge injection then charge conservation requires that $q_1(n - 1) = q_2(n)$. As a result, the difference equation for $V_{x1}(n)$ is:

$$V_{x1}(n) = \frac{a_0C_p}{C_p + C_x} \left[ V_{i1}(n) + \frac{1}{2} [V_N(n - 1) - V_N(n)] \right]$$  \hspace{1cm} (3.18)

It can be shown that the difference equation for $V_{x2}(n)$ is:

$$V_{x2}(n) = \frac{a_0C_p}{C_p + C_x} \left[ V_{i2}(n) + \frac{1}{2} [V_N(n) - V_N(n - 1)] \right]$$  \hspace{1cm} (3.19)

Subtracting equation 3.19 from equation 3.18 results in:

$$V_{xd}(n) = \frac{a_0C_p}{C_p + C_x} [V_{id}(n) + V_N(n - 1) - V_N(n)]$$  \hspace{1cm} (3.20)

Notice that the effective d-c gain is reduced because of the capacitive attenuation circuit at the output. The z-transform of equation 3.20 produces:

$$V_{xd}(z) = \frac{a_0C_p}{C_p + C_x} \left[ V_{id}(z) + +V_N(z) \left( z^{-1} - 1 \right) \right]$$  \hspace{1cm} (3.21)

The CDS transfer function $H_{CDS}(z)$ is:

$$H_{CDS}(z) = \frac{a_0C_p}{C_p + C_x} \left( z^{-1} - 1 \right)$$  \hspace{1cm} (3.22)
The squared frequency response magnitude of equation 3.22 is expressed as:

\[ |H_{CDS}(\omega)|^2 = 4a_0^2 \left( \frac{C_p}{C_p + C_x} \right)^2 \sin^2 \frac{\omega}{2} \]  

(3.23)

As with the multiply-by-two circuit, the magnitude of the CDS transfer function is 0 when \( \Omega = 4k\pi/T \), where \( k \) is an integer. Thus, the d-c noise is eliminated, the 1/f noise is effectively canceled but the CDS does not cancel thermal noise.

In order to prevent sampled charge in the offset cancel mode from being corrupted, the clocks \( \phi_1 \) and \( \phi_2 \) are non-overlapping. As with the multiply-by-two, charge injection is the primary source of differential error. In order to minimize the charge injection, minimum geometry switches should be used. Since excessive switch resistance can be a difficulty, the minimum possible channel length should be used as this defines a lower limit of charge injection and switch resistance that the process technology is capable of achieving.

A potential problem with open loop offset cancellation is dynamic range limitation. The product of the offset voltage and the d-c gain of the pre-amplifier circuit must not exceed the output dynamic range limits for complete offset cancellation to occur. Typically, it is desirable for the dynamic range to be wide enough to easily accept the output referred offset.

The regenerative latch is a digital circuit using the pre-amplifier system output. The operation of the latch will be discussed in chapter 4.

### 3.3 Pipeline A/D Converter Timing

Although the multiply-by-two and sample-and-hold use three clock phases, only two are non-overlapping. The clock phases \( \phi_{1m} \) and \( \phi_{3m} \) are non-overlapping while clock phase \( \phi_{2m} \) is a delayed version of \( \phi_{1m} \). The comparator pre-amplifier system uses two non-overlapping clock phases, \( \phi_{1p} \) and \( \phi_{2p} \). For a given stage in the pipeline, the multiply-by-two and comparator will concurrently be in the sample mode and offset cancel mode, respectively. Then, the multiply-by-two and comparator will concurrently be in the respective amplification modes. Note that generally each stage is either in a reset mode or an amplification mode. As a result, only two non-overlapping clocks are required for the reference non-restoring pipeline A/D converter. At first, the even stages are reset while the odd stage amplify and then the even stage amplify while the odd stages are reset.

The op-amp requires additional clocks to perform the common mode feedback function and the latch requires additional clocks to perform the latch reset. Pipeline converters are amenable to using the main non-overlapping clocks for these circuit specific functions [6, 1, 4]. In general, the common mode feedback and latch reset clocks will be considered separate but with the option of being determined by the main clocks.

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Chapter 4

BiCMOS Circuit Design

This chapter presents the design of the key circuit blocks in the pipeline A/D converter. The performance objectives for the operational amplifier and the comparator are derived from the requirements of high-performance switched-capacitor systems in general. High-performance circuits used in a switched-capacitor context can be implemented using BiCMOS process technology. Achieving these performance objectives involves circuit design and process design challenges. The focus in this thesis is to present the design of the operational amplifier and comparator for use in the pipeline A/D converter. Ultimately, the performance of these circuits is related to device performance. A brief description of the BiCMOS process used in the design is in Appendix A. A more complete description can be found in [19, 20].

In general, n-p-n devices offer superior gain and bandwidth over their p-n-p counterparts. As a result, the n-p-n device is chosen whenever possible in the circuit design. The use of CMOS devices simplifies the design of basic logic circuits, such as inverters. Realization of switched-capacitor circuits is possible using CMOS transmission gates. Active loads for n-p-n common emitter amplifiers can use either PMOS or p-n-p devices. As the p-n-p devices are not yet optimized in the M.I.T. BiCMOS process, PMOS active loads are used for such amplifiers. From an implementation point of view, this is not restrictive as most commercially available BiCMOS processes are designed for digital circuits and do not offer p-n-p devices.

Input differential pairs for the op-amp and comparator pre-amplifier utilize PMOS devices resulting in lower threshold voltage hysteresis [21] and lower 1/f noise Power Spectrum Density (PSD) compared to NMOS devices. As the op-amp is used in switched-capacitor circuits that perform Correlated Double Sampling (CDS), the 1/f noise is attenuated [9].

The BiCMOS pipeline A/D converter is fabricated on p/p+ epi-wafers permitting independent connection of the PMOS substrate. The source and substrate of the PMOS differential pair devices are connected together. This prevents the back-gate effect from coupling source-substrate noise voltage to drain noise current, and thus, to an equivalent gate-source noise voltage. In order to minimize coupling of the substrate to the op-amp circuit, the source and substrate of PMOS devices in current sources are connected together.
4.1 Operational Amplifier Design

4.1.1 Topology Selection

The design objectives for the operational amplifier are derived from the requirements of high-performance switched-capacitor systems. The dynamic response of the op-amp is critical to the throughput and accuracy of the pipeline A/D converter. The basic topology of the op-amp is selected so that the n-p-n devices available in BiCMOS can be best utilized. The switched-capacitor amplifier requirements for the pipeline A/D converter impose high-frequency and high dc-gain requirements on the op-amp. A folded-cascode topology can be used to achieve the high-frequency response but op-amps with such topologies suffer from relatively low d-c gain. A two-stage op-amp design can satisfy the high-frequency and high dc-gain requirements. Frequency compensation for the two-stage op-amp design is accomplished with pole-split frequency compensation. This is a powerful technique but can also involve challenging circuit design.

The two-stage op-amp is a fully differential design. Fully differential systems have become popular recently for implementing a variety of integrated mixed signal processing functions. The main advantage of using such topologies is that common mode noise components can be effectively canceled. An added benefit is the extended dynamic range of differential signals compared to single-ended signals. Disadvantages of fully differential systems include increased area, power and complexity. Another disadvantage is that fully differential circuits frequently require common mode feedback circuits to set the common mode level. The common mode feedback is needed since two degrees of freedom are present in differential signals, namely the differential mode and the common mode.

The op-amp circuit is presented in Figs. 4.1 and 4.2. The substrates for NMOS and PMOS devices are implicitly connected to \( V_{SS} \) and \( V_{DD} \), respectively, unless otherwise indicated. The p-well substrates for all n-p-n devices and poly-n\(^+\) capacitors are connected to \( V_{SS} \).

4.1.2 Overview of Op-Amp Circuit

The op-amp employs a PMOS differential pair in the first stage composed of devices \( M_1 \) and \( M_2 \), shown in Fig. 4.1 The PMOS devices provide a purely capacitive input impedance necessary for switched-capacitor systems. Observing the right half portion of Fig. 4.1, the input stage is actively loaded with transistor \( Q_7 \).

The second stage is a bipolar design consisting of common emitter amplifier \( Q_2 \) and cascode device \( Q_3 \). It can be shown that for a frequency compensated two-stage amplifier the non-dominant pole frequency is \( p_2 \approx -G_{m2}/C_L \) [13], where \( G_{m2} \) and \( C_L \) are the transconductance and load capacitance, respectively, of the second stage. The high transconductance of bipolar devices is used in the second stage to permit a high bandwidth by pushing the non-dominant pole out to a high frequency. In addition, this high transconductance permits a high d-c gain. The second stage
Figure 4.1: BiCMOS operational amplifier main circuit.
Figure 4.2: BiCMOS operational amplifier common mode feedback sense circuit.

employs a cascode structure to provide a large output resistance for high d-c gain. The input impedance to the second stage is relatively low compared to the output impedance of the first stage. As a result, transistor $Q_3$ is used as an emitter follower interposed between the first and second stages to minimize loading effects. The op-amp uses a pole-splitting frequency compensation capacitor $C_c$ and nulling resistor $R_c$. A low impedance output buffer is not needed for this op-amp for the intended switched-capacitor applications.

The fully differential op-amp requires a common mode feedback loop to set the output common mode level. This op-amp uses a dynamic common mode feedback scheme for this purpose [22, 23]. As the op-amp is a two-stage design, the common mode feedback circuit controls the effective first stage bias current to set the common mode levels of both the first and second stage outputs [24].

The input of the common mode amplifier is shown in Fig. 4.1 as node $V_{CM}$ at the gate of transistor $M_3$. An increase in this voltage causes each of the op-amp output voltages to decrease. If a disturbance causes the output common mode level to increase, the common mode sense circuit will correspondingly increase voltage $V_{CM}$. This causes the op-amp output common mode level to respond opposite to the disturbance, thus stabilizing the output common mode level. The common mode amplifier reference voltage is at node $V_{CMR}$ connected to the gate of $M_4$. Since a differential input stage is used, the common mode feedback will attempt to drive the error voltage to zero. Thus, the common mode output level can be set by reference voltage $V_{CMR}$. It can be seen from Fig. 4.1 that the common mode signal path is composed of the first and second stages of the differential amplifier in addition to
the current mirror $Q_7$, $Q_8$ and $Q_9$. The frequency compensation network serves both the differential mode and common mode amplifier. As a result, the common mode and differential mode amplifier dynamics are comparable. The unity-gain frequency of the common mode amplifier is lower compared to the differential mode amplifier. This is to ensure proper phase margin for the common mode amplifier as the common mode loop transmission has more high frequency poles than the differential mode loop transmission.

### 4.1.3 Frequency Response

As was described in section 4.1.2, the differential mode and common mode signal paths are similar. A two-stage model will be developed to analyze the frequency response for the differential and common mode amplifiers. The analysis is similar to that in [13, 14]. However, the analysis here accounts for the first stage Miller capacitance. The two-stage amplifier model is shown in Fig. 4.3. The first stage is represented with the transconductance generator $G_{m1}$ and the load impedance composed of $R_1$ and $C_1$. The input stage drain-gate capacitance is shown as capacitor $C_4$. The second stage is represented with the transconductance generator $G_{m2}$ and the load impedance composed of $R_2$ and $C_2$. The objective will be to find the ZSR (Zero State Response) system function $V_3(s)/V_1(s)$.

By considering KCL at node $v_2$:

$$[V_1(s) - V_2(s)]C_4s - G_{m1}V_1(s) - \frac{V_2(s)}{R_1} - V_2(s)C_1s + \frac{V_3(s) - V_2(s)}{R_c + 1/C_c} = 0. \quad (4.1)$$

Now, considering KCL at node $v_3$:

$$\frac{V_2(s) - V_3(s)}{R_c + 1/C_c} - G_{m2}V_2(s) - \frac{V_3(s)}{R_2} - V_3C_2s = 0. \quad (4.2)$$

These equations can be rewritten as follows:

$$V_2(s)\left(\frac{1}{R_1} + C_1s + C_4s + \frac{1}{R_c + 1/C_c}\right) - V_3(s)\left(\frac{1}{R_c + 1/C_c}\right) = V_1(s)(C_4(s) - G_{m1}) \quad (4.3)$$
\[ V_2(s) \left( \frac{1}{R_c + 1/C_c s} - G_{m2} \right) \]

\[-V_3(s) \left( \frac{1}{R_2} + C_2 s + \frac{1}{R_c + 1/C_c s} \right) = 0 \]  \hspace{1cm} (4.4)

Now, this system of equations 4.3 and 4.4 can be solved for \( V_3(s) \) in terms of \( V_1(s) \) yielding the system function \( a(s) = V_3(s)/V_1(s) \). After simplification of the resulting expressions, the system function is found to be:

\[ a(s) = \frac{G_{m1} G_{m2} R_1 R_2 (1 - C_4 s/G_{m1}) [1 + s C_c (R_c - 1/G_{m2})]}{1 + \gamma_1 s + \gamma_2 s^2 + \gamma_3 s^3} \]  \hspace{1cm} (4.5)

where the constants \( \gamma_1, \gamma_2 \) and \( \gamma_3 \) are:

\[ \gamma_1 = G_{m2} R_1 R_2 C_c + R_1 C_c + R_1 C_1 + R_1 C_4 R_2 C_c + R_2 C_2 + R_c C_c \]  \hspace{1cm} (4.6)

\[ \gamma_2 = R_1 C_c R_2 C_2 + R_1 C_1 R_2 C_c + R_1 C_4 R_2 C_2 + R_1 C_1 R_c C_c \]
\[ \hspace{2cm} + R_1 C_4 R_2 C_c + R_1 C_4 R_2 C_2 + R_1 C_1 R_c C_c + R_c C_c R_2 C_2 \]  \hspace{1cm} (4.7)

\[ \gamma_3 = R_1 C_4 R_c C_c R_2 C_2 + R_1 C_1 R_c C_c R_2 C_2 \]  \hspace{1cm} (4.8)

Now, the denominator \( d(s) \) of the system function \( a(s) \) can be generally expressed as:

\[ d(s) = \left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right) \]
\[ = 1 - s \left( \frac{1}{p_1} + \frac{1}{p_2} + \frac{1}{p_3} \right) + s^2 \left( \frac{1}{p_1 p_2} + \frac{1}{p_2 p_3} + \frac{1}{p_1 p_3} \right) \]
\[ - s^3 \left( \frac{1}{p_1 p_2 p_3} \right) \]  \hspace{1cm} (4.9)

For a properly compensated system, it is known a priori that the poles are widely separated so that a dominant pole approximation will be used,

\[ |p_3| \gg |p_2| \gg |p_1|. \]  \hspace{1cm} (4.10)

This permits the denominator \( d(s) \) to be simplified to:

\[ d(s) = 1 + \left( -\frac{1}{p_1} \right) s + \left( \frac{1}{p_1 p_2} \right) s^2 + \left( -\frac{1}{p_1 p_2 p_3} \right) s^3 \]  \hspace{1cm} (4.11)

This simplification now permits identification of the coefficients of \( d(s) \) with the constants \( \gamma_1, \gamma_2 \) and \( \gamma_3 \).

Identifying \(-1/p_1 \) with \( \gamma_1 \):

\[ -\frac{1}{p_1} \approx G_{m2} R_1 R_2 C_c (1 + \delta_1) \]  \hspace{1cm} (4.12)

39
where \( \delta_1 \) is:

\[
\delta_1 = \frac{1}{G_{m2}R_2} + \frac{C_1}{G_{m2}R_2C_c} + \frac{C_4}{G_{m2}R_2C_c} + \frac{1}{G_{m2}R_1} + \frac{C_2}{G_{m2}R_1C_c} + \frac{R_c}{G_{m2}R_1R_2} \tag{4.13}
\]

Several assumptions can be stated that can then simplify equation 4.12. These assumptions are:

\[
G_{m2}R_1 \gg 1 \tag{4.14}
\]
\[
G_{m2}R_2 \gg 1 \tag{4.15}
\]
\[
R_c \ll R_2 \tag{4.16}
\]
\[
C_4 \ll C_c \tag{4.17}
\]

Employing these assumptions, a first-order approximation can be expressed for \( p_1 \):

\[
p_1 = -\frac{1}{G_{m2}R_1R_2C_c + R_1C_c + R_1C_1 + R_2C_c + R_2C_2}. \tag{4.18}
\]

Typically, a zero-order approximation provides adequate accuracy:

\[
p_1 = -\frac{1}{G_{m2}R_1R_2C_c}. \tag{4.19}
\]

Evaluation of equation 4.18 should be used to validate the zero-order approximation. Identifying \( \frac{1}{p_1p_2} \) with \( \gamma_2 \):

\[
\frac{1}{p_1p_2} = R_1C_cR_2C_2 + R_1C_1R_2C_c + R_1C_1R_2C_2 + R_1C_1R_cC_c + R_1C_4R_2C_c + R_1C_4R_2C_2 + R_1C_4R_cC_c + R_cC_cR_2C_2 \tag{4.20}
\]

\[
\frac{1}{p_1p_2} = R_1C_cR_2C_2 + R_1C_1R_2C_c + R_1C_1R_2C_2 + R_1C_1R_cC_c + R_1C_4R_2C_c + R_1C_4R_2C_2 + R_1C_4R_cC_c + R_cC_cR_2C_2 \tag{4.21}
\]

Using equation 4.19, equation 4.20 can be solved for \( p_2 \). Simplifying the result of this substitution leads to:

\[
p_2 = \frac{-G_{m2}C_c}{C_1C_c(1+\delta_2) + C_2C_c(1+\delta_3) + C_4C_c(1+\delta_2) + C_1C_2 + C_4C_2} \tag{4.22}
\]

where \( \delta_2 \) and \( \delta_3 \) are:

\[
\delta_2 = \frac{R_c}{R_2} \tag{4.23}
\]
\[
\delta_3 = \frac{R_c}{R_1}. \tag{4.24}
\]

Adding to the assumptions given by equations 4.14 through 4.17,

\[
R_c \ll R_1 \tag{4.25}
\]
equation 4.22 is simplified to:

\[ p_2 = \frac{-G_{m2}C_c}{C_1C_c + C_2C_c + C_1C_2 + C_4(C_c + C_2)} \]  \hspace{1cm} (4.26)

Frequently, \( C_2 \) is larger than \( C_c, C_1 \) and \( C_4 \). When this is the case, equation 4.26 can be expressed as:

\[ p_2 \approx \frac{-G_{m2}}{C_2}. \]  \hspace{1cm} (4.27)

Since \( p_2 \) is the first non-dominant pole, the phase margin of the loop transmission \( a(s) \) is primarily determined by this location of this pole. Thus, it is important to use equation 4.26 to validate the approximations leading to equation 4.27.

Identifying \(-1/p_1p_2p_3\) with \( \gamma_3 \):

\[- \frac{1}{p_1p_2p_3} = R_cC_cR_2C_2R_1(C_4 + C_1) \]  \hspace{1cm} (4.28)

Using equations 4.19 and 4.26, equation 4.28 can be solved for \( p_3 \). Simplifying the result of this substitution leads to:

\[ p_3 = \frac{-1}{R_c} \left( \frac{1}{C_2} + \frac{1}{C_c} + \frac{1}{C_1 + C_4} \right) \]  \hspace{1cm} (4.29)

Usually, \( p_3 \) is far beyond the first non-dominant pole \( p_2 \). As a result, \( p_3 \) negligibly affects the frequency response of the system. In general, equation 4.29 should be checked to validate this assertion.

The system function \( a(s) \) also has two right-half plane zeroes. Referring to equation 4.5:

\[ z_1 = \frac{G_{m1}}{C_4} \]  \hspace{1cm} (4.30)

\[ z_2 = \frac{1}{C_c(1/G_{m2} - R_c)}. \]  \hspace{1cm} (4.31)

Right-half plane zeros are not desirable as they contribute negative phase-shift while increasing the magnitude. This degrades the phase-margin if these zeroes are in the vicinity of the unity-gain frequency of the loop-transmission. The zero \( z_2 \) can be pushed out to infinity by setting:

\[ R_c = \frac{1}{G_{m2}}. \]  \hspace{1cm} (4.32)

The d-c gain of the two-stage op-amp is seen to be simply:

\[ a_0 = G_{m1}G_{m2}R_1R_2 \]  \hspace{1cm} (4.33)

The unity-gain frequency can be approximated by considering only the dominant pole \( p_1 \) in \( a(s) \):

\[ a(s) \approx \frac{G_{m1}G_{m2}R_1R_2}{G_{m2}R_1R_2C_c s} = \frac{G_{m1}}{C_c s}. \]  \hspace{1cm} (4.34)
As a result, the unity-gain or crossover frequency is:

\[ \Omega_c \approx \frac{G_{m1}}{C_c} \]  

(4.35)

The first non-dominant pole is related to the unity-gain frequency by:

\[ \left| \frac{p_2}{\Omega_c} \right| = \frac{G_{m2}C_c}{G_{m1}C_2}. \]  

(4.36)

Since \( |p_2| \propto G_{m2} \), it is desirable for \( G_{m2} \) to be as large as possible. The zero \( z_1 \) is related to the unity-gain frequency by:

\[ \left| \frac{z_1}{\Omega_c} \right| = \frac{C_c}{C_4}. \]  

(4.37)

Thus, it is desirable that \( C_4 \) is as small as possible. When \( R_c = 0 \), the zero \( z_2 \) is related to the unity-gain frequency by:

\[ \left| \frac{z_2}{\Omega_c} \right| = \frac{G_{m2}}{G_{m1}} \]  

(4.38)

In the case of a BiCMOS two-stage op-amp using a MOS first stage and a bipolar second stage, \( G_{m2} \gg G_{m1} \) so \( z_2 \) is not critical. This is to be contrasted with CMOS two-stage op-amps where \( G_{m2} \approx G_{m1} \). Thus, \( z_2 \) plays more importance in CMOS op-amps and in that case it is critical that \( R_c \) is selected properly in order to compensate the op-amp properly.

It has been shown for the two-stage amplifier model in Fig. 4.3 that the frequency response is dictated primarily by a relatively low frequency dominant pole \( p_1 \) and a broad-banded non-dominant pole \( p_2 \). This constitutes the pole-split compensation for the amplifier. With the frequency response of a general two-stage amplifier determined, the differential and common mode amplifier frequency response can be considered in terms of the two-stage model.

With the two-stage model analyzed, the parameters in the two-stage model can now be expressed in terms of circuit parameters. Referring to Fig. 4.1 and observing the right-half side of the active circuit, it can be seen that for the differential mode:

\[
\begin{align*}
C_{1dm} &= C_{db1} + C_{ca7} \\
C_{2dm} &= C_{db19} + C_{cs3} + C_{nb} + C_L \\
C_{3dm} &= C_{gs1} \\
C_{4dm} &= C_{gd1}
\end{align*}
\]  

(4.39)  

(4.40)  

(4.41)  

(4.42)

The transconductances for the differential mode are readily found as:

\[
\begin{align*}
G_{m1dm} &= g_{m1} \\
G_{m2dm} &\approx \frac{g_{mq2}}{1 + V_{B2}/V_{th} + V_{E2}/V_{th}}
\end{align*}
\]  

(4.43)  

(4.44)
The resistances can be determined using Thevenin equivalents and are simplified as:

\[
R_{1dm} \approx r_{o1} \quad (4.45)
\]
\[
R_{2dm} \approx \left[ r_{o20}r_{o19}g_{m19} \right] \parallel \left[ r_{oq2}(1 + g_{mq2}R_E2)\beta \right] \quad (4.46)
\]

For the common mode, the parameters \( G_{m1} \) and \( R_1 \) are different. The first stage transconductance becomes:

\[
G_{m1cm} = \frac{g_m}{2} \quad (4.47)
\]

The first stage resistance is:

\[
R_{1cm} \approx \left[ r_{oq7}(1 + g_{mq7}R_{N1}) \right] \parallel \left[ 2r_{o10}r_{o9}g_{m9}g_{m1} \right] \parallel \left[ \beta(r_{x2} + \beta R_{E2}) \right] \quad (4.48)
\]

The differential input pair devices for the common mode and differential mode have the same geometry and bias current. As a result, the unity-gain frequencies for the common mode and differential mode are related as \( \Omega_{ccm} = \Omega_{cmd}/2 \).

### 4.1.4 Pole-Split Compensation Limitations

Two-stage op-amps typically involve the use of an emitter follower between the first stage and the second stage common emitter amplifier in order to prevent loading and consequent reduction in the d-c gain. The inclusion of the emitter follower can present difficulties because of an extra pole contributed essentially from the parasitic base resistance \( R_B \) and \( C_s \) of the common emitter amplifier. Referring to Fig. 4.1, the value of \( R_B \) for devices \( Q_2 \) and \( Q_5 \) in the second stage is important. An excessive value of \( R_B \) for these devices can lead to peaking in the op-amp frequency response magnitude in two-stage op-amp designs because of a failure in pole-splitting [25]. This peaking, of sufficient magnitude, can compromise the stability of the op-amp. The extra pole included from the emitter follower prevents high frequency broad-banding of the non-dominant pole \( p_2 \) and results in a complex pole pair in the vicinity of the crossover frequency. Typically, this complex pole pair will extend the bandwidth and can be exploited for broad-band amplifier applications but is not acceptable for high-frequency op-amp designs used in closed loops.

Given certain values for \( R_B \) and \( C_s \), the pole-splitting failure can arise from a second stage transconductance that is too large [25]. The second stage transconductance \( G_{m2} \) is determined by transistor \( Q_2 \) and can be shown to be:

\[
G_{m2} = \frac{I_{Q2}/V_{th}}{1 + V_{B2}/V_{th} + V_{E2}/V_{th}} \quad (4.49)
\]

where \( V_{th} \) is the thermal voltage \( kT_\theta/q \), \( V_{B2} \) is the quiescent voltage across \( R_{B2} \) and \( V_{E2} \) is the quiescent voltage across \( R_{E2} \). Reduction in the quiescent current \( I_{Q2} \) is the most direct way to reduce the transconductance but also reduces the positive slew rate and also reduces other bias currents unless the bias network is suitably designed. Increasing \( V_{B2} \) can only be accomplished by increasing \( R_{B2} \) when holding
Increasing $V_{E2}$ by increasing $R_{E2}$ is an effective method to reduce $G_{m2}$ without affecting the bias current. Notice also that increasing $R_{E2}$ decreases the effective capacitance seen by $R_B$. If $G_{m2}$ is reduced excessively to suppress peaking, then the phase-margin of the op-amp will suffer as the non-dominant pole is not sufficiently broad-banded. Although $G_{m2}$ is reduced, the d-c gain does not decrease significantly because the output resistance seen into the bipolar cascode increases, by virtue of increased $R_{E2}$, thus offsetting most of the reduction in transconductance. However, the second stage output resistance also depends on the Thevenin resistance into the PMOS active load. Thus, the amount of d-c gain recovered may be small if the PMOS active load dominates the total output resistance. When it is not possible to reduce $R_{B2}$, inclusion of extra emitter degeneration resistance $R_{E2}$ can be used to reduce peaking in a two-stage amplifier without changing the bias-current and possibly with only a modest reduction in d-c gain.

From an overall design standpoint, the strategy used to address the peaking is to first emphasize layout design techniques that can be used to minimize $R_B$. For a given process, this strategy can have the largest impact on the value of $R_B$. In the BICMOS op-amp circuit, the bipolar devices in the second stage use a p$^+$ base surround around the emitter in order to minimize $R_B$ and thus minimize the peaking. In addition, the emitter aspect ratio is chosen such that the longest dimension of the emitter is as close as possible to the p$^+$ base surround thus diminishing this base resistance contribution.

Since the absolute value of circuit parameters can be difficult to establish in integrated circuit processes, another strategy is to provide flexibility in the circuit design to permit tradeoffs if necessary. In particular, the bias current for the second stage should be independently variable from other bias currents. As will be seen in the discussion of the bias network, this bias circuit design has other advantages.

### 4.1.5 Feedback Amplifier Loop Transmission

The two-stage op-amp frequency response analysis above assumed that the op-amp input was driven with a voltage source. In the case where the op-amp is used in switched-capacitor closed-loop amplifiers, the op-amp inputs are no longer presented with voltage sources. The effect of the Miller capacitance $C_4$, shown in Fig. 4.3, on the loop transmission depends on the source impedance of the input. Analysis of the loop transmission for this case becomes relatively complex as the op-amp in the loop is an OTA (Output Transconductance Amplifier) design. As a result, the output voltage depends on the output current unlike in conventional op-amps that use low impedance output buffers. Fig. 4.4 shows a differential-mode model of a fully differential switched-capacitor closed loop amplifier utilizing a two-stage op-amp. The two halves of the op-amp are assumed to have the same parameters. Using this model, the objective is to determine the loop transmission of the closed-loop amplifier without approximation and then observe limiting cases. The loop transmission will be examined at d-c and at the unity-gain frequency of the loop.
Figure 4.4: Differential-mode model of a fully differential switched-capacitor closed-loop amplifier utilizing a two-stage op-amp. Identical op-amp halves are assumed.

The KCL equations for the system shown in Fig. 4.4 will first be derived:

\[
\frac{V_{s0}(s) - V_{s1}(s)}{Z_1} + \frac{V'_{s3}(s) - V_{s1}(s)}{Z_2} - V_{s1}(s)C_{3s} + (V_{s2}(s) - V_{s1}(s)) = 0 \tag{4.50}
\]

\[
\frac{V'_{s0}(s) - V_{s1}(s)}{Z_1} + \frac{V_{s3}(s) - V'_{s1}(s)}{Z_2} - V'_{s1}(s)C_{3s} + (V'_{s2}(s) - V'_{s1}(s)) = 0 \tag{4.51}
\]

\[
(V_{s1}(s) - V_{s2}(s))C_{4s} - G_{m1}V_{s1}(s) - \frac{V_{s2}(s)}{R_1} - V_{s2}(s)C_{1s} + \frac{V_{s3}(s) - V_{s2}(s)}{R_c + 1/C_{cs}} = 0 \tag{4.52}
\]

\[
(V'_{s1}(s) - V'_{s2}(s))C_{4s} - G_{m1}V'_{s1}(s) - \frac{V'_{s2}(s)}{R_1} - V'_{s2}(s)C_{1s} + \frac{V'_{s3}(s) - V'_{s2}(s)}{R_c + 1/C_{cs}} = 0 \tag{4.53}
\]

\[
\frac{V_{s2}(s) - V_{s3}(s)}{R_c + 1/C_{cs}} - G_{m2}V_{s2}(s) - \frac{V_{s3}(s)}{R_2} - V_{s3}(s)C_{2s} + \frac{V'_{s1}(s) - V_{s3}(s)}{Z_2} = 0 \tag{4.54}
\]
\[
\frac{V_{s2}'(s) - V_{s3}'(s)}{R_c + 1/C_c s} - G_{m2}V_{s2}'(s) - \frac{V_{s3}'(s)}{R_2} - V_{s3}(s)C_{2 s} + \frac{V_{s1}(s) - V_{s3}'(s)}{Z_2} = 0
\] (4.55)

The following definitions will simplify the analysis:

\begin{align*}
V_0(s) &\equiv V_{s0}(s) - V_{s0}'(s) & \quad (4.56) \\
V_1(s) &\equiv V_{s1}(s) - V_{s1}'(s) & \quad (4.57) \\
V_2(s) &\equiv V_{s2}(s) - V_{s2}'(s) & \quad (4.58) \\
V_3(s) &\equiv V_{s3}(s) - V_{s3}'(s) & \quad (4.59)
\end{align*}

Now, subtracting equations 4.51, 4.53, 4.55 from 4.50, 4.52, 4.54, respectively, and using the above definitions results in the following set of governing equations:

\[
\frac{V_0(s) - V_1(s)}{Z_1} + \frac{-V_3(s) - V_1(s)}{Z_2} - V_1(s)C_{3 s} + (V_2(s) - V_1(s))C_{4 s} = 0
\] (4.60)

\[
(V_1(s) - V_2(s))C_{4 s} - G_{m1}V_1(s) - \frac{V_2(s)}{R_1} - V_2(s)C_{1 s} + \frac{V_3(s) - V_2(s)}{R_c + 1/C_c s} = 0
\] (4.61)

\[
\frac{V_2(s) - V_3(s)}{R_c + 1/C_c s} - G_{m2}V_2(s) - \frac{V_3(s)}{R_2} - V_3(s)C_{2 s} + \frac{-V_1(s) - V_3(s)}{Z_2} = 0
\] (4.62)

These equations can be rewritten in a form amenable for representation by a block diagram:

\begin{align*}
V_1(s) &= \frac{V_0(s)(Z_2/Z_1) - V_3(s) + V_2(s)f_2(s)}{a_1(s)} & \quad (4.63) \\
V_2(s) &= V_1(s)a_2(s) + V_3(s)f_1(s) & \quad (4.64) \\
V_3(s) &= V_2(s)a_3(s) - V_1(s)b_1(s) & \quad (4.65)
\end{align*}

The system functions \(a_1(s), a_2(s), a_3(s), b_1(s), f_1(s)\) and \(f_2(s)\) are:

\begin{align*}
a_1(s) &= \frac{1}{Z_2 (1/Z_1 + 1/Z_2 + C_{3 s} + C_{4 s}) - C_{3 s} - G_{m1}} & \quad (4.66) \\
a_2(s) &= \frac{1/R_1 + 1/(R_c + 1/C_c s) + C_{1 s} + C_{4 s}}{1/(R_c + 1/C_c s) - G_{m2}} & \quad (4.67) \\
a_3(s) &= \frac{1/Z_2 + 1/R_2 + 1/(R_c + 1/C_c s) + C_{2 s}}{1/Z_2 + 1/R_2 + 1/(R_c + 1/C_c s) + C_{2 s}} & \quad (4.68)
\end{align*}
\[ b_1(s) = \frac{1}{Z_2 \left( \frac{1}{Z_2} + \frac{1}{R_2} + \frac{1}{(R_c + 1/C_c s) + C_2 s} \right)} \]  

(4.69)

\[ f_1(s) = \frac{1}{1 + (R_c + 1/C_c s)(1/R_1 + C_1 s + C_4 s)} \]  

(4.70)

\[ f_2(s) = Z_2 C_4 s \]  

(4.71)

A block diagram of this system of equations is shown in Fig. 4.5. At this point, the impedances \( Z_1 \) and \( Z_2 \) are introduced. For proper operation of switched-capacitor circuits, the \( RC \) time constant of the switch network must be much smaller than the sampling period of the system. As a result, the impedance of a series capacitor and sampling switch is dominated by the capacitor when the switch is on. Thus, the impedances \( Z_1 \) and \( Z_2 \) are:

\[ Z_1 = \frac{1}{C_{f1}s} \]  

(4.72)

\[ Z_2 = \frac{1}{C_{f2}s} \]  

(4.73)

With these impedances, the following definitions can be stated:

\[ \alpha_1 = \frac{1}{Z_2 \left( \frac{1}{Z_1} + \frac{1}{Z_2} + C_3 s + C_4 s \right)} = \frac{1}{1 + C_{f1}/C_{f2} + (C_3 + C_4)/C_{f2}} \]  

(4.74)

\[ \alpha_2 = Z_2 C_4 s = \frac{C_4}{C_{f2}} \]  

(4.75)

The block diagram in Fig. 4.5 demonstrates the loop transmission readily. By injecting \( V_T(s) \) at the indicated break in the loop, the loop transmission \(-g(s) = -V_3(s)/V_T(s)\). The system of equations that determines the loop transmission are derived from the block diagram and the definitions in equations 4.74 and 4.75 resulting in:

\[ V_1(s) - \alpha_1 \alpha_2 V_2(s) = -\alpha_1 V_T(s) \]  

(4.76)

\[ k_1(s)V_1(s) - V_2(s) + k_2(s)V_3(s) = 0 \]  

(4.77)

\[ k_3(s)V_1(s) - k_4(s)V_2(s) + V_3(s) = 0. \]  

(4.78)

where \( k_1(s) \), \( k_2(s) \), \( k_3(s) \) and \( k_4(s) \) are:

\[ k_1(s) = \frac{(C_4 s - G_{m1})R_1(1 + R_c C_c s)}{R_1 C_c s + (1 + R_c C_c s)(1 + R_1 C_1 s + R_1 C_4 s)} \]  

(4.79)

\[ k_2(s) = \frac{R_1 C_c s}{R_1 C_c s + (1 + R_c C_c s)(1 + R_1 C_1 s + R_1 C_4 s)} \]  

(4.80)

\[ k_3(s) = \frac{R_2 C_f 2 s(1 + R_c C_c s)}{1 + R_c C_c s + R_2 C_c s + (R_2 C_2 s + R_2 C_f 2 s)(1 + R_c C_c s)} \]  

(4.81)

\[ k_4(s) = \frac{R_2 C_c s - G_{m2} R_2(1 + R_c C_c s)}{1 + R_c C_c s + R_2 C_c s + (R_2 C_2 s + R_2 C_f 2 s)(1 + R_c C_c s)} \]  

(4.82)

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Figure 4.5: Block diagram of differential-mode model for a closed-loop switched-capacitor amplifier.
The system given by equations 4.76, 4.77 and 4.78 can now be solved for the loop transmission $-g(s) = -V_3(s)/V_T(s)$:

$$- g(s) = \frac{\alpha_1[-k_1(s)k_4(s) + k_3(s)]}{1 + k_2(s)k_4(s) + \alpha_1\alpha_2[k_1(s) - k_2(s)k_3(s)]} \quad (4.83)$$

It is of interest to evaluate the loop transmission $-g(s)$ for $s = 0$ thus determining the d-c gain of the loop. The result of this evaluation is:

$$-g(s)|_{s=0} = \frac{\alpha_1a_0}{1 + \alpha_1\alpha_2G_{m1}R_1} \quad (4.84)$$

where $a_0$ is the d-c gain of the op-amp. It is important to note that when $C_4 > 0$ the d-c loop gain $\alpha_1a_0$ is attenuated by the factor $1 + \alpha_1\alpha_2G_{m1}R_1$. Consider the ratio $\eta_g$ of the d-c loop transmissions as a function of $C_4$:

$$\eta_g = \frac{-g(s)|_{s=0,C_4=0}}{-g(s)|_{s=0,C_4>0}} \quad (4.85)$$

Using equations 4.74 and 4.75 this ratio becomes:

$$\eta_g = 1 + \frac{C_4(1 + G_{m1}R_1)}{C_{f1} + C_{f2} + C_3} \quad (4.86)$$

Notice that $G_{m1}R_1$ is the d-c gain of the first stage of the op-amp. The effect of the capacitance $C_4$ is increased by $1 + a_1$, hence the Miller effect. For a given feedback network and first stage gain $a_1 = G_{m1}R_1$, the ratio $\eta_g$ can become substantially greater than unity for large gate-drain capacitance $C_4$. Since the d-c gain of the loop determines the closed loop accuracy, the capacitance $C_4$ affects the overall system accuracy.

The loop transmission $-g(s)$ will now be examined for frequencies near the unity-gain frequency of the loop, $s = j\Omega_{cp}$. Referring to equations 4.79 through 4.82:

$$k_1(j\Omega_{cp}) \approx \frac{-G_{m1}}{(C_c + C_1 + C_4)j\Omega_{cp}} \quad (4.87)$$

$$k_2(j\Omega_{cp}) \approx \frac{C_c}{C_c + C_1 + C_4} \quad (4.88)$$

$$k_3(j\Omega_{cp}) \approx \frac{C_{f2}}{C_{f2} + C_2 + C_c} \quad (4.89)$$

$$k_4(j\Omega_{cp}) \approx \frac{-G_{m2}}{(C_c + C_2 + C_{f2})j\Omega_{cp}} \quad (4.90)$$

where it has been assumed that:

$$|R_cC_cj\Omega_{cp}| \ll 1, \quad |R_1C_cj\Omega_{cp}| \gg 1 \quad (4.91)$$

$$|R_1C_1j\Omega_{cp}| \gg 1, \quad |R_1C_4j\Omega_{cp}| \gg 1 \quad (4.92)$$

$$|R_2C_{f2}j\Omega_{cp}| \gg 1, \quad |R_2C_{f2}j\Omega_{cp}| \gg 1 \quad (4.93)$$

$$|R_2C_cj\Omega_{cp}| \gg 1, \quad |(G_{m2}/C_c)j\Omega_{cp}| \ll 1 \quad (4.94)$$

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These inequalities are well satisfied for typical values associated with high d-c gain and high unity-gain frequency op-amp designs. With the approximations in equations 4.87 through 4.90 in place, the loop transmission can be approximated as:

\[
-g(j\Omega_{cp}) \approx -\frac{k_1(j\Omega_{cp})}{k_2(j\Omega_{cp})}
\]  

(4.95)

where it is assumed that:

\[
|k_1(j\Omega_{cp})k_2(j\Omega_{cp})| \gg |k_3(j\Omega_{cp})| \\
|k_2(j\Omega_{cp})k_4(j\Omega_{cp})| \gg 1 \\
|k_2(j\Omega_{cp})k_4(j\Omega_{cp})| \gg \alpha_1\alpha_2 [k_1(j\Omega_{cp}) - k_2(j\Omega_{cp})k_3(j\Omega_{cp})]
\]

(4.96)  

(4.97)  

(4.98)

These assumptions can be shown to be satisfied for typical design values. Now, with the assumptions in place, equation 4.95 is supported. Using equations 4.87 and 4.88, the loop transmission can be expressed as:

\[
-g(j\Omega_{cp}) = \frac{\alpha_1 G_{m1}}{C_c j\Omega_{cp}}
\]

(4.99)

Thus, the unity-gain frequency for the loop is:

\[
\Omega_{cp} = \frac{\alpha_1 G_{m1}}{C_c}
\]

(4.100)

Since \(\alpha_1\) is relatively insensitive to \(C_4\), the unity-gain frequency of the loop is not affected greatly by the inclusion of \(C_4\). However, it is important to realize that the d-c gain of the loop is reduced by inclusion of \(C_4\).

### 4.1.6 Transient Response

In order to understand the settling time of a closed loop switched-capacitor amplifier, the step response of a two-pole feedback system will be analyzed. As was seen in the analysis of the op-amp frequency response, the first non-dominant pole and the dominant pole dictate the frequency response for a two-stage BiCMOS op-amp. Consider a two-pole feedback system with forward transmission \(a(s)\) and feedback transmission \(f(s)\). This system is shown in Fig. 4.6. For the settling time analysis, the feedback will be assumed to be a constant. Thus, the transmissions are:

\[
a(s) = \frac{a_0}{(1 + \tau_0 s)(1 + \tau_1 s)}
\]

(4.101)

\[
f(s) = f_0
\]

(4.102)

The closed loop system function will be denoted as \(A(s)\) where:

\[
A(s) = \frac{a(s)}{i + a(s)f(s)}
\]

(4.103)
Using equations 4.101 and 4.102 the closed loop system function can be expressed as:

\[ A(s) = A_0 \left( \frac{1}{1 + 2\zeta \frac{s}{\Omega_n} + \frac{s^2}{\Omega_n^2}} \right) \]  

(4.104)

where:

\[ A_0 = \frac{a_0}{1 + a_0 f_0} \]  

(4.105)

\[ \frac{2\zeta}{\Omega_n} = \frac{\tau_0 + \tau_1}{1 + a_0 f_0} \]  

(4.106)

\[ \frac{1}{\Omega_n^2} = \frac{\tau_0 \tau_1}{1 + a_0 f_0} \]  

(4.107)

Since the closed loop gains of individual switched-capacitor amplifier are relatively low in the pipeline converter, the loop transmission at d-c is large, hence \( a_0 f_0 \gg 1 \).

As a result:

\[ A_0 \approx \frac{1}{f_0} \]  

(4.108)

\[ \frac{2\zeta}{\Omega_n} \approx \frac{\tau_0 + \tau_1}{a_0 f_0} \]  

(4.109)

\[ \frac{1}{\Omega_n^2} \approx \frac{\tau_0 \tau_1}{a_0 f_0} \]  

(4.110)

Using equations 4.109 and 4.110, \( \zeta \) can be obtained:

\[ \zeta = \frac{\tau_0 + \tau_1}{2\sqrt{\tau_0 \tau_1 a_0 f_0}} \]  

(4.111)

Now, the two-stage op-amp results in pole-splitting so it can be assumed that \( \tau_0 \gg \tau_1 \).

Thus the quantities \( \zeta \) and \( \Omega_n \zeta \) become:

\[ \zeta = \frac{1}{2\sqrt{a_0 f_0}} \frac{\sqrt{\tau_0}}{\tau_1} \]  

(4.112)
\[ \Omega_n \zeta = \frac{1}{2\tau_1} \] (4.113)

It will be useful to express the quantities \( \zeta \) and \( \Omega_n \zeta \) as functions of \( a_0 f_0 \), \( \tau_0 \) and \( \phi_m \) instead of \( a_0 f_0 \), \( \tau_0 \) and \( \tau_1 \), where \( \phi_m \) is the phase-margin of the loop. Consider the loop transmission for the system:

\[-g(s) = \frac{a_0 f_0}{(1 + \tau_0 s)(1 + \tau_1 s)} \] (4.114)

At the crossover frequency of the loop, \( \Omega_{cp} \), the magnitude of each side of equation 4.114 results in:

\[ 1 = \frac{a_0 f_0}{\sqrt{[1 + (\Omega_{cp} \tau_0)^2][1 + (\Omega_{cp} \tau_1)^2]}} \] (4.115)

Near the crossover frequency, the phase angle of the loop transmission is:

\[ \arg[-g(j\Omega)] \approx -\frac{\pi}{2} - \tan^{-1} \Omega \tau_1 \] (4.116)

where it is assumed that \( \tau_0 \gg \tau_1 \). The phase margin of the system is denoted as \( \phi_m \):

\[ \phi_m = \pi + \arg[-g(j\Omega_{cp})] \] (4.117)

Combining equations 4.116 and 4.117 results in:

\[ \Omega_{cp} \tau_1 = \tan \left( \frac{\pi}{2} - \phi_m \right) = \frac{1}{\tan \phi_m} \] (4.118)

Using this result back into equation 4.115:

\[ 1 \approx \left( \frac{a_0 f_0}{\Omega_{cp} \tau_0} \right) \left( \frac{\tan \phi_m}{\sec \phi_m} \right) \] (4.119)

This can be simplified and expressed in terms of \( \Omega_{cp} \):

\[ \Omega_{cp} = \left( \frac{a_0 f_0}{\tau_0} \right) \sin \phi_m \] (4.120)

where the gain-bandwidth product is \( \Omega_{gb} \equiv a_0 f_0 / \tau_0 \). Using equations 4.118 and 4.120, equations 4.112 and 4.113 can be rewritten as:

\[ \zeta = \frac{\sin \phi_m}{2\sqrt{\cos \phi_m}} \] (4.121)

\[ \Omega_n \zeta = \frac{a_0 f_0 \sin^2 \phi_m}{2\tau_0 \cos \phi_m} \] (4.122)

The frequency \( \Omega_n \) can be determined by taking the ratio of equations 4.122 and 4.121:

\[ \Omega_n = \frac{a_0 f_0 \sin \phi_m}{\tau_0 \sqrt{\cos \phi_m}} \] (4.123)
The response $Y(s)$ of the closed system to an input $X(s) = x_0/s$ is $Y(s) = A(s)X(s)$ where $x_0$ is the input step amplitude. The inverse Laplace transform of $Y(s)$ yields [26]:

$$y(t) = x_0 \left( \frac{a_0}{1 + a_0 f_0} \right) \left[ 1 - \frac{1}{\sqrt{1 - \zeta^2}} e^{-\Omega_n \zeta t} \sin \left( \sqrt{1 - \zeta^2} \Omega_n t + \psi \right) \right]$$  \hspace{1cm} (4.124)

where $\tan \psi = \sqrt{1 - \zeta^2}/\zeta$. The output approaches the final value to within a tolerance $\delta$ when:

$$\frac{1}{\sqrt{1 - \zeta^2}} e^{-\Omega_n \zeta t_f} = \delta$$  \hspace{1cm} (4.125)

The time $t_f$ can be solved for yielding:

$$t_f = \frac{1}{\Omega_n \zeta} \ln \left( \frac{1}{\delta \sqrt{1 - \zeta^2}} \right)$$  \hspace{1cm} (4.126)

The time $t_x$ denotes the time that $y(t)$ first reaches:

$$y(t_x) = x_0 \left( \frac{a_0}{1 + a_0 f_0} \right)$$  \hspace{1cm} (4.127)

This value of $y(t)$ is reached when the following condition is met:

$$\sqrt{1 - \zeta^2} \Omega_n t_x + \psi = \pi, \quad 0 < \psi < \pi/2$$  \hspace{1cm} (4.128)

This allows $t_x$ to be determined:

$$t_x = \frac{\pi - \psi}{\Omega_n \sqrt{1 - \zeta^2}}$$  \hspace{1cm} (4.129)

The average slew rate of the output is the output voltage change over the time interval $t_x$ divided by $t_x$. As a result:

$$\frac{\Delta y(t)}{\Delta t} \approx \frac{x_0}{f_0 t_x}, \quad 0 < t < t_x$$  \hspace{1cm} (4.130)

Typically, this slew rate will exceed a maximum permissible slew rate dependent on the circuit implementation. In this event, the output $y(t)$ will exhibit slew rate limiting and the system will require a longer time to meet the tolerance $\delta$ predicted by $t_f$. The settling time then includes a slewing portion and a fine settling portion. A conservative way to express the settling time is to add the slewing and fine settling portions:

$$t_s = \frac{x_0}{f_0} \left[ \frac{\Delta y(t)}{\Delta t} \right]_{\text{max}}^{-1} + t_f - t_x$$  \hspace{1cm} (4.131)

This expression can overestimate the settling time because the output may only exceed the maximum slew rate for a brief time. If the maximum slew rate is not exceeded, then the settling time is essentially:

$$t_s = t_f$$  \hspace{1cm} (4.132)
Referring to Fig. 4.1, the positive slew rate is determined by the quiescent current in the second stage and the output load capacitance:

\[ S_R^+ = \frac{I_{M19}}{(C_L + C_c)} \]  

(4.133)

The negative slew-rate is typically limited by the first stage bias current and the compensation capacitance:

\[ S_R^- = \frac{I_{M9}}{C_c} \]  

(4.134)

The finite slew-rate of the op-amp typically constitutes 1/4 to 1/2 of the total settling time for the desired A/D converter throughput and full scale voltage. It is important to recognize that the slew rate component of the settling time can be reduced by scaling down the full scale voltage. Thus, for a given desired accuracy level, the full scale voltage should be chosen as small as possible.

### 4.1.7 Switched-Capacitor Common Mode Feedback

The dynamic common mode output level sense circuit is shown in Fig. 4.2. Capacitors \( C_{CM1} \) and \( C_{CM2} \) are used to derive voltage \( V_{CM} \) from \( V_{OUT1} \) and \( V_{OUT2} \). Voltage \( V_{CM} \) represents the output common mode level. By using capacitors to sense the output common mode level, the differential and common mode d-c gain of the op-amp are not affected. In addition, the use of a capacitor sense network does not degrade the differential output range. In order to provide a frequency independent common mode sense function with the capacitor network, the input to the common mode amplifier must also be capacitive. As a result, a MOS device is used for this input, namely \( M_3 \). The capacitive sense network is periodically refreshed by capacitors \( C_{CM3} \) and \( C_{CM4} \) using a MOS switch network and non-overlapping clock phases \( \phi_1 \) and \( \phi_2 \). The MOS switch network is composed of CMOS devices \( M_{25} \) through \( M_{36} \).

Assuming that the common mode amplifiers are matched, a half circuit suffices for analysis. The basic switched-capacitor common mode feedback half circuit is shown in Fig. 4.7. Notice that only half of the leakage current is directed from the common mode amplifier input. An ideal common mode amplifier will be assumed to simplify the analysis. Assuming that the \( RC \) time constants associated with the switches are sufficiently small compared to the common mode feedback clock period, charge transfer is complete and the switch resistance will be neglected. In Fig. 4.7, the common mode output is \( V_{cmo} \), the common mode reference is \( V_{cmr} \) and the refresh reference voltage is \( V_m \). The capacitor \( C_{cm3} \) is refreshed by connecting across \( V_m \) and then connecting across capacitor \( C_{cm1} \) using non-overlapping clock phases \( \phi_{f1} \) and \( \phi_{f2} \). Consider first the charge on \( C_{cm3} \):

\[ q_{cm3}(n-1) = C_{cm3} V_m(n-1) \]  

(4.135)

At this point in time, the charge on \( C_{cm1} \) is:

\[ q_{cm1}(n-1) = C_{cm1} [V_{cmo}(n-1) - V_{cmr}(n-1)] \]  

(4.136)
NOTE:
VF1 controls: SCM3, SCM4
VF2 controls: SCM1, SCM2

Figure 4.7: Basic switched-capacitor common mode feedback circuit with ideal common mode amplifier.
The total charge is then:

\[ q_1(n - 1) = q_{cm1}(n - 1) + q_{cm3}(n - 1) \]
\[ = C_{cm1}[V_{cmo}(n - 1) - V_{cmr}(n - 1)] + C_{cm3}V_m(n - 1) \]  \hspace{1cm} (4.137)

When capacitor \(C_{cm3}\) is connected across capacitor \(C_{cm1}\), the charge will redistribute and can be expressed as:

\[ q_2(n) = (C_{cm1} + C_{cm3})[V_{cmo}(n) - V_{cmr}(n)] \]  \hspace{1cm} (4.139)

Conservation of charge requires:

\[ q_2(n) - q_1(n - 1) = q_z(n) \]  \hspace{1cm} (4.140)

The quantity \(q_z(n)\) represents an arbitrary charge that arises from sources excluding \(V_m(n)\) and \(V_{cmr}(n)\). This charge \(q_z(n)\) is primarily developed from leakage currents at the common mode amplifier input, as shown in Fig. 4.7. The difference equation in equation 4.140 can now be written as:

\[ (C_{cm1} + C_{cm3})[V_{cmo}(n) - V_{cmr}(n)] - C_{cm3}V_m(n - 1) \]
\[ - C_{cm1}[V_{cmo}(n - 1) - V_{cmr}(n - 1)] = q_z(n) \]  \hspace{1cm} (4.141)

Performing the z-transform on each side of this equation assuming the zero-state and then collecting terms results in:

\[ V_{cmo}(z) = V_{cmr}(z) + V_m(z) \left( \frac{C_{cm3}}{C_{cm1} + C_{cm3}} \right) \left[ \frac{z^{-1}}{1 - C_{cm1}z^{-1}/(C_{cm1} + C_{cm3})} \right] \]
\[ + Q_z(z) \left( \frac{1}{C_{cm1} + C_{cm3}} \right) \left[ \frac{z^{-1}}{1 - C_{cm1}z^{-1}/(C_{cm1} + C_{cm3})} \right] \]  \hspace{1cm} (4.142)

It is important to notice that the common mode output responds directly to \(V_{cmr}(z)\) as an ideal common mode amplifier was assumed. With a finite bandwidth amplifier, the common mode output \(V_{cmo}(t)\) will respond to \(V_{cmr}(t)\) with a time-constant determined by the amplifier bandwidth. In this case, the amplifier time-constant would be reflected in \(V_{cmo}(n)\) and hence in \(V_{cmo}(z)\). The output \(V_{cmo}(z)\) responds to \(V_m(z)\) and \(Q_z(z)\) with time constants determined by the ratio of \(C_{cm3}\) to \(C_{cm1}\). This can be seen by observing the poles of the system functions that multiply \(V_m(z)\) and \(Q_z(z)\), respectively, in equation 4.142. As a result, the larger \(C_{cm3}\) is relative to \(C_{cm1}\) the faster that the output responds to \(V_m(z)\) and \(Q_z(z)\), respectively.

With the leakage current denoted as \(I_k(t)/2\), the charge \(q_z(t)\) that results after one common common feedback circuit clock period \(T_{cm}\) is:

\[ q_z(t) \equiv \int_{t-T_{cm}}^{t} \frac{I_k(t')}{2} \, dt' \]  \hspace{1cm} (4.143)
Typically, $I_k(t)$ is a constant $I_{k0}$. The above integral will now be evaluated for $t = nT_{cm}/2$:

$$q_z(nT_{cm}/2) = \frac{I_{k0}}{2} \left( nT_{cm}/2 - nT_{cm}/2 + T_{cm} \right)$$

$$q_z(n) = \frac{I_{k0}T_{cm}}{2}$$

(4.144)

Thus, $q_z(n)$ is a constant. For the case where $V_{cmr}(n)$ and $V_m(n)$ are also constant, equation 4.142 becomes:

$$V_{cmo}(z) = \frac{V_{cmo0}}{1 - z^{-1}} + \frac{V_{m0}}{1 - z^{-1}} \left( \frac{C_{cm3}}{C_{cm1} + C_{cm3}} \right) \left[ \frac{z^{-1}}{1 - C_{cm1}z^{-1}/(C_{cm1} + C_{cm3})} \right]$$

$$+ \frac{I_{k0}T_{cm}}{2(C_{cm1} + C_{cm3})(1 - z^{-1})} \left[ \frac{z^{-1}}{1 - C_{cm1}z^{-1}/(C_{cm1} + C_{cm3})} \right]$$

(4.146)

Using the final-value theorem for the z-transform,

$$\lim_{n \to \infty} V_{cmo}(n) = \lim_{z \to 1} (z - 1)V_{cmo}(z)$$

(4.147)

the final value of the output is determined as:

$$\lim_{n \to \infty} V_{cmo}(n) = V_{cmr0} + V_{m0} + \frac{I_{k0}T_{cm}}{2C_{cm3}}$$

(4.148)

Thus, for a given leakage current and capacitance it is important that the clock period is sufficiently small in order that the output common mode level $V_{cmo}(n)$ stays close to the target $V_{cmr}(n) + V_m(n)$. Notice that the last term in equation 4.148 depends only on the refresh capacitance $C_{cm3}$. With the non-overlapping clock phases, this capacitor provides the charge needed to support the leakage current $I_{k0}$ while maintaining a desirable output common mode level.

Since the leakage current is generally small, typically in the 1 pA to 1 nA range, the switches in Fig. 4.2 can use minimum geometry [24]. The gate-drain capacitance of the switches connected to the common mode amplifier input $V_{CM}$ constitutes an input impedance between the clock and $V_{CM}$. Thus, an inverting amplifier is completed with the feedback impedance consisting of the common mode sense capacitors. Since the clock swings the full power supply range, the resulting output common mode level deviation can be significant. Thus, using minimum geometry switches has the added advantage of minimizing the closed loop gain from the switch clocks to the common mode output.

### 4.1.8 Bias Network

Fig. 4.1 shows the bias circuit along with the main op-amp circuit. Current sources with an improved cascode [13] structure are used to provide larger output compliance along with higher effective output resistance. The general structure of the improved
Figure 4.8: General structure of an improved cascode current source.
cascode current source is shown in Fig. 4.8. The design of this current source is important for obtaining the highest possible d-c gain from the available devices. The following relations hold among the device geometries:

\[(W/L)_2 = (W/L)_3 = (W/L)_4 \quad (4.149)\]
\[(W/L)_5 = (W/L)_6 = N(W/L)_2 \quad (4.150)\]
\[(W/L)_2 = P(W/L)_1 \quad (4.151)\]

The drain currents are basically related as:

\[I_{d1} = I_{d2} = I_{d3} = I_{d4} = I_{ref} \quad (4.152)\]
\[I_{out} = NI_{ref} \quad (4.153)\]

The drain current for the MOS devices is simply:

\[I_d = \frac{k'W}{2L} (\Delta V)^2 \quad (4.154)\]

where \(\Delta V = V_{GS} - V_T\), \(k' = \mu C_{ox}\). The drain-source voltage \(V_{DS6}\) will be of interest. Notice that this voltage can be expressed via KVL as:

\[V_{DS6} = V_{GS1} + V_{GS2} - V_{GS3} - V_{GS5} \quad (4.155)\]

Since \((W/L)_2 = (W/L)_3\) and \(I_{d2} = I_{d3}\), it is found that \(V_{GS2} = V_{GS3}\). Thus:

\[V_{DS6} = V_{GS1} - V_{GS5} = \Delta V_1 - \Delta V_5 \quad (4.156)\]

Note that:

\[NI_{ref} = \frac{k'}{2}(W/L)_6 (\Delta V_6)^2 \quad (4.157)\]

Using equations 4.152, 4.154, 4.156 and 4.157 it is straightforward to show that:

\[V_{DS6} = \Delta V_6 (\sqrt{P} - 1) \quad (4.158)\]

Defining the voltage \(V_{cs} = V_{DD} - V_{out}\),

\[\min V_{cs} = V_{DS6} + \Delta V_5 = V_{DS6} + \Delta V_6 \quad (4.159)\]

Using equations 4.158 and 4.159:

\[\min V_{cs} = \sqrt{P} \Delta V_6 \quad (4.160)\]

In [13], the ratio \(P\) is chosen as 4. This results in \(V_{DS6} = \Delta V_6\) so that device \(M_{cs}\) is on the border between the ohmic and saturation regions. Second order effects in the MOS device I-V characteristic leads to a transition that is non-ideal. Biasing the device in this transition region results in a decrease of output resistance compared to biasing in saturation. In addition, device mismatches can result in a bias point that
would not place device $M_{c6}$ on the border between the ohmic and saturation region. As a result, a situation can then occur where device $M_{c6}$ is in the ohmic region. In this case, the output resistance can be significantly lower, depending on the operating point, compared to biasing in saturation. If this current source design were used as an active load of the op-amp second-stage, the d-c gain could be significantly lower. As a result, the ratio $P = 4$ should be avoided. By choosing $P > 4$, a margin of error for bias uncertainty is achieved although the output compliance is not as large as possible. However, a small reduction in the output compliance has far less impact on system accuracy than a potentially large decrease in the output resistance and hence the d-c gain of the op-amp. A ratio of $P \geq 5$ is preferred.

The current mirror $Q_7$, $Q_8$ and $Q_9$ acts as an active load for biasing the first stage in addition to being used as a current mirror for the common mode differential input pair $M_3$ and $M_4$. Since the tail currents for the differential and common mode differential pairs are the same, a 1:1 current mirror ratio is used to minimize systematic offset. Thus, the emitter degeneration resistors $R_{N1}$, $R_{N2}$, and $R_{N3}$ are all set equal.

Split bias current sources are provided for the op-amp for two reasons. First, this scheme permits independent control of the bias current of the first and second stages of the op-amp. This is important for decoupling the issues relating the first and second stages. With the first-stage bias current set, the unity-gain frequency is set since the unity-gain frequency depends on $G_{m1}$. The second-stage current is important in governing the frequency response because the non-dominant pole frequency and the pole-splitting depend on $G_{m2}$. Also, the second-stage current determines the positive slew rate. As a result, increasing the positive slew rate capability without increasing the unity-gain frequency, and thus decreasing phase-margin, can improve the settling time. In another scenario, positive slew rate can be traded off for reduced peaking without reduction in the unity-gain frequency. Thus, the op-amp circuit is more flexible to parameter variations with this kind of bias scheme.

A second reason for using a split bias scheme is to decouple differential output signals from the input stage bias network of the op-amp. During transient conditions, output signal swings can disturb the bias of the first stage leading to increased settling time. By using the split bias scheme, this coupling mechanism can be effectively reduced.

### 4.1.9 Differential Mode Thermal Noise

Thermal noise represents a substantial component of the total input referred noise. Analysis of the differential mode noise referred to the input basically involves the first stage of the op-amp. The noise contributed by the second-stage is attenuated by the first-stage gain when referred to the input. Typically, this attenuated component is much smaller than first-stage components. The incremental subcircuit used in the obtaining the first-stage noise components is shown in Fig. 4.9. The input devices $M_1$ and $M_2$ each contribute to the input referred noise by virtue of their channel
Figure 4.9: First-stage incremental subcircuit used for thermal noise analysis of op-amp.

resistance. The input referred PSD for a MOS device is shown in [13] and is:

\[
S_{\text{vg}} = 4kT_\theta \left( \frac{2}{3g_m} \right) \tag{4.161}
\]

The PSDs of devices \( M_1 \) and \( M_2 \) are uncorrelated so that the differential noise contributed by the input devices is:

\[
S_{\text{v1}} = \frac{8kT_\theta}{3} \left( \frac{1}{g_{m1}} + \frac{1}{g_{m2}} \right) \tag{4.162}
\]

The bipolar devices \( Q_7 \) and \( Q_8 \) can contribute a significant input referred noise component because of the large transconductance ratio between bipolar and MOS devices. The emitter resistance \( R_{N1} \) is used to reduce the input referred thermal noise due to \( Q_7 \) by reducing the effective transconductance of \( Q_7 \). However, the value of \( R_{N1} \) cannot be increased arbitrarily as an excessively large value would lead to saturation of \( Q_7 \) for the bias currents of interest. As a result, \( R_{N1} \) is chosen to reduce the effective transconductance of \( Q_7 \) while satisfying bias constraints. The input referred noise from the bipolar devices and degeneration resistors can be analyzed by considering the input referred noise contribution from each related source and then summing the independent results. The MOS devices, bipolar devices and degeneration resistors in the first-stage will be assumed to be independent while using the same parameter values. The Thevenin equivalent resistance seen into each base of \( Q_7 \) and \( Q_8 \) is denoted \( R_i \) while the equivalent resistance seen into each emitter of these devices is denoted \( R_o \). The following assumptions will then be used to simplify the analysis:

\[
R_N \equiv R_{N1} = R_{N2} = R_{N3} \tag{4.163}
\]
\[ \frac{1}{g_{m9}} \ll R_N \]  
\[ R_i \gg R_N \]  
\[ R_o \ll R_N \]  

Consider the current PSD \( S_{id7} \). The bottom leg of this current is connected to a relatively low resistance, dominated by the emitter resistance \( R_o \). The top leg is connected to an equivalent resistance that is \( R_i \parallel R_i \parallel R_N \approx R_N \). Thus, the top leg resistance is where most of the voltage will be developed due to this current PSD. This voltage \( v_1 \) drives both bases of the bipolar devices. As a result, the differential input referred thermal noise from \( S_{ib7} \) will be mostly canceled if \( M_1 \) and \( M_2 \) have the same parameter values. Even with expected mismatches, this current PSD does not significantly contribute to the input referred noise. A similar argument applies to current PSD \( S_{id8} \). Since voltage PSD \( S_{vrn3} \) drives both bipolar bases, a common mode input referred noise is the expected result so this PSD can also be neglected for the same reason the current PSDs were neglected.

Since it is assumed that \( R_i \gg R_N \), the voltage PSD \( S_{vb7} \) drives the base of \( Q_T \) directly resulting in the drain noise current PSD for \( M_1 \) as:

\[ S_{id1} = (g'_{m7})^2 S_{vb7} \]  

(4.167)

The voltage PSD \( S_{vb8} \) can be analyzed in the same manner resulting in the drain noise current PSD for \( M_2 \) as:

\[ S_{id2} = (g'_{m8})^2 S_{vb8} \]  

(4.168)

The effective bipolar transconductance is reduced because of the emitter degeneration and can be expressed as:

\[ g'_m = \frac{1}{\frac{1}{g_{mq}} + R_N(1 + 1/\beta)} \]  

(4.169)

With \( 1/g_{mq} \ll R_N \) and \( \beta \gg 1 \), this expression is simplified to:

\[ g'_m \approx \frac{1}{R_N} \]  

(4.170)

The input referred noise component is:

\[ S_{v2} = \left( \frac{g'_m}{g_m} \right)^2 (S_{vb7} + S_{vb8}) \]  

(4.171)

The noise contributed from the degeneration resistors can be found easily when using the assumption that \( R_o \ll R_N \). The input referred noise component then becomes:

\[ S_{v3} = \left( \frac{1}{g_m R_N} \right)^2 (S_{vrn1} + S_{vrn2}) \]  

(4.172)

The total input referred thermal noise is expressed as the sum of the three independent PSD components given by equations 4.162, 4.171 and 4.172. Since the parameter
values are equal between the two current source structures, the total input referred thermal noise PSD becomes:

\[ S_v = 8kT_\theta \left( \frac{2}{3g_m} + 8kT_\theta R_B \left( \frac{g'_m}{g_m} \right)^2 + 8kT_\theta R_N \left( \frac{1}{g_m R_N} \right)^2 \right) \] (4.173)

Using the approximation for \( g'_m \) in equation 4.170, and rearranging terms in equation 4.173, the total input referred noise PSD becomes:

\[ S_v = 8kT_\theta \left[ \frac{2}{3g_m} + \frac{R_B + R_N}{(g_m R_N)^2} \right] \] (4.174)

Since the unity-gain frequency of the loop transmission is proportional to \( g_m/C_c \), the input referred noise power is then proportional to \( kT_\theta/C_c \) when the second term is negligible compared to the first term in equation 4.174.

### 4.1.10 Power Supply and Common Mode Rejection Ratios

The power supply rejection of the op-amp is primarily a function of the circuit topology. A perfectly balanced fully differential architecture provides infinite power supply rejection for the differential mode. In practice, mismatches in circuit elements is the primary method for power supply noise transmission to differential mode noise. Mismatch in the first stage of the op-amp is most important as the resulting noise is not attenuated by the loop transmission. In general, the further down the forward transmission path that noise signals are injected, the more loop transmission that is available for rejection of the noise [26]. Thus, the Power Supply Rejection Ratio (PSRR) is highly dependent on the mismatch of the input differential pair and active load. Using high output resistance current sources to bias the input differential pair can improve the power supply rejection. Frequently, the current sources used to bias the op-amp are neglected as ideal current sources can be used in SPICE simulations. In an actual system, the current source implementation can modulate the reference bias current when there is power supply noise. This can be problematic at frequencies where the output impedance of even a cascoded current source can be seriously degraded. Thus, it is important to design the current sources used to provide reference bias currents to have the highest output impedance over the widest frequency range.

Differential mode errors arising from common mode signals occur when there are mismatches in the differential signal path. Since the op-amp uses a common mode feedback scheme, the common mode rejection is largely determined by the common mode feedback loop transmission below the \(-3dB\) frequency of the loop. Since the common mode closed loop gain is low and the gain-bandwidth product of the common mode loop is comparable to the differential loop, the \(-3dB\) frequency for this loop is relatively high. Above this frequency, the loop transmission magnitude is reduced and the common mode rejection properties are then determined by the input stage tail current source. Thus, in order to achieve a high Common Mode Rejection Ratio (CMRR), it is desirable to maintain a large common mode loop transmission and to use high output impedance current sources.
4.2 Comparator Pre-Amplifier Design

4.2.1 Topology Selection

The primary function of the comparator pre-amplifier is to provide sufficient gain to overcome the input referred offset of the latch circuit. As was discussed in 3, an open loop pre-amplifier circuit is chosen in order to meet the pipeline converter throughput and accuracy requirements. The open loop circuit is simpler compared to a feedback circuit but the open loop circuit involves a tradeoff between the d-c gain and dynamic range.

One possible pre-amplifier design uses a folded-cascode structure with a PMOS input differential pair connected to a n-p-n or NMOS bipolar cascode. However, such a structure suffers from low d-c gain because of the low transconductance of the input PMOS differential pair. The low input transconductance can be compensated by using high output resistance current sources in the output cascode. However, the gain bandwidth product of this amplifier at the desired -3dB frequency suffers because of the high resistance level in the output cascode. Another difficulty with using active loads with high output resistance is that the common mode operating point is difficult to establish because of the sensitivity in the operating point to the bias current. As a result, common mode feedback is then needed to set the output common mode level.

In order to alleviate these difficulties, the relatively high transconductance of n-p-n bipolar devices is exploited. By using n-p-n devices as amplifiers, the gain-bandwidth product needed for the pre-amplifier can be achieved. In addition, this high transconductance permits the use of relatively low valued resistor loads while achieving the desired d-c gain. As a result of the lower load resistor values, the common mode level is easier to set compared to using high resistance active loads, for a given bias current level. The desired pre-amplifier is a two-stage, fully differential design using a PMOS differential pair as the first stage and a bipolar differential pair with cascode devices in the second stage.

The pre-amplifier is presented in $F_{\infty}$. 4.10. The substrates for NMOS and PMOS devices are implicitly connected to $V_{SS}$ and $V_{DD}$, respectively, unless otherwise indicated. The p-well substrates for all n-p-n devices and poly-$n^+$ capacitors are connected to $V_{SS}$.

4.2.2 Overview of Comparator Pre-Amplifier Circuit

The pre-amplifier employs a PMOS differential pair in the first stage composed of devices $M_1$ and $M_2$, shown in Fig. 4.10. The PMOS devices provide a purely capacitive input impedance necessary for switched-capacitor systems. The first stage loads are composed essentially of resistors $R_{E1}$ and $R_{E2}$. The second stage uses a bipolar differential pair composed of transistors $Q_2$ and $Q_3$. A novel scheme is used to establish the bias of the second stage. The devices $Q_1$, $Q_2$, $Q_3$ and $Q_4$ comprise a current mirror using the first stage PMOS drains as reference currents thus establishing the bias for
Figure 4.10: BiCMOS comparator pre-amplifier.
the second stage differential pair. As a result, a separate current source is not needed to establish bias for the second stage. A cascode structure composed of devices $Q_6$ and $Q_8$ is used to extend the bandwidth of the pre-amplifier. Resistors $R_{L1}$, $R_{L2}$ and $R_{L3}$ are used as the loads for the second stage. A common mode feedback scheme is not needed for this fully differential pre-amplifier as the output common mode level is set by the bias current and the load resistors. Emitter followers $Q_7$ and $Q_9$ are used to buffer the second stage outputs.

### 4.2.3 Frequency Response

Wideband amplifier designs frequently employ cascode structures in order to extend the $-3\text{dB}$ bandwidth. Typically, the increased bandwidth resulting from this technique, and others, is welcome when the throughput of the circuit is the primary concern. However, the increased bandwidth of the circuit also increases the thermal noise power referred to the input and thus reduces the accuracy of a pipelined A/D converter employing such a circuit. Since the thermal noise PSD is difficult to reduce for MOS devices without great expense in power dissipation or area, it is important to realize that the bandwidth of the circuit should only be as high as is needed to meet the specification, with a reasonable margin. The frequency response requirements for the pre-amplifier do not require that the circuit use a cascode structure. However, without the cascode structure, the resulting bandwidth leaves little margin for error because of the gain-bandwidth product needed. Thus, the design strategy is to employ the cascode so that the circuit is capable of exceeding the frequency response specification. Then, the bandwidth of the circuit is intentionally reduced so that the input referred noise power does not become excessive.

Referring to Fig. 4.10 and considering the half circuit for differential operation, the dominant pole of the pre-amplifier is:

$$p_1 = -R_{L1}C_{L1}$$  \hspace{1cm} (4.175)

The first non-dominant pole is contributed by the cascode circuit and can be determined using the Miller approximation:

$$p_2 = \frac{-1}{g_{m5}R_{L1}(4g_{m9})C_{\mu5}}$$  \hspace{1cm} (4.176)

where it is assumed that $g_{m9} = g_{m10} = g_{m11} = g_{m12}$. The second non-dominant pole is contributed by the bipolar differential amplifier:

$$p_3 = \frac{-1}{g_{m2}(1/g_{m5})R_{E1}C_{\mu2}}$$  \hspace{1cm} (4.177)

The pre-amplifier also exhibits a right-half plane zero from the gate-drain capacitance of the input PMOS differential pair. In a manner similar to the frequency response of the op-amp, it can be shown that this right-half plane zero is located at:

$$z_1 = \frac{g_{m1}}{C_{gd1}}$$  \hspace{1cm} (4.178)
When the non-dominant poles and the right-half plane zero are sufficiently beyond the dominant pole, the -3dB frequency of the pre-amplifier is essentially:

\[
\Omega_b = \frac{1}{R_{L1}C_{L1}}
\]  

(4.179)

The differential d-c gain of the pre-amplifier is readily found as:

\[
a_0 = g_{m1} (R_{E1} \parallel r_{\pi2}) g'_{m2} R_{L1}
\]

(4.180)

where \( g'_{m2} \) is the effective transconductance of bipolar transistor \( Q_2 \) expressed as:

\[
g'_{m2} = \frac{I_2/V_{th}}{1 + V_{B2}/V_{th} + V_{E2}/V_{th}}
\]

(4.181)

and where \( I_2, V_{B2} \) and \( V_{E2} \) are the quiescent collector current, parasitic base resistor voltage and parasitic emitter resistance voltage, respectively. The d-c gain of the pre-amplifier system used in the comparator is affected by the gate-drain capacitance at the input PMOS differential pairs because of the Miller effect at the first stage. However, since the gain of the first stage is relatively low in the pre-amplifier, the effective input capacitance due to the Miller effect is not significant compared to coupling capacitors used between pre-amplifiers and between the second pre-amplifier and the latch.

### 4.2.4 Transient Response

There are two phases of operation of interest for the comparator pre-amplifier. The first is the amplification phase where two pre-amplifiers are connected together with the final output driving the latch. The second is the offset cancellation phase where each pre-amplifier is performing open loop offset cancellation independently.

The system function for the amplification phase is given as:

\[
A(s) = \frac{\alpha_p}{(1 + \tau_0)^2}
\]

(4.182)

where \( 1/\tau_0 \) is the dominant pole frequency and \( \alpha_p \) is the d-c gain of the system, including attenuation between pre-amplifiers. Consider an step input \( X(s) = x_0/s \) where \( x_0 \) is the step amplitude. Thus, \( Y(s) = A(s)X(s) \) is the ZSR output response. The inverse Laplace transform of \( Y(s) \) can be calculated as:

\[
y(t) = \alpha_p x_0 \left[ 1 - e^{-t/\tau_0} - \left( t/\tau_0 \right) e^{-t/\tau_0} \right] u(t)
\]

(4.183)

The worst case scenario in the amplification phase is when the smallest anticipated input is presented to the pre-amplifier system. The output of the pre-amplifier system must then amplify this voltage to reach the offset voltage of the latch, \( V_{OSL} \), in order to trigger a correct decision when the latch is strobed. It will be assumed that the
pre-amplifier was properly offset cancelled prior to the amplification phase. Consider \( f(t) \) where
\[
f(t) = (1 + m)e^{-m} \tag{4.184}
\]
and \( m = t/\tau_0 \). At the time \( t_a \), the pre-amplifier output is at \( V_{OSL} \) so \( f(t_a) \) is then related as:
\[
f(t_a) = 1 - \left| \frac{V_{OSL}}{a_p x_0} \right| \tag{4.185}
\]
Once the value of \( f(t_a) \) is known, equation 4.184 can be solved iteratively to determine \( m_a \) thus determining the amplification time \( t_a = m_a \tau_0 \).

For open loop offset cancellation, each pre-amplifier output must settle to the output referred offset, \( a_0 V_{OSP} \), where \( V_{OSP} \) is the input referred offset of the pre-amplifier. If the pre-amplifier output was previously at an initial voltage \( V(0) \), then the settling time \( t_{oc} \) has elapsed when:
\[
\left| \frac{V(0) - a_0 V_{OSP}}{a_0} \right| e^{-t_{oc}/\tau_0} = V_{err} \tag{4.186}
\]
where \( V_{err} \) is the input referred error due to incomplete settling. The settling time can be now be solved yielding:
\[
t_{oc} = \tau_0 \ln \left| \frac{V(0) - a_0 V_{OSP}}{a_0 V_{err}} \right| \tag{4.187}
\]
The worst case situation for the offset cancellation occurs when \( V(0) \) and \( V_{OSP} \) have the same sign.

In order to analyze the large signal behavior of the pre-amplifier, the differential halves will be assumed matched. Thus, \( R_{E3} = R_{E1} \) and \( R_{L2} = R_{L1} \). Also, \( I_{d9} = I_{d11} \). In a balanced state, \( V_{i1} = V_{i2} \). Thus, the current \( I_{c5} = I_{c6} \) and \( I_{c5} \) can be expressed as:
\[
I_{c5} = \left( \frac{I_{d3}}{2} + I_{d9} \right) \frac{R_{E1}}{2R_{E2}} \tag{4.188}
\]
Thus, \( V_{o1} = V_{o2} \) and \( V_{o1} \) can be expressed as:
\[
V_{o1} = V_{DD} - R_{L3} \left( \frac{I_{d3}}{2} + I_{d9} \right) \frac{R_{E1}}{R_{E2}} - R_{L1} \left( \frac{I_{d3}}{2} + I_{d9} \right) \frac{R_{E1}}{2R_{E2}} \tag{4.189}
\]

Now, suppose \( V_{i1} - V_{i2} = V_{id} \) where \( V_{id} < 0 \) and is of sufficient magnitude to cause device \( M_2 \) to be in the cutoff state. The base voltages \( V_{B2} \) and \( V_{B3} \) are related as:
\[
V_{B2} = (I_{d3} + I_{d9})R_{E1} + V_{BE1} \tag{4.190}
\]
\[
V_{B3} = I_{d9}R_{E1} + V_{BE4} \tag{4.191}
\]
Thus, it is found that:
\[
V_{B2} - V_{B3} = I_{d3}R_{E1} + \Delta V_{BE} \approx I_{d3}R_{E1} \tag{4.192}
\]

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When $I_{d3}R_{E1} \gg V_{th}$ then device $Q_3$ is in the cutoff state and $I_{eb} = 0$. The current $I_{c5}$ is then:

$$I_{c5} = (I_{d3} + I_{d9}) \frac{R_{E1}}{R_{E2}}$$  \hspace{1cm} (4.193)

Thus, the differential output voltage $V_{od} = V_{o1} - V_{o2}$ is determined as:

$$V_{od} = -R_{L1}(I_{d3} + I_{d9}) \frac{R_{E1}}{R_{E2}}$$  \hspace{1cm} (4.194)

The output common mode voltage is $V_{oc} = (V_{o1} + V_{o2})/2$ and is determined as:

$$V_{oc} = V_{DD} - R_{L3}(I_{d3} + I_{d9}) \frac{R_{E1}}{R_{E2}} - \frac{R_{L1}}{2}(I_{d3} + I_{d9}) \frac{R_{E1}}{R_{E2}}$$  \hspace{1cm} (4.195)

It should be noted that the common mode voltage changes between the balanced and unbalanced state for the comparator pre-amplifier. Subtracting equation 4.189 from equation 4.195, the change in the output common mode level is:

$$\Delta V_{oc} = - \left( \frac{R_{L3}}{2} + \frac{R_{L1}}{4} \right) \frac{R_{E1}I_{d3}}{R_{E2}}$$  \hspace{1cm} (4.196)

As long as there is no strict common mode requirement at the input of the latch, the change in the common mode level is not of concern for large input signals. The amplification time $t_a$ is not affected for large signals. Once the pre-amplifier system output reaches $V_{OSL}$, then the regenerative latch will quickly amplify this output and hold the result. With the pre-amplifier in an overdriven state, the offset cancellation time $t_{oc}$ can be degraded because the pre-amplifier must leave the overdriven state and then enter the linear operating region. For this pre-amplifier, this extra time is small relative to $t_{oc}$ predicted for the linear operating region. For the case of small input signals, where the pre-amplifier remains in the linear operating region, the output common mode level remains fixed so the issue of output common mode level change is not of concern.

### 4.2.5 Bias Network

The bias network for the pre-amplifier uses similar principles as with the op-amp. The input stage is biased with an improved cascode current to alleviate bias current modulation resulting from power supply variations. The emitter follower section is biased with an independent current source so as to minimize the disturbance of the input stage bias network under transient conditions. As with the op-amp, this can be important to prevent degradation in settling time; in the case of the pre-amplifier, an increase in the offset cancellation time would be of primary concern.

### 4.2.6 Differential Mode Thermal Noise

As with the op-amp, the input referred thermal noise of the pre-amplifier in the differential mode is a dominant component of the total input referred noise. The
Figure 4.11: Incremental circuit for thermal noise analysis of the comparator pre-amplifier.

noise contributed from the second stage will be neglected as it is attenuated by the gain of the first stage. This assertion can be verified for the two-stage comparator pre-amplifier circuit. The incremental circuit for the noise analysis is shown in Fig. 4.11. The incremental resistances of diode connected devices $Q_1$ and $Q_4$ has been neglected. Assuming the network is symmetrical between the left and right halves, the input referred thermal noise PSD is expressed as:

$$S_{\text{vid}} = 8kT \left( \frac{2}{3g_m} + \frac{1}{g_m^2 R_E} \right) \quad (4.197)$$

where $g_m$ is the transconductance of a PMOS input device and $R_E = R_{E1} = R_{E2}$.

4.2.7 Power Supply and Common Mode Rejection Ratios

Generally, the PSRR of the pre-amplifier depends on the matching properties of the input stage. The fully differential architecture helps to preserve a good power supply rejection ratio at high frequencies. As with the op-amp, attention is required for the design of the current sources used to establish the reference bias currents.

Since the comparator pre-amplifier does not use common mode feedback, the CMRR of the pre-amplifier is primarily dependent on the first stage tail current source. It is desirable to achieve a high output impedance current source to obtain a large CMRR.
4.3 Latch Design

4.3.1 Topology Selection

The purpose of the latch is to amplify the pre-amplifier output to generate a digital output and then hold the state of this digital output. Regenerative designs have been shown to achieve a minimum power-delay product to achieve the necessary amplification [27]. The latch design incorporates a PMOS differential pair in order to provide a simple method to interface a differential input without connecting directly to the latch outputs [17]. The latch is presented in Fig. 4.12.

4.3.2 Overview of Latch Circuit

The basic regenerative latch is composed of cross coupled inverter pairs $M_3$, $M_4$ and $M_5$, $M_6$. The transmission gate $M_8$, $M_9$ acts as a reset switch and device $M_7$ is the latch enable switch. The operation of the circuit is straightforward. The circuit is in the reset mode when $\bar{\phi}_1 = 1$ and $\phi_2 = 1$. When $\phi_2 = 0$, a differential voltage is developed across the latch outputs depending on the PMOS differential input pair. By allowing sufficient time for the differential voltage across the latch outputs to exceed the cross coupled inverter pair offset, the latch outputs will swing to the correct state when subsequently $\bar{\phi}_1 = 0$. The time constant for the cross coupled inverter pair loop transmission is basically $g_m/C_L$ where $g_m$ is the MOS device transconductance and $C_L$ is the capacitance present at the output of an inverter. Since this time constant is on the order of several nanoseconds, the positive feedback will result in a full output voltage in several time constants if the differential input voltage reasonably exceeds the offset voltage. Typically, the response time is less than 10 ns for the smallest anticipated inputs. The latch outputs are each buffered with CMOS inverters to provide the digital output for other circuits on the chip and for output pins. Both outputs are used to retain a fully differential system thus minimizing common mode noise.
Figure 4.12: Latch circuit.
Chapter 5

Simulation Results

This chapter presents the simulation results for the BiCMOS pipeline A/D converter. Simulation results are first presented for the individual circuit blocks used to synthesize the pipeline A/D converter. The simulation results are then shown for the first two stages of the pipeline A/D converter. Basic circuit simulations were performed with HSPICE on µVAX computers. Since predicting the behavior of switched-capacitor systems at the circuit level can be time consuming, the long transient solutions for the A/D converter system level were performed with HSPICE using a CRAY2 supercomputer. The HSPICE input file used for the BiCMOS pipeline A/D converter is given in appendix B.

5.1 BiCMOS Operational Amplifier

Table 5.1 gives a summary of the BiCMOS operational amplifier simulation results. The simulation results are presented in the following Figures. When the effect of mismatches is sought in the following simulations, only the op-amp mismatches are included. For these cases, 1% mismatch for MOS device channel lengths and 0.1% mismatch for passive components are used.

The differential mode frequency response is shown in Fig. 5.1. The common mode feedback loop is broken and the common mode frequency response is shown in Fig. 5.2.

With mismatches in place, the common mode rejection is shown in Fig. 5.3. The CMRR is the ratio of the common mode rejection frequency response to the differential mode frequency response. The positive and negative PSRRs are shown in Figs. 5.4 and 5.5, respectively. For these simulations, the op-amp was in a unity-gain connection. It should be noted that these rejection ratios imply small signal disturbances. In the actual system, the large signal sine wave or step response associated with the respective rejection ratios provides a more accurate measure of the differential error incurred.

The step response is shown in Fig. 5.6. A 5 V input is used and the settling time is determined for 16-bit accuracy based on a 10 V full scale. The step response is
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>differential mode d-c gain</td>
<td>114 dB</td>
</tr>
<tr>
<td>differential mode unity-gain frequency</td>
<td>150 MHz</td>
</tr>
<tr>
<td>differential mode phase margin</td>
<td>60°</td>
</tr>
<tr>
<td>common mode d-c gain</td>
<td>114 dB</td>
</tr>
<tr>
<td>common mode unity-gain frequency</td>
<td>71 MHz</td>
</tr>
<tr>
<td>common mode phase margin</td>
<td>65°</td>
</tr>
<tr>
<td>CMRR</td>
<td>&gt; 81 dB at 1 MHz</td>
</tr>
<tr>
<td>positive PSRR</td>
<td>&gt; 85 dB at 1 MHz</td>
</tr>
<tr>
<td>negative PSRR</td>
<td>&gt; 81 dB at 1 MHz</td>
</tr>
<tr>
<td>input referred noise</td>
<td>11 nV/√Hz</td>
</tr>
<tr>
<td>slew rate</td>
<td>330 V/μsec</td>
</tr>
<tr>
<td>capacitive loading per output</td>
<td>6 pF</td>
</tr>
<tr>
<td>step response max settling time (16-bit)</td>
<td>33 ns</td>
</tr>
<tr>
<td>differential output range</td>
<td>12 V</td>
</tr>
<tr>
<td>power supply</td>
<td>±5 V</td>
</tr>
<tr>
<td>power dissipation</td>
<td>82 mW</td>
</tr>
</tbody>
</table>

Table 5.1: BiCMOS operational amplifier simulation results.

obtained with a closed loop gain of -1 connection. This connection reflects the lowest loop transmission used for op-amps in the pipeline A/D converter. As a result, the worst case settling time can be predicted for the amplification mode of the switched-capacitor amplifiers. The step response including the effects of mismatches is shown in Fig. 5.7. The settling time is not affected when mismatches are included.

The zero input response for the op-amp used in the reset mode of the switched-capacitor amplifier is shown in Fig. 5.8. In this simulation, the op-amp is configured in a unity-gain connection and the initial differential output voltage is set to 5 V. The transient solution is then found. The effect of the reset switch resistance is included as this resistance degrades the phase margin. A reset switch resistance of 250Ω is used. The common mode dynamic response interacts with the differential mode dynamic response and degrades the settling time in this particular case. The settling time for the reset mode in this case is 48 ns to a 16-bit accuracy level for a 10 V full scale. The initial state assumed is important for determining the ZIR (Zero Input Response) settling time. The ZIR with mismatches included is shown in Fig. 5.9. The settling time in this case does not change compared to the perfectly balanced case.

### 5.2 BiCMOS Comparator Pre-Amplifier

Table 5.2 gives a summary of the BiCMOS comparator pre-amplifier simulation results. The simulation results are presented in the following Figures. When the effect of
Figure 5.1: Differential mode frequency response.

Figure 5.2: Common mode frequency response.
Figure 5.3: Common mode rejection.

Figure 5.4: Positive power supply rejection ratio.
Figure 5.5: Negative power supply rejection ratio.

Figure 5.6: Step response, closed loop gain $-1$. 
Figure 5.7: Step response, closed loop gain $-1$, mismatches included.

Figure 5.8: Zero input response for unity-gain connection.
Figure 5.9: Zero input response for unity-gain connection, mismatches included.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>d-c gain</td>
<td>33 dB</td>
</tr>
<tr>
<td>-3dB bandwidth</td>
<td>38 MHz</td>
</tr>
<tr>
<td>CMRR</td>
<td>&gt; 72 dB at 1 MHz</td>
</tr>
<tr>
<td>positive PSRR</td>
<td>&gt; 79 dB at 1 MHz</td>
</tr>
<tr>
<td>negative PSRR</td>
<td>&gt; 72 dB at 1 MHz</td>
</tr>
<tr>
<td>input referred noise</td>
<td>5 nV/√Hz</td>
</tr>
<tr>
<td>capacitive loading per output</td>
<td>5 pF</td>
</tr>
<tr>
<td>max offset cancel settling time (16-bit)</td>
<td>33 ns</td>
</tr>
<tr>
<td>differential output range</td>
<td>5 V</td>
</tr>
<tr>
<td>power supply</td>
<td>±5 V</td>
</tr>
<tr>
<td>power dissipation</td>
<td>33 mW</td>
</tr>
</tbody>
</table>

Table 5.2: BiCMOS comparator pre-amplifier simulation results.
mismatches is sought in the following simulations, only the pre-amplifier mismatches are included. For these cases, 1% mismatch for MOS device channel lengths and 0.1% mismatch for passive components are used.

Figs. 5.10 and 5.11 show the differential and common mode frequency response, respectively. The common mode rejection is shown in Fig. 5.12. The CMRR is the ratio of the common mode rejection frequency response to the differential mode frequency response. The positive power supply rejection is shown in Fig. 5.13 and the negative power supply rejection is shown in Fig. 5.14. The PSRR is then the ratio of the power supply rejection frequency response to the differential mode frequency response. It should be noted that these rejection ratios imply small signal disturbances. In the actual system, the large signal sine wave or step response associated with the respective rejection ratios provides a more accurate measure of the differential error incurred.

The offset cancellation step response is shown in Fig. 5.15. In this case, the differential input to the pre-amplifier is at a large value and then returned to zero. The output then settles to zero. The effect of mismatches on the offset cancellation step response is shown in Fig. 5.16. The settling time for this case does not increase over the perfectly balanced case.

Two pre-amplifiers are placed in cascade to determine the pre-amplifier system step response. The worst case scenario for the pre-amplifier system is when the input presented is one LSB. The output then must reach the latch offset before a decision can occur. For 16-bit quantization and 10 V full scale, the LSB is about 150 μV. The step response for this LSB input is shown in Fig. 5.17. The output reaches 100 mV in 16 ns. The d-c gain of the pre-amplifier system is 59 dB. As a result, the final value of the step response is about 140 mV. The pre-amplifier step response including mismatches is shown in Fig. 5.18. The response time is unchanged.

5.3 CMOS Latch

The simulation results for the latch are shown in Figs. 5.19 and 5.20. Referring to Fig. 5.19, the cross coupled inverter outputs are denoted as V(3) and V(4). The latch is initially in the reset mode. When the reset switch is turned off, a voltage developed across V(3) and V(4) as a result of a large differential input. When the latch is energized, the outputs diverge and the latch will then be in the hold mode. The clocks for the latch are shown in Fig. 5.20.

5.4 BiCMOS Pipeline A/D Converter

The entire switched-capacitor BiCMOS pipelined A/D converter presents a formidable simulation task from a circuit level. The use of a CRAY2 supercomputer greatly facilitated the transient solutions. The accuracy of the pipeline converter is determined primarily by the first few stages. As a result, placing focus on the first two stages
BICMOS Pre-Amp Differential Mode Frequency Response

Figure 5.10: Differential mode frequency response.

BICMOS Pre-Amp Common Mode Frequency Response

Figure 5.11: Common mode frequency response.
Figure 5.12: Common mode rejection.

Figure 5.13: Positive power supply rejection.
BICMOS Pre-Amp Negative Power Supply Frequency Response

![Frequency Response Graph]

Figure 5.14: Negative power supply rejection.

BICMOS Preamp Step Response

![Step Response Graph]

Figure 5.15: Offset cancellation step response.
Figure 5.16: Offset cancellation step response, mismatches included.

Figure 5.17: Pre-amplifier system step response for LSB input.
Figure 5.18: Pre-amplifier system step response for LSB input, mismatches included.

Figure 5.19: Latch outputs.
provides most of the information that is sought from the simulation.

The simulation effort of fully differential systems depends on the choice of common mode feedback network model. The use of the complete switched-capacitor common mode feedback circuit can greatly extend the simulation time because the common mode level must first stabilize from the initial conditions. The simulation of the first two stages of the pipeline use op-amps employing a simplified common mode feedback network. The primary function of the common mode feedback is to sense the output common mode level. As a result, voltage controlled voltage sources provide an easy means in HSPICE to devise a common mode feedback sense network.

This section presents the simulation results of the first two stages in the pipeline A/D converter. The first stage employs a sample-and-hold switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch. The second stage employs a multiply-by-two switched-capacitor amplifier, an offset cancelled pre-amplifier system and a latch. Other support circuitry, such as digital inverters, are included in the simulation.

Since charge injection errors are signal dependent, the input to the pipeline is a large value in order to examine the resulting system accuracy. However, choosing input signals that are decision levels exercise the comparators in the pipeline. The simulation presented in this section uses a large differential input signal, namely 5 V. Mismatches in the circuit blocks are not included in this case.

In Fig. 5.21, the analog output of the sample-and-hold is shown. Notice that the output alternately settles from 5 V and then to 0 V when reset. Fig. 5.22 shows the analog output for the multiply-by-two. Since the pipeline input is 5 V, the sample-
and-hold output is 5 V. As a result, the MSB is set to 1. This causes the next stage to perform \( V_{out} = 2V_{in} - V_{ref}/2 \), following the reference non-restoring algorithm. Thus, the output of the multiply-by-two will be 5 V. As a result, the LSB is set to 1. Figs. 5.23 and 5.24 show the digital outputs of the sample-and-hold and multiply-by-two stages, respectively. Detailed examination of the analog outputs reveals that this pipeline operates with 15-bit accuracy for a 10 V full scale. However, this only accounts for charge injection errors. In addition, noise and capacitor mismatch will act to reduce the accuracy further.

The clocks for the sample-and-hold analog system are shown in Fig. 5.25. These clocks correctly sequence the switched-capacitor sample-and-hold function. The sample-and-hold digital system clocks are shown in Fig. 5.26. These clocks correctly sequence the latch function in this stage. The clocks for the multiply-by-two analog system are shown in Fig. 5.27. These clocks correctly sequence the switched-capacitor multiply-by-two function. The clocks for the multiply-by-two digital system are shown in Fig. 5.28. These clocks correctly sequence the latch function in this stage.

The period of the clocks is 190 ns. Thus, the throughput of this pipeline is about 5.2 MHz. The clock timing allocates 50 ns for op-amp and pre-amp settling. A substantial amount of time is needed for the clock waveforms to slew. Additional time is allocated to assure non-overlapping clocks. Thus, the total overhead amounts to 90 ns. Less conservative clock timing for 6.25 MHz throughput rate was successful in maintaining more than 14 bits of accuracy.

**Pipeline ADC, N=2; Sample-and-Hold Analog Output**

![Graph showing analog output waveform](image)

Figure 5.21: Sample-and-hold analog output.
Pipeline ADC, $N=2$; Multiply-by-Two Analog Output

Figure 5.22: Multiply-by-two analog output.

Pipeline ADC, $N=2$; Sample-and-Hold Digital Output

Figure 5.23: Sample-and-hold digital output.
Pipeline ADC, N=2; Multiply-by-Two Digital Output

Figure 5.24: Multiply-by-two digital output.

Sample-and-Hold Analog System Clocks

Figure 5.25: Sample-and-hold analog system clocks.
Figure 5.26: Sample-and-hold digital system clocks.

Figure 5.27: Multiply-by-two analog system clocks.
Figure 5.28: Multiply-by-two digital system clocks.
Chapter 6

BiCMOS Op-Amp Test Results

A fully differential BiCMOS op-amp suitable for high performance switched-capacitor circuits was designed, fabricated and tested [28]. This op-amp employs a two-stage, pole-split compensation topology. The basic analog signal path of this op-amp is similar to that presented in this thesis. The op-amp design presented in this thesis addresses some of the limitations observed with the fabricated op-amp.

6.1 Op-Amp Measurements

Experimental results are summarized in Table 6.1. The key performance parameters are a d-c gain of 100 dB, a unity-gain frequency of 90 MHz, a phase margin of 45°, slew rate of 150 V/μs, capacitive loading of 7 pF per output, differential output range of 12 V, ±5 V power supply and 125 mW power dissipation. A 100 μA external current source was used to bias the op-amp. The op-amp is unity-gain stable with the above capacitive loading. The dynamic switched-capacitor common mode feedback was engaged for all op-amp measurements. The associated clock period was 6 μs for φ1 and φ2, respectively. For linear operation, each op-amp output can swing to within 2 V of a ±5 V power supply for zero output common mode level. Thus, each output can swing 6 V so the differential output range is 12 V. For ±3.5 V power supply, the differential output range is 6 V. Although the differential input referred thermal noise PSD was not measured, the simulated value was $1.21 \times 10^{-16}$ V$^2$/Hz or 11 nV/$\sqrt{\text{Hz}}$. A photograph of the op-amp die is shown in Fig. 6.1. The active die area is 1.0 mm x 1.2 mm.

The d-c gain was measured with the op-amp in an open loop connection. The measured value of the d-c gain was less than the target value. The reason for this is partly related to the design of the bias network. Also, the PMOS active loads in the second stage do not use sufficiently long channels.

In Fig. 6.2, the results of the unity-gain frequency measurement are shown. For this measurement, the op-amp is operated in an open-loop configuration. The top waveform is the differential input at 500 mV/div. and the bottom waveform is the differential output at 500 mV/div. The time scale is 5 ns/div. With an input fre-
Figure 6.1: Die photograph of BiCMOS operational amplifier
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>d-c gain</td>
<td>100 dB</td>
</tr>
<tr>
<td>unity-gain frequency</td>
<td>90 MHz</td>
</tr>
<tr>
<td>phase margin</td>
<td>45°</td>
</tr>
<tr>
<td>slew rate</td>
<td>150 V/μsec</td>
</tr>
<tr>
<td>capacitive loading per output</td>
<td>7 pF</td>
</tr>
<tr>
<td>differential output range</td>
<td>12 V</td>
</tr>
<tr>
<td>power supply</td>
<td>±5 V</td>
</tr>
<tr>
<td>power dissipation</td>
<td>125 mW</td>
</tr>
<tr>
<td>active die-area</td>
<td>1.0 mm × 1.2 mm</td>
</tr>
</tbody>
</table>

Table 6.1: BiCMOS operational amplifier measured results.

frequency of 90 MHz, it is seen that the input and output magnitudes are equal. The output waveform is 135° phase shifted with respect to the input waveform. Thus, the unity-gain frequency is 90 MHz with a 45° phase margin. The measured unity-gain frequency is less than the target value. The primary reason for this is that the oxide thickness for the capacitors was smaller than expected. As a result, the compensation capacitor is larger than the design value, thus reducing the unity-gain frequency.

In Fig. 6.3, the op-amp is configured in an open-loop configuration. The top (smaller) waveform is the differential input at 500 mV/div. and the bottom (larger) waveform is the differential output at 500 mV/div. The time scale is 50 ns/div. With an input frequency of 10 MHz, it is seen that the gain of the op-amp is about 11 and that the output waveform is 90° phase shifted with respect to the input waveform. Thus, the gain-bandwidth product of the op-amp is 110 MHz.

In Fig. 6.4, the op-amp is configured for a closed loop gain of −100. The top waveform is the differential input at 20 mV/div. and the bottom waveform is the differential output at 2 V/div. The time scale is 200 ns/div. With an input frequency of 1.1 MHz, the output magnitude is reduced 3 dB compared to a lower frequency case, for constant input magnitude. In addition, the output waveform is about 45° phase shifted with respect to the input waveform, compared to a lower frequency case. Thus, the − dB frequency of the closed loop is 1.1 MHz. This indicates a gain-bandwidth product of 110 MHz for the op-amp. Thus, the gain-bandwidth product has been measured using two different techniques.

In Fig. 6.5, the op-amp is configured for a closed loop gain of −2. The top waveform is the differential input at 2 V/div. and the bottom waveform is the differential output at 2 V/div. The time scale is 50 ns/div. Upon application of a step at the input, it is seen that the output exhibits slew rate limiting. The step response shows a slew rate limit of 150 V/μs for positive and negative output changes. In this closed loop gain of −2 configuration, the loop transmission is about 1/5 to 1/6 of the op-amp loop transmission because of attenuation from the feedback network, op-amp input
Figure 6.2: Unity-gain frequency measurement. Top: diff. input, 500 mV/div. Bottom: diff. output, 500 mV/div. Time scale: 5 ns/div. Unity-gain frequency is 90 MHz with 45° phase margin.
Figure 6.3: Open loop gain-bandwidth product measurement. Top: diff. input, 500 mV/div. Bottom: diff. output, 500 V/div. Time scale: 50 ns/div. Gain-bandwidth product is 110 MHz.
Figure 6.4: Closed loop gain-bandwidth product measurement. Top: diff. input, 20 mV/div. Bottom: diff. output, 2 V/div. Time scale: 200 ns/div. Gain-bandwidth product is 110 MHz.
capacitance and parasitic capacitance from the input pins on the chip-carrier. As a result of the reduced loop transmission, the closed loop exhibits nearly a single pole response after the slew rate limit portion is complete for this configuration.

The op-amp was configured in a closed loop unity-gain connection in order to measure the differential-mode PSRR (Power Supply Rejection Ratio). A PSRR of greater than 45 dB was measured for frequencies up to 1 MHz for the positive and negative power supply rails, respectively.

Op-amp circuits were operated from ±3.5 V up to ±5.5 V power supply, using the same common mode feedback clock period and bias current, without significant change in the performance parameters above. At ±5 V power supply operation, it is expected that certain NMOS devices will be operating near the NMOS drain-source voltage breakdown limit of 7 V. This drain-source voltage can be reduced by placing an NMOS, or n-p-n, cascode device in series with the drain. Process modifications for increasing the NMOS drain-source and n-p-n $L_{CEO}$ breakdown voltages are in progress.

This op-amp was also fabricated using a low-temperature selective silicon epitaxy BiCMOS. This process yielded functional op-amps. The gain-bandwidth product measurement is shown in Fig. 6.6. This gain-bandwidth product was measured using a closed loop gain of −100. The top waveform is the differential input at 5 mV/div.

Figure 6.5: Slew rate measurement. Top: diff. input, 2 V/div. Bottom: diff. output, 2 V/div. Time scale: 50 ns/div. Slew rate is 150 V/μs for positive and negative output changes.
Figure 6.6: Gain-bandwidth product measurement of low-temperature selective silicon epitaxy BiCMOS op-amp.

And the bottom waveform is the differential output at 500 mV/div. The time scale is 200 ns/div. A frequency of 1 MHz is the $-3$dB frequency for the loop. Thus, the gain-bandwidth product is approximately 100 MHz. Details concerning this low-temperature epitaxy are found in [29].
Chapter 7

Conclusion

7.1 Summary

This thesis has presented the design, analysis and simulation of high-performance, fully differential switched-capacitor circuit blocks that are to be used in a BiCMOS pipelined A/D converter. The operational amplifier design has emphasized dynamic response as this circuit primarily determines the throughput of the pipeline A/D converter. A novel comparator pre-amplifier design used in an open loop offset cancelled comparator has been presented. Simulations have indicated a pipeline throughput of greater than 5 MHz for a 10 V full scale. A high frequency, fully differential BiCMOS operational amplifier has been designed, fabricated and tested. The performance measures indicate that this BiCMOS op-amp is suitable for high-performance switched-capacitor applications.

7.2 Future Research

The design of the pipelined BiCMOS A/D converter can be optimized with simulation at the circuit and system level. Incorporating calibration schemes with pipeline architectures has the potential for realizing monolithic high-speed and high-accuracy A/D converters.
Appendix A

M.I.T. BiCMOS Process

A.1 Process Overview

The focus of the M.I.T. BiCMOS process is on building high precision and high speed analog/digital mixed systems for 10 V operation [19]. The process design reflects an emphasis on high performance analog circuit capability in addition to high density digital circuit capability. The devices available in the process are: NMOS, PMOS, vertical n-p-n, vertical p-n-p and poly-n+ capacitor. A cross section of the devices in this process is shown in Fig. A.1.

The process development approach is to integrate the bipolar devices into an existing twin-well CMOS process. The vertical n-p-n devices are fabricated in a selective epitaxial layer deposited after the LOCOS field oxidation step of the CMOS process [30]. This epitaxial layer is deposited on n+ buried islands, located in p-wells. The non-optimized vertical p-n-p bipolar structures are formed by depositing the selective epitaxial layer on CMOS p-wells, without the n+ buried islands, thus using the wells as the collectors. Since there is no buried layer for the p-n-p, its collector resistance is much higher than its n-p-n counterpart. The interconnect system for this BiCMOS process uses a single level of metal and polysilicon. Circuits are fabricated in n-well BiCMOS built on p/p+ epitaxial wafers so that the substrate potential of the PMOS devices can be independent of the power supply.

A.2 Key BiCMOS Device Parameter Summary

Table A.1 shows a summary of the key CMOS device parameters in the BiCMOS process [19]. The CMOS devices feature a 2 μm drawn channel length and a gate-oxide thickness of 23 nm. For the NMOS and PMOS devices, the respective values for the zero-bias threshold voltage are 0.7 V and −0.75 V. The subthreshold slopes are 90.7 mV/Decade and 86.5 mV/Decade. The back-body coefficients are 0.66 V1/2 and 0.26 V1/2, respectively. The drain-source breakdown voltages are 7.0 V and −20 V. The field threshold voltages are 12.9 V and −16.7 V, respectively.

Table A.2 shows a summary of the key Bipolar device parameters in the BiCMOS
Figure A.1: Cross section of the devices in the M.I.T. BiCMOS process.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>NMOS</th>
<th>PMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{\text{DRAWN}}$</td>
<td>2 $\mu$m</td>
<td>2 $\mu$m</td>
</tr>
<tr>
<td>$t_{OX}$</td>
<td>23 nm</td>
<td>23 nm</td>
</tr>
<tr>
<td>$V_{T0}$</td>
<td>0.70 V</td>
<td>-0.75 V</td>
</tr>
<tr>
<td>Sub. Slope</td>
<td>90.7 mV/Decade</td>
<td>86.5 mV/Decade</td>
</tr>
<tr>
<td>Back-Body Coef.</td>
<td>0.66 $V^{1/2}$</td>
<td>0.26 $V^{1/2}$</td>
</tr>
<tr>
<td>$V_{DS \text{ Break. Volt.}}$</td>
<td>7.0 V</td>
<td>-20 V</td>
</tr>
<tr>
<td>$V_T$ (Field)</td>
<td>12.9 V</td>
<td>-16.7 V</td>
</tr>
</tbody>
</table>

Table A.1: Summary of key CMOS device parameters in the M.I.T. BiCMOS process.

process [19]. As the p-n-p device is not optimized, the n-p-n device will be emphasized in the following discussion. The n-p-n bipolar device features a minimum emitter area of $4.5 \mu m \times 4.5 \mu m$, a maximum $h_{FE}$ of 70 and an Early voltage of 44 V. The series collector resistance $R_C$ is 165 $\Omega$ and the series emitter resistance $R_E$ is 11.5 $\Omega$. The series base resistance $R_B$ is estimated as 250 $\Omega$ based on op-amp performance. The collector-base breakdown voltage, $BV_{CBO}$, and the sustaining collector-emitter breakdown voltage, $LV_{CEO}$, are 33 V and 9.2 V respectively. The emitter-base breakdown voltage, $BV_{EBO}$, is 4 V. The maximum $f_T$ is 3.0 GHz for a $4.5 \mu m \times 18 \mu m$ device with $I_C = 5$ mA, $V_{BC} = -4$ V.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>n-p-n</th>
<th>p-n-p</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter Area (Min)</td>
<td>(4.5 μm)$^2$</td>
<td>(9.5 μm)$^2$</td>
</tr>
<tr>
<td>h$_{FE}$ (Max)</td>
<td>70</td>
<td>70</td>
</tr>
<tr>
<td>Early Voltage</td>
<td>44 V</td>
<td>125 V</td>
</tr>
<tr>
<td>$R_C$</td>
<td>165 Ω</td>
<td>7.5 kΩ</td>
</tr>
<tr>
<td>$R_E$</td>
<td>11.5 Ω</td>
<td>11.2 Ω</td>
</tr>
<tr>
<td>$R_B$</td>
<td>250 Ω (est.)</td>
<td>n.a.</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>33 V</td>
<td>&gt; 30 V</td>
</tr>
<tr>
<td>$LV_{CEO}$</td>
<td>9.2 V</td>
<td>&gt; 30 V</td>
</tr>
<tr>
<td>$BV_{EBO}$</td>
<td>4.0 V</td>
<td>33 V</td>
</tr>
<tr>
<td>$C_{jeo}$</td>
<td>77 fF</td>
<td>33 fF</td>
</tr>
<tr>
<td>$C_{jso}$</td>
<td>55.8 fF</td>
<td>51 fF</td>
</tr>
<tr>
<td>$C_{js0}$</td>
<td>320 fF</td>
<td>288 fF</td>
</tr>
<tr>
<td>$f_T$ (Max)</td>
<td>3.0 GHz</td>
<td>200 MHz</td>
</tr>
</tbody>
</table>

Table A.2: Summary of key bipolar device parameters in the M.I.T. BiCMOS process.
Appendix B

HSPICE Input File

The pipeline A/D converter HSPICE input file is given in this appendix. A hierarchical structure is used to build the simulation file. As a result, all of the subcircuits that comprise the pipeline A/D are included in this file.

switched-capacitor pipelined bicmos a/d converter
* sample-and-hold:
  * architecture similar to reference non-restoring
  * multiply-by-two circuit.
  * multiply-by-two:
  * reference non-restoring bicmos multiply-by-two circuit.
  * uses modified multiply-by-two switch arrangement.
  * includes reference switch network.
* comparator preamplifier system:
  * two stage comparator with open loop offset cancellation.
* latch:
  * cmos latch with differential input.
*
* andrew karanicolas
* mit microsystems technology laboratory
* 8-10-90

.include '/u/bicmos/ankleand/bicmos/bicmos_1'
* bicmos hspice models for mixed signal circuit simulation
* derived by ken o
* updated by andrew karanicolas 7-27-90

****************************************************************************** nmos model ****************************
.model nmos nmos
+level=3 vto=0.7 tox=2.3e-8 nsub=1.0e15 uo=550 cgso=3.5e-10
+cgdo=3.5e-10 cj=8.0e-5 mj=0.5 cjsw=5.0e-10 mjsw=0.5 tpg=1
+xj=0.6um ld=0.3um kappa=.15
+capop=4 xqc=.1

105
** nlev=2 kf=8.4e-27
 .model nmos_temp nmos
 +level=3 vto=0.7 tox=2.3e-8 nsub=1.0e15 uo=550 cgso=3.5e-10
 +cgdo=3.5e-10 cj=8.0e-5 mj=0.5 cjsw=5.0e-10 mjsw=0.5 tpg=1
 +xj=0.6um ld=0.3um kappa=.15
 +capop=4 xqc=.1
** nlev=2 kf=8.4e-27
 .model nmos1 nmos
 +level=3 vto=0.7 tox=2.3e-8 nsub=1.0e15 uo=550 cgso=3.5e-10
 +cgdo=3.5e-10 cj=8.0e-5 mj=0.5 cjsw=5.0e-10 mjsw=0.5 tpg=1
 +xj=0.6um ld=0.3um kappa=.15
 +capop=1 xqc=.1
** nlev=2 kf=8.4e-27

****************************************************************************** pmos model **************************************************************************
 .model pmos pmos
 +level=3 vto=-0.7 tox=2.3e-8 nsub=1.0e16 uo=220 cgso=3.5e-10
 +cgdo=3.5e-10 cj=2.0e-4 mj=0.5 cjsw=1.5e-9 mjsw=0.5 tpg=-1
 +xj=0.6um ld=0.3um kappa=1.5
 +capop=4 xqc=.1
** nlev=2 kf=4.2e-27
 .model pmos_temp pmos
 +level=3 vto=-0.7 tox=2.3e-8 nsub=1.0e16 uo=220 cgso=3.5e-10
 +cgdo=3.5e-10 cj=2.0e-4 mj=0.5 cjsw=1.5e-9 mjsw=0.5 tpg=-1
 +xj=0.6um ld=0.3um kappa=1.5
 +capop=4 xqc=.1
** nlev=2 kf=4.2e-27

****************************************************************************** npn model **************************************************************************
 .model npn npn
 +is=8.5e-18 bf=50 vaf=45 cjc=0.145p cje=0.1p cjs=.7p tf=15ps
 +rb=250 rc=60 re=3.5
 .include '/u/bicmos/ankleand/bca2d01/spice/lib/lib001.spi'
 * bca2d01 circuit library
 * andrew karanicolas
 * mit microsystems technology laboratory
 * 7-10-90

 .subckt opamp_c005 1 2 3 4 100 101 24 31
106
* two stage, fully differential bicmos operational amplifier
* with dynamic common mode feedback.
* andrew karanicolas
* mit microsystems technology laboratory
* 7-12-90

* core file used for a/d system level simulation

* this file has the new op-amp circuit, bcoa04, that is to be used
* in a pipelined a/d converter.

*.include '/u/bicmos/ankleand/bca2d01/spice/opamp/p006.spi'
* estimated parasitic capacitances for bicmos op-amp
* andrew karanicolas
* mit microsystems technology laboratory
* 7-5-90

* differential mode differential pair
  cpar1 18 0 1.5p
  cpar2 5 0 .4p
  cpar3 8 0 .4p

* emitter follower
  cpar4 6 0 .1p
  cpar5 9 0 .1p

* common emitter amplifier
  cpar6 7 0 .1p
  cpar7 10 0 .1p

* common mode differential pair
  cpar8 19 0 1.5p
  cpar9 12 0 1.5p

* common mode current mirror
  cpar10 15 0 .1p
  cpar11 14 0 .1p
  cpar12 15 0 .1p

* first stage bias network
  cpar13 20 0 1.5p
  cpar14 22 0 1.5p
cpar15 21 0 .2p
cpar16 23 0 .2p
cpar17 28 0 .2p

* second stage bias network
cpar18 25 0 1.5p
cpar19 27 0 1.5p
cpar20 26 0 .2p
cpar21 29 0 .2p
cpar22 30 0 .2p

* input-output feedback capacitance
*cpar23 1 3 .001p
*cpar24 2 4 .001p

* differential mode input stage
m1 5 1 18 18 pmos l=4u w=200u
m2 8 2 18 18 pmos l=4u w=200u

* emitter follower
q1 0 5 6 100 npn1
q4 0 8 9 100 npn1

* second stage bipolar section
q2 7 6 34 100 npn1
q3 3 11 7 100 npn1
q5 10 9 35 100 npn1
q6 4 11 10 100 npn1
re4 34 100 5
re5 35 100 5

* common mode input stage
m3 12 200 19 19 pmos l=4u w=200u
m4 100 37 19 19 pmos l=4u w=200u
vcm 37 0 0

* common mode current mirror
q7 5 12 15 100 npn1
q8 8 12 14 100 npn1
q9 12 12 13 100 npn1
re1 15 100 250
re2 14 100 250
re3 13 100 250
* dynamic common mode feedback network
ecm1 200 1000 3 0 .5
eem2 1000 0 4 0 .5

* input stage bias network reference
m5 24 24 22 22 pmos l=5u w=25u
m6 22 22 101 101 pmos l=5u w=150u
m7 100 24 20 20 pmos l=5u w=150u
m8 20 22 101 101 pmos l=5u w=150u

* second stage bias network reference
m13 31 31 27 27 pmos l=5u w=25u
m14 27 27 101 101 pmos l=5u w=150u
m15 100 31 25 25 pmos l=5u w=150u
m16 25 27 101 101 pmos l=5u w=150u

* second stage active load
m19 3 25 29 29 pmos l=5u w=750u
m20 29 27 101 101 pmos l=5u w=750u
m23 4 25 26 26 pmos l=5u w=750u
m24 26 27 101 101 pmos l=5u w=750u

* differential mode tail current source
m9 18 20 23 23 pmos l=5u w=300u
m10 23 22 101 101 pmos l=5u w=300u

* emitter follower bias
m21 16 20 28 28 pmos l=5u w=200u
m22 28 22 101 101 pmos l=5u w=200u
q10 6 16 100 100 npn
q11 9 16 100 100 npn
q12 16 16 100 100 npn

* second stage cascode bias
q13 11 11 17 100 npn
q14 17 17 36 100 npn
re6 36 100 120
m17 11 25 30 30 pmos l=5u w=300u
m18 30 27 101 101 pmos l=5u w=300u

* common mode tail current source
m11 19 20 21 21 pmos l=5u w=300u
m12 21 22 101 101 pmos l=5u w=300u

* compensation network
ccl 5 32 1.5p
ccl 32 3 15
ccl 8 33 1.5p
ccl 33 4 15
.ends

.subckt opamp_d005 1 2 3 4 100 101 24 31
.include '/u/bicmos/ankanleand/bca2d01/spice/opamp/d005.spi'
* two stage, fully differential bicmos operational amplifier
* with dynamic common mode feedback.
*
* includes mismatches:
* 0.1% resistor, capacitor
* 1.0% mos channel length.
*
* andrew karanicolas
* mit microsystems technology laboratory
* 7-12-90
*
* core file used for a/d system level simulation

* this file has the new op-amp circuit, .coa04, that is to be used
* in a pipelined a/d converter.

*.include '/u/bicmos/ankanleand/bca2d01/spice/opamp/p005.spi'
* estimated parasitic capacitances for bicmos op-amp
* andrew karanicolas
* mit microsystems technology laboratory
* 7-5-90

* differential mode differential pair
cpar1 18 0 1.5p
cpar2 5 0 .4p
cpar3 8 0 .4p

* emitter follower
cpar4 6 0 .1p
cpar5 9 0 .1p

* common emitter amplifier
cpar6 7 0 .1p
cpar7 10 0 .1p

* common mode differential pair
 cpar8 19 0 1.5p
 cpar9 12 0 1.5p

* common mode current mirror
 cpar10 13 0 .1p
 cpar11 14 0 .1p
 cpar12 15 0 .1p

* first stage bias network
 cpar13 20 0 1.5p
 cpar14 22 0 1.5p
 cpar15 21 0 .2p
 cpar16 23 0 .2p
 cpar17 28 0 .2p

* second stage bias network
 cpar18 25 0 1.5p
 cpar19 27 0 1.5p
 cpar20 26 0 .2p
 cpar21 29 0 .2p
 cpar22 30 0 .2p

* input-output feedback capacitance
* cpar23 1 3 .001p
* cpar24 2 4 .001p

* differential mode input stage
 m1 5 1 18 18 pmos l=3.96u w=200u
 m2 8 2 18 18 pmos l=4u w=200u

* emitter follower
 q1 0 5 6 100 npn1
 q4 0 8 9 100 npn1

* second stage bipolar section
 q2 7 6 34 100 npn1
 q3 3 11 7 100 npn1
 q5 10 9 35 100 npn1
 q6 4 11 10 100 npn1
re4 34 100 4.995
re5 35 100 5

* common mode input stage
m3 12 200 19 19 pmos l=3.96u w=200u
m4 100 37 19 19 pmos l=4u w=200u
vcm 37 0 0

* common mode current mirror
q7 5 12 15 100 npn1
q8 8 12 14 100 npn1
q9 12 12 13 100 npn1
re1 15 100 250
re2 14 100 250
re3 13 100 249.75

* dynamic common mode feedback network
ecm1 200 1000 3 0 .4995
ecm2 1000 0 4 0 .5

* input stage bias network reference
m5 24 24 22 22 pmos l=5u w=25u
m6 22 22 101 101 pmos l=5u w=150u
m7 100 24 20 20 pmos l=5u w=150u
m8 20 22 101 101 pmos l=5u w=150u

* second stage bias network reference
m13 31 31 27 27 pmos l=5u w=25u
m14 27 27 101 101 pmos l=5u w=150u
m15 100 31 25 25 pmos l=5u w=150u
m16 25 27 101 101 pmos l=5u w=150u

* second stage active load
m19 3 25 29 29 pmos l=5u w=750u
m20 29 27 101 101 pmos l=5u w=750u
m23 4 25 26 26 pmos l=4.95u w=750u
m24 26 27 101 101 pmos l=4.95u w=750u

* differential mode tail current source
m9 18 20 23 23 pmos l=5u w=300u
m10 23 22 101 101 pmos l=5u w=300u

* emitter follower bias
m21 16 20 28 28 pmos l=5u w=200u
m22 28 22 101 101 pmos l=5u w=200u
q10 6 16 100 100 npn1
q11 9 16 100 100 npn1
q12 16 16 100 100 npn1

* second stage cascode bias
q13 11 11 17 100 npn1
q14 17 17 36 100 npn1
re6 36 100 120
m17 11 25 30 30 pmos l=5u w=300u
m18 30 27 101 101 pmos l=5u w=300u

* common mode tail current source
m11 19 20 21 21 pmos l=4.95u w=300u
m12 21 22 101 101 pmos l=4.95u w=300u

* compensation network
c1 5 32 1.5p
rc1 32 3 15
c2 8 33 1.5p
rc2 33 4 15
.ends

.subckt opamp_cf005 1 2 3 4 100 101 24 31 204 205 206 207
.include './bicmos/ankleand/bca2d01/spice/opamp/cf005.spi'
* trio stage, fully differential bicmos operational amplifier
* with dynamic common mode feedback.
* andrew karanicolas
* mit microsystems technology laboratory
* 7-12-90
*
* core file used for a/d system level simulation

* this file has the new op-amp circuit, bcoa04, that is to be used
* in a pipelined a/d converter.

*.include './bicmos/ankleand/bca2d01/spice/opamp/p005.spi'
* estimated parasitic capacitances for bicmos op-amp
* andrew karanicolas
* mit microsystems technology laboratory
* 7-5-90

* differential mode differential pair
cpar1 18 0 1.5p
cpar2 5 0 .4p
cpar3 8 0 .4p

* emitter follower
  cpar4 6 0 .1p
cpar5 9 0 .1p

* common emitter amplifier
  cpar6 7 0 .1p
cpar7 10 0 .1p

* common mode differential pair
  cpar8 19 0 1.5p
cpar9 12 0 1.5p

* common mode current mirror
  cpar10 13 0 .1p
cpar11 14 0 .1p
cpar12 15 0 .1p

* first stage bias network
  cpar13 20 0 1.5p
cpar14 22 0 1.5p
cpar15 21 0 .2p
cpar16 23 0 .2p
cpar17 28 0 .2p

* second stage bias network
  cpar18 25 0 1.5p
cpar19 27 0 1.5p
cpar20 26 0 .2p
cpar21 29 0 .2p
cpar22 30 0 .2p

* input-output feedback capacitance
  *cpar23 1 3 .001p
  *cpar24 2 4 .001p

* differential mode input stage
  m1 5 1 18 18 pmos l=4u w=200u
  m2 8 2 18 18 pmcs l=4u w=200u
* emitter follower
q1 0 5 6 100 npn1
q4 0 8 9 100 npn1

* second stage bipolar section
q2 7 6 34 100 npn1
q3 3 11 7 100 npn1
q5 10 9 35 100 npn1
q6 4 11 10 100 npn1
re4 34 100 5
re5 35 100 5

* common mode input stage
m3 12 200 19 19 pmos l=4u w=200u
m4 100 37 19 19 pmos l=4u w=200u
vcm 37 0 0

* common mode current mirror
q7 5 12 15 100 npn1
q8 8 12 14 100 npn1
q9 12 12 13 100 npn1
re1 15 100 250
re2 14 100 250
re3 13 100 250

* dynamic common mode feedback network
ccm1 3 200 1p
ccm2 4 200 1p
m25 4 204 201 100 nmos l=3u w=10u
m26 4 205 201 101 pmos l=3u w=10u
m27 200 204 202 100 nmos l=3u w=10u
m28 200 205 202 101 pmos l=3u w=10u
m29 3 204 203 100 nmos l=3u w=10u
m30 3 205 203 101 pmos l=3u w=10u
ccm3 203 202 1p
ccm4 201 202 1p
m31 201 206 0 100 nmos l=3u w=10u
m32 201 207 0 101 pmos l=3u w=10u
m33 202 206 0 100 nmos l=3u w=10u
m34 202 207 0 101 pmos l=3u w=10u
m35 203 206 0 100 nmos l=3u w=10u
m36 203 207 0 101 pmos l=3u w=10u
* input stage bias network reference
m5 24 24 22 22 pmos l=5u w=25u
m6 22 22 101 101 pmos l=5u w=150u
m7 100 24 20 20 pmos l=5u w=150u
m8 20 22 101 101 pmos l=5u w=150u

* second stage bias network reference
m13 31 31 27 27 pmos l=5u w=25u
m14 27 27 101 101 pmos l=5u w=150u
m15 100 31 25 25 pmos l=5u w=150u
m16 25 27 101 101 pmos l=5u w=150u

* second stage active load
m19 3 25 29 29 pmos l=5u w=750u
m20 29 27 101 101 pmos l=5u w=750u
m23 4 25 26 26 pmos l=5u w=750u
m24 26 27 101 101 pmos l=5u w=750u

* differential mode tail current source
m9 18 20 23 23 pmos l=5u w=300u
m10 23 22 101 101 pmos l=5u w=300u

* emitter follower bias
m21 16 20 28 28 pmos l=5u w=200u
m22 28 22 101 101 pmos l=5u w=200u
q10 6 16 100 100 npn1
q11 9 16 100 100 npn1
q12 16 16 100 100 npn1

* second stage cascode bias
q13 11 11 17 100 npn1
q14 17 17 36 100 npn1
re6 36 100 120
m17 11 25 30 30 pmos l=5u w=300u
m18 30 27 101 101 pmos l=5u w=300u

* common mode tail current source
m11 19 20 21 21 pmos l=5u w=300u
m12 21 22 101 101 pmos l=5u w=300u

* compensation network
cc1 5 32 1.5p
rc1 32 3 15
cc2 8 33 1.5p
rc2 33 4 15
.ends

.subckt opamp_df005 1 2 3 4 100 101 24 31 204 205 206 207
.include '/u/bicmos/ankleand/bca2d01/spice/opamp/df005.spi'
* two stage, fully differential bicmos operational amplifier
* with dynamic common mode feedback.
*
* includes mismatches:
* 0.1\% resistor, capacitor
* 1.0\% mos channel length.
*
* andrew karanicolas
* mit microsystems technology laboratory
* 7-12-90
*
* core file used for a/d system level simulation
*
* this file has the new op-amp circuit, bcoa04, that is to be used
* in a pipelined a/d converter.

.include '/u/bicmos/ankleand/bca2d01/spice/opamp/p005.spi'
* estimated parasitic capacitances for bicmos op-amp
* andrew karanicolas
* mit microsystems technology laboratory
* 7-5-90
*
* differential mode differential pair
cpar1 18 0 1.5p
cpar2 5 0 .4p
cpar3 8 0 .4p
*
* emitter follower
cpar4 6 0 .1p
cpar5 9 0 .1p
*
* common emitter amplifier
cpar6 7 0 .1p
cpar7 10 0 .1p
*
* common mode differential pair
cpar8 19 0 1.5p
cpar9 12 0 1.5p

* common mode current mirror
cpar10 13 0 .1p
cpar11 14 0 .1p
cpar12 15 0 .1p

* first stage bias network
cpar13 20 0 1.5p
cpar14 22 0 1.5p
cpar15 21 0 .2p
cpar16 23 0 .2p
cpar17 28 0 .2p

* second stage bias network
cpar18 25 0 1.5p
cpar19 27 0 1.5p
cpar20 26 0 .2p
cpar21 29 0 .2p
cpar22 30 0 .2p

* input-output feedback capacitance
*cpar23 1 3 .001p
*cpar24 2 4 .001p

* differential mode input stage
m1 5 1 18 18 pmos l=3.96u w=200u
m2 8 2 18 18 pmos l=4u w=200u

* emitter follower
q1 0 5 6 100 npn1
q4 0 8 9 100 npn1

* second stage bipolar section
q2 7 6 34 100 npn1
q3 3 11 7 100 npn1
q5 10 9 35 100 npn1
q6 4 11 10 100 npn1
re4 34 100 4.995
re5 35 100 5

* common mode input stage
m3 12 200 19 19 pmos l=3.96u w=200u
m4 100 37 19 19 pmos l=4u w=200u
vcm 37 0 0

* common mode current mirror
q7 5 12 15 100 npn1
q8 8 12 14 100 npn1
q9 12 12 13 100 npn1
re1 15 100 250
re2 14 100 250
re3 13 100 249.75

* dynamic common mode feedback network
ccm1 3 200 .999p
ccm2 4 200 1p
m25 4 204 201 100 nmos l=2.97u w=10u
m26 4 205 201 101 pmos l=2.97u w=10u
m27 200 204 202 100 nmos l=3u w=10u
m28 200 205 202 101 pmos l=3u w=10u
m29 3 204 203 100 nmos l=3u w=10u
m30 3 205 203 101 pmos l=3u w=10u
ccm3 203 202 .999p
ccm4 201 202 1p
m31 201 206 0 100 nmos l=2.97u w=10u
m32 201 207 0 101 pmos l=2.97u w=10u
m33 202 206 0 100 nmos l=3u w=10u
m34 202 207 0 101 pmos l=3u w=10u
m35 203 206 0 100 nmos l=2.97u w=10u
m36 203 207 0 101 pmos l=2.97u w=10u

* input stage bias network reference
m5 24 24 22 22 pmos l=5u w=25u
m6 22 22 101 101 pmos l=5u w=150u
m7 100 24 20 20 pmos l=5u w=150u
m8 20 22 101 101 pmos l=5u w=150u

* second stage bias network reference
m13 31 31 27 27 pmos l=5u w=25u
m14 27 27 101 101 pmos l=5u w=150u
m15 100 31 25 25 pmos l=5u w=150u
m16 25 27 101 101 pmos l=5u w=150u

* second stage active load
m19 3 25 29 29 pmos l=5u w=750u
m20 29 27 101 101 pmos l=5u w=750u
m23 4 25 26 26 pmos l=4.95u w=750u
m24 26 27 101 101 pmos l=4.95u w=750u

* differential mode tail current source
m9 18 20 23 23 pmos l=5u w=300u
m10 23 22 101 101 pmos l=5u w=300u

* emitter follower bias
m21 16 20 28 28 pmos l=5u w=200u
m22 28 22 101 101 pmos l=5u w=200u
q10 6 16 100 100 npn1
q11 9 16 100 100 npn1
q12 16 16 100 100 npn1

* second stage cascode bias
q13 11 11 17 100 npn1
q14 17 17 36 100 npn1
re6 36 100 120
m17 11 25 30 30 pmos l=5u w=300u
m18 30 27 101 101 pmos l=5u w=300u

* common mode tail current source
m11 19 20 21 21 pmos l=4.95u w=300u
m12 21 22 101 101 pmos l=4.95u w=300u

* compensation network
c1 5 32 1.5p
c1 32 3 15
c2 8 33 1.5p
c2 33 4 15
.ends

.subckt preamp_c015 1 2 3 4 100 101 18 23
.include '/u/bicmos/ankleand/bca2d01/spice/preamp/c015.spi'
* fully differential bicmos comparator pre-amplifier.
* andrew karanicolas
* mit microsystems technology laboratory
* 7-6-90
*
* core file used for a/d system level simulation

* this file has the new comparator circuit, bccm01, that is to be used
* in a pipelined a/d converter.
*include '/u/bicmos/ankleand/bca2d01/spice/preampl/p015.spi'
* estimated parasitic capacitances for bicmos comparator pre-amplifier
* andrew karanicolas
* mit microsystems technology laboratory
* 7-8-90

* differential mode differential pair
cpar1 14 0 1.5p
cpar2 5 0 .2p
cpar3 6 0 .2p
cpar4 19 0 .1p
cpar5 20 0 .1p

* bipolar differential amplifier
cpar6 11 0 .2p
cpar7 7 0 .2p
cpar8 8 0 .2p
cpar9 9 0 .2p
cpar10 10 0 .2p

* amplifier bias network
cpar11 16 0 1p
cpar12 17 0 1p
cpar13 18 0 1p
cpar14 15 0 .2p
cpar15 27 0 .2p
cpar16 28 0 .2p
cpar17 29 0 .2p
cpar18 24 0 .2p
cpar19 25 0 .2p
cpar20 26 0 .2p

* output buffer network
cpar21 3 0 .2p
cpar22 4 0 .2p

* input-output feedback capacitance
*cpar23 1 3 .001p
*cpar24 2 4 .001p

* input pmos differential pair
m1 5 1 14 14 pmos l=3u w=400u
m2 6 2 14 14 pmos l=3u w=400u

* bipolar differential pair
q1 5 5 19 100 npn1
q2 7 5 11 100 npn1
q3 8 6 11 100 npn1
q4 6 6 20 100 npn1
re1 19 100 750
re2 11 100 750
re3 20 100 750

* bipolar cascode
q5 9 13 7 100 npn1
q6 10 13 8 100 npn1
rl1 12 9 2.5k
rl2 12 10 2.5k
rl3 101 12 500

* output buffer
q7 101 9 3 100 npn1
q8 101 10 4 100 npn1

* output load
c11 9 0 1.2p
c12 10 0 1.2p
c13 3 0 2p
c14 4 0 2p

* bias network
m3 14 16 15 15 pmos l=5u w=300u
m4 15 17 101 101 pmos l=5u w=300u
m5 0 18 16 16 pmos l=5u w=300u
m6 16 17 101 101 pmos l=5u w=300u
m7 18 18 17 17 pmos l=5u w=50u
m8 17 17 101 101 pmos l=5u w=300u
m9 5 16 27 27 pmos l=5u w=50u
m10 27 17 101 101 pmos l=5u w=50u
m11 6 16 28 28 pmos l=5u w=50u
m12 28 17 101 101 pmos l=5u w=50u
m13 13 16 29 29 pmos l=5u w=50u
m14 29 17 101 101 pmos l=5u w=50u
q9 \ 13 13 21 100 npn1
q10 21 21 22 100 npn1
q11 22 22 30 100 npn1
q12 30 30 100 100 npn1
q13 23 23 24 100 npn1
q14 3 23 25 100 npn1
q15 4 23 26 100 npn1
re4 24 100 100
re5 25 100 100
re6 26 100 100
.ends

*.subckt preamp_d015 1 2 3 4 100 101 18 23
*.include '/u/bicmos/ankleand/bca2d01/spice/preamp/d015.spi'
*.ends

.subckt latch_c004 1 2 3 4 100 101 10 11 12 13
.include '/u/bicmos/ankleand/bca2d01/spice/latch/c004.spi'
* cmos latch.
* andrew karanicolas
* mit microsystems technology laboratory
* 8-6-90

* this file describes the cmos latch to be used in comparator bccm01
* in the pipelined a/d converter.

*.include '/u/bicmos/ankleand/bca2d01/spice/latch/p004.spi'
* estimated parasitic capacitances for cmos latch
* andrew karanicolas
* mit microsystems technology laboratory
* 7-8-90

* regenerative latch
cpar1 3 0 .5p
cpar2 4 0 .5p
cpar3 5 0 .2p

* clock drivers
cpar4 11 0 .1p
cpar5 13 0 .1p

* differential input pair
cpar6 6 0 .2p

* bias network
cpar7 8 0 .2p
cpar8 9 0 .2p

* input pmos differential pair
m1 3 1 6 6 pmos l=3u w=10u
m2 4 2 6 6 pmos l=3u w=10u

* regenerative latch
m3 3 4 5 101 pmos1 l=3u w=10u
m4 3 4 100 100 nmos1 l=3u w=5u
m5 4 3 5 101 pmos1 l=3u w=10u
m6 4 3 100 100 nmos1 l=3u w=5u
m7 5 11 101 101 pmos1 l=3u w=20u
m8 3 13 4 101 pmos1 l=3u w=10u
m9 3 12 4 100 nmos1 l=3u w=5u

* bias circuit
m10 6 9 7 7 pmos l=3u w=60u
m11 7 8 101 101 pmos l=3u w=60u
m12 0 10 9 9 pmos l=3u w=60u
m13 9 8 101 101 pmos l=3u w=60u
m14 10 10 8 8 pmos l=3u w=10u
m15 8 8 101 101 pmos l=3u w=60u
.ends

*.subckt latch_d004 1 2 3 4 100 101 10 11 12 13
*.include '/u/bicmos/ankleand/bca2d01/spice/latch/d004.spi'
*.ends

.subckt trgl 1 2 3 4 100 101
.include '/u/bicmos/ankleand/bca2d01/spice/digital/trg001.spi'
* mos transmission gate.
* andrew karanicolas
* mit microsystems technology laboratory
* 7-16-90
*
* minimum geometry for analog switches: wn=5u, wp=5u, ln=2u, lp=2u

m1 1 3 2 100 nmos l=ln w=wn ad=60p as=60p pd=52u ps=52u
m2 1 4 2 101 pmos l=lp w=wp ad=120p as=60p pd=104u ps=52u
.ends

.subckt invl 1 2 3 4
.include '/u/bicmos/ankleand/bca2d01/spice/digital/inv001.spi'
* cmos inverter
* andrew karanicolas
* mit microsystems technology laboratory
* 7-24-90
*
* minimum geometry for inverter: wn=5u, wp=5u, ln=2u, lp=2u

m1 2 1 4 4 pmos l=lp w=wp ad=120p as=60p pd=104u ps=52u
m2 2 1 3 3 nmos l=ln w=wn ad=60p as=60p pd=52u ps=52u
.ends

.subckt comp_c001 1 2 3 4 100 101 80 81 82 83 41 42 43 44
.include '/u/bicmos/ankleand/bca2d01/spice/comp/c001.spi'
* open loop offset cancelled comparator pre-amplifier
* * andrew karanicolas
* * mit microsystems technology laboratory
* 8-3-90
*
* pre-amplifier 1
x1 5 6 7 8 100 101 80 81 preamp_c015

* switched-capacitor network 1
xsp1 1 5 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp2 5 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp3 9 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
cp1 7 9 2p

xsp9 2 6 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp10 6 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp11 10 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
cp2 8 10 2p

* pre-amplifier 2
x2 11 12 13 14 100 101 82 83 preamp_c015

* switched-capacitor network 2
xsp4 9 11 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp5 11 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp6 15 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
cp3 13 15 2p

xsp12 10 12 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp13 12 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp14 16 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
cp4 14 16 2p

* output switched capacitor network
xsp7 15 3 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp8 3 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u

xsp15 16 4 41 42 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsp16 4 0 43 44 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
.ends

*.subckt comp_d001 1 2 3 4 100 101 80 81 82 83 41 42 43 44
*.include '/u/bicmos/ankleand/bca2d01/spice/comp/d001.spi'
*.ends

.subckt mult2_cr001 1 2 13 14 3 4 100 101 24 31 41 42 43 44 45 46 47 48 49 50
.include '/u/bicmos/ankleand/bca2d01/spice/mult2/cr001.spi'
* reference non-restoring bicmos multiply-by-two circuit.
* uses modified multiply-by-two switch arrangement.
* includes reference switch network.
* andrew karanicolas
* mit microsystems technology laboratory
* 8-6-90

* operational amplifier
x1 11 12 4 3 100 101 24 31 opamp_c005

* switched capacitor network
xsm1 1 7 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsm2 1 8 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsm3 5 8 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm4 7 3 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm5 11 3 41 42 100 101 trg1 wn=10u wp=10u ln=3u lp=3u
cm1 7 11 1p
cm2 8 11 1p

xsm6 2 10 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsm7 2 9 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsm8 6 9 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm9 10 4 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm10 12 4 41 42 100 101 trg1 wn=10u wp=10u ln=3u lp=3u
cm3 9 12 1p
cm4 10 12 lp

xsm11 13 5 47 48 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm12 14 6 47 48 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm13 14 5 49 50 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsm14 13 6 49 50 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
.ends

*.subckt mult2_dr001 1 2 13 14 3 4 100 101 24 31 41 42 43 44 45 46 47 48 49 50
*.include '/u/bicmos/ankleand/bca2d01/spice/mult2/dr001.spi'
*.ends

*.subckt mult2_cfr001 1 2 13 14 3 4 100 101 24 31 204 205 206 207
** 41 42 43 44 45 46 47 48 49 50
*.include '/u/bicmos/ankleand/bca2d01/spice/mult2/cfr001.spi'
*.ends

*.subckt mult2_dfr001 1 2 13 14 3 4 100 101 24 31 204 205 206 207
** 41 42 43 44 45 46 47 48 49 50
*.include '/u/bicmcs/ankleand/bca2d01/spice/mult2/dfr001.spi'
*.ends

.subckt sah_c001 1 2 3 4 100 101 24 31 41 42 43 44 45 46
.include '/u/bicmos/ankleand/bca2d01/spice/sah/c001.spi'
* bicmos sample-and-hold
* andrew karanicolas
* mit microsystems technology laboratory
* 8-10-90

* operational amplifier
x1 7 8 4 3 100 101 24 31 opamp_c005

* switched capacitor network
xsh1 1 5 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsh2 5 3 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsh3 7 3 41 42 100 101 trg1 wn=10u wp=10u ln=3u lp=3u
csh1 5 7 1p

xsh4 2 6 43 44 100 101 trg1 wn=8u wp=20u ln=3u lp=3u
xsh5 4 6 45 46 100 101 trg1 wn=5u wp=10u ln=3u lp=3u
xsh6 8 4 41 42 100 101 trg1 wn=10u wp=10u ln=3u lp=3u
csh2 6 8 1p
.ends

127
* subckt sah_d001 1 2 3 4 100 101 24 31 41 42 43 44 45 46
  * include '/u/bicmos/ankleand/bca2d01/spice/sah/d001.spi'
  * ends

* subckt sah_cf001 1 2 3 4 100 101 24 31 204 205 206 207 41 42 43 44 45 46
  * include '/u/bicmos/ankleand/bca2d01/spice/sah/cf001.spi'
  * ends

* subckt sah_df001 1 2 3 4 100 101 24 31 204 205 206 207 41 42 43 44 45 46
  * include '/u/bicmos/ankleand/bca2d01/spice/sah/df001.spi'
  * ends

.subckt bit_cr001 1 2 13 14 3 4 19 20 100 101 102 103 24 31
+ 80 81 82 83 84 501 502 503 504 505 506 507
.include '/u/bicmos/ankleand/bca2d01/spice/bit/cr001.spi'
* multiply-by-two:
  * reference non-restoring bicmos multiply-by-two circuit.
  * uses modified multiply-by-two switch arrangement.
  * includes reference switch network.
* comparator preamplifier system:
  * two stage comparator with open loop offset cancellation.
* latch:
  * cmos latch with differential input.
  *
* andrew karanicolas
* mit microsystems technology laboratory
* 8-7-90

* multiply-by-two
x1 1 2 13 14 3 4 100 101 24 31 41 42 43 44 45 46 47 48 49 50 mult2_cr001

* comparator preamplifier system
x2 3 4 17 18 100 101 80 81 82 83 45 46 41 42 comp_c001

* latch
x3 17 18 19 20 102 103 84 51 52 53 latch_c004

* clock drivers
* multiply-by-two
xinv1 501 42 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv2 42 41 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv3 502 44 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv4 44 43 102 103 inv1 wn=10u wp=20u ln=3u lp=3u

128
xinv5  503  46  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv6  46  45  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u

* clock drivers
* reference voltage switch network
xinv7  504  48  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv8  48  47  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv9  505  50  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv10  50  49  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u

* clock drivers
* latch
xinv11  506  600  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv12  600  51  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv13  507  53  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
xinv14  53  52  102  103  inv1  wn=10u  wp=20u  ln=3u  lp=3u
.ends

.subckt  bit0_c001  1  2  3  4  19  20  100  101  102  103  24  31
+  80  81  82  83  84  501  502  503  506  507
.include  /u/bicmos/ankleand/bca2d01/spice/bit0/c001.spi'
* sample-and-hold:
*     architecture similar to reference non-restoring
*     multiply-by-two circuit.
* comparator preamplifier system:
*     two stage comparator with open loop offset cancellation.
* latch:
*     cmos latch with differential input.
*
* andrew karanicolas
* mit microsystems technology laboratory
* 8-10-90

* sample-and-hold
x1  1  2  3  4  100  101  24  31  41  42  43  44  45  46  sah_c001

* comparator preamplifier system
x2  3  4  17  18  100  101  80  81  82  83  45  46  41  42  comp_c001

* latch
x3  17  18  19  20  102  103  84  51  52  53  latch_c004

* clock drivers
* sample-and-hold
xinv1 501 42 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv2 42 41 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv3 502 44 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv4 44 43 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv5 503 46 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv6 46 45 102 103 inv1 wn=10u wp=20u ln=3u lp=3u

* clock drivers
* latch
xinv7 506 600 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv8 600 51 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv9 507 53 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv10 53 52 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
.ends
.include '/u/bicmos/ankleand/bca2d01/spice/sources/ck008.spi'
* clock sources for pipelined bicmos a/d converter, no cmfb clocks
* andrew karanicolas
* mit microsystems technology laboratory
* 8-6-90
*
* multiply-by-two clock waveforms
* period = 160ns
* guard = 5ns
* tr = 10ns
* tf = 10ns

* multiply-by-two and comparator preamplifier system clocks
vphi11 501 0 pulse(5 -5 0 10n 10n 100n 190n)
vphi12 502 0 pulse(5 -5 5n 10n 10n 100n 190n)
vphi13 503 0 pulse(-5 5 20n 10n 10n 65n 190n)
vphi21 1501 0 pulse(-5 5 0 10n 10n 70n 190n)
vphi22 1502 0 pulse(-5 5 5n 10n 10n 70n 190n)
vphi23 1503 0 pulse(-5 5 100n 10n 10n 65n 190n)

* latch clocks
vphi14 506 0 pulse(-5 5 0 10n 10n 80n 190n)
vphi15 507 0 pulse(-5 5 5n 10n 10n 80n 190n)

vphi24 1506 0 pulse(-5 5 80n 10n 10n 80n 190n)

vphi25 1507 0 pulse(-5 5 85n 10n 10n 80n 190n)

* pipeline stage 0
x1 1 2 3 4 19 20 100 101 102 103 24 31 80 81 82 83 84 + 501 502 503 506 507 bit0_c001

xinv1 19 300 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv2 300 1505 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv3 20 301 102 103 inv1 wn=10u wp=20u ln=3u lp=3u
xinv4 301 1504 102 103 inv1 wn=10u wp=20u ln=3u lp=3u

* pipeline stage 2
x2 3 4 13 14 5 6 1019 1020 100 101 102 103 1024 1031 1080 1081 1082 1083 1084 + 1501 1502 1503 1504 1505 1506 1507 bit_cr001

* input network
vin1 1 0 2.5
ein2 2 0 1 0 -1
vrl 13 0 2.5
er2 14 0 13 0 -1

* output load
cli 5 15 3p
cli2 6 16 3p
rl1 15 0 50
rl2 16 0 50

* power supply
vdd 101 0 5
vss 100 0 -5
vkp 103 0 5
vkn 102 0 -5
ibias01 24 0 .35m
ibias02 31 0 .40m
ibias03 80 0 .85m
ibias04 0 81 .25m
ibias05 82 0 .85m
ibias06 0 83 .25m
ibias07 84 0 .10m
.options nomod ingold=2 numdgt=7 acout=0 itli=1000 dv=5 method=gear lvtim=2
+ absv=1e-12 relv=5e-3 absi=1e-14 reli=5e-6 trtol=10 chgtol=1e-18
+ imax=16 acct

.nodeset
+ 37:5 =-3.307283e+00 37:6 =-4.122131e+00 37:7 =-4.119508e+00
+ 37:8 =-3.307283e+00 37:9 =-4.122131e+00 37:10 =-4.119508e+00
+ 37:11 =-3.265138e+00 37:12 =-4.107775e+00 37:13 =-4.914850e+00
+ 37:14 =-4.914495e+00 37:15 =-4.914495e+00 37:16 =-4.185278e+00
+ 37:17 =-4.084528e+00 37:18 = 1.191400e+00 37:19 = 1.189721e+00
+ 37:20 = 2.325243e+00 37:21 = 3.771810e+00 37:22 = 3.524709e+00
+ 37:23 = 3.771836e+00 37:25 = 2.191729e+00 37:26 = 3.675570e+00
+ 37:27 = 3.470094e+00 37:28 = 3.712398e+00 37:29 = 3.675570e+00
+ 37:30 = 3.638556e+00 37:32 =-2.437570e-02 37:33 =-2.437570e-02
+ 37:34 =-4.989751e+00 37:35 =-4.989751e+00 37:36 =-4.913919e+00
+ 37:37 = 0. 37:200 =-2.437570e-02 37:1000 =-1.218785e-02
+ 62:5 =-3.307283e+00 62:6 =-4.122131e+00 62:7 =-4.119508e+00
+ 62:8 =-3.307283e+00 62:9 =-4.122131e+00 62:10 =-4.119508e+00
+ 62:11 =-3.255138e+00 62:12 =-4.107775e+00 62:13 =-4.914850e+00
+ 62:14 =-4.914495e+00 62:15 =-4.914495e+00 62:16 =-4.185278e+00
+ 62:17 =-4.084528e+00 62:18 = 1.191400e+00 62:19 = 1.189721e+00
+ 62:20 = 2.325243e+00 62:21 = 3.771810e+00 62:22 = 3.524709e+00
+ 62:23 = 3.771836e+00 62:25 = 2.191729e+00 62:26 = 3.675570e+00
+ 62:27 = 3.470094e+00 62:28 = 3.712398e+00 62:29 = 3.675570e+00
+ 62:34 =-4.989751e+00 62:35 =-4.989751e+00 62:36 =-4.913919e+00
+ 62:37 = 0. 62:200 =-2.437570e-02 62:1000 =-1.218785e-02

.tran 1n 380n
.print tran v(3,4) v(19,20) v(5,6) v(1019,1020)

.width out=80
.end
Bibliography


