A DIGITALLY INTERPOLATING FREQUENCY SYNTHESIZER

by

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ABSTRACT

Feedback systems have often been used for frequency synthesizers. Within this framework, speed of response to input changes and resolution have been mutually exclusive goals. An interpolative technique is proposed to achieve higher resolution without loss of speed of response. The effects of this interpolative technique on spectral purity are derived analytically. A breadboard feasibility study was built, based on a 1 Hz to 1 MHz output range with 1 Hz resolution, 10 ms settling time and greater than 50 dB spectral purity. The feasibility study shows that the effectiveness of this technique is limited only by circuit complexity rather than theoretical considerations.
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PART ONE
THEORETICAL CONSIDERATIONS
Chapter One

INTRODUCTION

My goal is to probe into the theoretical and experimental limitations of a relatively unconventional technique of frequency synthesis. By using a mixture of both feedback and open-loop control to determine the overall characteristics of the output oscillator, I hope to overcome a number of the limitations that normally tend to decrease the usefulness of a variable-frequency generator.

For the sake of specificity, I have attached the acronym Digitally Interpolating Frequency Synthesizer, to this method of frequency generation. As brief background development will give the necessary insight into why this project evolved the topology it did.

My initial object was to explore the field of frequency generation. That is, how one might formulate a method by which the frequency of an oscillator could be precisely related to some known input variable. Based on my interest in classical control theory, I decided on a feedback approach. A feedback-over-open-loop strategy has a good deal to offer. For one, feedback systems can often suppress variations due to uncertainties in some system parameters. Secondly, whereas direct (open-loop) generation techniques vary from individual system to system, feedback (control) techniques do not. They are usually categorized and discussed in terms of general system topologies. Thus, going the route of feedback makes available the great wealth of control analysis techniques.
The basic topology of a feedback frequency synthesizer is shown in Figure 1. The fundamental premise on which a synthesizer is built is that there exists a reference frequency, a standard, with characteristics which are well known and not likely to change. (For example, a temperature-compensated crystal oscillator, accurate to 1 part in $10^7$ per year, over a 0° to 50° C temperature variations.) Most likely, however, being able to produce one frequency extremely accurately is not highly useful. So, a second oscillator is constructed with far lower stability, but a much larger range of output frequency, with the hope that, through feedback, the second oscillator can be made to hold to a desired frequency within its output range, yet be forced to exhibit the stability and spectral purity of the reference. The functional dependence of $f_{\text{out}}$ to $f_{\text{ref}}$ can be obtained through standard block diagram manipulation:

$$f_{\text{out}} = \frac{a(s)}{1 + a(s) \frac{1}{N}} \cdot f_{\text{ref}}$$

Looking at the steady state situation, where $a(s) = a_0$, with the additional constraint that $a_0 \cdot \frac{1}{N} \gg 1$

$$f_{\text{out}} = N \cdot f_{\text{ref}}$$

Under the above conditions, if the attenuation factor could be maintained as pure as the reference, the battle would be won. Since the loop variables are frequency, not voltage, the attenuation cannot be
realized by a passive resistive network. In its place a digital divide-
by-N counter is used—the dual in the frequency domain to a voltage
divider.

Unfortunately, a closer inspection of the proposed solution reveals
that it is not optimum in every respect. Since the divide-by-N counter
is realized by a digital counter, \( N \) can no longer be continuous—it can
assume only integer values. Thus, resolution, or how finely the output
can be tuned, seems to be limiting the usefulness of the synthesizer.

Yet even without too much deliberation, a way out can be realized.
Since resolution is now upper-bounded by the reference frequency, why
not just reduce the reference frequency? Speciously, this seems like
a very viable solution. If 1 Hz resolution is desired, then use a 1 Hz
reference oscillator. (It is really irrelevant that low frequency
standards are not available—high frequency standards can always be
digitally divided down.) This approach removes the limit of obtaining
high resolution, but places in its stead an even more fundamental prob-
lem—speed of response. That is to say, given that \( f_{\text{out}} = N_1 \cdot f_{\text{ref}} \)
and \( N \) is instantaneously changed to some new \( N \), say \( N_2 \), (perhaps by
changing the programming of the divide-by-N counter), how long does it
take before the output frequency settles to within some fraction \( \delta \) of
its new steady state value: \( f_{\text{out}} = N_2 \cdot f_{\text{ref}} \cdot (1 - \delta) \)? The fact that
the variables of this control loop are frequency, imposes severe limits
on the speed of response of the system. Implicit to a measurement of
frequency is a time period, \( T = \frac{1}{f} \). If a frequency-dependent variable
changes, the change cannot manifest itself until one period has passed.
(Note: It is important to remember that a periodic waveform, passed through a digital gate is stripped of all information except for the location in time of threshold voltage crossings. By definition, therefore, information can be transmitted but once a cycle.) This leads one to justly believe that a frequency-locked loop is a sampled-date system. Once this association is made, the reasons for the limitation of speed of response by reference frequency become all too clear.\textsuperscript{1,2} All loop variables (except for the output), are running either at or near the reference frequency. If now the divide-by-\(N\) counter is reprogrammed to a new \(N\), the loop cannot act on (nor even know about) this information for a time equal to a period of the reference frequency. So if \(1\) Hz resolution is desired, the loop cannot possibly change synthesized frequencies and settle in less than one second. The problem is compounded even further when it is realized that these delays introduced by operation of a control loop at frequencies approaching its sampling (reference) frequency cause the system to exhibit highly underdamped, almost oscillatory system behavior. So one must further reduce the speed of the loop to obtain a margin of stability. The limiting case leads us to believe that a system with infinite resolution would take forever to reach final value!

The above reasoning seems to imply that speed of response and high resolution are mutually-exclusive goals. The entire question hinges on the integer nature of \(N\). With the system described above, it would be impossible to synthesize a frequency
\[ f_{out} = (N + \delta) \cdot f_{ref} \quad 0 \leq \delta < 1 \]

(\delta = 0 \text{ is admitted to being degenerate, corresponding to } f_{out} = N \cdot f_{ref})

N must be kept an integer, but there is nothing preventing N from being a time-varying integer. So it would seem that a much better solution would be to maintain a high reference frequency (thus assuring reasonable settling time), and interpolate those frequencies between \( f_{ref} \cdot N \) and \( f_{ref} \cdot (N + 1) \), by forcing N to behave as if it were not an integer. This solution of digitally interpolating the value of N forms the basic premise on which this thesis is structured. Theoretical calculation and breadboard feasibility study are based on a reference frequency of 10 kHz and an output frequency range from the voltage controlled oscillator of 5 MHz to 6 MHz, with 1 Hz resolution.

In order to make an analytical discussion of the digital interpolation technique meaningful, the basic control loop and its related dynamics must first be established.
Chapter Two

BASIC LOOP DYNAMICS

An issue that must be settled is the order of the loop. If
\[ a(s) = \frac{P(s)}{Q(s)} \]
where \( P(s) \) and \( Q(s) \) are polynomials in \( s \), the order of the loop is determined by the highest power term in \( Q(s) \). A common practice is to employ a phase detector as the summing junction of Figure 1. The phase detector integrates the frequency difference applied to its inputs:

\[ \phi(t) = \frac{1}{k} \int (f_r - f_f) \, dt \quad \text{or} \quad \phi(s) = \frac{(f_r - f_f)}{ks} \]

where \( k \) is the appropriate scale factor. See Figure 2, Block 1. The motivation for using a phase detector is simple. The dc gain of an integrator is infinite. If the phase detector output is to be finite, the dc input must be zero, implying that \( f_r = f_f \), and consequently the output frequency is identically equal to the desired output value, since \( f_{\text{out}} = N \cdot f_r (= f_f) \). There is no steady state frequency error.

There is equally good motivation for introducing a second pole into the loop transmission. For the first order case, the loop transmission equals

\[ G(s) = -\frac{K_{vco}}{ks} \quad \text{and} \quad \frac{f_{\text{out}}}{f_{\text{ref}}} = \frac{N}{(\frac{K_{vco}}{kN}) \cdot s + 1} \]

The step response is the familiar exponential rise which reaches steady state value only in the limit as \( t \) approaches infinity. For a second
FIGURE 2
order system with complex poles (a lax restriction, to be shown shortly), the step response will reach (overshoot) final value in a time short compared to the first order case. An equally important reason for increasing loop order is that the digital interpolation technique depends on the phase relation of \( f_{\text{ref}} \) and \( f_f \), being a known constant. By adding a second pole, specifically at the origin, the phase difference (error) is driven to zero in the same manner that the integration in the phase detector forced zero frequency error. See Figure 2, Block 2. The zero phase error is attributable to the double integration, rather than a gain constant and is hence insensitive to changes in loop parameters.

The advantages of a third or higher order system can best be measured by the use of an analytic tool known as error coefficients.\(^3\) With a minimal amount of Laplace transform manipulation it can be shown that if the error signal \( f_e(s) (= f_r - f_f(s)) \), is written as a Taylor series in ascending powers of \( s \):

\[
f_e(s) = f_{e0} + f_{e1} \cdot s + f_{e2} \cdot s^2 + \ldots + f_{en} \cdot s^n
\]

then the steady state error after the application of an input \( u_{-1}(t) \) is \( f_{en-1} \), where \( u_{-1}(t) \) is the unit step function, \( u_{-2}(t) \) is the unit ramp function, etc. It can also be shown that if, through some range of frequencies, the loop transmission is proportional to \( 1/s^n \), then the first \( n \) error coefficients (\( f_{e0} \) through \( f_{en-1} \)) behave as if they were zero, through that range of frequencies. Thus if the reference frequency were not a reference, but rather some changing frequency
which the synthesizer must constantly try to follow (for example, a satellite would receive a constant frequency transmission as an input whose frequency and rate of change of frequency were time-varying because of Doppler shift), it would be possible to insure zero frequency tracking error even with input acceleration components, by making the loop transmission proportional to $1/s^3$. But a frequency synthesizer need not suffer with the problems of tracking moving inputs. The input is a reference frequency and is fixed. Although $N$ (the setting of the digital counter) is changed, it is changed in a very specific manner--the user might change a front-panel setting to effect this change in $N$, and then very possibly not change the value of $N$ for quite some time. So at worst, $N$ will undergo a step change, but there will never be a need to follow a series of fast changing setting. Demands of a frequency synthesizer dictate therefore, that loop order complexity never need to exceed two.\textsuperscript{16}

It should be pointed out that feeding-back around a double integration usually leads to instability. Compensation, the technique of advantageous modification of loop dynamics, will be discussed once the descriptive loop block diagram has been replaced by a functional block diagram, with elements containing specified experimental gain constants and precise frequency dependence.
Chapter Three
THEORY OF DIGITAL INTERPOLATION

Within the framework of a second order system, the control loop has evolved the topology shown in Figure 2.

As stated in the introduction, the synthesizer, in its present state, lacks the capability of producing non-integer multiples of the reference frequency, i.e. it is impossible to produce an \( f_{out} \) such that:

\[
f_{out} = (N + \alpha) \cdot f_{ref} \quad 0 \leq \alpha < 1,
\]

except for the case of alpha equals zero, which is degenerate. \(^5\) Suppose, however, \( N \) were not time invariant. Suppose, in fact, that the divide-by-\( N \) counter were programmed in the following manner: Given some arbitrary time \( \delta \), the counter would first divide by \( N \) for a time of \( \delta \cdot (1 - \alpha) \) seconds, and then would divide by \( N + 1 \) for a time of \( \delta \cdot \alpha \) seconds. Under these conditions, the average \( f_{out} \), averaged over a time interval much larger than \( \delta \), would equal \( (N + \alpha) \cdot f_{ref} \), the desired output frequency. The goal, however, is that the short term average, averaged over one cycle, as well as the long term average, be correct.

As a thought experiment, assume that \( f_{out} \) were held to the desired output frequency, \( f_{out} = (N + \alpha) \cdot f_{ref} \), by somehow reaching in to the circuit. Looking at Figure 3, \( f_f \), the feedback, scaled-down
FIGURE 3

Block 3

$\phi_c(t)$

$\phi_e(t)$

$\int dt$

$f_r$

$\frac{1}{N}$ or $\frac{1}{N+1}$

$N$ set by user

$voltage\ controlled\ oscillator$

$f_{out}$

$\int dt$

$f_f$

$f_{ref}$
version of the output is

\[ f_f = \frac{N + \alpha}{N} \cdot f_{\text{ref}}, \text{ if the counter is set to divide by } N \]

\[ = \frac{N + \alpha}{N + 1} \cdot f_{\text{ref}}, \text{ if the counter is set to divide by } N + 1 \]

\( f_f \) is alternately slightly greater, and then slightly less than \( f_{\text{ref}} \). This frequency difference is integrated:

\[ \phi_e(t) = \frac{1}{k} \int (f_r - f_f) \cdot dt \]

With a careful choice of the bounds of integration, it can be shown that \( \phi_e(t) \) will then be some sort of periodic ramp of phase error. By assumption, the voltage controlled oscillator output frequency is equally to \((N + \alpha) \cdot f_{\text{ref}}\) and is not changing. If so, the output of the integrator must be constant, implying the input to the integrator must be zero. Therefore, if this synthesizer is to produce the correct frequency, a time-varying phase correction signal, \( \phi_c(t) \), must be added to \( \phi_e(t) \) so that their sum is zero, the integrator sees no error and the loop holds to the desired output frequency. See Figure 3, Block 3. This implies that \( \phi_e(t) = - \phi_c(t) \). Calculation of the phase error signal is rather complex and could best be understood in terms of the actual hardware implementation. The actual synthesizer replaces the divide-by-N counter and phase comparator by the circuitry of Figure 4, Blocks 1 through 4.
Let us take an aside for a moment to prove that if an integer multiple of the reference frequency is being produced (i.e. $\alpha = 0$), then the blocks enclosed within the dashed lines of Figure 4 do indeed function as a divide-by-$N$ counter/phase comparator combination. Assume that for the sake of argument, the desired voltage controlled oscillator output frequency is 5 MHz. The voltage controlled oscillator (Figure 4, Block 8) is fed into the VCO-accumulator (Block 1), whose output increases one count for every cycle of the voltage controlled oscillator. The N-accumulator (Figure 4, Block 3) is clocked in a somewhat different manner. Its output jumps $N$ counts once during every period of the reference frequency. With a reference period of 100 $\mu$sec (= 1/10 kHz) and a desired output of 5 MHz, the number of counts per step would be: 

$$5 \times 10^6 \text{ counts per second} \times 10^{-4} \text{ seconds per reference period} = 500 \text{ counts per reference period}.$$ 

These accumulators are fed into the comparator (Figure 4, Block 2), whose output is a logical 1 if the number of counts in the VCO-accumulator is greater than corresponding number of counts in the N-accumulator. (Note: throughout the entire discussion, both of the accumulators will be considered to be infinite in length. This assumption will be made valid in the actual circuitry by digital gating of the carry bits of the accumulators.)

Assuming the loop was locked, that the output was at the desired 5 MHz, the value of the accumulators, and the corresponding phase comparator output might look like something depicted in Figure 5a. Since the loop bandwidth, as noted in the introduction, has purposely been reduced substantially below 10 kHz, for reasons of stability, the loop
simply responds to the average value of the square wave. It is not hard to see that as the phase of the voltage controlled oscillator changes with respect to the 10 kHz reference, the average value of the square wave (the phase detector output) changes. Note that the phase error, \( \phi_e(t) \), the average value of the square wave, must be zero because of the integration that follows this phase detector output. So the new components of Figure 4 do operate as hoped.

We are now in a position to calculate \( \phi_e(t) \), under the assumption that the output frequency is somehow being held at the desired output value: 
\[
\text{f}_{\text{out}} = (N + \alpha) \cdot f_{\text{ref}}.
\]
By assumption, the VCO-accumulator increases \( 10^4 \cdot (N + \alpha) \) counts per second, and the N-accumulator increases at a rate of \( 10^4 \cdot N \) counts per second. If the \( \alpha \)-accumulator (Figure 4, Block 4) were disabled, the N- and VCO-accumulators would slip in phase at a rate of \([10^4 \cdot (N + \alpha)] - [10^4 \cdot N] = 10^4 \cdot \alpha \) cycles per second.

But the N-accumulator has really two inputs. It can increase its counts by N every 100 \( \mu \)sec, or by one, by a carry from the \( \alpha \)-accumulator. The \( \alpha \)-accumulator is a four decade counter with counting scheme identical to that of the N-accumulator, except that its counts per reference period is determined by \( \alpha \) rather than N. A quick calculation reveals that a four decade counter, counting at a rate of \( 10^4 \cdot \alpha \) counts per second, will overflow at a rate of \( 10^4 \cdot \alpha \) counts per second. Therefore, if the carry of the \( \alpha \)-accumulator is fed into the N-accumulator, the average change of phase between the N- and VCO-accumulators will be zero. This is shown pictorially in Figure 6. Since counters cannot really be off by a fraction of a count, Figure 6 actually is an indica-
phase (count) difference = (counts in VCO-accumulator) - (counts in N-accumulator)

$-1 \text{ count}$

$\alpha$-accumulator overflow

$t$

$10^4 \cdot \alpha \text{ seconds}$

$2 \cdot 10^4 \cdot \alpha \text{ seconds}$
tion by what fraction of a cycle (count) in time does the VCO-accumulator clock before the N-accumulator.

This effectively says that if the voltage controlled oscillator were held at the desired output frequency, \( \phi_e(t) \) would look precisely like Figure 6, a sawtooth ramp with frequency \( 10^4 \cdot \alpha \) Hz. If the loop is to actually hold this output frequency, then \( \phi_c(t) \) must equal \(-\phi_e(t)\), as previously stated. The problem of producing \( \phi_c(t) \) is solved once it is realized that \( \phi_e(t) \) is nothing more than a digital-to-analog-converted output of the value of the \( \alpha \)-accumulator. It becomes a matter of simply choosing the appropriate scale factor. See Figure 4, Block 9. Somehow, the phase error attributable to the ramp \( \phi_e(t) \) must be contrasted to the maximum phase error signal producible by the phase detector in order to arrive at the proper weighting factor.

This can be done in two steps. First, the total range of the phase detector is realized to be one cycle of the reference frequency.\(^6,7\) This is obvious from in inspection of Figure 5b. If the difference in the number of counts between the \( N \) and VCO-accumulators increases sufficiently, so that the value of the VCO-accumulator falls out of the shaded region bounded by the counts in the \( N \)-accumulator, then the comparator will no longer change state. One register will always be greater than the other. The phase detector output will be pinned at either a logical 1 or 0, depending on the state of the comparator. The height of the band is then the maximum number of counts by which the two accumulators can differ, and still maintain a monotonic and linear relationship between count differential and phase detector.
output. The height of the band, as indicated on the figure, is N. The calculation of the digital-to-analog converter scale factor can now be completed by realizing that, from Figure 6, the maximum phase slippage is a one count (1 cycle) difference in value between the N- and VCO-accumulators, when the loop is operating properly. Since this phase slippage is one count out of a possible N, then the full scale output of the digital-to-analog-converted value of the α-accumulator must be \( \frac{1}{N} \) times the full scale output of the phase detector. Correspondingly, the least significant digit of the α-accumulator is \( 10^{-4} \) times full scale, since the α-accumulator is a 4 decade realization.
Chapter Four

FREQUENCY-DOMAIN-RELATED CONSIDERATIONS

A frequency synthesizer cannot be deemed worthy of its name if its output is not spectrally pure. If the output of the integrator, (the input to the voltage controlled oscillator) remains constant for a given N, then the output of the voltage controlled oscillator must, be definition, remain at one frequency, and hence be spectrally pure. However, there exist two very possible sources which could cause the integrator to change value--these two sources are the phase detector output, and the digital interpolation correction signal. The digital interpolation signal will only present a major problem if not precisely set to the proper value. Unfortunately, the phase detector (and the digital interpolation circuitry, to a much smaller extent) present a problem of a different, more fundamental nature. The origin of the problem lies in the sampled nature of the loop. The phase detector output has previously been treated as a slow-varying, dc-like signal, motivated by the argument that the loop bandwidth (having purposely been reduced way below 10 kHz for reasons of stability) cannot possibly follow the 10 kHz duty-cycle modulated square wave phase detector output, and simply follows the average value. Unfortunately, this can only be true in the limit of zero loop bandwidth, a case which certainly has other, more severe problems.

It therefore seems nonzero loop bandwidth implies spectral impurity. Since there are 10 kHz signals now present in the loop, one
would imagine that with a linear system (as this is), that the output would contain sidebands at frequencies equal to:

\[ f_{\text{ref}} \cdot (N + \alpha) \pm k \cdot 10 \text{ kHz} \]

where \( k \) is any integer.\(^8\) All hope is not lost. Whereas complete spectral purity is not realizable, it can be approached within an arbitrarily small amount, limited only by the complexity of the circuit used, how far one is willing to go. The first step is to attenuate the 10 kHz component of the phase detector output with a separate low pass filter, instead of depending on the low pass nature of the loop. If the corner frequency of the filter is auspiciously situated above loop crossover, yet somewhere below 10 kHz, then a sufficiently high order Butterworth filter should provide ample attenuation, without affecting loop stability.

A second, more powerful approach is to use a lower order filter in conjunction with an average and hold. Averaging, and then holding the output of the integrator over one cycle of the reference period, should entirely eliminate any periodic error attributable to the reference frequency.\(^9\) From a practical standpoint, there will be some periodic error due to the nonzero, though small error introduced by a real world sample-and-hold process. This periodic, residual error can now be reduced with the above mentioned low pass filter.

It perhaps seems that the topological location of this filtering within the loop has been changed for no apparent reason. From directly
following the phase detector, it now follows the integrator. See Figure 7, Blocks 10 and 11. By linear system theory, there can be no difference in performance with respect to attenuation of 10 kHz components of the phase detector. However, this average and hold/low pass filter combination could also help suppress reference frequency sidebands introduced by the digital interpolation circuitry, since it, too, is updated at a 10 kHz rate.

Linear system theory also states that the act of low pass filtering must phase shift the output with respect to the input. Such a delay tends to denegrate digital interpolation correction effectiveness, since the digital interpolation technique depends on a precise phaser relationship between phase detector output and digital interpolation correction signal. So the act of sliding the filtering past the integrator is well justified.

Up to this point, it has been assumed that the digital interpolation circuitry is perfectly adjusted, thus not contributing to the spectral impurity of the output. In reality, such perfect tuning is not possible. It might be worthwhile, in the light of evaluation of experimental results, to spend a modest amount of effort discussing the effects of incomplete phase-error cancellation.

If \( \phi_e(t) \) is not completely cancelled by \( \phi_c(t) \), there will be a scaled down version of Figure 6 applied to the input of the integrator. Most of the energy of such a signal would be at the fundamental of the sawtooth frequency, \( 10^4 \cdot \alpha \) Hz. Some energy will be at the higher harmonics, as dictated by Fourier analysis. Since the waveform is
really a staircase ramp, with steps spaced 100 μsec apart, there will be a very small amount of energy at multiples of 10 kHz. This error signal is integrated, and then applied to the voltage controlled oscillator, frequency modulating the output.\textsuperscript{17} What we are after is how the energy of voltage controlled oscillator output signal is spread, given that its input is being frequency modulated by some abstruse waveform. The only hope of arriving at any mathematically manageable result is to abandon the true waveshape of the phase error signal, and assume a sinusoidal perturbation of the same approximate magnitude.

In a frequency modulated wave with sinusoidal modulation the instantaneous angular velocity is varied according to the relation:

\[ \omega_i = \omega + 2\pi \cdot \Delta f \cdot \cos \omega_m t \]

where \( \omega \) is the average of unmodulated frequency of the oscillator, \( \Delta f \) is the maximum frequency displacement, and \( \omega \) is \( 2\pi \) times the modulating frequency, \( f_m \).

Since in general, a periodic wave can be written as \( x(t) = \sin \phi(t) \), and since \( \phi(t) = \int_0^t \omega_i \cdot dt \), \( x(t) \), for FM modulation can then be written as

\[ x(t) = A \sin \left( \omega t + \frac{2\pi f_m}{2\pi f_m} \cdot \sin \omega_m t \right) \]

or \( x(t) = A \sin \left( \omega t + m_f \cdot \sin 2\pi f_m \cdot t \right) \).
where \( m_f = \text{(maximum frequency deviation)} \div \text{(modulating frequency)}. \)

The frequency components contained in \( x(t) \) can be determined by expanding the right-hand side of the equation by the trigonometric formula for the sum of two angles. \( x(t) \) can then be written as

\[
x(t) = A\{J_0(m_f) \sin \omega t \\
+ J_1(m_f)[\sin (\omega + \omega_m)t - \sin (\omega - \omega_m)t] \\
+ J_2(m_f)[\sin (\omega + 2\omega_m)t - \sin (\omega - 2\omega_m)t] \\
+ J_3(m_f)[\sin (\omega + 3\omega_m)t - \sin (\omega - 3\omega_m)t] \\
+ \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots
\]

where \( J_n(m_f) \) means the Bessel function of the first kind and \( n \)-th order, with argument \( m_f \).

The output spectrum will then contain energy at the carrier frequency, plus and minus integer multiples of the modulation frequency, with sideband amplitudes governed by the ratio of Bessel functions.

The modulation index, \( m_f \), is the key parameter. For the case of the voltage controlled oscillator, \( m_f = \frac{\Delta V \cdot K_{vco}}{10^4 \cdot \alpha} \), where \( \Delta V \) = the amplitude of the sinusoidal perturbations at the input, and \( K_{vco} \) is the familiar gain constant, in Hz per volt.

The problem of sideband location and amplitude is no longer unman-
ageable. Once the value of $m_f$ has been calculated, the amplitude of the sidebands can be obtained by consulting a table of Bessel functions. Appendix One graphically tabularizes the amplitude of the fundamental and first five sideband pairs, as a function of $m_f$. Note that as $\Delta V$ and correspondingly $m_f$, go to zero, so do all the sideband amplitudes. It is also interesting to note that in this realm of a small $m_f$ ($m_f \approx 0$), the only sideband of any substantial magnitude is the first, with amplitude approximately equal to one half $m_f$. (This last result is based on the more-or-less linear slope of the graph of the first sideband component, near the origin.)

A second less profound frequency-domain-related issue is the range of the output of the oscillator. The range of the output frequency now obtainable is $5 \text{ MHz} \leq f_{\text{out}} \leq 6 \text{ MHz}$. This 20% range is limited by dynamic range considerations of the voltage controlled oscillator. It might prove more worthwhile if the output could be made to cover a more useful frequency range, say 1 Hz to 1 MHz. This can be easily accomplished by mixing the output of the voltage controlled oscillator with a 5 MHz phase-locked standard, and low pass filtering. See Figure 7, Blocks 12, 13, and 14.
Chapter Five
SPEED OF RESPONSE

Within the framework of a linear system, once the system loop dynamics are established, the step response and its respective settling time are completely determined. However, settling time can be shortened, independent of loop dynamics, by the use of loop-variable presetting: Given even a fairly rudimentary knowledge of the oscillator's open loop characteristics, a "look-up" table is prepared so that, for a given input, the input voltage to the voltage controlled oscillator is preset to a value close to its final, steady state. See Figure 7, Block 15. For example: If settling time is defined as the time to be within .1% of final value, with fractional error, $f_e$, having exponential dependence: $f_e = \exp(-t/T)$; then settling time, $t_s$, equals 6.9T, $[\exp(-6.9) = .001]$. Presetting to within 10% of final value immediately after application of the step implies $f_e = .1 \exp (-t/T)$. Thus $t_s$ equals 4.6T, $[\exp(-4.6) = .01]$. In other words, the loop has to settle to only 1% of its detected error value to reach an overall error of .1%, with a saving of 2.3T seconds.

One need not resort to specific step response equations to appreciate the value of presetting. Regardless of the manner in which a system proceeds to reach final value, if all necessary variables are initially preset to a value close to their final, intuitively, the system must reach steady state faster. This result will be particularly useful when a step change in synthesized frequency is demanded which far exceeds the limit imposed for linear system response.
PART TWO

EXPERIMENTAL VERIFICATION
Chapter Six
DISCUSSION OF CONSTITUENT PARTS

The finalized block diagram of the Digitally Interpolating Frequency Synthesizer used for experimental verification is shown in Figure 7.

A 5 MHz temperature-compensated crystal oscillator is used for the output reference oscillator (Figure 7, Block 12). Since this 5 MHz signal is to be phase-locked to the 10 kHz reference, the 10 kHz reference frequency is derived by a digital, divide-by-500 counter. (Figure 7, Block 1)

The voltage controlled oscillator (see Figure 8), is a modified-Pierce Oscillator\(^{18}\), whose frequency is controlled by a set of six variable-capacitance diodes. The diodes are used in a back-to-back configuration to reduce second harmonic distortion. The output, a TTL-compatible 10-12 MHz square wave, is fed into a divide-by-two flip-flop. The flip-flop insures that there will always be a large frequency difference between voltage controlled oscillator and the 5 MHz local oscillator, thus preventing any problem of the voltage controlled oscillator locking to the 5 MHz reference through the output mixer. (The output mixer is a standard transconductance amplifier\(^{15}\), ran at low levels to prevent harmonic distortion, whose output is followed by a stage of gain. See Figure 9.) The transfer characteristic of voltage controlled oscillator output frequency versus input voltage is shown in Figure 10. The graphically derived incremental gain, \(\frac{\Delta f}{\Delta V}\), is given in Table 6.1.

The use of an analog switch, (Figure 7, Block 16), is motivated
<table>
<thead>
<tr>
<th>Frequency</th>
<th>Incremental Gain (kHz/Volt)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.00</td>
<td>66</td>
</tr>
<tr>
<td>5.10</td>
<td>250</td>
</tr>
<tr>
<td>5.20</td>
<td>225</td>
</tr>
<tr>
<td>5.30</td>
<td>180</td>
</tr>
<tr>
<td>5.40</td>
<td>165</td>
</tr>
<tr>
<td>5.50</td>
<td>158</td>
</tr>
<tr>
<td>5.60</td>
<td>130</td>
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<tr>
<td>5.70</td>
<td>120</td>
</tr>
<tr>
<td>5.80</td>
<td>95</td>
</tr>
<tr>
<td>5.90</td>
<td>87</td>
</tr>
<tr>
<td>6.00</td>
<td>82</td>
</tr>
</tbody>
</table>
by practical considerations, as yet not mentioned. See Figure 11. The voltage of a logic '1' is apt to change with temperature, supply voltage, etc. In previous diagrams, the output of the comparator (a digital gate) drove directly into the integrator, and as such, would render the system highly sensitive to such changes in digital gate output voltage. (If the peak value of the square wave changes, so must its average.) This problem is solved by inserting an analog switch between phase detector output and integrator. An analog switch is not susceptible to power supply and temperature variations, and assumes an output voltage of ground, or a well-defined reference voltage, depending on the logical input applied. It was derived in Chapter Three that the digital interpolation correction voltage was inversely proportional to \( N \), for a given full-scale amplitude of phase detector output. Electronically, this is hard to implement. Since electronic linear scaling is much easier than taking the reciprocal, the full scale value of the digital interpolation correction voltage is kept constant, and the full scale value of the phase detector output is changed by changing the analog switch voltage. The switch voltage magnitude is 5 Volts, when \( N \) is set to 500, and scales linearly with \( N \). Since the analog switch works in conjunction with the phase comparator circuitry (Figure 12), it is best to describe their operation by one, overall, transfer function:

\[
\frac{V_{\text{out}}}{\phi_{\text{in}}} = \frac{5 \text{ Volts}}{2\pi} \cdot \frac{N}{500} \quad \text{(Volts per radian)}
\]
FIGURE 11
FIGURE 12 - Part 2
This 20% ($\frac{600}{500}$) change in phase detector gain will not affect stability, as its gain change will be precisely cancelled by a similar effect in the divide-by-N counter.

The initial condition presetter (See Figure 13) takes advantage of the reasonably linear transfer function of the voltage controlled oscillator. Notice that the curvature of the graph of Figure 11 does not change substantially. The circuitry of Figure 13 realizes a straight line approximation (the dashed line of Figure 10) to the voltage controlled oscillator transfer characteristic. Note that out of 12 Volts full scale, the linear approximation, with no extra diode breakpoint network, is never off by more than 0.5V, or 4%.

The digital interpolation circuitry (Figure 11) and the analog switch output are summed together, and fed into the integrator (Figure 11). Proper scaling of the correction term is accomplished by setting

$$\frac{D_0}{R_D} \frac{A_0}{R_A} = \frac{1}{N},$$

where $D_0$ is the full scale amplitude of the digital-to-analog converter (Amplifier B63), $A_0$ is the analog switch reference voltage, and $R_A$ and $R_D$ are the resistances shown.

A two stage sample-and-hold (Figure 14) is used to circumvent the problem of high-speed-acquisition sampling. Each sampling gate is closed for 40 μsec, which is more than ample time to reach steady state.

The loop low pass filter, also in Figure 14, a five pole active Butterworth filter, has a 1 kHz corner frequency. The output low
pass filter is a tandem combination of a seven pole L-C filter with a 1 MHz corner frequency, followed by a seven pole L-C filter with corner a 15 MHz frequency, to insure that no unwanted high frequency signals were passed through to the output.
Chapter Seven

STABILITY CONSIDERATIONS

As mentioned in a previous chapter, closing the loop around a double integration must lead to instability, unless some form of compensation is employed. The descriptive blocks of Figure 7 have now been replaced by their electronic counterparts, each with its respective transfer function. See Figure 15. These explicit relationships make it possible to explore the compensation issue in proper numerical detail.

To retain maximum speed of response and desensitivity, lead compensation (the addition of a zero-pole pair) will be used. The most convenient location to realize the zero is in the integrator. (Admittedly the pole cannot help stability. It does however insure that the output of the integrator is continuous, and attenuative to 10 kHz, a necessary condition for proper operation of the sample-and-hold.)

The loop was designed to reach unity gain at approximately 30 Hz, the geometric mean of the lowest synthesized frequency (1 Hz) and the break frequency of the loop filter (1 kHz). The expression for the loop gain is, without compensation:

\[ G_1(s) = \frac{2\pi}{s} \cdot \frac{5}{2\pi} \cdot \frac{N}{500} \cdot e^{-10^{-4}\cdot s} \cdot F(s) \cdot \frac{1}{N} K_{vco}(N) \cdot e^{-10^{-4}\cdot s} \]

\[ = \frac{e^{-1.5\times10^{-4}\cdot s}}{s^2} \cdot F(s) \cdot K_{vco}(N) \]
where \[ F(s) = \frac{1}{(\frac{s}{6280})^2 + (\frac{2 \cos 36^\circ}{6280}) \cdot s + 1} \cdot \frac{1}{(\frac{s}{6280})^2 + (\frac{2 \cos 72^\circ}{6280}) \cdot s + 1} \cdot \frac{1}{\frac{s}{6280} + 1} \]

the last term in \( e^{-s} \), and the extra block in Figure 15 take into account the sampled nature of the loop, and is in no way related to the sample and hold process.\(^1\) The delay corresponding to \( e^{-0.5 \times 10^{-4}s} \) is 50 \( \mu \)sec implying that on the average, information is delayed one-half of a reference period.

Note that the explicit dependence of \( G_1(s) \) on \( N \) disappears because of the linear dependence of analog switch voltage on \( N \). However, \( N \) is still implicitly involved because the incremental gain of the voltage controlled oscillator is not constant, but is dependent on output frequency, in other words, \( N \).

Performance of the digital interpolation technique was worsened by the sample and hold, and hence was not used in the final circuit. This was due to a subtle timing problem in the design of the sample and hold, rather than to any theoretical misconception. Therefore, \( G_1(s) \), the loop transmission with one of the two time delays deleted, instead of \( G_1(s) \) will be considered, in order to insure agreement between theory and experiment. A bode plot of \( G_1(s) \) shows that unity gain occurs at 40 Hz for the lowest value of \( K_{VCO} \), and 79 Hz for the highest. See Figure 16. Experimentally, this is born out by Figures 17a and 17b,
which show the oscillation frequencies obtained when the compensation zero is not present.

There might seem to be some ambiguity as to where to put the zero, since crossover frequency is dependent on the oscillator gain constant. For a zero and two lower frequency poles, the phase margin increases with increasing loop gain. The solution used was to compensate the system for lowest loop gain, since this would yield worse case phase margin. This technique will break down once loop gain increases sufficiently to bring the loop filter poles into play. Hopefully the loop filter won't greatly affect stability, since the higher frequency poles are a factor of 30 higher than the zero location.

The lowest gain occurs at 5 MHz, and hence the zero is placed at crossover frequency for this value of gain—96.6 dB at 200 rad/sec, with the pole at 1 kHz. The expression for the loop gain with compensation becomes:

\[ G_2(s) = \frac{e^{-\frac{10^{-4}s}{2}}}{s^2} \cdot F(s) \cdot \frac{.005s + 1}{1.6 \times 10^{-4}s + 1} \cdot K_{vco} (N) \]

\( G_2(s) \) is graphed along with \( G_1(s) \) in Figure 16, for the case of \( K_{vco} = 58820 \). The phase margin is 46.5°.

Table 7.1 lists loop gain and the corresponding phase margin for a representative sampling of possible output frequencies (different values of \( N \)). (The three place accuracy of Table 7.1 was obtained from a computer generated Bode plot. See Appendix 2.) These analytically derived phase margins can be checked by information obtained from
### TABLE 7.1

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Loop Gain (x1000)</th>
<th>Computer Phase Margin (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.00</td>
<td>66</td>
<td>46.4</td>
</tr>
<tr>
<td>5.10</td>
<td>250</td>
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<td>47.4</td>
</tr>
<tr>
<td>6.00</td>
<td>82</td>
<td>47.4</td>
</tr>
</tbody>
</table>

### TABLE 7.2

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>$P_0$</th>
<th>Second Order Zeta</th>
<th>Second Order Phase Margin (°)</th>
<th>Computed Phase Margin (°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.00</td>
<td>1.2</td>
<td>.46</td>
<td>48</td>
<td>46.4</td>
</tr>
<tr>
<td>5.10</td>
<td>1.38</td>
<td>.30</td>
<td>33</td>
<td>29.0</td>
</tr>
<tr>
<td>5.20</td>
<td>1.38</td>
<td>.30</td>
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<td>33.4</td>
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<td>1.22</td>
<td>.44</td>
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</tr>
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<td>1.24</td>
<td>.42</td>
<td>45</td>
<td>41.8</td>
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<td>5.50</td>
<td>1.25</td>
<td>.415</td>
<td>44</td>
<td>42.5</td>
</tr>
<tr>
<td>5.60</td>
<td>1.26</td>
<td>.40</td>
<td>43</td>
<td>45.4</td>
</tr>
<tr>
<td>5.70</td>
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<td>.38</td>
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<td>46.3</td>
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<tr>
<td>5.80</td>
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<td>47.4</td>
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<tr>
<td>6.00</td>
<td>1.28</td>
<td>.38</td>
<td>41</td>
<td>47.4</td>
</tr>
</tbody>
</table>
experimentally exciting the linear step response of the system at dif-
ferent frequencies. (Measuring the step response implies disconnecting
the initial condition presetter or the linearity constraint will be
violated). Figures 18a through k are an oscilloscope presentation of
the voltage applied to the voltage controlled oscillator under a 40 kHz
change in desired output frequency (N was switched electronically).
Note that on the photographs that the gain of the voltage controlled
oscillator is inversely proportional to the amount of voltage change
of the step. Table 7.2 list the normalized peak overshoot, $P_o$, the
corresponding closed loop damping ratio, and the respective phase margin,
derived as if $P_o$ were taken from a second order system. The final
column of Table 7.2 is the phase margin obtained from the Bode plot of
$G_2(s)$ of Figure 16, repeated for convenience. Experiment agrees most
adequately with theory. The predicted phase margin is off by at most
6.4°, the average error is 3.9°, which, considering the complexity of
the system, is a rather astounding result.
FIGURE 18
Chapter Eight
PRESETTER EFFECTIVENESS

The most direct way to demonstrate presetter effectiveness is to simply perform an A-B comparison of the step response with, and without presetting. Figures 19 and 20 do just that.

These figures show the input voltage to the voltage controlled oscillator, as various amplitude output frequency changes are commanded. Figure 19 applies a step of 40 kHz. Without presetting, Figure 19a settling time is approximately 15 μsec. Figure 19b shows that with presetting, the time to settle to 10% is reduced to perhaps 12 μsec. More substantially, however, overshoot is reduced by a factor of five.

Figure 20 applies a step of 800 kHz, a step size that is well out of the range of linearity. For this case, the effect is even more dramatic. Figure 20a settles in 100 μsec, whereas Figure 20b, with presetting, settles in 15 μsec. Overshoot is reduced from 200% to 15%.

Settling time could have been shortened even further if more care had been taken to approximating the voltage controlled oscillator open-loop characteristic. Nonetheless, even with this single-line approximation, the usefulness of this technique is adequately demonstrated.
Chapter Nine
EXPERIMENTAL EFFECTIVENESS OF THE DIGITAL INTERPOLATION CORRECTION SIGNAL

The experimental results of Chapters Six through Eight show that the theoretical calculations of Part One are truly indicative of the performance of a phase locked loop. What remains to be demonstrated is the synthesizer raison d'être. The fact that the system can have 500 Hz closed loop bandwidth (using Figure 18b and the relation \( \omega_n = \frac{2}{T_r} \)), is of no great importance unless frequencies well below the reference and closed-loop-bandwidth frequencies can be synthesized with high spectral purity.

One comment is in order with respect to interpreting the spectrum analyzer output. The fraction \( \alpha \) was chosen to be .01, corresponding to 100 Hz. A 100 Hz signal was used for two very practical reasons. First, because of breadboard construction techniques, 60 Hz signal were omnipresent in ground loops and direct radiation from nearby sources as fluorescent lights and electromagnets. (The system, even when run on batteries still contained 60 Hz sidebands only 40 dB down.) So choosing 100 Hz placed any sideband far enough away from 60 Hz signal to be distinctly recognizable, with no ambiguity. There still is the possibility of using a synthesized frequency of say 40 Hz lower (rather than higher) than the unwanted 60 Hz. This brings up the second reason; the bandwidth of the spectrum analyzer used was a minimum of 10 Hz. Hence a 20 or 30 Hz signal would hardly be discernable from the main synthesized
frequency.

In light of the above issues, the spectrum analyzer output is based on a center frequency of 5.0001 MHz, implying \( N = 500 \), and \( \alpha = .01 \).

A run of spectrum analyzer output without correction signal must be made to establish some kind of reference on which a comparison may be based. We shall be able to use the results of Chapter Four to calculate an order of magnitude estimate of the sideband amplitudes.

Without any correction, the periodic phase error applied to the integrator input should be approximately one five-hundredth times the full scale value of the phase detector, times the closed-loop gain of the system, evaluated at 100 Hz. Ignoring any loop attenuation as a first cut, the voltage controlled oscillator would see approximately one millivolt. A 1 mV signal would translate into an

\[
m_f = \frac{60\text{kHz/volt} \times 1 \text{ mV}}{100 \text{ Hz}} = .6
\]

Checking Appendix One yields a first harmonic of 0.26 the amplitude of the carrier, which translates to approximately -12 dB. This figure, plus any loop attenuation is certainly not terribly out of agreement with the experiment value of -18 dB shown of Figure 21a.

Connecting the correction circuitry, the true worth of the digital interpolation technique is seen. The first sideband drops more than 30 dB below the uncorrected value, and approximately 50 dB below the fundamental. See Figure 21b. A quick calculation reveals the approxi-
Center frequency: 5.0001 MHz
H-scale: 100 Hz/major division
V-scale: 10 dB/major division

FIGURE 21a
Center Frequency = 5.0001 MHz
H-scale: 50Hz/major division
V-scale: 10dB/major division

FIGURE 21b
mate voltage magnitude of the frequency modulating signal applied to
the voltage controlled oscillator:

\[-50 \text{ dB} = \frac{1}{300} = \frac{m_f}{2} = \frac{\Delta f}{2 \cdot f_m} = \frac{\Delta V \cdot K_{vco}}{2 \cdot f_m} = \frac{\Delta V \cdot 60 \text{ kHz/volt}}{2 \cdot 100 \text{ Hz}}\]

This implies that \(\Delta V = 10^{-5}\) volts or 10 \(\mu\)V. This sort of error is well
within component tolerance and accuracy.

In as much as spectrum analyzer bandwidth precludes the measure-
ment of a 1 Hz (\(\alpha = .0001\)) synthesized signal and its (unwanted) side-
bands, it is still possible to obtain some information as to the spec-
tral purity of such a low frequency signal. The method used is simply
a visual inspection of the signal present at the output of the mixer/
low pass filter combination, as viewed on an oscilloscope. The syn-
thesizer is set to \(N = 500\), \(\alpha = .0001\), implying a synthesized frequency
of 5.000001 MHz (5 MHz + 1 Hz). The output mixer/low pass filter com-
bination effectively subtracts off the 5 MHz, leaving the 1 Hz signal.

Figure 22a shows the output with no phase correction voltage
added. The average frequency is right; the period is one second. But,
the phase pattern (the actual shape of the waveform) is not. Figure
22b shows the same 1 Hz signal with the correction circuit applied.
Although a mathematical analysis of harmonic content is not possible
from such a picture, it is safe to say that there is a vast improvement
from the uncorrected case.

The data of Part Two more or less speaks for itself, in terms of
a conclusion. The feasibility breadboard model shows that the technique
of digital interpolation is a very viable method for increasing the speed of response without deteriorating synthesizer resolution. The results seem to indicate that if there exists any limit to the interpolation technique, it lies not in the validity of the theory, but rather in the method of circuit implementation.
PART THREE
SUPPORTIVE INFORMATION
APPENDIX I
POLES OF \( AF \)?
\[
\begin{align*}
\text{\( \square : \)} & \quad 0, 0, -6.28E3, -6.28E3, Q  \\
\text{LIST ON ONE LINE: } \omega \text{n1}, \text{ZETA1}, \omega \text{n2}, \text{ZETA2}, \ldots
\end{align*}
\]
\[
\begin{align*}
\text{\( \square : \)} & \quad 6.28E3, (200 \pm 5), 6.28E3, 200 \pm 2.5
\end{align*}
\]
ZEROS OF \( AF \)?
\[
\begin{align*}
\text{\( \square : \)} & \quad -200, E
\end{align*}
\]
DELAY TIME?
\[
\begin{align*}
\text{\( \square : \)} & \quad 5E^{-5}
\end{align*}
\]

| \( \omega \) | 20LOG|H(\( \omega \)| | ANG(\( \omega \)| |
|---|---|---|
| 1.000E01 | 56.4017 | -177.5527 |
| 1.259E01 | 52.4080 | -176.9208 |
| 1.585E01 | 48.4180 | -176.1270 |
| 1.995E01 | 44.4338 | -175.1311 |
| 2.512E01 | 40.4588 | -173.8842 |
| 3.162E01 | 36.4980 | -172.3279 |
| 3.981E01 | 32.5595 | -170.3949 |
| 5.012E01 | 28.6551 | -168.0123 |
| 6.310E01 | 24.8025 | -165.1099 |
| 7.943E01 | 21.0263 | -161.6363 |
| 1.000E02 | 17.3589 | -157.5862 |
| 1.259E02 | 13.8387 | -153.0373 |
| 1.585E02 | 10.5046 | -148.1844 |
| 1.995E02 | 7.3865 | -143.3510 |
| 2.512E02 | 4.4957 | -138.9551 |
| 3.162E02 | 1.8206 | -135.4396 |
| 3.981E02 | -0.6698 | -133.2016 |
| 5.012E02 | -3.0155 | -132.5626 |
| 6.310E02 | -5.2575 | -133.7850 |
| 7.943E02 | -7.4317 | -137.1170 |
| 1.000E03 | -9.5681 | -142.8432 |
| 1.259E03 | -11.6926 | -151.3321 |
| 1.585E03 | -13.8293 | -163.0816 |
| 1.995E03 | -16.0040 | -178.7730 |
| 2.512E03 | -18.2473 | -199.3600 |
| 3.162E03 | -20.5984 | -226.2711 |
| 3.981E03 | -23.1311 | -262.0020 |
| 5.012E03 | -26.1959 | -311.7648 |
APPENDIX II
1 MA V
POLES OF AF?
□:
0, 0, -6.28E3, -6.28E3, Q
LIST ON ONE LINE: \( \omega N1, ZETA1, \omega N2, ZETA2, \ldots \)
□:
6.28E3, (200±5), 6.28E3, 200±2.5
ZEROS OF AF?
□:
-200, E
DELAY TIME?
□:
5E-5

| \( \omega \)  | 20LOG|\( \mathcal{H}(\omega) \) | \( \text{ANG}(\omega) \) |
|----------------|----------------------|----------------------|
| 3.800E02       | -96.5702             | -133.5344            |
| 1.250E03       | -108.0178            | -151.0239            |
| 1.120E03       | -107.0046            | -146.6486            |
| 9.100E02       | -105.0868            | -140.1871            |
| 8.400E02       | -104.3437            | -138.2749            |
| 8.100E02       | -104.0049            | -137.5055            |
| 6.800E02       | -102.3611            | -134.6242            |
| 6.300E02       | -101.6339            | -133.7704            |
| 5.100E02       | -99.5793             | -132.5869            |
| 4.700E02       | -98.7640             | -132.5642            |
| 4.500E02       | -98.3242             | -132.6449            |
BIBLIOGRAPHY


