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Fabrication of Six Degrees-of-Freedom Hexflex Positioner With Integrated Strain Sensing Using Nonlithographically Based Microfabrication

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A process flow is described for the low cost, flexible fabrication of metal microelectromechanical systems (MEMS) with high performance integrated sensing. The process is capable of producing new designs in ≈1 week at an average unit cost of <$1 k/device even at batch sizes of ≈1–10, with expected sensing performance limits of about 135 dB over a 10 kHz sensor bandwidth. This is a ≈20× reduction in cost, ≈25× reduction in time, and potentially >30× increase in sensing dynamic range over comparable state-of-the-art compliant nanopositioners. The nonlithographically based microfabrication (NLBM) process is uniquely suited to create high performance nanopositioning architectures which are customizable to the positioning requirements of a range of nanoscale applications. These can significantly reduce the cost of nanomanufacturing research and development, as well as accelerate the development of new processes and the testing of fabrication process chains without excess capital investment. A six degrees-of-freedom (6DOF) flexural nanopositioner with integrated sensing for all 6DOF was fabricated using the newly developed process chain. The fabrication process was measured to have ≈30 μm alignment. Sensor arm, flexure, and trace widths of 150 μm, 150 μm, and 800 μm, respectively, were demonstrated. Process capabilities suggest lower bounds of 25 μm, 50 μm, and 100 μm, respectively. Dynamic range sensing of 52 dB was demonstrated for the nanopositioner over a 10 kHz sensor bandwidth. Improvements are proposed to approach sensor performance of about 135 dB over a 10 kHz sensor bandwidth. [DOI: 10.1115/1.4049123]

Keywords: piezoresistor, microfabrication, nanopositioner, strain gage, sensor, Schottky diode, nonlithographically based microfabrication

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1 Introduction

This work demonstrates a nonlithographically based microfabrication (NLBM) process flow which can be used to fabricate metal micro-electromechanical systems (MEMS) with integrated sensing and do so in small batches (<10 devices) with low average device cost (<$1 k/device). This will allow for low-cost customizable nanopositioning architectures with integrated position sensing to be created [1,2] for a range of micro-/nano-manufacturing and metrology applications. Customized positioning platforms can surmount one of the main hurdles to nanomanufacturing research and development [3–8], as well as enable further developments through cost and customization benefits in personalized medicine [7], high-performance and parallel atomic force microscopy (AFM) metrology [6,9–12], improving accelerometers [13–15], and advanced memory storage [4,16]. This will accelerate the testing and development of new micronano fabrication processes, especially those using arrays [5]. It will also aid in the testing of fabrication process chains without excess capital investment, an active area of micromanufacturing research [17,18].

1.1 Motivation. Micro-electromechanical systems positioning require integrated sensing to take full advantage of miniaturization to ensure that the metrology component does not dominate the device and cost. Laser interferometry can run to ≈$1-10 k/axis [19] and can occupy upward a footprint much larger than the MEMS device in some cases [20]. Integrated sensing bypasses these size and cost issues by operating within the device footprint and utilizing similar (cost) fabrication processes. Such integrated sensing generally requires nm to μm scale electrical structures to be created on the MEMS device. A range of transducers are used in MEMS [8], including piezoresistive [2,21], capacitive [21], electrothermal [22], and piezoelectric [23].

A fabrication process for feasible, customizable, mesoscale MEMS nanopositioners must be able to meet several requirements in order to produce a device with integrated sensing: (i) bulk micromachine μm to mm scale mechanical structures out of robust materials like metals, (ii) surface micromachine nm to mm scale electrical structures on the surface of the mechanical structure, and (iii) do all of this at low device and production cost per device in order to make small batch sizes (<100) typical of research and development. Standard MEMS fabrication processes cannot feasibly access this region [24] due to the high capital costs and low process flexibility.

No established fabrication process chain can simultaneously meet all the requirements laid out above as shown in Table 1. Traditional fabrication can produce mm and larger scale parts and do so out of many different materials. The wide range of material choice gives designers the freedom to find the material that is best suited for the application in this case a robust material that can sustain handling, attachment of payloads, scratches, and prolonged use. However, traditional fabrication processes struggle to create extremely thin patterned layers of materials commonly

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Table 1 Comparison of fabrication methods

Requirement	Capability	Macroscale fabrication	MEMS lithographic fabrication	NLBM
Mechanical structures	Bulk μmachining	✓	✓	✓
Electrical structures	Surface μmachining		✓	✓
Robust material	Metals, polymers	✓		✓
Low average cost in small batches	<$1 k/device	✓		✓

used for integrated electronics. Integrated circuit-based MEMS microfabrication can produce structures over the correct size scales; however, it has significant limitations in the material selection as bulk microfabricated mechanical structures are typically made from crystalline materials [8,25]. Integrated circuit (IC) microfabrication has been used to create micro- and mesoscale nanopositioners; however, it results in high costs (≈$20 k just for equipment costs), long fabrication times (≈6 months) and brittle structures that are unsuited for general operation [2]. Neither fabrication process alone meets all the requirements for the creation of a customizable low-cost per device MEMS nanopositioner with integrated sensing. A hybrid process-NLBM-is needed to draw from the strengths of each of these to make a feasible fabrication process chain.

A range of nonlithographically based fabrication processes have shown the potential to generate needed structures while meeting the conditions described above [26,27]. But these cannot be presently integrated together due to fabrication incompatibilities. Previous work has been done on bulk micromachining of metal mesoscale structures [17,26,28–33], and this work has shown micromilling to be an accurate and effective method of creating μm to cm scale structures. Surface micromachined electrical structures have also been demonstrated [27,34,35]; however, these two types of structures have not generally been integrated due to interfaces incompatibilities. Here, we will demonstrate a fabrication process chain that is capable of meeting both bulk and surface micromachining requirements as well as cost limitations, all while handling the challenges of the multiscale interfaces.

1.2 Hexflex Nanopositioner. The nonlithographically based microfabrication process was driven by the need to fabricate a metal MEMS nanopositioner based around the mesoscale Hexflex architecture [36] required for nanomanufacturing [37], as shown in Fig. 1. The Hexflex architecture is a six degrees-of-freedom (6DOF) planar flexural nanopositioning platform which is linked to ground via six flexural bearings in series, each of which provides a location of integrated strain sensing [2]. The sensors are designed via previously described work on semiconductor interfaces [38] and piezoresistor performance [39,40]. Integrating sensing was the main thrust of this work; however, full 6DOF actuation may be integrated into the design via three paddles on the central stage. Each bears magnetic Halbach arrays that can be driven bidirectionally via Lorentz force generation, and in 2DOF, either vertically or in-plane [41,42].

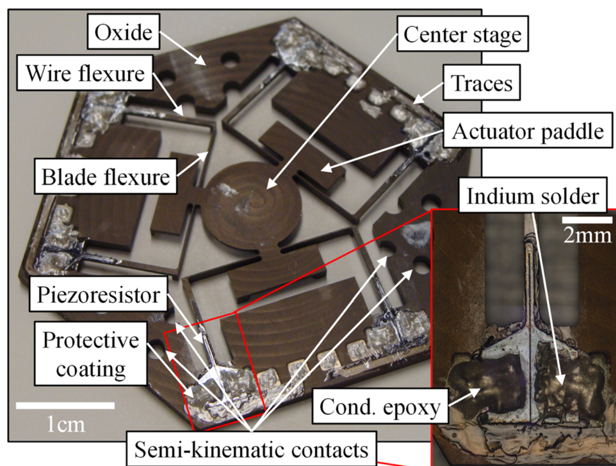

Fig. 1 Fabricated metal flexural nanopositioner with single crystalline silicon piezoresistor integrated sensing. The final fabricated device is shown, with 150 μm arm dimension single crystal silicon piezoresistors cured to titanium flexures.

Previous work on the Hexflex architecture has produced this topology on the microscale [43,44], the mesoscale [2], and the macroscale [36]. Unfortunately, none of these designs have produced a platform that can be feasibly used for nanomanufacturing/metrology research and development [8,37] which requires (i) low per-device cost, even in small batches, (ii) robustness during operation, and (iii) both integrated sensing and actuation. The new NLBM fabrication process is required to create the Hexflex architecture that can meet all three of these requirements.

2 Fabrication Process Overview

2.1 Flow. The overall process flow is discussed here to provide a high-level understanding of the fabrication process chain. The NLBM process occurs in four main steps: (i) bulk micromachining, (ii) surface micromachining, (iii) sensor integration, and (iv) circuit bonding, as shown in Fig. 2.

These steps are summarized here and will be described in more detail below. The bulk micromachining step forms the mechanical structure of the device. The surface micromachining step creates electrical traces and insulation on the device surface. The sensors are formed and cured to the device in the sensor integration step using the thin film patterning and transfer process (TFPT). The circuit bonding step links the sensors up with the surface circuitry to form integrated strain sensors. The order of the operations has been chosen to decouple the fabrication process to maximize the process chain flexibility. The substrate and sensors are produced separately and then joined at the sensor integration step.

The TFPT process occurs in five main steps, (i) lamination, (ii) patterning, (iii) etching, (iv) transfer, and (v) delamination, as shown in Fig. 3 and described in more detail below. These steps are used to anchor a thin wafer to a more rigid handling surface,

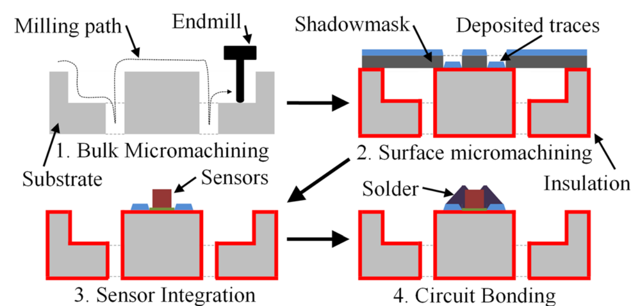

Fig. 2 Schematic of NLBM process steps, showing 1—bulk micromachining of the metal/polymer mechanical structure, 2—surface micromachining of the electrical traces for the sensors, 3—Sensor integration to attach the piezoresistors, and 4—circuit bonding to link the piezoresistors into the surface electrical structures

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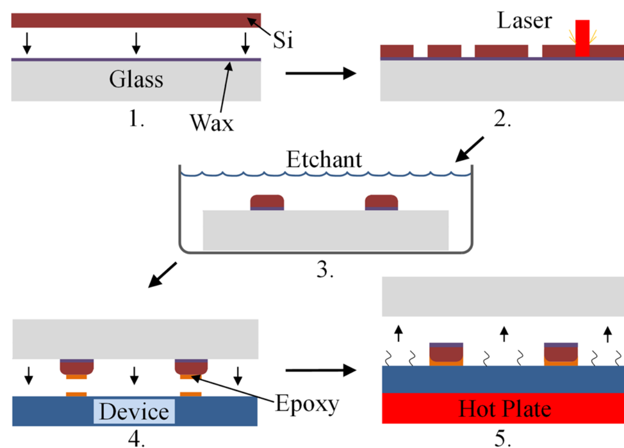

Fig. 3 Schematic of TFPT process steps, showing 1—lamination of a thin silicon wafer to a glass substrate with adhesive wax, 2—laser patterning of the silicon, 3—etching of the laser-induced damage, 4—transfer of the patterned silicon to the device, and 5—delamination of the stamp

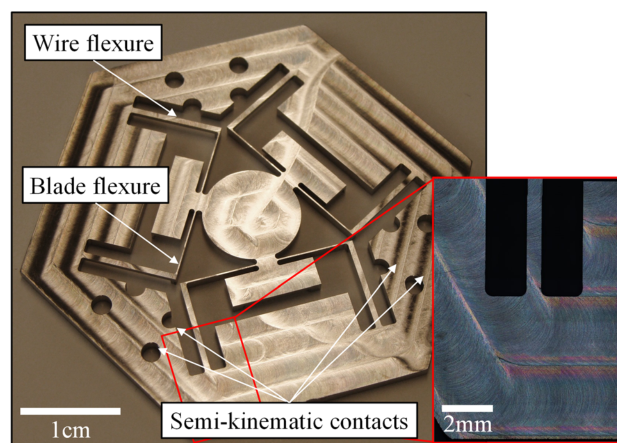

Fig. 4 Bulk micromachined metal mechanical structure, produced with micromilling. This is the titanium body of the Hexflex flexural nanopositioner.

cut structures into the wafer, remove laser damage and transfer the shapes to the device.

2.2 Generalization. The NLBM process envisioned here has broad application beyond the Hexflex nanopositioner. The process has been laid out in order to be generalizable to other structures, size scales, substrate materials, and other sensors [8] including carbon nanotubes [45], commercial piezoresistors [46], and printed strain gages [47]. Fundamentally, the process requires two features. First, that the substrate surface be nonconductive and adhesive compatible (temperature-wise). This leaves the design open to high temperature plastics, metals (which can be coated with an insulator), ceramics, glasses, or other materials. Second, the sensor surface must at some point be accessible for TFPT. Later, steps could attach further structures above and around the sensor surface if desired. Multiple TFPT steps could be carried out for sensors at different orientations, and TFPT stamps with step height variations could be developed for sensors at different heights in the structure. All parts of the NLBM process chain can be shifted in and out depending on material and rate requirements as noted in the scaling sections and expanded in Ref. [37]. The process decoupling between sensor and structure maximizes flexibility and enables the use of a wide range of materials. The process chain draws from both conventional machining and microfabrication to produce a hybrid assembly of methods that do not rely exclusively on costly and inflexible photolithography to transfer geometry to the device structure.

3 Bulk Micromachining

The bulk micromachining step covers the fabrication of the mechanically active substrate structure. The flexible elements, stage, and mechanical ground are formed in this step, as well as for the surfaces on which the electronics will be located. The focus of this research is on producing a process chain tuned to high flexibility, small batch size and low per-device cost, all to enable nanomanufacturing/metrology research and development. Mechanical micromilling was found to satisfy these conditions due to its relatively rapid ($\approx$4 h) fabrication rate, single device batch size, flexibility, and low cost ($200). The structure produced by micromilling in the bulk micromachining step is shown Fig. 4.

A hexagonal structure is created by micromilling titanium 6Al-4V stock on both surfaces. This produces a relatively smooth flat surface for electrical structure, shown face up in Fig. 4, while the flexure width and stage ribbing are formed via milling from the other side. The stock is held to the pallet using Electron Microscopy Sciences (Hatfield, PA) Crystalbond 509 , a thermally activated wax adhesive, with Cospheric (Santa Barbara, CA) SLGMS-2.52 75–90 μm soda-lime glass microspheres mixed in to ensure the stock and pallet maintain parallelism. Titanium is used for the excellent flexural properties and the ability to generate a mechanically robust oxide. Micromilling allows for 3D structures to be added to the normally planar Hexflex structure [2]. The wire and blade flexures are produced during the underside milling operation, so the whole device is released only in the final cutting operation. Semikinematic contacts are machined into the device structure to aid in alignment with the sensors during the later sensor integration transfer operation. Flexures were repeatably cut down to 150 μm width, with a measured variability of about 5 μm. Fabrication tests were successful down to flexure widths of 50 μm without significant alteration in the process. Below this level the flexures started to distort during cutting despite the adhesion to the substrate. Further details of the alignment, calibration, and handling are found in Ref. [37].

3.1 Scaling. Mechanical micromilling was adopted for the bulk micromachining step in this research to meet the demands of high flexibility, small batch size (down to a single device) and short lead time. This is by no means the only way of generating a micromechanical structure. Several others methods are suggested which shift the process chain toward higher volume, lower flexibility, including titanium DRIE [48], chemical machining [49], electrochemical machining [50], and LIGA [25].

4 Surface Micromachining

The surface micromachining step covers the fabrication of the electrically active surface structures. The traces and contact pads for linking the device into off-structure circuitry are formed in this step. Because the focus of this research is on producing a process chain tuned to high flexibility, small batch size and low per-device cost, processes were chosen that enabled rapid design changes with little cost/time investment. Insulation of the bulk structure by anodization and thermal oxide growth followed by deposition through a mechanical shadow mask was found to satisfy these conditions due to the relatively rapid ($\approx$3 days) fabrication rate, single device batch size, flexibility, and low cost ($200). This time is dominated by a 48 h thermal oxide growth step. The structure produced by insulation and deposition in the surface micromachining step is shown in Fig. 5.

A titania film is grown over the whole surface of the device, dulling the surface finish. A mechanical shadow mask is used to impart a pattern to the deposition, resulting in conductive surface electrical traces for linking the integrated sensing to off-device

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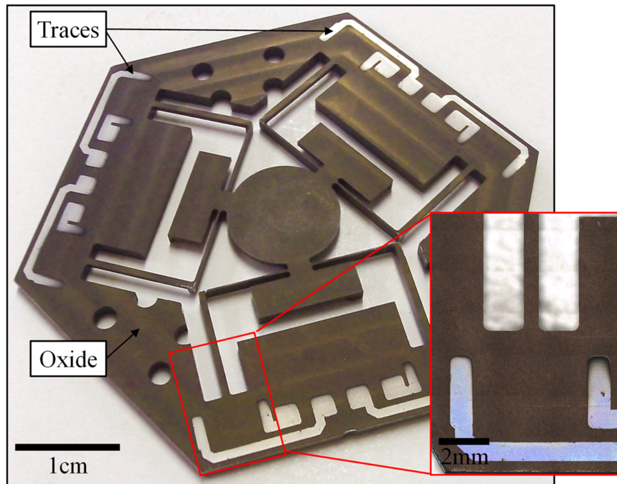

Fig. 5 Device with surface micromachined electrical structures, which are traces for circuit routing

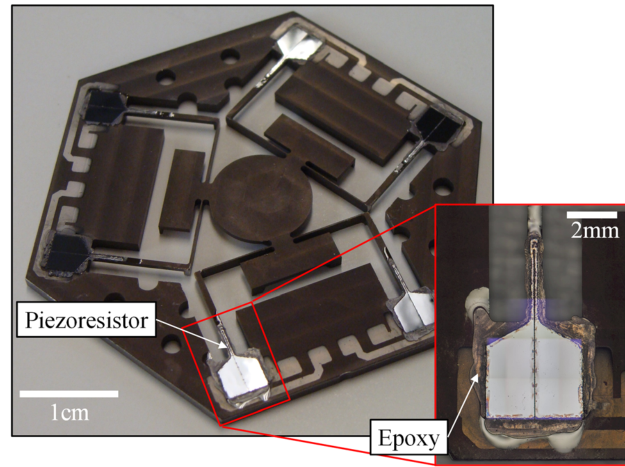

Fig. 6 Device with single crystalline silicon piezoresistors attached to the titanium flexures via the thin film patterning and transfer process

electronics [37]. A trace width of 800 μm was used for low resistance and robustness; however, the micromilling process can produce traces down to about 100 μm. These traces are shown in detail Fig. 5, where the sharp edges and high-fidelity pattern transfer can be observed. A slight shadowing effect is visible in the films due to the non-normal alignment of the source to the surface.

The oxide film growth process was tuned to optimize three main parameters: mechanical strength, electrical resistance, and uniformity. The thermal growth time, temperature, and anodization voltage were adjusted via the relations found in Refs. [51–54]. The titania film has excellent mechanical properties and can be produced in a simple, low-cost manner. Unfortunately, the combination of the trace, titania and bulk substrate form a metal-semiconductor-metal interface, which generates a complex Schottky barrier [55,56]. Two methods are proposed to improve the electrical properties of the titania film. First, the trace metal can be changed to generate a large Schottky barrier with the titania. Second, the bulk titanium can be biased to the maximum voltage observed on the surface, which is typically 5 V. Further details of the approaches, insulation, and deposition are found in Ref. [37].

4.1 Scaling. Electrochemical/thermal oxide formation and e-beam deposition through a mechanical shadow mask were adopted for the surface micromachining step in this research in order to meet the demands of high flexibility, small batch size (down to a single device) and short lead time. The insulation process and e-beam deposition are both fundamentally parallel processes, so the rate may be easily increased by processing multiple devices in parallel. This makes the surface micromachining step significantly more amenable to shifting along the rate scale than the bulk micromachining step. Several others methods are suggested which operate at other rate/flexibility scales, including other physical vapor deposition methods [25] and aerosol jet printing [57].

5 Sensor Integration

The sensor integration step covers the fabrication and placement of the device sensing onto the mechanical structure. This research focused on single crystalline silicon piezoresistors, and the TFPT process was developed to integrate these into the titanium device. The focus on high flexibility, small batch size, and low per-device cost led to the use of laser patterning of the silicon and manual preparation of the stamp. These steps can be used to rapidly produce new designs ($\approx$2 days) in small batches, and at low cost ($150).

A laser scribe is used to pattern thin silicon stock, which is transferred to the surface of the device via a handling stamp. The silicon piezoresistors are aligned to the device using semikinematic contacts and cured onto the base of the flexures, as shown in Fig. 6. Further details on the fabrication processes and parameters are found in Ref. [37].

5.1 Lamination. The first step of TFPT is the lamination of thin silicon wafer stock to a handling substrate which was a cut glass slide for this research. Two sides of the stamp are the original edges of the glass slide, so these surfaces are largely perpendicular to one another and flat. These edges will be brought into contact with semikinematic contacts throughout the process to act as references from which to determine alignment. The stock is visually placed on the stamp within approximately 1 mm of the location of the final, patterned gage. The silicon is adhered to the stamp by wicking Electron Microscopy Sciences (Hatfield, PA) MWM100 Black Mounting Wax (hydrofluoric acid resistant) under the silicon while on a hotplate bringing the stamp to 130 °C. The wax forms a 25–30 μm layer under the silicon, which will settle out to form a roughly even layer under the silicon and will expel air pockets if given sufficient time. The stamp is then prepared for patterning by coating with a thin organic film (hairspray), as shown in Fig. 7. This protects the silicon surface and captures the debris for easy removal.

5.2 Patterning. The second step of TFPT is the patterning of the silicon stock to create the desired piezoresistor shape in the desired location. An Electrox (Letchworth Garden City, Hertfordshire, UK) E-Box workstation with a 20 W Scorpion Rapide II Yb:fiber laser is used for the patterning process, combined with a semikinematic alignment fixture as shown in Fig. 8.

The laser cutting parameters have been optimized to maximize the thermal cutting efficiency per area of surface generated by the cut. A three step shape is cut into the silicon stock: the pattern, radial detiling and theta detiling, all as shown in Fig. 9. The detailed calibration and laser parameter selection methods are described in Ref. [37]. Piezoresistor arm widths of 150 μm were used as these were observed to easily survive the cleaning process. Improvements in the cleaning process to make it more gentle will enable the utilization of the observed patterning capability to create arm widths down to 45 μm, or about 25 μm after etching [37], which is about an order of magnitude smaller than commercial cured gages.

The patterned silicon is cleaned to remove part of the laser generated debris on the surface of the piezoresistor. A 60 s soak in

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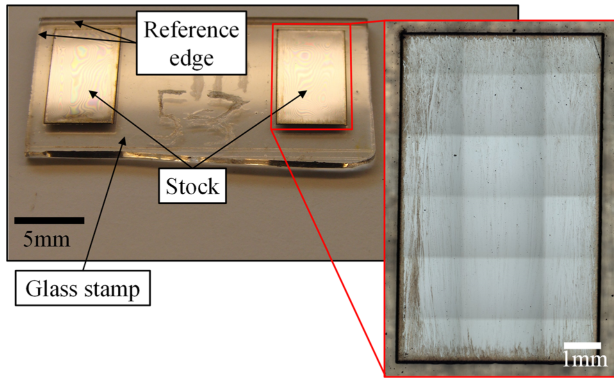

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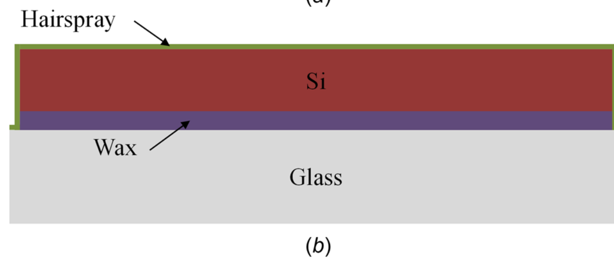


(*b*)

Fig. 7 (*a*) Stamp with laminated stock (*b*) schematic of stamp at completion of lamination step. Silicon stock has been attached to a glass stamp with wax, and a layer of hairspray has been coated over the surface of the stamp.

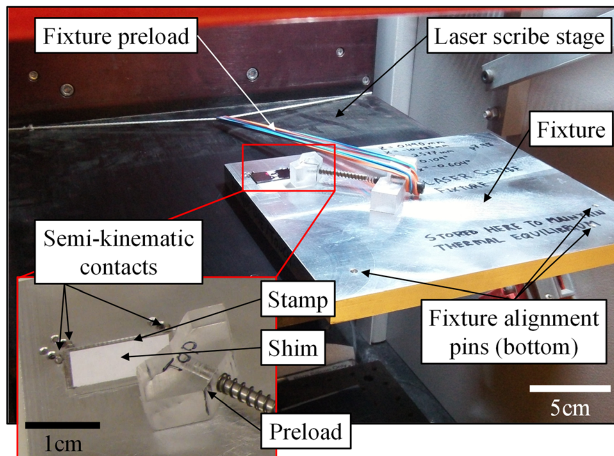


Fig. 8 Glass stamp in laser scribe fixture, which is used to align the gage patterning to the coordinate frame defined by the edges of the stamp

distilled water is sufficient to remove the hairspray, and part of the secondary built-up edge (BUE) deposited onto the silicon surface during the cutting, as shown in Fig. 10. The remainder of the secondary BUE above heat damaged hairspray is removed via an acetone soak.

5.3 Etching. The primary BUE and laser induced crack damage is removed from the silicon surface in the etching step. Two etches are used; a hexane etch of the wax and a nitric/hydrofluoric etch of the silicon. The wax etch (150 s in hexane) removes any wax that was melted and ejected from the cut during the patterning step. This undercuts the wax holding the silicon tiling, allowing these pieces to be removed with soap and water. These pieces fall off leaving the silicon piezoresistors behind on the stamp, as shown in Fig. 11. The kinematic contact surfaces on the side of the stamp are covered in MWM100 to protect them from the silicon etchant which is used next.

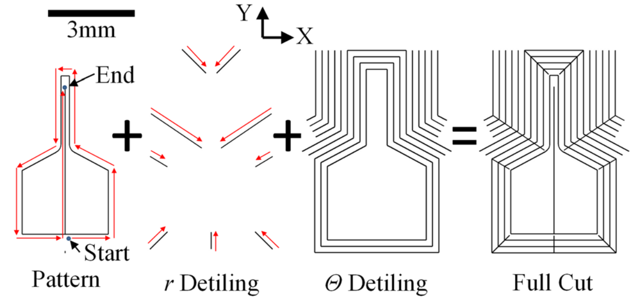
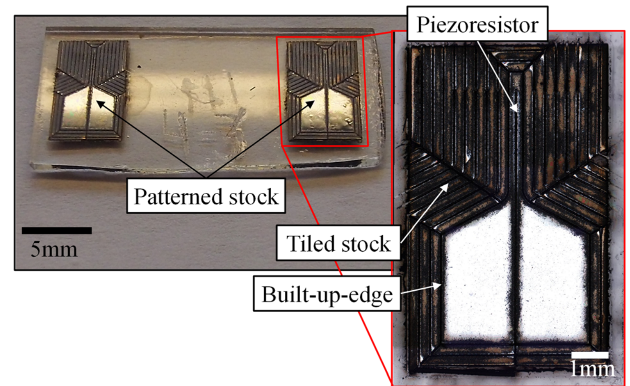


Fig. 9 Silicon cutting pattern, composed of three layers: (i) the piezoresistor shape, cut first, then (ii) the radial detiling lines cut to reduce thermal stresses, and finally (iii) the theta detiling lines cut to break the unwanted silicon into removable pieces



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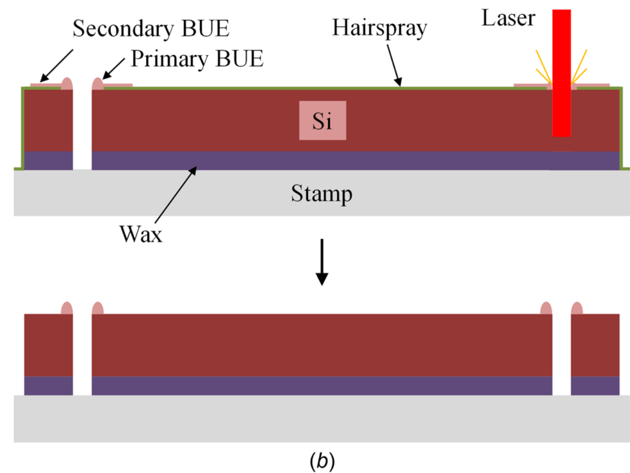

(*b*)

Fig. 10 (a) Stamp with cleaned piezoresistors, showing the removal of BUE. (b) Schematic of stamp at completion of patterning step. The silicon stock has been laser cut into the shape of the piezoresistor. This generates both primary and secondary BUE. The secondary BUE is removed upon washing off the hairspray layer, as shown in the bottom figure.

The stamp is submerged in a 100 mL silicon etching solution composed of nine parts nitric acid (69%) to 1 part hydrofluoric acid (49%) ratio by volume. This removes 20 μm of silicon at an average rate of 2.4 μm/min without agitation [37]. The surfaces of the stamp and piezoresistors are cleaned with soap and water to remove all contaminants left over from the etching step. This results in a stamp as shown in Fig. 12.

The primary BUE and all visible laser induced damage are removed during this process. This raises the uniaxial fracture strain of the piezoresistors from a measured value of 180 $\mu\varepsilon$ to

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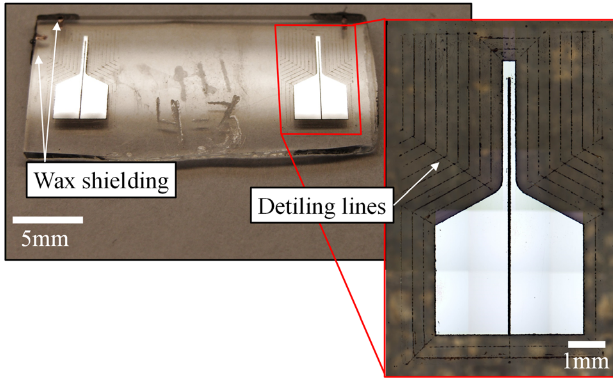

Fig. 11 Cleaned and detailed stamp prepared for etching

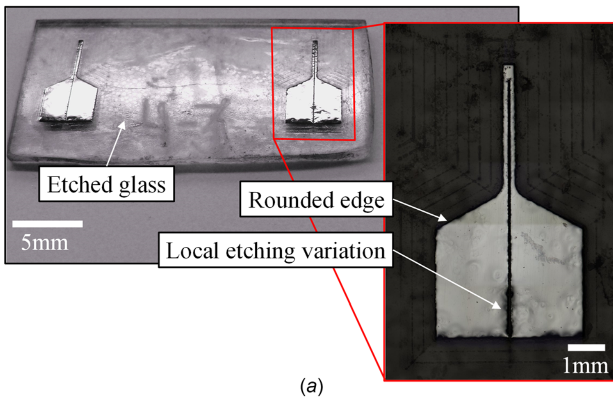

Fig. 12 (*a*) Etched and cleaned stamp prepared for the transfer step. (*b*) Schematic of stamp at completion of etching step. The patterned silicon is under-etched with hexane, which aids the removal of the unwanted silicon. This under-etched silicon is then chemically etched to remove the laser damage and fillet the corners.

about 2500 $\mu\varepsilon$. This is due to the etch removing the high-stress heat affected zone (HAZ) and rounding out the sharp stress concentrating corners as shown in Fig. 13. The details of the etch parameters are found in Ref. [37].

5.4 Transfer. The piezoresistive sensors are prepared and attached to the mechanical substrate in the transfer step. The stamp is placed back on a hotplate at 130 °C for 20 min to wick the wax back under the piezoresistors, as it has been under-etched by the earlier silicon etch. This reforms the adhesion layer to be able to evenly distribute the high pressure of the epoxy cure (240 kPa). The stamp surface is shielded from adhesion to the epoxy by a thin layer of molybdenum disulfide (MDS) from McMaster (Ontario, ON, Canada), as shown in Fig. 14. MDS is a dry lubricant which can be obtained in spray form.

The transfer process is carried out with a fixture to ensure proper alignment. Epoxy is placed on the piezoresistor surface as well as their eventual contact location on the mechanical structure. Vishay (Raleigh, NC) M-Bond 600 epoxy is used for its low cure temperature (>75 °C), which provides greater flexibility in material and process parameter selection. The epoxy is air dried

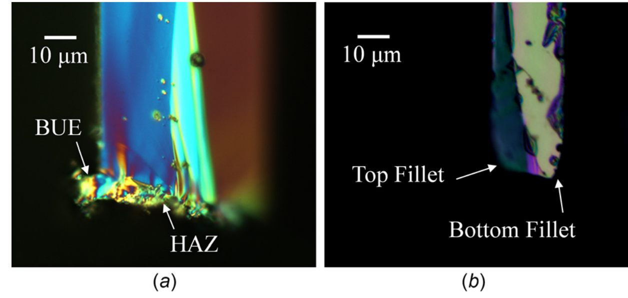

Fig. 13 Effect of etching on the laser cut edges of the thin silicon wafer. The wafer edge is shown before the etching in (*a*), with the BUE and heat affected zone indicated for clarity. The wafer is etched by about 25 μm, resulting in the profile shown in (*b*), showing significant filleting of the top corner, and less of the bottom corner.

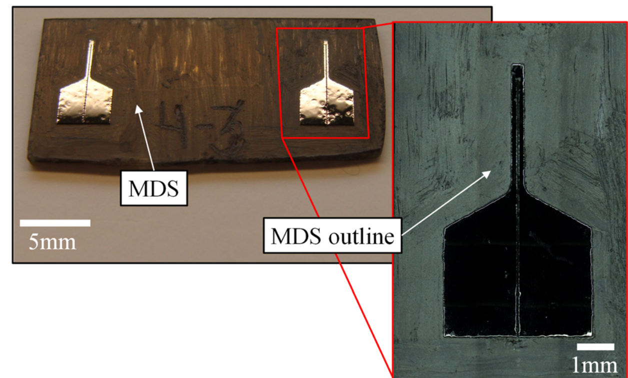

Fig. 14 Stamp prepared for transfer to the device

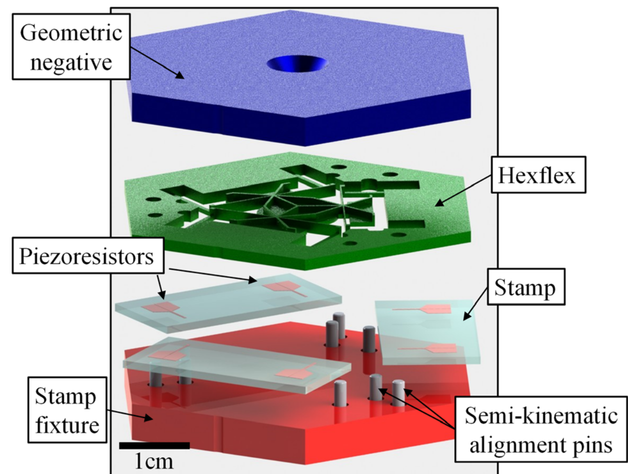

Fig. 15 Exploded view of transfer fixture setup, showing main components in the stack. The alignment pins are within the perimeter of the Hexflex so that the stamps can be pressed toward the center to preload.

for about 10 min, and then the surfaces are pressed together in the transfer fixture, with components as shown in Fig. 15, at 240 kPa to ensure an even glue line of about $9 \pm 2\,\mu$m. The cure is carried out at 150 °C for 45 min, with a 5 °C/min ramp. The alignment is ensured with a semikinematic fixture that holds the stamps and Hexflex mechanical structure. The geometric negative is a flat plate machined with the inverse geometry of the Hexflex, which ensures that the compressive preload is evenly distributed over the

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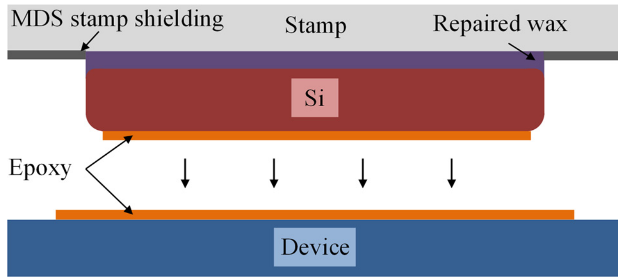

Fig. 16 Schematic of transfer step, showing the filleted silicon piezoresistors with repaired wax adhesion layer being transferred to the device surface. The stamp surface is covered with MDS to prevent epoxy adhesion to the stamp.

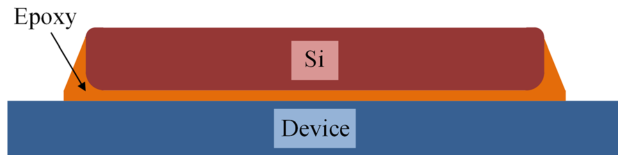

Fig. 17 Schematic of delamination step, showing the piezoresistor cured to the device surface after the stamp is removed and the adhesive wax is cleaned off from the surface

back of the Hexflex. The transfer process, fixture, and preload mechanism details are described in Ref. [37].

The transfer step is shown schematically in Fig. 16, with the repaired wax anchoring, the MDS stamp shielding, and the epoxy transfer operation. The patterned silicon is moved from the stamp to the final location on the mechanical structure and cured in place. This is all done using semikinematic alignment to ensure controlled gage placement.

5.5 Delamination. The stamp is removed from the cured piezoresistors in the delamination step. The device and attached stamp are heated on a hotplate to approximately 90 °C, which is sufficient to liquefy the wax anchoring the piezoresistors to the stamp. The stamp is gently peeled off, leaving the exposed piezoresistors attached to the mechanical structure, as shown in Fig. 6 and schematically in Fig. 17. The piezoresistor surface is cleaned with hexane and soapy water [37].

5.6 Scaling. The steps composing thin film patterning and transfer (except the etching step) are largely serial. Stock placement, detiling, stamp cleaning, stamp shielding, and transfer all require fine control of delicate structures. This process could be made more robust with more automated handling and computer vision. A more extensive acetone soak to clean the patterned gage in conjunction with correctly tuned laser detiling and ultrasonication may prove effective at replacing many of the manual steps required for this process, thus simplifying the automation.

6 Circuit Bonding

The circuit bonding step covers the attachment of the sensors to the deposited electrical structures. This research focused on the use of tabletop indium soldering [38]. The requirements of high flexibility, small batch size, and low per-device cost led to the development of a combined indium soldering and conductive epoxy operation for generating contacts to the silicon. These soldered contacts require little preparation time ($\approx$1 h) and are produced at low cost ($10). The completed device with sensor circuitry bonded to surface electrical features is shown in Fig. 18.

Electrical contacts are formed to the silicon piezoresistors in the metal-semiconductor contact step. The immobilized structure is placed on a hotplate to raise the surface temperature of the mechanical structure to $\approx$150 °C. A soldering iron set to 290 °C is wetted in pure indium and touched off against the contact pads of the piezoresistors, leaving behind indium contacts whose performance is described in Ref. [38]. Chemtronic (Kennesaw, GA) Circuitworks CW2400 two part epoxy is used to link the soldered contact pads to the electrical traces deposited onto the surface of the mechanical structure. The applied epoxy is cured at 65 °C for 10 min. Finally, a protective coat of Gagekote #8 from Vishay (Raleigh, NC) is applied to the surface electrical structures, including the piezoresistors. This coating aids in strain transfer to the piezoresistor, prevents damage to the structures, and reduces noise at the sensor and resists delamination. Further details of the circuit bonding process are found in Ref. [37].

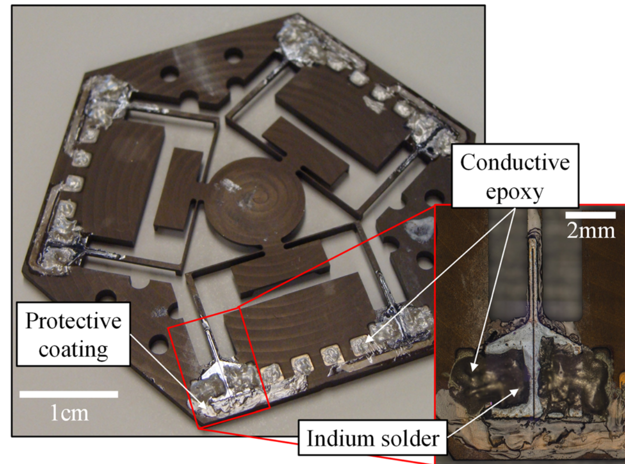

Fig. 18 Device with piezoresistors integrated into the surface electrical structures via the circuit bonding process

6.1 Scaling. While hand soldering was used during initial development, the metal-semiconductor contact process could be adjusted to increase the fabrication scale. These pads could be defined and formed earlier in the process of TFPT if the contact pad location is known. Metal film deposition onto the silicon stock would enable contact to be made without direct soldering. Local doping could also be carried out to suppress the Schottky barrier at the contact pads. The metal film deposition would generally require typical photolithographic processes which are associated with decreased flexibility but increased scale.

Precision dispersion and handling systems could be used to automate the epoxy and acrylic handling. Further metal deposition or aerosol jet printing could also be used in place of conductive epoxy for a more parallelizable process. Finally, the protective coat is not a high precision operation and could be sprayed over the sensors and electrical structure without covering the electrical contact pads.

7 Process Validation

7.1 Device. A Hexflex nanopositioning stage was fabricated to demonstrate the capabilities of the NLBM process. This device is shown in detail in Fig. 19 below. The underside of the device is shown for added detail, as this side shows the ribbing and other structures. The top side (+Z) is planar to facilitate the deposition of traces and sensors. Wire flexures of equal width and thickness (600 μm) are used to allow both in- and out-of-plane motion of the stage. The blade flexures are of reduced thickness (150 μm) but larger z-axis width (1.5 mm) to offer little stiffness to motion of the stage along the wire flexure axis while not deflecting during out-of-plane motion. Nearly all out-of-plane motion then occurs in the wire flexures which have the integrated strain sensors,

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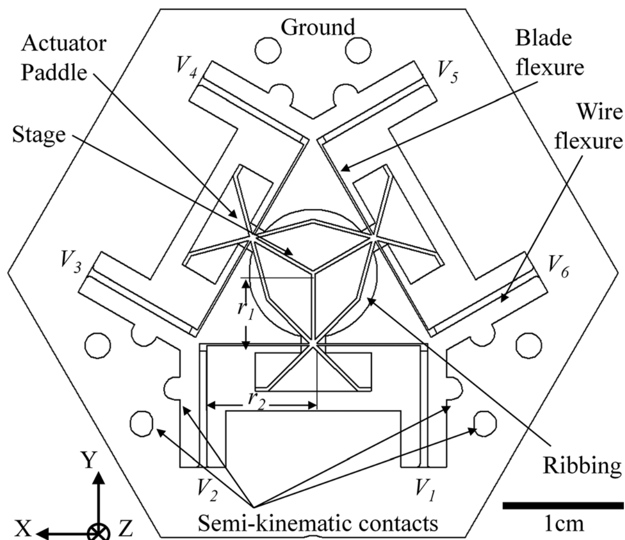

Fig. 19 Diagram of the Hexflex nanopositioner structure from the underside. The main components are identified including the flexure bearings, actuator paddles and center stage, rigidified with ribbing. Semikinematic contacts are located in four of the twelve holes piercing the structure.

labeled $V_{1\text{–}6}$. Each piezoresistor is placed to one side of the in-plane bending neutral axis of the wire flexure to read in-plane motion. The sets of gages (1–2, 3–4, and 5–6) are placed on opposite sides of the neutral plane. Out-of-plane motion generates equal signals from both sensors in the set, while in-plane motion then generates opposing signals. This allows for the motions to be mathematically distinguished from one another at the voltage end.

Actuator paddles are located with triangular symmetry for the placement of actuator magnets. Three force-based dual-axis Lorentz coil actuators can be used to drive the stage motion [2,41,43]. Ribbing is used to link these paddles to the center stage in order to resist the drumhead vibration of the stage and high mass paddles typical of fully planar Hexflex designs [2]. The center stage is ≈1 cm diameter and is intended to carry a nanometrology/manufacturing payload.

The sensor integration is carried out with TFPT using a 50 μm (110) p-type silicon wafer with 2.8×10^{17}cm^{-3} doping. The gages were further annealed at 20 V to stabilize performance and reduce barrier noise/resistance. Six low noise Wheatstone bridge circuits [40] were linked to the six integrated piezoresistors in the device. The gain on each bridge was set to 12 as determined by the maximal utilization of the Analog-to-Digital onverter (ADC) voltage range [40]. Low noise metal film resistors were used to complete and balance the quarter bridges [58,59]. The Hexflex was seated in a holder for mechanical anchoring as well as alignment of the electrical spring-pin contacts and potential actuation coils. The finished device seated in the holder is shown in Fig. 20.

7.2 Fabrication Results. The fabrication process was found to produce all structures within the desired limits. The sensor location is the most crucial parameter of the NLBM process, as the sensor is 50 μm from the edge of the flexure and must not significantly overshoot this edge. The scale of the errors occurring in this alignment is tabulated in Table 2. The ≈2 standard deviation 95% error is listed for each source and this is geometrically summed to find the net error of about ±27 μm for the NLBM process.

The transfer process for TPFT showed approximately ±3 μm repeatability precure. The dominant error source is from the curing process, where the heated epoxy and wax films pull the sensors off alignment. The main error was observed to occur in the asymmetric coating of epoxy onto the thin piezoresistor arms. The

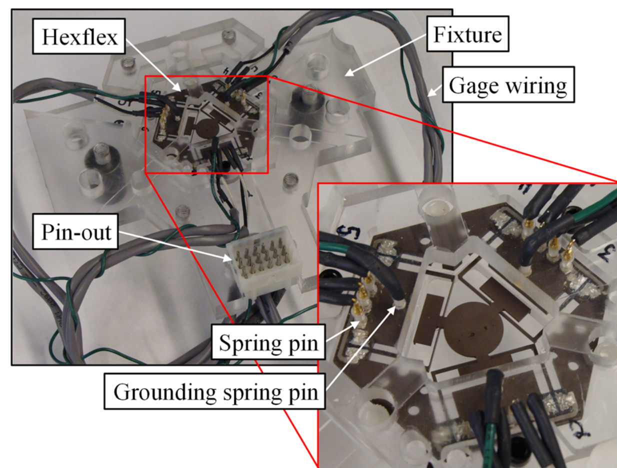

Fig. 20 Hexflex device in testing fixture, with electrical connections to the surface deposited traces

Table 2 Sensor integration error budget

Source	Error (±μm) 95%
Micromilling	3
Micromill tooling	4
Pattern calibration	6
Laser and fixture	6
Repair	4
Transfer fixture	3
Cure	25
Sum	27

epoxy is compressed during the transfer and ends up largely on one side of the piezoresistor arms. This generates a slight transverse force on the gage, with reduced effect along the axis of the gage. The error standard deviation was observed to be ≈5 μm for evenly coated sensors but rose to ≈30 μm when the epoxy was coated onto the gage unevenly. The asymmetrical epoxy placement is an artifact of the manual application and is thus not fundamental to the system. Improved epoxy placement via automated systems or masking operations would minimize this effect and is expected to reduce the curing error to ≈5 μm, and thus the whole error to ≈12 μm 95%.

The net fabrication parameters for the main component are listed in Table 3. This shows the capability of the NLBM process in terms of feature fabrication control and alignment. The characteristic error is broken into two terms, the average error and the 95% variation in this error. The values were measured over multiple locations on the device as all the structures occur in six fold symmetry. These two parameters give an insight into the scale of the process errors both repeatable and nonrepeatable.

The sensor location is described in detail previously. It was desired to keep the sensor 50 μm from the edge of the flexure. An average value of 65 μm was observed for this, well within acceptable values. This alignment is a function of many steps as

Table 3 NLBM process error

Component	Desired (μm)	Error ± 95% (μm)
Sensor X location	50	15 ± 27
Piezoresistor arm width	150	3 ± 5
Wire flexure width	600	0 ± 4
Blade flexure width	150	6 ± 4
Trace width	800	−55 ± 80
Trace location	1000	30 ± 30

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Table 4 Process times and costs

Main step	Substep	Man-hours (h)	Total time (h)	Marginal equipment and material cost ($)
Bulk micromachining	Micromilling	3	5	200
Surface micromachining	Insulation	1	50	<10
Surface micromachining	Deposition	4	4	200
Sensor integration	Stock forming	0.5	0.5	<10
Sensor integration	Lamination	1.5	2.5	<10
Sensor integration	Prepatterning stamp prep	0.5	0.5	<10
Sensor integration	Patterning	1.25	1.25	50
Sensor integration	Pre-etching stamp prep	1.5	1.5	<10
Sensor integration	Etching	1	1	<10
Sensor integration	Pretransfer stamp prep	2.5	3	<10
Sensor integration	Transfer	1.5	7.5	<10
Sensor integration	Delamination	1	1	<10
Circuit bonding	metal-semiconductor contact	1	1	<10
Circuit bonding	Circuit completion	1	1	<10
Circuit bonding	Protective coating	0.5	1	<10
	Total	21.75	80.75	450–580

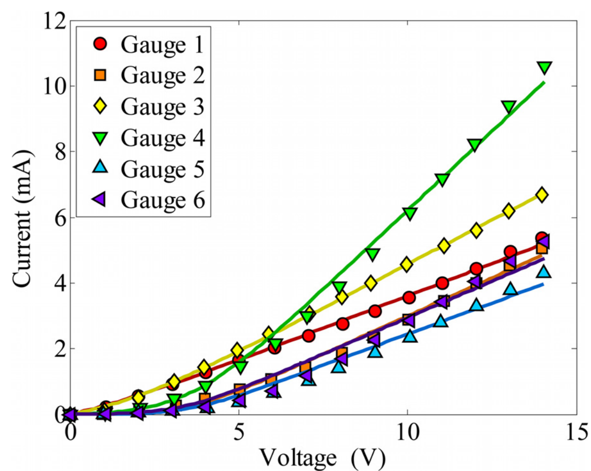

Fig. 21 I–V characteristics of the six piezoresistive sensors on the Hexflex

described above. The piezoresistor arms are accurately captured due to the repeatability of the laser patterning and chemical etch. The wire and blade flexure widths are produced by the micromill which has 3 μm cutting accuracy. The excess error is likely due to substrate flexing during machining. The trace width and location are functions of the mechanical shadow mask used to pattern the deposited traces. The finite thickness of this mask combined with a slightly off-axis material source to generate a sine-error reduction in trace width, which also shifted the trace center location. This can be resolved with thinner shadow mask structures or more normal alignment to the source. The parameters listed above show that NLBM holds the potential to be used for fabricating a range of meso-/microscale devices with micron-scale accuracies.

The estimated time and materials cost to produce a device via the NLBM process are shown in Table 4 below and described in more detail in Ref. [37].

7.3 I–V Characteristics. The current–voltage performance of the integrated piezoresistive sensors were measured using a four-point probe setup and are shown for comparison in Fig. 21. The I–V curves show the expected diode behavior of an exponentially decaying resistance in series with an ohmic resistor.

The overall I–V parameters for the gages are listed in Table 5, along with the standard deviations on the average values. The predicted values are drawn from models generated in previous work on semiconductor piezoresistor design [38,39]. The bonding parameter, β, describes the variation of the ohmic resistivity from a baseline best-case term associated with ideal operating conditions [38].

Table 5 I–V parameters

	β		Ohmic R (kΩ)		V_{b0} (V)	
Gage	Predicted	Measured	Predicted	Measured	Predicted	Measured
1	1.4	1.5	2.5	1.4	0.83	12
2	1.4	12	2.2	1.8	3.5	5.1
3	1.4	2.1	1.9	1.9	1.5	1.2
4	1.4	5.8	1.0	0.88	3.6	4.7
5	1.4	16	2.6	2.0	3.6	5.3
6	1.4	9.6	2.3	1.6	3.4	5.4
Average	1.4	7.8 ± 5.7	2.1 ± 0.6	1.6 ± 0.4	2.7 ± 1.2	5.5 ± 3.2

Gage 4 shows a reduced ohmic resistance compared to the other five gages. This is due to incomplete cut through the silicon during the patterning step. This effect was found to be correlated with starting up, so could usually be mitigated by carrying out several warm-up passes. Gages 1 and 3 show similar I–V, noise, and gage factor characteristics to the rest of the gages, but with a significantly reduced diode offset at low voltages. This is consistent with a shunt resistance in parallel to the gage, passing through a gap or scratch in the oxide insulation.

7.4 Noise Characteristics. The noise characteristics of the piezoresistors were measured by placing the device within a Faraday cage and measuring its output with a 50 kHz National Instruments (Austin, TX USA) NI9239 ADC. The power spectral densities are shown for comparison in Fig. 22.

The noise shows the expected 1/f-like performance, dominated by the Schottky barrier flicker noise. The observed average Hooge constant values and scaling factors are shown in Table 6, along with the bonding parameter which indicates the bond quality and the standard deviations on the average values. This is a slightly above to the expected value of 0.26 or $10^{-0.59}$ [39], likely due to the same surface contamination which raised the bonding parameter. The average frequency scaling term, δ, lies slightly above the expected value of 0.18 [39]. The increased slope of the flicker noise would suggest the increasing contribution of new physical phenomena such as diffusion processes, or the generation of mechanical defects due to damage from the fabrication process [60]. Little correlation is observed between the bonding parameter and noise constants.

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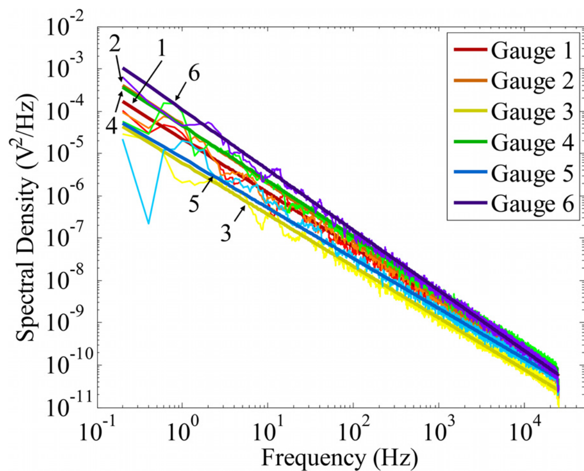

Fig. 22 Noise characteristics of the six piezoresistive sensors on the Hexflex. The different gages best fit lines are labeled for identification.

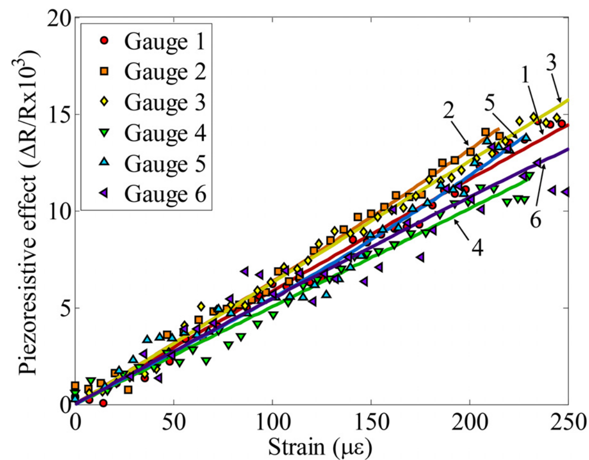

Fig. 23 Out-of-plane gage factor characteristics of the piezoresistive sensors on the Hexflex. The different gages best fit lines are labeled for identification.

Table 6 Noise parameters

Gage	β	$\log(\alpha_{sb})$	δ
1	1.5	0.35	0.27
2	12	0.18	0.36
3	2.1	−0.45	0.22
4	5.8	0.49	0.31
5	16	−0.67	0.19
6	9.6	0.52	0.42
Avg.	7.8 ± 5.7	0.073 ± 0.509	0.29 ± 0.09

7.5 Gage Factors. The gage factors of the piezoresistors were measured by enforcing stage displacements with an Instron (Norwood, MA) 5869 Test Frame. The frame used a Solartron (West Sussex, UK) ACR15 LVDT with 100 nm resolution to drive the stage while simultaneously measuring the sensor outputs. The stage was driven along its Z axis, normal to the plane of the device, to measure the out-of-plane sensitivity of the piezoresistors. The setup for doing so is shown in Ref. [37].

The performance was measured over a few hundred microstrain to capture the small signal gage factor behavior the focus of this work. The measured displacement, δ, is translated into effective strain, ε_{eff}, via the flexure force to strain gain, ε_F, and strain geometry gain G_{SG}, while the measured voltage output from the bridge V is translated into fractional resistance change $\Delta R/R$ via the bridge strain type, N_ε, source voltage V_S, span temperature compensation gain G_{STC}, and amplifier gain G [40], as was done in Ref. [39]

$$\overbrace{(\delta\varepsilon_F G_{SG})}^{\varepsilon_{\text{eff}}} G_F = \overbrace{\left(\frac{V}{N_\varepsilon V_S G_{\text{STC}} G}\right)}^{\Delta R/R} \tag{1}$$

Both the in- and out-of-plane gage factor can be accounted for in Eq. (1) through the adjustment of the strain geometry gain as described in Ref. [37]. The out-of-plane strain geometry term is approximately 0.84, while the in-plane term is approximately 0.28 [37,40]. The dynamic range of the in-plane sensing should then be about 33% (−10 dB) of the out-of-plane sensing. The strain versus resistance relations for the piezoresistors are shown in Fig. 23 for out-of-plane sensing and Fig. 24 for in-of-plane sensing. The errors due to measurement (Linear Variable Differential Transformer LVDT and ADC) are captured in the scale of the data points.

The in- and out-of-plane gage factors show similar trends, which is expected given that both motions are driving the piezoresistor in the same fashion.

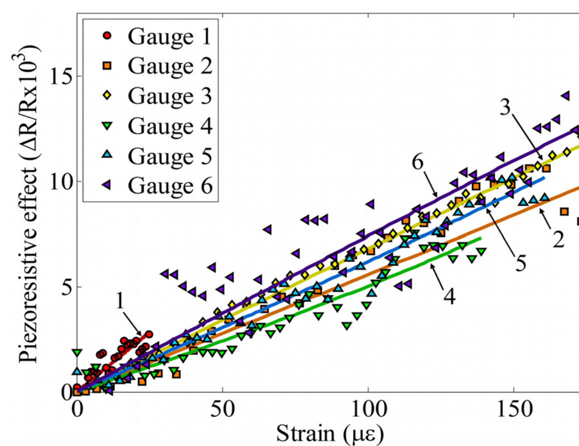

Fig. 24 In-plane gage factor characteristics of the piezoresistive sensors on the Hexflex

The gage factor for each device was determined by fitting a linear position-voltage coefficient and a third-order nonlinear term to the data [39]. The piezoresistors are designed to have a gage factor of 127 in both axes. The measured gage factors are normalized to the intrinsic gage factor (GF) of the silicon, $G_{F0} = 167$, at the device doping level via the ratio $r_{\text{GF}} = G_F/G_{F0}$ to capture the attenuation of the gage factor. Both the gage factors and their associated ratios are shown in Table 7 for comparison between the gages.

Both the in- and out-of-plane models are found to over predict the gage factor ratio by an average of 11%. The error in the gage factor model prediction may be due to a range of sources. Primarily, the error is occurring for gages 1 and 3, where the I–V model incorrectly predicts a significantly higher gage factor due to the low β. This is consistent with the oxide shunt resistance model proposed earlier, which would mitigate the effect of the barrier resistance without improving the gage factor. Absent gages 1 and 3 the average in- and out-of-plane model error is 1% and 3%, respectively, so the models appear to be capturing the dominant gage factor attenuation effects. Several sources are suggested to account for the slight underprediction, including: (i) wafer flat misalignment, (ii) gage misalignment, (iii) flexure fillets strain attenuation, (iv) Schottky barrier piezoresistance [61], (v) test fixture compliance, and (vi) gage factor nonlinearity coupled with thermal preload, all described in more detail in Ref. [37].

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Table 7 Measured gage factors

Gage	Predicted		Out-of-plane			In-plane		
			Measured		Model error	Measured		Model error
	GF	r_{GF} (%)	GF	r_{GF} (%)	Δr_{GF} (%)	GF	r_{GF} (%)	Δr_{GF} (%)
1	130	78	59	35	43	113	68	10
2	62	37	63	38	−1	55	33	4
3	115	69	63	38	31	68	41	28
4	52	31	50	30	1	48	29	3
5	59	35	53	32	3	61	36	−1
6	71	42	55	33	9	75	45	−2
Avg.	81	49	57	34	15	70	42	7

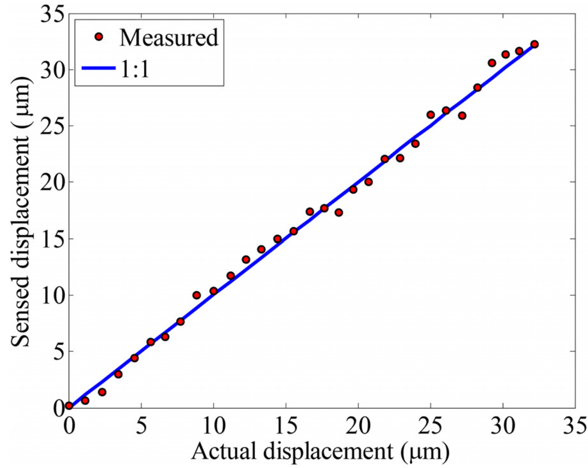

Fig. 25 Motion sensing capability of the integrated sensing demonstrated for the out-of-plane linear displacement trajectory. The 1:1 correct reading is shown with the solid line.

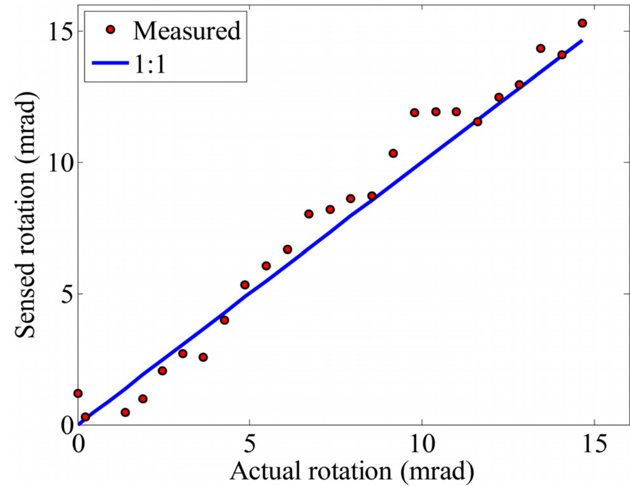

Fig. 26 Motion tracking capability of the integrated sensing demonstrated for the in-plane rotary displacement trajectory. The 1:1 correct reading is shown with the solid line.

7.6 Motion Sensing. The positioning capability of the device can be studied by comparing the known stage location to the sensor indicated stage location after calibration. This is done using the measurements of the gage factor. A known displacement was enforced on the device, and the gage responses measured. In the first case, the center stage is translated out-of-plane. In the second case, the center state is rotated around an out-of-plane axis. The sensor responses were measured to determine performance. The sensed displacement for each sensor is then combined via a calibration matrix described in Ref. [37]. Both tests subject all the gages to equal displacements. The errors due to measurement (LVDT and ADC) are captured in the scale of the data points (Fig. 25).

The sensors are shown to provide accurate sensing over the range of motion studied in this test, with root-mean-square (RMS) error of 0.70 μm. The flicker noise on the sensors is attenuated by about 2.5× via the six sensor averaging, as captured in **M** [40]. The sensed and known positions are compared for the in-plane case in Fig. 26, which shows the same trends as the out-of-plane case, just with a proportionally larger RMS error of 0.88 mrad, due to the lower strain sensitivity.

The gage factor and dominant noise characteristics of the sensors allow for a measurement of the sensing dynamic range, calculated for a system with 1 kHz stage bandwidth and 10 kHz sensing bandwidth. The integrated sensing is designed to have a resolution of 69 dB dynamic range out-of-plane, and 59 dB in-plane over a 10 kHz sensor bandwidth. The measured dynamic range is 52 dB out-of-plane and 41 dB in-plane, corresponding to an approximate range of 320 μm out-of-plane/290 μm in-plane, and a resolution of 0.79 μm out-of-plane/2.5 μm in-plane. The reduction in performance is likely due to several factors including the low substrate temperature during indium soldering which raised β from 1.2 to about 7.8, contamination which raised both the noise and β, and variation in gage placement affecting the strain sensitivity of the gages. These issues could be fixed with several changes including: (i) more consistent and higher heating, (ii) reduced surface contamination, and (iii) improved gage placement accuracy [39]. These changes can potentially drive the bonding parameter back toward unity, the noise down to values observed in earlier work [39], and raise the sensitivity of the in-plane sensing. Additional significant performance improvements (>60 dB) can be accessed via raising the bridge source voltage from 10 V to 20 V and doping the gage bond-pads via spray on dopants [62] or electrical discharge doping [63], as has been discussed in Ref. [39]. The cumulative performance boost of these suggested changes is predicted via previously developed models [39,40] to push the dynamic range up to about 132 dB, corresponding to a resolution below 1 nm in both axes.

8 Conclusion

The purpose of this work is to generate a process flow which can be used to fabricate metal MEMS with integrated sensing, and do so flexibly, in small batches, with low perdevice cost. The process can produce new designs in ≈1 week at an average unit cost of <$1 k/device even at batch sizes of ≈1–10, with expected sensing performance limits of about 132 dB over a 10 kHz sensor bandwidth. This is a ≈20× reduction in cost, ≈25× reduction in time, and potentially >30× increase in sensing dynamic range over comparable state-of-the-art compliant nanopositioners. The

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NLBM process was used to create a low-cost customizable nano-positioning architecture that is feasible for use in a range of micro-/nano- manufacturing and metrology operations. The customizable architecture will help surmount one of the significant hurdles of nanomanufacturing research and development.

A Hexflex 6DOF nanopositioner with titanium flexures and integrated silicon piezoresistive sensing was fabricated using NLBM. The process was shown to enable alignment of device components on the scale of 10s of microns. 150 μm piezoresistor arm widths were demonstrated, with suggestions made for how to reach the expected lower bound of 25 μm. Flexures of 150 μm and 600 μm were demonstrated on the mechanical structure, with a lower bound of $\approx$50 μm expected for the process. Electrical traces of 800 μm width were used to ensure low resistance, with a lower bound of $\approx$100 μm expected for the process.

The integrated piezoresistive sensing was designed to have a gage factor of about 125 but was reduced to about 70 due to lower substrate temperatures during soldering, all as predicted by design theory [38]. The sensors were measured to have a dynamic range of 52 dB over a 10 kHz sensor bandwidth, limited by the Schottky barrier noise. Several suggestions were proposed for boosting the performance to $\approx$132 dB over a 10 kHz sensor bandwidth, including raising the bridge voltage to 20 V and doping the contact pads through either spray on dopants or electrical discharge doping. These improvements will all increase the benefits of NLBM, enabling a wider range of MEMS devices to be produced quickly, in small batches and at low cost.

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