CIRCUIT DESIGN FOR
1–10 MHZ DC-DC CONVERSION

by

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ABSTRACT

In the 1–10 MHz range the energy storage elements in a dc-dc converter become small enough to permit hybrid fabrication and automated assembly. This facilitates the assembly of very high density power converters. Unfortunately, the parasitic energy storage elements that occur in the components and their interconnections are a major obstacle to operating efficiently at these elevated frequencies. This thesis, which is part of an MIT project to develop miniature supplies and advanced conversion techniques, shows that the detailed effects of these parasitics on the converter topology can be understood, and, in many cases, overcome.

After examining two topological families (the square-wave converter and the quasi-resonant converter) the thesis describes a resonant forward converter that has features in common with both. The development of a prototype point-of-load converter using this topology is then presented. An experimental 50 W, 40 V to 8 V converter, constructed with standard components and assembly techniques, achieves a power conversion density without a heatsink of 70 W/in³ and an operating efficiency of 83%. A hybrid assembly of a 40 V to 5 V version of the same circuit on a copper thick film substrate achieves 106 W/in³ conversion density and 85% efficiency.

Despite using unpackaged components, the high frequency converter is still limited by the effect of unwanted parasitics. These parasitics are worse than they have to be because the components have been developed for general purpose use, rather than optimized for a specific application. Specialized component work that was motivated by the prototype development is therefore discussed, with the focus on specialized controller/driver I.C.s that were developed for the prototype converter. Results from this work demonstrate that CMOS is a viable technology for high frequency controller/drivers, both in terms of power dissipation and operating speed.

Thesis Supervisor: Dr. Martin F. Schlecht
Title: Associate Professor of Electrical Engineering
Acknowledgements

As I approach the end of my M.I.T. experience I would like to take this opportunity to reflect on the different people that have played a part in my development, and acknowledge their contribution to this thesis, to my engineering skills, and to my character. I would like to begin by thanking my thesis adviser, Professor Marty Schlecht, for his help and guidance, both in my Doctoral program and in supervising the research for this thesis, and also for his friendship throughout my graduate studies. I would also like to thank my thesis committee, Professors John G. Kassakian, Hae-Seung (Harry) Lee, and James K. Roberge, for their advice and help with the thesis.

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My spiritual home at M.I.T. has been the Lab, which was EPSEL and is now called LEES. In EPSEL I found friends, role models, and colleagues, among both staff and students. In my early years my seniors, and mentors, among the graduate students were Marty Schlecht, Tom Warner and Paul Basore. The most important thing I learned from them was to show an interest in others’ work and to share one's skills. My peers and close friends were Andy Goldberg and Gary Fedder, and more recently, Clem Karl and Seth Sanders. The young fellas, friends and colleagues, were, and are: Barry Cuipepper, Gerrardo Molina, Brett Miwa, Loveday Mweene, Tom Major, John Ofori, Len Fitzelle, Dan McCarthy, and Karen Walrath. In the tradition of Lab members supporting each other, Karen deserves special acknowledgement for her help with computer simulation tools, right up to the end.
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At M.I.T. I spent a lot of time and energy playing, coaching, and teaching rugby. It took a lot of my time, but it also kept me sane, and provided a link to my New Zealand roots. Much like the Lab, the rugby team is a very supportive organization, looking out for the youngsters, and bringing them along, both in their play on the field and in their lives off. The club also functions as a broad support system, providing friends and contacts all over the Institute. My peers on the team, over the years, included John Polcari, Tony Eastland, Jeff Anderson, George Walrond, Chris Kedzie, Matt Tobin, Reg Gott, Joe Goss, Mike Murphy, Bruce Johnson, George Kraynak, Tienie Van Schoor, and Brian Tarras. All these guys are good friends, and they all put an effort into helping the younger guys develop. I would especially like to thank Tienie, for his help in completing the preparation of this document. Another friend, the patriarch of the M.I.T.R.F.C., is Jim Culliton. His involvement gives stability and continuity to the club, not to mention providing a summer training camp location at Oak Bluffs on the Vineyard. Things get a bit crazy with Joan Rice trying to organise a feed for 30 guys. Thanks, Jim and Joan. The younger generation, many of whom have now surpassed us older guys, include Joe Kwansowski, Barry Culpepper, Jens Legallet, John Suber, Inpachelvan (Chevy) Vithiananthan, T.J. Cradick, Tom Murray, Dan McCarthy, Marcos Esterman, and Evan (Elmo) Pratt. Many, many others have come and gone. I thank them all, and hope that the spirit and camaraderie of the team continues on long into the future. A special mention for that rolling stone, the boy from Kaikorange in the Bay of Islands (N.Z.), Richard Reneti. He helped me show the Yanks the Kiwi style of play. Cheers big Richard, te nakau hipa.

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Moving into the final stages of this monologue, it's time to think about home, Te Atatu, New Zealand. I gained a lot from my education at M.I.T., but I also lost
a lot in travelling so far away from family. I haven't been there, not for the deaths of Grandma and Grandad Casey, not for the births of my nieces Bree and Beth (and I left just after Jenna was born), not to see my younger siblings grow up. I haven't been a part of all of that, and I missed the rough times as well as the good, when my help and support was needed. So, to my immediate family, Mum, Dad, Mary, Katherine, Margaret, Richard, Patrick and Andrew, I would like to say I'm sorry. You are all a big part of my being here and I hope I have the chance to make some of what I owe up to you.

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Chapter 1

INTRODUCTION

This thesis describes contributions by the author to an on-going project at MIT, that addresses the development of the next generation of power electronic conversion and power supply distribution techniques. The specific focus of this thesis is on the development of 1–10 MHz dc-dc converters to be used for the supply and distribution of electrical energy within large electronic equipment, such as computers. In this application, today’s 10–100 kHz power supplies are inordinately large; they require expensive and bulky busswork to distribute the load current at the various low voltage levels, and they compromise the reliability of the overall system [1,2].

As an example of the present state of power conversion practice, consider the electronics of a personal computer, an IBM PC-XT, shown in Fig. 1.1. The power supply can be seen in the upper right region of the photograph. This is a 150 W supply which occupies 240 in³, therefore the power conversion density is approximately 0.65 W/in³, and the power supply occupies roughly 20% of the total system volume. When we look at the internal assembly of the supply, which is shown in Fig. 1.2, we see that the major contributions to the bulk are the large, individually packaged components which are distributed throughout the volume.

Contrast the supply of Fig. 1.2 with the converter module of Fig. 1.3. This is a 50 W dc-dc converter that occupies 0.5 in³, giving a power conversion density of 100 W/in³, which with the addition of a heat sink will still achieve 50 W/in³. The
Figure 1.1: Personal Computer Electronics

Figure 1.2: Computer Power Supply
converter, which was developed at MIT, operates at 5 MHz, and is an example of the next generation of power converter topologies and assembly techniques.

This particular converter has been developed as a point-of-load converter to be used in a distributed supply system [3,4]. In this system, the modules are physically distributed throughout a volume of electronics with energy supplied to each module from a loosely regulated distribution buss, as shown in Fig. 1.4. The energy is distributed to the modules at a voltage considerably higher than the load voltage (e.g. 40 V or 200 V). Each module regulates its own output voltage, monitors the power drawn by its load, and uses the same cooling system as the signal-processing electronics. This distributed system dramatically reduces the busswork, and the associated system packaging problems, when compared to the centralized power supply system it replaces.
1.1 Power Supply Technology

1.1.1 Present State

During the last two decades, steady advances in integrated circuit processing have allowed electronic circuit designers to incorporate more and more circuitry on a given chip, with the circuitry able to operate at progressively higher frequencies. The increasing level of integration has facilitated the assembly of more complex and powerful electronic systems, with higher reliability, but at the same time the power dissipated in a given volume of electronics has increased. Meanwhile, power conversion and distribution technology has remained relatively static, evolving slowly in response to changing demands. Power supply miniaturization efforts have been
completely outpaced by electronic circuit miniaturization. As a result, the power supply has become a major component of the volume and cost of the total electronic system.

As the volumetric power consumption of the electronic load has increased, the busswork needed to maintain regulated voltages within a given volume has also had to increase. However, the power distribution architecture has remained unchanged, with centralized supplies feeding extensive busswork. These centralized supplies impede the implementation of reliable, fault tolerant, systems since a single component failure in the supply tends to bring the entire system down.

Another feature of contemporary power supply practice is a proliferation of custom power supply designs. This proliferation has been encouraged by strong relationships between a converter's rating, size, and cost. The on-going duplication of engineering effort is in strong contrast to signal electronic design practice, where integration has allowed the circuit designer to operate at a much higher system level than before. Also, the lack of standardization in the converter designs, components, assembly techniques, cooling systems, and distribution busswork has deprived the industry of economies of scale.

1.1.2 Direction: Power Supply Miniaturization

The power conversion and distribution techniques in common practice are clearly due for a major overhaul, and this is imperative for the large electronic systems of the future as the move is made to lower-voltage logic supply standards (e.g. 3.3 V). This consideration has motivated a great deal of research in recent years on the development of miniature power supplies, with miniaturization being achieved by operating at higher switching frequencies because of the smaller energy storage elements that result. Miniaturization requires major improvements in the topologies, components, and construction techniques used in contemporary converter circuits, but the potential rewards are immense, as evidenced by the converter of Fig. 1.3. Ultimately, as each element of the solution is pushed to the limit, the conversion
density and efficiency should only be constrained by fundamental material limits. As practical converters approach these limits, it should encourage the stability and standardization that has been lacking in the power conversion business to date [5].

As important as the development of miniature converters is the need to develop power distribution architectures that utilize these converters in an intelligent fashion, such as the distributed supply system we outlined above. At the same time the converters must support the architectures, and must be of sufficiently high performance to help win acceptance by system designers of any new supply scheme. Actually, no element of the problem can be isolated; the distribution architecture, the converter topology, the circuit components, and the construction techniques must all be complementary, and so each of these elements must be considered when developing solutions.

1.2 Research Efforts

1.2.1 The MIT Program

A comprehensive program was initiated at MIT some four years ago to address the whole issue of high-frequency high-density power conversion. One important part of the program has been the development of specialized, semiconductor and energy storage components. Another contribution has been research into advanced construction techniques, particularly for hybrid assembly of power converters to achieve structural and thermal units that are compact, reliable, and cost effective. The endeavours in both of these areas have been motivated by the research on power conversion topologies that are discussed within this document.

1.2.2 Development of Miniature Supplies

At best, today’s 10–100 kHz supplies achieve power conversion densities of 3–5 W/in.$^3$. Research efforts have focused on achieving conversion densities of
50 W/in.\(^3\) by operating in the 1–10 MHz frequency range. As a converter's energy storage components become smaller due to this increase in frequency, the total converter volume begins to be dominated by packaging and heat sink volume. So, the obstacle to increasing the power conversion density is being able to simultaneously raise the frequency and maintain (or even improve) the overall efficiency.

Existing component technology permits efficient power conversion in the [4] 1–10 MHz range, but the topologies and assembly techniques commonly used do not. Energy storage components are available that are relatively lossless in this frequency range, and high-speed power semiconductor devices, such as power MOSFETs and Schottky diodes, are capable of very fast switching (even for a 100 ns switching period) since they are majority carrier devices and do not exhibit recovery phenomena.

The conversion efficiency is instead limited by the effect of reactive parasitics. These parasitic energy storage elements occur in the power, control, instrumentation, and drive components, as well as in the physical assembly and the distribution buss. They cause losses in proportion to the product of the energy they store and the switching frequency. As the energy stored in these parasitics becomes significant compared to the energy transferred each cycle, they increasingly dominate the converter's operation. Not only do they lower the efficiency, but they also contribute to load regulation, internal noise generation, and noise that is both radiated and conducted externally.

The different research efforts focused on developing miniature power supplies by the power electronic community over the last five years can be characterized as attempts to come to terms with the parasitic energy storage elements. In the 10–100 kHz switching frequency range, the power converter could be analyzed as a network of ideal lumped elements, with the parasitic reactances causing "second order" effects. In the 1–10 MHz range, however, the parasitics must be considered as explicit circuit elements and their effect on the circuit operation understood.

In most converters there are one, or possibly two, dominant parasitics that com-
promise the efficiency. Therefore, a common response has been to focus on these dominant parasitics in the development of high frequency converter topologies. In contrast, the approach pursued in this work has been to achieve a detailed understanding of the effects of all of the converter parasitics, and then to use this knowledge to advantage. For a particular topology, detailed knowledge of the loss mechanisms and component limitations can be used to motivate specific component and assembly optimizations, not only to increase the operating frequency or efficiency, but also to improve other performance characteristics such as the converter's dynamic response or the reduction of radiated noise. The detailed understanding can also be used to motivate new or modified topologies that not only accommodate the existing reactive parasitics but, wherever possible, use them.

1.3 Contributions of this Thesis

This thesis documents contributions to the development of high-frequency circuit topologies for the MIT high-density power supply project. Specifically, this work has achieved an understanding of the detailed operation of both high-frequency square-wave switching converters and quasi-resonant converters [6] so that analytic comparisons could be made between the two. The results were presented in [7]. It also developed a resonant forward converter topology to a prototype, high frequency, low volume, point-of-load power supply for a distributed power system. This work was presented in [8] and a hybrid assembly of this same circuit, which is the converter shown in Fig. 1.3, is to be presented in [9]. The experimental point-of-load supply motivated the development of specialized components for high-frequency power converters, which are described in [10-16]. One area of the component work, the development of specialized controller/driver integrated circuits, was an integral part of this thesis and will be presented in [17]. Ancilliary results, both of this and other research programs, are alternate power conversion topologies and modifications to basic topologies, that result from the detailed understanding of the interaction between topologies and component parasitics. Some of these modified
topologies are being actively pursued.

1.3.1 Thesis Contents

The organization of this document follows the order of the contributions listed above closely and is as follows. The next chapter presents the basic story that is developed in Chapters 3, 4, and 5, of how reactive parasitics limit converter performance, and how different topological options can overcome these limitations. Chapter 3 discusses square-wave switching techniques, particularly the effects of parasitics on high-frequency operation, and shows how to account for these effects rather than dismissing them. Chapter 4 focuses on resonant and quasi-resonant switching, again demonstrating that the effects of unwanted parasitics can be quantified. This chapter includes a quantitative comparison between the square-wave and quasi-resonant topologies, based on losses. The chapter concludes by discussing the performance of the quasi-resonant topology, in the form of a quasi-resonant flyback converter, the point-of-load supply application. Chapter 5 presents a Resonant Forward Converter (RFC) topology, contrasts its operation with the other topologies, and traces its development as a prototype point-of-load converter. This chapter concludes with the experimental results of the hybrid converter. Component and assembly developments motivated by the RFC topology are then presented in Chapter 6. Chapter 7 describes one of the specific component development projects: the development of integrated control and drive circuitry for the three power MOSFETs used in the point-of-load RFC converter. A collection of topological issues are discussed in Chapter 8 to demonstrate the type of ideas that a detailed understanding of the converters operation suggest. The document concludes by summarizing the contribution made by this work and making recommendations for future work in this field.
Chapter 2

Overview: Topologies and Frequency

A power circuit's size generally decreases with its switching frequency because of the smaller reactive components that result. Ultimately, however, the operating frequency of a particular converter topology is limited by losses that are proportional to the frequency. These losses are due to finite length switch transitions, parasitic reactances, and hysteretic behavior in magnetic and capacitive material. For today's square-wave power converters using power MOSFETs, Schottky diodes, ferrite cores and ceramic capacitors, interconnected with standard PCB techniques, 300–500 kHz appears to be the point at which these losses give unacceptable efficiencies. Furthermore, it is the presence of parasitic reactances that dominates this limit in frequency. As a consequence, power supply miniaturization efforts have become focused on the development of topologies (specifically resonant dc-dc converters) that can reach into the 1–10 MHz range by accommodating these parasitics. This high-frequency work has been very beneficial, even for our understanding of square-wave conversion, by focusing attention on the details of how parasitic reactances influence the converter's operation.

Unfortunately, the pursuit of very high operating frequency seems to have become a goal in itself. It is important to remember that the overall design goal is not to maximize the converter's frequency, but rather to achieve an acceptable
mix of factors such as efficiency, dynamic performance, density and cost. In this context, the questions that arise are: what topologies are more efficient in particular frequency ranges? what tradeoffs exist between these options? The purpose of this thesis is, therefore, to address the selection of high frequency power converter topologies from this perspective.

Square-wave and resonant converter topologies are examined in detail in Chapters 3 and 4. Frequency and power levels are established where, on the basis of overall efficiency, it becomes favorable to move from the square-wave to the resonant switching approach. The tradeoffs involved in making this move, and the drawbacks of the resonant techniques, are discussed. This knowledge is then used to propose topological solutions that achieve a compromise between the losses of the square-wave topologies and the limitations of the resonant topologies. The experimental development of one such topology, the Resonant Forward Converter, is presented in Chapter 5. Chapter 6 motivates and describes component optimizations to improve the Resonant Forward Converter's performance.

The viability of the resonant switching approach in practical applications is also examined, using the Resonant Forward Converter as the vehicle for this discussion. In particular the implementation of suitable high frequency control is addressed in Chapter 7, where the development of experimental devices for the Resonant Forward Converter is presented. In Chapter 8 a collection of topological issues are presented to demonstrate that a detailed knowledge of the effects of parasitic reactances can be used to advantage. The thesis concludes by summarizing the results of each section of the work, and uses these results to address the question of the overall benefit of moving away from square-wave operation.

The remainder of this chapter uses a simple down-converter application to illustrate the basic points that are developed in more detail in the subsequent chapters.
2.1 Square-Wave vs. Resonant Switching

As stated above, the ultimate limit to the switching frequency in a square-wave converter, using power MOSFETs and Schottky diodes, is power dissipation caused by parasitic elements. Consider, for example, the down converter of Fig. 2.1a, which is operating with a 50% duty ratio. The ideal switch stresses are shown in Fig. 2.1b, with the current and voltage transitions depicted as instantaneously.

There are three parasitic reactances that effect the operation of this converter: the junction capacitances of the semiconductor devices, $C_f$ (often labelled $C_{oss}$) and $C_d$, and the parasitic inductance, $L_s$, between the two switch paths which comes from the components and their interconnection. The effect of these parasitics on the converter’s operation is quite complex (and is developed in Chapter 3). Basically, the parasitics increase the switching stresses on the devices and contribute losses in their interaction with the power converter.

Consider, for example, the MOSFET’s output capacitance, $C_f$. When the MOSFET turns on, this capacitor, which was charged to $V_{in}$, is discharged through the MOSFET’s channel. An energy equal to $\frac{1}{2}C_fV_{in}^2$ is lost. Similarly, every switching cycle losses occur which are proportional to the energy stored in the diode’s capacitance, $\frac{1}{2}C_dV_{in}^2$, and the energy stored in the parasitic inductance, $\frac{1}{2}L_pI_o^2$. As the product of these losses each cycle and the switching frequency becomes a significant fraction of the converter’s output power, $P_o$, the overall converter operation becomes increasingly inefficient.

Different components and different construction techniques can be used to reduce a converter’s parasitic elements, but there are other design tradeoffs to consider. Again let us take the MOSFET’s output capacitance as an example. A smaller MOSFET die could be used to reduce the junction capacitance, but only at the cost of a larger on-state resistance and, therefore, a larger conduction loss.

If increasing the converter’s operating frequency without increasing its losses is
the goal, a resonant converter could be used to overcome a debilitating reactive parasitic. For instance, the same down-converter discussed above could be implemented using the quasi-resonant switching topology, shown in Fig. 2.3a [6]. This topology uses a resonant capacitor in parallel with the MOSFET, and a resonant inductor in the loop of the semiconductor devices, so that two of the reactive parasitics of Fig. 2.2 are incorporated in the resonant elements of this topology. However, the explicit resonant elements that still must be added are just the beginning of the increased complexity imposed by this topology (as Chapter 4 will discuss).
Figure 2.2: Square-Wave Down Converter with Parasitics

The ideal waveforms of the quasi-resonant converter are shown in Fig. 2.3b. Again, the detailed operation is quite complex, but the waveforms of Fig. 2.3b tell much of the story. This topology’s accommodation of the parasitic elements that were in series and parallel with the MOSFET can be seen in the slow and smooth transitions of the MOSFET’s voltage and current waveforms, which are in contrast to the step changes of Fig. 2.1b. Only the MOSFET’s current waveform makes a step change when it turns off; its voltage remains at zero. When the MOSFET turns on, both its voltage and its current are at zero. Because both of the MOSFETs transitions occur at zero voltage, this condition is referred to as a zero-voltage switching topology. Furthermore, and not so apparent, the energy stored in $C_r$ and $L_r$ prior to turn-off is not lost during the resonant ring.

One visible penalty of the resonant approach is that the MOSFET’s voltage waveform now has a peak value of $2V_{in}$, twice the peak stress that it had in the square-wave converter. If the die size of the MOSFET is kept constant, a doubling of its voltage rating will increase its on-state resistance and therefore result in higher conduction losses. Another drawback is the changed input current waveform. The average value of the input current, $I_{in-ave}$, is the same but the harmonic content is increased. The higher rms value of the current increases the conduction losses in the input filter stage. The capacitor in the input filter is sized to give a certain voltage ripple when driven by the ac component of the input current waveform. So,
Figure 2.3: Ideal, Quasi-Resonant Down Converter
the input capacitor will have to be larger with the increase in the harmonic content (approximately 30% in this case).

The tradeoffs above are for the ideal operation of a quasi-resonant converter. The operation is much more complicated when non-idealities are considered. First, there is the effect of the parasitic element that the topology did not account for, namely the diode's capacitance, $C_d$. As the waveforms of Fig. 2.3b show, the diode is still subjected to a step change in its voltage. This parasitic capacitance is therefore a source of dissipation, just as it was for the square-wave converter.

The most severe problem is the effect of load variation, however. The ideal waveforms of Fig. 2.3b corresponded to a particular value of load current. A higher value of current will increase the peak MOSFET voltage, further increasing the voltage rating and therefore also increasing the on-state resistance and conduction losses. A lower value of current, on the other hand, will not allow the MOSFET voltage to ring back down to zero before the MOSFET turns on. Therefore, the MOSFET voltage will go through a step change, contributing loss, just as it did in the square-wave converter.

In addition, there are problems controlling the quasi-resonant converter. Even if a restricted load range is specified such that the peak MOSFET voltage stresses are acceptable, variable frequency control must be employed which is complicated in its implementation and causes problems with EMI noise suppression.

While the resonant approach permits operation at high-frequencies, there are numerous tradeoffs involved with this choice. The next question is: is there a middle ground between the square-wave and resonant switching approaches? Ideally, what we would like to have is a square-wave like power transfer scheme (meaning no excess off- or on-state stresses) with the benign switch transitions of the resonant approach. This issue is explored in Chapter 3 and a particular example is developed all the way to a working converter in Chapter 5. We can consider a simplified example here.
To highlight the important features of this work, consider the converter of Fig. 2.4a. There is a resonant capacitor in parallel with the MOSFET and a resonant inductor in series with the MOSFET, just as in the quasi-resonant converter circuit of Fig. 2.3a. The difference is that now the rectifying diode is connected to a mid-point tap on the resonant inductor, which is itself connected between the MOSFET's source and the converter's ground. The MOSFET and the diode are incrementally in parallel in this circuit, so while the resonant capacitor is shown in parallel with the MOSFET, it could as easily be placed in parallel with the diode. Therefore, this circuit incorporates both of the device capacitances. Again, the detailed behavior is quite complex, and is developed for a converter with a transformer in Chapter 5, but the basic resonant waveforms shown in Fig. 2.4b reveal the fundamental points. First, both semiconductor devices have slow, smooth voltage transitions. Second, the resonance occurs when both devices are non-conducting, so these benign transitions are independent of load. The peak MOSFET voltage is increased to approximately $3.3V_{in}$, but in contrast to the resonant circuit, this is independent of load. The peak diode voltage is approximately the same as before. In fact, transformer versions of this circuit have lower peak stresses than the ideal stresses in the resonant circuit, as explained in Chapter 5.

The problem with the converter of Fig. 2.4 as it stands is that it has no regulation capability. Modifications that allow it to achieve regulation without incurring unreasonable losses are presented in Chapters 5 and 8. However, the basic converter does permit very high frequency power transfer, and because of the independence of the resonant action from the level of load, it has distinct advantages over the resonant circuit of Fig. 2.3. It also has the benefit of fixed-frequency operation.

The important question remaining to be answered is: can either of these resonant converters really improve on the overall performance of a square-wave converter? Can they, for instance, be controlled with sufficiently high bandwidth to take advantage of the potential reduction in filter requirements that the higher switching frequency implies? The specific issue of high-frequency control for a converter re-
Figure 2.4: Resonant Peak-Detector Converter
lated to that of Fig. 2.4, but using a transformer, is addressed in Chapter 7. Also, can energy storage components continue to operate at the same energy densities at these high frequencies and continue to operate efficiently? These component related issues are addressed in Chapters 3, 4, 5, and 6.

In the discussion so far, we have neglected an issue that is becoming increasingly important and so deserves particular attention in our study. This is the problem of rectification efficiency for low voltage supplies. A 0.5 V Schottky diode drop, in a 5 V power supply, accounts for 10% dissipation of the total delivered power. Newer, lower voltage Schottkys have become available with drops on the order of 0.35 V, reducing the rectifier losses by about 30%. However, the rectifier still represents a substantial portion of the total loss in the converter, and this problem will be worse with 3 V output voltages.

In general, the power circuit that supplies the low voltage output takes the energy from a much higher voltage. So, to avoid an unreasonable combination of high voltage and high current stresses in the semiconductor devices, transformer circuits are used. These circuits operate much like the simple down-converters we have been describing, with the important difference being the effect of an additional parasitic reactance: the transformer's magnetizing inductance (the transformer's leakage inductance adds to the parasitic inductance, $L_\alpha$, discussed above). The voltage stresses on the semiconductor components are considerably higher in the resonant transformer circuits than in the square-wave transformer circuits. In addition, the new, low-voltage Schottkys have large leakage currents, so the issue of reverse voltage stress on the rectifier component has become critically important.

One approach that is being pursued to improve rectification efficiency is to replace the rectification diodes with controlled switches that are turned on when the rectifier would have been on, but are designed to have lower on-state voltages. This technique is referred to as synchronous rectification and is discussed in relation to different converter topologies in Chapters 3, 4, 6 and 8. Factors that determine the viability of synchronous rectification include the relationship between the rms
and average values of the current waveform, the need to provide the gate drive signal and gate drive energy for these devices, and losses in the power circuit caused by the synchronous rectifier's output capacitance. The choice of power converter topology has a strong influence on all of these factors.

The ability to implement synchronous rectification is a good example of a factor that can easily shift the balance between a square-wave converter and a higher frequency resonant circuit for a particular application. So, when conclusions are made about this balance, particularly for the range of voltage and power levels where both square-wave and resonant switching seem attractive, it is important to realize that this is a dynamic balance. There is no right or wrong topology, only a better topology for a specific application using the components available at that time.
Chapter 3

Square-Wave Converters

This chapter examines high-frequency, square-wave power conversion in detail, focusing on the effects of parasitic energy storage elements on the converter’s operation.

3.1 Basic Operation

The canonical switching cell [18] of a square-wave converter is shown in Fig. 3.1a and the ideal switching waveforms are shown in Fig. 3.1b. The basic principle of operation is to adjust the duty ratio of the switch, \( D \), to achieve a desired average value of the output voltage. For the ideal network of Fig. 3.1a this relationship is,

\[
V_{o-\text{ave}} = DV_{\text{in}} \tag{3.1}
\]

and

\[
I_{\text{in-ave}} = DI_o \tag{3.2}
\]

The rms input current can be calculated as,

\[
I_{\text{in-rms}} = \sqrt{D}I_o = \frac{I_{\text{in-ave}}}{\sqrt{D}} \tag{3.3}
\]
The basic cell of Fig. 3.1a can achieve both up-conversion and down-conversion, depending on the direction of the power flow (which is determined by the sign of the output current, $I_o$). The simple up-down converter topology differs only slightly from the cell of Fig. 3.1a, with the incremental current source switching between two voltage sources of opposite polarity that are the source and load, respectively.

The simplistic representation of Fig. 3.1 ignores ripple in the current and voltage waveforms. This ripple exists because the physical reactive components only approximate the incremental sources. It also assumes instantaneous (and therefore lossless) switch transitions, whereas in reality the double pole switch is implemented with imperfect semiconductor switching devices, as shown in the down converter of Fig. 3.1c. The analysis of a practical converter therefore requires much more detailed models, particularly if the switch transition times become a significant fraction of the total period.

A first order correction to the idealized model that accounts for load dependent switching losses is shown in Fig. 3.1d, where finite transition times for the controlled switch, $t_{on}$ and $t_{off}$, have been introduced. During the switch's turn-on transition the free-wheeling diode holds the voltage of node $X$ at zero until the controlled switch picks up the full output current. Conversely, during the controlled switch's turn-off transition, the diode does not become forward-biased, and so pick up any of the load current, until the switch supports the full input voltage.

For low-frequency converters with relatively slow switch transitions, this simplistic explanation is reasonably accurate and predicts switching losses of $[4] \frac{1}{2} V_{in} I_o (t_{on} + t_{off})$ each cycle. This also changes the input-output relationships to,

$$V_{o-ave} = \frac{(DT - t_{on} + \frac{t_{off}}{2})}{T} V_{in}$$  \hspace{1cm} (3.4)

and
Figure 3.1: Canonical Switching Cell and Waveforms

\[
I_{in-ave} = \frac{(DT - \frac{t_{on}}{2} + t_{off})}{T} I_o
\]  
(3.5)

For a desired input-output voltage ratio and a specific power level the effect of the finite transitions is to increase the average input current by an amount equal to

\[
\Delta I_{in-ave} = \frac{t_{on} + t_{off}}{2T} I_o
\]  
(3.6)

which, when multiplied by the input voltage, exactly accounts for the switching loss.

For a high-frequency converter implemented with high-speed semiconductor devices (typically the power MOSFET and power Schottky), however, the above ex-
planation is too simplistic. The detailed switching behavior and switching losses are instead dominated by the parasitic reactive elements that are present in the components and their interconnection.

![Circuit Diagram]

Figure 3.2: Square-Wave Down Converter with Parasitics

### 3.2 High-Frequency Switching Transitions

#### 3.2.1 Converter Parasitics

The detailed switching operation of a high-frequency (1 MHz range) square-wave converter, utilizing a power MOSFET and Schottky diode, can be modelled by the equivalent circuit of Fig. 3.2. The capacitances shown in parallel with the semiconductor devices are their own junction capacitances. The output capacitance of the MOSFET, $C_f$, is actually the parallel combination of the drain-source capacitance, $C_{DS}$, and the drain-gate or ‘Miller’ capacitance, $C_{DG}$, giving $C_f = C_{DS} + C_{DG}$. This combined output capacitance of the MOSFET is also commonly referred to as $C_{oss}$.

The MOSFET’s channel is controlled by the gate-source voltage, which in turn is controlled by the gate drive circuitry that charges and discharges the two gate capacitances, $C_{DG}$ and $C_{GS}$. Because the gate-drain capacitance couples the power circuit and the gate drive circuit, the interaction of these circuits (the ‘Miller’ effect) is an important part of the detailed analysis. Also, both device capacitances are
nonlinear, being junction capacitances, which must be considered in the analysis. The nonlinearity generally takes the form of a square law relationship so that if we define \( C_{f_0} \) as the MOSFET's incremental capacitance at its rated voltage, \( V_{f_{-\text{max}}} \), then the incremental capacitance as a function of voltage is approximately

\[
C_f(V) = C_{f_0} \sqrt{\frac{V_{f_{-\text{max}}}}{V}}
\]  
(3.7)

and similarly for the diode

\[
C_d(V) = C_{d_0} \sqrt{\frac{V_{d_{-\text{max}}}}{V}}
\]  
(3.8)

The rated voltages for the diode, \( V_{d_{-\text{max}}} \), and the MOSFET, \( V_{f_{-\text{max}}} \), may well be different. These incremental capacitances are calculated by differentiating the charge stored in each parasitic capacitance with respect to voltage. The relationship for the charges are

\[
Q_f(V) = 2C_{f_0} \sqrt{V_{f_{-\text{max}}}V} = 2C_f(V)V
\]  
(3.9)

and

\[
Q_d(V) = 2C_{d_0} \sqrt{V_{d_{-\text{max}}}V} = 2C_d(V)V
\]  
(3.10)

The parasitic inductance, \( L_s \), is the sum of the inductances in the loop of the semiconductor devices and the input capacitor, where the input capacitor is modelled in Fig. 3.2 by the input voltage source. The inductance comes from the components and their interconnection, and in transformer circuits includes the leakage inductance of the transformer. Typical values for this inductance vary from 1–2 nH to 100–200 nH, which is discussed further in Section 3.3.3.

\footnote{The capacitance does not have a singularity at \( V = 0 \) because of the junctions built-in voltage}
3.2.2 Operation Neglecting Parasitic Inductance

The MOSFET's gate voltage controls the state of the MOSFET throughout both its switch transitions, and this voltage is, in turn, determined by the charge on the MOSFET's gate. The MOSFET's channel acts as a controlled current source with the magnitude determined by the gate voltage, so both switching transitions are charge controlled transitions. Figure 3.3 shows the approximate voltage and current waveforms of the MOSFET during the two switch transitions, and also shows the corresponding gate voltage and gate charge. To understand how the power and gate drive circuits interact with the parasitic device capacitances, we will initially neglect the effect of the loop inductance, $L_a$, and examine the transitions that result.

**Turn-off:** The turn-off transition begins with the MOSFET's channel changing from a conducting to a non-conducting state. Prior to turn-off the MOSFET carries the full load current, $I_o$, and has a small voltage drop due to its on-state resistance of $V_{DS-on} \approx I_o R_{DS-on}$. The channel starts to turn off when the gate-source voltage just supports the channel's current with the MOSFET in the linear region (point a of Fig. 3.3a), and the channel is completely non-conducting when the voltage falls below the threshold voltage (point b of Fig. 3.3a). As the current in the channel falls, the load current transfers to the two device capacitances of Fig. 3.2, $C_f$ and $C_d$, which begin to charge and discharge, respectively. The time required to remove the charge $\Delta Q_1$ is,

$$ t_{a-b} = \frac{\Delta Q_1}{I_{gate}} \quad (3.11) $$

which for a reasonable level of gate current is short ($\sim 5$ ns). During this time the MOSFET’s drain voltage rises to,

$$ V_{DS-b} \approx I_o R_{DS-on} + t_{a-b} \frac{I_o}{2} (C_f + C_d) \quad (3.12) $$

40
which is also typically negligible.

Once the channel is off, the output current proceeds to discharge node \( X \) of Fig. 3.2, with the current splitting between the MOSFET and diode paths in the ratio of the incremental device capacitances. There are three components of the discharging current, as shown in Fig. 3.4. One component, \( i_1 \), is the current that charges the MOSFET's drain-source capacitance, \( C_{DS} \). Another component, \( i_2 \), is the current that charges the MOSFET's drain-gate or 'Miller' capacitance, \( C_{DG} \), and also flows through the gate drive impedance, \( Z_G \). The third component of the current, \( i_3 \), is the current that discharges the diode's capacitance, \( C_d \). Assuming that the gate voltage is relatively constant during this interval the currents are
\[ i_1 = \left( \frac{C_{DS}}{C_{DS} + C_{DG} + C_d} \right) I_o \]  \hspace{1cm} (3.13)

\[ i_2 = \left( \frac{C_{DG}}{C_{DS} + C_{DG} + C_d} \right) I_o \]  \hspace{1cm} (3.14)

\[ i_3 = \left( \frac{C_d}{C_{DS} + C_{DG} + C_d} \right) I_o \]  \hspace{1cm} (3.15)

with the sum of the components being, as stated above,

\[ i_1 + i_2 + i_3 = I_o \]  \hspace{1cm} (3.16)

The MOSFET capacitances, \( C_{DG} \) and \( C_{DS} \), get smaller as node X discharges, and the diode capacitance gets larger in accordance with (3.7) and (3.8). So \( i_1 \) and \( i_2 \) become progressively smaller and \( i_3 \) progressively larger throughout the transition. To keep the MOSFET off while its drain voltage rises, during the interval b-c of Fig. 3.3a, the gate drive circuitry must sink the drain-gate portion of the current (\( i_2 \)) while holding the gate-source voltage below the threshold voltage, or

\[ V_{GS} \simeq i_2 Z_G \leq V_{th} \]  \hspace{1cm} (3.17)
Although the capacitances are non-linear, there is a fixed amount of charge that has to be removed from node $X$ which is approximately $\Delta Q = (C_f + C_d)V_{in}$, so the discharge time can be estimated as

$$t_{b\rightarrow c} = \frac{(C_f + C_d)V_{in}}{I_o}\quad(3.18)$$

or more accurately, using (3.9) and (3.10), as

$$t_{b\rightarrow c} = \frac{2[C_f(V_{in}) + C_d(V_{in})] V_{in}}{I_o}\quad(3.19)$$

This discharge time is generally the dominant component of the transition time, $t_{off}$.

The discharge of node $X$ continues until the voltage is clamped by the freewheeling diode becoming forward-biased. Because the MOSFET's voltage and current are never coincident during the switching transition, the entire turn-off process is lossless, provided the channel remains non-conducting while the drain voltage rises.

**Turn-on:** The turn-on transition begins when the MOSFET's gate voltage reaches the device's threshold voltage (point $d$ of Fig. 3.3b), and the transition is complete when the drain-source voltage falls to the on-state voltage (point $f$ of Fig. 3.3b). During the transition interval, there are load-dependent switching losses of approximately

$$E = \frac{1}{2} V_{in} I_o t_{on}\quad(3.20)$$

just as were predicted by the simplified model we discussed earlier. Because the state of the MOSFET is controlled by the gate voltage, the duration of the transition, $t_{on}$, is determined by the required charge and the gate drive current as
\[ t_{on} = \frac{\Delta Q_2}{I_{gate}} \]  

(3.21)

The first part of this charge, transferred during the d-e interval of Fig. 3.3b, is essentially identical to \( \Delta Q_1 \) since it corresponds to the charge in the inversion layer of the MOSFET’s channel. The rest of the charge, which is generally the dominant component, is the ‘Miller’ charge, \( Q_{DG} \), and its transfer allows the drain voltage to fall in the e-f interval of Fig. 3.3b. The load-dependent power dissipation, \( P_{ld} \), can be calculated by combining (3.20) and (3.21) and multiplying the result by the switching frequency as

\[ P_{ld} = \frac{V_{in} I_0 \Delta Q_2}{2I_{gate}} f_{sw} \]  

(3.22)

Using the approximation that \( \Delta Q_2 \simeq Q_{DG} \) this can be simplified to

\[ P_{ld} \simeq \frac{V_{in} I_0 Q_{DG}}{2I_{gate}} f_{sw} \]  

(3.23)

In addition to the load dependent losses, the forced charging and discharging of the device capacitances during the turn-on transition also contribute losses. As the MOSFET's voltage collapses, its output capacitance is discharged through its channel, and at the same time the diode's capacitance is charged from the input voltage source, through the channel. All of the energy stored in the MOSFET’s capacitance is dissipated. To calculate this energy accurately, we need to take the nonlinearity of the capacitor into account. The stored energy can be calculated as

\[ E = \int_0^Q V dQ = \int_0^V V \frac{dQ}{dV} dV \]  

(3.24)

so making the substitution that \( \frac{dQ}{dV} = C_f(V) \) from (3.7), we can calculate the energy stored in the MOSFET's capacitance when it is charged to \( V_{in} \) as
\[ E = \int_0^{V_{in}} V \left( C_f \sqrt{\frac{V_{f-max}}{V}} \right) dV = \frac{2}{3} \left( C_f \sqrt{V_{f-max}} \right) V_{in}^{1.5} \]  

which is the energy lost each cycle when the MOSFET turns on. As a general function of voltage, the stored energy can also be written as

\[ E(V) = \frac{4}{3} \left( \frac{1}{2} C_f(V)V^2 \right) \]

While the MOSFET's capacitance is discharged by turning on the channel, the diode's capacitance is charged. The energy stored in the diode's capacitance when it is charged to \( V_{in} \) is

\[ E = \frac{2}{3} \left( C_d \sqrt{V_{d-max}^1} \right) = \frac{4}{3} \left( \frac{1}{2} C_d(V_{in})V_{in}^2 \right) \]

All of the charge is supplied to the capacitance from the input voltage source and is equal to

\[ Q_d(V_{in}) = 2C_d \sqrt{V_{d-max}^1} = 2C_d(V_{in})V_{in} \]

The source provides an energy equal to \( Q_dV_{in} \), so the energy lost in charging \( C_d \) is

\[ E = Q_dV_{in} - \frac{2}{3} \left( C_d \sqrt{V_{d-max}^1} \right) = \frac{4}{3} \left( C_d \sqrt{V_{d-max}^1} \right) V_{in}^{1.5} \]

Comparing (3.27) and (3.29) reveals that twice the energy that is stored in the diode's nonlinear capacitance when it is in its off state is lost in charging it.

We can also express the MOSFET's 'Miller' charge in terms of the off-state voltage, \( V_{in} \), using \( Q_{DG0} \) to represent the charge at \( V_{f-max} \), as

\[ Q_{DG}(V_{in}) = Q_{DG0} \sqrt{\frac{V_{in}}{V_{f-max}}} = 2C_{DG}(V_{in})V_{in} \]
where

\[ Q_{DG_0} = 2C_{DG_0} V_f \text{-max} \quad (3.31) \]

Substituting (3.31) into (3.23) gives

\[ P_{ld} \approx \frac{V_{in} I_0 C_{DG_0} \sqrt{V_{in} V_f \text{-max}}}{I_{gate}} f_{sw} = \frac{V_{in}^2 I_0 C_{DG}(V_{in})}{I_{gate}} f_{sw} \quad (3.32) \]

for the load-dependent switching loss. Likewise, the power dissipation due to the capacitive switching losses, \( P_{sw-m} \) and \( P_{sw-d} \) can be written using (3.25) and (3.29) as

\[ P_{sw-m} = \frac{2}{3} \left( C_f \sqrt{V_f \text{-max}} V_{in}^{1.5} \right) f_{sw} = \frac{2}{3} \left( C_f(V_{in}) V_{in}^2 \right) f_{sw} \quad (3.33) \]

\[ P_{sw-d} = \frac{4}{3} \left( C_d \sqrt{V_d \text{-max}} V_{in}^{1.5} \right) f_{sw} = \frac{4}{3} \left( C_d(V_{in}) V_{in}^2 \right) f_{sw} \quad (3.34) \]

3.2.3 Operation Including Parasitic Inductance

\textbf{Turn-off:} Let us now examine the effects of the parasitic inductance on the turn-off transition, beginning with the extreme of a relatively small inductance. The parasitic inductance alters the turn-off transition by introducing a high-frequency (much higher than the switching frequency) resonance between itself and the series combination of the two device capacitances, \( C_f \) and \( C_d \), as node \( X \) discharges. Instead of the load current immediately splitting between \( C_f \) and \( C_d \) in the ratio of their incremental capacitances when the MOSFET turns off, the commutation is delayed slightly. During the subsequent discharge the capacitor currents oscillate around the value they would have had in the absence of the inductor, and the capacitor voltages have corresponding high-frequency ringing components. If the frequency of the oscillation is high enough, however, the current commutation
process is not significantly disturbed. A rough criteria for this is that the period of oscillation be less than the discharge time, or

$$T_{osc} \approx 2\pi \sqrt{\frac{L_s C_f C_d}{C_f + C_d}} < t_{on} \tag{3.35}$$

When the voltage at node $X$ reaches zero, the diode becomes forward-biased, and the diode's capacitance is removed from the oscillation. The parasitic inductance and the MOSFET capacitance continue to ring, however, causing some overshoot in the MOSFET's voltage. The amplitude of this overshoot is the product of the portion of $I_o$ still flowing through the inductor when the diode turns on and the characteristic impedance, $\sqrt{L_p/C_f}$, of the ringing circuit.

If all of $I_o$ were still flowing in the parasitic inductance when the diode turned on, quite a large overshoot would result. Fortunately, the nonlinear nature of both $C_f$ and $C_d$ results in the diode's capacitance being considerably larger than the MOSFET's capacitance as the voltage of node $X$ approaches zero. In the absence of the inductance, the current $I_o$ splits in the ratio of these device capacitances, as discussed previously, so as the voltage approaches zero most of the current flows through $C_d$ rather than through $C_f$, assuming that the current has had time to commutate. The excess MOSFET voltage is therefore not as great as would otherwise be expected, provided the condition of (3.35) is satisfied.

Some energy is lost during the high-frequency oscillation that occurs as node $X$ discharges, and whatever energy remains in the inductor when the diode clamps the voltage is lost in the subsequent ring with the MOSFET's capacitance. The precise amount of energy lost due to the high frequency oscillations is difficult to quantify, since it is dependent on the damping, the relative timing of the ring, and the discharge time\footnote{If the discharge time exactly matched a half-cycle of the ring the diode would clamp with little or no current in the leakage inductance and with the MOSFET fully charged.}, but it can be as large as the energy that is initially stored in the parasitic inductance.
If, on the other hand, the period of the resonance between the inductor and the series combination of $C_f$ and $C_d$ is long compared to the discharge time (which is generally true in transformer circuits), then there is not any appreciable commutation of the inductor current during the transition. In this case, the MOSFET is subjected to an appreciable overvoltage ring once node $X$ has discharged to zero, and the inductor's energy, which does not change significantly, will subsequently be dissipated. This extreme condition often calls for the consideration of clamp or snubber circuits to limit the MOSFET's voltage.

**Turn-on:** The effect of the parasitic inductance on the turn-on transition is also very dependent on the size of the inductance. If the inductance is relatively large the MOSFET can turn on hard, and its drain-source voltage can drop to zero (the on-state voltage), without it having to pick up much of the load current. The change in the inductor current as the drain-source voltage falls is approximately

$$\Delta I = \frac{V_{in}t_{on}}{2L_s} \tag{3.36}$$

So, for

$$L_s \gg \frac{V_{in}t_{on}}{2I_o} \tag{3.37}$$

$\Delta I$ is not significant. In this case the load dependent switching losses are avoided in the MOSFET at turn-on, but the energy that is stored in the parasitic inductance, most of which will be lost at the subsequent turn-off transition, is

$$\frac{1}{2} L_s I_o^2 = \frac{1}{2} \left( \frac{V_{in}t_{on}I_o}{2} \right) \frac{I_o}{\Delta I} \tag{3.38}$$

which will be considerably higher than the load dependent losses if $\Delta I \ll I_o$.

Assuming that the MOSFET's voltage falls linearly, the inductor current increases quadratically during the transition. The switching losses in the MOSFET
can be calculated for $\Delta I < I_o$ as

$$E = \frac{V_{in}^2 I_{on}^2}{24L}$$

$$= \Delta I \frac{V_{in} I_{on}}{12} \quad (3.39)$$

If $\Delta I = I_o$, then the sum of (3.38) and (3.39) gives a potential loss per cycle of $\frac{2}{3}(\frac{1}{2} V_{in} I_o I_{on})$, which is less than the loss in the absence of the inductance. This sum includes the inductor's energy, which may or may not be lost in the subsequent turn-off transition, so the inclusion of some parasitic inductance can actually lower the switching losses.

Once the MOSFET is on, the inductor current builds up linearly, and when it reaches the level of the output current, the diode turns off. The off-state voltage of the diode is $V_{in}$, so once the diode has turned off its device capacitance begins to charge towards this level through the parasitic inductance. The inductance and the diode's capacitance ring together, with the capacitor voltage ringing around $V_{in}$. Because all of the charge on the diode's capacitance comes from the input, when the ring finally decays the energy lost is identical to what we calculated in (3.29), when the diode's capacitance was charged through the resistance of the MOSFET's channel and the inductance was neglected.

Unfortunately, the diode's voltage rings around $V_{in}$, which was the nominal off-state voltage in the absence of the inductance, so the voltage rating of the diode generally has to increase. Because the junction capacitance is nonlinear it may, depending on the damping, actually ring to higher than twice $V_{in}$. The typical result is that the diode's voltage withstanding capability has to be doubled.

In most applications, with the notable exception of transformer circuits with safety isolation requirements, the leakage inductance can be made fairly small. So, as the MOSFET's drain voltage collapses, the load current commutates to the in-
ductor and the diode capacitance begins to charge. The amplitude of the subsequent voltage oscillation at node $X$ can therefore be much smaller than $V_{in}$. The criteria for the inductance is

$$L_s < \frac{V_{in} t_{on}}{2 I_o} \quad (3.40)$$

### 3.2.4 Experimental Verification

The detailed behavior we have described has been verified both by simulation of high-frequency converters and from observation of an experimental 1 MHz square-wave converter\(^3\).

Figure 3.5a presents the results of a SPICE simulation of the turn-off transition of the experimental circuit. It shows the degree to which the load current commutates to the diode's capacitance during the transition, as well as the subsequent overvoltage on the MOSFET, for the case where the parasitic inductance is small. Figure 3.5b shows the actual MOSFET's voltage in the experimental circuit. The overshoot in this case is seen to be only 15\% of $V_{in}$.

The turn-on transition is shown in Fig. 3.6. As can be seen, the overshoot in the diodes voltage is very small, indicating that the parasitic inductance is quite small and that the diode had commutated off while the MOSFET voltage was falling. The figure also shows that a turn-on time for the MOSFET of approximately 15 ns can be achieved.

\(^3\)This work was reported in [7], with the experimental converter described in detail in [19].
(a) SPICE Simulation

(b) MOSFET Voltage (20 V/div, 10 nsec/div)

Figure 3.5: Waveforms at Turn-Off
3.3 Component Selection and Parasitics

3.3.1 MOSFET Selection

There are four loss mechanisms associated with the MOSFET. Two of them were covered above: the load dependent switching loss, $P_{id}$ of (3.32), and the turn-on loss of the MOSFET discharging its own output capacitance, $P_{sw-m}$ of (3.33). The other losses are the on-state conduction losses in the MOSFET and the gate drive losses.

The conduction loss, $P_{cond.}$, equals

$$P_{cond.} = I_{rms}^2 R_{DS-on}$$  \hspace{1cm} (3.41)

and the gate drive loss, $P_{gate}$, equals
\[ P_{gate} = Q_g V_{dd} f_{sw} \]  

(3.42)

where one component of \( Q_g \) is the gate-source charge, which is equal to \( C_{GS} V_{dd} \), and the other component of the charge is the 'Miller' charge, \( Q_{DG} \), as expressed in (3.30).

In choosing a MOSFET die size for a particular application, a common objective is to minimize the sum of the losses expressed by (3.32), (3.33), (3.41), and (3.42). Three of these losses are proportional to the device capacitances, which are in direct proportion to the area of the die. The other loss, the conduction loss, is proportional to the device resistance, which is inversely proportional to the area. If all of the other variables: the gate-drive current \( (I_{gate}) \), the MOSFET's voltage rating \( (V_{f_{-max}}) \), the voltage stress (in this case \( V_{in} \)), the gate-drive voltage \( (V_{dd}) \), the switching frequency \( (f_{sw}) \), and the power level \( (I_o) \), are held constant, the sum of the dissipation components can be expressed as,

\[ P_{diss} = K_1 A + \frac{K_2}{A} \]  

(3.43)

where \( A \) is the area of the MOSFET die. This expression has a minimum value when

\[ K_1 A = \frac{K_2}{A} \]  

(3.44)

meaning that the dissipation proportional to area equals the dissipation inversely proportional to area. In reality there are only discrete values of die area available, but the desire to balance the conduction and capacitive losses serves to guide the selection of an appropriate device for a particular application.

In the region of minimum loss, the total loss is not a particularly strong function of the device area. As a result, the exact die size is not critical, as long as the two losses of (3.43) are of the same order. For instance, if a die size of area \( A_2 \) has a
loss proportional to area of $K_1 A_2$ and a loss that is inversely proportional to area of $K_2 / A_2$, then the optimal area can be calculated from the actual area and the distribution of losses as

$$A_1 = A_2 \sqrt{\frac{K_2}{K_1 A_2}}$$  \hspace{1cm} (3.45)

and the minimum losses can be expressed as

$$P_{\text{min}} = 2(K_1 A_2) \frac{A_1}{A_2} = 2 \left( \frac{K_2}{A_2} \right) \frac{A_2}{A_1}$$  \hspace{1cm} (3.46)

The ratio of the actual power dissipation to the minimum power dissipation can be calculated as

$$\frac{P}{P_{\text{min}}} = \frac{\left( \frac{A_2}{A_1} \right)^2 + 1}{2 \left( \frac{A_2}{A_1} \right)}$$  \hspace{1cm} (3.47)

These expressions show that the total loss is relatively insensitive to variation in die size. If the die is twice the optimal size, then the loss proportional to area is doubled and the loss inversely proportional to area is halved, so the total loss is only increased by 25%.

The on-state resistances and off-state capacitances of the 100V, 200V, and 400V MOSFETs commonly available today [20] are shown in Table 3.1 for each of five die sizes. Both the total and the Miller portion of the gate charge for each device is shown in Table 3.2. These parameters can be used to select a MOSFET die size for a particular application.

**Example:** We are to choose a MOSFET for a 50 W, 50 V–5 V down converter operated at 1 MHz. At full load the MOSFET is on for 10% of the time, carrying a current of $I_o = 10$ A. The rms current is $\sqrt{D} I_o$, so the conduction losses can be calculated using (3.41). We can begin the process of choosing an appropriate die
by, possibly naively, assuming that we are prepared to sacrifice 1% of the operating power, or 0.5 W, to the conduction loss mechanism. We would then be looking for an $R_{DS-on}$ of $\simeq 50 \text{ m}\Omega$. This would suggest using the 100 V, die size 5, MOSFET of Table 3.1. To ascertain whether this is a reasonable die size, we need to compare the 0.5 W conduction loss with the frequency-dependent losses of (3.33), (3.30) and (3.42). With a 10 V gate drive, using $Q_g = 63 \text{ nC}$ from Table 3.2 we can calculate the gate drive losses at 1 MHz, using (3.42), as 0.63 W. The incremental capacitance of the MOSFET at $V_{in}$ can be calculated from 3.7 as

$$C_f(V_{in}) = C_{d} \sqrt{\frac{V_{f-max}}{V_{in}}}$$

$$= 500 \sqrt{\frac{100}{50}} \text{ pF}$$

$$= 707 \text{ pF}$$

(3.48)  

(3.49)

so the turn-on switching losses can be calculated from (3.33) as 1.2 W. The charge stored in the Miller Capacitor at $V_{in}$ can be calculated from (3.30) as

$$Q_{DG}(V_{in}) = Q_{DG} \sqrt{\frac{V_{in}}{V_{f-max}}}$$

$$= 36 \text{ nC} \sqrt{\frac{50}{100}}$$

$$= 25.5 \text{ nC}$$

(3.50)  

(3.51)

and the load-dependent losses can be calculated from (3.23), using $I_{gate} = 2 \text{ A}$, as
\[ P_{ld} = \frac{V_{in}I_oQ_{DG}}{2I_{gate}} f_{sw} = 3.2 \text{ W} \]  \hspace{1cm} (3.52)

The sum of the capacitive losses is 5 W, which is 10 times greater than the 0.5 W conduction loss. Using (3.45), we can calculate the optimum area as

\[ A_1 = A_2 \sqrt{\frac{0.5}{5}} = 0.3A_2 \]  \hspace{1cm} (3.53)

and the minimum power can be calculated from (3.46) as

\[ P_{min} = 2 \left( \frac{K_2}{A_2} \right) \frac{A_2}{A_1} = 3.3 \text{ W} \]  \hspace{1cm} (3.54)

So if we use die size 3, instead of die size 5, we can reduce the total losses from 5.5 W to approximately 3.3 W.

<table>
<thead>
<tr>
<th>die size</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{mx} (volts)</td>
<td>R_{ds} (\Omega)</td>
<td>C_{fs} (pF)</td>
<td>R_{ds} (\Omega)</td>
<td>C_{fs} (pF)</td>
<td>R_{ds} (\Omega)</td>
</tr>
<tr>
<td>100</td>
<td>.6</td>
<td>40</td>
<td>.3</td>
<td>100</td>
<td>.18</td>
</tr>
<tr>
<td>200</td>
<td>1.5</td>
<td>20</td>
<td>.8</td>
<td>50</td>
<td>.4</td>
</tr>
<tr>
<td>400</td>
<td>3.6</td>
<td>9</td>
<td>1.8</td>
<td>25</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 3.1: Resistance and Capacitance of MOSFET Dice

<table>
<thead>
<tr>
<th>die size</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{mx} (volts)</td>
<td>Q_{gd} (nC)</td>
<td>Q_{g} (nC)</td>
<td>Q_{gd} (nC)</td>
<td>Q_{g} (nC)</td>
<td>Q_{gd} (nC)</td>
</tr>
<tr>
<td>100</td>
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<tr>
<td>200</td>
<td>3</td>
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<tr>
<td>400</td>
<td>3</td>
<td>6</td>
<td>6</td>
<td>12</td>
<td>7</td>
</tr>
</tbody>
</table>

Table 3.2: Gate-Drain(Miller) Charge and Total Gate Charge of MOSFET Dice

56
3.3.2 Schottky Diode Selection

The selection of a diode for a particular converter application is very similar to the MOSFET selection process described above. At low current levels, the Schottky diode has exponential voltage-current characteristics, but as the current level increases its resistance becomes dominant. Figure 3.7a shows several forward voltage operating points for a particular Schottky diode [21, pp. c11-c14]. The transition from the exponential to resistive behavior can clearly be seen. The resistive component can be estimated by the slope of the line that is tangential to the high current part of the curve, and the junction voltage can be modelled by the value of voltage where this line intersects the axis. This allows us to identify the parameters for the diode model shown in Fig. 3.7b. For this particular diode, the results are $R_d \simeq 12.5 \text{ m}\Omega$ and $V_{rect} \simeq 0.7 \text{ V}$.

Electrical specifications for two diodes with this forward voltage characteristic, but different reverse blocking voltages, are shown in Table 3.3. These devices, members of the IR50SQ series, have die sizes of 0.125 in by 0.125 in, but similar devices with different die sizes are available. As with the MOSFET, some parameters are proportional and some inversely proportional to the area of the die. The capacitance and the reverse leakage current, for instance, are proportional to the area, and the resistance, $R_d$, is inversely proportional to the area. The typical goal, just as in the MOSFET selection, is to choose a die size for a particular application that minimizes the total losses, by balancing the losses that are proportional to die area with the losses that are inversely proportional.

<table>
<thead>
<tr>
<th>$V_R$</th>
<th>50 V</th>
<th>100 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{do}$</td>
<td>250 pF</td>
<td>115 pF</td>
</tr>
<tr>
<td>$I_R(25\degree C)$</td>
<td>5 mA</td>
<td>1 mA</td>
</tr>
<tr>
<td>$I_R(125\degree C)$</td>
<td>13 mA</td>
<td>7 mA</td>
</tr>
</tbody>
</table>

Table 3.3: Characteristics of IR50SQ Type Schottky Rectifiers
Figure 3.7: Forward Conduction and Approximate Model for Schottky Rectifier
One of the losses that is proportional to die area is the capacitive charging loss of (3.29), written here in terms of the off state voltage, $V_{d-off}$, as,

$$ P = \frac{2}{3} \left( 2V_{d-off}^2 C_d \sqrt{\frac{V_{d-max}}{V_{d-off}}} \right) f_{sw} \quad (3.55) $$

where $V_{d-off}$ is equal to $V_{in}$ in the down converter circuit. The other loss that is proportional to area is due to reverse conduction when the diode is in its off state. The leakage current for the diode of Table 3.3 gives a linear relationship when the current is plotted against the reverse voltage on a log vs. linear (current vs. voltage, respectively) plot. The normalized reverse current as a function of the normalized reverse voltage is

$$ \left( \frac{I_r}{I_R} \right) = 10^{0.8 \left( \frac{V_r}{V_R} \right)} \quad (3.56) $$

The off-state voltage is fairly constant in the switching converters we are discussing, and occurs for $D$ of the time, so the loss due to reverse conduction can be calculated as

$$ P = DV_{d-off}I_r \quad (3.57) $$

where $I_r$ is the reverse current evaluated from (3.56) with $V_r = V_{d-off}$.

The loss that is inversely proportional to area is the conduction loss contributed by the resistive component of the forward drop. This loss can be expressed as

$$ P = I_{d-rms}^2 R_d \quad (3.58) $$

For a basic converter such as the down-converter with negligible current ripple, the diode's rms current is

$$ I_{d-rms} = \sqrt{1 - DI_o} \quad (3.59) $$
so the loss can be written

$$P = (1 - D)I_o^2R_d$$  \hspace{1cm} (3.60)

Once again, while there are not a continuum of die sizes available to choose from, we can use (3.55) (3.57) and (3.60) to guide our selection.

**Example:** If we used the 100 V diode of Table 3.3 in a 50 W, 50 V to 5 V, down converter operated at 1 MHz, we can calculate the resistive portion of the conductive losses as 1.13 W using \((1 - D) = 0.9, R_d = 12.5 \text{ m}\Omega, \text{ and } I_o = 10 \text{ A}\) in (3.60). The capacitive portion of the losses we can calculate from (3.55) as 0.54 W using \(V_{in} = 50 \text{ V}, C_{do} = 115 \text{ pF}, V_{d-max} = 100 \text{ V}\). The reverse conduction current can be calculated from (3.56) as approximately \(0.4I_R\), given that the off-state voltage is half the rated voltage. The loss due to this reverse conduction current varies from 18 mW to 0.13 W as the diode's junction temperature varies from 25°C to 125°C. In the high temperature extreme, this gives a loss inversely proportional to area of 1.13 W and a loss proportional to area of 0.67 W. These losses are comparable, therefore this particular diode appears to be a reasonable choice. A larger die area will achieve a lower total loss, but, as we showed in the previous section, the function does not have a sharp minimum. The optimum area, \(A_1\), can be calculated from the area, \(A_2\), and the losses using (3.45) as

$$\frac{A_1}{A_2} = \sqrt{\frac{1.13}{0.67}} \approx 1.3$$  \hspace{1cm} (3.61)

The power dissipation with this diode can be compared with the power dissipation using the optimal die size, using (3.47), as

$$P = 1.03 P_{\text{min}}$$  \hspace{1cm} (3.62)

The area dependent component of the power dissipation caused by this diode is
within 3% of minimum, so there is little motivation to select a different die size for this application. The loss due to the junction drop, \( V_{rect} \), is independent of area and is equal to \( I_{d-ave} V_{rect} \) which in this case is equal to 6.3 W, so the total dissipation due to the free-wheeling diode is 8.1 W. This loss is rather excessive for the 50 W power level. This provides a compelling reason to consider introducing a transformer into the topology, so that the diode is not subjected to both the peak voltage and the peak current.

### 3.3.3 Parasitic Inductance

Figure 3.8 shows one possible arrangement of the canonical cell’s components if hybrid fabrication is used. Given typical dimensions, and using multiple bond wires to approximate a conducting sheet as shown in the figure, a parasitic inductance of 15 nH or less is possible. This number is consistent with the inductance of a TO-220 package (which has roughly 5 nH per lead) and also with the calculated inductance of a thin conducting annulus having an inner diameter of 0.75 cm and an outer diameter of 1.5 cm (14 nH) [22]. By contrast, if leaded, packaged components are used, each device contributes about 10 nH, and because the components are mounted perpendicular to the interconnection surface, this component inductance is in addition to the interconnect inductance, giving a total parasitic inductance on the order of 59 nH.

Another configuration of the unpackaged components is shown in the side view in Fig. 3.9. This layout requires a substrate with multiple layers for interconnection and again uses multiple, parallel wire bonds. The inductance of this layout can be estimated using a one-turn solenoidal approximation, as \( L_s \approx \mu_0 A/W \), where \( A \) is the cross-sectional area of the loop and \( W \) is the conductor width (into the page of Fig. 3.9). The dominant contributions to the area of this loop, and therefore to the inductance, come from the capacitor\(^4\) and the wire bonds. Given typical dimensions

\(^4\)Capacitors are being developed with both polarity terminations made on one end to minimize this loop.
for components, and the thickness of dielectric layers on hybrid substrates, parasitic inductances of less than 5 nH can readily be achieved (with care, as small as 1–2 nH). The disadvantage of this configuration is the additional thermal impedance of the dielectric layer beneath the semiconductor devices.

In many applications, it is necessary to introduce a transformer into the canoni-
cal cell's loop\textsuperscript{5}. Often there are strict spacing and insulation requirements between the primary and secondary windings to meet safety isolation specifications. If so, the transformer's leakage inductance is fairly large (e.g. 100's of nH) and this leakage inductance adds to the parasitic inductance in the canonical cell's loop. Even where it is possible to achieve very good coupling between the primary and secondary windings, small interconnection inductances on the low voltage side become very significant, because they are magnified by the turns ratio squared when referred to the primary. In a 50V to 5V flyback-converter (10:1 turns-ratio), for instance, a 2 nH parasitic inductance on the secondary is equivalent to a 200 nH inductance on the primary side.

3.3.4 Filter Components

The switching converter transfers energy through the canonical cell in pulses. Consequently, filter components are required on both the input and output of the canonical cell to smooth the power flow from the source and to the load. A down-converter with second order input \((L - C)\) and output filters is shown in Fig. 3.10. The input filter is designed to draw a smooth current from the input voltage source, with the capacitor of the input filter stage functioning as the incremental voltage source of the canonical cell. Similarly, the output filter is designed to deliver a steady voltage to the load with the inductor of the filter forming the incremental current source of the canonical cell. These filter elements are the major contributors to the volume and cost of a given converter; as a result, the sizing of these components is a critical part of the overall design.

A detailed, and unnecessarily difficult, approach to this type of filter design is to first express the pulsed waveform, be it current or voltage, in a Fourier series, then to multiply each component in the series by the gain and phase of the filter's transfer function at that frequency, which for these second-order filters can be found from

\textsuperscript{5}Transformer circuits are described in Section 3.4.
Figure 3.10: Down Converter with L-C Input and Output Filters

\[ G(j\omega) = \frac{1}{1 + (j\omega)^2LC} \]  

(3.63)

The filter’s output can be found by summing the resultant series. The filter design process then involves adjusting the value of the capacitance and inductance to achieve the desired ripple.

A simpler approach to sizing the filter components is to deal with the component one at a time. In the output filter of Fig. 3.10, for example, the frequency components of the inductor current can be estimated (neglecting output ripple) as,

\[ i_{Lo}(j\omega) \simeq \frac{v_i(j\omega)}{j\omega L} \]  

(3.64)

where \( v_i \) is the rectangular voltage waveform driving the filter. Similarly, the frequency components of the output voltage can be estimated as

\[ v_o(j\omega) \simeq \frac{1}{j\omega C} i_{Lo}(j\omega) \]

\[ \simeq \frac{v_i(j\omega)}{(j\omega)^2LC} \]  

(3.65)
Comparing (3.63) and (3.65), we see that for \( j\omega \gg LC \) these expressions are essentially identical, and this condition is typically true in practical filter designs. The importance of this simplified approach is that it allows the filter to be designed in the time, rather than the frequency, domain. In the output filter, for example, if the ac component of the rectangular input voltage is integrated over a cycle the ac current ripple can be calculated as 

\[
i_{L_{\text{AC}}} = \frac{1}{L} \int v_{i_{\text{AC}}} \, dt
\]  

(3.66)

and

\[
v_{C_{\text{AC}}} = \frac{1}{LC} \int \int v_{i_{\text{AC}}} \, d^2t
\]  

(3.67)

**Example:** Consider the output filter in the square-wave down-converter, which must filter a square-wave voltage waveform. The average value of the voltage is \( DV_{\text{in}} \), so when the ac component is integrated a triangular current ripple results. The peak-peak value of the current ripple is

\[
\Delta I_L = \frac{V_{\text{in}}(1 - D)DT}{L}
\]  

(3.68)

This triangular ripple current flows in the capacitor, resulting in a quadratic ripple voltage. The peak-peak ripple voltage can be calculated as

\[
\Delta V_C = \frac{1}{LC} \frac{V_{\text{in}}(1 - D)DT^2}{4}
\]  

(3.69)

Similarly, the peak-peak ripple current in the input filter can be calculated as

\[
\Delta I_{\text{in}} = \frac{1}{L_{\text{in}}C_{\text{in}}} \frac{I_o(1 - D)DT^2}{4}
\]  

(3.70)
These expressions show clearly why the filters become smaller with increasing frequency, and also show the effect of the duty ratio on the required amount of filtering.

Given that it is the $LC$ product that is important, there is some latitude in sizing these components, which allows us to introduce other factors such as the relative cost, or size, of inductance versus capacitance. The ability to trade off between the filter components is restricted, however, by the effect of ripple in the first filter component's energy storage on the power circuit. In the output filter of Fig. 3.10, for instance, which filters a rectangular voltage waveform, the filter inductor cannot be sized too small, since excessive ripple in the inductor current increases the rms current of all of the canonical cells components, thereby increasing their dissipation. On the verge of discontinuous operation, when the ripple in the current equals twice the average value, the rms current is increased by a factor of $\sqrt{4/3} \approx 1.15$, so the resistive losses go up by 33%. With a ripple that is half this value (the current going from $0.5I_o$ to $1.5I_o$), the rms current only increases by $\sqrt{13/12} \approx 1.04$, with the resistive losses therefore increasing by 8%. As the ripple gets smaller, the increase in losses from the ideal, no-ripple case become insignificant. With a ripple that is 40% of $I_o$ (from $0.8I_o$ to $1.2I_o$), the rms current increases by less than 1% and the losses go up by only 1.3%.

If the current ripple is too large, there is also the danger of the current waveform going discontinuous, which may complicate control implementation. A large ripple current also has the effect of changing the value of the current during the turn-on and turn-off transitions, with the turn-on current decreasing and the turn-off current increasing. Because the turn-on transition is the lossy transition, this may prove to be advantageous in terms of the overall switching losses, and this issue is explored in more detail in Chapter 8.

If we consider the input filter, which filters rectangular pulses of current, then a filter capacitor that is too small will result in large voltage ripples in the canonical cell. This will increase the off-state voltage stresses of both the diode and the MOSFET, which may mean having to use devices with higher voltage ratings, and
therefore worse $RC$ products. Certainly a high ripple voltage will increase the reverse conduction losses in the diode as this current is highly nonlinear (increasing sharply with voltage). As with the current ripple, voltage ripple in the canonical cell will allow the turn-on and turn-off stresses to be different. Unfortunately, it increases the turn-on stress and decreases the turn-off stress. This is generally a disadvantage because the turn-on transition is the lossy and stressful transition.

### 3.4 Converters with Transformers

In applications that require input-to-output isolation or high voltage conversion ratios, transformers are required. In addition to providing isolation, the transformers also transform the voltage level of the processed energy by the turns ratio of the transformer, $N$, so the impedance level of the energy is transformed by $N^2$. This impedance transformation allows the semiconductor devices to operate with either high-voltage and low-current or low-voltage and high-current stresses, whereas in the basic switching converter the devices are subjected to both high-voltage and high-current stresses.

There are, however, several penalties that result from including the transformer in the converter. One effect is the introduction of an additional parasitic element, the transformer's magnetizing inductance. In the flyback circuit of Fig. 3.12, which is essentially an isolated up-down converter, the magnetizing inductance is consistent with the canonical cell's filter inductance. However, in the forward converter of Fig. 3.11, which is essentially an isolated down-converter, the magnetizing inductance is completely parasitic. In either case, the need to balance the volt-seconds of the magnetizing inductance results in increased off-state voltage stress for the primary side MOSFETs, and for a nominal 50% duty ratio the stress is typically doubled. A second effect is the addition of the transformer's leakage inductance to the parasitic inductance of the canonical cell's loop. A third effect is the magnification of the component and interconnection inductance on the low-voltage side by $N^2$, when referred to the high-voltage side.
Because the MOSFET switches at a higher voltage, the switching losses will generally increase. The higher off-state voltage may also mean that a device with a higher voltage rating must be used. For a fixed die size, the resistance will typically double (at least) in order to achieve twice the voltage rating, as we saw in Table 3.1 [23, p.99]. When compared to a converter without a transformer, however, the conduction losses are lower since the RMS value of the current waveform is inversely proportional to the square root of the duty ratio. For a 50 V–5 V converter, for example, the duty ratio will increase from \( d = 0.1 \) without a transformer to \( d = 0.5 \) with a transformer, so the mean-squared-value of the current, \( I_{rms}^2 \), will decrease by a factor of 5. So even with twice the on-state resistance, the conduction losses will go down by a factor of 2.5. This means that a smaller die size can be used to reduce the sum of the switching and conduction losses.

The addition of the transformer's leakage inductance to the canonical cell's loop can be a problem. If safety isolation is required, the leakage inductance will be significantly larger than the 10–15 nH value we assumed earlier. Not only is more energy dissipated, but the commutation of current during the switch transitions is affected.

In a single-ended forward-converter with a primary side clamp winding (Fig. 3.11), the primary-to-secondary leakage inductance is not a major problem. If the two primary windings were perfectly coupled, there would be no loss of energy. Instead, any energy stored in the leakage inductance is returned to the source through the clamp winding during the MOSFET's off-time. The leakage inductance does have the effect of delaying the commutation of the load current from the free-wheeling diode to the secondary winding, however, so some of the overall conduction period is lost which results in higher device stresses. The leakage inductance between the primary winding and the clamp winding is the parasitic element that must be minimized. Fortunately, these windings do not have to be isolated so, if they are carefully designed and fabricated, the transformer's leakage inductance can be kept quite small.
Figure 3.11: Single-Ended Forward Converter with Clamp Winding

A relatively simple extension of this single-ended converter is one where the clamp winding diode is replaced with a MOSFET and a center-tapped secondary winding is used to achieve a double-ended forward-converter circuit (Fig. 3.12). As in all double-ended converters, this circuit delivers power throughout most of the switching period, thereby reducing the input and output filtering requirements dramatically. It also allows the transformer to operate symmetrically around zero flux, although this requires additional control to balance the volt-seconds applied to the transformer.

Because there is always a path for the output current to flow, the free-wheeling diode is now redundant and the current-source that feeds the output voltage stage can be removed. The leakage inductance is now the only element separating the input and output voltages. It is, therefore, the dominant contribution to load regulation. One positive consequence of this is that, if the leakage inductance can be minimized, the capacitance on the high-voltage primary acts to hold-up the output voltage during load transients.

The turn-off transition of each primary side MOSFET is essentially lossless, just as in the basic switching converter, provided the gate voltage is maintained below
threshold as the drain voltage rises. As the drain voltage of the newly turned off MOSFET rises, charged by the magnetizing current and the load current (which will begin to commutate as the drain voltage exceeds \( V_m \)), the drain voltage of the complementary device falls. Eventually the voltage is clamped by the body diode of the complementary device becoming forward-biased. As long as the MOSFET’s turn-on transition is delayed beyond the point at which this voltage is clamped, the turn-on is essentially lossless.

There are some charging losses on the secondary side, however. The load current begins to commutate from one secondary winding to the other once the polarity of the voltage across the transformer charges. When this voltage is subsequently clamped, the commutation continues. Once the current in the diode which was conducting falls to zero, it is charged to its off-state voltage through a ring with the leakage inductance. Once again, there is both loss and overvoltage stress as a consequence of this resonant charging.

In this double-ended circuit, the input voltage is applied to the primary of the transformer throughout the cycle except for the intervals where the current is commutating from one primary winding to the other. The average rectified voltage
can only be controlled, therefore, by controlling the relative duration of these commutating intervals. These intervals are dependent on the amount of capacitance in parallel with the MOSFETs, the magnitude of magnetizing and leakage inductances, and the magnetizing and load currents. This issue has been studied [24], and schemes devised where load regulation (due to leakage and resistive drops) is compensated for (to first order) by designing the converter to have appropriately shorter commutating intervals as the load current rises. One way to achieve this is to size the commutating capacitance so that the change in commutation time with load current cancels out the effect of load regulation.

Varying the frequency also provides some measure of control. Increasing the frequency reduces the peak magnetizing current, which is the current that flows during the commutation transition. With a lower current, the transition interval is longer and yet the overall period is shorter, so the average output voltage is reduced. The opposite is true if the frequency is reduced. The problem with this type of solution is the undesirability of variable frequency control schemes from the viewpoint of EMI suppression, particularly if a large frequency variation is required. Instead, a pre-regulation or post-regulation stage can be used to correct for variations in both the input and the load, and the double-ended forward-converter can be used for its ability to transform the impedance level of the energy with high operating efficiency. Another possible control technique is to vary the dc level of the magnetizing current, so that the magnetizing current is different for the two turn-off transitions.

This double-ended forward-converter is very similar in operation to lossless H-bridge circuits, which have been developed by a number of researchers [25-28]. The lossless transitions are essentially identical, the difference being that two primary windings are used to halve the number of primary switches (though each one is at twice the voltage), and that the drive is simplified (the MOSFETs have common sources). The ability to apply zero volts to the transformer for some portion of the cycle has been lost, however.
Let us now turn our attention to the flyback converter topology, which is shown in Fig. 3.13. For a nominal 50% duty ratio, the off-state voltage of the MOSFET must be greater than twice $V_{in}$ if the current in the magnetizing inductance is to commutate from the input to the output. The drain of the MOSFET corresponds to node $X$ of the switching converter we discussed earlier. The leakage inductance causes an overvoltage ring with the capacitance of this node, with the ring driven by the load current. For a given leakage inductance, reducing this ringing voltage by adding extra capacitance to the node means incurring increased losses when the node discharges at turn-on. An alternative is to clamp this voltage above $2V_{in}$ to provide the volt-seconds across the leakage inductance. A high-speed clamping device, such as a tranzorb, can be used or, where the leakage energy is sufficiently small, the MOSFET itself can be avalanched.

![Diagram of Single-Ended Flyback Converter](image)

**Figure 3.13: Single-Ended Flyback Converter**

To minimize the input and output filter requirements, two flyback circuits can be used, configured in parallel and operated out of phase. Unlike the forward-converter circuits where the input and output voltages were separated only by the leakage inductance, in the flyback-converter they are now also separated by the magnetizing inductance. Although this inductance can be fairly small, particularly if the converter is designed for discontinuous conduction, the capacitance on the
high-voltage side is not as effective in providing hold-up energy. This has been addressed in the work described in [29], where an additional primary side MOSFET was used to couple the transformer primary to a high-voltage capacitor, while the magnetizing inductance discharged to the secondary.

While the implementation of [29] seems somewhat awkward, it does suggest using an additional winding on the secondary side, at a higher voltage and tightly coupled to the main secondary winding. A possible solution is to use two synchronous rectifiers on the secondary side (Fig. 3.14): one to provide efficient rectification, and the other to couple the output to a high-voltage hold-up capacitor through a tightly coupled winding.

![Diagram of secondary side synchronous rectification](image)

Figure 3.14: Secondary Side Synchronous Rectification

### 3.5 Synchronous Rectification

*Synchronous rectification* is a technique that is often referred to as the solution to high rectification losses. The basic principle is to replace a junction rectifier with a controlled switch, and to gate the switch so that it is conducting whenever the diode would have conducted [30]. The intention is to reduce the rectification losses by achieving a lower voltage drop across the controlled switch than appeared across the sum of the junction and resistive drops of the rectifier that it replaced. The
controlled switch that is generally considered for high-frequency applications being the power MOSFET.

The synchronous rectifier is required to block reverse voltages. Therefore, if a power MOSFET is used it must be configured so that when it conducts, the current flows from source to drain, as shown in Fig. 3.15a. Otherwise the MOSFET’s body diode, which is in parallel with the device, will provide a conducting path for reverse currents.

![Diagram of synchronous rectifier](image)

(a)

![Diagram of gate drive circuit](image)

(b)

Figure 3.15: Synchronous Rectifier

The gate drive for a power MOSFET synchronous rectifier can be derived in a number of ways, with one simple method being a drive circuit, driven by a comparator that senses the polarity of the applied voltage, as shown in Fig. 3.15b. As
the MOSFET's body-diode becomes forward biased the comparator senses this positive voltage and gates the MOSFET on. Similarly, as the current, and therefore the MOSFET's source-drain voltage, falls to zero and attempts to go negative, the comparator senses this and turns the device off. This technique is fine for low-frequency applications but is problematic with increasing frequency because delays in the circuitry cause the MOSFET to turn on and off after the rectifier voltage changes sign.

If the MOSFET is not turned on when it first becomes forward-biased, its body-diode will begin to conduct, and this diode current will subsequently transfer to the MOSFET when it turns on. The only deleterious effect is that the losses are somewhat higher as the rectifier drop is the body-diode drop for a while. Delay at the turn-off transition is more critical, however, as if the MOSFET remains conducting for any appreciable time after the drain-source voltage has reversed sign large reverse currents will flow and energy will be removed from the rectified output. Some of this energy will be stored in whatever parasitic inductance is in series with the rectifier and so will cause overvoltage ringing with the synchronous rectifier's output capacitance when the MOSFET finally turns off.

It is imperative for the implementation of high-frequency synchronous rectification that the gate drive waveforms fall within the desired forward conduction period. The MOSFET's body-diode can then be used to conduct at the extremes of the conduction period. This imposes a condition on the body-diode, namely that it have good forward and reverse recovery characteristics, that is not satisfied by the devices that are currently commercially available. In fact to operate as 1–10 MHz rectifiers the body-diodes require recovery times on the order of nanoseconds, compared to the 100's of nanoseconds of the available devices. The experimental device that is described in Section 6.2.2 is being developed to meet these recovery criteria.

One alternative to using the MOSFET's body-diode for conduction at the ends of the cycle is to use a Schottky diode in parallel with the device. In addition to
possessing adequate speed for this application, the Schottky has the advantage over
the body-diode of a lower junction drop, and so improved efficiency. However, there
are several disadvantages; the first is that the total rectifier capacitance, which is
one of the device parasitics whose effect on the power topology we have discussed
in detail, is increased. The second disadvantage is that to be effective at high
frequencies the Schottky may have to be integrated with the MOSFET, which entails
considerably more complex and expensive processing. If it is not integrated, the
parasitic inductance in the loop of a discrete MOSFET and discrete Schottky will
impede current transfer and may prevent this transfer in the required time.

Consider, for example, a parasitic inductance as small as 1–2 nH which could
be achieved in a hybrid assembly, though with considerable effort. In a 50 W, 5 V,
interleaved supply with 0–20 A sawtooth output current waveforms, the transfer of
current from the Schottky to the MOSFET, when the MOSFET turns on, would be
quite rapid as the current is low at the beginning of the conduction interval. Near
the end of the cycle, however, when the MOSFET turns off, it would require 20–40
nano-volt-seconds across the leakage inductance to transfer the 20 A of current from
the MOSFET to the Schottky.

If, in this example, we were attempting to improve on the rectification efficiency
of a 0.35 V Schottky operating at 50% duty-cycle at 10 MHz, then the total rectifier
volt-second product we would be trying to improve on is 175 nano-volt-seconds. The
20–40 nano-volt-seconds devoted to the inductance is fairly significant on this scale,
and represents a potential loss that could be avoided by integrating the Schottky
contact with the MOSFET. This example also serves to illustrate the point that the
critical issue in this current transfer process between a synchronous rectifier and a
parallel diode is the value of the current when the MOSFET rectifier turns on and
off.
3.5.1 Comparing Total Losses

The resistance of the synchronous rectifier MOSFET is inversely proportional to the die area, so irrespective of the Schottky rectifier's forward voltage drop, a MOSFET can be found that will have a lower conduction loss. As the die size increases, however, so does the capacitive energy, which includes the gate drive energy, the energy stored in the MOSFET's output capacitance, and energy lost in the power circuit in charging and discharging this capacitance. As the frequency increases the capacitive energy losses will eventually negate the savings in conduction loss. Therefore, for a given MOSFET process and available Schottky rectifier technology, there is generally a break-even frequency above which synchronous rectification can only be beneficially employed in conjunction with either lossless gate drive techniques, or by using a converter topology with lower rectifier-capacitance losses.

In a square-wave converter, the total losses in a Schottky rectifier are (as in Section 3.3.2),

\[ P = I_{ave}V_{rect} + I_{rms}^2R_d + V_{off}I_r + \frac{2}{3}V_{off}Q_d(V_{off})f_{sw} \]  \hspace{1cm} (3.71)

where \( I_{ave}, I_{rms}, V_{off}, \) and \( f_{sw} \) are determined by the application, the topology, and the loading, while \( V_{rect}, R_d, \) and \( Q_d(V_{off}) \) depend on the characteristics of the Schottky process and the die size (which is chosen to minimize the loss).

Similarly, the total losses in a MOSFET applied as a synchronous rectifier in a square-wave converter are

\[ P = I_{rms}^2R_{DS-on} + \frac{2}{3}V_{off}Q_f(V_{off})f_{sw} + Q_{gate}V_{gate}f_{sw} \]  \hspace{1cm} (3.72)

where \( R_{DS-on}, Q_f(V_{off}), \) and \( Q_{gate}V_{gate} \) are dependent on the characteristics of the MOSFET process and the die size chosen.
Example: In a 1 MHz, 50 W, 5 V output, dual forward converter circuit at full load the rectifiers are required to carry 50% duty ratio sawtooth current waveforms with a peak current of 20 A. The currents and voltages can be calculated as $I_{\text{ave}} = 5 \text{ A}$, $I_{\text{rms}} = \frac{20}{\sqrt{2}} \approx 8.2 \text{ A}$, $V_{\text{off}} = 10 \text{ V}$. If we consider the USD900 series of Schottky rectifiers for this application [31, pp. 4:153-4:154], we find that at 125°C these devices have $V_{\text{rect}} = 0.3 \text{ V}$, $R_d = 100 \text{ mΩ}$, $I_r(10 \text{ V}) = 15 \text{ mA}$ and $Q_d(10 \text{ V}) = 28.3 \text{ nC}$. If a single die is used, the four dissipation terms of (3.71) can be calculated as 1.5 W, 6.7 W, 0.15 W, and 0.2 W respectively. This die area is far from optimal, since the resistive loss is more than ten times greater than the sum of the reverse conduction and capacitive losses, which are both proportional to area. Using (3.45) we can calculate the optimum area as

$$A_{\text{min}} = A_2 \sqrt{\frac{6.7}{0.35}} = 4.4 A_2$$

and the area dependent portion of the power dissipation will have a minimum of (from (3.46)),

$$P_{A_{\text{min}}} = 2(K_2 A_2) \frac{A_{\text{min}}}{A_2} = 3 \text{ W}$$

If we use 4 of the basic USD900 dies, the area-dependent power dissipation will be, from (3.46), within 0.5% of this 3 W value, and the total loss caused by each Schottky rectifier will be 4.5 W, a very significant fraction of the 50 W output power.

Let us now examine the losses in this application of a synchronous rectifier using a standard commercial 50 V MOSFET process, such as that used to fabricate the BUZ10 [32, pages 102-107]. The device parameters are $R_{DS_{\text{on}}} = 0.85 \text{ mΩ}$, $Q_f(10 \text{ V}) = 17.4 \text{ nC}$, and $Q_{\text{gate}}(10 \text{ V}) = 21.3 \text{ nC}$. For a single BUZ10 die the loss components can be calculated from (3.72) as 5.7 W, 0.12 W, and 0.21 W respectively. The optimum area can be calculated from (3.45) as
\[ A_{\text{min}} = A_2 \sqrt{\frac{5.7}{0.33}} = 4.16 A_2 \]  

(3.75)

and the minimum loss can be calculated as

\[ P_{A_{\text{min}}} = 2(K_2 A_2) \frac{A_{\text{min}}}{A_2} = 2.75 W \]

(3.76)

If 4 BUZ10 dies are used, the total dissipation due to each synchronous rectifier will be 2.75 W as compared to the 4.5 W of loss due to the USD900 Schottky rectifiers. So based solely on losses, without considering the additional cost and complexity of implementation, the synchronous rectifier approach is preferable for this particular application.

This example brings out several important points. The first is that with low forward voltage drop Schottky rectifiers the losses due to reverse conduction are comparable to the capacitive losses in the 1 MHz range. The reverse conduction current increases sharply with reverse voltage, so this can be a dominant source of loss in a resonant topology where the voltage stresses are typically higher. The reverse current is also a strong function of temperature, increasing with increasing die temperature, but the effect this has on the total dissipation is balanced somewhat by a decreasing \( V_{\text{rect}} \) as the temperature increases. In this example, the total dissipation in each Schottky would be about 4.25 W at 25°C compared to the 4.5 W at 125°C. If the reverse conduction is a major problem in a resonant topology it motivates additional effort in the thermal packaging to keep the die temperature down. The other point is that the synchronous rectifier's losses are increasing faster with frequency than the Schottky's. For this converter topology and these particular device processes, the break-even frequency is approximately 5 MHz. For synchronous rectification to be viable above this frequency range either a different topology would have to be used or loss-less gate drive techniques employed. Given that the goal is to reduce the rectification losses, improved device technologies are required, both for Schottky rectifiers and for low voltage MOSFETs that can be
applied as synchronous rectifiers.
Chapter 4

Resonant and Quasi-Resonant Converters

This chapter examines high-frequency resonant power conversion, particularly the ability of resonant conversion to overcome the limitations of square-wave conversion caused by the device and layout parasitics, as described in Chapter 3. After reviewing the basic principles behind resonant conversion, the discussion focuses on the quasi-resonant converter family. The attributes of this converter family are discussed and its disadvantages raised, specifically the inability to accommodate one of the parasitic device capacitances, and also the effect of load variation on the device stresses.

The results of an analytic comparison between the square-wave and quasi-resonant approaches, based on total losses, is then presented. Using data from commercially available semiconductor devices, conservative estimates are given for the switching frequency at which the resonant approach becomes advantageous. The chapter concludes with an examination of the Quasi-Resonant Flyback Converter, which has been vigorously promoted by some researchers for point-of-load supply applications.
4.1 Resonant Converters

In the discussion of the square-wave switching converter in Chapter 3, it became clear that the voltage and current stresses during the turn-on transition were the major source of switching loss. Consequently, resonant switching has been employed in high-frequency converter circuits to allow the power MOSFET to operate with either zero-current or zero-voltage switching transitions [33–36]. These resonant converters use second-order \( L-C \) tank circuits to control the rate of rise of the switch voltages and/or currents. Ideally, the very circuit parasitics that limited the square-wave converter's performance are incorporated into the resonant tank, and at sufficiently high frequencies, the circuit parasitics can themselves be the tank elements.

Figure 4.1a shows a simple resonant dc-ac inverter which uses switches to apply a square-wave of voltage across a series resonant \( L-C-R \) circuit (with the resistor being the load). If the switching frequency equals the tank's resonant frequency and if the \( Q \) is sufficiently high, then the fundamental component of the square wave appears across the resistor and the harmonics appear primarily across the inductor. This results in an approximately sinusoidal load current, in phase with the applied voltage, as shown in Fig. 4.1b. This current can be rectified and filtered to achieve dc-dc conversion.

Because the switch current is zero at the switching instants, the load-dependent switching losses are minimal. However, there are still losses associated with charging and discharging the parasitic device capacitances during the switching transitions, as the semiconductor devices are subjected to step changes in voltage. These losses can be avoided by switching at zero-voltage, instead of zero-current, using a converter that is the dual of the circuit of Fig. 4.1a\(^1\). By avoiding the capacitive losses, this converter is able to operate very efficiently at very high frequencies as has been demonstrated in [38, 39].

\(^1\)This is a current-mode [37] as opposed to voltage-mode converter, using a parallel \( L-C-R \) instead of a series \( L-C-R \) load.
Figure 4.1: Voltage Source Resonant Converter

The zero-current or zero-voltage transition is the strength of the resonant converter. The penalty is that both the peak and rms value of the current through the switches (series L-C-R), or the voltage across the switches (parallel L-C-R) are higher than in a square-wave converter, resulting in higher conduction losses and increased filtering requirements. Further, in satisfying the high $Q$ requirement, considerably more energy is stored in the reactive elements than is transferred to the load each cycle. In general this means that a classical resonant converter can be constructed to run with comparable efficiency to a square-wave converter at elevated frequencies [40–42] but without achieving any significant advantages in terms of power conversion density over the lower frequency square-wave design. This argument has been raised with respect to recent research efforts in [43].

The power flow in a resonant converter is controlled by varying the switching frequency. For example, in the circuit of Fig. 4.1 the impedance of the tank circuit increases as the frequency is moved away from resonance, and so the load current
is reduced. The farther the switching frequency is moved from resonance, the less power is delivered to the load. Unfortunately, away from resonance, the load current is no longer in phase with the square-wave voltage, so switching no longer occurs at zero current. This can be remedied by using a discontinuous mode of operation: turning a switch on, allowing a half-cycle ring, B then turning the switch off at zero current prior to turning the complementary switch on. Similarly, in a zero-voltage topology the switch is turned off for a half cycle voltage ring. By varying the delay between the end of one ring and the start of the next, the average power delivered to the load is controlled.

Single-ended resonant topologies that operate in the discontinuous mode with rectified loads have come to be called “quasi-resonant converters” [6, 44, 45], and have received considerable attention in recent years as candidate topologies to carry conversion circuitry to new levels of density and efficiency. The remainder of this chapter addresses these topologies, focusing in particular on the comparison between these converters and the conventional square-wave switching converters of Chapter 3.

4.2 Quasi-Resonant Converters

As we concluded above, the dc-dc converter family that is commonly termed quasi-resonant is essentially composed of single-ended resonant converters that operate discontinuously with rectified loads. In examining their operation, however, it is more convenient to think of the quasi-resonant converter as a modification of the basic square-wave converter, which is the development presented in references [44, 45]. The modification calls for a resonant inductor to be placed in the canonical cell's loop and a resonant capacitor placed in parallel with either the controlled switch (MOSFET) or the diode of the square-wave converter. This change can be made to all of the dc-dc converter configurations, with essentially identical results, so we will restrict our discussion here to the quasi-resonant down-converter.
Before discussing the operation, it is first necessary to recognize that there are two possible topological variations for the down-converter alone. Figure 4.2a shows the converter with the resonant capacitor placed in parallel with the MOSFET, and Fig. 4.3a shows the converter with the capacitor placed in parallel with the diode\(^2\). In both cases some, if not all, of the resonant capacitor is supplied by the parasitic capacitance of the device that the resonant capacitor is in parallel with, making that parasitic an integral part of the converter.

### 4.2.1 Ideal Operation

Operating waveforms for the zero-voltage quasi-resonant converter are shown in Fig. 4.2b. The analysis is idealized in that parasitic elements are neglected and the resonant components are assumed to be linear. Starting with the MOSFET on, delivering power to the load, the operation throughout the cycle can be explained as follows. When the MOSFET turns off, the load current, which had been flowing through the MOSFET’s channel, commutates to the parallel capacitance, \(C_r\). The current charges the capacitor, whose voltage increases linearly. When the voltage across the MOSFET reaches the level of the input voltage, the free-wheeling diode becomes forward biased, clamping the voltage of node \(X\) at zero. Since the resonant inductor, \(L_r\), still carries the full load current, a resonant ring follows between the resonant inductor and the MOSFET’s capacitance. The MOSFET capacitance’s voltage rings around \(V_{in}\) and the resonant inductor’s current rings around zero. The ringing component of the capacitor’s voltage is

\[
V_r = I_o \sqrt{\frac{L_r}{C_r}}
\]  

and the frequency of the resonance is

\(^2\)These two topologies correspond to the voltage-mode and current-mode resonant converters discussed previously, and are commonly referred to as zero-voltage and zero-current quasi-resonant converters, respectively.
\[ \omega_r = \frac{1}{\sqrt{L_r C_r}} \]  

(4.2)

If the resonant components are sized so that at the rated load current \( V_r = V_{in} \), then the resonant capacitor's voltage and the resonant inductor's current both ring to zero after three-quarters of a resonant period, as shown in Fig. 4.2. The MOSFET can be turned on at this point, with a zero-voltage, and therefore essentially lossless, switch transition. Once the MOSFET turns on, the current in the resonant inductor ramps up linearly until it equals the load current, at which time the free-wheeling diode turns off. We will discuss the diode's turn-off transition in more detail later, particularly the effect of the device's parasitic capacitance.

The ideal operation of a zero-current quasi-resonant converter is quite similar to the zero-voltage converter, as the ideal waveforms of Fig. 4.3b show. In this case the resonant action is initiated by the MOSFET turning on. Once the MOSFET is on, the full input voltage is across the resonant inductor, so the current, \( I_{L_r} \), increases linearly. When the current equals the load current, the free-wheeling diode turns off, and a ring ensues between the resonant inductor and the capacitance that is in parallel with the diode. The resonant capacitor's voltage rings around \( V_{in} \), with a magnitude of \( V_r = V_{in} \), and the resonant inductor's current rings around \( I_o \), with the magnitude of the ring being

\[ I_r = V_{in} \sqrt{\frac{C}{L}} \]  

(4.3)

If the resonant components are sized to give \( I_r = I_o \) at the rated load, then after three-quarters of a resonant cycle the resonant current rings to zero and the resonant capacitor's voltage is at \( V_{in} \). The MOSFET can be turned off at this point with both zero-current and zero-voltage stresses. Once the MOSFET is off, the load current linearly discharges the resonant capacitance. This discharge continues until the diode clamps the voltage of node \( X \) at zero volts and picks up the load current.

The resonant inductor includes any parasitic inductance in the canonical cell's
Figure 4.2: Zero-Voltage Quasi-Resonant Converter
Figure 4.3: Zero-Current Quasi-Resonant Converter
loop, and the resonant capacitor includes the capacitance of the device it is in parallel with. So both types of quasi-resonant converter incorporate two of the three parasitic reactances of the square-wave converter examined in Chapter 3. While the two converter circuits have been characterized as zero-voltage and zero-current types, both here and in the literature, this is somewhat misleading. The waveforms of Figs. 4.2 and 4.3 show that both circuits operate with both types of transition. The difference is in which semiconductor device experiences the zero-voltage, and which experiences the zero-current, transition. In the circuit of Fig. 4.2, the MOSFET has the zero-voltage transition and the diode has the zero-current transition, whereas in the circuit of Fig. 4.3, the opposite is true.

4.2.2 Effect of Additional Parasitic

The semiconductor device that has the zero-current switch transitions has one transition in which its voltage makes a step change. In the zero-current converter this occurs for the MOSFET when it turns on, and in the zero-voltage converter it occurs for the diode when its current falls to zero and it turns off.

Because the MOSFET's current is zero when it turns on in the zero-current converter, there are no load-dependent losses. The MOSFET turns on, however, with the same drain-source voltage as it has in a square-wave converter, so the switching losses from discharging its own output capacitance persist. The rms current is higher in the resonant circuit, so to achieve comparable conduction losses the MOSFET chosen will typically have a larger device capacitance than its counterpart in the square-wave converter. The MOSFET capacitive switching loss at turn-on is, therefore, generally greater in a zero-current quasi-resonant design than in a square-wave design.

In the zero-voltage converter, the resonant capacitor is in parallel with the MOSFET, so the MOSFET's capacitive switching losses are avoided. Instead, the troublesome parasitic is the capacitance of the diode. The step change in diode voltage when it turns off can have several effects. The first is that the diode's capacitor
charges through the resonant inductor which, since the damping is low, causes the diode voltage to ring to twice \( V_{in} \), as shown in Fig. 4.4. This increased stress requires a diode with a higher voltage rating, which results in increased diode conduction losses. Meanwhile, if the ring is damped out as shown in Fig. 4.4a, energy is lost in charging the diode, just as in the square-wave converter. (If the same die size is used for the diode, the energy loss will be identical.)

The second effect occurs if the diode’s capacitance is substantial compared to the main resonant capacitor. If so, the parasitic oscillation may not decay before the next switch transition. The simulation waveforms in Fig. 4.4b show what happens in such a case. Although it may seem desirable that the oscillation energy not be lost, any energy that remains in the oscillation when the MOSFET subsequently turns off impacts the entire circuit operation. It may cause the MOSFET to no longer have a zero-voltage turn-on transition, as shown in Fig. 4.4b. Furthermore, because the input-to-output voltage conversion ratio is determined by the average voltages across the semiconductor elements, this ratio becomes extremely sensitive to load variations. To avoid this condition, the oscillation can be damped by adding a series R-C in parallel with the diode. Unfortunately, the capacitance in series with the required damping resistance incurs additional dissipation, since it is charged in the same manner as the rectifier.

Whether the parasitic ring decays or not, it is a potential source of radiated EMI because the oscillating current flows around the canonical-cell’s loop. The resulting high-frequency magnetic field must be shielded, not only from areas external to the converter, but also from sensitive internal areas such as high-impedance analog nodes in the sensing and control circuitry. While the same problem exists in the square-wave converter, every effort is usually made there to minimize the area, and thereby the inductance, of the canonical cell’s loop. This is not so easily done in the quasi-resonant application due to the addition of the explicit resonant inductor.
Figure 4.4: Step-Change in Diode Voltage
4.2.3 Load Dependence

In the ideal converter described above, the resonance was set to allow benign switch transitions while minimizing the device voltage and current stresses. In the case of the zero-voltage converter the ringing voltage equalled the input voltage, and in the zero-current converter the ringing current equalled the load current. Thus, the waveforms of Figs. 4.2 and 4.3 correspond to the situation where the characteristic impedance of the resonant elements exactly equals the ratio $V_{in}/I_o$. Equivalently, the "optimal" load current in both cases is

$$I_{opt} \simeq \frac{V_{in}}{\sqrt{L_c/C_r}}$$  \hspace{1cm} (4.4)

Unfortunately, as the load current changes, so does the circuit's operation. For example, if the load current in a zero-voltage converter is less than the optimal current, the MOSFET's drain-source voltage will not ring back to zero before it begins to rise again. Therefore, the MOSFET will be forced to undergo a step change in its voltage at turn-on, as shown in Fig. 4.5a. The drain-source voltage at turn-on is lower than in the square-wave converter, so the energy stored in the MOSFET's capacitance is not as large. However, the energy stored in any external resonant capacitance which has been added will also be dissipated.

A load current that is higher than the optimal value will increase the peak MOSFET voltage. Generally this means a higher device rating, which will result in increased conduction losses. For a specified range of operating load current, a compromise must be made between the device's off-state voltage and an acceptable level of turn-on voltage.

As an example of how significant the turn-on loss can be, consider a converter that is designed for a load current which varies from half the rated load current, $0.5I_o$, to one and a half times the rated load current, $1.5I_o$. If the resonant elements are chosen to give the optimal waveforms at the maximum current, then the value
of the resonant capacitor will be

\[ C_r = \frac{1}{\omega_r} \left( \frac{1.5I_o}{V_{in}} \right) \approx \frac{3}{8\pi} \left( \frac{I_o}{V_{in}} \right) \frac{1}{f_s} \] \hspace{1cm} (4.5)

When the converter is operated at its rated load, \( I_o \), the amplitude of the voltage ring is only two-thirds of \( V_{in} \), so the MOSFET will have a step change in voltage at turn-on of \( V_{in}/3 \). The energy lost per cycle can be expressed as

\[ E = \frac{1}{2} C_r \left( \frac{V_{in}}{3} \right)^2 \] \hspace{1cm} (4.6)

which can be rewritten using (4.5) as
\[ E = \frac{1}{24\pi} \left( \frac{V_{in}I_o}{2} \right) \frac{1}{f_s} \]  

(4.7)

and for an effective duty ratio of 0.5 (so that \( V_o \approx 0.5V_{in} \)), this can be rewritten as

\[ E = \frac{1}{24\pi} \left( \frac{P_o}{f_s} \right) \]  

(4.8)

which is 1.3% of the rated power, regardless of frequency.

If the load current is reduced to half the rated load current, the step change in the MOSFET's turn-on voltage is two-thirds of \( V_{in} \), and the corresponding loss is approximately 5% of full power (which is 10% of operating power at \( I_o/2 \)).

An alternate design approach is to set the characteristic impedance so that \( I_{opt} \approx 0.5I_o \). With a load current higher than \( I_{opt} \), the MOSFET voltage will attempt to ring negative, but is prevented from doing so by the body diode of the MOSFET. This would result in a maximum voltage of \( 4V_{in} \) at \( 1.5I_o \), dictating a device with at least twice the conduction resistance.

In the zero-current converter the problem is reversed. If the load current is greater than \( I_{opt} \), the MOSFET current does not return to zero at the end of its resonant ring, as Fig. 4.5b shows. Besides the switching stress that results when the MOSFET is turned off under this condition, there is additional energy to drive the ring between the resonant inductor and the junction capacitance of the MOSFET when the MOSFET turns off. The amplitude of the ring will be greater, which may increase the MOSFET's voltage rating. Further, the energy stored in the resonant inductor at the beginning of the ring is either lost, if the ring decays or, if it doesn't the operation of the circuit will be detrimentally affected, as it was in the case of the undamped ring in the zero-voltage converter described in Section 4.2.2.

Given these problems for the zero-current converter, one is typically forced to size the resonant elements for the largest load current expected. While this approach avoids the step-change in current at the turn-off transition, it does increase the
resonant energy and therefore the circulating current that the MOSFET has to carry. This substantially increases the conduction losses in the MOSFET.

4.2.4 Current Waveform Parameters

In the zero-voltage and the zero-current converters, the maximum voltage stress of both the MOSFET and the diode can be at least twice $V_{in}$. The on-state resistance of these components is, therefore, higher than it would be in a square-wave converter, assuming the same die size is used. As for the currents, under the optimal conditions of Figs. 4.2 and 4.3, the average current through both devices is the same as in a square-wave converter. For the device that is off during the resonance (the MOSFET in the zero-voltage and the diode in the zero-current), the rms currents are nearly identical in the two cases. However, the device that is conducting during the resonance has a mean-square current that is approximately 50% higher than in the square-wave converter.

4.2.5 Gate-Drive Power

One important advantage of any zero-voltage resonant converter is the reduced gate-drive power that results. This occurs because the Miller feedback charge is not supplied by the gate drive circuit's power supply. Instead, this charge is removed from the drive's negative supply as the drain voltage rings up and is returned to the same supply as the voltage rings back down. Another way to think of this is that when the drive's pull-up device is activated to turn the MOSFET on, the Miller charge is already 'on' the gate, so the gate drive power is reduced. This typically halves the gate drive loss.
4.2.6 Summary of Tradeoffs Associated with Quasi-Resonant Converters

The square-wave converter was seen in Chapter 3 to have switching losses associated with the energy stored in the junction capacitances, the time required to turn the MOSFET on, and the energy stored in the parasitic inductance. The quasi-resonant converter, operated at its optimal load, avoids the turn-on transition losses, the inductor energy losses, and one of the junction capacitor energy losses. The minimum penalty for using the quasi-resonant rather than the square-wave converter is a doubling of the voltage ratings of both semiconductor devices, causing higher conduction losses if the same die size is used. Further, if the power circuit's operating condition changes, then the transitions are no longer benign unless an additional penalty in the off-state voltage is accepted.

The quasi-resonant approach also shares many of the disadvantages of conventional resonant techniques when compared to fixed-frequency square-wave conversion. These are, increased circuit complexity, additional filtering requirements, and variable frequency control. The variable frequency control is not so much a problem of implementation (though it is certainly not as elegant as PWM control), but more a problem of achieving adequate EMI suppression, when the frequency is both unknown and changing over a wide range.

4.3 Comparison Between Quasi-Resonant and Square-Wave Converter

Without considering the costs associated with the increased complexity of the quasi-resonant converters due to the resonant elements and the variable frequency control, one can, simply by equating losses, make an estimate of the change-over frequency below which square-wave switching is more efficient than quasi-resonant switching. To do so requires assumptions that may not be valid in every application, and which are dependent on the characteristics of available components. Just such an analytic
comparison was performed as part of this thesis, using the present generation of MOSFETs and Schottky diodes to compare the square-wave converter with the zero-voltage quasi-resonant converter. This work was reported in detail in [7].

The study was based on available data for the five standard MOSFET die sizes, and accounted for all of the loss mechanisms discussed in this and the preceding chapter. The MOSFET's conduction loss in the square-wave converter was set equal to 1% of the power ($R_{ds}I_o = 0.01V_{in}$), and the input voltage was set equal to 80% of the device rating to allow for the square-wave converter's parasitic overvoltage ring at turn-off. This resulted in the relationship between die size, voltage rating, and converter power (or current) shown in Table 4.3.

If the square-wave converter operating at full load is compared to the quasi-resonant converter operating optimally at the same load, the change-over frequencies at which the saved switching losses equal the additional conduction losses shown in Table 4.3 result. The change-over frequency is quite high for the low power applications, as expected, because of the relatively low load-dependent switching losses in the square-wave converter and the additional energy associated with the resonant action in the quasi-resonant circuit.

A further comparison was made between the square-wave converter and a quasi-resonant converter designed to operate optimally with a 50% overload in $I_o$, as described in Section 4.2.3. As expected, the change-over frequencies moved up, which is shown in Table 4.3. If the quasi-resonant converter were instead designed for the wider load range of $0.5I_o$ to $1.5I_o$, then the increase in change-over frequency at $I_o$ would be approximately four times greater (1.3% additional loss to 5% additional loss).

In the above study a constant value of $L_p$ was used. As the current increases, therefore, the change-over frequency drops because the energy lost in the parasitic inductance becomes a dominant component of the square-wave converter's switching loss. At these higher power levels the converter could instead be implemented with
multiple canonical cells, composed of smaller devices. This effectively lowers $L_p$, and therefore decreases the energy lost, though at the expense of additional fabrication complexity. This is another argument for modularity, based purely on parasitics and efficiency, to add to the arguments made in Chapter 1.

It should also be noted that while in the square-wave converter design the die size is chosen to minimize the sum of the conduction and switching losses, one is free in the quasi-resonant converter to use a larger die (or parallel devices) to minimize the conduction losses. There are limits, however; the total device capacitance cannot exceed the desired resonant capacitance, eventually savings in conduction loss will be offset by increased gate-drive energy (and losses), and of course there are economic considerations, since the larger devices are more expensive.

4.4 Quasi-Resonant Flyback Converter

One particular application where the quasi-resonant converter has received considerable attention is for dc-dc conversion with transformer isolation [46], specifically aimed at the distributed power supply application outlined in Chapter 1. The advantage of the quasi-resonant technique in this application is the simplicity of the zero-voltage quasi-resonant flyback converter, which is shown in Fig. 4.6. The transformer’s leakage inductance is utilized as the converter’s resonant inductor, and the transformer’s magnetizing inductance is utilized as the canonical cell’s filter inductor. While it does not require the addition of explicit resonant components, the converter has the same drawbacks as a square-wave flyback circuit, namely the magnetizing inductance appearing between the primary and secondary voltage sources, in addition to the drawbacks of the quasi-resonant circuits.

This converter has the load dependence problems we discussed in Section 4.2.3, and the operating frequency must change over a wide range to control the output voltage. The problems associated with the rectifier capacitance in the zero-voltage converter are mitigated in this converter by the effect of the transformer’s turns-
ratio, since the rectifiers are on the low-voltage secondary and so are quite small when referred to the primary. The high-frequency oscillation that occurs when the diodes turn off is still a source of noise, however, and while the energy involved in the ring is reduced, the path of the high-frequency current is through the transformer and so is an important EMI concern. Furthermore, present and future efforts to use lower-voltage Schottkys and synchronous rectifiers to improve the efficiency of low voltage rectification, will bring the rectifier capacitance problem back into focus as the rectifier's capacitance will probably increase dramatically.
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<th>2</th>
<th>3</th>
<th>4</th>
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<td>$P_o$</td>
<td>$I_o$</td>
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</tr>
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Table 4.1: Current and Power for each MOSFET Die

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<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
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<td>1</td>
<td>($\text{MHz}$)</td>
<td>2</td>
<td>($\text{MHz}$)</td>
<td>3</td>
</tr>
<tr>
<td>80</td>
<td>3</td>
<td>2.2</td>
<td>1.1</td>
<td>.72</td>
<td>.34</td>
</tr>
<tr>
<td>160</td>
<td>3.2</td>
<td>1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>.88</td>
</tr>
</tbody>
</table>

Table 4.2: Change-Over Frequency (Optimal Load)

<table>
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<tr>
<th>$V_{\text{in}}$ ($\text{volts}$)</th>
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<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>($\text{MHz}$)</td>
<td>1</td>
<td>($\text{MHz}$)</td>
<td>2</td>
<td>($\text{MHz}$)</td>
<td>3</td>
</tr>
<tr>
<td>80</td>
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<tr>
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<td>2.8</td>
<td>2.2</td>
<td>1.8</td>
<td>1.2</td>
</tr>
</tbody>
</table>

Table 4.3: Change-Over Frequency (Light Load)
Chapter 5

A High-Frequency, Low-Volume, Point-of-Load Power Supply

This chapter begins by introducing a high-frequency converter topology, the Resonant Forward Converter. This converter uses a transformer and operates with a combined square-wave switching and resonant nature, much like the Quasi-Resonant Flyback converter, but has several distinct advantages for a point-of-load supply application. It incorporates two of the parasitic reactances of the canonical cell in its basic operation, just as the quasi-resonant circuit does, but because it utilizes both of the device capacitances, it avoids the charging losses of the quasi-resonant circuit. Also in contrast to the quasi-resonant converter, its operation is substantially independent of load variations. Another advantage of the Resonant Forward Converter is that its fundamental performance is based on fixed-frequency operation.

The resonant forward converter has two disadvantages. The first is that it has no basic regulation mechanism, so it must be used in conjunction with other regulating power stages if regulation is required. The other disadvantage is that the unused, and therefore undesirable, parasitic reactance is the inductance of the canonical cell, which includes the leakage of the transformer. The need to minimize this parasitic tends to restrict the converter to applications that do not require safety isolation between primary and secondary windings, so that tight coupling through the transformer can be achieved.
After discussing the converter's basic operation, this chapter proceeds to describe the development of an experimental point-of-load supply based on this topology. This development included the interleaving of out-of-phase converters to achieve continuous power flow between primary and secondary. Also, a pre-regulation stage, that was merged with the main converter to reduce device stresses and losses, was added. Experimental results are presented from a converter constructed with standard components and assembled using PCB\textsuperscript{1} technology. The chapter concludes by motivating subsequent developments for the converter, with the relevant results to date presented in the following chapters.

5.1 A Resonant Forward Converter

5.1.1 Ideal Operation

The basic form of the circuit discussed throughout this chapter is shown in Fig. 5.1a. This topology is that of a single-ended forward converter, without the transformer reset clamp circuitry of Section 3.4, to which a resonant inductor and capacitor have been added. Consequently, it is referred to as a resonant forward-converter.

The resonant inductor is in parallel with the transformer, and so can be naturally supplied by the magnetizing inductance of the transformer; the resonant capacitor is incrementally in parallel with both semiconductor devices (neglecting leakage inductance), and so incorporates both device capacitances.

The basic operation of the resonant forward-converter is shown by the waveforms of Fig. 5.1b. While the MOSFET is on, the transformer delivers the load current from the primary to the secondary, where it is supplied to the output through the rectifying diode. The MOSFET's current consists, therefore, of the load current plus the current in the 'magnetizing', or 'resonant' inductor. The magnetizing current, $I_{Lr}$, ramps up linearly during this time, as shown in Fig. 5.1.

\textsuperscript{1}Printed Circuit Board
(a) Ideal Converter Topology

(b) Ideal Waveforms

Figure 5.1: Resonant Forward Converter
When the MOSFET turns off, whatever current it was carrying commutates to its parallel capacitance, $C_f$, causing the drain voltage to rise. Since the MOSFET and the rectifier on the secondary are incrementally in parallel, the same rising voltage reverse biases the rectifier, interrupting the flow of current to the output. The magnetizing current continues to flow, however, so a resonant ring ensues between the magnetizing inductance and the parallel combination of the semiconductor devices' capacitances and any external capacitances that have been added.

Viewed from the primary side, the voltage on the resonant capacitor rings around the input voltage while the resonant current rings symmetrically around zero. Eventually, as the waveforms of Fig. 5.1b show, the MOSFET's drain voltage rings back to zero, which allows the MOSFET to be turned on with a zero-voltage transition. The timing of this turn-on is not critical, however, since the voltage is attempting to ring negative but is clamped just below zero, by the MOSFET's body diode and the output diode, where it remains until the magnetizing current goes positive.

Let us contrast the operation of this resonant forward-converter with the quasi-resonant converter of Chapter 4. First, in the forward-converter the resonance occurs when both semiconductor devices are non-conducting, allowing them both to enjoy benign turn-on and turn-off voltage transitions. Also, the resonant inductance is the magnetizing inductance, and the current in this inductance is independent of the load current, so the resonant ring is independent of load. Furthermore, the resonant current is the current that sets the flux in the transformer, so the transformer automatically operates with its flux centered around zero.

Because the resonance is independent of load current, not only does the MOSFET's voltage always return to zero, but the peak voltage stress is also independent of load. It is instead only a function of the input voltage and the duty ratio. This can be explained, assuming linear components, as follows. Since the resonant ring begins with the resonant inductor carrying a positive current, $I_o$, the amplitude of the ringing component of the capacitor's voltage is greater than the dc level, $V_{in}$. If the angle between the start of the ring and the point where the capacitor voltage
equals $V_{in}$ (which is also the point of peak resonant current, $I_p$) is denoted by an angle $\alpha$ (as in Fig. 5.1b), then we can write

$$\frac{V_{in}}{V_p} = \sin \alpha$$

(5.1)

and

$$\frac{I_{a}}{I_p} = \cos \alpha$$

(5.2)

The duration of the ring is

$$(\pi + 2\alpha)\sqrt{L_rC_{tot}} = (1 - D)/f_{sw}$$

(5.3)

where the total capacitance is the sum of the MOSFET's parallel capacitance and the diode's parallel capacitance reflected through the transformer (i.e., $C_{tot} = C_f + C'_r$).

Now, from the change in the magnetizing current during the on-time of the MOSFET, we can derive the relationship,

$$I_{a} = \frac{V_{in}D}{2L_rf_{sw}}$$

(5.4)

Combining (5.3) and (5.4) gives

$$\tan \alpha = \frac{2(1 - D)/D}{\pi + 2\alpha}$$

(5.5)

This equation can be solved numerically for a given value of duty ratio to determine the peak voltage across the MOSFET, which equals $(V_{in} + V_p)$. With a 50% duty ratio, for example, it equals $3.28V_{in}$. This is lower than the peak stress in the optimally designed quasi-resonant flyback converter, operating at full load ($4V_{in}$ for $D = 50\%$). The comparison becomes much more favorable if we instead consider
the peak stress in a quasi-resonant converter designed for a 3:1 load range \((8V_{in})\), as described in Section 4.2.3.

The peak ringing voltage is also independent of the component values. This gives the designer complete freedom to trade off the characteristic impedance of the ring against the resonant frequency without affecting the MOSFET's or diode's voltage ratings.

### 5.1.2 Effects of the Leakage Inductance

In any practical implementation, there is parasitic inductance associated with the transformer coupling and the interconnection of the components. A significant fraction of this comes from the connections on the low-voltage, high-current secondary. Assuming that this parasitic inductance, viewed from the primary side of the forward converter, can be kept as low as a few percent of the magnetizing inductance, and representing it as a single secondary side element as shown in Fig. 5.2, the operation of the circuit is modified in the following ways (see Fig. 5.4).

![Resonant Forward Converter with Leakage Inductance](image)

**Figure 5.2: Resonant Forward Converter with Leakage Inductance**

When the MOSFET turns on, the output current cannot make a step change
to its final value. Instead, it rises exponentially with a time constant that is generally comparable to the on-time. This slow rise in the load current actually makes the turn-on transitions of both the MOSFET and diode more benign than before. Unfortunately, the positive volt-seconds that must be applied across the leakage inductance during the on-time reduce the output voltage, and because this reduction is load-dependent it contributes a slight load regulation to the converter. Also, the rms value of the current waveform increases so the conduction losses are higher.

A simple model for the rectification process is shown in Fig. 5.3. In the absence of parasitic inductance, $L_{lk}$, the current waveform is approximately square, with the value determined by the voltage applied across the effective series resistance, $R_s$. This lumped resistance is used to represent all the conduction losses associated with the load current that occur in the transformer, the primary MOSFET, the resistive part of the Schottky rectifier, and the capacitive filters on primary and secondary. This current can be calculated as

$$I_{sec} = \left(\frac{V_{sec} - V_o - V_{rec}}{R_s}\right)$$

The average output current, $I_{ave}$, equals $DI_{sec}$, so the incremental output impedance, $Z_{out}$, which equals $-dV_o/dI_{ave}$, can be expressed as

Figure 5.3: Lumped Model of Rectification Process
$$Z_{out} = \frac{R_s}{D}$$  \hspace{1cm} (5.7)

The parasitic inductance alters this current waveform from a square wave to an exponential waveform, as shown in Fig. 5.4. One measure of the triangularity of this waveform is to relate the peak and average currents as

$$I_{pk} = k\frac{I_{ave}}{D}$$  \hspace{1cm} (5.8)

In one extreme, where the $L_{lk}/R_s$ time constant, $\tau$, is short compared to the conduction time, the current waveshape is relatively square and the value of $k$ approaches 1. In the other extreme the $L/R$ time constant is long compared to the half-cycle, the current waveform is triangular, and $k$ approaches 2.

The exponential current waveform can be expressed as

$$i(t) = \frac{V_{sec} - V_o - V_{rec}}{R_s} \left(1 - e^{-t/\tau}\right)$$  \hspace{1cm} (5.9)

The peak current occurs at $t = DT$, and equals

$$i(pk) = \frac{V_{sec} - V_o - V_{rec}}{R_s} \left(1 - e^{-DT/\tau}\right)$$  \hspace{1cm} (5.10)

The average current can be calculated as

$$i(ave) = \frac{V_{sec} - V_o - V_{rec}}{TR_s} \left[DT - \tau(1 - e^{-DT/\tau})\right]$$  \hspace{1cm} (5.11)

so $k$, the measure of triangularity, can be expressed as

$$k = \frac{D(1 - e^{-DT/\tau})}{D - \tau/T(1 - e^{-DT/\tau})}$$  \hspace{1cm} (5.12)

The expression for the average current can be used to evaluate the output impedance as,
\[ Z_{out} = \frac{R_s}{D} \left( \frac{1}{1 - \tau/DT(1 - e^{-DT/\tau})} \right) \] (5.13)

For the limiting case of a time constant much less than the conduction time, these expressions reduce to the square-wave current expressions derived above, with \( k \) approaching 1, as we said earlier.

In the other extreme, where the time constant is much longer than the conduction time, the expressions simplify to

\[ I_{pk} \simeq (V_{sec} - V_o - V_{rec}) \frac{DT}{L_{lk}} \] (5.14)

\[ I_{av} \simeq \frac{D}{2} (V_{sec} - V_o - V_{rec}) \frac{DT}{L_{lk}} \] (5.15)

\[ Z_{out} \simeq \frac{R_s}{D} \left( \frac{2\tau}{DT} \right) = \frac{2L_{lk}}{D^2T} \] (5.16)

and, as before, \( k \) is approximately 2. The expression for the output impedance shows that it is increased over the case where the inductance was negligible by a factor that is twice the ratio between the time constant and the conduction time. An analytic expression can also be derived for the rms current, which increases as the waveshape becomes more triangular. In the extremes this can be expressed as \( I_{rms} = (I_{ave}/\sqrt{d}) \) for the square wave and \( I_{rms} = \sqrt{4/3}(I_{ave}/\sqrt{d}) \) for the sawtooth waveform.

The leakage inductance also affects the MOSFET's turn-off transition. The load current component of the MOSFET's current does not drop immediately to zero, as it did before. Instead, this load component of the current continues to flow until enough negative volt-seconds have been applied across the leakage inductance to force it to zero. Two changes in the basic waveforms result.

The first change is that immediately following turn-off, the MOSFET's drain
trace(a): $L_{lk} = 0$

trace(b): $L'_{lk} = 0.015L_r, C'_r = 0.1C_{tot}$

Figure 5.4: Effect of Leakage Inductance on Switch Waveforms
voltage rises faster than before because it is being charged by the higher current. This faster rise places a greater switching stress on the MOSFET and its gate drive, and causes the resonant voltage to reach its peak earlier and return to zero earlier than before, as shown in the top waveform of Fig. 5.4.

The second change to the waveforms is the presence of a high-frequency ring which occurs when the output rectifier finally turns off. By the time the secondary current reaches zero, allowing the diode to turn off, the MOSFET voltage has risen to approximately

\[ V_a = (I'_{pk} + I_a) \sqrt{\frac{L'_{tk}}{C_f}} \]  \hspace{1cm} (5.17)

where \( I'_{pk} \) is the peak load current as seen from the primary and \( L'_{tk} \) is the leakage inductance referred to the primary.

Whereas, before the device capacitances were incrementally in parallel, they are now separated by the leakage inductance, and at the point that the diode recovers they are at different voltages. A parasitic oscillation occurs between the leakage inductance and the series combination of \( C_f \) and \( C'_f \), therefore, with the ring driven by this voltage difference. However, because the leakage inductance is much smaller than the main resonant inductance, and the series combination of the capacitors is less than the smaller of the two capacitors, this parasitic ringing occurs at a much higher frequency than the main resonant frequency. Even if lightly damped, this ring generally decays away by the time the main resonance reaches its peak voltage, as shown in the bottom waveform of Fig. 5.4. Therefore, this parasitic ring does not impact the peak off-state voltage of the semiconductor elements, in contrast to the effect of the parasitic ring in the quasi-resonant circuit.

The energy that is lost in the series ring between two capacitors and an inductor can be calculated by taking the difference between the initial and final energy storage. In this case the initial energy is all stored in the capacitor \( C_f \) and equals
\[ E_{\text{init}} = \frac{1}{2} C_f V_a^2 \quad (5.18) \]

By the time the ring decays, the same charge is distributed over the two capacitors so the final voltage is,

\[ V_{\text{final}} = \frac{Q_{\text{init}}}{(C_f + C'_r)} = \frac{C_f V_a}{(C_f + C'_r)} \quad (5.19) \]

so the final energy is

\[ E_{\text{final}} = \frac{1}{2} (C_f + C'_r) V_{\text{final}}^2 \]

\[ = \frac{1}{2} \frac{(C_f V_a)^2}{(C_f + C'_r)} \quad (5.20) \]

The energy lost by the time the ring has decayed equals

\[ E_{\text{diss}} = E_{\text{init}} - E_{\text{final}} \]

\[ = \frac{1}{2} C_f V_a^2 \left( \frac{C_r}{C_f + C'_r} \right) \quad (5.21) \]

and using (5.17), this can be rewritten as

\[ E_{\text{diss}} = \frac{1}{2} \frac{L'_{\text{lk}} (I'_{pk} + I_\alpha)^2}{L_r} \left( \frac{C'_r}{C_f + C'_r} \right) \quad (5.22) \]

If we expand this expression to

\[ E_{\text{diss}} = \frac{1}{2} L'_{\text{lk}} I_{pk}^2 \left( \frac{C'_r}{C_f + C'_r} \right) + \frac{1}{2} L_r I_\alpha^2 \left( \frac{L'_{\text{lk}}}{L_r} \right) \left( \frac{C'_r}{C_f + C'_r} \right) + \frac{1}{2} L'_{\text{lk}} 2I'_{pk} I_\alpha \left( \frac{C'_r}{C_f + C'_r} \right) \quad (5.23) \]
and use the relationships of (5.4) and (5.8) to simplify the third term, the result is

\[
E_{\text{diss}} = \frac{1}{2} L_{ik}^l I_{pk}^2 \left( \frac{C_f C_r}{C_f + C_r} \right) + \frac{1}{2} L_r I_{\alpha}^2 \left( \frac{L_{ik} l}{L_r} \right) \left( \frac{C_f C_r}{C_f + C_r} \right) + \frac{k L_{ik} l}{L_r} \left( \frac{C_r}{C_f + C_r} \right) E_{\text{cycle}}
\]

(5.24)

As the equation shows, there are three components of the dissipation. One is proportional to the energy stored in the leakage inductance, one is proportional to the energy stored in the transformers magnetizing inductance, and one is proportional to the energy transferred to the load each cycle, \(E_{\text{cycle}}\).

**Example:** Let us assume that we have a design with \(I_{pk} \approx 2I_{\alpha}\). If we are prepared to surrender 1% of operating efficiency to this loss mechanism, then for a \(C_f^l/C_f\) ratio of 0.5, (5.24) indicates that a leakage inductance as high as 3% of the magnetizing (resonant) inductance can be tolerated for a \(k\) of 1, or 1.5% for a \(k\) of 2.

### 5.1.3 Effects of Nonlinear Junction Capacitance

Another deviation from the idealized operation of the resonant forward converter, as described in Section 5.1.1, that is encountered in any practical implementation is caused by the non-linear capacitance of the MOSFET and the secondary-side rectifier. In a high-frequency converter, the required value of resonant capacitance is so small that these two capacitors combine to provide much, if not all, of what is needed. Because the incremental capacitance of these junction capacitors changes with voltage, the resonant waveforms are altered from those of Fig. 5.1b.

The charge stored on the MOSFET's junction capacitance goes as

\[
Q(V) = K \sqrt{V}
\]

(5.25)

so the incremental capacitance goes as
\[ C_{\text{inc}} = \frac{dQ}{dV} \]

\[ = \frac{K}{2} \frac{1}{\sqrt{V}} \]  \hspace{1cm} (5.26)

At the point where the resonance is initiated by the turn-off of the MOSFET, the value of incremental capacitance is at its highest value and so the resonance starts out slowly. At the peak of the resonance, the incremental capacitance is at its lowest value, however, so the voltage changes more rapidly than before. The effect is to increase the proportion of time that the voltage is below the value of \( V_{\text{in}} \) and decrease the proportion of time that it is above \( V_{\text{in}} \). The average voltage over the cycle must be the same to balance the volt-seconds across the transformer, however. The result is that the voltage excursion is much higher than was calculated for a linear capacitor.

The difference between the linear and non-linear capacitor oscillations are shown in Fig. 5.5a, where a square-law non-linearity is used to represent the junction capacitances. With the nonlinear capacitance, the device's peak voltage stresses are increased by approximately 30% over the linear capacitance case. This means that a device with a higher voltage rating must be used, which for the same die size means that the on-state resistance, and therefore the conduction losses, will be higher. It is important to note that this effect is not unique to the Resonant Forward Converter, but is exhibited by all of the single-ended resonant circuits\(^2\) that utilize junction capacitances as resonant elements.

The combination of linear capacitance and non-linear capacitance has lower peak voltage stress than the pure non-linearity. This is a good argument for minimizing the device's junction capacitance so that if it does not supply all of the required resonant capacitance, some linear capacitance can be added.

The negative impact of the non-linear capacitance in this particular situation

\(^2\)Including the zero-voltage quasi-resonant and Class-E converters.
(a) Capacitance $\propto \sqrt{1/V}$

(b) Proposed Circuit to Reverse Nonlinearity

(c) Waveforms for Reversed Nonlinearity

Figure 5.5: Effects of Non-Linear Resonant Capacitance
motivated efforts to instead use non-linearities to good effect. If, in this resonant application, the non-linearity had been reversed so that the incremental capacitance started small and then got larger as the voltage increased, then the peak voltage stress would actually have been lower than for the linear capacitor.

The type of non-linearity we have just described can be achieved by using a diode and a capacitor as shown in the circuit of Fig. 5.5b. The key to the operation of this non-linear capacitance is that the capacitor labeled $C_{BIG}$ is charged to a voltage higher than the peak MOSFET voltage. Thus, the diode in series with this capacitor is always reverse biased, and the value of its incremental capacitance, $C_d$, increases as the MOSFET’s drain-source voltage increases. The capacitance across the MOSFET has been increased by the series combination of $C_{BIG}$ and $C_d$, which if $C_{BIG}$ is much greater than $C_d$ is approximately $C_d$. Figure 5.5c shows the effect on the resonant waveforms of adding this type of non-linear capacitance to the resonant circuit.

The scheme we have just proposed is self-regulating in the sense that if the peak drain voltage ever exceeds the capacitor voltage, the diode becomes forward-biased and therefore charges the capacitor up to the correct value. Furthermore, in the situation of a severe transient it acts as a clamp on the drain voltage. This scheme does require two components, rather than one, to add capacitance, but both components can be achieved in fairly small devices and will provide savings not only in peak device rating (and therefore conduction losses) but also in energy lost due to reverse leakage currents in the semiconductor elements. This technique can be used in conjunction with any of the zero-voltage topologies, and is really very similar to the lossless H-bridge scheme we discussed in Section 3.4.

The ability to add either some linear capacitance or some of this favorably non-linear capacitance to the resonant circuit requires that the junction capacitances not provide all of the resonant capacitance. This is yet another reason for minimizing these capacitances through optimized device fabrication, as described further in Section 6.2.1.
5.2 The Dual Forward Converter

In single-ended converter circuits, a large fraction of the overall volume is devoted to the input and output filters. While operating at a higher frequency helps to shrink these filter elements, they remain the major component of total size and cost. This is particularly true of filters for regulated, low-voltage, high-current outputs, with strict ripple requirements since it is more difficult to achieve high energy densities at low voltages with existing capacitor technology.

The essence of the problem is that these single-ended circuits only deliver energy through the transformer for part of the cycle. Earlier we raised this issue in the context of square-wave converters (see Section 3.4). As discussed then, the solution is to either use a double-ended power circuit, or to interleave two or more single-ended circuits. Power can then flow from input to output 100% of the time, and the filter elements can be made correspondingly small.

For the resonant forward converter we have been examining, it is not possible to configure a double-ended circuit since the resonant action dictates that the transformer voltage follow the ring while the MOSFET is off rather than be constrained through a coupled winding by the on-state of another MOSFET. Instead, an interleaved circuit, using two single-ended converters connected in parallel and operated out of phase, must be used, as shown in Fig. 5.6.

If there were no leakage inductance (which limits the rate at which each half-circuit picks up the load current) and no ripple current associated with the resonant inductors, then the input and output filter elements would be superfluous. As it is, any ripple that does exist is significantly less than for a single-ended converter and the ripple frequency is at twice the frequency of operation. Furthermore, the buss capacitance on the primary side is incrementally separated from the secondary side capacitance by only one of the leakage inductances throughout the cycle, so it contributes to hold-up of the output voltage during load transients.
This interleaved converter structure, which we call the dual converter, does increase the number of components, but because each section handles less of the total power, it does not increase the total component power rating. For example, in the dual resonant forward-converter the two MOSFETs can be implemented using the same area as the original single MOSFET. The total conduction losses remain unchanged and the gate drive energy is the same. With each resonant capacitance reduced by a factor of two, the resonant inductance must double to maintain the same resonant frequency, which means that the characteristic impedance of the resonance increases by four. The magnetic energy storage requirement of each half-circuit is consequently halved, so the total energy storage is the same. There are, therefore, no fundamental penalties associated with the dual converter, other than the increase of parts and interconnection.
5.3 Regulation

The dual resonant forward converter of the previous section cannot, by itself, regulate the output voltage. So, in an application calling for regulation, it must be used in conjunction with either pre-regulation or post-regulation circuitry. This would seem to be a prohibitive requirement, in terms of increased parts count and higher losses, when compared to a converter that can provide regulation in a single stage. Fortunately, for an input voltage range that is restricted and with reasonable load regulation it is possible to utilize regulation circuitry that does not have to be rated for the full converter power.

Such a scheme has been developed to take advantage of the limited conversion ratio needed, and it permits efficient square-wave switching at very high frequencies in either a pre-regulation or a post-regulation stage. This scheme does not contribute excessive losses when compared with other regulation mechanisms, and because it is a constant frequency approach, it can be used with both resonant and quasi-resonant converters if EMI considerations make variable frequency control undesirable.

The pre-regulator is shown in Fig. 5.7a. It is essentially an up-converter that controls the voltage presented to the dual resonant forward converter, $V_{bus}$. However, instead of the controlled switch being connected to ground, and thus having to withstand the full output voltage of the up-converter, it is instead connected to a midpoint voltage formed by two capacitors which split the dc bus. The capacitors are sufficiently large, that on the time scale of the switching period the midpoint can be regarded as an incremental ground. The two voltages, $V_{mid}$ and $V_{bus}$, are chosen to be below and above the expected extremes of input voltage variation, respectively. This ensures that over the full range of input voltage, control can be maintained over the current flow within the up-converter. In fact, like any conventional up-converter, the rectifying diode and the MOSFET’s body diode prevent the voltage of the upper output node being lower than the input voltage and the
voltage of the lower output node being higher than the input.

![Diagram of a dual resonant forward converter](image)

Figure 5.7: Pre-Regulation Scheme

The value of this pre-regulator scheme is that both semiconductor elements are only subjected to the difference between the voltage extremes, rather than the peak voltage which would be the case in a conventional up-converter. Consequently, the device ratings are lower and a given on-state resistance can be achieved in a smaller die size with reduced junction capacitance. The smaller capacitance, coupled with the lower switching voltage, results in a dramatic reduction in the energy stored in the junction capacitances. A very high switching frequency can therefore be used without incurring significant losses.

Another advantage of the lower switching voltage is that the stress on the input filter elements is reduced. So, along with efficient high-frequency operation, small filter elements can be used to maintain the high conversion densities of the dual
resonant forward converter circuit.

To appreciate the impact of this pre-regulator stage on a practical converter, let us consider a 50 W system whose input voltage varies from 34 V to 42 V. With a nominal input voltage of 38 V, the input current is 1.3 A. A MOSFET and Schottky diode selected for this application will typically have a combined capacitance of 200 pF, or less. Using this number, the capacitive energy loss would therefore be 6.4 nJ/cycle. A parasitic inductance of 10 nH, \(^3\) would contribute another 8.5 nJ/cycle. Finally if the switch transition took 4 ns to complete\(^3\), a further 45 nJ/cycle would be lost. With these numbers, which are very reasonable, operation at 5 MHz would create only 0.3 watts of switching loss.

If the midpoint node formed by the capacitors is to act as a dc voltage source, then the net charge flowing into the node must be zero. The MOSFET of the up-converter supplies charge to this node, so there must be some means to remove it. One possible method is to use the transformer of the forward converter to remove charge when the transformer is delivering energy from primary to secondary. This can be achieved by connecting the midpoint to a tap on the transformer through a Schottky diode, as shown in Fig. 5.7b. If the midpoint voltage is low, this diode is reverse-biased and therefore no charge is removed. Over time, however, it is charged up by the up-converter so that the diode is periodically forward-biased when the transformer is delivering power. On average, the transformer draws energy from the midpoint node and the main buss node in the exact proportion that it is delivered to these nodes by the up-converter. The ratio between the two voltages is determined by the transformer tap.

If the control circuit for this pre-regulator stage were required to provide line regulation only, it would simply have to maintain the correct voltage difference between the main buss and the midpoint. The dual forward converter would then be presented with a constant voltage, as long as the line voltage was between the specified bounds. However, the effect of load regulation requires that \(V_{bus}\) be varied

\(^3\)which we argued was easily achievable in Section 3.2.3
in response to changing load currents, so some form of feedback control is required. It is worth noting that the power supply for the controller/driver for the controlled switch in this up-converter scheme is naturally provided by the voltage difference between the main bus voltage and the midpoint voltage.

\[ \begin{align*}
C_1 &= 200\,\text{nF} & L_1 &= 30\,\mu\text{H} & N_1 &= \text{IRF630} \\
C_2 &= 300\,\text{nF} & L_2 &= 2\,\mu\text{H} & N_2 &= \text{IRF630} \\
C_3 &= 100\,\text{nF} & D_1 &= \text{IR11DQ06} & N_3 &= \text{IRFD120} \\
C_4 &= 30\,\text{nF} & D_2 &= \text{IR11DQ06} & T_1 &= T_2 \\
C_5 &= 30\,\text{nF} & D_3 &= \text{IR11DQ06} & \text{N} &= \text{Ferroxcube} \\
C_6 &= 400\,\text{nF} & D_4 &= \text{IR31DQ06} & 1107\text{PA40} \\
& & D_5 &= \text{IR31DQ06} & 12/9 : 3
\end{align*} \]

Figure 5.8: Prototype 3.6 MHz Resonant Forward Converter with 2 MHz Pre-Regulator
5.4 Experimental Converter for Point-of-Load Supply

5.4.1 Experimental Results

A series of experimental converters was developed to demonstrate the feasibility of the resonant forward converter of Section 5.1, the dual resonant forward converter of Section 5.2, and finally the dual resonant forward converter with the pre-regulator stage of Section 5.3. The final prototype included all of the aspects of the earlier work and thus is the only one documented here.

A 50 W prototype that operated the main MOSFETs at 3.6 MHz, and the pre-regulator at 2 MHz was constructed. The converter was designed for an input voltage range of 32-40 volts, so the voltage tap was made at turn 9 of a 12-turn primary transformer winding. The circuit schematic, component values and parts list are given in Fig. 5.8.

Standard components and construction techniques were employed, so the demonstrated switching frequency, power density, and efficiency are all lower than will eventually be possible with specialized devices and fabrication techniques. In fact the subsequent hybrid converter assemblies using the same standard components, which is described further in Section 5.5, improved significantly in each of these categories.

The prototype circuit was constructed on a printed circuit board with no heat sinking of individual components, so that a compact assembly could be achieved, as shown in Fig. 5.9. This approach is a far cry from hybrid fabrication, which was used for subsequent prototype developments, because packaged components were used here. There were only two layers of interconnect, separated by 1/16 in, so it was difficult to keep the parasitic inductances down. Within these constraints, however, extreme care was exercised to minimize the parasitic inductance of the interconnections. The overall dimensions of the circuit, with no heatsink and ignor-
ing the gate drive (which was mounted on a separate board), are 1 9/16 in long by 10/16 in wide and 3/4 in high.

The voltage waveforms of the two MOSFETs of the dual converter are shown for 0% and 100% load in Figs. 5.10a and 5.10b. These waveforms are very similar to the simulated waveforms shown in Section 5.1, and demonstrate the independence of the resonance, and therefore the peak device voltage, from the level of load current. The effect of the non-linear junction capacitance is evident in the waveshapes. The faster initial rise and the subsequent high-frequency oscillation caused at high load currents by the leakage inductance can also be seen. The parasitic ring does indeed decay before the main resonance reaches its peak, as we argued in Section 5.1.2, and thus it does not impact the peak device stress. The balance between the waveforms of the two half circuits is quite remarkable, given that the semiconductor devices and the transformers provide all of the resonant inductance and capacitance.

Figures 5.10c and 5.10d show the voltages across one of the primary side MOSFETs and across the corresponding transformer’s secondary winding. The secondary voltage provides a measure of the rectifier’s voltage. The parasitic oscillation is seen to occur principally across the rectifier, but, as before, it decays as the
(a) drain-source waveforms, unloaded

(b) drain-source waveforms, full load
Figure 5.10: Experimental Waveforms
resonant voltage rises and so does not contribute to a higher peak voltage. It should also be noted that, due to the care taken in layout and instrumentation, this circuit operates very cleanly.

The pre-regulator stage was operated at a frequency of 2 MHz, and the ability to operate with an input voltage from 31-40 volts was demonstrated, as shown in Table 5.1. The operating efficiency was 83% with the highest input voltage and fell to approximately 80% at the lowest voltage. Therefore, the regulation scheme cost us approximately 3% of the operating power which seems quite reasonable, and this was with 100 V components used in the pre-regulator stage rather than the 20 V devices that would be practicable. It should therefore be possible to reduce this loss dramatically with appropriate devices.

<table>
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<tr>
<th>d_{pr}</th>
<th>V_{in} (volts)</th>
<th>I_{in} (amps)</th>
<th>P_{in} (watts)</th>
<th>V_{out} (volts)</th>
<th>P_{out} (watts)</th>
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<td>.03</td>
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<tr>
<td>0</td>
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<td>59.2</td>
<td>8.17</td>
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<td></td>
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<tr>
<td>1</td>
<td>31.3</td>
<td>1.95</td>
<td>61</td>
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<tr>
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<td>60.2</td>
<td>8.17</td>
<td>49</td>
<td>81.4%</td>
</tr>
</tbody>
</table>

Table 5.1: Operating Levels for Different Input Voltages

5.4.2 Performance Limitations

To be more specific in citing limitations on the converter's performance, the capacitance of the available MOSFET limited the operating frequency, the transformer design with its bifilar windings had considerably more leakage inductance than desired, and the Schottky rectifiers (that were available at that time) had relatively high forward drops. The available low-voltage MOSFETs were completely unsuitable for implementing either the pre-regulator stage efficiently or for attempting to implement synchronous rectification. Further, the two controller/drivers that were
required had to be assembled using multiple packaged parts and therefore ended up as bulky as the power converter itself. Even so, this prototype work pushed all of the components to their limits, and so was an honest test of the topologies ability to accommodate the dominant parasitics.

The various limitations motivated the development work on components and assembly techniques that is presented in the next chapter. This includes on-going work developing specialized components for the converter, including specialized MOSFETs, low-leakage transformers, and also custom controller/driver ICs that are described in Chapter 7. Topological modifications have also been proposed to overcome some of the operating limitations of the converter, and for the implementation of synchronous rectification. These ideas are presented, with other topological ideas, in Chapter 8. The developments included successive stages of hybrid assembly of the experimental converter, the results of which are described below. These hybrid assemblies simultaneously achieved lower output voltages and improved the operating efficiency.

5.5 Experimental Results of the Hybrid Converter

The hybrid versions of the dual resonant forward converter used almost the same set of components as the experimental prototype described in the previous section. The transformers were different, however, using the barrel windings described in Section 6.1.2. These transformers have less leakage inductance and winding resistance than the bifilar windings. Another difference between the earlier prototype work and the hybridized converter is that Schottky rectifiers with lower forward voltage drops became available, and these were used to achieve higher rectification efficiency. The remaining components were essentially the same, but an important difference was that unpackaged parts were used so that the converter could be assembled with minimal interconnection parasitics.

Table 5.2 summarizes the results of successive iterations of hybrid construction.
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<th>III</th>
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<tbody>
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<td>Construction</td>
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<td>Cu Hybrid</td>
<td>Cu Hybrid</td>
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<td>7:1 Cu foil</td>
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<td>0.35V</td>
</tr>
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<td>5.3V</td>
<td>5.0V</td>
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</tr>
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</tr>
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<td>65W/in&lt;sup&gt;3&lt;/sup&gt;</td>
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<td>5MHz</td>
<td>5MHz</td>
</tr>
<tr>
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<td>83/81</td>
<td>82/80</td>
<td>82/80</td>
<td>85/83</td>
</tr>
</tbody>
</table>

Table 5.2: Results of Successive Hybrid Assemblies

The combination of improved transformers and lower drop rectifiers permitted the hybrid converters to deliver the same power at a lower output voltage while maintaining the same overall efficiency. The improvement in conversion density was due to the unpackaged parts and also to a reduction in the height of the transformers, which were the components with the highest profile. The hybrid converters did include the driver ICs for the power MOSFETs, but the rest of the control circuitry was external. The critical components required to complete the stand alone power conversion module, therefore, are controller/driver ICs. The preliminary work in this area is described in Chapter 7.
Chapter 6

Developments for the Resonant Forward Converter

This chapter describes several research efforts that were complimentary to the prototype development work described at the end of the last chapter. The link between these different research projects and this thesis is that the results of the high frequency topology development motivated these other efforts. These projects included the development of a thick-film hybrid facility to facilitate the construction of high-density converters, specialized semiconductor development, and magnetic component studies that led to optimized transformer design procedures. This chapter gives an overview of the progress made in each of these areas.

6.1 Hybrid Construction of the Resonant Forward Converter

6.1.1 Thick Film Facility

A thick film facility was established in the MIT Microsystems Technology Laboratory to facilitate the assembly of high performance, high density, power circuits [47]. In the initial phase, gold thick film inks were used with alumina substrates, and the facility was used to investigate the suitability of hybrid processing and packaging for the fabrication of high-density power supplies.
One of the issues investigated was the ability to build up layers of arbitrary thickness through multiple print-dry-fire cycles to achieve low resistance interconnection. Another important issue was the minimization of parasitic inductances through the use of multiple layer interconnections. Considerable effort was also expended developing assembly methods that achieved good electrical and good thermal characteristics for die and component attachment to the substrate. Another important issue was ease of assembly and rework capability, which necessitated the use of different temperature solders so that a temperature hierarchy could be established for successive stages of assembly and disassembly.

The gold thick film capability was successfully developed to the point where high performance power circuits could be assembled, with the obvious drawback of this technology for commercial applications being the high cost of working with gold. An effort was therefore initiated to develop a similar power circuit assembly capability using copper inks, which are, in comparison, relatively inexpensive. The major problem with working with copper is surface oxidation of the copper. The inked substrate itself must be fired in a Nitrogen environment to limit this tarnishing, and all of the adhesion properties (e.g. between copper and substrate, between multiple copper layers, solder attachments and wire bonding to the copper) are compromised by this oxidation. Techniques were developed to address each of these adhesion problems [48], and the copper thick film facility was then used to fabricate several iterations of hybridized versions of the dual resonant forward converter of Section 5.4. The results of this work are described in Section 5.5.

6.1.2 Barrel Winding for Hybrid Assemblies

The bifilar transformer windings used in the experimental converter described in Section 5.4 had considerably more leakage and winding resistance than desired. To permit manual assembly, the thickness of wire used in this winding was greater than the skin depth, so the utilization of copper was poor and the proximity effect losses were high. Further, the radius of curvature of the wire limited the coupling between
primary and secondary windings. These bifilar windings became particularly inadequate, as other improvements in the successive iterations of hybrid development permitted lower output voltages and so required transformers with increased turns-ratios. The higher turns-ratios magnified not only the value of the transformer's leakage but also the parasitic inductance of the secondary interconnections. The secondary windings emerged from the transformers as multiple wires that then had to be joined and connected to the rectifiers, rather than as low inductance sheets, so the interconnection parasitic was relatively high for these bifilar windings.

To improve the converter performance, the bifilar windings were replaced by barrel windings [49]. These windings permitted the primary and secondary currents to flow in adjacent sheets, as shown in Fig. 6.1. The thickness of these sheets was kept to a skin depth, to utilize the copper and avoid circulating current losses, and the sheets were spaced tightly to minimize the leakage. Also, termination tabs were made contiguous to the sheet windings so that the intra-winding and secondary interconnection parasitics could be kept to a minimum.

![Diagram of Barrel Winding Transformer with 7:1 Turns Ratio and Interleaved Secondaries](image)

**Figure 6.1: Barrel Winding Transformer with 7:1 Turns Ratio and Interleaved Secondaries**

Initially, the barrel windings were constructed using successive layers of pre-cut
copper foil and insulating tape. This construction technique was quite arduous and the results were not very repeatable, so flexible PCB material\(^1\) was subsequently used. The copper covered flex was patterned and etched using standard PCB technology. The resulting strip was wrapped to form the barrel winding and the intra-winding and external interconnections were then made by folding and soldering the contiguous tabs.

6.2 Power Semiconductor Components

6.2.1 Low Capacitance MOSFET with Integral Driver

The ultimate limit on the switching frequency of the resonant forward converter was shown in Section 5.1.1 to be the size of the resonant capacitor, the dominant component of which was the MOSFET's capacitance. A specialized MOSFET structure was therefore developed to minimize this capacitance. Figure 6.2 shows a cross-sectional view of a vertical diffused MOS (DMOS) power FET that was developed and fabricated in the MIT Microsystems Technology Laboratory for this application \([14]\). The structure is conventional except that the gate electrode has been lifted as it passes over the lightly doped \(N^-\) epitaxial region to reduce the drain-gate capacitance.

When the MOSFET is on, electrons flow from the source to the drain. First they flow horizontally through the conducting channel beneath the gate, and then they spread out as they progress vertically downward through the \(N^-\) drift region. The area of the device available for conduction is somewhat less than the total area since the current does not spread out completely underneath the P-wells. The device capacitance depends on the full area used, so the area beneath the P-wells prevents the MOSFET from achieving its theoretical minimum \(RC\) product. It is desirable, therefore, to make the P-wells as small as possible.\(^1\) Today's commercial devices typically have 30 \(\mu\)m P-well widths, but available lithographic capabilities

\(^1\) double sided copper on Kapton (flex)
Figure 6.2: Vertical DMOS FET

can be used to reduce this to approximately 10 μm, and this was the well width used in the experimental MOSFET.

The raised gate mentioned above has the effect of reducing the accumulation charge beneath the gate oxide. It also reduces the current spreading and increases the on-state resistance of the MOSFET. The penalty is small for the corresponding savings in capacitance, however. Design simulations for the experimental device showed that the drain-gate capacitance could be reduced by a factor of two while increasing the on-state resistance by only 5 percent. The experimental device confirmed these projections, as can be seen in Table 6.1, which compares the MIT device to a commercial device with the same on-state resistance and voltage rating.

Another important consideration for the power MOSFET in the resonant forward converter, and for any high-frequency converter, is the gate drive, particularly the ability to turn the MOSFET off rapidly when it is carrying its peak current. The transformer's leakage inductance forces this current to flow into the device capaci-
<table>
<thead>
<tr>
<th></th>
<th>((V_{ds} = 25\text{V}, V_{gs} = 0\text{V}))</th>
<th>IR 200\text{V}, 0.5\text{\ Omega}</th>
<th>MIT 200\text{V}, 0.5\text{\ \Omega}</th>
<th>red. fac.</th>
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<tr>
<td>(C_{oss}(\text{pF}))</td>
<td>154</td>
<td>76</td>
<td>0.49</td>
<td></td>
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<tr>
<td>(C_{iss}(\text{pF}))</td>
<td>450</td>
<td>320</td>
<td>0.71</td>
<td></td>
</tr>
</tbody>
</table>

Table 6.1: Comparison with commercial FET

stances after the channel becomes non-conducting, as shown in Fig. 6.3. This current splits in the ratio of the capacitances, and the portion that flows in the drain-gate capacitance has to flow through the gate drive impedance, which includes parasitic resistance in the MOSFET's gate structure, interconnection inductance, and the on-state resistance of the pull-down transistor. Now, to keep the MOSFET's channel non-conducting and so avoid conduction losses, the voltage drop across this gate impedance has to be less than the MOSFET's threshold voltage, and this must be true for any point on the MOSFET die to avoid localized conduction that would lead to thermal hotspots.

![Current Flow at Turn-Off](image)

Figure 6.3: Current Flow at Turn-Off

The solution that has been employed in the experimental device is to integrate the turn-off driver throughout the power MOSFET, avoiding the voltage drops
across the gate structure and the interconnection inductance. The pull-down transistor used to turn the MOSFET off is a lateral MOSFET constructed in an extended P-well, as shown in Fig. 6.4. This pull-down driver is interdigitated with the power device on the same die. The experimental integrated pull-down device has an on-state resistance of 2.4$\Omega$ with a gate-source voltage of 12 V. The power MOSFET has a threshold voltage of approximately 3 V, so a current as high as 1.25 A can flow in the drain-gate capacitance following turn-off without turning the MOSFET channel back on. The drain-gate capacitance is less than half of the total output capacitance so the total current driving the drain can be considerably larger.

![Diagram](image)

Figure 6.4: Integrated Turn-Off Device

6.2.2 Low Capacitance, Fast Recovery, Low Voltage MOSFET

We have identified two applications for an improved low voltage MOSFET in our previous discussions. The first is as a synchronous rectifier element to replace a Schottky diode and so reduce rectification losses. The second is as a low voltage,
low capacitance, device for the pre-regulation scheme of Section 5.3. For the synchronous rectifier application, it is important that the recovery times of the MOSFET's body diode be on the order of nanoseconds, if the device is to be used in the 5-10 MHz range, as discussed in Section 3.5. For both applications it is important to minimize the device's $RC$ products ($R_{on}C_{iss}$ and $R_{on}C_{oss}$). The device will then have less capacitive energy requirements for a given on-state resistance, which will allow it to operate more efficiently at higher frequencies.

A special device has been developed at MIT [16] to meet the need for low capacitance and short body-diode recovery times in a low-voltage power MOSFET. This device has been designed without a lightly doped drain region, which is a feature of other power MOSFETs, because of the low off-state voltage requirement (25 V). To minimize the resistance per unit die area, a vertical gate structure has been used, which permits source and drain connections to be made on opposite faces of the die. Although a U-groove would yield a higher packing density, a V-groove structure (as shown in Fig. 6.5) is used because it results in smaller drain-gate capacitance. Design studies show that an $R_{on}C_{iss}$ product of 20 pFΩ, and an $R_{on}C_{oss}$ product of 10 pFΩ, can be achieved, whereas the 100 V MOSFETs in Table 3.1 have $R_{on}C_{iss}$ products of $\approx 120$ pFΩ and $R_{on}C_{iss}$ products of $\approx 75$ pFΩ.

![Diagram](image_url)

Figure 6.5: Low Voltage Fast Recovery V Groove MOSFET
Because it has no lightly doped drift region, the device has a short base body-diode, rather than the p-i-n body-diode normally present in higher voltage MOS-FETs. The reverse recovery time of the short base diode is dependent on the transit time, rather than the minority carrier lifetime. Since the transit time is proportional to the square of the off-state voltage, it can be very short for a device designed to withstand only 25 V. The experimental device is expected to have recovery times on the order of a nanosecond, and is currently being fabricated.

6.3 Optimized Transformer Design

The bifilar-wound transformers of the experimental prototype severely limited the performance of the converter, and while the barrel windings used in the hybrid assemblies were a distinct improvement, there were still marked problems. Chief amongst these was the difficulty in trading-off copper and hysteresis losses, the construction complexity, and the difficulty in achieving repeatable characteristics from transformer to transformer. This last limitation is of considerable concern, because of the desire to achieve balanced operation between the two halves of the dual resonant forward converter.

To address all of these concerns, a comprehensive study was carried out of 1–10 MHz transformers [10]. The first part of this work required the experimental measurement of core loss of various high-frequency magnetic materials at the flux levels typically found in power conversion transformers, since this information was not previously available. Numerical simulation tools were then employed to determine the conduction and core losses for complex magnetic, and winding structures. This information was used to identify certain structures which were easy to manufacture, promised consistent characteristics, and efficiently employed the available volume without incurring unnecessary losses. The winding structure that was selected was the spiral winding, which is shown in a cut-away view in Fig. 6.6, and studies were made of the advantages of interleaving multiple spiral windings (at the expense of additional manufacturing effort).
Figure 6.6: Spiral Winding Transformer

All of the information from the various sections of the transformer study was then integrated into an optimization program, so that for a specified total loss (and a certain level of transformer construction complexity), a transformer could be designed with a minimum footprint area. Similarly, for a given footprint the design procedure would yield a transformer with minimum total loss.

This optimization program was used to design a spiral winding transformer to replace the barrel winding of the hybrid prototype. The comparison between the two transformers is shown in Table 6.2. For the same footprint, the total dissipation in the optimized transformer is seen to just over one third of the dissipation in the barrel winding transformer, and this is actually achieved in a smaller volume as the height is not as great. Given that the loss in two of these barrel winding transformers represents approximately 6% of the 50 W output power, the ability to reduce this by a factor of three is a significant contribution to improving the overall efficiency of the converter.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Barrel</th>
<th>Optimized</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetizing inductance</td>
<td>$L_m$</td>
<td>2.5μH</td>
<td>2.5μH</td>
</tr>
<tr>
<td>Turns</td>
<td>$N$</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>Magnetizing current</td>
<td>$i_m$</td>
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<td>0.9 A</td>
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<tr>
<td>Load current</td>
<td>$i_l$</td>
<td>2.86 A</td>
<td>2.86 A</td>
</tr>
<tr>
<td>Diameter</td>
<td>$d$</td>
<td>1.1 cm</td>
<td>1.1 cm</td>
</tr>
<tr>
<td>Height</td>
<td>$h$</td>
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<td>3.6/3.9 mm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>$P_t$</td>
<td>1.5 W</td>
<td>1.1/0.65 W</td>
</tr>
</tbody>
</table>

Table 6.2: Comparison of Optimized Transformer with Barrel Winding
Chapter 7

Integrated CMOS Controller/Drivers for Resonant Forward Converter

This chapter describes the design, implementation, and experimental evaluation of custom CMOS controller/driver I.C.s for the experimental dual resonant forward converter of Sections 5.4 and 6.1.

7.1 Background: Need for Library of High Performance Sub-Circuits to Implement Custom Controller/Drivers for High Frequency Converters

A critical element in achieving high-density modular converters is the integration of the control and drive functions in a minimum number of ICs. These must be specialized ICs, developed and optimized for each converter application, rather than general purpose devices applied in conjunction with discrete components. Much of the specialized nature of the control is the performance of housekeeping functions that can be implemented with simple logic circuitry, and the unique nature of the analog sensing in that particular application. To avoid unnecessary duplication of IC design effort, and so reduce the design time and cost, a library of functional building
blocks that can be rapidly assembled to implement custom controller/drivers needs to be developed.

The choice of process technology for these custom ICs is important. In the past, bipolar circuitry has had a _de facto_ lock on high frequency controller/driver applications, for reasons that evolved from driver considerations. In fact, bipolar driver ICs \(^1\) have been used extensively to drive power MOSFETs in the last decade, and as frequencies have increased they have proved equal to the task of operating in the 1–10 MHz range. However, these bipolar drivers have excessive static, and dynamic, power dissipation.

CMOS drivers\(^2\) have been commercially developed as an alternative to the bipolar devices, and because they avoid the static power dissipation of the bipolar drivers they have been widely applied at frequencies below 100 KHz. The limitation on operating frequency of these CMOS devices has been imposed by relatively slow switching speeds, which manifest themselves in the commercial devices as delays, (on the order of 100 ns) and shoot-through currents in the output stage that cause noise problems and dynamic dissipation.

Another important technology to consider is biMOS, which is regarded by many as the technology of the future. This is a mixture of bipolar and CMOS, which permits the designer to utilize each process in areas of the design where it performs well. It is, however, not really a viable commercial process at this time and is considerably more complex than either the bipolar or CMOS processes on their own.

Despite its limitations, CMOS is a particularly attractive process for the development of a library of functional controller/driver building blocks for the following reasons. The first is the convenience of the MOSIS\(^3\) fabrication program, and its

\(^1\)such as the DS0026 [50].
\(^2\)such as the D469 [51] and the TSC429 [52].
\(^3\)MOS Implementation Service - a DARPA supported fabrication program operated by the Information Sciences Institute of the University of Southern California. Users submit their layouts in CIF format and one of a number of different vendors manufactures the IC, depending on the availability of their process line. Total turn-around from submitting the design to receiving packaged parts is
availability to both academic and industrial users, and the shared sub-cell mindset already associated with the MOSIS program because of the VLSI work that it supports. A second reason is the low power dissipation of CMOS, since the ultimate limit on the ability to achieve high power conversion densities is the need to remove internally dissipated energy from the converter module. In low power applications, such as the 50 W point-of-load converter module, this control/drive power can be a significant fraction of the total dissipation. Finally, a third reason to work in CMOS is the ongoing improvement in resolution (and therefore circuit densities) and operating speeds of this technology, which is being vigorously pushed for VLSI applications. If scalable design rules are used, basic circuit modules don’t become obsolete with these process advancements, which is a particularly valuable feature for a library of functional cells.

The fundamental question that needs to be answered before CMOS can be used as the process for high-frequency power controller/driver ICs is: is the process fast enough to adequately provide the needed analog functions? If it is a viable technology, then to what frequency is it viable? And, can it be made sufficiently stable over temperature and from sample to sample?

### 7.2 Goals of CMOS Controller/Driver Development

There were two goals of this work on integrated CMOS driver/controller ICs. One goal was to answer the questions raised above regarding the suitability of CMOS as the process for developing custom high-frequency controller/drivers. The other goal was to develop custom integrated control/drive ICs for the experimental Resonant Forward Converter of Section 5.4. The approach taken was to develop open loop controller/driver ICs for the prototype converter, and by attempting to maximize the performance of the different blocks of sub-circuitry in successive design iterations approximately 10 weeks. Because many projects share each wafer the cost is extremely low, as little as $400 for four packaged parts or $2,000 for 10 packaged parts.
to answer the fundamental questions about the viability of CMOS technology for the high-frequency controller/driver application.

The experimental converter requires two controller/driver ICs which are labeled U1 and U2 in Fig. 7.1. The performance specifications that we aimed to meet for these two open-loop controller/driver ICs are described below.

![Diagram of Two Controller/Driver ICs]

Figure 7.1: Two Controller/Driver ICs

### 7.2.1 Specifications for the Two Controller/Driver ICs

The IC labeled U1 in Fig. 7.1 must drive the two resonant MOSFETs of the dual resonant forward converter, and so has been designated as the Dual Driver. The design goal for the Dual Driver IC is to achieve two outputs that are 50% duty ratio square-waves, 180° out of phase, at a stable frequency that can be adjusted between 5-10 MHz. Also, both outputs must be able to drive a 300 pF load capacitance (which represents the gate capacitance of the specialized MOSFET of Section 6.2.1)
with a rise and fall time of less than 10 ns, and additional outputs must be provided so that the IC can drive MOSFETs that incorporate the integrated shorting switch described in Chapter 6).

There were three complete iterations of the Dual Driver design (including fabrication). Successive iterations attempted to improve the performance of each functional building block to better meet the overall specifications of the IC, and to explore the limitations of the technology.

The IC labeled U2 in Fig. 7.1 must drive the pre-regulator MOSFET of Section 5.4, and so has been designated the **Pre-Regulator Driver**. This MOSFET is part of an up-converter, so the IC must be able to generate variable duty ratio gate drive signals in response to an external command voltage. It is critical that the relationship between input voltage and duty ratio be monotonic. This particular Pulse Width Modulation (PWM) block will ultimately be included in a feedback control scheme, where linearity of the input voltage to duty ratio relationship (the slope corresponds to incremental gain) is not that critical. There are other PWM applications, however, where linearity is important and so achieving good linearity was also a design goal.

To alleviate anticipated EMI problems we decided that rather than having its own clock generator, the Pre-Regulator drive frequency should be at half the frequency of, and synchronized to, the switching of the main MOSFETs. The performance requirements for the driver stage of the Pre-Regulator IC are essentially the same as the Dual Driver's driver stage.

The experience gained from the Dual Driver development encouraged us to perform the necessary design iterations for the Pre-Regulator driver without committing to fabrication. As a result, only a single fabrication of the prototype IC was required to meet the desired performance criteria.
7.2.2 Dual Driver

A simplified block diagram of the prototype Dual Driver IC is shown in Fig. 7.2. An external resistor is used to set the oscillation frequency, and this clock frequency is digitally divided to yield a 50% duty ratio signal. The 50% duty ratio signal is then passed through a phase-splitter stage that generates two out-of-phase signals. Finally, these signals are buffered to provide the low impedance output required to drive the capacitive load. The additional drives for the shorting switches are also shown in Fig. 7.2. The actual device included a few additional blocks, specifically an extra divider in the main chain that could be switched in or out, and a third divider block with some buffering that was used to provide the synchronizing drive (at half the frequency) for the Pre-Regulator controller/driver. The design and performance of each of the functional blocks of Fig. 7.2 is described in the next section.

Features that the prototype Dual Driver IC did not incorporate, but would ultimately be required, in a stand-alone converter module are housekeeping features such as start-up sequencing, lock-out control, and the ability to synchronize multiple modules.

![Figure 7.2: Dual Driver Block Diagram](image-url)
7.2.3 Pre-Regulator Driver

The block diagram of the prototype Pre-Regulator Driver IC is shown in Fig. 7.3. There are two input signals. One is the synchronizing clock signal from the Dual Driver, and the other is an analog voltage that commands the duty ratio of the output. As Fig. 7.3 shows, the synchronizing signal is used to generate a pulse that is, in turn, used to periodically reset an integrator. This creates a sawtooth waveform. The sawtooth waveform is then used as one input to a comparator, with the other input being the Command Voltage, to implement the triangle intercept technique for generating a PWM signal.

In this prototype Pre-Regulator Driver, an external resistor is used to control the current source that sets the slope of the sawtooth waveform, as shown in Fig. 7.3. An additional resistor, which is not shown in the figure, is used to establish the bias currents in the comparator. Ultimately both of these external components could be eliminated.

The prototype Pre-Regulator Driver is an open-loop device which in our application will eventually be placed in a feedback loop. So looking beyond this work, the next set of issues that must be addressed to achieve a stand-alone converter include: current and voltage sensing, transmitting information across the isolation barrier, incorporating amplification and compensation in the Pre-Regulator IC, and the same type of housekeeping issues the dual driver faces, particularly the sharing of currents between multiple units with paralleled output stages.

7.3 Integrated Controller/Driver Building Blocks

The design, implementation, and experimental performance in the prototype controller/driver ICs of the functional building blocks needed to implement the Dual Driver and Pre-Regulator Driver ICs of Figs. 7.2 and 7.3 are described in this section.
7.3.1 Schmitt Trigger Oscillator

The basic principle of the oscillator design was to time the duration of a linear ramp waveform between two voltage levels, $V_H$ and $V_L$. This was implemented, as shown in Fig. 7.4, with a current-sourced inverter stage charging a capacitor used to generate the triangle waveform, and a Schmitt Trigger buffer used to set the switching voltage levels.

Figure 7.5 shows the triangle intercept waveforms that generate the clock period. The ramp-up and ramp-down currents are assumed to be the same, $I$, so the time spent charging the capacitor, $C$, through $(V_H - V_L)$ is $T'/2$. This time is equal to

$$\frac{T'}{2} = \frac{(V_H - V_L)C'}{I} \quad (7.1)$$

After the ramp voltage reaches the Schmitt trigger's threshold, there is a delay (designated $\delta$ in Fig. 7.5) before the current source is switched to charge the capacitor in the other direction. This delay is the sum of the propagation delays through the Schmitt trigger and the current-sourced inverter. By the time the cur-
Figure 7.4: Schmitt Trigger Oscillator

Figure 7.5: Details of Intercept Waveforms

rent source has switched, the voltage has gone past the Schmitt trigger's switching level, so there is a further delay of $\delta$ before the capacitor reaches the switching level again (as shown in Fig. 7.4). So the total period, including delays, is

$$T = \frac{2(V_H - V_L)C}{I} + 4\delta$$  \hspace{1cm} (7.2)
The critical issue in the oscillator design was to minimize the temperature dependence of the operating frequency. To this end, efforts were made to minimize the variation of the charging currents, and the Schmitt trigger's threshold levels with respect to temperature, and also to minimize the delay around the loop ($\delta$). These efforts are described below.

**Current Source Biasing:** The current sources for the oscillator stage were generated using an off-chip resistor, $R_{ext}$, and the simple current mirror circuitry shown in Fig. 7.6. The width-to-length ($W/L$) ratios of the p-channel and n-channel MOSFETs are shown in the figure. Note that the dimensions are in $\mu$m. These ratios were chosen to achieve a bias current that is relatively independent of the device parameters and, therefore, parameter variations. This was achieved by dropping most of the available power supply voltage across the bias resistor. In this way large relative changes in device parameters do not cause corresponding large changes in the bias currents.

![Current Source Circuitry](image)

**Figure 7.6: Current Source Circuitry**

The large-signal device behavior of the MOSFETs can be approximately modeled by [53],
\[ I_D = \begin{cases} 
(W/L)K'\left[2(V_{gs} - V_t)V_{ds} - V_{ds}^2\right] & V_{ds} < (V_{gs} - V_t) \cdots (a) \\
(W/L)K'(V_{gs} - V_t)^2 & V_{ds} > (V_{gs} - V_t) \cdots (b)
\end{cases} \quad (7.3) \]

where \( V_t \) is the threshold voltage, and \( K' \) (which is different for n-channel and p-channel devices) is a measure of the conductivity of the inversion layer formed under the gate oxide that can be expressed as,

\[ K' = \frac{\mu \varepsilon_{ox}}{t_{ox}} \quad (7.4) \]

The voltage drop across the series connection of the bias resistor and the diode-connected n-channel MOSFET (N1 of Fig. 7.6) equals the supply voltage, and so can be written

\[ V_{DD} = I_D R + V_{GS} \quad (7.5) \]

and if (7.3b) is used to eliminate \( V_{GS} \) from this expression, it can be rewritten as,

\[ V_{DD} = I_D R + V_t + \sqrt{\frac{2I_D}{K'(W/L)N_1}} \quad (7.6) \]

This equation, which is quadratic in \( \sqrt{I_D} \), can easily be solved. Using the nominal process parameters for the MOSIS 3\( \mu \)m CMOS process of \( K'_n \approx 23 \mu A/V^2 \) and \( V_t \approx 0.75 \) V and a bias resistor of 130 k\( \Omega \), then with a 10 V power supply and a \((W/L)N_1 = 5\) the drain current is \( I_D \approx 63 \mu A \). The corresponding gate-source voltage is \( V_{GS} \approx V_t + 1 \approx 1.75 \) V, and the voltage drop across the bias resistor is approximately 8.25 V.

**Schmitt Trigger Design:** To appreciate the operation of the Schmitt trigger used in this design, it is first necessary to understand what factors determine the switching level of a simple inverter stage. A fairly good argument can be made based
solely on matching pull-up and pull down current sources. For example, consider
the inverter stage shown in Fig. 7.7.

Figure 7.7: Basic Inverter

The input voltage at which the pull-up and pull-down current sources match can
be calculated by setting

\[ I_{N1} = I_{P1} \]  \hspace{1cm} (7.7)

Assuming that both devices are saturated during the switching transition this ex-
pression can be rewritten using (7.3b) as

\[ \left( \frac{W}{L} \right)_{N1} K'_n(V_G - V_t)^2 = \left( \frac{W}{L} \right)_{P1} K'_p(V_{DD} - V_G + V_{tp})^2 \]  \hspace{1cm} (7.8)

For the purpose of initial design estimates, we can assume that \( V_t \approx -V_{tp} \approx 1 \text{ V} \).
So if we were interested in the ratio between the \( W/L \) of the P channel device and
the \( W/L \) of the N channel device that would be required to achieve a switching
level of \( V_{DD}/2 \), then the answer would be

152
\[
\left( \frac{W}{L} \right)_{N_1} K'_n \simeq \left( \frac{W}{L} \right)_{P_1} K'_p
\]

which is a well known result. Because we arrived at this point by equating the output currents, it should not come as a great surprise that this is also the criteria for achieving symmetric pull-up and pull-down transitions. It is common to assume that \( K'_n / K'_p \simeq 2 \), which dictates that the p-channel MOSFET have twice the \((W/L)\) ratio of the n-channel device, to achieve approximate symmetry in switching level and output transitions. This \( K'_n / K'_p \) ratio is only approximate as it varies between 2 and 4 for different fabrication runs. The nominal values of \( K'_n \) and \( K'_p \) are 23 \( \mu \)A/V\(^2\) and 7.5 \( \mu \)A/V\(^2\) respectively for the MOSIS 3\( \mu \)m process, which would give a \( K'_n / K'_p \) ratio of about 3, but the value is typically closer to 2.5.

Turning our attention to the Schmitt trigger circuit, the basic circuitry is shown in Fig. 7.8 and the operation can be explained as follows. If the input is low, then the output of the second inverter (which is the Schmitt trigger output) is also low, which means that the latching pull-up device, P2, is on. Similarly, if the input to the Schmitt trigger is high, then the output is high, and so the latching pull-down device is on. The regenerative action that occurs during switching is due to these latching devices. With the middle node of the Schmitt trigger, (labeled X in the figure), in its high state (input low) P2 is on. When the input voltage reaches the upper switching level going high, node X starts to swing low, when it reaches the switching level of the second inverter P2 turns off and N2 turns on to help pull node X down. Similarly, going in the other direction, when the input voltage reaches the switching level going low, then node X starts to swing high, and changes the state of the output which turns P2 back on and N2 off.

The switching voltage levels can be set, at least to a first approximation, using the same type of current balancing arguments we used for the simple inverter above. The upper Schmitt trigger switching voltage, which occurs when the input is low and going high, can be calculated from
\[ I_{N1} = I_{P1} + I_{P2} \] (7.10)

With P2 hard on, i.e., \( V_{GS} = V_{DD} + V_{tp} \), this can be rewritten

\[ \left( \frac{W}{L} \right)_{N1} K'_n(V_G - V_{tn})^2 = \left( \frac{W}{L} \right)_{P1} K'_p(V_{DD} - V_G + V_{tp})^2 + \left( \frac{W}{L} \right)_{P2} K'_p(V_{DD} + V_{tp})^2 \] (7.11)

Similarly for the lower Schmitt trigger level, which occurs when the input is high and going low, the switching voltage can be calculated from

\[ \left( \frac{W}{L} \right)_{P1} K'_p(V_{DD} - V_G + V_{tp})^2 = \left( \frac{W}{L} \right)_{N1} K'_n(V_G - V_{tn})^2 + \left( \frac{W}{L} \right)_{N2} K'_n(V_{DD} - V_{tn})^2 \] (7.12)

Consider, for example, trying to achieve switching voltages of 7 V and 3 V for \( V_H \) and \( V_L \) respectively. Again, we will assume that \( V_{tn} \approx -V_{tp} \approx 1 \text{ V} \), and we will use a \( K'_n/K'_p \) ratio of 2.5. Then equations (7.11) and (7.12) yield
\[ 90 \left( \frac{W}{L} \right)_{N1} \approx 4 \left( \frac{W}{L} \right)_{P1} + 81 \left( \frac{W}{L} \right)_{P2} \] \hfill (7.13)

and,

\[ 14.5 \left( \frac{W}{L} \right)_{P1} \approx 4 \left( \frac{W}{L} \right)_{N1} + 81 \left( \frac{W}{L} \right)_{N2} \] \hfill (7.14)

Assuming all of the \((W/L)\) ratios are in the same range, the smaller term on the right hand side of these equations can be ignored, simplifying these expressions to,

\[ \left( \frac{W}{L} \right)_{N1} \approx 0.9 \left( \frac{W}{L} \right)_{P2} \] \hfill (7.15)

and,

\[ \left( \frac{W}{L} \right)_{P1} \approx 5.6 \left( \frac{W}{L} \right)_{N2} \] \hfill (7.16)

A set of \((W/L)\) ratios that fits these relationships is \((W/L)_{N1} = 5/5, (W/L)_{P1} = 10/5, (W/L)_{N2} = 5/14, (W/L)_{P1} = 10/9\). These are the width/length ratios that were used in the experimental Schmitt trigger, which is shown in Fig. 7.9a. A SPICE simulation of the Schmitt trigger's input/output waveforms is shown in Fig. 7.9b. The SPICE models came from a previous MOSIS fabrication run. The thresholds are by no means identical to our design goals, but our rough calculations certainly put them in the right range.

**Minimizing Delay:** Because it is a majority carrier device, the MOSFET is potentially capable of very high speed operation. However, its performance is limited by parasitics and particularly parasitic capacitances. For a given MOSFET process, there is a minimum channel length \((L_{\text{min}})\) and a minimum width \((W_{\text{min}})\). For a circuit that is implemented with minimum size devices, the channel resistances will go as \(L_{\text{min}}/W_{\text{min}}\) and the gate capacitances will go as \(L_{\text{min}} \times W_{\text{min}}\). This results
Figure 7.9: Experimental Schmitt Trigger
in $RC$ products that go as $L_{\text{min}}^2$. So, based on this argument, the key to minimizing delay is simply to use minimum length MOSFET channels, with device width being fairly unimportant.

This argument holds as long as the dominant parasitic capacitance at an output is the input (gate) capacitance of the different loads that are being driven by this output. For logic gates with a reasonable number of loads (high fanout) or driving large interconnection capacitances this is true, but it does not apply for a chain of single gates with short interconnection lengths, where the object is to minimize the delay. In this case there is in fact a fairly substantial component of parasitic capacitance that is independent of gate width, so there is some benefit to increasing the width. In fact, the constant parasitic is the capacitance between the device's drain region and the substrate. The reason that this parasitic is constant is that there are minimum dimensions for this region which are larger than $W_{\text{min}}$. So, the device width can be increased until it equals the minimum width of the diffusion region without causing this parasitic capacitance to increase. In the case of the 3$\mu$m CMOS process the minimum dimension for this drain diffusion is 10 $\mu$m $\times$ 10 $\mu$m, so a standard CMOS inverter that has minimum delay will have $(W/L)_P = (20/10)$ and $(W/L)_N = (10/10)$.

**Experimental Results:** The circuit diagram of the complete oscillator stage, including the biasing, is shown in Fig. 7.10a. This was the final oscillator design, which was an improvement on the earlier designs. The oscillation frequency can be adjusted over a very wide range. The nominal upper operating frequency of 20 MHz is shown in Fig. 7.10b. The temperature dependence of the first design efforts were unsatisfactory, as much as a 3 ns/10°C change, which means that with a 50°C temperature variation the frequency of a 10 MHz clock would change by 15% (36% for a 20 MHz clock). The final design achieved less than 0.5 ns/10°C variation, so on the order of a 2.5% change of a 10 MHz clock (5% for the 20 MHz), for a 50°C variation.
(a) Circuit Implementation

(b) Experimental Waveforms

Figure 7.10: Experimental Oscillator
7.3.2 Phase Splitter

Relative timing of the drives to multiple power devices is a critical issue, particularly with power MOSFETs because of their rapid switching speed. In controllers implemented with standard logic ICs; for example, explicit delays are often added to one or more drive signal paths to rule out any possibility of conduction overlap. It is, therefore, critical to be able to generate out-of-phase drive signals that are timed more accurately than even an inverter delay.

The block diagram of the experimental phase splitter is shown in Fig. 7.11a and the detailed circuit diagram is shown with relevant \((W/L)\) ratios in Fig. 7.11b. From a static viewpoint, the two outputs are out of phase since one signal path has one inverter more than the other signal path. The effort in this design has been focused on achieving equal delays in the two signal paths in order to keep the signals perfectly out-of-phase. Crude \(RC\) models of the switching dynamics were used to develop this design.

The initial assumption was that in addition to balancing the delay in the two paths, we also wanted to lower the driving impedance as we went through the phase splitter so that the phase splitter could be then merged with the following Buffer. If we consider each unit-width of an inverter stage to have an effective resistance, \(r\), and capacitance, \(c\), then we decided to achieve the desired output impedance by scaling the inverters in the two-inverter path equally, so that the first inverter is \(b\) units wide and the second inverter \(b^2\) units wide. Similarly, the first two inverters in the three-inverter path are scaled by \(a\) and \(a^2\) respectively. Because we wanted both paths to have the same output impedance, the third inverter in the three inverter path was also \(b^2\) units wide. These scaling factors are shown in Fig. 7.11a, along with the input capacitance to each inverter stage (which is shown beneath the input) and the driving resistance of each inverter stage (which is shown above the inverters output).

The total delay through each path can be calculated by summing the component
delays, and these can be estimated from the $RC$ product of each stage. For example, the output resistance of the first inverter in the three inverter path is $r/a$ and the input capacitance to the next inverter is $a^2 \times c$, so the delay through this stage is approximately $(a)rc$. Similarly, the next delay in the three inverter path is $(b/a)^2rc$ and the delay in the two inverter path is $(b)rc$. So, equating the delays in the two paths yields

$$(a)rc + \frac{b}{a}^2rc = (b)rc \tag{7.17}$$

Canceling out the common $rc$ product in this expression gives

$$b^2 - ba^2 + a^3 = 0 \tag{7.18}$$

There are many pairs of numbers, $(a : b)$, that either exactly satisfy or come very close to satisfying (7.18). For ease of layout we were interested in whole number solutions, examples of which are $(a : b)$s of (4:8), (5:7), (5:18) \ldots. The minimum width of a MOSFET in the $3\mu m$ CMOS process is $4\mu m$, so the (4:8) and (5:7) pairs represent possible device widths for the input inverters. The absolute value of delay is proportional to the value of $b$ (either the 8 or the 7), so we chose the (5:7) pair, which resulted in the phase splitter circuitry shown in Fig. 7.11. The two transitions of the buffered outputs of the experimental phase splitter are shown in Fig. 7.12a. One transition is very well balanced with the two waveforms crossing right at the level of half the supply voltage, the other transition is a little off with the waveforms crossing about 1 V higher. The $\frac{dV}{dt}$ of the waveforms is about 4 V/ns as they cross, which indicates that they are timed to approximately 0.5 ns using the expression shown in the figure.
Figure 7.11: Phase Splitter
\[ \Delta t = 2\Delta V \left( \frac{dv}{dt} \right)^{-1} \]

Figure 7.12: Effect of Delay on Transition
7.3.3 Divider

The purpose of the divider is to generate a 50% duty ratio output from an input clock that is at twice the desired output frequency. The relative timing is not critical in the dual forward converter application because the two converters are independent, but there are other power converter applications where an accurate 50% duty ratio is very important (such as an H-bridge). The goal for the divider design was therefore to achieve a completely symmetric output waveform.

Asymmetry in the output waveform is caused by different delays between the active transition of the input waveform and the subsequent output transitions, as shown in Fig. 7.13. The difference between the duration of the high state and the duration of the low state is twice the difference in delays, as shown in the figure.

A Master-Slave $J-K$ Flip-Flop was used to implement the experimental divider, the logic schematic of which is shown in Fig. 7.14a. The experimental input and output waveforms are shown in Fig. 7.14b. The difference in time between the duration of the low and high states, $t_L - t_H$, is approximately 8 ns. This means that the difference in the delays, $(\delta_1 - \delta_2)$, is 4 ns. This can be understood by examining the detailed signal propagation in the $R-S$ latch which is the building block of the $J-K$ Flip-Flop.

The implementation and operation of a standard $R-S$ latch is shown in Fig. 7.15. The latch is implemented using cross-coupled NOR gates, as shown in the figure, and each NOR gate is assumed to have a switching delay of $\delta$. For example, when the $S$ input goes high there is a delay of $\delta$ before the $Q$ output goes low. With $Q$ high, the lower NOR gate inverts it to give $\overline{Q}$ low, so after $Q$ goes low there is a further delay of $\delta$ before $\overline{Q}$ changes state to a high logic level. The other switching transition of the latch is very similar. First $R$ goes high, which is followed a delay of $\delta$ later by $\overline{Q}$ going low. After $\overline{Q}$ has gone low there is a further delay of $\delta$ before $Q$ goes high. In a Master-Slave Flip-Flop the alternate rising edges of the $R$ and $S$ inputs are synchronized to the successive rising edge of the external clock, so it
\[ t_H = T - \delta_1 + \delta_2 \]
\[ t_L = T - \delta_2 + \delta_1 \]
\[ t_H - t_L = 2(\delta_2 - \delta_1) \]

Figure 7.13: Divider Asymmetry

is the propagation delay of the NOR gate used to implement the latch that causes the difference in delays for the two transitions of the divider.

Since completing the fabrication of the prototype ICs, we have returned to examine this issue of differential delay, and have developed a divider design that achieves nearly identical delays for the two transitions of the latch. This design is presented below and builds on the basic principle demonstrated by the phase splitter of matching the delays through two different paths.
(a) Master-Slave $J - K$ Flip-Flop Divider

(b) Experimental Waveforms

Figure 7.14: Experimental Divider
7.3.4 Improved Divider Design

Before trying to balance the delays in the two signal paths of the divider, we first attempted to minimize the delay through the \( R - S \) latch. We had used NOR gates to implement the \( R - S \) latch, with the NOR gate implemented as shown in Fig. 7.16. The devices are sized here to achieve approximately symmetric switching transitions using \( K_n' / K_p' \sim 2 \). If we assume that the two p-channel MOSFETs have pull-up resistances of \( R \), and that the output capacitance of the gate is \( C' \), then the pull-up and pull-down time constants are approximately \( 2RC' \).
Figure 7.16: NOR Gate Implementation

What if we had instead used NAND gates to implement the $R-S$ latch? Fig. 7.17 shows a NAND gate implemented with the same pull-up devices as Fig. 7.16. Because the high resistance pull-up devices are now in parallel, rather than in series, the pull-up and pull-down time constants are reduced to approximately $RC$, so the gate delay should be roughly halved.

The next step is to balance the delay through the two signal paths of the $R-S$ latch. The $S$ to $Q$ delay should be made $2\delta$, as shown in Fig. 7.18a, to balance the two delays, each of a single $\delta$, in the $R$ to $Q$ signal path. This can be achieved with the circuitry of Fig. 7.18b. Simulations of the complete divider, implemented with this latch, are shown in Fig. 7.19. The delay from input to output is almost identical for the two transitions. Figure 7.19c shows the transitions superimposed, showing that they are well timed.
7.3.5 Buffer Stage

We argued in the introductory section of this chapter that the lack of a high-performance CMOS driver stage had prevented CMOS technology from being utilized for controller/driver applications in the 1–10 MHz range. The development of a suitable driver stage was therefore a critical portion of this work.

The driver stage we developed is very simple, and is essentially a series of cascaded inverters, with each inverter stage being progressively larger to achieve a lower driving impedance. If a simple $RC$ model of the inverter is used, a scaling factor can be calculated that achieves a given impedance transformation with minimum delay. The result is a scaling factor of $\epsilon$ [53, pp. 258-261]. To achieve a driving impedance change from a minimum size inverter ($Z_{\text{min}}$) to a desired output impedance ($Z_{\text{out}}$) with minimum delay therefore requires $n$ stages, where
Figure 7.18: Balancing R - S Latch Delays
(a) two delay transition

(b) single delay transition
Figure 7.19: SPICE Simulation of Balanced Divider

\[ n \approx \ln \left( \frac{Z_{\text{out}}}{Z_{\text{in}}} \right) \]  \hspace{1cm} (7.19)

The sensitivity of the delay to changes in scaling factor is not particularly strong, however, so a slightly larger scaling factor can be used to effect a compromise between delay and the additional complexity of extra stages. The scaling factor we used was 5, which is shown by the MOSFET \((W/L)\) ratios of Fig. 7.20a.

The integrated shorting switch for the specialized MOSFET of Section 6.2.2 plays the same role as the output driver's pull down device in the stage, so it can be driven by the input signal to the last inverter stage, as shown in Fig. 7.20b. It is critical that this node be capable of driving the off-chip capacitance represented by the shorting switch without compromising the performance of the driver. We used SPICE simulations to study this drive scheme, paying particular attention to shoot
through currents, and found it to be completely adequate.

**Layout:** There were two critical issues to address in the layout of the driver stage. The first issue concerned the gate time constant, or, more specifically, the effect on the switch transitions of the delay contributed by the gate structure, particularly for remote portions of the gate. The commercial CMOS drivers we described earlier used long serpentine gate structures, resulting in considerable conduction overlap for the pull-up and pull-down devices, which caused large shoot-through currents during the switching transitions. We attempted to minimize this effect by limiting ourselves to gate structures with a maximum time constant of 1 ns.

A strip of interconnect of length $L$ and width $W$ has a total resistance $R = \rho L / W$, where $\rho$ is the sheet resistance with units of $\Omega/\square$, and a total capacitance of $C = C'L W$, where $C'$ is the capacitance/(unit square). So the total $RC$ product (which gives a conservative measure of delay for a discrete length of a distributed network) is $RC = \rho C'L^2$. The upper limit on the resistance of MOSIS's polysilicon gates are 30 $\Omega/\square$ and 80 $\Omega/\square$ for N and P channel MOSFETs respectively, and the oxide capacitance is nominally 0.7 fF/(\mu m)^2. These numbers give a 1 ns product with 210 \mu m and 130 \mu m gate lengths for the N and P channel MOSFETs. In our layout we therefore limited the gate poly lengths to no more than 100 \mu m. This means that the 8,000 \mu m wide P channel pull-up device was implemented with 80 separate gate fingers, with all of these fingers connected at the ends with metal interconnect.

The other issue of importance in the layout of the driver (buffer) was to minimize the inductance in the loops that charge and discharge the load. The charging loop is shown in Fig. 7.21a. The charging current comes from the off-chip bypass capacitor, $C_{ext}$, flows across the chip through the power supply lines, through the pull-up device, and out to the load. The current returns to the chip through the ground wiring, flows across the chip in the ground supply lines, and then back out to the capacitor. Similarly, as shown in Fig. 7.21b, the discharging loop is from
the load capacitance (the power MOSFET's gate capacitance) to the chip, then through the pull-down device on the chip, and back out to the load. We attempted to minimize the inductance of both of these loops by getting on and off the chip with multiple parallel interconnections, and, wherever possible, by using multiple overlapping conductor sheets both on and off the chip.

**Experimental Results:** Figure 7.22 shows the output waveforms of the experimental driver stage with a 300pF capacitive load. Although the experimental driver was mounted in a standard, 0.6in., 28 pin, DIP package, which limited the ability to minimize the critical inductances, this performance is better than the industry workhorse, the bipolar DS0026 driver IC, packaged in a mini-DIP.

The critical result is the reduced internal power dissipation. As we said earlier, the commercial bipolar and CMOS drivers both have excessive power dissipation in the 1–10 MHz range. The entire Dual Driver IC, oscillator, dividers, multiplexers, phase splitter, and drivers dissipated approximately 200 mW when operated at 5 MHz with a 10 V supply. With a capacitive load of $C_L$ the losses increased almost exactly by $C_LV_D^2$, so the effect of the load on shoot-through current, and associated losses, was deemed to be negligible.
Figure 7.20: Driver Circuitry for Power MOSFET with Integrated Shorting Switch
(a) charging loop

(b) discharging loop

Figure 7.21: Critical Charging and Discharging Loops of Driver
(a) Rise Time Driving 300 pF

(b) Fall Time Driving 300 pF

Figure 7.22: Buffer Output Driving 300 pF Load
7.3.6 Level Shifting of the Synchronization Signal

The synchronizing signal for the Pre-Regulator Driver IC comes from the Dual Driver. In the resonant forward converter application of Section 5.4, the supply rails of these two ICs are separated by $V_{\text{mid}}$, which is about 30 V. The synchronizing signal therefore has to be level shifted 30 V, which can be accomplished using the circuitry of Fig. 7.23. The output of the Dual Driver pulls up, and down, to both of its rails and thus has a voltage swing of $(V_{DD1} - V_{SS1})$. The input to the Pre-Regulator has this same voltage swing but the absolute voltage levels are raised by the level shifting capacitor which is charged to $V_{is}$, which is approximately equal to $V_{\text{mid}}$.

Ideally, the input voltage approaches, but does not exceed, the power supply rails of the Pre-Regulator Driver. If it does go outside the supply rails, it will turn on the input protection diodes each cycle. For the lower protection diode to be non-conducting during the time when the output of the Dual Driver is low the level shifting capacitor must be charged to greater than $V_{\text{mid}}$, or

$$V_{is} \geq V_{\text{mid}}$$

(7.20)

If this were not the case then the input to the Pre-Regulator would go below the lower supply rail of the Pre-Regulator Driver each cycle. This would forward-bias the input protection diode, which would turn on and charge the level shifting capacitor up until its voltage reached $V_{\text{mid}}$. Similarly, to keep the upper protection diode off when the Dual Driver's output is high, the sum of the output voltage and the level shifting voltage must be less than the level of the Pre-Regulator Driver's upper supply rail, or

$$V_{DD1} + V_{is} \leq V_{\text{buss}}$$

(7.21)

Now, because $V_{is} \geq V_{\text{mid}}$, this means that
Again, if the level shift voltage was high enough such that the inequality of (7.21) was not satisfied, then the upper input protection diode would turn on each cycle and discharge the level shifting capacitor until the condition was met.

The real point here is that the input voltage signal to any CMOS IC should stay within the IC’s voltage rails. In this case it means that the Pre-Regulator’s voltage supply should be greater than the Dual Driver’s. To limit any charging currents that do flow, particularly when the converter is powering up, we added current limiting resistors in series with the protection diodes, which are shown in Fig. 7.24.

\[ V_{buss} - V_{mid} \geq V_{DD1} \] (7.22)

Figure 7.23: Level Shifting of the Synchronization Signal
7.3.7 Pulse Generator

The function of the pulse generator is to produce a short sharp pulse whenever a rising edge is applied to it. This was achieved using the logic circuitry shown in Fig. 7.24. This circuit uses a race hazard condition to obtain a dynamic pulse, from what is ostensibly a static logic configuration. Viewed statically, the output of a NAND gate with inverted inputs is always a logical high, but if there is a short overlap of the two inputs in the high state, then the output will go low for the duration of the overlap. This overlap occurs on one transition of the input, resulting in an edge-triggered pulse, as shown in Fig. 7.24.

![Diagram of a race hazard pulse generator](image)

Figure 7.24: Race Hazard Pulse Generator

The detailed circuitry used for this pulse generator is shown in Fig. 7.25. The
'fast' input to the NAND gate, the signal that doesn't pass through the delay path, is tied to the NAND gate input that has the least coupling capacitance to the output node. This minimizes the effect of charge injection. In addition, a (2/3) n-channel MOSFET was used to cancel the charge injected by this 'fast' input, which is also shown in the schematic. Simulations were used to verify this pulse generator technique. The delay was adjusted by changing the size of the inverters in the delay path. A simulation of the pulse generator output is shown in Fig. 7.26a and the experimental pulse is shown in Fig. 7.26b.

![Diagram of pulse generator circuit](image)

Figure 7.25: Experimental Pulse Generator Circuit

### 7.3.8 Sawtooth Generator

The sawtooth was generated as shown in Fig. 7.27. A current source was used to charge up a capacitor, and a shorting switch was used to periodically discharge the capacitor. The discharging switch was driven with the output of the pulse generator and was sized to discharge the capacitor comfortably within the available time. The two issues in determining whether the shorting switch discharges the capacitor adequately, or not, each cycle, are the duration of the pulse from the pulse generator, $T_p$, and the resistance of the shorting switch. Basically the pulse
(a) SPICE simulation of pulse circuitry

(b) experimental pulse waveform

Figure 7.26: Pulse Generator Output
must last for many $RC$ time constants (we designed for $T_p \approx 10\tau = 10RC$). Process variations should not cause the ratio of $T_p/\tau$ to change significantly because both $\tau$ and $T_p$ are approximately proportional to the processes’ $R \times C$ product.

![Sawtooth Generator Diagram](image)

Figure 7.27: Sawtooth Generator

The detailed circuitry of the sawtooth generator and the associated biasing stage are shown in Fig. 7.28. A MOSFET's gate capacitance is highly non-linear in the region of its threshold voltage, so an n-channel device has a highly nonlinear capacitance between 0 and 2 V. As a result, the integrating capacitor was implemented using the gate of a p-channel MOSFET. Simulations of the combined pulse generator and sawtooth are shown in Fig. 7.28a and 7.28b, where the same bias current is used at two different clock frequencies. The operation of the experimental sawtooth could not be directly examined, but can be inferred from the overall results of the PWM output described in the next section.

### 7.3.9 Comparator-PWM Output

The comparator is used to generate the PWM waveform by comparing the sawtooth waveform with the analog input voltage. The circuit diagram of the comparator is shown in Fig. 7.29. The basic circuit operation is as follows. Starting on the left of Fig. 7.29, the two input signals are level shifted by P1 and P2, $(\frac{10}{3})$, which
operate as current-source loaded source-follower stages. These level shifted signals are then applied to the differential amplifier input transistors, P3 and P4, \((\frac{40}{3})\). The differential pair has a current doubling load formed by N1 and N2, \((\frac{5}{3})\). The output signal of the differential amplifier is then applied to a high gain amplifier stage, the common source amplifier of N3, \((\frac{20}{3})\), and its current-source load, to generate an output voltage that swings to both supply rails.

Simulations of the comparator's output are shown in Fig. 7.30 along with both input waveforms. The comparator delays are different for the two transitions, so the full range of the sawtooth waveform is not used.

**Experimental Results:** The experimental Pre-Regulator IC worked extremely well. Synchronized to a 2 MHz external clock, the IC achieved a variable duty ratio output as a function of input voltage as shown in the graph of Fig. 7.31. The output waveforms that correspond to the smallest and largest of these duty ratios are shown in Fig. 7.32. Initially there was a slight jitter in the duty ratio for low command
voltages, but this was overcome by increasing the bias current of the comparator. This makes intuitive sense since it implies that the problem was caused by charge injection into the high impedance nodes of the comparator, and that by effectively lowering the impedance of these nodes the charge injection was not as significant. We also found that there was a minimum length pulse that we could obtain from the comparator even for negative input voltages, and this could not be reduced short of removing the synchronizing clock signal. The cause would again seem to be charge injection, and this behavior is consistent with the right-half-plane zero in the differential amplifier's frequency response. This zero is due to transmission of the input signal directly to the output of the differential amplifier stage through the drain-gate capacitance's of the differential pair. The duration of this minimum pulse was about 20 ns, which corresponds to 4 % of the period at 2 MHz. It seems likely that this effect could be mitigated by attempting to cancel the injected charge.

The final question remaining to be answered is: how fast will the comparator and the overall PWM circuit operate? Without providing a definitive answer, we can at least demonstrate a PWM output at 5 MHz, as shown in Fig. 7.33. The upper waveform is the command input and the lower waveform is the PWM output, so the
(a) 0.5 V command voltage with 5 V peak sawtooth

(b) 2.5 V command voltage with 5 V peak sawtooth
(c) 4.5 V command voltage with 5 V peak sawtooth

Figure 7.30: SPICE Simulation of Comparator

Figure 7.31: Input Voltage vs. Output Duty Ratio at 2 MHz
(a) 10% duty ratio at 2 MHz

(b) 90% duty ratio at 2 MHz

Figure 7.32: Experimental PWM Operation
IC is going through step changes in the duty ratio. The minimum pulse width was again 20 ns, which means that the duty ratio can only go as low as 10%. To extend the frequency of operation, this minimum pulse width will have to be reduced.

Figure 7.33: 5 MHz PWMed Operation
Chapter 8

Some Alternative Topologies

This chapter presents several power circuit topologies and modifications to existing topologies that result from the detailed study of converter parasitics and their effects on the ideal operation of a particular converter topology. In the first section, techniques to reduce the turn-on stress and loss of the square-wave converter are examined. These are techniques that attempt to preserve the square-wave power transfer while achieving resonant switch transitions. In the second section, some ideas are presented for improving the performance of the resonant forward converter topology. These proposed modifications are all concerned with the rectification process, attempting to reduce the rectification loss, reduce the load regulation, and also propose a lossless drive scheme for incorporating synchronous rectifier devices.

8.1 Achieving Lossless Turn-On Transitions

In Chapter 3 we saw that the square-wave converter's turn-off transition causes a natural, and basically lossless, transfer of current from the MOSFET to the Schottky diode. This occurs because current is flowing from the node that needs to be discharged (node $X$ of Fig. 8.1), to the output, at the turn-off instant. The turn-on transition, by contrast, involves the forced charging and discharging of capacitances common to node $X$ in a dissipative manner, and the switch transition also results in load-dependent losses. We will now examine a number of techniques that avoid
some or all of these turn-on losses.

8.1.1 Discontinuous Operation

Converters designed with significant current ripple in the canonical cell’s filter inductor have smaller inductive energy storage requirements and more rapid response to load current transients, but at the expense of increased rms current stresses and capacitive filtering requirements. More relevant to the topic to be discussed here, however, is that a high-current ripple design also has different current stresses during the two switch transitions. With this difference it is possible to achieve an overall reduction in switching losses.

Consider, for example, a converter that is designed to be on the verge of continuous conduction at full-load. The MOSFET’s turn-on transition occurs with zero current in the canonical cell’s filter inductor so there are no load-dependent losses. The capacitive switching losses persist, however. The turn-off transition occurs with approximately twice the current it did before (with negligible ripple), so to keep the channel non-conducting and therefore remain lossless, the gate drive must sink twice the current it did before while still holding the gate voltage below threshold. The energy stored in the parasitic inductance at turn-off is increased by a factor of four, part of which is lost and may also lead to a higher MOSFET overvoltage, depending on the precise relationship between the ringing frequency and discharge time.

If the converter operates at a fixed frequency, then, with lower than full load, the current will fall to zero, allowing the diode to commutate off, prior to the MOSFET turn-on. Node $X$ will proceed to charge up, with both device capacitances being charged in a ringing manner through the filter inductance of the canonical cell. If this ring were allowed to proceed, node $X$ would ring towards twice $V_{out}$ and would settle at $V_{out}$ if the ring were allowed to damp out. If $V_{in}$ is less than $2V_{out}$, node $X$ would ring as high as $V_{in}$, at which point the MOSFET’s body-diode will turn on and clamp this node until the filter inductor’s current falls to zero.
When the MOSFET turns on, the loss associated with charging the diode capacitance is less than before, since some of the charge has been supplied from the lower voltage output instead of all coming from the input. Similarly, some of the energy in the MOSFET's output capacitance is returned to the input voltage source (and some stored in the filter inductor) during the ring. As a result, the turn-on loss due to the MOSFET discharging its own output capacitance is also reduced. In general there is some energy in the filter inductor when the MOSFET turns on, but most of this will be recovered. Overall the switching losses are reduced, and the higher the voltage of node $X$ when the MOSFET turns on, the less total loss.

Unfortunately, the ringing frequency of the filter inductance and the parallel combination of $C_f$ and $C_d$ is typically on the order of the switching frequency. So, unless a significant portion of the cycle is sacrificed to this reset mechanism, the rise in the voltage of node $X$ prior to the MOSFET turn-on is not very significant. Losing a portion of the cycle has the effect of increasing the rms current which has motivated work on achieving a more rapid transition by allowing the filter inductor's current to go negative before the resonant reset begins.

8.1.2 Zero-Voltage Resonant Transition Converter

If the free-wheeling diode of the switching converter of Fig. 3.2 is replaced by a controlled switch, as shown in Fig. 8.1, then the current in the filter inductor, $I_o$, can go negative prior to turning the switch off. The result is a transition which is completely analogous to the lossless turn-off transition of the switching converter that we have already discussed. The current drives the voltage of node $X$ up until the main MOSFET's body-diode is forward biased and clamps it at $V_m$. Providing the MOSFET turns on before the current has fallen to zero, an essentially lossless turn-on transition results.

There are several penalties associated with achieving this lossless turn-on transition. The first penalty is that energy is taken from the load, stored in the filter inductor, and some of it is transferred back to the source during the reset process.
This means that the amount of energy transferred to the load each cycle by the canonical cell has to increase. So, in addition to the filter inductor's current going negative there is an increase in the peak positive current. Therefore, the \textit{rms} current is higher, the capacitive filter requirements are higher, and the peak inductive energy storage is increased. If the switching frequency changes with load so that a constant reset current is used, then the amount of energy returned to the input each cycle will remain constant. It is generally more desirable, however, to operate with fixed frequency control, which means that the $\Delta I$ each cycle will be constant. If the converter is operating completely unloaded, approximately one quarter of the rated load energy ($\frac{1}{2} L_I (\Delta I/2)^2$ vs. $\frac{1}{2} L_I (\Delta I)^2$) is cycled between the input and output each cycle.

Another drawback of this scheme is the need to synchronously drive the MOSFET that replaces the freewheeling diode. It is critical that only one device be on at a time, because conduction overlap will short out the input. Both switching transitions will be initiated by the device that is on, turning off. The complementary device should not be turned on until its body-diode has picked up the filter inductor's current, so the two MOSFET drives need to be fairly accurately timed. Synchronizing the drive is made somewhat difficult because the two MOSFET sources move relative to each other as the two devices switch. There is also the additional gate drive energy for the MOSFET that is acting as a synchronous
rectifier to be considered, although the overall rectifier losses may well be reduced.

This Zero-Voltage Resonant Transition technique has been utilized in a high-frequency converter design [29]. A numerical example presented with this work argued that with an input voltage on the order of 50 V, at a power level of 50 W, this technique will achieve higher efficiency than a standard square-wave converter for any switching frequency above about 200 kHz. The experimental results reported with this work were quite impressive. A dual flyback converter design operating at 1 MHz, employing the zero-voltage resonant transition technique, delivered 40 W from a semi-regulated 50 V buss (within 10%) to a regulated 3.3 V output with total operating efficiency (including drive and control power) of 76%.

The two MOSFETs in the flyback circuit are isolated by the transformer, so there is additional difficulty in providing synchronized gate drives. The synchronized switch on the low voltage secondary does, however, function as a low voltage synchronous rectifier.

8.1.3 Auxiliary MOSFET Square-Wave Converter

There are other schemes that can be used to achieve more benign turn-on transitions in the square-wave converter that are very similar to the forced commutation principles that are applied in SCR circuits. The circuit of Fig. 8.2 shows a possible implementation using an auxiliary MOSFET and a reset inductor (a series diode is shown to block negative voltages when the main MOSFET is on). The operation of this circuit is identical to that of a conventional square-wave converter, as described in Chapter 3, until the turn-on transition. The current commutation process begins with the auxiliary MOSFET being turned on. This applies the output voltage across the reset inductor, and the current in the reset inductance therefore increases linearly. When the reset current reaches the filter inductor's current, the free-wheeling diode turns off and a ring ensues between the reset inductance and the parallel combination of the device capacitances (node X rings around $V_o$, and as high as twice $V_o$ just as it does in the discontinuous converter). If the voltage of node
$X$ rings as high as the input voltage, it is clamped by the main MOSFETs body
diode, and this MOSFET can then be turned on with a zero-voltage transition.

When the main MOSFET turns on, the commutation circuit is carrying current,
and the reset inductance has stored energy that must subsequently be recovered.
One way to achieve this is to leave the auxiliary MOSFET on and clear the reset
inductance to the input voltage source through the main MOSFET, with the series
diode preventing the current in the reset branch going negative. A variation on this
approach would be to turn the auxiliary device off, and clear the reset inductance to
the main MOSFET's gate, as shown in Fig. 8.3a, thereby synchronizing the switch-
ing of the two MOSFETs, and supplying some, if not all, of the main MOSFET's
gate energy directly from the power circuit.

While this auxiliary switch scheme allows the main MOSFET to achieve benign
switching transitions, the auxiliary MOSFET contributes switching losses from its
own turn-on transition and there are conduction losses in both the auxiliary MOS-
FET and the series diode during the reset. Both MOSFET turn-on transitions are
zero-current transitions, however, so there are no load-dependent losses. In addi-
tion, the reset current does not have to flow for much of the cycle so the rms
current in the auxiliary MOSFET can be quite low. This means that a device can
be used that is much smaller than the main MOSFET, and because the auxiliary
MOSFET's capacitance is only charged to the output voltage, the additional ca-
pacitive switching losses can also be kept relatively small. It is also important to
note that the auxiliary MOSFET and main MOSFET have common sources so the
implementation of synchronous drive signals should be relatively straightforward.

A variation on this forced commutation scheme is to transformer-couple the
commutation circuit with the canonical cell's filter inductor as shown in Fig. 8.3b.
The magnetizing inductance of the transformer can function as the filter inductor.
This coupling allows a tradeoff between the auxiliary MOSFET's turn-on voltage
and the reset current and reset time. The turn-on voltage of the auxiliary MOSFET
will increase by $\frac{1}{n}$, the current in the reset branch required to initiate the resonance
(a) ideal topology

(b) resonant reset waveforms

Figure 8.2: Auxiliary MOSFET Square-Wave Converter
Figure 8.3: Variations on Auxiliary MOSFET Converters
will be reduced from $I_o$ to $\frac{n}{n+1}I_o$, and the subsequent ring will behave as if each of the ringing elements had been reduced to $\frac{n}{n+1}$ of its nominal value. The auxiliary MOSFET is only required to carry $\frac{n}{n+1}$ of the resonant current. For example, with a 1:1 turns ratio the turn-on voltage will double, but the reset current and time will both be halved.

There are many other forced commutation schemes that can be considered, but the underlying consideration that energy must be stored in an inductor prior to the charging of node $X$ will remain, and while some of this energy will be recovered, the total amount of energy lost in the commutation process must be less than the turn-on energy we are trying to save.

### 8.1.4 Summary of Lossless Turn-On Techniques

The switching converter operating in a discontinuous mode was seen to be capable of lossless transitions, but the resonance between the filter inductor and the capacitance of node $X$ was too slow and the voltage was only ringing towards twice $V_o$. The resonant transition technique addressed these limitations by storing energy in the filter inductor and thus driving the resonance. The disadvantage was the need for synchronized drives and a large amount of energy that was simply cycled from input to output. In a fixed-frequency converter, this cycled energy actually increased as the load was reduced. In the auxiliary MOSFET scheme, described last, the converter does not have to operate discontinuously and the reset inductor can be much smaller in value than the filter inductor, permitting more rapid commutation. Also, the two MOSFETs have common sources, so the gate drives can be easily synchronized, and even implemented, in a single integrated circuit. The disadvantages are: a minimum of three additional components, and once again the resonant reset ring is only driven by the output voltage.
8.2 Modifications for Resonant Forward Converter

This section presents several proposed topological modifications for the secondary side of the Resonant Forward Converter topology that are intended to address some of the limitations uncovered in Chapter 5. These ideas are not completely topology-specific, however, since they are applicable to other members of the forward converter family of topologies. Some of these techniques could also be applied to other single-ended circuits that are being developed for high-frequency operation, if they are configured as dual units. Nevertheless, in this section the Pre-Regulated Dual Resonant Forward Converter of Section 5.4 is used as the vehicle to describe and demonstrate these techniques.

8.2.1 Lossless Gate Drives for Synchronous Rectifiers

The principle of synchronous rectification is discussed in Chapter 3, and requirements are established there for the successful implementation of synchronous rectification in high-frequency converters. These requirements are: that the gate drive be well synchronized, that it fall within the desired conduction interval, and that loss-less gate drive techniques be used to achieve efficient operation for frequencies on the order of the break-even frequency of the available MOSFET technology.

A technique that fulfills these requirements for the dual resonant forward converter is shown in Fig. 8.4. The gates of the MOSFETs are connected in a cross coupled fashion to the complementary secondary winding, which results in the gate drive waveforms shown in Fig. 8.4. These gate drives are well synchronized to the conduction period, because the primary side MOSFETs (whose turn-off transitions initiate the basic resonances that provide the gate drive) are driven by complementary signals. Furthermore, the Synchronous Rectifier gate capacitance is incorporated into the resonant circuit, being incrementally in parallel with the primary and secondary switch capacitances, so the gate drive energy is supplied in a lossless fashion.
Figure 8.4: Synchronous Rectifier Drive Scheme
The gate drive signal itself has essentially the same waveshape as the drain-source voltage of the primary MOSFET during its off-state resonance, except that the magnitude of this voltage is reduced by the turns-ratio of the transformer. The drain-source voltage for linear resonant capacitors can be expressed during the resonance as

\[ v_{ds}(t) = V_{in} + V_p \sin(\omega t - \alpha) \]  \hspace{1cm} (8.1)

Now, for a 50% duty ratio we found that \( \alpha = 26^\circ \) and that \( V_p = 2.28V_{in} \). So for an input voltage of 40 V, with a transformer turns-ratio of seven to one (for a 5 V output), the synchronous rectifier gate voltage can be expressed as

\[ v_{gs}(t) \simeq 6 + 13 \sin(\omega t - \alpha) \text{V} \] \hspace{1cm} (8.2)

For a given threshold voltage of the synchronous rectifier, \( V_{th} \), the proportion of time that the gate drive is above the threshold can be written as

\[ \frac{t_{on}}{dT} = \frac{\pi + 2\beta}{\pi + 2\alpha} \] \hspace{1cm} (8.3)

and \( \beta \) can be calculated from,

\[ 13 \sin \beta = 6 - V_{th} \] \hspace{1cm} (8.4)

A 2 V threshold voltage would yield \( \beta = 18^\circ \), which, if substituted into equation 8.3 (with \( \alpha = 26^\circ \)), would indicate that the gate drive voltage is above the threshold for 93% of the conduction interval.

If the resonant capacitance is dominated by nonlinear junction capacitances, as it is for the high-frequency resonant forward converter, then the gate drive waveform will be somewhat different as we discussed in Section 5.1.3. The peak of the voltage
will be higher and the beginning and end portions of the waveform will be lower; thus the time spent above threshold will be reduced.

While this drive scheme addresses several key problems of high-frequency synchronous rectifier implementation, there is still the problem caused by the current that is being carried by the MOSFET when its channel turns off. The leakage inductance of the transformer prevents this current from being rapidly reduced to zero, so as the MOSFET turns off an alternate conduction path is required for this current. One option is an integrated parallel Schottky contact, and another is to utilize the MOSFET's own body diode, as we discussed in Chapter 3. The first option entails considerable additional processing effort and is therefore not terribly attractive. The second option cannot be implemented with today's power MOSFETs because of their poor recovery times, and this was one motivation for the work on specialized synchronous rectifiers described in Section 6.2.2. A third option, which is explored in the next section, is to tailor the rectified current waveform so that the current is low at both ends of the synchronous rectifier conduction interval.

8.2.2 Resonant Secondary

The resonant forward converter utilizes all of the parasitics of a switching forward converter except for the leakage inductance of the transformer and associated interconnection. In Section 5.1.2 we showed that the leakage causes a slow rise in the secondary current which makes the turn-on transition of both primary and secondary switching elements quite benign. However, we also saw that this benign transition was achieved at the expense of increased load regulation, and a very high frequency ring that occurs at turn-off and is a source of loss. Finally, as we saw above, another effect of the leakage inductance is that it impedes the use of synchronous rectifiers to improve rectification efficiency.

Notwithstanding the negative effects of the leakage inductance, we concluded in Section 5.1.2 that a leakage inductance on the order of 1-2% of the transformer's magnetizing inductance could be tolerated without unacceptable degradation in
performance. If such a small leakage were unattainable, however, (e.g. because of safety isolation requirements) there is a modification to the basic topology that could mitigate the effects of the leakage inductance.

The modified topology utilizes the leakage inductance of the forward converter’s transformer and an output filter capacitance in a ring that occurs while the primary side MOSFET and the secondary rectifier are on. The modified secondary of the single-ended resonant forward converter is shown with the basic waveforms in Fig. 8.6 and the operation can be explained as follows.

As the primary and secondary switching devices begin to conduct, the difference between the voltage across the transformer secondary and the output capacitor’s voltage appears across the leakage inductance (neglecting rectifier drop). A resonance ensues: first the secondary current builds while the capacitor voltage \( V_c \) continues to fall, continuing until the current in the leakage inductance equals the output current \( I_o \). The elements continue to ring with the secondary current rising until the capacitor voltage equals the secondary voltage \( V_{sec} \) and then beginning to fall as the capacitor voltage rises above this. Eventually, the current attempts to ring negative and is prevented from doing so by the rectifier. Ideally the point at which this current reaches zero corresponds to the instant when the transformer secondary voltage begins to fall because of the primary MOSFET’s turn-off transition. The periodic cycle is completed during the subsequent off-time of both switching devices as the capacitor voltage is discharged linearly by the output current.

During the resonance, the capacitor voltage rings around the value of the transformer secondary voltage \( V_{sec} \) and the transformer current rings around the value of the output current \( I_o \), as shown in Fig. 8.6. The average value of this resonant current equals \( I_o \). With reference to Fig. 8.6, and using the same basic terminology that we used for the primary MOSFET resonance in Section 5.1.1 (which is very similar), we can write
(a) Equivalent Circuit

(b) Output Waveforms

Figure 8.5: Resonant Secondary
\[
\frac{I_o}{I_p} = \sin \alpha 
\]  \hspace{1cm} (8.5)

and

\[
\frac{V_a}{V_p} = \cos \alpha 
\]  \hspace{1cm} (8.6)

If the resonance is exactly timed to coincide with the on-state of the primary MOS-FET, then the duration of the ring can be expressed as

\[
(\pi + 2\alpha)\sqrt{L_{lk}C_o} = (1 - D)/f_{sw} 
\]  \hspace{1cm} (8.7)

The value of \( V_a \), the initial voltage difference that appears across the leakage inductance, can be calculated from the change in voltage that occurs when the output current linearly discharges the resonant capacitor while the transformer secondary is nonconducting, as

\[
V_a = \frac{I_o(1 - D)}{2C_o f_{sw}} 
\]  \hspace{1cm} (8.8)

Combining these relationships gives

\[
\tan \alpha = \frac{2D/(1 - D)}{\pi + 2\alpha} 
\]  \hspace{1cm} (8.9)

This transcendental equation is very similar to (5.5), the difference being a reversal in the relationship between the ringing interval and the duty ratio. Here, a higher duty ratio means more time available for the resonance, whereas in Section 5.1.1 the resonance occurred during the off-state, or \((1 - D)\), interval. As before, for a duty ratio of 50\%, (8.9) yields an \( \alpha \) of 26\(^\circ\). The relationship between the \( \text{rms} \) and average value of the secondary current can be determined analytically. For a 50\% duty ratio and an \( \alpha \) of 26\(^\circ\) this results in \( I_{\text{rms}} \approx 1.15 \left( I_{av}/\sqrt{d} \right) \), which is almost identical.
to the value for a sawtooth waveform of $I_{rms} = \left(\frac{2}{\sqrt{3}}\right) \left(\frac{I_{av}}{\sqrt{d}}\right) \simeq 1.15 \left(\frac{I_{av}}{\sqrt{d}}\right)$, which we discussed in Section 5.1.2.

Because the average voltage across the leakage inductance during the conduction period is zero, it does not contribute to load regulation in this scheme. Also, since the sinusoidal pulse of secondary current builds up from zero and rings down to zero prior to turn-off, both of the switch transitions are benign. The zero-current turn-off mitigates the problem of the lossy high-frequency ring. Furthermore, if this technique is applied in conjunction with the synchronous rectifier drive of the previous section, then the secondary current can be commutated off by the synchronous rectifier gate drive. Any residual current could flow into the parallel body-diode, or even the device’s output capacitance, since there should be very little energy associated with this current.

A definite drawback of this scheme is the more complex output filter stage required, and the fact that the current source load on the resonant output capacitance represents an additional impedance appearing in series between the capacitors that hold up the output voltage during load transients and the primary side capacitors. This inductance must only be a current source on the time scale of the switching period however, so an inductance that is, say, a factor of ten larger than the leakage inductance could be used.

### 8.2.3 Post-Regulation Utilizing Synchronous Rectifiers

The transformer in the Resonant Forward Converter achieves both isolation and impedance transformation, but a penalty is paid for this. Ideally, the forward converter is acting to periodically connect incremental voltage sources, but in reality the filter capacitors on the input and output sides of the transformer are separated by the leakage inductance and the resistance of the primary and secondary loops. It is the impedance separating these capacitors that causes load regulation, and also degrades the dynamic performance of the circuit. Generally, load transients must be handled by the secondary side capacitor until the primary side control can
respond, and this includes the delay involved with transmitting a signal across the isolation barrier.

The previous sections described techniques for reducing the resistive and inductive portions of this effective isolation impedance. Now we will consider a technique intended to cancel these dynamic changes out, so that incrementally the capacitors are back in parallel. The idea is to use synchronous rectifiers on the output to post-regulate the transformer output voltage, and so regulate against load changes. Used in conjunction with a pre-regulator stage, which is designed to overcome input voltage variations and supply the transformers with a well regulated bus voltage, this post-regulation scheme should permit separate, and independent, control on input and output sides of the transformer. By placing the primary and secondary capacitances incrementally in parallel, it also improves the ability to respond to load transients, allowing voltage hold-up capacitance to be provided on the high-voltage side. Another benefit of this scheme is that high-frequency feedback across the transformers isolation barrier is no longer required.

While an additional linear regulating element could be used to implement this post-regulation, the need to minimize the losses on the low voltage, high current, secondary side make this unattractive. The idea could be incorporated, however, with the synchronous rectifier drive scheme previously described by controlling the synchronous rectifier’s conduction resistance. One way to control the on-state resistance of the synchronous rectifiers would be to contact the bulk region under the gate, rather than shorting it to the source, and controlling the back gate bias. This body effect is not particularly strong, however, so a large control voltage would be required. Instead, the synchronous rectifiers could be operated as linear regulating elements by controlling either the level of their gate voltages or the duration of their on-times.

While this proposed post-regulation is dissipative in nature, it would not contribute any additional loss when the converter operates at its peak power level. Instead, it would be implemented so that the synchronous rectifiers are fully on at
peak power, and have a higher voltage drop as the output current falls. This means that the other losses in the converter will be falling as the post-regulator losses become significant. For example, if the load regulation over the full operating range were, say, 10%, then the peak dissipation from this scheme would in fact only be 2.5% of the full rated power and this dissipation would occur when the converter is operating at half its rated power.
Chapter 9

Conclusions

The power supply is essential to any electronic system, and has become a dominant component in modern electronic equipment because of its bulk, power dissipation and cost. The frontier of recent power supply research and development has been characterized by efforts to improve the efficiency, conversion density, and operating frequency of the power electronics. The ultimate goal of this development is the implementation of new and advanced distribution architectures, and the development of converter modules that can be manufactured and applied as standard components. The barrier to achieving these goals is the effect of parasitic reactance on the converter's operation as the frequency of operation increases. This thesis has focused on understanding the detailed effects of these parasitics, demonstrating that this knowledge can be used to improve a converter's operation, and developing new topologies that overcome, or utilize, the parasitics.

There are three important parasitics in the basic square-wave converter topologies: two device capacitances, and one inductance (which comes from the components and their interconnection, and includes the transformer leakage in transformer circuits). Understanding the detailed converter operation, particularly during the switching transitions, involved studying the oscillations between these three reactive components, as opposed to the more familiar two-reactance oscillations. While this analysis is more complicated, this thesis demonstrated that the detailed operation of the high-frequency square-wave converter can be understood in terms of the
oscillations that occur between these three reactances. The thesis also showed that this knowledge can be used to design more efficient, high-frequency square-wave converters.

The parasitic reactance losses in the square-wave converter have caused many people to turn away from square-wave conversion at high-frequencies and instead use resonant switching. With resonant switching, the dominant parasitics are incorporated into a resonant load and the switches undergo benign transitions. However, the resonant circuits have several fundamental disadvantages, which include: increased device stresses, additional filtering requirements, and variable frequency control. The variable frequency control is a problem, because EMI filters are typically tuned to reject noise over a narrow frequency band. The thesis discussed these tradeoffs between the square-wave and resonant approaches.

A particular resonant topology that has been used for high-frequency dc/dc conversion is the quasi-resonant converter, which has lower device stresses than the full resonant topologies. It was shown that the quasi-resonant converter has severe disadvantages when compared to a square-wave converter. The variable frequency control problem is particularly acute with this topology, since it requires a much wider range of frequency variation than full resonant circuits. Another problem with this converter is that its operation is strongly dependent on load. It was shown that if the quasi-resonant converter is designed for a wide load range, it loses the advantage of lower device stresses. On the other hand, if it is designed for a narrow load range, and is subsequently operated unloaded, it loses the benign switching transitions and experiences the same switching losses as the square-wave converter.

In the quasi-resonant topologies, two of the three parasitic reactances of the canonical switching cell are incorporated into the resonant load, namely, one of the device capacitances and the parasitic inductance. The third reactance, the other device capacitance, is often neglected, but it can severely impact the converters operation. The thesis showed that the effect of this additional reactance can be
understood, and quantified, by again considering networks with three reactances.

It was found that an important difference between the action of the parasitics in the resonant and square-wave topologies is that in the resonant circuits, only two of the reactances are involved in an oscillation at a time. In the square-wave converter, however, all three reactances are involved in high-frequency oscillations during both switching transitions. In the resonant circuit, the resonant inductor takes part in both the main and the parasitic resonance. As a result, it was demonstrated that the frequency and impedance of the parasitic oscillation is often comparable to the main resonance, producing a strong impact on the converters operation.

In a transformer application, such as a quasi-resonant flyback converter, the unused parasitic of the quasi-resonant circuit is the rectifier capacitance on the secondary, which is much smaller than the capacitance of the MOSFET, when referred to the primary. This mitigates the effects of the unwanted parasitic. Future efforts to improve low-voltage rectification efficiency are likely to dramatically increase the value of the rectifiers capacitance, which will bring the parasitic oscillation problem back into focus.

The thesis presented a resonant forward converter circuit that was developed to address the major weaknesses of the above quasi-resonant circuit. This converter is intended for applications where safety isolation is not required, so that the parasitic inductance can be minimized. Its operation is independent of load and is at a fixed frequency. This converter has lower device stresses than the quasi-resonant converter, operates its transformer symmetrically around zero flux, and uses both device capacitances in its resonant operation. There is still a parasitic oscillation caused by the neglected reactance, the parasitic inductance, which rings with the series combination of the device capacitances during the main resonance. However, the frequency of this parasitic ring is much higher than the main resonant frequency and the ring is well damped. Unfortunately this resonant forward converter has very limited regulation capability. To provide regulation in a point-of-load application, a square-wave pre-regulator stage was developed, which has extremely low switching
stresses. As a result, even though it is a square-wave stage, it can operate efficiently at very high frequencies.

The above resonant forward converter topology was used to implement a hybridized 40 V to 5 V converter, which achieved 100 W/in.\(^3\) conversion density, and 85% operating efficiency. Two interleaved converters were used operating at 5 MHz to achieve a ripple frequency of 10 MHz. The pre-regulator was designed to achieve regulation with an input voltage range of 30–40 V, and was operated at 2 MHz, dissipating only 2% of the total rated operating power.

A detailed understanding of a power converter's operation, and the effects of the parasitics on the operation, can be used to develop new converter topologies that exploit or overcome the parasitics. Topologies have been developed that use all three of the reactive parasitics. One example is the resonant forward converter topology, with resonant secondary, that was described in Section 8.2.2. Others researchers have accomplished this use of parasitics for the quasi-resonant topologies, which were described in [54].

While the resonant topologies discussed above permit higher frequency operation, they have significant drawbacks when compared to the square-wave converter. In particular the lower voltage stresses in the square-wave converter, especially for the rectifier component (because low-drop Schottkys have significant leakage), give it a strong advantage. It is, however, critical to reduce the switching losses to achieve higher conversion densities. Ideally a power conversion topology should operate with the low device stresses of the square-wave converter, and yet also achieve the benign switch transitions of the resonant converters. For this reason, the square-wave topologies with resonant commutation circuits, that were introduced in Chapter 8, seem particularly attractive for future miniaturization efforts.

Conventional, packaged components used in power converters are developed for general purpose use, rather than for specific applications. As a result, compromises are made in the component characteristics. While it may be sufficient to use unpackaged parts in high-performance, high-density, hybrid converter assemblies,
there is considerable advantage to be gained from developing specialized components for specific applications. This is particularly true of control/drive ICs, where many external components are required in conjunction with general purpose ICs. For this reason, a library of controller/driver integrated sub-cells needs to be developed so that application-specific designs can be rapidly implemented. CMOS is the ideal technology for this development, namely because of the library sub-cell mentality that is used by VLSI designers, the scaleability of the designs, the standardization of CMOS processes, and the intrinsically low power dissipation. Unfortunately, commercial CMOS controller/drivers have been inadequate in the 1–10 MHz range, because of excessive delays and dissipation caused by the parasitics in the integrated devices and their interconnections. The research presented here has shown that these problems can be overcome, and has initiated the development of high-performance CMOS controller/driver sub-cells, for high-frequency power conversion.

In conclusion, high-performance circuit design involves confronting and overcoming parasitics, and power circuit design is no exception. Whereas, in an iC the parasitics are in the junctions and the interconnections, in a high-frequency power converter the parasitics are found mainly in the reactances of the semiconductor devices and their interconnections. To achieve very high power conversion densities and operating efficiencies, power circuit designs will be required to devote the same attention to parasitic effects as are given to the ICs that they power.
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