Dynamic Error Correction Method
For High-Speed Analog-to-Digital Converters

by

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Abstract

This thesis presents a dynamic error correction method for improving analog-to-digital converters (ADCs) for spectral analysis applications. In particular, the correction method is aimed at reducing ADC error responsible for generating harmonic distortion components in the presence of large narrowband signals. At the heart of the correction method lies a two-dimensional error correction table that represents error in the "phase plane" of the analog input. That is, error values are indexed by both the ADC state and the slope of the analog input at the time of conversion.

Several applications of this method upon real converters are presented as experimental verification. For a pure sinewave input, compensation reduced the peak harmonic distortion components of a 12-bit, 5 MHz subranging converter by 10 dB over a 100 kHz bandwidth. Similarly, harmonic distortion was reduced by 5 dB over a 4 MHz bandwidth for an 8-bit, 50 MHz flash converter sampling at 25 MHz. Other results obtained using more complex input signals reveal the potential of the phase plane compensation method for solving real-world problems.

Thesis Supervisor: James K. Roberge
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To my mother and my father
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Chapter 1

Introduction

The research presented in this thesis focuses on error reduction techniques for improving the dynamic performance of high-speed analog-to-digital converters (ADCs). The need for enhanced ADCs can almost be taken for granted, since the ever growing desire to perform signal processing operations in the digital domain requires converters with increasingly higher sample rates and wider dynamic ranges. Consider the fact that, operating solely in the analog domain, one can obtain receivers with dynamic ranges in excess of 80 decibels (dB) and bandwidths of up to several tens of megahertz. Likewise, dynamic range in the digital domain is limited only by the digital word size of the hardware used, while bandwidth is determined by the conversion sample-rate. In translating between these two domains, however, one is fortunate to find an ADC with 12 bits (72 dB) of dynamic range valid over several megahertz. ADC technology is at least an order of magnitude behind current receiver technology and hence a limiting factor in the design of modern communication systems.

1.1 Motivation

Obviously, for error correction to be needed, ADCs must exhibit some element of error in the first place. In addition, the effect of this error upon digital systems must be significant enough to warrant the investigation of its removal. The ideas presented in this thesis grew out of initial efforts to understand these two issues more fully.1

Over the past three years a test bed has been developed at Lincoln Laboratory to characterize the performance of state-of-the-art ADCs with regard to applications in the communications/radar area. Of particular interest was the response of the ADC to large narrowband signals. Specific tests using sinusoids as models for narrowband signals were formulated to characterize the ADC's non-ideal (erroneous) behavior in ways meaningful to the intended applications, such as peak harmonic distortion versus input signal level and residual error versus input level.

An early conclusion from this work is that harmonic distortion generated by the ADC effectively reduces its dynamic range for applications involving spectral analysis. This is because the harmonic spurs, most of which are aliased, cannot be discerned from real signals by the signal processing algorithms. Any application using spectral analysis to detect signals needs to define a false-alarm threshold such that any signal which rises above it is virtually guaranteed to be a real signal and not some ADC-generated distortion component. Furthermore, to account for worst-case scenarios, this threshold must be placed above the highest harmonic spur generated by the ADC while sampling a sinewave of any amplitude or frequency in the desired band. This point of view toward ADC behavior indicates that an $N$-bit converter does not necessarily exhibit $N$-bits of spur-free dynamic range.

To reduce the level of harmonic distortion, many manufacturers recommend placing a sample-hold circuit (SHC) before the ADC. Since converter distortion depends mainly on the slope of the analog signal, significant improvement can be obtained by making the signal static at the time of conversion. The research completed at Lincoln Laboratory confirms that harmonic distortion is indeed reduced by using SHCs. However, even though some improvement is achieved, significant distortion still remains apparently because of problems in the SHCs themselves as well as interactions between the SHC and the ADC.

The results of the above research motivate the search for post-sampling algorithms that can remove the errors causing harmonic distortion from the converter's output. The problem presented is not trivial, since in general ADC harmonic distortion is a complex function of the frequency of the input signal as well as its amplitude. Although several papers and reports have been published outlining cor-
rection schemes for ADCs,\textsuperscript{2} \textsuperscript{3} \textsuperscript{4} the ideas presented by them are essentially static in nature and lack pertinence to the dynamic applications central to this study. Preliminary attempts at compensating ADCs with correction tables indexed by the ADC state demonstrated the repeatability of ADC error, yet failed to provide favorable results over wide frequency and amplitude ranges.\textsuperscript{5}

The solution presented in this thesis is unique in that it involves the application of a two-dimensional correction table to the converter's output sequence. It was felt that the addition of a second index to the table, an estimate of analog input slope, would allow the successful compensation of a broader class of signals. The structure of the two-dimensional table is analogous to the phase plane used to portray solutions to second order differential equations, since the phase plane is typically defined with an axis for the solution as well as an axis for the derivative of the solution.

The proposed "phase plane" correction table has the potential to remove ADC-generated harmonic distortion from a sinewave of any amplitude or frequency. It also allows the compensation of distortion components that are out of phase with the fundamental sinusoid, an ability lacking in one-dimensional methods. This feature derives from the property that the added dimension permits the compensation of converters with transfer functions that are not strictly real or memoryless.

1.2 Organization

The bulk of the thesis is divided into five chapters. Chapter 2 briefly develops the background needed for a full comprehension of the correction ideas presented in Chapter 3. Included in this discussion are basic quantization concepts, the types of ADCs examined, possible sources of harmonic distortion, and traditional methods for improving converter linearity.

In Chapter 3 two novel ways of approaching ADC error are presented. These are the statistical methods used to obtain ADC error and the organization of error


data into a two dimensional table, such that an error value is indexed by both ADC state and analog input slope at the time of conversion. This chapter will also contain sections on possible structures for implementing the phase plane compensation method.

Chapter 4 covers the experimental techniques used to test the compensation method as well as data obtained from several example applications. Data are presented that indicate several possible benefits of the phase plane method, for example:

1) Reduction of harmonic distortion in an ADC over a specified operating range.

2) Extension of an ADC's linearity to higher bandwidths.

3) Operation without the use of sample-hold circuits (in some cases).

Finally, conclusions will be presented in Chapter 5 along with a discussion of the limitations and applicability of the phase-plane approach. The chapter is concluded with recommendations for further research.
Chapter 2

Background Material

This chapter briefly reviews some of the basic concepts concerning analog-to-digital conversion. Sections are included that deal with ideal quantization concepts and the types of conversion architectures typically employed for high-speed conversion. Moreover, the possible sources of distortion from these architectures is reviewed, along with current approaches towards removing this distortion.

2.1 Quantization Concepts

The most natural place to begin this discussion is with a review of ideal ADC behavior. An ideal ADC or quantizer is a memoryless device which translates a continuous voltage range into a discrete number range (see fig. 2.1). Since the application of this function on an analog signal results in a loss of information, it is clear that the ideal ADC (and hence any real implementation) will exhibit a certain amount of inherent error, typically called quantization error or quantization noise. The shape of the quantization error waveform obtained when quantizing the input signal shown in figure 2.1 is also shown in that figure. The error waveform can be seen to oscillate over an interval of width one quantization step $Q$ or one least-significant-bit (LSB). The power in the quantization error waveform is commonly calculated by assuming it has a uniform probability density function (PDF) over this interval. This assumption yields the equation,

$$P_Q = Q^2/12R$$  \hspace{1cm} (2.1)

where $P_Q$ is the quantization noise power in watts, $Q$ is the quantum in volts and $R$ is the input resistance of the ADC in ohms.
For most devices dynamic range is defined as the ratio of the largest signal level to the smallest signal level that the device can accommodate. The dynamic range of an ideal \( N \)-bit converter is defined in essentially the same manner. It is typically expressed in terms of the signal-to-noise ratio of the device sampling a full-scale sinewave, where the noise is equal to the quantization noise:

\[
\text{SNR} = 10 \log \left( \frac{\text{Full-Scale Power}}{\text{Quantizing Power}} \right) \text{ dB.}
\]  

(2.2)

The full scale power \( P_{FS} \) is defined as:

\[
P_{FS} = (Q2^{N-1})^2/2R,
\]  

(2.3)

where \( N \) is the number of bits in the converter. Combining equations 2.1,2.2, and 2.3, yields:

\[
\text{SNR} \approx 6N + 1.8 \text{ dB.}
\]  

(2.4)

Equation 2.4 will be referred to the "6N" rule for estimating ADC dynamic range. This equation has a certain amount of intuitive appeal since one might expect the performance of the ADC to deteriorate at power levels lower than \( P_Q \). Applying this rule to a 12-bit converter, one would expect a dynamic range of roughly 72 dB.

Additional insight on the nature of the quantization error can be obtained through a straightforward computer simulation of an ideal 12-bit ADC using a sine
function for the simulated signal and a nearest integer function for the simulated ADC. Examination of the frequency content of a sampled version of the quantization error waveform can be performed by applying the Fast Fourier Transform (FFT) algorithm\textsuperscript{1} to the computer generated ADC samples. The FFT spectrum shown in figure 2.2 indicates that the sampled error waveform consists entirely of harmonics of the input sinewave.

Note that all of the power spectra presented in this thesis are displayed as a spectrum analyzer would show them. Power levels indicate actual power levels in the analog waveform and are not normalized as in most digital signal processing applications. Likewise, frequency represents the actual frequency of the signal and is not normalized to the sample rate. In the present simulation, one quantum $Q$ equals one millivolt and the input resistance equals 50 Ohms. The converter is sampling at 4.096 MHz.

The vertical line at 400 kHz represents the input sinewave, while the numbered spurs are at the harmonic frequencies of the input, which are aliased into the

Nyquist bandwidth. For reference, two horizontal lines have been drawn on the plot indicating the full scale power level \( P_{FS} \) and the quantizing power level \( P_Q \) in decibels relative to one milliwatt (dBm). One can see that no spur exceeds the \( P_Q \) level, while further analysis reveals that the sum of all spurs yields exactly \( P_Q \) as expected.

It is important to keep in mind that the input signal in this case is only a sinusoid. Sampling a more complex signal, or even a sinewave of a different frequency or amplitude, will produce a different sampled error waveform and hence a different power spectrum. In fact, the level of the quantization harmonics can be reduced by making the input signal sufficiently complex to destroy the periodicity of the error waveform. One simple and effective way of ensuring this complexity is to add a small amount of noise to the input signal before it is quantized, a process known as dithering.\(^2\)

The effects of dithering can be understood by returning to the ADC simulation. Figure 2.3 shows the spectrum of the original sinewave plus noise added before quantization with the computer’s nearest integer function. The noise is Gaussian with a power level equal to the quantizing power. The figure reveals that the energy previously contained in the quantization harmonics has been distributed over the entire Nyquist bandwidth. The input signal now rises above a noise floor that is much lower than the quantization harmonics of the previous figure. The average noise floor rises about three decibels above the line labelled \( P_{QF} \) that indicates the average quantizing power filtered into the resolution bandwidth of the FFT. The 3 dB difference reflects the fact that the signal now has twice as much noise power: the original quantization error plus the added dithering noise.

The implications of the above simulation are very important. Although adding noise decreases the signal-to-noise ratio, it allows a gain in the effective dynamic range of the ADC when it is used as a spectral analysis tool. This is because the indicator of dynamic range in spectral analysis is not the signal-to-total-noise ratio but the false-alarm threshold level used to screen out both noise and other spurious occurrences. Adding noise to an ideal converter allows this threshold to be lowered (and hence dynamic range to be increased) by any desired amount.

The actual amount of gain achieved depends on the resolution bandwidth of the FFT, which in turn depends on the number of points processed by the FFT. The

Figure 2.3: FFT spectrum of a quantized sinewave plus noise.

The exact expression for this "processing gain", which is equivalent to the difference between $P_Q$ and $P_{QF}$, is:

$$PG = 10 \log \frac{\text{Nyquist Bandwidth}}{\text{Window Bandwidth}} = 10 \log \left( \frac{K}{2c_W} \right) \text{ dB}, \quad (2.5)$$

where $K$ is the number of points in the FFT and $c_W$ is the resolution bandwidth of the window divided by that of a rectangular window. Thus, for the rectangular window, $c_W = 1$. Every time the number of points is doubled, the average noise floor is lowered by 3 dB. The previous two FFTs were each performed with 4096 points, yielding a processing gain of about 33 dB.

An important conclusion to be learned from this section, then, is that the "6N" rule for dynamic range is not entirely appropriate for ADCs used in spectral analysis applications. An ideal converter can have a dynamic range much greater than the "6N" rule implies, as long as it is dithered correctly and enough samples are processed by the digital signal processing algorithms. In practice, however, no real converter can benefit indefinitely from processing gain. At some point the device's harmonic distortion components will be revealed and at this point the false-alarm threshold is fixed by the highest harmonic. In this case the "6N" rule is still useful
for obtaining a grasp of the effective dynamic range or spur-free range of the device. For instance, a 12-bit device can have 13-bits of spur-free range (using the "6N" rule) if its peak harmonic distortion components are always 6 dB below the device’s \( P_Q \) level.

2.2 Conversion Circuits

The purpose of this section is to review the structure and performance of the conversion circuits typically used to realize the behavior of the ideal quantizer discussed in the previous section. Although many different structures exist, this discussion restricts itself to those circuits that can give the desired resolution (8 to 12 bits) at the high frequencies needed (1 to 100 MHz). First, the flash or parallel converter is discussed, followed by the sample-hold circuit used to improve flash converter performance. The subranging converter, which uses flash converters and sample-holds as components, is discussed next. The basic structure and some non-ideal, distortion generating effects will be examined for each circuit. Much of the material in this section, unless otherwise noted, can be found in the reference cited below.

2.2.1 Flash Converters

Flash converters are the fastest circuits for digitizing signals because they perform the conversion in parallel. Figure 2.4 shows a block diagram for a typical \( N \)-bit flash converter. The input signal is measured with a bank of \( 2^N - 1 \) latched comparators referenced one LSB apart. The encoding circuit merely determines the point in the string lying between on comparators and off comparators and translates this point into the desired \( N \)-bit representation. The circuit’s speed derives from the need to wait only the time required for a single comparator to settle (since they are all in parallel) before encoding.

From the standpoint of implementation, the flash converter’s only drawback is its complexity, since the number of comparators doubles every time the resolution is increased by one bit. This complexity typically places a limit on resolution of about 8 to 10 bits.

From the standpoint of performance, however, the flash converter has other problems. Namely, as the frequency of the analog input signal increases, the con-

Figure 2.4: Block diagram of a flash converter.
verter's linearity is degraded. One probable source of this distortion lies in the input capacitance of the comparators as seen by the reference network, labelled $C_R$ in the figure. This capacitance is variable and depends upon the differential input to the comparator (which depends, in turn, upon the analog input and the comparator's position in the ladder). The current needed to charge the $C_R$ for each comparator comes through the reference network, hence distorting the voltage references during sudden changes of capacitance (i.e. rapid variations in analog input).

Another likely source of distortion results from deviations in comparator settling times. The time required for each comparator to propagate its decision to its output varies because each comparator is slightly different. At low frequencies this presents no real problem. However, when the input signal is changing very rapidly, the comparator bank may not present a proper reading to the encoding circuit. Instead of one breakpoint between on and off comparators, one or two comparators below the desired breakpoint might remain off instead of on, thus confusing the encoding circuit. Depending on the position of the desired breakpoint, this behavior could result in a reading that is off by an LSB or so; or worse, a dropout to zero or full-scale.

Figure 2.5 shows the spectral response of a TRW TDC-1007J 8-bit flash converter sampling a spectrally pure 4 MHz sinewave at 12.288 MHz. The frequency content of the sampled signal contains a significant amount of harmonic distortion, dominated by the second which rises about 2 dB above the quantizing power level. In this instance, the spur-free range of the converter is some 2 dB less than the expected dynamic range of an 8-bit converter (using the "6N" rule).

### 2.2.2 Sample-Hold Circuits

As a means of correcting the above phenomena, many manufacturers recommend placing a sample-hold circuit (SHC) before the analog input. An SHC functions as a device that tracks the signal in one mode, then switches to another mode where the sampled signal is held at a constant level. The simple reasoning behind its use is that by presenting a static signal to the flash converter, most of the dynamic problems would be avoided. By the time the comparators are latched, the reference ladder input capacitance will have charged completely, while the held signal will have had sufficient time to propagate through every comparator.

Figure 2.6 shows a circuit diagram of a common SHC topology. An important element in the SHC is the analog switch, implemented here with a quad-diode bridge.
configuration. The switch is controlled with an external strobe that changes the bias of the diodes by raising or lowering certain nodes in the bridge. This configuration allows the very high-speed switching of analog signals with sub-nanosecond transition times. Following the switch is a capacitor used as storage for the sample while it is being converted by the ADC. Usually, the SHC is preceded and followed by high-impedence unity gain buffers. The preceding buffer provides current gain for charging the capacitor, while the succeeding buffer prevents the discharge of the capacitor into the quantizer.

Theoretically, placing an ideal sample-hold before a flash converter should result in a converter exhibiting only its constant static errors. However, in practice, any real implementation results in reduced quantizer distortion combined with SHC distortion. This can be seen in figure 2.7, which shows the spectral response of another TRW TDC-1007 converter sampling under the same conditions as in figure 2.5 but using a sample-hold circuit to “freeze” the input. In this case many of the harmonics have been reduced, yet the third is still only a couple of dB below \( P_q \). Though the converter is now achieving the expected 8-bit spur-free range, it is obvious that a reduction in the remaining spurs is required to approach the ideal
performance shown in figure 2.3.

In attempting to determine the source of the remaining distortions, one can try simulating a realistic model of an SHC followed by an ideal quantizer, though this approach is bound to neglect certain interactions between real SHCs and real ADCs. Judging from manufacturer’s specifications, there appears to be many possible SHC error sources to model. However, simple simulations show that properties such as the feedthrough of the input signal through the switch or the droop rate of the capacitor in hold-mode do not generate any harmonic distortion, since an SHC with these properties is still a linear circuit. Thus one must turn to nonlinear effects or processes that depend upon the input signal level in order to accurately model SHCs.

One such signal-dependent effect lies in a model developed for the quad-diode switch. This model indicates that the switch will not acquire a sample at equally spaced intervals of precisely one period \( \tau \). Rather, due to its structure, a slight variation in sample time will occur from sample to sample, a phenomena called aperture jitter. The nature of the quad-diode switch is such that it does not turn off until the hold-command signal or its complement intersects the analog signal,

---

as shown in figure 2.8. Thus the degree of error in the held signal depends upon
the level of the analog input at the sampling time as well as its slope. Computer
simulation of this phenomena shows that, with the proper choice of parameters,
this effect can yield odd harmonic distortion components that depend upon the
frequency of the input sinewave. The importance of this jitter phenomena to the
development of compensation ideas will become more evident in section 2.3 and
chapter 3.

In addition, there are several other possible signal dependent error sources com-
ing from the SHC that could be modelled. These include such features as the
sample-to-hold offset coming from stray charge being transferred from the switch
to the hold capacitor as well as nonlinear droop rates caused by signal-dependent
switch capacitances. It is also reasonable to expect the quantizer to exhibit some
element of dynamic error, since the signal presented to it is static for only a part of
the sampling period $\tau$. 

Figure 2.7: FFT response of a flash converter with sample-hold.
2.2.3 Subranging Converters

The last conversion circuit to be reviewed is the subranging ADC, an architecture that is used in high speed applications that require more bits than is possible to attain with the flash converter. The principle behind its operation is a two-stage conversion, a coarse conversion on the original input and a fine conversion on the amplified difference between the input and the coarse conversion.

As shown in figure 2.9 for a 12-bit example, the subranging converter is implemented in a fairly straightforward manner. The input signal is first passed through a sample-hold circuit that serves two purposes. It not only presents a static signal to the coarse converter, but also saves this signal for future reference. The coarse estimate is obtained with a 6-bit flash converter, then stored in a register and converted back to analog with a 6-bit digital-to-analog converter (DAC) having at least 12 bits of accuracy. This analog version of the digital coarse conversion is subtracted from the original analog sample, which has been stored for reference in an analog delay line. The difference is then amplified and converted with a 7-bit flash converter to form the fine estimate. The two estimates are then added together to form a 12-bit
output.

The extra bit is needed to smooth out transitions between adjacent coarse estimates. For example, if there is a mismatch between a threshold voltage in the coarse ADC and the corresponding output voltage in the DAC, the output of the subtracting circuit could fall outside the expected interval of 0 to 1 LSB of the coarse conversion. This overflow case is handled by the extra bit in the fine converter and corrected for in the digital correction logic that follows, a process called digitally corrected subranging. An interesting point concerning this process, and one of the reasons why sub-ranging converters are successful, is that the coarse ADC does not need an accuracy equal to the overall accuracy of the converter. As long as the DAC has the required accuracy, the digitally corrected subranging can account for coarse ADC errors.

Probably the most significant source of error in the subranging converter, then, is the coarse DAC. Any errors entering from this device are more significant than those resulting from the fine conversion process. Also, some element of error must be attributed to the SHC that acquires the signal initially, since it too must have an accuracy equal to the overall number of bits. A third possible source of error resides in the analog subtraction circuit, which must operate linearly in the face of rapidly varying signals. In fact, due to an almost inevitable mismatch between the time delays of the coarse conversion and the analog delay line, the amplifier following the subtraction circuit can be repeatedly driven into saturation.

Subranging converters typically perform very well when the signal remains within one coarse interval. However, when the signal begins to cross into adjacent sub-
ranging intervals, the performance deteriorates because of the interval mismatch remaining in spite of the digitally corrected subranging as well as amplifier saturation problems. Finally, as the signal approaches full scale, the dynamic behavior of the coarse flash converter becomes the dominant issue. Typical full scale behavior can be seen in the FFT spectrum shown in figure 2.10 for an Analog Devices MOD1205 12-bit, 5 MHz converter sampling a 2 MHz sinewave. Note the dominance of the second harmonic rising almost 8 dB above the $P_q$ level. The noise floor of this device and of subranging converters in general is considerably higher than the $P_{QF}$ level, probably due to the fact that any noise at the input is amplified prior to the fine conversion. In terms of spectral analysis, though, the limiting factor is the power in the peak harmonic spur.

### 2.3 Correction Schemes

With the inability of ADC circuits to perform adequately for certain applications, the search has been initiated for error correction schemes external to the device that can compensate undesirable behavior. To this end, much progress has already been
accomplished. The purpose of this section is to review elements of ideas already developed and to indicate where the appropriateness of these ideas diminishes with respect to spectral analysis applications. In general, the existing methods can be classified as static or dynamic, in order to separate those that deal primarily with static or DC behavior from those that deal with frequency related effects.

2.3.1 Static Methods

One of the more thorough discussions of error correction methods is presented in a doctoral dissertation by Millman.\textsuperscript{5} This work presents a fairly general approach toward formulating the most effective error-correction scheme for a given data conversion device ranging from ADCs and DACs to analog multipliers and angular-to-digital converters.

The key to the method presented is the search for the minimum set of orthogonal basis functions that will reach the most points in the device’s error space or error as a function of output level. Once this basis is found, the correction scheme is implemented by installing these functions with adjustable gains such that they can modify the converter’s output. For an $N$-bit converter, the object is to try to reduce $2^N$ correction values (one for each state) into only $N$ or so correction functions that can be adjusted to achieve the desired accuracy.

The nature of the basis functions depends upon the purpose of the converter as well as its internal structure. For example, a DAC would most likely use the square-wave Walsh functions to account for errors in bit weights and undesired bit interactions, while an ADC might use the power series or Legendre polynomials.

This approach is interesting and useful, but it only considers static effects and does not provide a satisfactory way of measuring ADC error. Presumably, one would need a higher quality “golden” ADC as reference, or perhaps a golden DAC to convert the sample back to analog and match it with the input. This approach will not work for the high-frequency spectral applications of interest because the devices are already approaching the limits of technology. Any reference converter would insert errors into the measurement that would be just as significant as those coming from the device under test.

The need for higher precision devices in order to measure ADC error is addressed

in a paper by Sloane.\textsuperscript{6} He overcomes this problem by using decaying exponentials generated from simple RC circuits as test signals to the ADC. A knowledge of the PDF of these signals allows one to measure error indirectly by analyzing histograms of large buffers of the ADC's output sequence.

The remainder of Sloane's technique involves transforming the measured errors into a measure of the actual bit weights for the device. In other words, the value of the $n$th bit of the device is modified from the ideal value of $2^{-n}$ to $2^{-n} - e_n$, where $e_n$ is the error contained in the weight of the $n$th bit. This approach is similar to Millman's work, in that the $2^N$ error values are accounted for with only $N$ modifications. However, the applications intended are still static in nature and it is not clear how to incorporate frequency dependent effects.

\subsection*{2.3.2 Dynamic Methods}

A paper by Vanden Bossche et. al.\textsuperscript{7} effectively translates Sloane's ideas into dynamic applications. Instead of decaying exponentials, a sinewave is employed as the test signal. Again, knowledge of the test signal's PDF allows the extraction of error information from large buffers of data. Using this method, one can measure the ADC's performance at any desired frequency, provided the frequency chosen does not result in only a reduced number of ADC states being excited (e.g. the Nyquist frequency). The authors do not outline a viable correction scheme with these ideas but instead offer them as a means to determine bit failures occurring in successive approximation ADCs, so that circuit adjustments can be made.

A method inherently different from the above methods, yet more relevant to spectral analysis applications, is given by Irons.\textsuperscript{8} By considering the amplitudes of the first $M$ harmonics in the FFT spectrum of a sampled sinewave, a trigonometric transformation yields a power series representation of the ADC's actual transfer function. Thus, an inverse transfer function or lookup table can be programmed into a memory chip positioned at the output of the ADC. The ADC's state will address the location in the memory containing the desired state and output this as the correct sample. This method, used currently in some actual ADC designs, avoids


reducing errors into a set of basis functions, since memory is relatively inexpensive and $2^N$ samples can be adequately accomodated by several moderately sized chips.

The results published by Irons show that this method can reduce dominant harmonic components by as much as 15 dB. Furthermore, they show that a converter's nonlinearities are repeatable, remaining constant over at least several hours. However, there are two basic problems with this method. The first and most obvious is that changing the sinewave frequency or amplitude will render the lookup table ineffective and even detrimental. This is because ADC error is also a function of analog slope, as described in the previous section, and changing the amplitude or frequency of a sinewave also changes its slope at every point.

The second problem with the lookup table approach is more subtle. Since the table is only one-dimensional, it is a memoryless function. As such it can only reduce harmonic components that are in-phase with the fundamental. Unfortunately, many error sources in the ADC are related to what the signal is doing at the time of conversion. They take on different values depending on whether the analog input is increasing or decreasing, which results in a sort of “hysteresis” effect. These error sources tend to generate harmonic products that are out of phase with the fundamental. Thus, careful examination of the FFT results will show that each harmonic has an in-phase and a quadrature-phase component 90 degrees out of phase with the fundamental. These quadrature components cannot be compensated by the lookup table approach and will always present a limit to one-dimensional compensation methods.

Further work by Irons\(^9\) is directed at solving the second problem. In particular, analysis of the aperture jitter phenomena described in section 2.2.2 revealed its generation of quadrature-phase error components. If this were an accurate model of all quadrature-phase sources, it might be possible to remove them or “de-jitter” the samples in preparation for lookup table compensation. An attempt was made to accomplish this by estimating the analog slope at sample-time with the uncorrected ADC samples. Using this estimate the error due to aperture jitter could be removed by projecting the sample back to the desired sample-time. The results were inconclusive but helped to generate the advanced compensation ideas presented in the next chapter.

In summary, the correction ideas presented in this section can best be characterized by their diversity. The most important point that might be learned from these examples is that the approach one uses to correct an ADC will be tailored by the application it is intended for. In this sense the ideas presented in the next chapter, rather than growing completely from existing methods, will differ as thoroughly from the above methods as they differ among themselves.
Chapter 3

Phase Plane Compensation

The purpose of this chapter is to present a new approach toward ADC compensation that yields promising results for dynamic applications. At the heart of this approach lies a two-dimensional correction table that removes ADC-generated harmonic distortion from sampled sinusoids varying widely over frequency and amplitude.

The method is referred to as phase plane compensation (PPC) because the structure of the correction table mimics the phase plane used to portray solutions to second order differential equations. In other words the correction table represents the phase plane through which the input signal travels. One axis is defined for the ADC state, while another is defined for the slope of the analog input at sample-time. This representation naturally accommodates error effects which are dependent upon the slope of the analog input and so should theoretically be able to remove the quadrature-phase components discussed in section 2.3 that limit one dimensional correction schemes. The trajectory of the input signal through the phase plane determines the sequence of error values to be subtracted from the ADC samples. Thus the compensation of sinewaves differing in frequency or amplitude is now made possible because a different trajectory is followed for every distinct frequency and amplitude combination. Figure 3.1 illustrates this property by displaying in the phase plane the trajectories of three sinewaves differing in frequency and amplitude.

The first section of this chapter will be devoted to briefly tracing the development of ideas from previous methods to the phase plane method. This section will not only review the results that suggested the investigation of the phase plane approach but also introduce a new means of measuring ADC error that makes this approach possible. The next section will explore the simplest possible architectures for implementing the PPC scheme for the correction of ADCs in real time. Three
structures are presented that may be chosen on the basis of bandwidth requirements. The third section will discuss the issues involved with using digital filters to obtain derivative estimates. Finally, the important process of table construction will be reviewed in the last section.

3.1 Development of Ideas

A brief summary of key results will show more clearly why the PPC method was adopted as the solution to removing ADC harmonic distortion from sampled sinusoids. Initially, the approach of Irons was considered the most relevant of the correction schemes presented in section 2.3 because it was centered upon spectral analysis applications. One of its limitations, discussed previously, is its inability to remove quadrature-phase harmonic components. Thus, the first steps taken involved determining how to remove this limitation to compensation schemes.
3.1.1 Measuring Error

The method that eventually solved the problem of removing quadrature distortion components grew from a new way of measuring ADC error. This measurement technique differs from any previous method because it involves the removal of an estimate of the input signal from a large buffer of ADC data and processing the residual errors left behind. Its own history can be traced to the residual error test which has been used widely to characterize the behavior of high-speed ADCs.\footnote{M. Neil and A. Muto, “Tests Unearth A-D Converter’s Real-World Performance,” Electronics, February 24, 1982, pp. 127-132.} \footnote{T. E. Linnenbrink, “Effective Bits: Is That All There Is?” IEEE Trans. on Instrumentation and Measurement, Vol. IM-33, No. 3, September, 1984, pp. 184-187.}

In the residual error test, a pure sinewave at a known frequency is sampled by the ADC. From a \( K \)-point buffer of ADC samples an estimate of the amplitude and phase of the sinewave can be obtained through either the Discrete Fourier Transform (DFT) algorithm evaluated at the given frequency or nonlinear least-squares techniques. In this thesis the rectangularly windowed DFT is the chosen approach and is defined as:

\[
X(\omega_l) = \frac{1}{K} \sum_{k=0}^{K-1} x(k) e^{-j\omega_l k \tau}
\]  
(3.1)

where the \( x(k) \) are the ADC samples, \( X(\omega_l) \) is a complex number containing the amplitude and phase information at the desired frequency \( \omega_l \), and \( \tau \) is the sample period. Once the amplitude and phase are known, an ideal sinewave of the given parameters is subtracted from the buffer of ADC samples, leaving a buffer of residual errors. This buffer contains the lump sum of all error sources generated from the ADC including quantization effects and harmonic distortion. The rest of the residual error test involves computing the power of this error sequence and dividing it by the quantizing power level \( P_Q \). The base-two logarithm of this number is then taken to form a “bits lost” measurement of the ADC’s performance. It should be noted that the above computation usually takes place on a computer having access to raw ADC data via some I/O arrangement.

One might notice that an alternative to reducing the information contained in the entire error buffer into a single residual power measurement is to process the error samples in terms of key parameters such as the ADC state that generated each error sample. This is the basis of the new ADC error measurement technique, which
will henceforth be referred to as the residual error measurement (REM) technique. The procedure is identical to the residual error test until the buffer of residual errors is generated. At this point the errors are accumulated in an array indexed by the ADC state responsible for each error sample. The number of error values accumulated in each entry of the error array is recorded in a second array. The process is repeated for $M$ buffers to insure that enough samples are accumulated for each ADC state. Finally, the average error for each state is computed using the second array. Thus an average error curve for the ADC's transfer function at a particular sinuswave frequency and amplitude is formed.

Since the above measurement technique is central to the PPC scheme as well, a review some of the issues associated with it is appropriate here. First of all, one might object to this procedure on the grounds that the "ideal" signal is estimated from the non-ideal samples of the ADC, many of which contain a significant amount of error. Although this is a valid objection, it is also clear that the effect of one LSB error in one ADC state upon the amplitude and phase of a buffer of 4000 points is going to be second order. There is no absolute standard for measurement here. The errors are considered to be deviations from statistical averages, a reasonable consideration provided the converter is already performing adequately well.

Another important point to note is that the input signal to the ADC must be highly filtered (pure) to prevent source distortion from appearing in the error measurements. This can be achieved with a high-quality low pass filter. Also, the signal must be dithered to prevent ideal quantization error from entering the measurement as well.

A third consideration arises from using the $K$-point DFT to estimate the amplitude and phase of the sampled sinuswave. Since the buffer is effectively the rectangularly windowed version of an infinite sequence, $\sin(K\omega/2)/\sin(\omega/2)$ distortion will occur in the frequency domain unless the buffer contains an integer number of sinuswave periods. This spectral distortion naturally invalidates any estimates of amplitude and phase coming from the DFT. It can be avoided by obeying the following relation between the calibration frequency $f_c$ and the sample rate $f_s$ ($= 1/\tau$):

$$f_c = l\frac{f_s}{K}, \quad l = 0, 1, 2, 3, \ldots$$  \hspace{2cm} (3.2)

Note that $\omega_l = 2\pi f_c/f_s$. In order to satisfy this relation exactly one must reference the calibration source and the sampling source to the same highly stable oscillator, otherwise frequency drifts between the two sources will introduce the above spectral
distortion.

One final issue places another constraint upon the choice of calibration frequency. Not only must an integer number of periods fill the ADC buffer, but also every ADC state should be included among a sample space of some \( M \), \( K \)-point buffers. Otherwise, the measured error function will be undefined at certain ADC states. For example, setting the calibration frequency equal to the Nyquist frequency satisfies equation 3.2 but could conceivably excite only two of the ADC states. An additional constraint that avoids this situation is to keep \( l \) in equation 3.2 an odd number, i.e. include an odd number of periods in the \( K \)-point buffers. This restriction forces the phase argument of the sampled sinewave to take on all \( K \) possible values.

3.1.2 Removing Quadrature-Phase Components

Figure 3.2 shows a typical error function for an Analog Devices MOD-1205 12 bit, 5 MHz converter. In this case, \( f_s = 4.096 \) MHz, and \( f_c = .499 \) MHz. The measurement was repeated with 100 buffers of 4096 points each. The curve is interesting because it indicates two sources of error. The error contributed by the coarse conversion process determines the relative deviations between the 32 subranging intervals. Within each subranging interval, the error due to the fine conversion is repeated more or less identically.

Figure 3.3 shows FFT spectra before and after error correction using the error function shown in figure 3.2. The components remaining after correction can be shown to be in quadrature to the fundamental. At this point, the residual error measurement technique has not gained significantly over the power series compensation discussed by Irons. The improvement obtained through either method is roughly the same, with both methods limited by the presence of quadrature-use distortion components.

The advantage offered by the REM technique lies in its ability to perform additional processing upon the error data. One possibility is to compute the standard deviation of the error measurement as a function of ADC state. This operation shows that some states have a much wider error distribution than others. These wide distribution regions are the points suspected of introducing quadrature-phase distortion components. Indeed, further analysis also made possible by the REM approach allows the classification of error by the polarity of the analog slope in addition to the ADC state. This results in the formation of two error functions: one to be applied if the signal is increasing, the other if decreasing. When these func-
tions are examined (see fig. 3.4) it becomes clear that the regions of wide standard deviation found on the original error function were caused by the averaging of two different error values depending on the polarity of the analog slope. A final check made by computing the standard deviations of the dual error functions reveals that the spread in error samples is now uniformly one-half LSB as expected.

Obviously, in order to implement such a slope-polarity based scheme some form of slope estimation is needed in order to indicate which function to apply. For simulation purposes, this can be obtained from the derivative of the estimated sinewave. However, a more practical approach was taken by using a polynomial based slope estimator developed by Irons for his work in de-jittering ADC data. The use of this estimator in the dual slope scheme generates the remarkable compensation results shown by the FFT in figure 3.5. Using this method, all distortion components, both in-phase and quadrature, are driven into the noise floor.

Unfortunately, these encouraging results are accompanied by the disappointing feature of sensitivity to the test sinewave parameters. Changing the amplitude by as little as several decibels turns the compensation from remarkable to disastrous. Similar behavior results from changing the frequency. A solution to this problem
Figure 3.3: FFT response before (above) and after (below) error correction using the error function shown in figure 3.2.
Figure 3.4: Error functions for positive (above) and negative (below) slopes.
Figure 3.5: FFT response after correction with the slope-polarity error functions can be imagined that would involve constructing separate tables for every amplitude and frequency combination and using some type of high-speed converter and Fourier Transform hardware to estimate which table is most appropriate for a given sequence of data. This solution, besides being enormously complex, would not fare well upon more complex signals containing multiple tones.

Fortunately, the presence of easily implemented slope estimators suggests the construction of a single table in the phase plane that can integrate the information needed to compensate any frequency and amplitude combination. In effect, the PPC method takes the slope-polarity scheme which already utilizes a second (albeit binary) dimension and increases the resolution along the second axis.

3.2 Implementation of the Phase Plane Method

The concept of a phase plane correction table has been introduced and the results encouraging its investigation have been presented. This section will outline four possible means of implementing this two dimensional correction approach. Basically, all four of the structures are very similar. Their main differences lie in their means
of obtaining the slope estimate for the second index to the correction table. It is desirable but not necessary to obtain this slope estimate in real time on a sample by sample basis. Three of the structures presented adhere to this property. The fourth uses an FFT and other hardware to provide compensation on a block of some \( K \) samples at a time.

### 3.2.1 Single Converter Architecture

The simplest structure for performing PPC is shown in figure 3.6. This architecture derives its slope estimate from the uncompensated ADC samples with a digital differentiating filter. While the types of filters available for this task are described in detail in section 3.3, adequate performance can be obtained with the simple Central Difference Estimator (CDE):

\[
\hat{x}(k) = \frac{x(k + 1) - x(k - 1)}{2\tau} \tag{3.3}
\]

where the \( x(k) \) are the indexed samples and \( \tau \) is the sampling interval. The only problem with the CDE is that its frequency response rolls off significantly from the ideal at frequencies greater than one-half of the Nyquist frequency or one-fourth of the sampling frequency. Restricting the input signal to frequencies well below this point, however, yields satisfactory performance. In fact, two examples discussed in chapter 4 utilize the CDE in this single converter architecture.

The operation of this architecture is straightforward. Immediately following the converter, the ADC samples are sent through two paths. One path leads into the differentiating filter while the other goes through a delay line equal to the delay of the filter. The output of the filter and the output of the delay line index
the appropriate cell of the correction table memory. The error thus indexed is subtracted from the ADC state \( x(k) \) to form \( \hat{x}(k) \), the corrected output state.

Note that \( \hat{x}(k) \) will be some \( q \) bits wider than \( x(k) \) depending upon the quantization performed upon the error points. This is typical of all architectures but does not mean that the converter can now be considered an \( (N + q) \)-bit converter. Rather, the extra bits are needed to specify the \( N \)-bit ADC states more precisely so that their overall accuracy is increased but not their resolution. This is an important point and worth considering further. The example in section 2.1 involving the simulation of an ideal quantizer shows that the effective resolution or dynamic range of a converter can be increased through processing gain provided the threshold voltages have sufficient accuracy. However, in order to realize this increase one must dither the input and increase the number of points processed by digital signal processing algorithms like the FFT and finite impulse response (FIR) filters.

The correction table memory can be implemented with either a read-only-memory (ROM) or a random-access-memory (RAM), depending upon the long-term stability of the ADC. The simplest choice is to use a ROM that is programmed once during an initial calibration phase and then placed into the compensation structure permanently. If the ADC tends to drift due to aging or temperature variations, a RAM would be used to facilitate periodic recalibration.

### 3.2.2 Multi-Rate Sampling Architecture

Figure 3.7 illustrates a slightly more complex implementation of the PPC method. This approach requires two ADCs. One ADC supplies samples with the desired resolution at the desired sampling rate, while the second ADC provides samples of a (usually) reduced number of bits at a sampling rate which is a factor of 8 or 10 higher than the first ADC's. For instance, this structure could be suitably implemented with a 12 bit subranging converter sampling at 10 MHz and a 6-bit flash converter sampling at 80 MHz.

Prior to sampling, the analog input is channelled into each converter. The output of the high-speed converter is sent through a differentiating filter, whose output is delayed a certain number of high-speed periods and then downsampled to the same rate as the slower converter. The output of the low-speed converter is delayed some number of low-speed periods so that the the sample \( x(k) \) appears at the index to the correction table at the same time as the slope estimate \( \hat{x}(k) \). From this point on the compensation proceeds in exactly the same manner as the single
converter architecture. Obviously, matching the delays of the two paths is an issue that requires scrutiny during the design phase.

Note that the high-speed converter is employed solely to supply derivative estimates for the correction table. Since it runs at a much higher sampling rate, it can provide an estimate of the slope of the signal in a time frame situated more closely to the desired sample-time. In this case the valid frequency range of the CDE operating on the high-speed samples extends well beyond the Nyquist frequency of the low-speed samples, though more complex differentiating filters might be used to average out noise.

Another advantage of the multi-rate scheme lies in its ability to shift the point where the derivative is taken to any point in the sampling period. This ability is useful in the event that some delay property in the ADC under compensation places more emphasis upon the behavior of the signal at some time prior to the actual instant when the sample is taken. If this turns out to be the case for some converter, then this multi-rate compensation architecture should provide a wider bandwidth of successful compensation, since it has access to a more relevant parameter.

3.2.3 Analog Derivative Architecture

A third possible implementation architecture is one that also uses two ADCs, yet in this case they sample at the same rate. The slope estimate comes from an analog differentiator which is sampled by the second ADC (see fig 3.8). This structure would be ideal for the fastest converters for which it is difficult to obtain the even
higher speed converters needed for the multi-rate scheme.

In terms of the digital hardware involved, this circuit is the simplest of all. The output of the two converters immediately index the desired location in the correction table memory. As in the previous examples, the indexed error value is subtracted from the ADC sample to form the corrected sample. Note that any delay between the two paths in this case must be dealt with in the analog domain.

The difficult part about implementing this structure lies in the design of an analog differentiator that works over the required frequency range. A simple op-amp design can be found in Senturia and Wedlock. However, the use of op-amps restricts the frequency range considerably.

### 3.2.4 Block Compensation Architecture

A fourth architecture that may be useful for some applications is shown in figure 3.9. This architecture processes blocks of \( K \) data points to form the compensated output. Whether or not it can provide a continuous stream of data depends on the speed of the digital hardware used. In many cases, however, discontinuous blocks of data are acceptable.

This architecture works by first collecting a buffer of \( K \) points. An "ideal" estimate of the analog derivative at each sample is formed as follows. First, an FFT is performed on the buffer to estimate the amplitude, frequency, and phase for the dominant components of the signal. The continuous-time input signal can be approximated with the sum of the dominant sinewave components. The time

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derivative is formed by summing the derivative of each component. In hardware, the derivative operation can be performed by adding 90 degrees to the phase and scaling the amplitude by a constant proportional to the frequency of the component.

Once the time derivative is formed, the compensation proceeds in the same manner as the previous architectures. The data buffer and the derivative samples are used to index values in the correction table memory that are subsequently added to the buffer points to form the corrected output samples.

Note that this architecture assumes a signal containing only narrowband energy at a limited number of frequencies. It would be difficult to operate it successfully in the presence of wideband signals.

### 3.3 Digital Differentiating Filters

This section will explore some of the alternatives available for implementing the digital differentiating filter required for the first two architectures discussed in the previous section. The frequency response of the Central Difference Estimator, which is used to generate some of the experimental results in chapter 4, is examined. It is compared to the ideal frequency response of a differentiator as well as the response of other more sophisticated implementations. The effect of windowing the
filter coefficients in order to smooth out the ripples caused by using a finite-length coefficient sequence will also be demonstrated. Finally, the issue of causality is examined and the behavior of the causal Backward Difference Estimator (BDE) is discussed. Almost all of the material presented in this section is available in more detail in the text by Hamming.\footnote{R.W. Hamming, \textit{Digital Filters}, Second Edition, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1983.}

The CDE has been introduced previously in equation 3.3. Without loss of generality one can set $\tau = 1$ and use the Discrete Time Fourier Transform to compute the frequency response $H(\omega)$ of this filter:

$$H(\omega) = j \sin(\omega).$$  \hfill (3.4)

The ideal response $\hat{H}(\omega)$ of a differentiating filter derives from:

$$\frac{d}{dt}[e^{j\omega t}] = j \omega e^{j\omega t},$$  \hfill (3.5)

which immediately yields,

$$\hat{H}(\omega) = j \omega,$$  \hfill (3.6)

where $\omega = 2\pi f/f_s$. Figure 3.10 shows the magnitude of the frequency response of the ideal filter plotted with that of the CDE both as a function of frequency normalized to the sample rate. Note that the phase of the frequency response for both the ideal filter and the CDE is a constant equal to $\pi/2$, since both responses are purely imaginary. As the figure indicates, the CDE response falls off rapidly from the ideal as $f/f_s$ passes one-fourth, and thus the filter cannot be used in this region.

In order to rectify this behavior a more sophisticated filter is needed. The steps taken to generate an arbitrary length FIR digital differentiating filter are presented here. The most general operation of filtering a sequence $x(k)$ with a $(2P + 1)$-point FIR filter is defined as

$$y(k) = \sum_{m=-P}^{P} h(m)x(k - m)$$  \hfill (3.7)

where the $h(m)$ are the filter coefficients and $y(k)$ is the filtered output. Choosing $h(m) = -h(-m)$, or filter coefficients with odd symmetry, yields the frequency response

$$H(\omega) = h(0) + j(2h(1) \sin(\omega) + 2h(2) \sin(2\omega) + \cdots + 2h(P) \sin(P\omega)),$$  \hfill (3.8)
Figure 3.10: Frequency response of the Central Difference Estimator and an ideal differentiator.
which is purely imaginary as desired if $h(0)$ is set to zero. The remaining problem is to choose $h(m)$ such that

$$H(\omega) = \sum_{m=1}^{P} 2h(m) \sin(m\omega) = \begin{cases} \omega & \text{if } |\omega| \leq \omega_c \\ 0 & \text{if } |\omega| > \omega_c \end{cases} \quad (3.9)$$

where the cutoff frequency $\omega_c$ is defined to allow the suppression of high-frequency noise components. The solution is obtained using the Fourier Series expansion technique, i.e. multiply both sides by $\sin(n\omega)$ and integrate:

$$\int_{-\pi}^{\pi} H(\omega) \sin(n\omega) = 2 \int_{0}^{\omega_c} \omega \sin(n\omega) \quad (3.10)$$

$$2\pi h(n) = 2 \frac{\sin(n\omega_c) - n\omega_c \cos(n\omega_c)}{n^2} \quad (3.11)$$

Now that an equation for the coefficients has been derived, the performance of the resulting filter can be compared to the ideal. Choosing $P = 10$ and $\omega_c = 0.3$ results in the frequency response shown in figure 3.11. Note how the solution tracks the ideal response and dies off much more sharply than the CDE. The ripples are caused by truncating a series that should ideally be of an infinite length. One way of reducing the ripples is to window the coefficients with the so-called Sigma Factors:

$$\sigma(P, m) = \frac{\sin(\pi m/P)}{\pi m/P} \quad (3.12)$$

This windowing of the coefficients in the time-domain can be alternately viewed as the convolution in the frequency domain of the rippled frequency response with a rectangular window of width $\omega = 2\pi/P$. In other words, the ripples are smoothed by taking the average of the frequency response over a width $f/f_s = 1/P$.

Figure 3.12 shows the effect of applying the sigma factors to the coefficients derived for the previous filter. The ripples of this smoothed filter are seen to have been reduced quite significantly, and a corresponding increase is obtained in the transition from derivative-band to stop-band.

There is an issue here concerning the fact that the differentiating filters thus created (including the CDE) are noncausal, i.e. they require future samples to determine the current derivative. From an heuristic point of view this seems to be acceptable since obtaining the most accurate derivative should require samples both prior to and after the desired time. The successive points are needed to place a sort of limitation on the behavior of the signal. However, in terms of ADC correction, it seems inappropriate to view ADC error as a function of future ADC samples. A
Figure 3.11: Frequency response of an FIR differentiating filter.

Figure 3.12: Frequency response of a smoothed FIR differentiating filter.
better solution might be obtained through the modeling of ADC history with causal filters.

One such causal filter that could be used is the Backward Difference Estimator (BDE):

$$\dot{x}(k) = (x(k) - x(k - 1))/\tau$$  \hspace{1cm} (3.13)

The frequency response of this filter (with $\tau = 1$) is:

$$H(\omega) = 1 - \cos(\omega) + j \sin(\omega).$$ \hspace{1cm} (3.14)

The magnitude of this function can be seen in figure 3.13 and compared with the response of both the ideal filter and the CDE. Although the BDE can be seen to track the ideal response better than the CDE, it has a troublesome phase response as shown in figure 3.14. Instead of the ideal constant phase at $\pi/2$, the BDE's phase decreases linearly from $\pi/2$ to zero. In spite of this undesirable behavior, the BDE presents a means of resolving the above issue on causality. Typical compensation results achieved with both the causal BDE and the noncausal differentiating filters are given in chapter 4.
3.4 Table Construction

One final aspect of the phase plane compensation method needing clarification is the generation of the correction table itself. It might be said that the whole PPC scheme hinges on the ability to construct a correction table. Fortunately, a method does exist, and the purpose of this chapter is to consider some of the issues involved and outline the approach finally taken.

One problem faced in creating the phase plane table is that of filling up a region of the phase plane that will contain any conceivable signal that might occur in the desired application. Of course, for one-dimensional schemes the region is clearly defined by the full-scale range of the converter. For the phase plane approach the region will typically include the entire ADC state axis as well as an area extending into both the positive and negative slope directions. The actual application will determine the exact shape of this region. For instance, most communications applications involving band-limited signals will seldom encounter a case where the signal exceeds the region bounded by the trajectory of a full scale sinewave at the maximum frequency in the band. The shape of this region is elliptical as can be
seen by referring to figure 3.1. One means of filling the operating region of the phase plane, then, is to start with a full scale sinewave at the maximum allowed frequency and decrement its amplitude to zero, thus tracing a series of concentric ellipses. As will be indicated later, this is the method currently employed for table construction.

An objection may be raised at this point concerning the wisdom of obtaining error information from the ADC at a single frequency, since to be successful the table must perform well over a wide range of frequencies. This objection is valid but results from viewing the compensation in the frequency domain. The basic assumption of the phase plane approach is that ADC error can be completely predicted by the two parameters ADC state and analog slope. If this is a valid assumption, then the frequency of the signal is irrelevant. The error response for each point in the phase plane is expected to be the same regardless of the frequency of the signal that excited that point. However, if higher order effects such as second or third derivatives do turn out to be significant then the table will require additional dimensions as well as calibrations at a number of different frequencies in order to exercise every point.

A third issue concerning the table involves its resolution. Although the phase plane used in the analysis of nonlinear dynamics is a continuous plane, the implementation of a phase plane correction table with a finite number of points requires quantization along both the state axis and the slope axis. It is tempting to consider defining a table with a horizontal resolution equal to the ADC’s LSB. An equally fine quantization along the vertical axis would require $2^{2N}$ points for an $N$-bit converter or 16 “Mega-points” for a 12-bit application. In spite of the fact that memory is fairly cheap, the size of such a table and the time required to generate error data to fill it immediately renders this resolution level impractical. Furthermore, the inaccuracy of the slope estimator (due to noise) would most likely preclude any advantage obtained through such resolution along the vertical axis. Clearly some additional quantization is needed. This issue will be reconsidered during the discussion of specific examples in chapter 4.

In terms of hardware, the following items are required for table construction. First, for reasons similar to those discussed previously, the calibration process requires a highly stable reference oscillator to synchronize the calibration signal source to the sampling source. Second, a high speed digital data buffer is needed to collect the ADC data and send it to a computer for further analysis (unless a dedicated
system is constructed for recalibration purposes). Third, a noise generator is needed for dithering the input signal. And fourth, the calibration signal must be low-pass filtered to prevent any source distortion from entering the calibration process.

One might note that for periodic recalibration, the integration of the above calibration system into the final application system is not an altogether unfeasible task. Considering that most communication systems already contain FFT hardware, the only additional items needed would be a highly filtered (pure) calibration source and a digital error processor capable of both applying the algorithm described below to the ADC samples, and also storing error measurements in the correction RAM.

Consideration of the above issues leads to the following method for generating tables. As discussed above, the table is constructed by linearly stepping a full scale sinusoid to zero amplitude level. The size of each step will be determined by the resolution of the table. At each step the following operations are performed:

1) A buffer of K points is collected and a DFT is performed to find the amplitude and phase of the calibrating sinewave.
2) An ideal sinewave (with floating point precision) is subtracted from the ADC data to arrive at a buffer containing residual errors.
3) The errors are accumulated in a matrix. Each error value is added to the matrix cell corresponding to the ADC state and estimate of analog input slope which accompanied the error point.
4) Steps 1 through 3 are repeated M times for averaging purposes.
5) The calibrating signal is decremented in amplitude for the next step.

After the last step is completed, the average error associated with each matrix cell is computed by dividing the total error accumulated in that cell by the number of error samples it has accumulated. The final error is then quantized to the desired word size to complete the table construction.

It will be noted that a good deal of the above method is based upon the residual error measurement technique discussed in section 3.1.1. The flexibility of this measurement technique cannot be overemphasized. It allows the classification of error values in terms of almost any parameter desired. For instance, if higher order effects were to be investigated, the REM technique would allow the classification of error by second and higher derivatives.

This section brings to a close our discussion of the phase plane compensation method. Results are presented in the next chapter for several examples that indicate the potential of this approach to solving real problems.
Chapter 4

Experimental Verification

The preceding chapter has developed the phase plane compensation approach in some detail, including approaches to implementation, table construction, and error measurement. At this point the ideas are ready to be tested. The purpose of this chapter is to present the results of performing phase plane compensation upon several actual ADCs.

Data will be shown for both the Analog Devices MOD-1205 subranging converter and the TRW TDC-1025 flash converter. These two devices are presented because they are typical choices for video-speed applications and because they are improved remarkably through compensation. Results are also shown for the Burr-Brown ADC-600, which is an excellent converter to begin with but difficult to improve greatly with compensation. The issue of using causal or noncausal filters for obtaining derivative estimates, first introduced in section 3.3, is considered further through the comparison of results obtained using the causal BDE and the noncausal CDE. Finally, results of compensating ADCs sampling signals other than pure sinewaves is included to indicate the potential of this method for solving real-world problems. Prior to showing this data, however, a discussion of the equipment and procedures used to test the uncompensated and compensated devices is in order.

4.1 Testing ADC Performance

The subject of testing analog-to-digital converters is a controversial one, mainly because there are a variety of possible approaches. The literature abounds with papers describing ways to measure such parameters as bits lost, aperture jitter, harmonic distortion and dropout behavior. The intent of this section is not to discuss the strengths and weaknesses of all the available means of testing ADCs but
to outline the particular test used to measure the improvements afforded through compensation in the examples to come.

4.1.1 ADC Test Bed

The philosophy held throughout the development of Lincoln Laboratory’s ADC test bed is that it should test the converters in an environment closely resembling that of the intended application for the device. Since the intended applications in this case primarily involve spectral analysis, the test bed is completely focused upon dynamic testing, with test results obtained through the processing of ADC data entirely in the digital domain. This approach differs not only from the static approaches used by many manufacturers to measure ADC resolution, but also from those dynamic approaches that convert the digital samples back to analog for testing. The Lincoln test bed is ideal for testing converters for digital signal processing applications.

A block diagram of the complete test bed is shown in figure 4.1. As indicated, test signals for the analog input can be either purely sinusoidal, purely noise (for noise-power ratio testing) or a combination sinusoid plus noise for dithering purposes. Before reaching the ADC device under test (DUT), the signals are heavily filtered with a signal conditioning unit. This unit houses a selection of low-pass filters having 90 dB stopbands and cutoff frequencies at octave values ranging from 500 kHz to 20 MHz. After filtering, the signals are combined and sent to the ADC. A third synthesizer provides clock signals to the DUT.

Immediately following the DUT is a high speed data buffer for collecting buffers of 128 K contiguous, 16-bit wide samples at clock rates of up to 250 MHz. This unit sends its captured data at reduced rates over the GPIO bus to an HP9000, model 20 computer for processing into test results. The computer also controls the instruments such as signal sources over the GPIB for the complete automation of tests. Not shown in the figure is a digital magnetic tape recorder for archiving test data.

The flexibility of the above test bed is one of its greatest assets. Not only does it provide a wide variety of testing options but also a perfect environment for investigating compensation approaches. It contains everything needed to simulate the phase plane compensation approach on real converters. The implementation of the single-converter architecture (see 3.2.1) is accomplished in software and easily tested with real ADC data. It can safely be said that the development of the new compensation ideas upon which this thesis is based would not have been possible

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Figure 4.1: Block diagram of Lincoln's ADC test bed.
without the use of this unique facility.

4.1.2 Spurious-Free Signal-Range Test

The test chosen as the most meaningful for measuring compensation effects is the Spurious-Free Signal-Range Test (SFSR). Initially developed to assist in setting the gain and dynamic range of the receiver that would be placed in front of the ADC in a real application, the SFSR test records the behavior of the ADC to sinusoidal excitation varying over the ADC's entire dynamic range. The parameter of interest is the difference in power level between the fundamental and the highest spur detected over the entire Nyquist bandwidth of the FFT spectrum. This is plotted versus the amplitude of the input sinewave at a particular sinewave test frequency.

The peak spur will usually be a random occurrence until the sinewave reaches a level that begins to stress the ADC into generating harmonic distortion components. For the results in the next sections, the rectangular window is used before transforming into the frequency domain to allow the most processing gain with the minimum amount of processing. Needless to say, in producing results care is taken to insure that the test frequency coincides with an FFT cell frequency.

Figure 4.2 shows the SFSR curve for a typical 8-bit flash converter. The "8-bit lower bound" line is defined as the difference between the input power level and the $P_Q$ level for the device. It represents the behavior of a device that obeys the "6N" rule and hence is independent of the processing gain. Another reference line labelled "Desired Response" indicates the performance of an ideal 8-bit converter given the amount of processing performed with the samples. This represents a false-alarm threshold in the FFT spectrum placed roughly 10 dB above the $P_{SF}$ level in order to screen out most random noise occurrences. One should remember that for all FFT-related data presented here, the power levels are shown as the analog input would appear on some analog measuring apparatus like a spectrum analyzer. Thus $P_{FS}$ represents the full scale input power level of the converter and is not arbitrarily set to zero decibels as in most digital signal processing applications.

The curve shows that for low input levels, higher bits of spur-free range (based on the "6N" rule) are achieved through processing gain because the spurs are lower than $P_Q$. As the signal level increases, however, harmonic distortion components begin to rise and pull down the SFSR curve until it eventually violates the "8-bit lower bound" line. An alternate way of viewing the same behavior is shown in
Figure 4.2: SFSR curve for a typical flash converter.
Figure 4.3: Power level of the maximum spur versus input level.

Figure 4.3. Here the power level of the maximum spur in the Nyquist bandwidth is shown, again plotted versus input level, along with the measured power of the fundamental. The SFSR curve plots nothing more than the difference between the two.

The SFSR curve is useful for both setting the operating range of the converter and indicating its subsequent performance. For instance, in order to maximize the input signal range while minimizing the spur threshold level, one traces along the peak spur curve in figure 4.3 starting at -50 dB. When a local maximum on the curve is encountered, a horizontal projection is drawn until it intersects the curve again. If the intersection lies near another local maximum, then a projection from this local maximum is drawn, and so on. The process ends when the projection intersects a point that lies on the upper region of the curve, where it increases with a slope greater than 1 dB/dB. The input level corresponding to this point, \( P_{\text{max}} \), is then regarded as the maximum power level for the input signal (instead of full scale). The power level that the horizontal projection is drawn at, \( \text{MAX} P_{\text{spur}} \), becomes the false-alarm threshold for deciding on the validity of a signal. When
these points are transferred to the SFSR curve in figure 4.2, the restricted response is seen to be slightly greater than the "6N" rule for an 8-bit converter, although the response is now shifted to lower input levels.

Based on this description, it should be obvious that the SFSR test provides a natural way of looking at how well compensation improves an ADC. A compensated ADC should show an SFSR response rising above the uncompensated response toward the "desired response" line at levels where harmonic distortion is significant. Alternatively, the peak spur curve is expected to drop to lower power levels. In addition, performing the SFSR test at several frequencies will allow the examination of compensation effects versus frequency.

4.2 Two Compensation Examples using the CDE

This section presents the compensation results obtained from two actual converters. The first converter shown is the Analog Devices MOD-1205. This converter is a 12-bit, 5 MHz subsampling device that lends itself well to compensation, mainly because it is stable over long periods of time. Correction tables several weeks old have demonstrated consistent improvement on this device. The second converter shown is the TRW TDC-1025, an 8-bit, 50 MHz flash converter. Compensation results obtained from this device indicate a wideband effect that may eliminate the need for using sample-hold circuits. Both compensation results were achieved by simulating the single-converter architecture on the ADC, with the Central Difference Estimator used to obtain slope estimates.

4.2.1 Analog Devices' MOD-1205

Figure 4.4 shows a phase plane compensation table obtained from the MOD-1205 converter. Error is shown on a 3D curve plotted against the ADC state and slope. One quantization interval for the device is plotted in the vertical direction for comparison to the error values in the plot. The application is for a 100 kHz bandwidth centered around 450 kHz, with a sample rate of 4.096 MHz.

Note the smoothness of the surface shown in the figure. Initial efforts using a table as small as 1024 points (32x32) provided outstanding performance against large amplitude signals, but a higher resolution was needed to obtain good results at low amplitudes. The table shown in the figure actually has 256 points defined along the ADC state axis and 128 along the slope axis, with a total of 256x128 =
Figure 4.4: Phase-plane compensation table for Analog Devices’ MOD-1205.

32768 points. For purposes of visual clarity, the computer plot shows the table at reduced resolution.

In terms of calibration, the following points are pertinent. First, the table was calibrated at a frequency of 497 kHz. Second, noise was added at a level of $P_Q$ to dither the signal. Third, the calibrating sinewave was decremented to zero in 512 steps. Finally, at each step a buffer of 16384 points was time-aliased (i.e. overlapped) into a buffer of 4096 points before using the DFT to estimate the signal’s amplitude and phase.

The method of time-aliasing is applied to almost all the data presented here and is used to average out noise effects without increasing the number of points used in signal processing algorithms like the DFT. In effect, time aliasing provides the processing gain of a high resolution DFT or FFT with the computational efficiency of a low resolution one. The result is an undersampled high resolution spectrum.

The total time required for the calibration is on the order of 3 hours. This may seem unreasonably long but it can be decreased by almost any factor with the use of more efficient transform algorithms or dedicated DSP hardware.

FFT spectra of a full scale tone before and after compensation are shown in figure 4.5 for a signal at the calibration frequency. Note the labelling of certain aliased harmonic spurs that rise above an arbitrary power level. The spectra indicate some
of the potential of the phase plane method, showing a decrease of about 30 dB in
the peak spur level.

Figure 4.6 shows the results of performing an SFSR test upon the uncompens-
sated and compensated ADC with a 491 kHz tone and a 391 kHz tone. Several
improvements are indicated here. Not only has compensation extended the 12-bit
behavior of the ADC to the upper 16 dB of its signal range, but much of the com-
pen sated SFSR curve has shifted toward higher resolution, i.e. more bits of spur-free
range. The effect of compensation is to move the worst case point on the SFSR
curve to lower input levels, where the limited resolution of the table affects its abil-
ity to compensate. The curves show that the overall reduction in peak distortion
level (determined by worst case points) is approximately 10 dB.

The glitch near the middle of the SFSR curves that pulls even the compensated
response down toward less resolution is attributed to the mismatch between the
lowest subranging interval and its surrounding intervals. Unfortunately, at this low
power level only a handful of different correction values are indexed by the signal,
making compensation difficult.

The fact that at some point compensation is limited by the resolution of the
table poses an interesting dilemma. On one hand, it is desirable to compensate
the ADC equally well over its entire dynamic range. This is difficult to do with a
table of limited resolution because large amplitude signals can index a much larger
number of distinct error values than a small signal can. Thus it is desirable to
increase the resolution of the table. On the other hand, the problem of dealing
with the 16 Mega-point table discussed in the previous chapter tends to prohibit
this. The optimal resolution has yet to be discovered, though a practical solution
might be achieved by implementing the table with a variable resolution. The outer
limits could afford to remain coarse while the resolution of the inner region or other
key areas of the phase plane could be increased dramatically. This approach, an
dexample of which can be seen in figure 4.7, would probably outperform the usual
constant resolution table and at the same time require only a moderate increase in
memory.

Another important result indicated by the SFSR curves is the performance ver-
sus frequency of the compensation method in this application. It is clear that the
491 kHz tone, which is nearer the table's calibration frequency, has been compen-
sated somewhat better than the tone lying 100 kHz away, though both are markedly
better than the uncompensated tone. This type of behavior could be the result of
Figure 4.5: FFT response before (above) and after (below) phase plane compensation for MOD-1205.
performance limitations imposed by the CDE estimator. Or it may indicate that the relatively straightforward implementation discussed so far needs to be modified for subranging ADCs like the MOD-1205 that have a complex internal structure for subtracting and delaying the analog signal. Possible solutions for extending the bandwidth of compensation in this case might range from optimizing the derivative estimator (see section 4.3) to including more parameters such as higher order derivatives in the lookup table.

In spite of all the issues listed above, the results of compensating the MOD-1205 are truly remarkable, since an SFSR increase of 16 dB has been obtained. These results were made possible with the CDE because the highest frequency of interest was still at roughly one-tenth of the sample rate. In order to obtain these results at any point in the Nyquist bandwidth, one must turn to the more complex differentiating filters discussed in section 3.3.
Figure 4.7: Illustration of a variable resolution scheme for the phase plane table.
4.2.2 TRW’s TDC-1025

A second application of the phase plane technique shows a wider useful bandwidth than the previous one. Figure 4.8 displays the correction table obtained from the TDC-1025 flash converter. The table has a resolution of 64x64 (4096 points) and was made with a 3.9875 MHz sinewave being sampled at 25.6 MHz (slightly more than half of its maximum rate). During calibration, the signal was stepped to zero in 128 steps, and at each step buffers of 16384 points were processed. Total calibration time was roughly three-quarters of an hour. The large spikes seen on the perimeter of the table are from cells that have accumulated too few samples for statistical accuracy and do not adversely affect the performance of the table.

The SFSR curves in figure 4.9 indicate both an improvement of about 5 dB in the worst case point on the SFSR curve and a possible 3.9 MHz bandwidth achieved from this application. In this case the effect of compensation upon the ADC is to linearize it for frequencies near the upper end of the band without degrading its normal acceptable behavior for frequencies near the lower end. The simpler structure of this flash converter probably accounts for the wider range of validity for this application.

An interesting point to note here is that this flash converter is being used with-
out the use of a sample-hold circuit at the input. The favorable results suggest the possibility of eliminating sample-hold circuits from flash converter architectures. The main reason for using sample-holds is to avoid letting signals with high frequency components distort the ADC's response. However, if these distortions are predictable and removable through compensation, then the sample-hold may not be needed. Of course, the difference in hardware between a sample-hold circuit and an elaborate correction scheme presents a tradeoff that would need to be resolved for every application. The sample-hold is attractive because it is small and its presence always benefits the ADC regardless of temperature variations and aging. Compensation is attractive because it can potentially outperform the sample-hold in improving ADC performance.

4.3 Causal or Noncausal Estimators?

This section is included in order to present results that address whether the differentiating filter should be causal or noncausal. As introduced in section 3.3, the question was raised as to whether future samples should have anything to do with
the ADC error of previous samples. The question was left unresolved in that section because it depended on the converter's requirements. If the real issue is to obtain the best possible slope estimate at a given sample-time then noncausal filters are needed to bring to bear as much information concerning the path of the signal as possible. However, if the true information needed is some measure of the ADC's history up to the point when the sample is taken then any estimate that utilizes future samples would be misleading.

The question might be restated as "what is the optimal parameter to use for the second dimension?" In this case optimal means optimal in the sense of maximizing the performance of compensation over frequency. It should be noted that the above questions would not even have been considered had the MOD-1205 results shown in the previous section presented a constant compensation at different frequencies. However, the rolloff in performance as a function of distance from the calibration frequency brought the issue to light. At first the performance limitation was attributed to the nonideal frequency response of the CDE. However, a table was made with the "ideal" estimate derived from differentiating the DFT-estimated sinewave, but performance over frequency was nearly identical. The problem was clearly due to using the derivative as the index into the second dimension.

An important point to consider is that the whole problem can be bypassed by using a table that has more dimensions, with higher order derivatives as indices. In much the same way as the phase plane table allowed for error values at a given ADC state to change as the analog slope changed, this multi-dimensional table would be able to account for changes in the phase plane error values as the frequency changed. However, a multi-dimensional table would require much more memory and would be much more difficult to calibrate. The motivation behind the optimization of the second dimension is to keep the compensation approach as straightforward as possible.

Another point to consider is that the performance of any two estimators near the calibration frequency should be nearly identical. This is because the desired optimal parameter will remain unchanged with respect to the parameter in use until the sinewave parameters change. Since changes due to amplitude variations are accounted for during calibration, the only parameter-change that will draw out any difference is a change in sinewave frequency. When this happens the difference in performance between the two estimators will become apparent, since the estimator which is closer to the ideal will perform better than the one which is a poorer
approximation.

In order to obtain data comparing estimators, the MOD-1205 was re-examined by compensating it in two different ways. The first approach used the "ideal" derivative estimator obtained from differentiating the DFT estimate of the sinewave, while the second approach used the Backward Difference Estimator (BDE) described in 3.3. A test program was then developed to measure the SFSR parameter as a function of frequency with amplitude held constant. The DFT-based estimator was chosen over the CDE because it supplies the most accurate estimate of the derivative.

Testing the two compensation schemes in this manner produced the interesting results shown in figure 4.10. The frequency was varied from 500 kHz to 80 kHz over several different low-pass filters. The amplitude was held at about full scale throughout. The gaps in the curves represent frequencies that could not be tested due to lack of the proper filter needed to purify the tone. As can be seen in the figure, the performance of the BDE is vastly superior to that of the DFT-based derivative. While the DFT-based derivative performance drops to about the level of the uncompensated ADC by 250 kHz, the BDE is still improving the converter by 15 dB. This means that, whatever the optimal parameter is for the MOD-1205, it is estimated more closely with the causal BDE than it is with the noncausal estimates provided by differentiating filters.

It is interesting to speculate on what this optimal parameter might be given the above data. Since the BDE is completely determined by the current state and the previous state, the results could be indicating that a state-space approach is all that is required. In other words, the correction table could just as well be structured with the current ADC state on one axis and the previous state on the other. Higher order effects could then be accounted for through the inclusion of additional past states into multi-dimensional tables. This has some intuitive appeal as well since the only information available concerning the history of the ADC is contained within its previous samples. If this is indeed the most optimal approach then not only is the causal estimate supported, but the name of the compensation method might need to be changed from "phase plane" to something like "state space."

However, an equally plausible alternate interpretation might allow the retention of the original name as well as require the use of noncausal estimators. The alternative enters in with the ambiguity over what the BDE is actually estimating. As the previous paragraph indicates it can be considered a means of measuring the ADC

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Figure 4.10: SFSR versus frequency for MOD-1205 using the “ideal” derivative estimator (above) and the BDE (below).
state history. But, upon closer inspection, it can also be viewed as an estimate of the slope of the analog input midway between two samples. In other words, there may be a delay mechanism in the ADC that places more emphasis on the slope at some time prior to the instant the sample is acquired. The BDE might be giving us an estimate closer to this optimal point than the CDE or any differentiator can provide. However, just because the BDE is a causal estimator does not mean that a more complex midpoint differentiating filter would be causal. In fact it would have to be noncausal to remain anti-symmetric about the midpoint of interest.

Unfortunately, instead of resolving the issues, this section has only succeeded in making them even more complex. The questions presented here can only be settled through additional investigation. Experimenting with the dual converter multi-rate architecture, for example, would be an excellent way of testing the latter hypothesis, since it would easily allow varying the delay between differentiator and sampler. The only point in this section that cannot be argued with is that, at least for the MOD-1205, the BDE provides a better estimate for the second dimension than the CDE.

4.4 Compensating Burr-Brown’s ADC-600

The results shown in this section illustrate the performance of compensation on a converter that is already an excellent device. As might be anticipated, compensating a device which is functioning very well to begin with is not very easy. The Burr-Brown ADC-600 is a 12-bit, 10 MHz subranging converter that rarely exhibits harmonic distortion components in excess of the \( P_Q \) level. Because the spurs are usually so close to the noise floor, a good deal of processing is required to resolve them adequately. This, coupled with the fact that the device is somewhat more temperature sensitive than the MOD-1205 makes the ADC-600 difficult to improve through compensation.

Of course, the problem of temperature sensitivity can be overcome fairly easily by keeping the converter in a temperature-controlled oven. Although a little cumbersome, this solution would be welcomed in many applications if it allowed a significant gain in spur-free range. Another solution would be to make separate tables to be used at different temperatures.

Figure 4.11 shows a compensation table obtained from the ADC-600 using the BDE for the slope estimate. The table has a resolution of 256x128 (the same as
the MOD-1205's) and was made with a .99875 MHz sinewave sampled at 5.12 MHz. The test sinewave was decremented to zero in 512 steps, with a total of 32768 points processed at each step.

Note the rotation of the table in the phase plane due to the nature of the BDE. This rotation is a function of frequency so that, as the sinewave frequency is lowered, the signal cannot quite reach full scale without falling off the table. Averaging several tables at different frequencies should overcome this problem, although it is not very serious anyway.

Note also the randomness of the table. The only prominent feature visible is a ridge extending across the table near half-scale more or less independently of slope. Almost all of the errors are contained within an LSB peak-to-peak variation.

Figure 4.12 shows compensated and uncompensated SFDR curves at .99875 MHz and .80125 MHz. Although significant improvement on the order of 15 dB can be seen for signals near full-scale, the overall improvement in spur-free range is about 3 dB. The problem presented by the ADC-600 is one of not enough table resolution where it is most needed. The signal level where compensation begins to not have much effect is where only 4 or 5 points are being indexed in the correction table. Unlike the MOD-1205, the ADC-600 has most of its problems at this point instead of near full scale. The reason for its low-level problems is probably due to the presence
of the ridge, which tends to get sampled more often when the signal amplitude is small.

Although difficult to attain, 3 dB is still a significant improvement for a converter that already performs very well. Efforts to get more out of the ADC-600 will probably involve increasing the table's resolution at points lying close to the ridge.

4.5 Performance on Typical Signals

This section is included as a means of presenting additional data that the reader may find interesting. After reviewing the above results, one may be thinking that it is fine to be able to remove distortion from sinusoids, but most applications involve signals with energy at more than one frequency. How well will compensation work on real-world applications?

First of all sinusoids were chosen as test signals in the previous examples because they typically stress the ADC the most and hence any gain through compensation is immediately apparent and easy to measure. Second, the effects of compensation on signals that are essentially broadband noise are going to be fairly insignificant and difficult to measure, mainly because most ADCs perform quite well against these signals. However, there is a class of signals between these two extremes that can be fairly stressful to the converter and hence should be correctable.

One almost trivial example of this class is a frequency-modulated (FM) signal. Figure 4.13 shows FFT spectra of an FM signal before and after compensation. The converter employed in this example is the same MOD-1205 used to generate the previous results, with the CDE used for slope estimation. The FM signal sweeps the frequency range of 100 kHz centered at 450 kHz with a modulation frequency of 6 kHz. The data in this example are windowed with a Gaussian window having 90 dB sidelobe suppression to avoid spectral smearing. A total of 4096 points were transformed by the FFT.

Note the decrease in level by about 12 dB of the clump of frequencies located around the second harmonic of the signal. This is an outstanding performance even though the distortion lies outside the band of interest. The signal could just as well have been set up with the "second" harmonics aliasing into the signal band, in which case compensation would still have removed these now significant sources of distortion.

A second illustration of this class of signals is a signal containing information at
Figure 4.12: SFSR test results before and after compensation for ADC-600 at .99875 MHz (above) and .80125 MHz (below).
Figure 4.13: FFT spectra of an FM signal before (above) and after (below) compensation for MOD-1205.
energies less than the harmonic distortion level of the ADC. This test helps illustrate the basic theme of the entire thesis. It was performed on the same TDC-1025 as discussed in 4.2.2. The test signal applied to the converter consists of a full-scale (pure) sinewave at 4 MHz and an FM signal near 8 MHz with a power level almost 20 dB below the converter's quantizing power level.

As can be seen in figure 4.14, the uncompensated response shows ADC distortion components rising above the level of the FM signal by about 2 dB. In this case, a typical communications system would not be able to detect the FM signal because of the distortion. However, in the compensated response the FM signal can easily be detected, since the distortion has been driven into the noise floor. Compensation has linearized the ADC in the face of stressful signals so that very low amplitude signals can now be processed. An interesting point to note is that this performance was achieved with a three-month old correction table.

These two examples indicate the potential of the phase plane method for solving many real problems that require more dynamic range than hardware solutions can provide. These results, coupled with the results of the previous sections, indicate that the phase plane approach is a promising means of improving ADCs for applications involving spectral analysis. The next chapter provides a summary of the results and lists a few directions for further research.
Figure 4.14: FFT spectra of a signal containing energy below the harmonic distortion level of the ADC—uncompensated above, compensated below.
Chapter 5

Conclusions

A good deal of information has been presented in the preceding four chapters. A new approach toward compensating ADCs has been developed, and results have been presented supporting its use in spectral analysis applications requiring wide dynamic range. The purpose of this chapter is to summarize some of the key ideas and results that have been presented using a ‘pros and cons’ format for discussion.

The phase plane compensation method is a two-dimensional correction table in which the analog derivative of the input signal determines in part the magnitude of the error to be removed from each sample. It is an easily implemented approach that has yielded a number of promising results in one such implementation. First, it offers the ability to remove ADC distortion components from a sampled sinewave over a wide frequency and amplitude range. Second, in the MOD-1205 example the Central Difference Estimator allows an improvement (in worst case performance) of 10 dB in spur-free range over an effective compensation bandwidth of about 20% of the calibration frequency. The bandwidth figure can probably be increased by a factor of two by using the Backward Difference Estimator. A means of constructing digital differentiating filters presented in section 3.3 should allow the same results to be obtained anywhere within the Nyquist bandwidth. Third, in the TDC-1025 example the CDE provides an effective compensation bandwidth of possibly 100% of the calibration frequency. Here the results suggest the possibility of improving flash ADCs without using sample-hold circuits. Finally, preliminary results shown in section 4.4 show that compensation can be expected to be equally helpful with removing distortion from real signals that contain information.

As for results that are somewhat disappointing, a number of discoveries have also been made. First, the method has not yet demonstrated the ability to compensate an ADC over the entire Nyquist bandwidth of the device. Although several
architectures have been introduced that can supply the necessary slope estimate over the Nyquist bandwidth, the improvement afforded through compensation has not been shown to be constant over this range. Until this happens manufacturers will not be able to package a phase plane compensator with each device. The approach remains application specific and hence must be implemented by the user. Second, as illustrated by the ADC-600 example, the actual improvement obtained through compensation is not always very impressive and varies from device to device, though it appears to be able to improve any flash or subranging architecture to a certain extent. Finally, one must remember that the phase plane approach is directed only at applications in which signals have energy at a limited number of discrete frequencies. Whether or not it can improve a converter for broadband applications is difficult to determine.

There are a number of issues that have been presented throughout the preceding chapters that deserve further research. Some of these may help to reduce the number of ‘cons’ that are listed above. First, the issue of making tables with varying resolution should be addressed. There is a high probability that this approach will help attack worst-case or problem areas of the phase plane such as extremely low signal levels or abrupt ridges in the table. Second, the search for an optimal estimator for the second dimension should be continued. Although the BDE provides a remarkable improvement over the CDE, it still does not solve all problems occurring when the frequency is changed. The key to this search could lie in varying the delay before sample-time that the derivative is taken. Or it might be solved by considering only past states in the estimate. A third issue lies in the investigation of the performance of the three other architectures described. The implementation of the multi-rate structure would provide a natural way of searching for the optimal delay between derivative and sample. Finally, the actual bounds placed on compensation should be sought out. Thus far it seems as if an unlimited improvement can be obtained for full scale signals at the calibration frequency, provided enough processing is performed. It will be interesting to determine what mechanism finally limits this performance.
References

Chapter 1


Chapter 2


Chapter 3


