Driving Emerging Technologies From Concept to Reality: A Case Study of Carbon Nanotubes

By

Rebecca Ho

B.S., The University of Texas at Austin (2017)
S. M., Massachusetts Institute of Technology (2019)

Submitted to the Department of Electrical Engineering and Computer Science in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2023

Authored by: Rebecca Ho
Department of Electrical Engineering and Computer Science
May 18, 2023

Certified by: Max M. Shulaker
Research Scientist, Research Laboratory of Electronics
Thesis Supervisor

Certified by: Hae-Seung Lee
Professor of Advanced Television and Signal Processing
Thesis Supervisor

Accepted by: Leslie A. Kolodziejski
Professor of Electrical Engineering and Computer Science
Chair, Department Committee on Graduate Students

Driving Emerging Nanotechnologies From Concept to Reality: A Case Study of Carbon Nanotubes

By

Rebecca Ho

Submitted to the Department of Electrical Engineering and Computer Science on May 18, 2023, in partial fulfillment of the requirements for the degree of Doctor of Philosophy of Electrical Engineering and Computer Science

Abstract

The evolution of electronics has transformed nearly every aspect of society and has been fueled by decades of relentless device scaling. However, electronics is facing a paradigm shift as serious obstacles challenge future progress. Continued scaling is growing increasingly difficult and already yields diminishing energy efficiency benefits. At the same time, other obstacles such as data bandwidth bottlenecks, interconnect density limitations, and reliability are limiting computing performance. Therefore, traditional routes to progress are insufficient, and new approaches must be investigated if we are to continue the technological advancement society has come to expect.

One major thrust toward overcoming these obstacles is the search for alternative, beyond-silicon technologies. Yet despite the promise of these emerging nanotechnologies, their nascency has made their integration into practical and useful electronic systems challenging. In my thesis, I aim to tackle this challenge and present a roadmap for how such new and immature nanotechnologies can be leveraged to not only set the foundation for futuristic next-generation hardware, but also realize *practical systems* that can have an impact today. As a case study, I use carbon nanotubes (CNTs) to demonstrate a realistic roadmap for commercially realizing these next-generation technologies. First, I show, for the first time, that every type of today's conventional circuitry (digital, analog, and mixed-signal circuits) can be fabricated with CNT field-effect transistors (CNFETs). This provides a pathway for adopting these futuristic technologies today. Second, to show how CNFETs can play a role in the next generation of computing systems, I leverage the unique low-temperature fabrication of CNFETs alongside emerging memory technologies to achieve the finest 3D integration of emerging technologies to date, which I further use to enable a new circuit design technique. Third, to show how CNFETs can enable futuristic electronic systems that can impact application spaces beyond conventional computing, I leverage VLSI-compatible foundry fabrication of CNFETs to realize BioSensor chips capable of detecting and identifying infectious pathogens in liquid. These experimental demonstrations of CNFETs in today's (conventional circuitry), tomorrow's (dense fine-grained 3D systems), and futuristic (healthcare diagnostics) applications explicitly demonstrate a practical

roadmap for how emerging nanotechnologies can be developed for near-term adoption while providing longer-term motivation for enabling next-generation electronic systems.

Thesis Supervisor: Max M. Shulaker
Title: Research Scientist, Research Laboratory of Electronics

Thesis Supervisor: Hae-Seung Lee
Title: Professor of Advanced Television and Signal Processing

Thesis Reader: Marc Baldo
Title: RLE Director, Dugald C. Jackson Professor in Electrical Engineering

Acknowledgments

Most of this document consists of a culmination of work throughout the past 6 years, a straightforward synopsis of experimental work and scientific findings. However, despite the ability to organize it in hindsight, oftentimes this work did not feel straightforward at all. There were countless hours in the lab, many days when I did not know what I was doing or what direction to go in, and a fear that in the end nothing would work out. But there was a lot of joy and growth in this process as well, and that was because of the countless people who supported me during my time at MIT. This thesis may be the end result of all the work of my PhD, but these people and the memories we shared are the story behind it.

I would first like to acknowledge my advisor, Professor Max Shulaker. It's probably no surprise that the professors at MIT have high expectations for their students, but I'll always appreciate how Max showed us firsthand how to meet them. He welcomed impromptu meetings, delivered crash courses on device physics, thoughtfully helped us build engaging narratives for our work, and even worked directly alongside us in the lab. He thought not only about the research his students were conducting in the present, but also the tools they'd need to be successful in the future. So, to Max – thank you for helping me find direction in all of this, for taking a chance on me, and for teaching me lessons and skills that are critical to the foundation for my life after MIT. You took something as miniscule as a carbon nanotube and made it into a research group, a government research program, and the foundation for multiple careers and friendships.

I would also like to thank my co-advisor, Professor Hae-Seung (Harry) Lee, who taught me almost everything I know about circuit design. I hadn't even seen an op-amp circuit schematic before taking his class, and within months I was able to build one. Beyond circuits, Harry was incredibly supportive and reliable, even during a global pandemic and his numerous leadership positions across MIT. Thank you, Harry, for your patience, kindness, time, and expertise. It's been a true privilege to learn from and work with you.

To my third thesis committee member, Professor Marc Baldo, thank you for your support in helping me prepare my defense and thesis, your insights and expertise were greatly appreciated. To my academic advisor, Professor Elfar Adalsteinsson, thank you for guiding me through the entire PhD process. Your warmth and kindness made me feel immediately welcome upon my arrival at MIT. I would also like to acknowledge Professor Deji Akinwande at The University of Texas at Austin, who first introduced me to the world of microelectronics and nanofabrication and encouraged me to apply to PhD programs. I wouldn't be on the path I am today without the initial opportunity to work in the Akinwande lab at UT.

This work was completed with the support and guidance of many people at Analog Devices, Inc. (ADI), including Dr. Sam Fuller, Susan Feindt, Denis Murphy, and John Siket. It also would not have been possible without the staff of the MIT Microsystems and Technology Lab (MTL) and MIT Nano, including Bob Bicchieri, Dave Terry, Dennis Ward, Donal Jamieson, Kurt Broderick, Eric Lim, Paul Tierney, Vicky Diadiuk, Jorg Scholvin, Whitney Hess, and Dave

Dunham. They trained me on the tools in the lab, answered frantic phone calls and texts, and even came in on the weekends to help meet crucial deadlines. I will miss our conversations during those long days in the fab. I'd also like to thank the numerous admin who have helped and supported me throughout the years, including Joseph Baylon, Jessie-Leigh Thomas, Cathy Bourgeois, Elizabeth Kubicki, and Joanna MacIver. And to my therapist, Maryam Khodadoust – it has been easy when times are hard to question if I made the right choice pursuing grad school, but reflecting on who I was when I started and who I am now (thanks to you), I wouldn't have wanted life to go any other way.

This work was by no means completed alone, and I have the NOVELS group at MIT to thank for sharing their knowledge and building many of the foundational tools and processes used to complete this research. To Professor Gage Hills, Professor Tathagata Srimani, Dr. Mindy Bishop, Dr. Pritpal Kanhaiya, Dr. Christian Lau, Aya Amer, Minghan Chao, and Andrew Yu, it was an incredible experience to work alongside and get to know you all. To Christian and Pritpal, who started with me at MIT, I always felt so lucky to be able to say that I shared an office with two of my closest friends.

I would also like to acknowledge all the friends I've made during my time at MIT, who made Boston feel like a second home. To Maz Abulnaga, Shankara Anand, Alex Barksdale, Jessica Boles, Sarah Cen, Maddie Dery, Adam Fisch, Julie Kim, Tae Kim, Daniel Lerner, Katie Lewis, Aaron Lu, Joseph Maalouf, Vipasha Mittal, Mihika Moult, Hannah Nierle, Milica Notaros, Josh Perozek, and Marlyse Reeves, I have had so much fun with you all, from exploring the northeast, coffee runs to Flour, and trying to get the most out of our Student Life fees. To Kevin Yee and Jason Zhang – I'm so grateful that somehow we went from being placed in the same first-year interest group at UT to all finding ourselves in Boston at the same time, and that we stayed close through it all.

I have also been fortunate to be supported from afar through friends from Texas, including Weston O'Donnell, Kimmy Burns, Crystal Choi, Roger Craycroft, Sreyas Mahadevan, Danielle McGuinness, Ross Neuman, Matt Owens, Hannah Senter, Ashika Sethi, and Stephanie Slapik. It really means a lot when you can live thousands of miles apart and still feel like your friendship is unchanged. Thank you for always welcoming me back home.

To my extended family – Alice Denham, Dough Denham, Briana Denham, Caitlyn Denham, Chi Ho, Carol Wu, and my Granddaddy, William Trenary, I love you all and I look forward to visiting soon.

To my brother, Garrison Ho, I'm so glad that we both ended up in the northeast at the same time. Getting to know and learn from you is one of the best things to come from these past few years. I'll always admire how you pursue your passions, even when it means defying convention. I don't think I would have ever developed the courage to do the same if I hadn't watched you do it first.

Lastly, to my parents Julianne Trenary and Horace Ho, thank you for everything. The brevity of this passage is only because no amount of words (even 90 pages of them!) could capture the gratitude and love I feel for you both. In more ways than you know, this work is for you.

This work was supported by the resources of numerous groups at MIT, including the Microsystems Technology Laboratories (MTL), the Research Laboratory of Electronics (RLE), MIT Nano, the Medical Electronic Device Realization Center (MEDRC), and the Center for Integrated Circuits and Systems (CICS); industry partners, including Analog Devices, Inc. (ADI), Taiwan Semiconductor Manufacturing Company (TSMC), and SkyWater Technology; and government agencies, including the Defense Advanced Research Projects Agency (DARPA), the Air Force Research Laboratory (AFRL), the National Science Foundation (NSF), and the NSF Graduate Research Fellowships Program (GRFP).

Table of Contents

List of Figures

Permission

Part of this thesis has been reproduced with permission from R. Ho *et al.*:

1. Ho, Rebecca, Christian Lau, Gage Hills, and Max Shulaker. 2019. "Carbon Nanotube CMOS Analog Circuitry." *IEEE Transactions on Nanotechnology*, 1–1. https://doi.org/10.1109/TNANO.2019.2902739.
2. Amer, Aya G., Rebecca Ho, Gage Hills, Anantha P. Chandrakasan, and Max M. Shulaker. 2019. "29.8 SHARC: Self-Healing Analog with RRAM and CNFETs." In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, 470–72. IEEE.

Chapter 1: Introduction

1.1 Background

For decades, physical and equivalent scaling of silicon field-effect transistors (FETs) has been governed by Moore's law, which posited the number of components per integrated circuit would double every 1-2 years [Moore 1965]. This scaling has enabled incredible advancements in technology, from the billions of transistors that run our smartphones to the rise of machine learning and fully autonomous vehicles. Greater device density has also yielded improvements in computing energy efficiency, as stated by Dennard Scaling [Dennard 1974]. However, silicon scaling is realizing diminishing returns (Dennard Scaling ended over a decade ago) and is also becoming increasingly difficult [Liebmann 2016; Gielen 2008]. These challenges have motivated the search for alternative beyond-silicon technologies that could continue the growth predicted by Moore and Dennard.

One promising candidate is carbon nanotubes (CNTs), an emerging nanotechnology which exhibits excellent electrostatic control due to their nanometer thin body (~1 nm CNT diameter) and simultaneously high carrier transport [Appenzeller 2008; Franklin 2012; Tulevski 2014; Hills 2015]. These properties have benefits for a range of applications, spanning high performance energy-efficient computing to biological sensing for healthcare application [Shulaker 2017]. It is projected that digital circuits fabricated with CNT field-effect transistors (CNFETs, Fig. 1) would enable a 10× improvement in energy-delay product (EDP: a metric of energy efficiency), versus silicon FETs [Hills 2018]. The low-temperature (<400 °C) fabrication of CNFETs also enables new three-dimensional (3D) system architectures, such as monolithic-3D integration, whereby circuit layers are sequentially fabricated on top of one another all over the same starting substrate.

Additionally, because CNTs have such high surface-area-to-volume ratio, they are incredibly sensitive to their surrounding environment. Although this property necessitates certain encapsulation and packaging techniques for realizing reliable circuits, it also implies that CNFETs can be used as a powerful tool for an entirely different purpose: sensing.

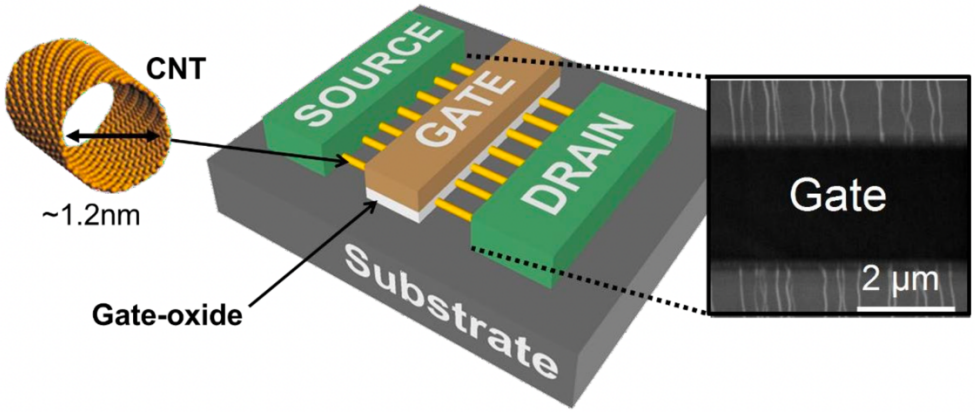

Figure 1.1. Schematic of carbon nanotube field-effect transistor (CNFET) with multiple parallel CNTs (nanocylinders made with atomically thin sheet of carbon atoms with diameter ~ 1 nm) bridging the source to drain contact. Conductance of the CNTs is modulated by the gate to turn the transistor on or off.

Beyond showing promise for a range of applications, CNT technology is rapidly maturing. Recent advancements in CNFET CMOS fabrication have led to the first beyond-silicon modern microprocessor, and this technology has recently been integrated in VLSI-compatible commercial fabrication facilities and foundries [Hills 2019; Bishop 2020]. As large-scale CNFET manufacturing becomes a reality, the question of where and how this technology is most useful grows more pertinent. Just as physical scaling of silicon FETs and new system architectures enabled the higher processing capabilities that fuel machine learning-based systems today, emerging technologies such as CNFETs could be the foundation of revolutionary technologies that are currently only in ideation. The ability to mass produce fully electronic CNFET sensing

platforms could enable more-personalized healthcare by tracking important biomarkers on a regular basis, while 3D system architectures leveraging CNFETs could drastically reduce the time and energy currently consumed capturing and computing on the "data deluge" experienced by many systems. However, before the full potential of CNFET technology can be realized, CNFET research and development must progress to make CNT technology commercially viable.

1.2 Contributions

This thesis leverages recent progress in CNFET fabrication to build a roadmap for these next-generation technologies. Through demonstrations of CNFETs in conventional circuits that can be built today, we show a straightforward on-ramp to the adoption of CNFET technology in current systems, which is a critical step toward realizing applications of CNFETs beyond conventional computing. Then, we show new applications in 3D system architectures and healthcare are a real possibility, demonstrating monolithic 3D chips consisting of CNFETs built directly on top of resistive random-access memory (RRAM), and CNFET BioSensor chips that can successfully detect 3 different pathogenic bacteria. This thesis thus starts with what is possible today, followed by experimental demonstrations of the exciting new applications of CNFET technology that could be realized tomorrow. Specifically, this work shows:

1) **Advancements in State-of-the-Art Circuitry:** All prior demonstrations of circuits built with CNFETs have been limited to digital components. For the first time, we show CNFETs can be used to build both analog and mixed-signal circuits, experimentally demonstrating a CNFET-based differential amplifier, a two-stage operational amplifier (op-amp), a 4-bit digital-to-analog converter (DAC), and a 4-bit successive approximation (SAR) analog-to-

digital converter (ADC). These circuits show CNFETs can be used to build *any* type of system that exists today (spanning digital, analog, and mixed-signal circuits).

Because of both the energy efficiency benefits and sensing capabilities of CNTs, such CNFET circuits promise to impact application spaces such as sensing and low-power IoT applications. Analog and mixed-signal circuits are critical components in sensing platforms, as they comprise sensor-interface circuits which convert and process signals transduced by sensors. Increasing sensor density allows for a diverse set of data to be captured; however, the amount of time and power required to move data between sensing and analog blocks are bottlenecks for data processing. Further energy efficiency benefits can be realized by integrating sensor and sensor-interface circuits on the same chip, thereby minimizing this data movement. Using CNFET-based analog circuitry, we demonstrate a complete front-end analog subsystem which integrates a CNFET-based breath sensor with an analog sensor-interface circuit (transimpedance amplifier followed by a voltage follower). This work thus shows an integrated sensor/sensor-interface circuit built from the same technology all on one chip. Importantly, the energy efficiency benefits of CNTs can now be realized in new application spaces outside of digital circuitry, such as low-power edge applications like remote sensing.

2) **New System Architectures:** For big-data applications, the vast majority of compute energy and time is spent moving data between on-chip compute and off-chip memory (known as the "memory wall") [Wulf 1995; Sze 2020]. Fine-grained integration of logic and memory is key to overcoming this bottleneck [Banerjee 2001], and one promising candidate toward realizing this goal is monolithic 3D integration. As opposed to conventional chip stacking,

which requires physically large through-silicon vias (TSVs) to connect vertical layers[1], monolithic 3D integration uses conventional back-end-of-the-line (BEOL) metal vias to achieve >100× higher interconnect density [Batude 2011; Panth 2013; Bishop 2019]. This massive increase in connectivity enables substantially higher bandwidth (and thus more efficient data movement) between chip layers.

Monolithic 3D integration can be achieved with CNFETs due to their low-temperature fabrication (<400°C), enabling the realization of systems beyond current state-of-the-art architectures. We leverage this property of CNFET fabrication to build extremely fine-grained 3D circuits, which are composed of individual resistive random-access memory (RRAM) cells integrated with individual CNFETs. Owing to this ultra-fine-grained integration, these circuits enable a design "trick" called Self-Healing Analog with RRAM and CNFETs (SHARC), which overcomes challenges presented by metallic CNTs (m-CNTs) in analog and mixed-signal circuits (m-CNTs result in conductive shorts between the CNFET source and drain, resulting in catastrophic circuit failure). The RRAM serve as FET-level "fuses," which can effectively remove m-CNTs or leaky CNFETs from the circuit; this technique was used to realize large-scale mixed-signal and analog circuits. By creating 3D circuits with fine-grained integration at the individual device level, we demonstrate how 3D system architectures can enable exciting new circuit topologies.

3) **Applications Beyond Conventional Computing – Biomedical Sensing:** Healthcare providers often begin treating patients at the point-of-care with empiric therapy: in the absence of precise information regarding their disease, patients are prescribed treatment based on an

[1] TSVs have a typical diameter of 5 μm and inter-TSV pitch of 20 μm [Batude 2011].

"educated guess" by their physician. Often multiple days pass before a complete diagnosis is made and targeted therapy – treatment specific to the patient's disease – can be administered. Leveraging the sensing capabilities of CNFETs and benefits of 200 mm wafer-scale and VLSI-compatible CNFET foundry fabrication, we experimentally demonstrate a real-world application of CNT technology: performing rapid disease diagnostics by detecting and identifying infectious pathogens. This is achieved by combining CNFETs with the mature sensing modality of antibody-based targeted antigen binding, creating BioSensor chips capable of detecting three different infectious pathogens simultaneously through multiplexing across hundreds of functionalized CNFET-antibody biosensors within each chip. As a case study, this technology is compared with the conventional diagnostic process for a urinary tract infection (UTI) to show the potential this work has to improve patient care by decreasing time to targeted treatment at the point of care. On a broader scale, these multiplexed BioSensor chips demonstrate a novel application space beyond conventional computing in which CNT technology can have an important impact.

This thesis shows that CNT technology is not only feasible, but it also has exciting potential at multiple levels of the development stack: from near-term applications implementing existing circuits, to futuristic application spaces such as multiplexed biomedical sensing for healthcare. The integration of CNFETs into everyday devices is a crucial step in realizing the full potential of this emerging technology and moving into the next generation of computing and healthcare. By demonstrating the broad impact emerging nanotechnologies such as CNTs can have, this work shows why continued research in both CNTs and other emerging technologies is critical for continuing the historical trend of technology advancements revolutionizing our daily lives.

Chapter 2:
Advancements in State of the Art –
The First Carbon Nanotube CMOS Analog Circuitry

2.1 Benefits of Carbon Nanotubes for Digital and Analog Circuitry

Carbon nanotubes (CNTs) are an emerging nanotechnology for next-generation electronics [Hills 2018; Shulaker 2013a]. CNTs can be used to form CNT field-effect transistors (CNFETs), which owing to their nanometer thin body (~1 nm CNT diameter) exhibit excellent electrostatic control and simultaneously high carrier transport [Appenzeller 2008; Franklin 2012; Tulevski 2014]. Due to these properties, digital circuits fabricated with CNFETs promise a 10× improvement in energy-delay product (EDP: a metric of energy efficiency), versus silicon FETs [Hills 2018].

Despite these advantages, there remain major challenges towards realizing a future CNFET technology. While a full complementary (CMOS) CNFET technology is required to realize the above energy-efficiency benefits [Weste 2010], all complete digital CNFET systems have been fabricated from PMOS-only CNFETs [Shulaker 2013a; Shulaker 2013b; Shulaker 2014; Shulaker 2017], and all reported CNFET CMOS demonstrations have been limited to only individual devices, small-scale circuits, or digital logic [Lau 2018; Shahrjerdi 2013; Yang 2017; Liyanage 2014; Zhang 2011; Ha 2015]. Importantly, due to the lack of a robust CNFET CMOS process, there has been no reported demonstration of CNFET CMOS analog circuitry (while the vast majority of circuitry in a system today is digital logic, analog circuits are still essential for applications ranging from sense amplifiers for memory arrays to high speed input/output links [Hodges 2004]). Moreover, similar to benefits for digital logic, CNFET CMOS promise analog

circuit performance benefits, providing additional motivation to realize CNFET CMOS for analog circuitry (Fig. 2.1).

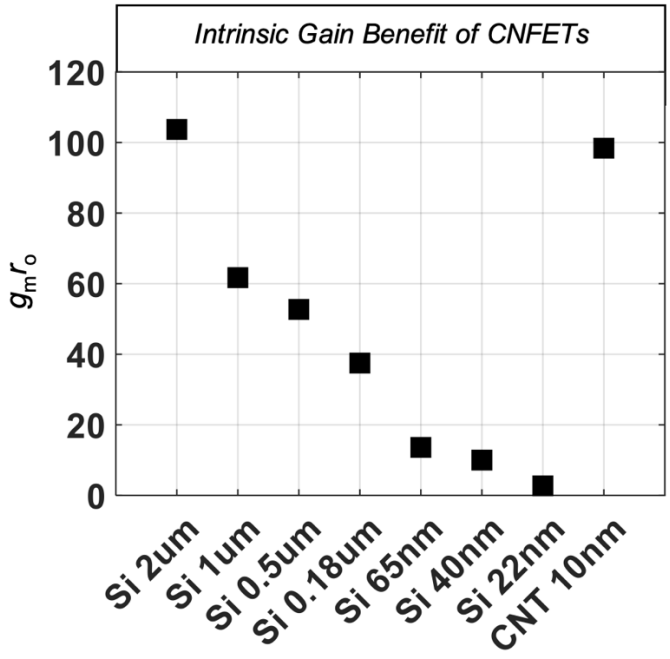

Figure 2.1. Intrinsic gain ($g_m r_o$) [Razavi 2017] benefits of CNFETs. The intrinsic gain is extracted from circuit simulations (Cadence Spectre®) using commercial process design kits (PDKs) for silicon CMOS and using an experimentally calibrated compact model for CNFETs (calibrated using CNFETs with sub-10 nm channel length) [Lee 2015].

2.2 CNFET CMOS Process Flow

Fig. 2.2 shows our CNFET CMOS fabrication flow [Lau 2018]. The CNFETs are fabricated with a back-gate device structure with a metal gate (Pt) and high-*k* gate dielectric (20 nm HfO_2 deposited through atomic layer deposition, ALD). Post gate-stack fabrication, the CNTs are

deposited through a solution-based incubation process [NanoIntegris]. This solution-based CNT deposition enables the entire CNFET fabrication process to be low temperature (<250 °C)[2].

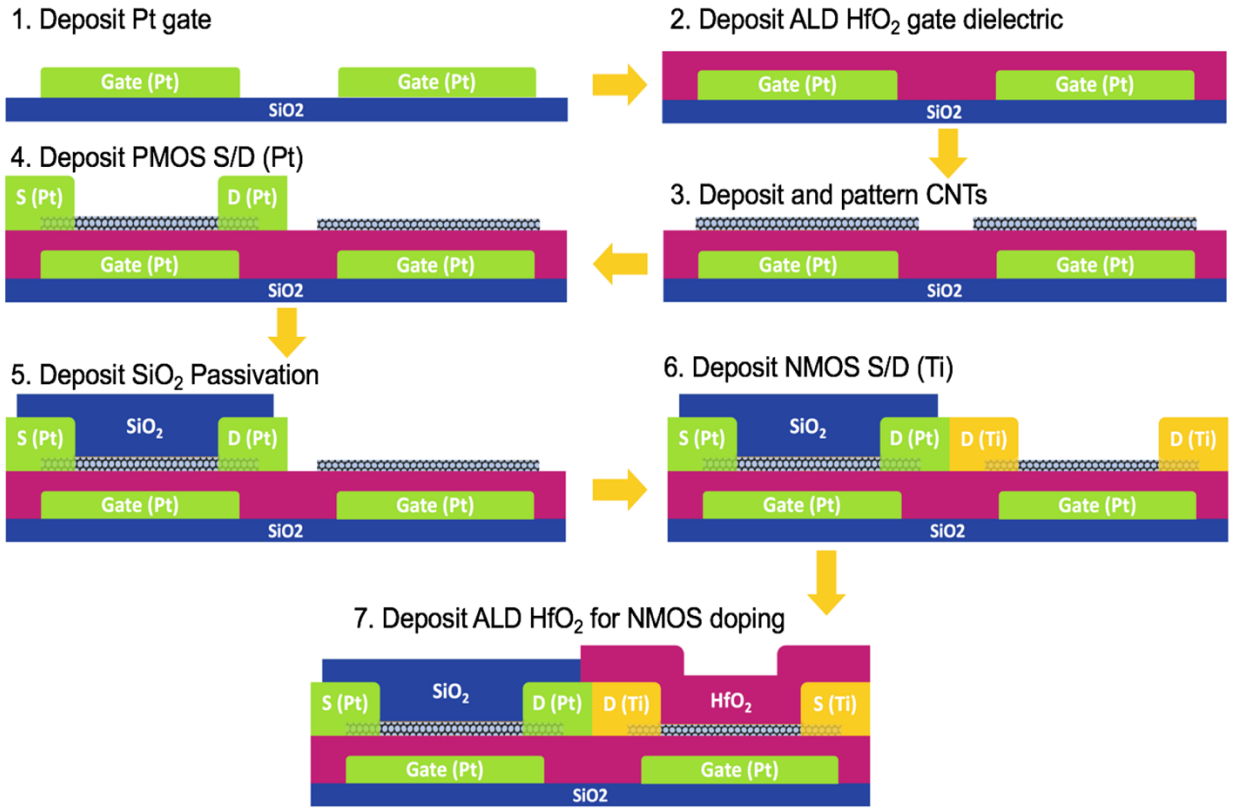

Figure 2.2. CNFET CMOS process flow. A back-gate geometry is used for both the PMOS and NMOS CNFETs. All low-temperature (<250 °C) processing is performed with solid-state and silicon CMOS compatible materials.

To fabricate the PMOS and NMOS CNFETs, we leverage a dual doping strategy which uses both source and drain metal contact work function engineering as well as oxide-based electrostatic doping. The source and drain are lithographically patterned (0.5 nm Ti / 45 nm Pt for PMOS, 75

[2] The high-temperature growth process of CNTs is decoupled from the wafer substrate by using a solution-based incubation process to deposit CNTs. Such low-temperature fabrication enables greater CNFET integration, as the CNFETs can be fabricated in the back-end-of-line (BEOL) directly over silicon CMOS substrates.

nm Ti for NMOS), and the PMOS CNFETs are encapsulated with SiO_X while the NMOS devices are encapsulated with ALD-deposited HfO_X (the stoichiometry of the SiO_X and HfO_X sets the threshold voltage of the PMOS and NMOS, respectively). This CNFET CMOS process leverages only solid-state and silicon CMOS compatible materials, and results in well-matched PMOS and NMOS CNFETs (Fig. 2.3).

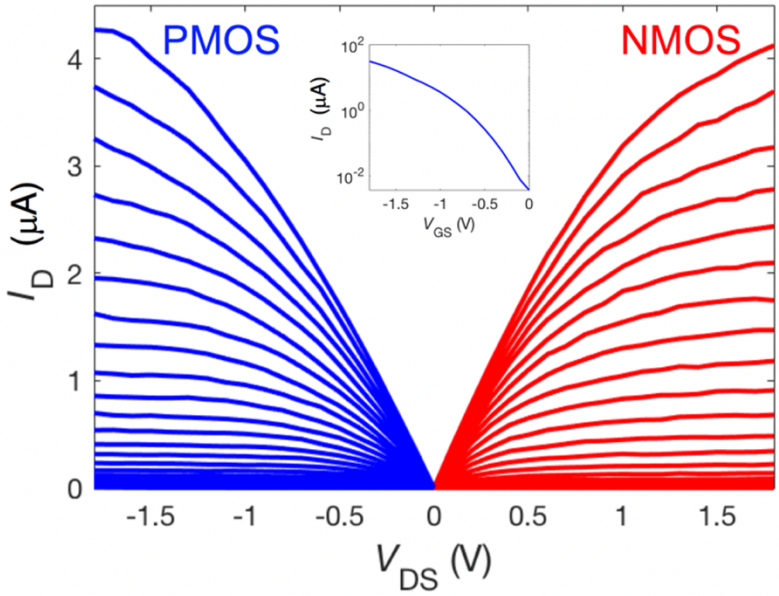

Figure 2.3. Characteristics of PMOS and NMOS CNFETs with a channel length of ~2.5 μm and width of ~4 μm. I_D-V_{DS} curves show well-matched CNFET CMOS (i.e., with similar on-current for both NMOS and PMOS). V_{GS} range from 0 V to V_{DD} (1.8 V) with an increment of 0.1 V (for NMOS, V_{GS} from 0 to -V_{DD} for PMOS). Inset shows an I_D-V_{GS} curve of a PMOS CNFET with I_{ON}/I_{OFF} > 8000.

2.3 Experimental Demonstrations of CNFET CMOS Analog Circuitry

As an initial demonstration of CNFET-based analog circuits, we fabricate a fundamental analog building-block: a two-stage op-amp [Razavi 2017]. Fig. 2.4a displays the circuit schematic

of our two-stage op-amp, while Fig 2.4b shows a scanning electron microscopy (SEM) image of a fabricated CNFET CMOS op-amp. Fig. 2.4c displays a voltage transfer curve for a differential amplifier (the first stage of the op-amp shown in Fig. 2.4a). Measurements of multiple instances of a two-stage op-amp are overlaid in Fig. 2.4d, where the differential input voltage ($\Delta V_{in} = V_{in}^{+} - V_{in}^{-}$) is swept from -1 to 1 V (with a supply voltage of 2 V). The op-amp achieves a maximum gain >700 (Fig. 2.4e). Device mismatch is minimal, with the average offset voltage (V_{OFFSET}, defined as the differential input voltage that achieves maximum gain) being $V_{OFFSET} < 12$ mV.

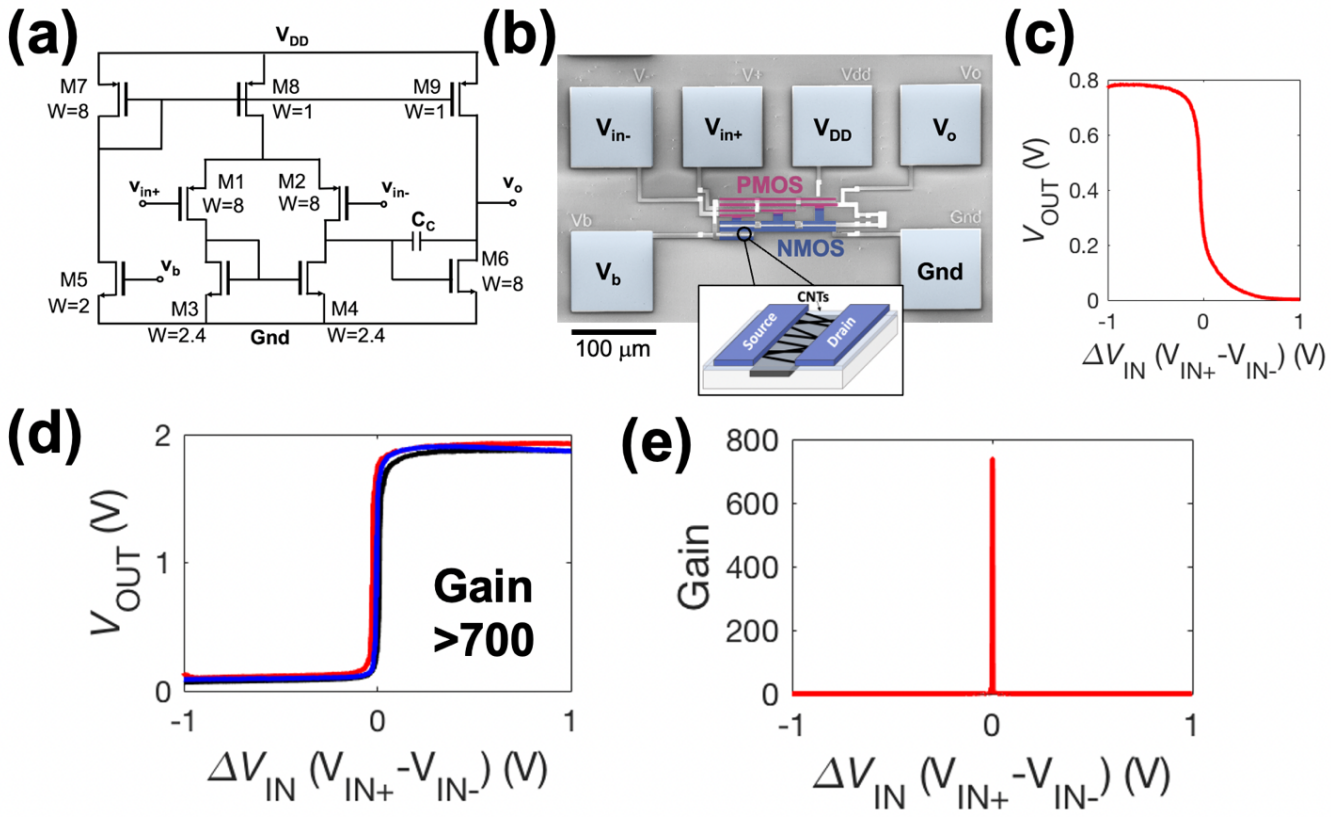

Figure 2.4. Experimental demonstration of a single-ended two-stage op-amp using CNFETs. (a) The topology of the op-amp is a differential amplifier followed by a common-source 2nd stage. (b) SEM of the fabricated op-amp. (c) Measured waveforms of a CNFET-based differential amplifier (first stage of the two-stage topology) and (d) multiple (three) instances of a two-stage op-amp, where the output voltage is a function of ΔV_{in} ($V_{in}^{+} - V_{in}^{-}$). The output swing is >90% of V_{DD} and average $V_{OFFSET} < 12$ mV, indicating well-matched devices. (e) Derivative of the transfer-curve for the two-stage op-amp, showing gain >700.

Leveraging this building block, we demonstrate a CNFET-based analog sub-system: a front-end integrated sensor and sensor interface circuit that converts the resistance change of a chemoresistive CNFET sensor into a buffered output voltage. The sub-system consists of a transimpedance amplifier (TIA) to convert the input current (a function of the chemoresistive CNFET sensor) to a voltage, cascaded to a voltage buffer. To characterize the sub-system, we initially fabricate the circuit shown in Fig. 2.5a. The CNFET chemoresistive gas sensor is replaced with an externally controlled current source (I_{IN}) to remove any variability introduced by the sensor itself. An SEM (false-colored for clarity) of the fabricated circuit is shown in Fig. 2.5b. To characterize the circuit, we sweep a DC current at the input of the system and measure the corresponding voltage output from the voltage buffer. Fig. 2.5c shows the measured output (with a 2 V supply voltage); as expected, the output voltage changes linearly with the input current over the entire input range (10 μA to 50 μA, designed the match the chemoresistive sensor). To quantify the linearity of the response, we calculate the coefficient of determination, R^2, for the measured response to a best-fit linear line [Rao 2001]. The average R^2 across the entire input range is 0.999, illustrating high linearity (*e.g.*, the measured response closely follows a linear relationship to input current). Moreover, Fig. 2.5d shows 100 repeated measured waveforms overlaid on top of one-another, illustrating robust operation with minimal drift.

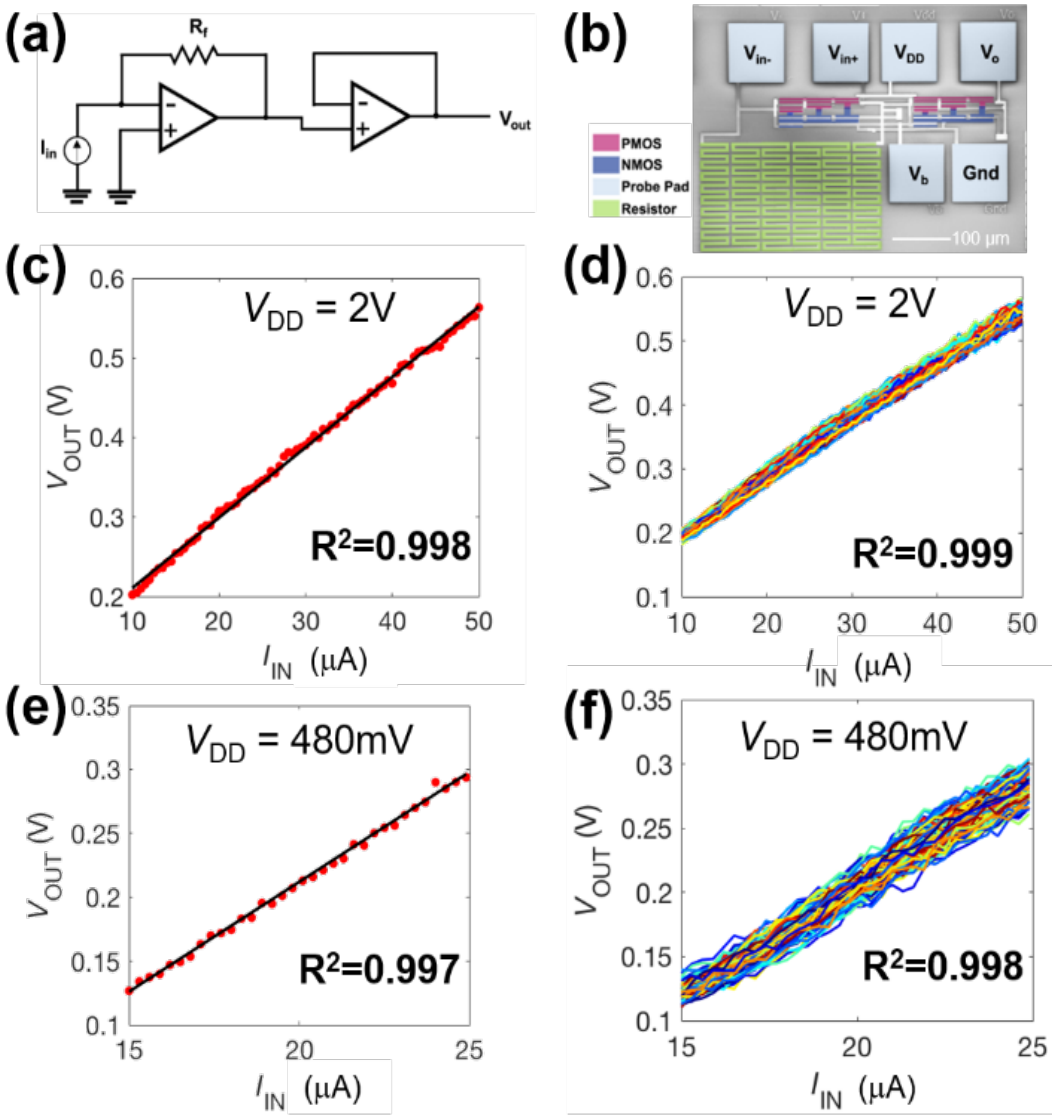

Figure 2.5. Characterization of analog sub-system, with the CNFET sensor replaced with an external current source. (a-b) Schematic and SEM. (c) Measured linear response of the sub-system, converting input current to output voltage. (d) 100 repeated measurement cycles, illustrating minimum drift. (e-f) Repeated measurements of (c-d), with supply voltage reduced from 2 V to 480 mV. Functionality and linearity are not sacrificed even at scaled <500 mV supply voltages.

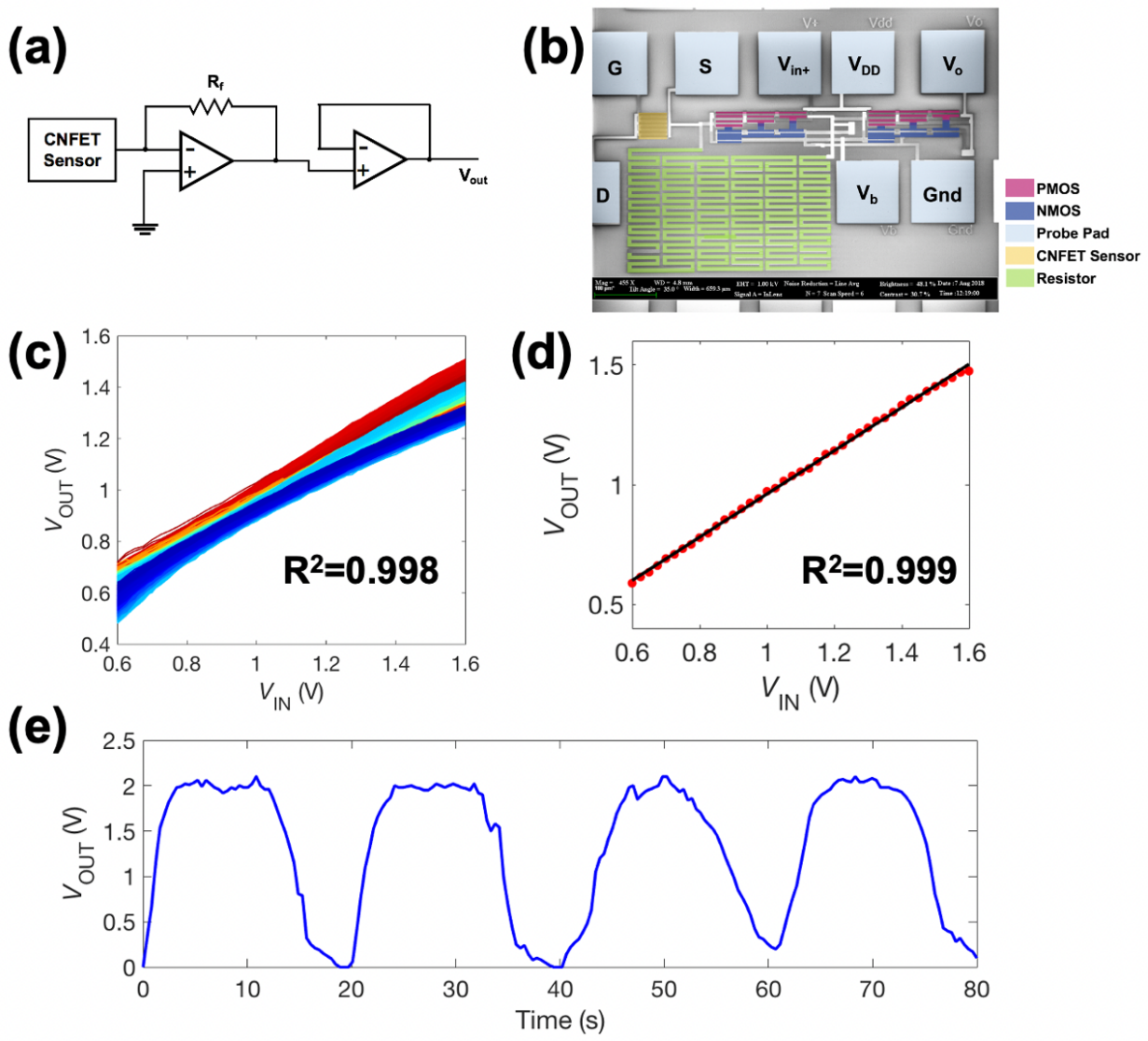

Figure 2.6. Characterization of analog sub-system, with an on-chip integrated CNFET chemoresistive breath sensor. (a-b) schematic and SEM. (c) Measured linear response of the sub-system, measured by keeping the sensor in N_2 ambient air and sweeping the input voltage, V_{IN+}, applied across the sensor. The response is highly linear with a R^2 value of 0.999. (d) 10,000 repeated measurement cycles, illustrating minimum drift. The first 2500 cycles are red, the next 2500 cycles are yellow, the next 2500 cycles and light blue, and the last 2500 cycles are dark blue. The spread in the measured outputs is not random noise, but rather minor slow drift of the circuit after constant measuring for 12 hours. Future work can improve upon stability by optimizing the gate stack to minimize interface traps at the CNT-gate dielectric interface. (e) Measured response of the sub-system in response to alternative exposures to warm breath and N_2. The oscillating response in the circuit illustrates correct functionality of the integrated sensor/ sensor interface circuit.

Fig. 2.6 shows the complete integrated sensor and sensor interface sub-system. As shown in the schematic in Fig. 2.6a, an on-chip integrated CNFET chemoresistive gas sensor replaces the external DC current supply at the input of the TIA. The CNFET chemoresistive gas sensor is fabricated using the same process flow shown in Fig. 2.2[3], but all of the oxide covering the CNFET chemoresistive gas sensor is removed with a dilute HF wet etch[4]. Thus, the CNFET chemoresistive gas sensor is exposed to the environment, while all other CNFETs (e.g., the CNFETs comprising the amplifiers) are encapsulated with a dielectric and are thus protected from the ambient. An SEM of the fabricated sub-system is shown in Fig. 2.6b. To characterize the response of the sub-system, the sensor is kept in a controlled constant ambient (*e.g.*, dry air), and the input voltage (V_{IN}, Fig. 2.6c-d) applied across the sensor is swept. Similar to the sub-system in Fig. 2.5 with a constant current source as the input, the measured output voltage (V_{OUT}) of the sub-system exhibits high linearity (R^2 value of 0.999 to a best-fit linear line). Moreover, Fig. 2.6d shows the circuit is robust and air-stable: 10,000 repeated DC measurements performed over 12 hours illustrate minimal drift.

To test the full integrated sensor and sensor interface circuity, we alternate between one-minute intervals of breathing and blowing N_2 gas directly over the sensor. The CNFET gas sensor reversibly responds to warm breath, resulting in the front-end sub-system voltage output toggling between ~0 V and ~2 V, illustrating correct functionality of the circuit with successful detection and response to breath.

[3] The CNFET chemoresistive gas sensor is also functionalized with a polymer to increase its sensitivity to ambient conditions. There is rich literature describing the design and fabrication of CNFET gas sensors [Liu 2015; Kong 2000; T. Zhang 2006].

[4] The dilute HF wet etch has a high etch selectivity of SiO_X over HfO_X and does not etch or degrade the CNTs.

2.4 Conclusion

We present the first demonstration of CNFET CMOS analog circuits by fabricating foundational building block op-amps up to an analog-based sensor interface circuit. As an experimental demonstration, we integrate the sensor interface circuit with an on-chip chemoresistive CNFET gas sensor, illustrating response and detection of breath. The CNFET CMOS analog circuits achieve high gain (>700) and linearity and operate at scaled sub-500 mV supply voltages (without sacrificing linearity). Through these demonstrations, we show how the energy efficiency benefits of CNFETs can be used in application spaces outside of digital circuits, such as low-power IoT and sensing applications. Thus, this experimental work is a key step towards demonstrating analog functionality that is essential for a future CNFET CMOS technology.

Chapter 3:
New System Architectures Through Monolithic 3D Integration – SHARC

3.1 Overcoming Challenges to Computing

Advancements in device scaling and computing have revolutionized technology; electronic systems such as computers have gone from filling entire rooms to fitting in the palm of our hands. To most, the advancement of technology has felt like a natural occurrence. Whether it be integrating another processor onto our smartphones or allowing an online chatbot to write our essays, the rapid progression of technological systems over the past few decades has made these advancements feel inevitable. However, the relentless demand for faster, smarter computing is currently being met by three major challenges which must be overcome to continue the progress we have come to expect: the first, known as the compute wall, refers to the speed and energy limitations of the logic performing computations [Villa 2014]; the second, the memory wall, is caused by the limited size of on-chip and memory and bottleneck between off-chip memory and on-chip compute due to limited data bandwidth [Wulf 1995]; and the third, the connectivity wall, refers broadly to limited physical connectivity, ranging from connections between components, memory arrays, dies, etc. [Shulaker 2017].

A long sought-after approach toward overcoming these challenges has been to build 3D systems, which would allow us to continue achieving gains in circuit density and thereby computation. Due to the high processing temperatures (>1000 °C) required in doping and annealing steps of conventional silicon FETs, building any additional device layers in silicon would damage the devices beneath them. To achieve 3D architectures with conventional silicon,

device layers must instead be fabricated separately and then integrated together through wafer or die bonding; this process is commonly known as chip stacking. This method is inherently limited in precision, which necessitates through-silicon via (TSV) interconnects of relatively large size and pitch (their diameter is on the order of microns, while that of silicon FETs is in nanometers) [Batude 2011; Panth 2013].

One promising alternative towards overcoming these challenges is monolithic 3D integration. By leveraging the low-temperature (<400 °C) processing of emerging technologies, monolithic 3D integration allows device layers to be sequentially built directly on top of one another all on the same substrate. Inter-layer vias (ILVs) can be the same size as metal layer vias (which at aggressive technology nodes have a pitch of <100 nm), enabling fine-grained and ultra-dense connectivity that is orders of magnitude (>100×) greater than that of chip stacking [Bishop 2019].

Owing to their low-temperature fabrication, CNFETs are a natural candidate for monolithic 3D integration. By building 3D systems with CNFETs, which could still use advanced silicon technology as the first layer, 3D systems beyond the current state-of-the-art architectures could be realized. This could enable systems that overcome the current "walls" with which computing is currently faced, such as through finely connecting sensing blocks, memory, and compute [Shulaker 2017] or the proposed silicon-digital and CNFET-analog architecture proposed in Chapter 4, and vastly expands the realm of possibility for new circuit topologies that leverage emerging nanotechnologies.

Here, we demonstrate a design trick enabled by the fine-grained connectivity of monolithic 3D integration called Self-Healing Analog with RRAM and CNFETs (SHARC). These circuits leverage RRAM and CNFETs to overcome challenges presented by metallic CNTs (m-CNTs), which cause conductive shorts between CNFET source and drain, resulting in catastrophic circuit

failure. Through SHARC, we realize the first large-scale mixed signal and analog circuits built with CNFETs and demonstrate the finest-grained connectivity achieved with monolithic 3D integration.

3.2 Demonstration of Monolithic 3D Integration: SHARC

While CNFETs promise performance benefits for analog circuitry, CNTs suffer from a major inherent imperfection: every ensemble of CNTs contains some metallic-CNTs (m-CNTs), which cause an electrical short between the CNFET source and drain. This results in substantial leakage current and degradation in circuit performance (or even catastrophic circuit failure). Although techniques have been developed to further purify CNT solutions and enable the demonstration of digital CNFET circuits (digital circuits can still maintain correct functional operation even in the presence of a limited number of m-CNTs) [Zhang 2009; Hills 2019], m-CNTs present a major obstacle to realizing large-scale analog and mixed-signal circuits. The effects of a single m-CNT on the performance of an 8-bit digital-to-analog converter (DAC) designed with a folded-cascode op-amp are displayed in Fig. 3.1 for different locations of the m-CNT within the circuit, illustrating that even a *single* m-CNT can cause catastrophic circuit failure for analog circuits (*e.g.*, the output of the DAC latches to either V_{DD} of ground due to a single m-CNT placed within a single CNFET in the circuit).

SHARC is a new circuit design technique that overcomes the presence of m-CNTs in analog circuits. By combining the programmability of non-volatile resistive-RAM (RRAM) with the ability to fabricate monolithic 3D circuits with CNFETs, a circuit can "self-heal" in the presence of m-CNTs. This work was performed in collaboration with Aya Amer, who performed the simulations and layout of this project.

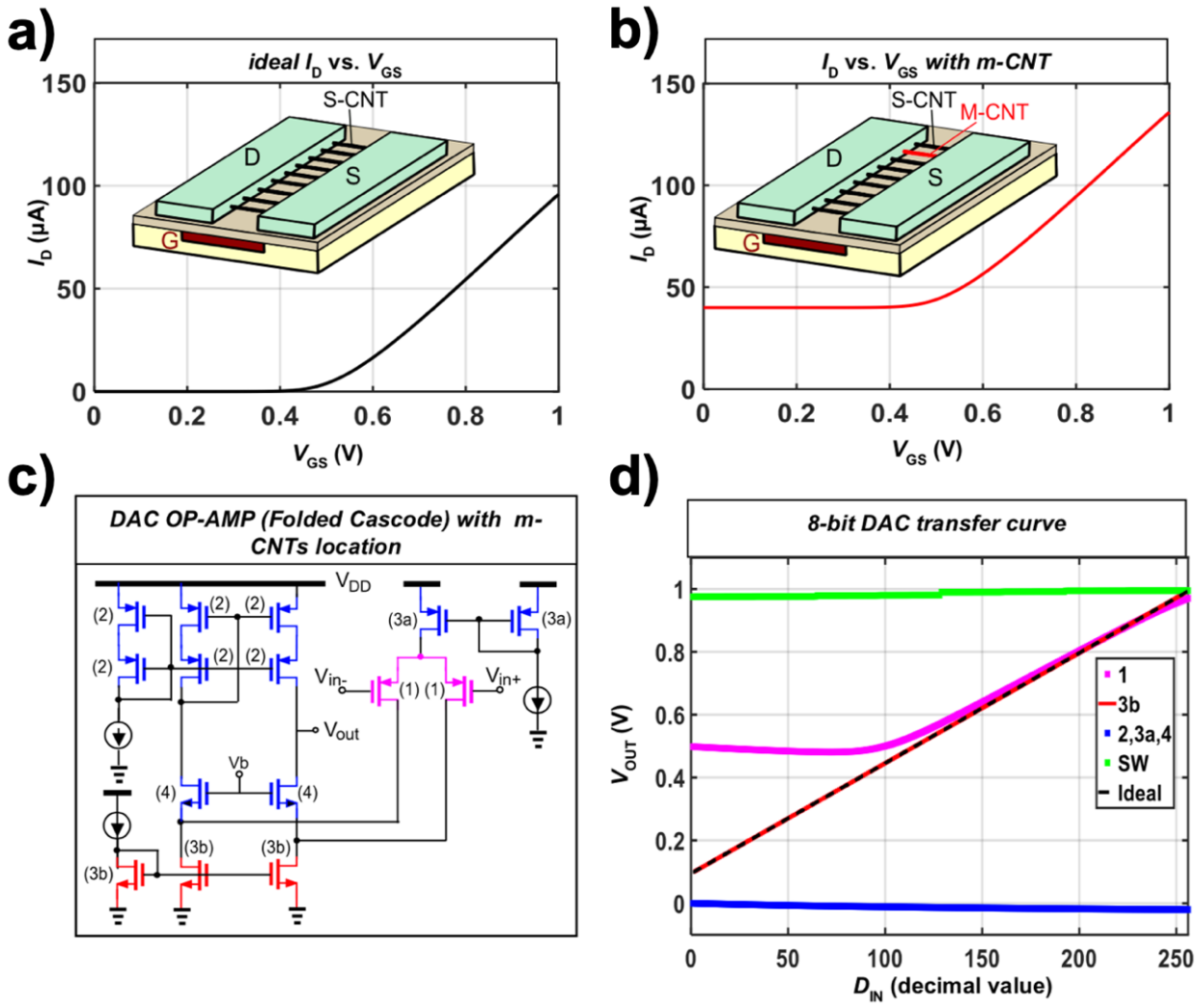

Figure 3.1. CNFET schematics and I_D-V_{GS} curves for (a) a CNFET with all semiconducting-CNTs (s-CNTs) and (b) a CNFET with a single m-CNT. Leakage current (defined as the current through the transistor when it is off) is higher in the presence of an m-CNT. (c) Schematic of an 8-bit DAC designed with an op-amp. Transistors in the DAC are color-coded to match (d) graph of the output voltage of the DAC with different placements of a single m-CNT in the CNFET channel. The compact model used for circuit simulations is calibrated to experimental data for the 10 nm technology node (m-CNT off-state resistance is 25 KΩ).

3.3 Principles of SHARC

A key component of SHARC is RRAM, an emerging type of non-volatile memory that is low-cost and backend-of-the-line (BEOL)-compatible. Its low-temperature fabrication and simple structure, consisting of a thin metal oxide layer between two metal electrodes, enables straightforward integration of RRAM cells into both conventional CMOS fabrication and 3D circuit architectures. Each RRAM cell can exist in one of two states: a low-resistance state (LRS) or high-resistance state (HRS). After fabrication, RRAM exists in a HRS and must be initialized through a "forming" process, where a (generally high) voltage is applied across the electrodes to set it to a LRS. The process by which RRAM first enters a LRS is interpreted to be a dielectric soft breakdown. Specifically, it is believed the high electric field breaks oxygen atoms from the lattice and causes them to drift toward the anode, while simultaneously generating defects in the bulk oxide. The oxygen vacancies create conductive filaments in the bulk oxide through which current can more easily flow [Janousch 2007]. Once formed, the RRAM can then be programmed by "set" and "reset" steps. The "reset" process is performed by flowing current through the RRAM cell; oxygen migration causes the oxygen vacancies that form the conductive filament to fill, bringing the RRAM back to a HRS. The RRAM can be "set" back to a LRS by again applying a voltage across the electrodes to reform the conductive filament. Because of defects generated during the "form" process, the voltage required for setting the RRAM is usually lower than that for forming [Wong 2012]. Fig. 3.2 displays a fabricated RRAM cell and the current through an RRAM cell during the "form," "set," and "reset" processes.

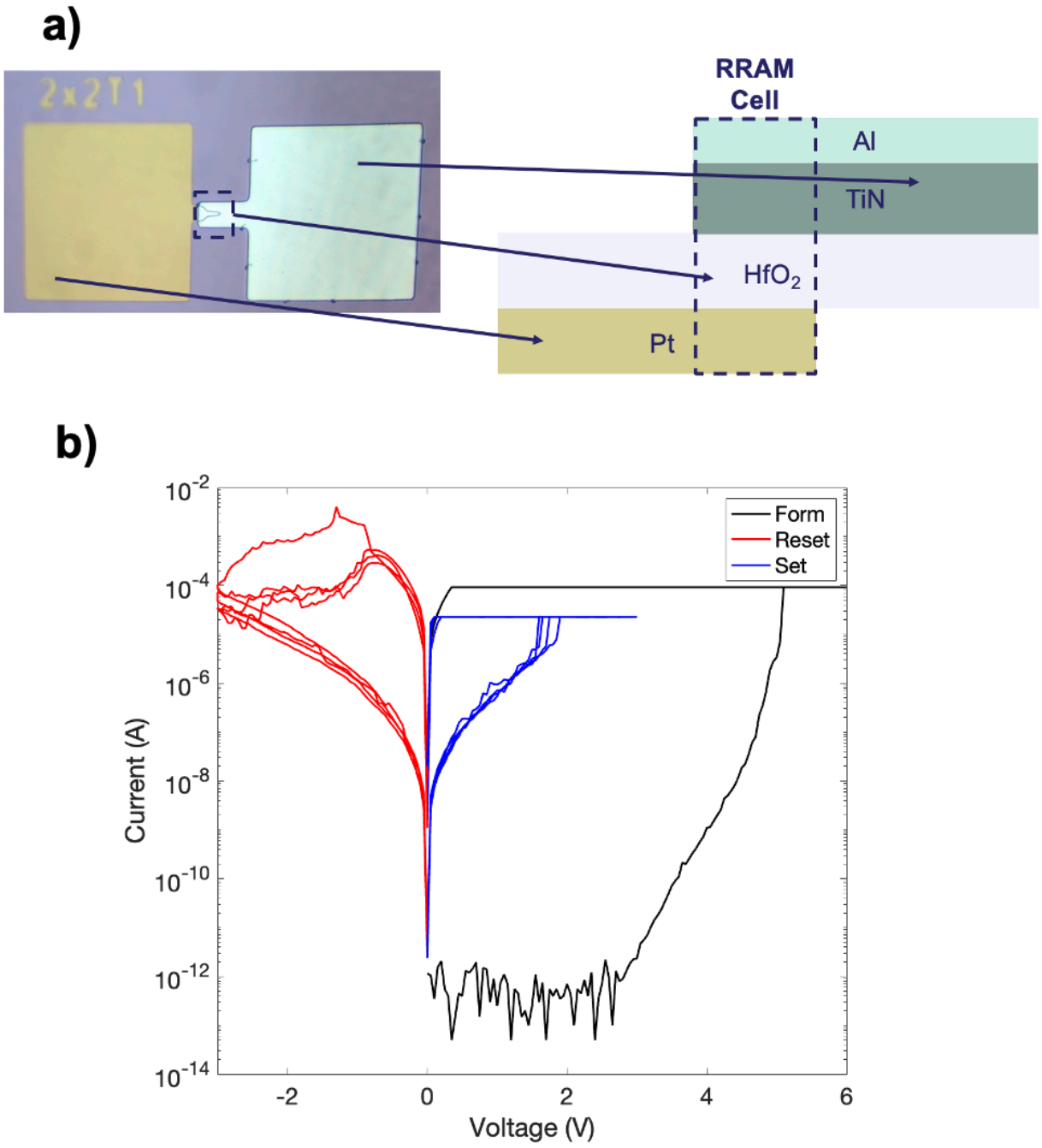

Figure 3.2. Resistive random-access memory (RRAM). (a) RRAM cell fabricated at MIT and its corresponding layers. The two metal electrodes were fabricated with Pt and TiN/Al. HfO_2 was used for the metal oxide. (b) Current through an RRAM cell for the "form," "set" and "reset" processes. 6V is applied across the RRAM electrodes to "form" the RRAM, which for this device occurs around 5V. Current is applied to "reset" the RRAM to a HRS. Around 4 mA was required for the reset. A voltage is applied again to "set" the RRAM back to a LRS. This voltage (around 1.8V) is notably lower than the voltage required to form the RRAM. The "set" and "reset" steps were repeated 9 times for this RRAM cell.

The process of SHARC is displayed in Fig. 3.3. First, CNFETs are fabricated, with each CNFET in the circuit topology split into multiple minimum-width FETs (which we refer to as "sub-CNFETs"). An RRAM cell is fabricated directly over (or under) the source or drain contact of each CNFET so that each CNFET is in series with an RRAM cell. Critically, the RRAM fabrication directly over or under the sub-CNFET contact minimizes the area penalty of SHARC and is directly enabled by the low-temperature fabrication of the CNFETs and RRAM (*e.g.*, the high-temperature >1000 °C fabrication of silicon FETs would damage or destroy any devices previously fabricated underneath the silicon FET on a wafer). Both RRAM and CNFETs require <400 °C processing, and thus naturally enable such heterogeneous monolithic 3D integration.

After fabricating the RRAM and CNFETs, the RRAM cells are then "formed" by applying a positive voltage across the RRAM electrodes, which sets the RRAM into a LRS. The RRAM stack is designed so that its form voltage is higher than the operating voltage of the circuit, preventing any unwanted programming of the RRAM during circuit operation. Next, a voltage is applied across the source and drain of each CNFET, with the gates of the CNFETs biased so that each transistor is in its off-state (*e.g.*, $|V_{GS}| < |V_{TH}|$). Thus, if a CNFET contains only semiconducting CNTs (s-CNTs), it will not conduct current. However, if a CNFET contains an m-CNT, the m-CNT is ungated and thus still conducts current. With sufficient biasing and current, the RRAM in series with CNFETs containing m-CNTs are reset to their HRS. This effectively "self-heals" the circuit, by automatically programming the RRAM in series with CNFETs containing m-CNTs in a high-resistance, effectively removing that CNFET from the circuit. To ensure proper resetting of the RRAM, the reset current of the RRAM should be designed to be less than the off-state leakage current through an m-CNT (<100 μA for a scaled technology node). The last step in the SHARC process is to fabricate the final metal layers of the circuit. The final result is a CNFET circuit where

sub-CNFETs containing only s-CNTs are in series with RRAM in a LRS, while sub-CNFETs containing any m-CNTs are in series with RRAM in a HRS. Post self-healing, CNFETs containing m-CNTs experimentally exhibit $I_{ON}/I_{OFF} > 1000$ and I_{OFF} reduces >800×.

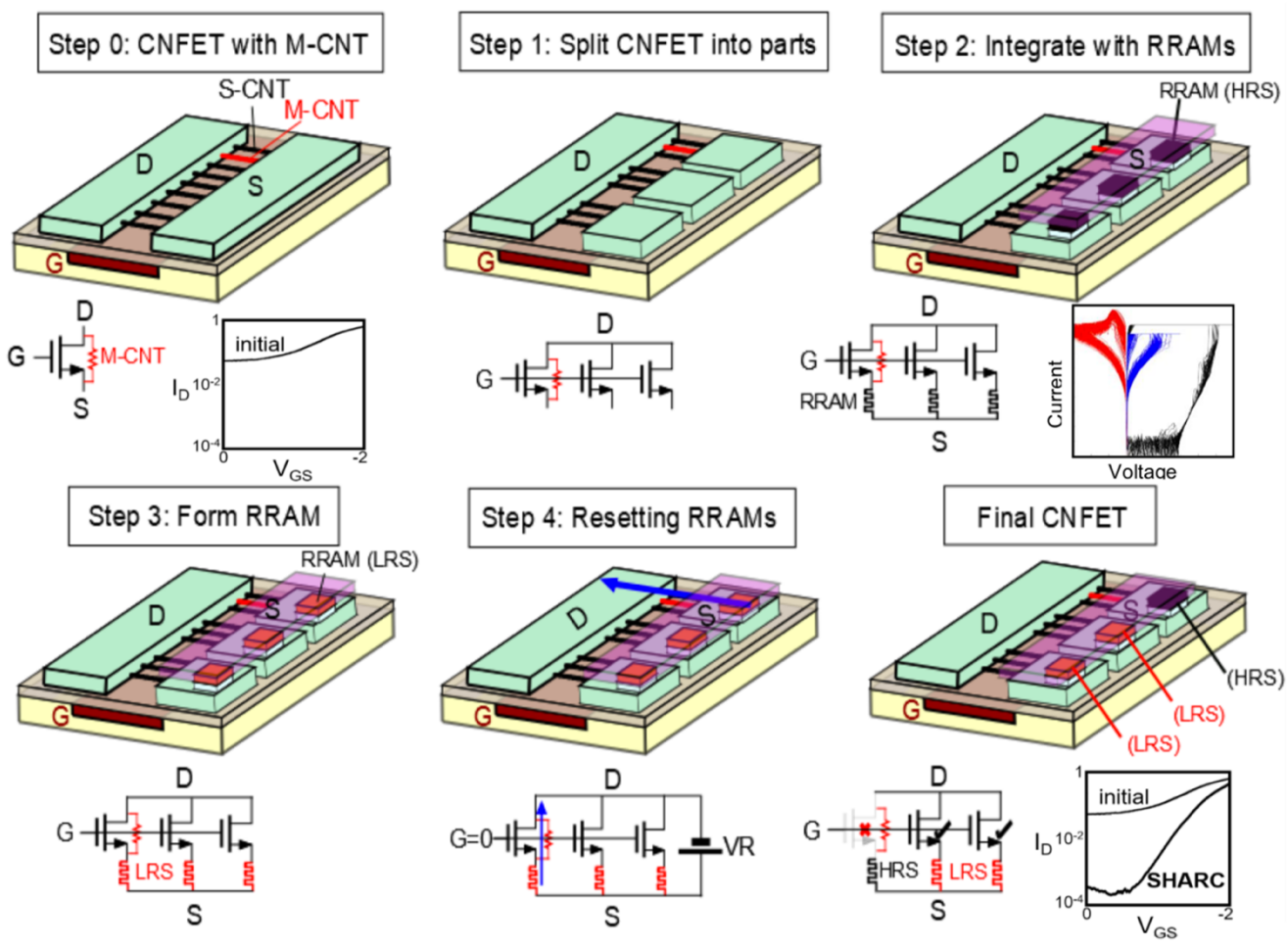

Figure 3.3. Principles of SHARC. The initial and final I_D-V_{GS} curves when using SHARC are shown in step 0 and the final step. I_{ON}/I_{OFF} of all sub-CNFETs combined is improved from ~10 before SHARC to >1000 in the final step. Steps 1 through 4 illustrate how the RRAM is first formed to a low-resistance state (LRS) and then reset to a high-resistance state (HRS) in the presence of an m-CNT. In the final step, an RRAM in a high-resistance state is shown in series with a sub-CNFET containing an m-CNT.

CNFET + RRAM cells are fabricated in a special layout structure with inter-digitated electrodes and minimal metal pitch to maintain transistor matching in analog circuit blocks. Shown in Fig. 3.4, transistors are laid out in such a way to increase the probability that m-CNTs are shared by matched pairs. However, future work should include optimizing this method for guaranteed transistor matching.

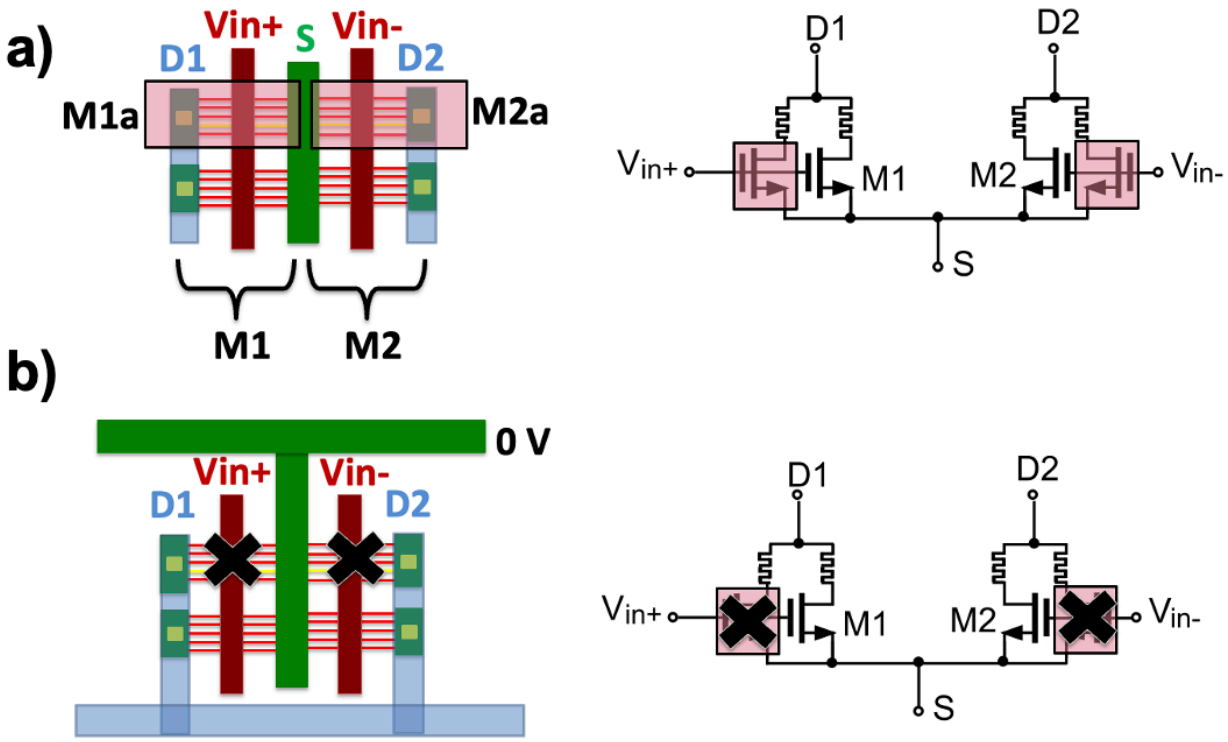

Figure 3.4. Layout strategy of SHARC to maintain transistor matching (a) before and (b) after self-healing.

SHARC is a broad technique that can be applied to a wide range of analog circuit blocks and scales to larger-scale circuits, since SHARC only has to be performed once for all CNFETs in parallel. Additional parameters in the circuit design of SHARC, such as the minimum ratio between RRAM high- and low-resistance states (in order to prevent drawing excessive current

from the power supply) or RRAM cell placement (*e.g.*, on the drain of input CNFETs instead of the source), must also be taken into consideration, and are analyzed in detail in [Amer 2019].

The key benefits of SHARC are: (1) since the m-CNTs provide the current path for resetting the RRAM during the self-healing process (*e.g.*, RRAM programming), the self-healing process occurs automatically (2) RRAM is non-volatile, allowing the circuit to retains its healed configuration (though due to their programmability, the RRAM can potentially be reprogrammed repeatedly in the future), and (3) because of the low-temperature fabrication of both CNFETs and RRAM (<300 °C), they can be fabricated directly vertically overlapping one-another in a monolithic 3D fashion, minimizing area penalty associated with SHARC and achieving ultra-fine-grained connectivity.

3.4 SHARC Process Flow

The fabrication process flow for SHARC is displayed in Fig. 3.5. First, the bottom electrodes of the RRAM are lithographically patterned and deposited (3 nm Ti/ 30 nm Pt), followed by deposition of the RRAM oxide (5 nm HfO_2). Prior to the deposition of the RRAM top electrodes, a 2-minute oxygen plasma descum is performed to remove any residue on the circuit's surface and prevent delamination of later metal layers. A back-gate geometry is used for the CNFETs, allowing the top RRAM electrodes and gates of the CNFETs (25 nm TiN/ 25 nm Pt) to be deposited simultaneously (this is not a requirement, but highlights how process complexity can be reduced through careful processing-circuit co-optimization). The RRAM are then formed to their low-resistance state. The CNFETs are fabricated up to the source/drain layer by the same process described in Section 2.2, with slight modifications to the source/drain metal layer (1 nm Ti/ 70 nm Pt for PMOS, 72 nm Ti/ 3 nm Pt for NMOS). A sacrificial metal layer (0.5 nm Ti/ 15 nm Al) is

deposited to perform the circuit self-healing step. The sacrificial metal layer is removed, and the CNFETs are passivated and doped as described in Section 2.2. In the final step of the process, the final metal routing layer is lithographically defined and deposited.

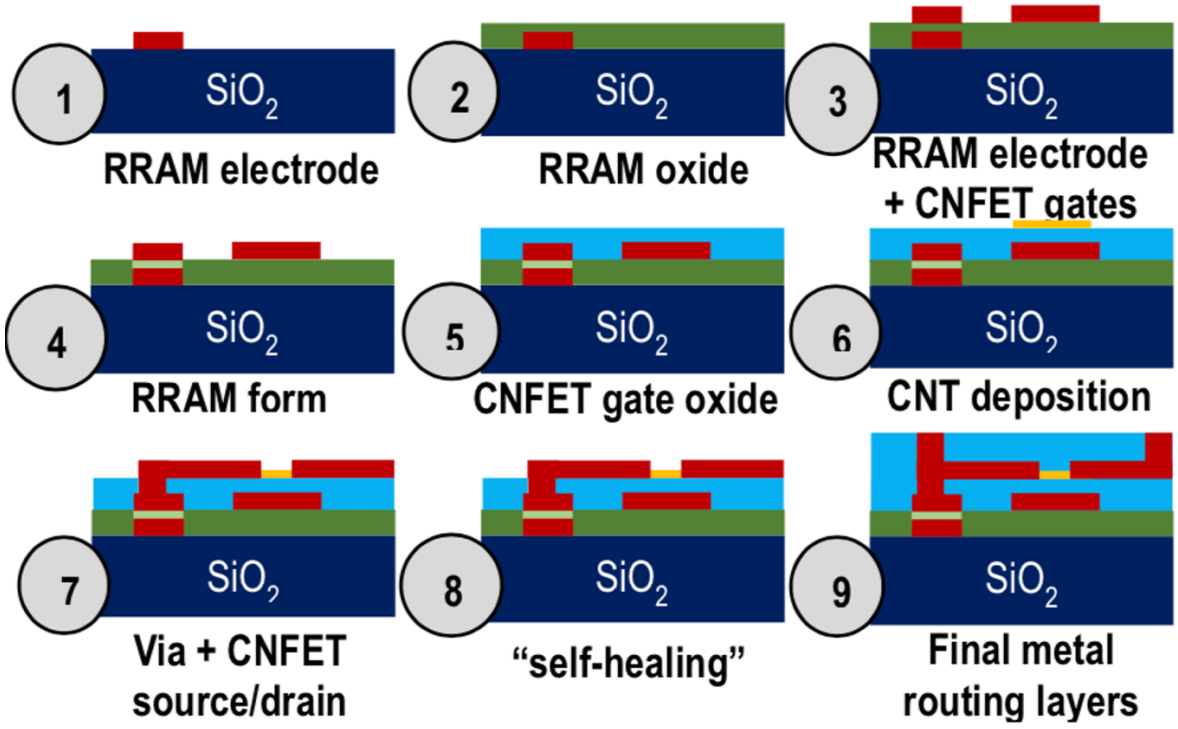

Figure 3.5. Fabrication process flow of SHARC.

3.5 Experimental Demonstration of SHARC

As an experimental demonstration of SHARC with analog and mixed-signal circuits, we use SHARC to fabricate a two-stage op-amp, 4-bit digital-to-analog converter (DAC, SHARC implemented in the two-stage op-amp and switches), and a 4-bit successive approximation register analog-to-digital converter (SAR ADC, SHARC implemented in the strong-arm latch and switches). All demonstrations are implemented at a relaxed 2 µm technology node due to the limitations of an academic fabrication facility (importantly, SHARC, the CNFET CMOS

process, and all other aspects of this work can be scaled to arbitrary technology nodes). As an example of the impact of SHARC, Fig. 3.6 shows the effects of an m-CNT on a two-stage op-amp. Without SHARC, a single m-CNT within the circuit can reduce gain by >100 dB (making the amplifier an attenuator). However, with SHARC, the worst-case gain reduction is <3 dB. To illustrate a functional circuit implementing SHARC (e.g., that the circuit still functions with the full monolithic 3D process flow integrating RRAM and CNFETs), we fabricate this two-stage op-amp using SHARC. The results are shown in Figure 3.6; gain is >800 and matches simulations performed with experimentally calibrated CNFET and RRAM compact models. Fig. 3.7 displays the schematic and die image of a 4b DAC. The measured transfer characteristics show monotonic behavior with non-linearity and gain error (due to large parasitic caps and routing resistance). Fig. 3.8 shows the SAR ADC schematic, its die image and its transfer characteristics.

These circuits are the first demonstration of mixed-signal and complex analog CNFET circuits, and the largest and most complex reported CNFET CMOS circuits to-date (see Table 3.1 for comparison to previous works [Yang 2017; Geier 2015; Han 2017; Tang 2018; Zhang 2018]).

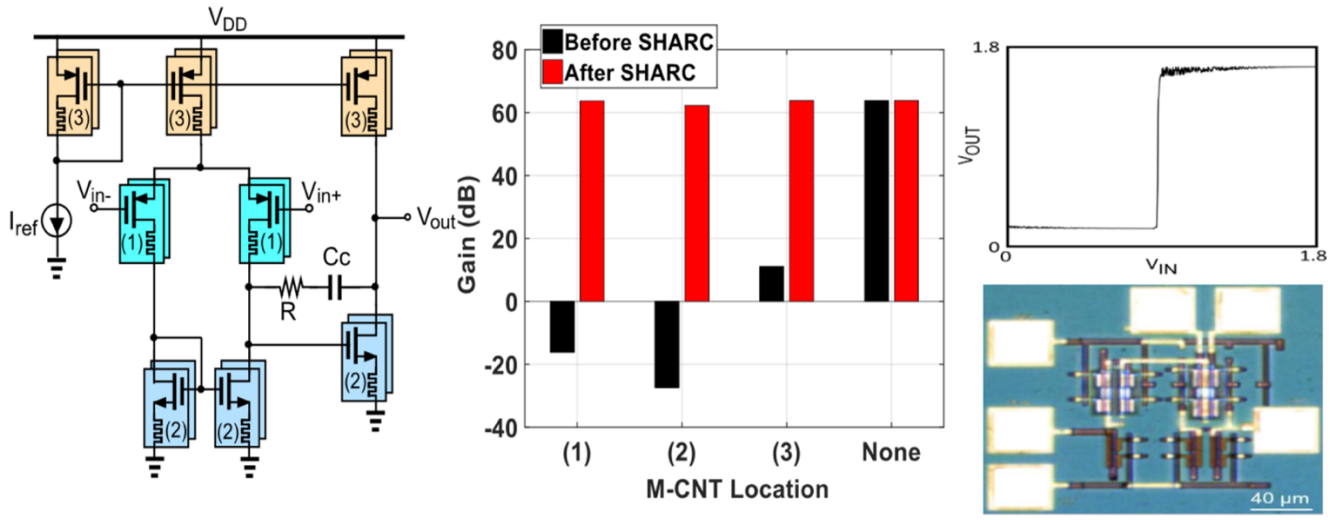

Figure 3.6. Two-stage op-amp with SHARC. (left) Schematic. (middle) Gain (dB) of op-amp when an m-CNT is located in different locations of the op-amp (labeled in schematic) before and after SHARC. Before SHARC, gain can reduce by >100 dB, while after SHARC gain is reduced by a maximum of 3 dB. (right) Die photo and experimental measurement of op-amp using SHARC, achieving gain >800.

Table 3.1. Comparison of this work to state-of-the-art CNFET CMOS demonstrations.

Circuit	CNFETs per Circuit	Reference
4b-ADC	**306**	**This Work**
4-bit full adder	132	Yang et al.
Inverter	2	
SRAM Cell	6	Geier et al.
Inverter	2	Han et al.
Ring Oscillator	12	
Inverter	2	Tang et al.
Inverter	2	Zhang et al.

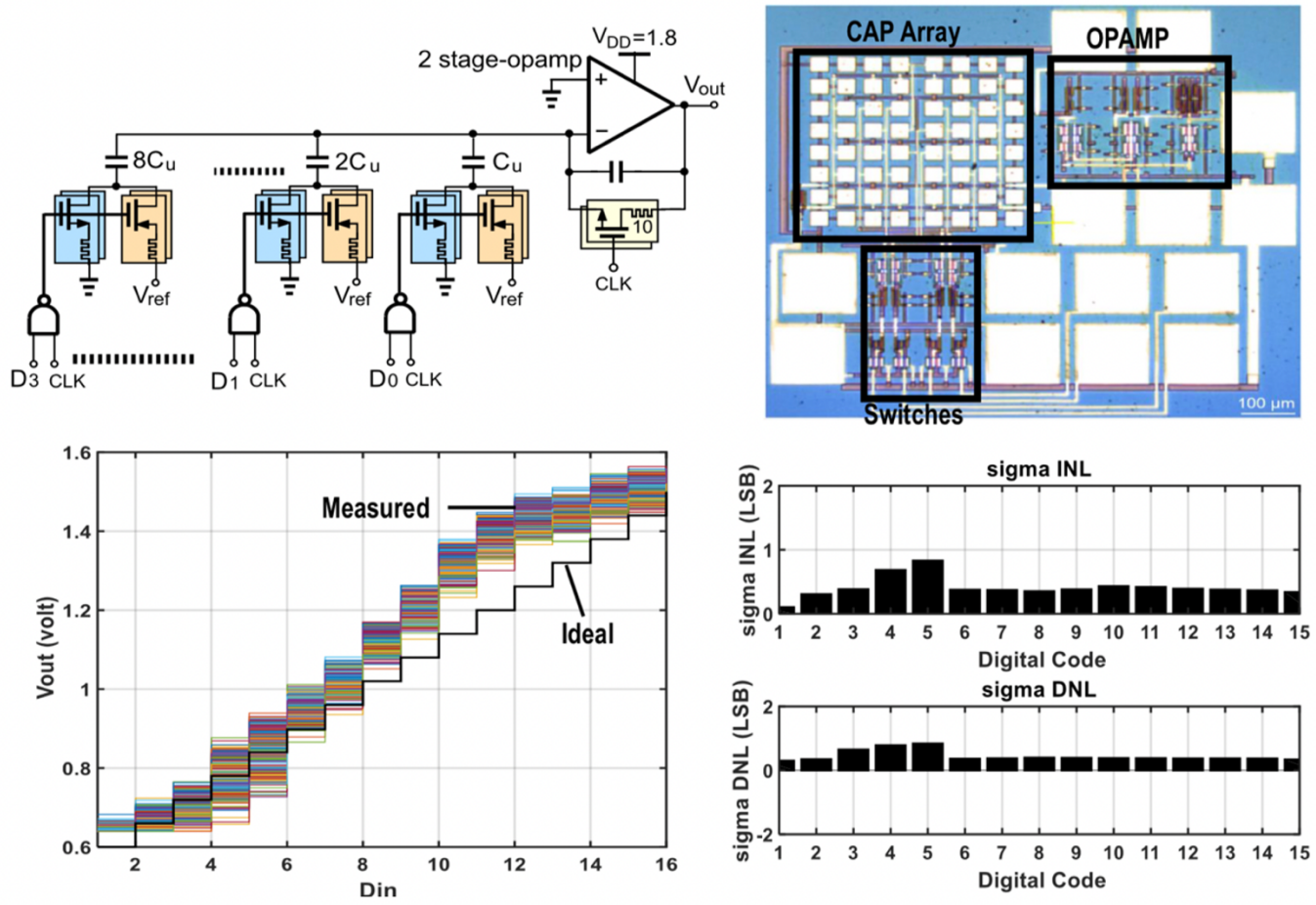

Figure 3.7. 4-bit capacitive DAC with SHARC. (top) Schematic and die photo. (bottom) Measured characteristics show the monotonic behavior with offset (50mV) and non-linearity where the maximum σ_{INL} and σ_{DNL} is 0.8 LSB.

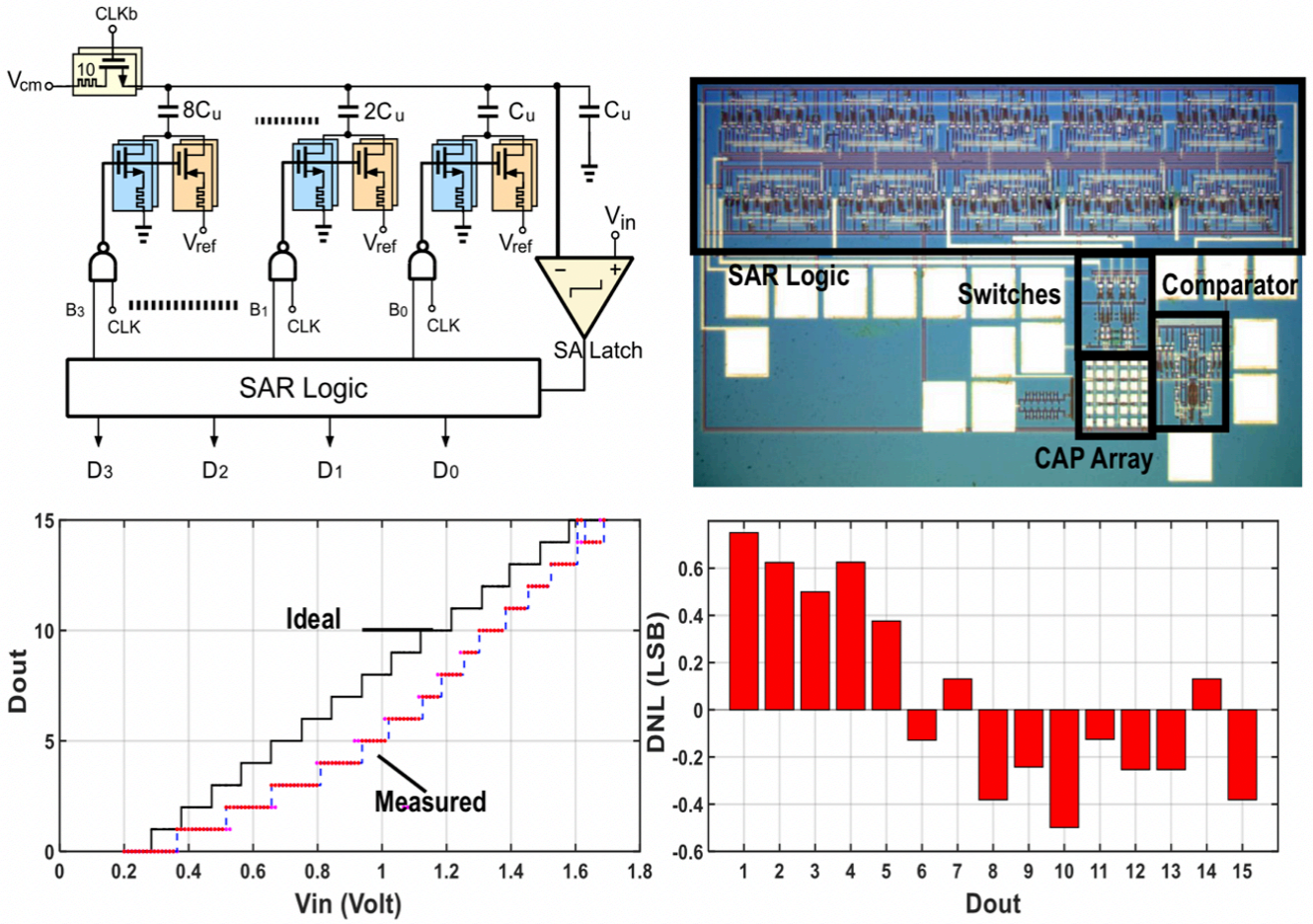

Figure 3.8. 4-Bit SAR ADC with SHARC. (top) Schematic and die photo. (bottom) Measured characteristics show the ADC behavior with offset (35mV), non-linearity and gain error whereas the DNL (-0.5 LSB→0.75 LSB).

3.6 Conclusion

We experimentally validate a new circuit design technique, SHARC, that overcomes the presence of m-CNTs on analog circuits. This technique is enabled by the programmability of non-volatile RRAM, and it utilizes the ability to fabricate monolithic 3D circuits with CNFETs. By placing RRAM in series with the CNFETs, the circuit is able to automatically "self-heal" by resetting any RRAM in series with an m-CNT to its high-resistance state. Importantly, by integrating RRAM and CNFET cells through shared metal layers and removing the need for

interconnects between device layers, SHARC demonstrates the finest-grained connectivity achieved through monolithic 3D integration to-date.

Using SHARC, we experimentally demonstrate the first mixed-signal and complex analog circuits with CNFETs. The implementation of SHARC at the CNFET-level gives it versatility; it can be combined with additional existing circuit techniques to further improve performance, such as technology node scaling to improve energy efficiency and existing circuit topologies to improve linearity. Thus, SHARC can be leveraged to realize large-scale, energy-efficient analog and mixed-signal circuits with CNFETs.

Chapter 4: Towards High-Performance Analog Circuitry with CNFETs

4.1 Overcoming Scaling Effects on Analog Circuitry

Having experimentally demonstrated that analog and mixed-signal circuits can be successfully fabricated using CNFETs, the focus can now shift to more rigorous analysis of CNFET technology and monolithic 3D integration in the analog and mixed-signal domains. Analog circuitry is currently facing its own set of challenges, in part due to the exact approach used to overcome challenges in digital systems: scaling. Analog and digital circuits are often built on the same chip, meaning both circuits are affected by device scaling. While scaling of silicon FETs has computing efficiency benefits for digital circuitry [Dennard 1974], it also results in lower device intrinsic gain and thus negatively effects analog circuits (Fig. 2.1).

The degradation of intrinsic gain poses new obstacles for analog circuit design. Less gain produces a need for more complex circuitry to meet speed and resolution requirements, which results in reduced signal range and greater power requirements. Advanced design techniques such as digital calibration, zero-crossing-based circuits, and time-interleaving circuits have all been developed to address these challenges [Miyahara 2013; Chang 2014; Kull 2018]. Circuit performance can also be improved by giving analog circuit blocks a separate, higher power supply than that for digital. From a system point of view this is not optimal, as this requires another power supply off-chip or additional circuitry such as level shifters, DC-DC converters, etc. A naïve solution to overcoming these challenges in silicon could be to build analog circuit blocks at a relaxed node and digital circuits at an advanced node. However, this approach would necessitate discrete analog and digital chips and thus is not practical for traditional silicon circuits.

Building analog circuits with CNFETs could offer important benefits for overcoming some of the challenges analog circuitry is currently facing. First, CNFETs offer the potential for additional performance benefits for analog circuits. They have superior carrier transport even at very thin semiconductor body thickness when compared to conventional bulk semiconductors, which results in CNFETs having a higher effective drive current at scaled supply voltages and a lower gate capacitance. In addition to higher mobility and lower capacitance, CNFETs have high intrinsic gain even at scaled technology nodes (Fig. 2.1) [Hills 2018]. Analog circuits built with advanced CNFET technology could operate at lower supply voltages without requiring additional complex circuitry to compensate for the loss in signal range. Thus, CNFETs could enable simpler low-power high-performance ADCs. Second, because of the low-temperature fabrication of CNFETs and high interconnect density of monolithic 3D integration [Batude 2011; Panth 2013], separate CNFET analog circuitry could be built directly on top of a digital silicon chip (Fig. 4.1). With the analog and digital circuits being fabricated in separate processes, the performance benefits of both silicon and CNFETs could be realized for optimal chip design.

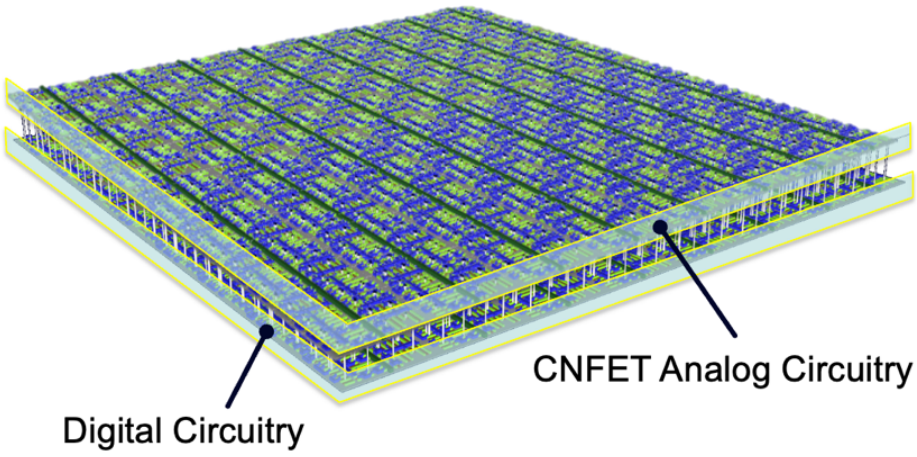

Figure 4.1. Illustration of a 3D chip where the analog circuitry is built separately on top of a digital substrate, leveraging monolithic 3D integration. This circuit topology can be realized with CNFETs due to their low-temperature fabrication and the high interconnect density achieved with monolithic 3D integration.

4.2 A Low-Power CNT CMOS Pipeline ADC

As a further exploration of how the benefits of CNFETs could be utilized in analog circuitry, preliminary simulations of a 10-bit pipeline ADC using 7-nm CNFET technology were performed. A compact model for CNFETs calibrated to experimental data for sub-10 nm nodes was used for all simulations [Hills 2018]. The ADC consists of 10x 1.5-bit stages (Fig. 4.2). 1.5-bit stages were used because they introduce redundancy into bit decisions, which increases the ADC's tolerance of component imperfections. The output of a typical 1.5-bit stage is shown in Fig. 4.3. The input is sampled on a sampling StrongARM latch and multiplying digital-to-analog converter (MDAC) in Stage 1, with the decision bits from the StrongARM latch being outputted to the MDAC to calculate the residue for the next stage. Fig. 4.4 displays the schematic of the sampling StrongARM latch. The MDAC is shown in Fig. 4.5. All subsequent stages consist of a differential StrongARM latch (Fig. 4.6) and MDAC. Within each MDAC is a two-stage fully differential op-amp with

common-mode feedback (CMFB). The op-amp topology and open-loop gain and phase margin are shown in Fig. 4.7.

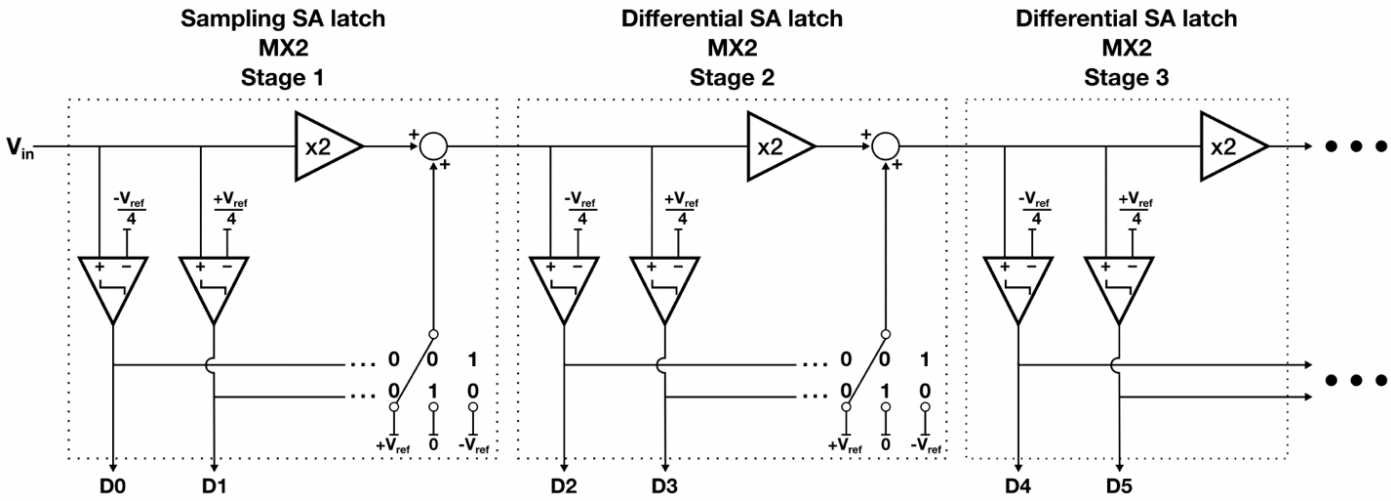

Figure 4.2. Pipeline ADC architecture. The differential input is sampled on two StrongARM (SA) latches in stage 1, and a multiply-by-2 (MX2) DAC is used to calculate the residue. For an input of 00 the residue is $2V_{IN} + V_{REF}$, for 01 it is $2V_{IN}$, and for 10 it is $2V_{IN} - V_{REF}$, where V_{REF} = 250 mV in this design. For all subsequent stages, differential StrongARM latches are used to make bit decisions.

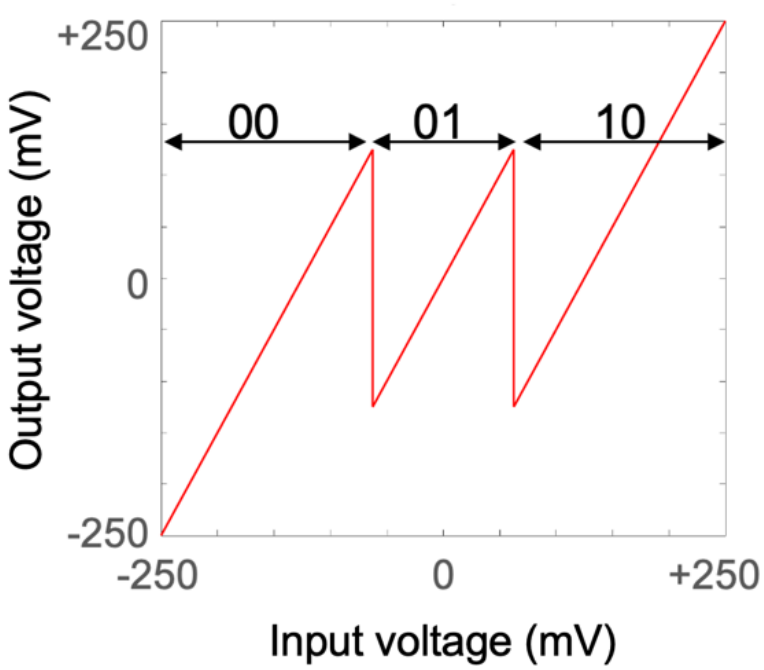

Figure 4.3. 1.5-bit stage output. In a 1.5-bit stage, 2 StrongARM latches are used to determine if the input is below $-V_{REF}/4$ (00 output), between $-V_{REF}/4$ and $+V_{REF}/4$ (01 output), or above $+V_{REF}/4$ (10 output), where V_{REF} = 250 mV in this design.

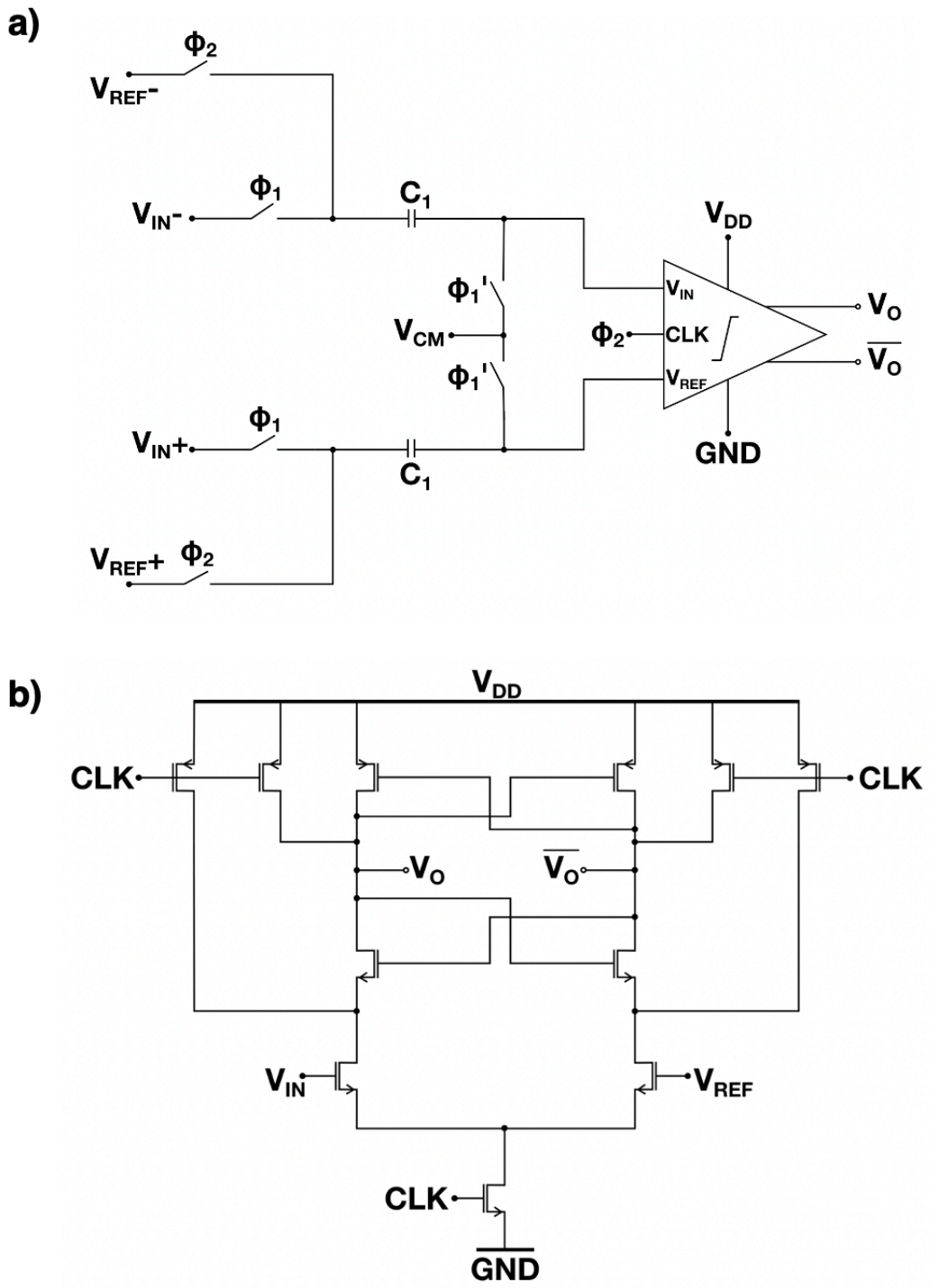

Figure 4.4. Sampling StrongARM latch. (a) Schematic showing sampling circuitry and StrongARM latch inputs and outputs. The differential input is sampled on sampling capacitors (C_1) in the first phase of the clock cycle (φ_1). $\pm V_{REF}/4$ is subtracted from the input in the second phase of the clock cycle (φ_2). φ_1 is slightly delayed from φ_1' for charge injection purposes. (b) Schematic of the StrongARM latch. Inverters are applied at the StrongARM latch outputs. $V_{REF} = V_{CM} = 250$ mV in this design.

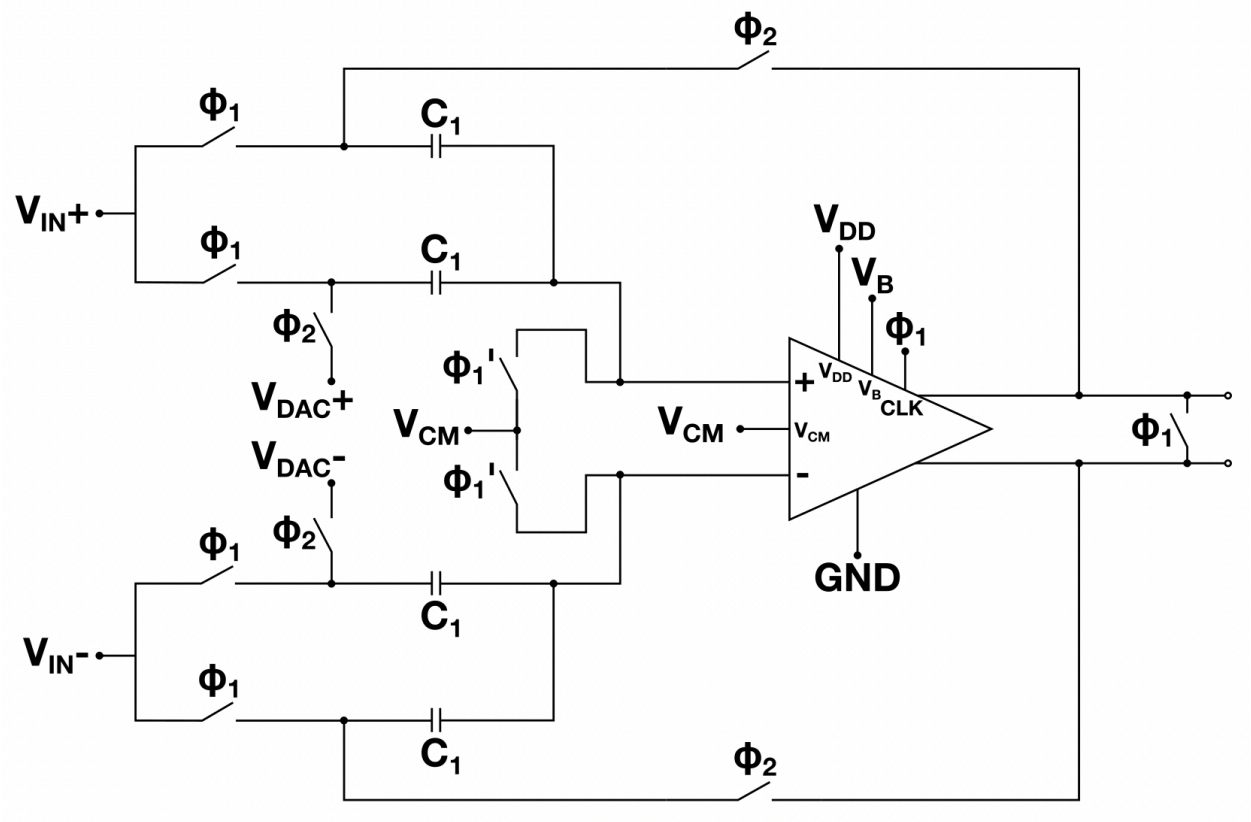

Figure 4.5. Multiply-by-two digital-to-analog converter. The differential input ($V_{IN} = V_{IN}+ - V_{IN}-$) is sampled on sampling capacitors (C_1) in the first phase of the clock cycle (φ_1). In the second phase of the clock cycle (φ_2), a voltage dependent on the bit decision from the StrongARM latch ($V_{DAC} = V_{DAC}+ - V_{DAC}-$) is applied at the input. Based on labels in this schematic, $V_{OUT} = 2V_{IN}–V_{DAC}$. $V_{DAC} = -250$ mV for 00, $V_{DAC} = 0$ for 01, and $V_{DAC} = 250$ mV for 10). φ_1 is slightly delayed from φ_1' for charge injection purposes. Within each MDAC is a 2-stage fully differential op-amp.

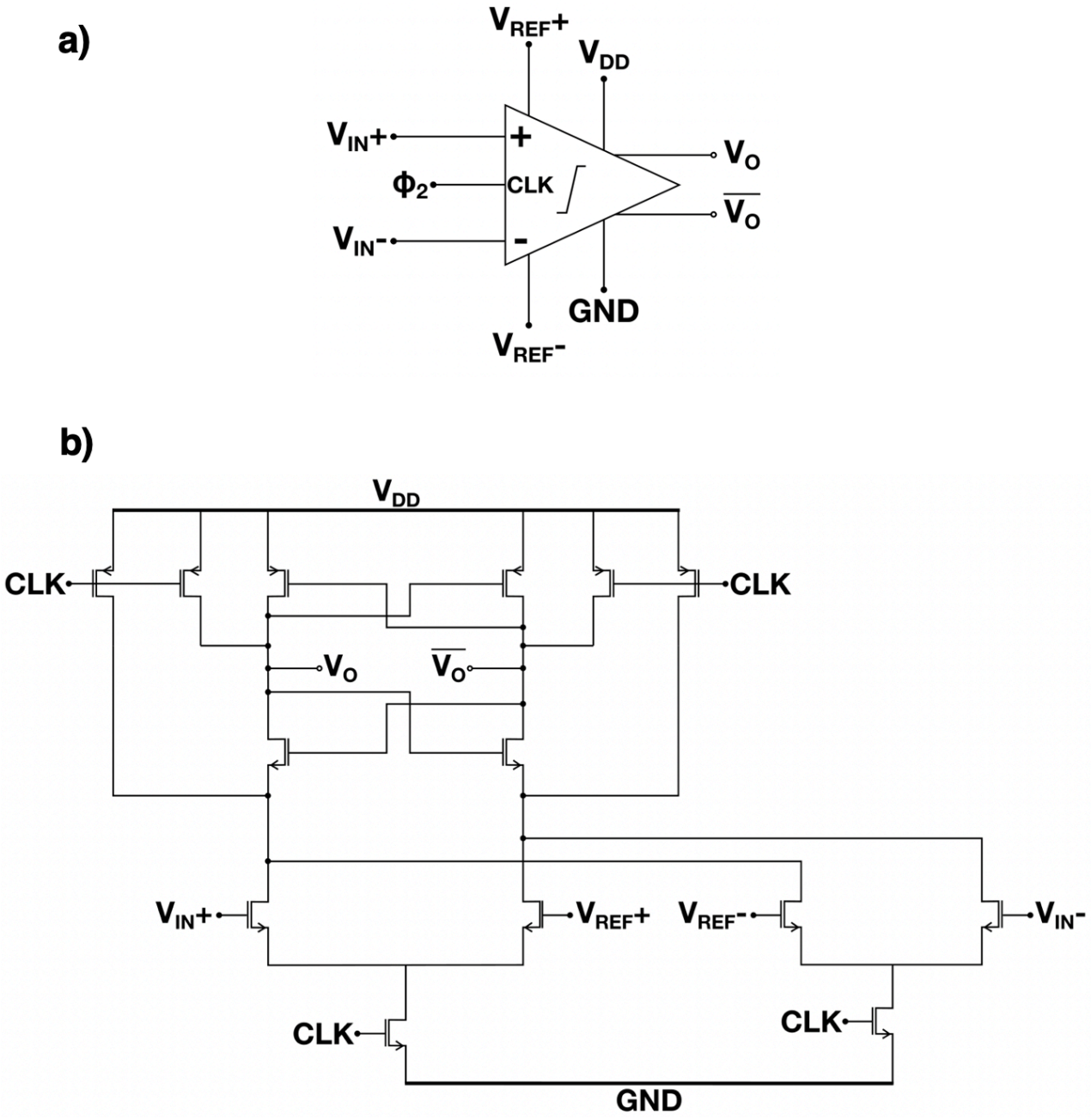

Figure 4.6. Differential StrongARM latch. (a) Circuit schematic showing StrongARM latch inputs and outputs. Two differential inputs ($V_{IN} = V_{IN}+ - V_{IN}-$ and $V_{REF} = V_{REF}+ - V_{REF}-$) are input to the StrongARM latch. (b) Transistor-level circuit diagram. For these schematics, $V_{REF} = \pm 250\text{mV} / 4 = \pm 62.5$ mV. Inverters are applied at the outputs (not shown).

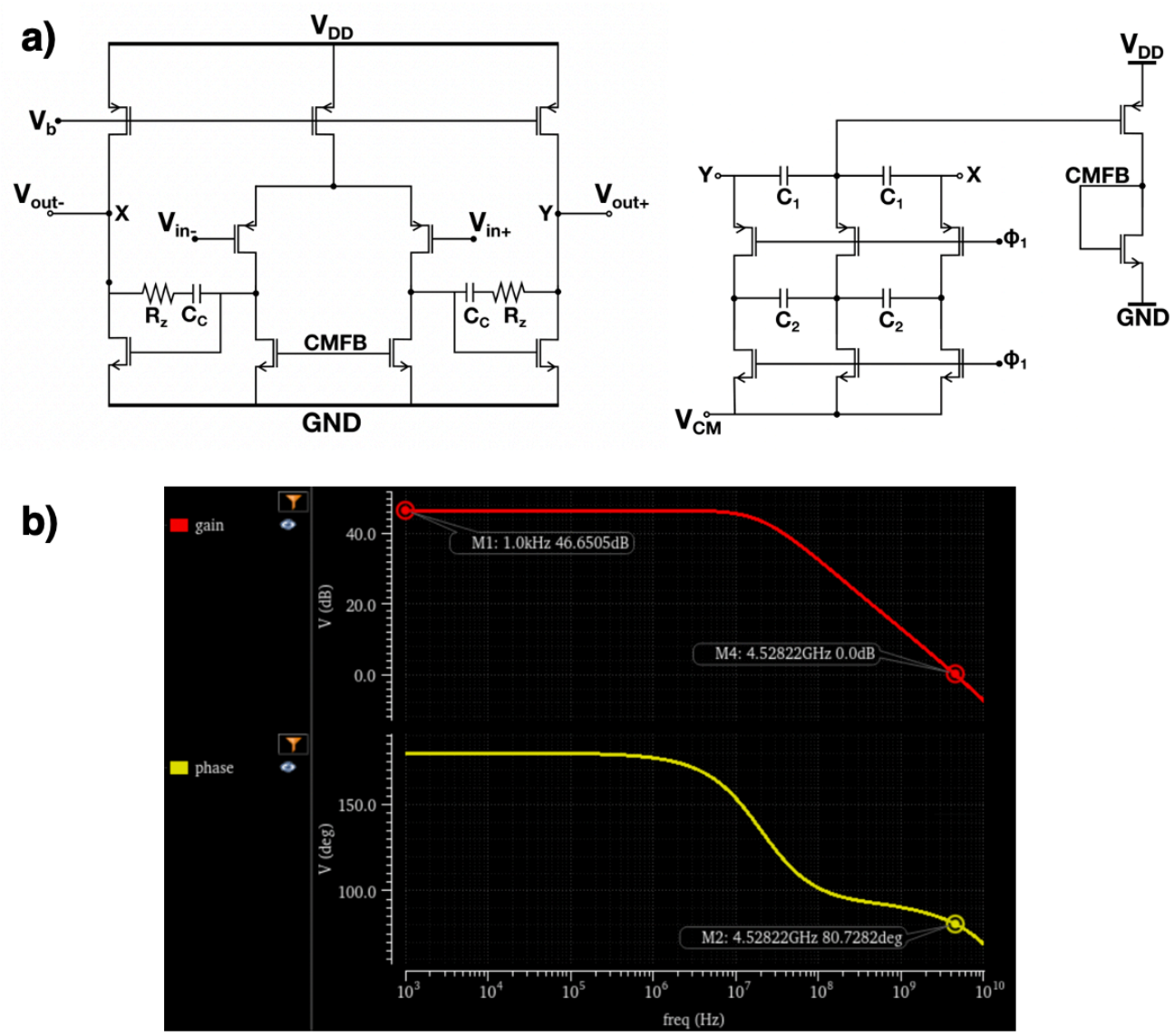

Figure 4.7. 2-stage fully differential op-amp with CMFB. (a) Circuit schematic. (b) Op-amp DC open-loop gain and phase margin. Each op-amp has a gain of 46.65 dB and unity-gain frequency (f_u) of 4.53 GHz. At f_u the phase margin is 80.73°.

The ADC runs on a scaled supply voltage of 500 mV at a clock frequency of 83 MHz. It consumes 0.64 mW of power, giving it a Walden figure of merit (FOM_W) of 7.5 fJ/conversion step ($FOM_W = \frac{Power}{f_s * 2^{ENOB}}$, where ENOB is effective number of bits and f_s is the sampling frequency. f_s =

$2*f_b$, where f_b is the signal bandwidth). FOM_W relates ADC performance to power consumption. This calculation assumes an ENOB of 10, which is optimistic.

Shown in Fig. 4.8, a differential input from -250 to 250 mV was applied to the input of the ADC and the subsequent output was measured and digitally calibrated [Karanicolas 1993]. The differential nonlinearity (DNL) of the response improved with digital calibration performed after the measurement (Fig. 4.9).

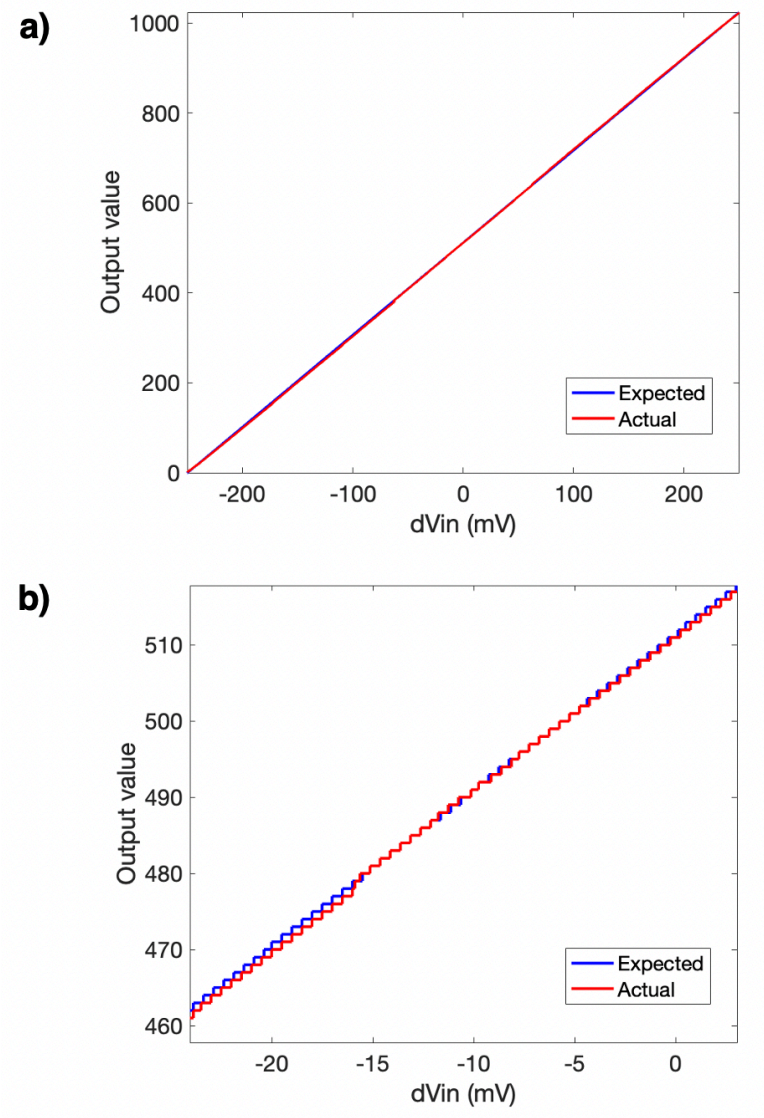

Figure 4.8. (a) Output of the ADC across a differential input of -250 to 250 mV and (b) magnified version of the output across -25 to 5 mV. The simulated ADC output is in red, while the expected output is in blue.

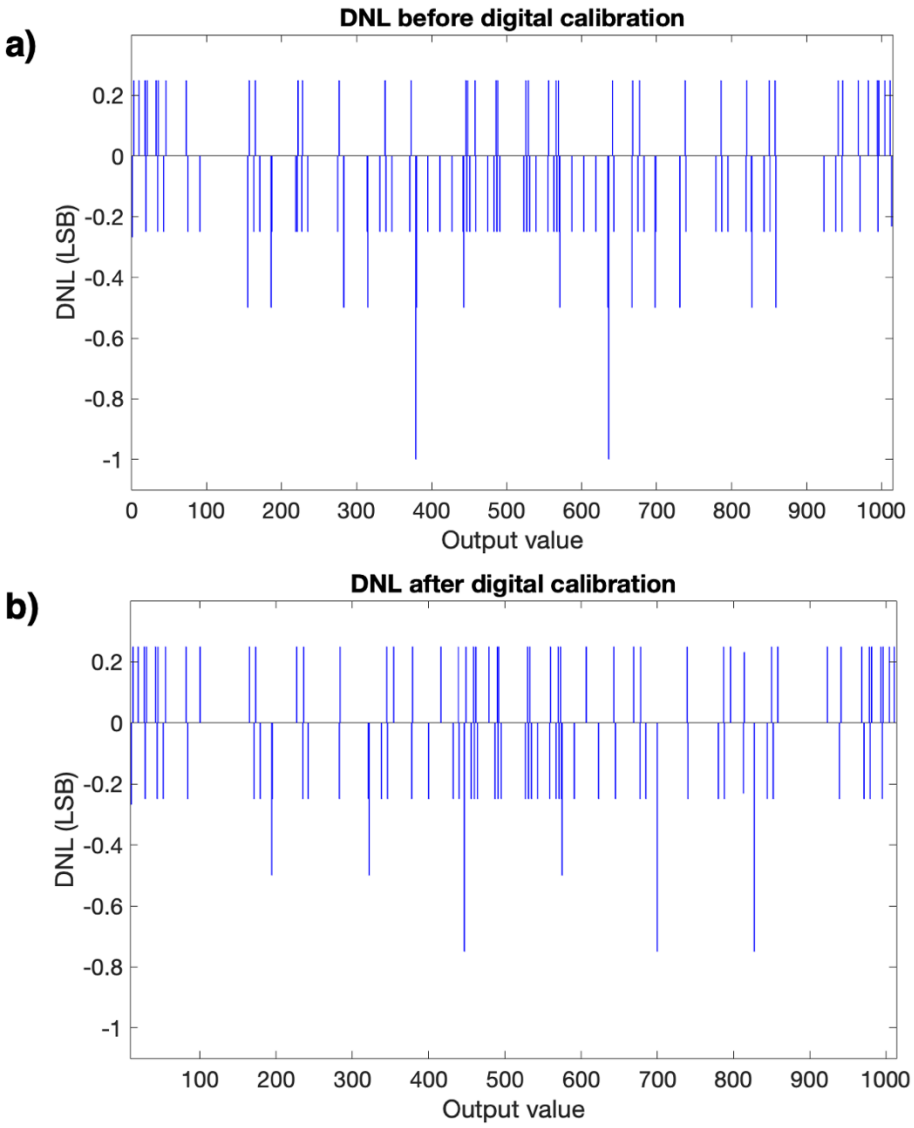

Figure 4.9. DNL of the ADC output (a) before and (b) after digital calibration.

These simulations show promising results for designing low-power analog circuits with advanced CNFET technology. However, future work will need to incorporate and optimize for device noise and parasitic capacitance. The layout of the ADC is shown in Fig. 4.10.

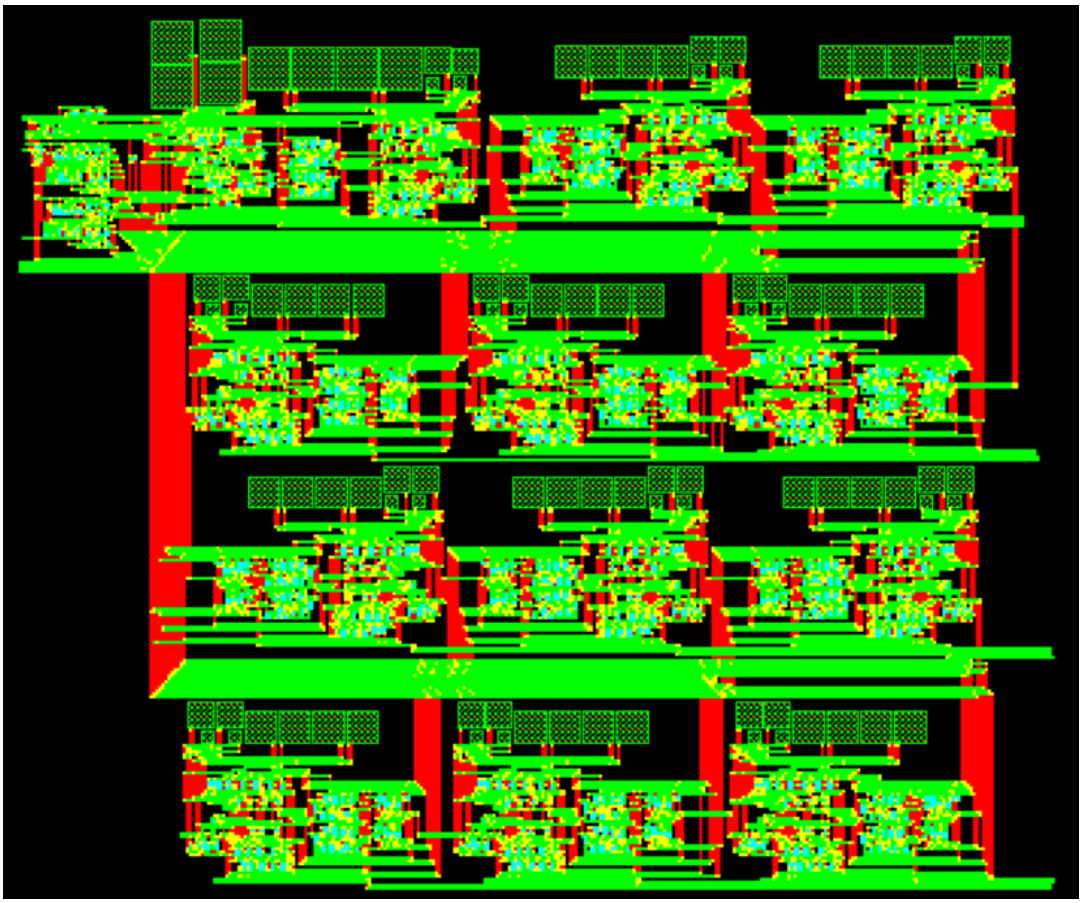

Figure 4.10. Layout of a 10-bit CNFET-based pipeline ADC. Extra stages were added in the layout for additional bit precision and testing purposes.

4.3 *1/f* Noise Considerations

Noise is an important consideration when designing high performance analog circuits, as excessive noise can negatively affect circuit resolution and signal-to-noise ratio (SNR). There are multiple sources of noise (shot, thermal, etc.), but of particular interest to CNFETs is low-frequency (*1/f*) noise, as previous studies have reported notably high *1/f* noise in devices made with CNTs [Collins 2000].

1/f noise is a concern across advanced CMOS transistors because it is inversely related to device area. Physical scaling of devices has thus necessitated accurate noise models to address

these effects. Models of *1/f* noise are generally based on two approaches: fluctuation in the mobility of free carriers in the conducting channel, and fluctuation in the number of carriers due to generation-recombination noise between the channel conduction band and traps in the oxide layer [Nemirovsky 2011].

Developing a model of *1/f* noise requires noise characterization of the devices, which is typically done by measuring S_{Id}, the current noise power spectral density (PSD). Measurements of device transconductance (g_m) allows for the voltage input-referred noise PSD (S_{VG}) to be calculated ($S_{VG} = S_{Id}/g_m$).

Previous work shows CNTs have *1/f* noise amplitude (A)[5] 4-10 orders of magnitude higher than conventional conductors, which the authors propose is due to surface fluctuations [Collins 2000]. Later work argues that *1/f* noise in CNFETs is inversely related to the number of carriers in the device and independent of metal contacts. The authors of these papers suggest adding multiple CNTs in parallel to increase the number of charge carriers and lower *1/f* noise [Appenzeller 2007; Lin 2007].

With the recent development of a robust CMOS CNFET process flow and realization of the first analog circuits made with CNFETs, it is important to understand device *1/f* noise to enable the development of more advanced circuitry. We sought to characterize the *1/f* noise in our devices across multiple parameters, including different fabrication methods and device areas.

[5] The authors of this paper define noise power $S_{VG} = AV^2/f^{\beta}$, where β is used to determine how 1/f-like the noise power is and A is the dimensionless noise amplitude coefficient. By plotting A versus sample resistance (R) over their sample set, they found a direct proportionality between A and R where $A/R = 10^{-11}\ \Omega^{-1}$. To compare to other materials, A was found by using a characteristic device resistance $R = 100\ \Omega$.

4.4 *1/f* Noise in CNFETs: Experiment and Measurement Setup

The process flow used to fabricate CMOS CNFETs for noise characterization is the same as that described in Section 2.2. An additional step referred to as RINSE (removal of incubated nanotubes through selective exfoliation) is added after CNT deposition, which consists of adhesion coating followed by >1 hour soak and sonication in n-methyl-pyrrolidinone to remove large polymer clusters left from CNT incubation [Hills 2019]. All PMOS FETs are passivated with 100nm of SiO_2 unless stated otherwise. All anneals are performed at 275°C in N_2 for 5 min. A noise analyzer and parameter analyzer are used to measure S_{Id}, g_m, and I_D across different bias conditions at room temperature (Fig. 4.11). S_{VG} is calculated using measured S_{Id} and g_m.

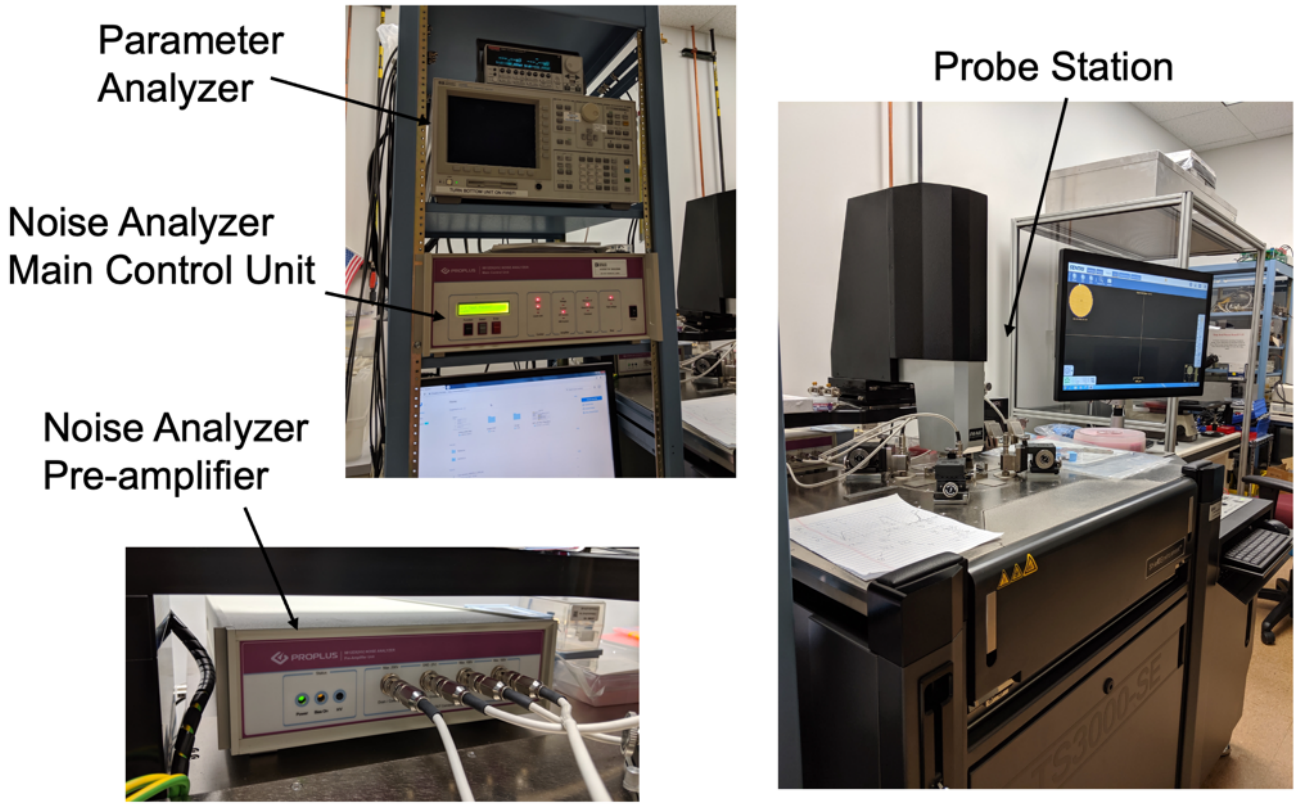

Figure 4.11. Noise measurement setup. All measurements were performed at Analog Devices, Inc.

4.5 *1/f* Noise in CNFETs: Measurement Results

Measurements of PMOS CNFETs show that *1/f* noise decreases when device width and length are increased (Fig. 4.12).

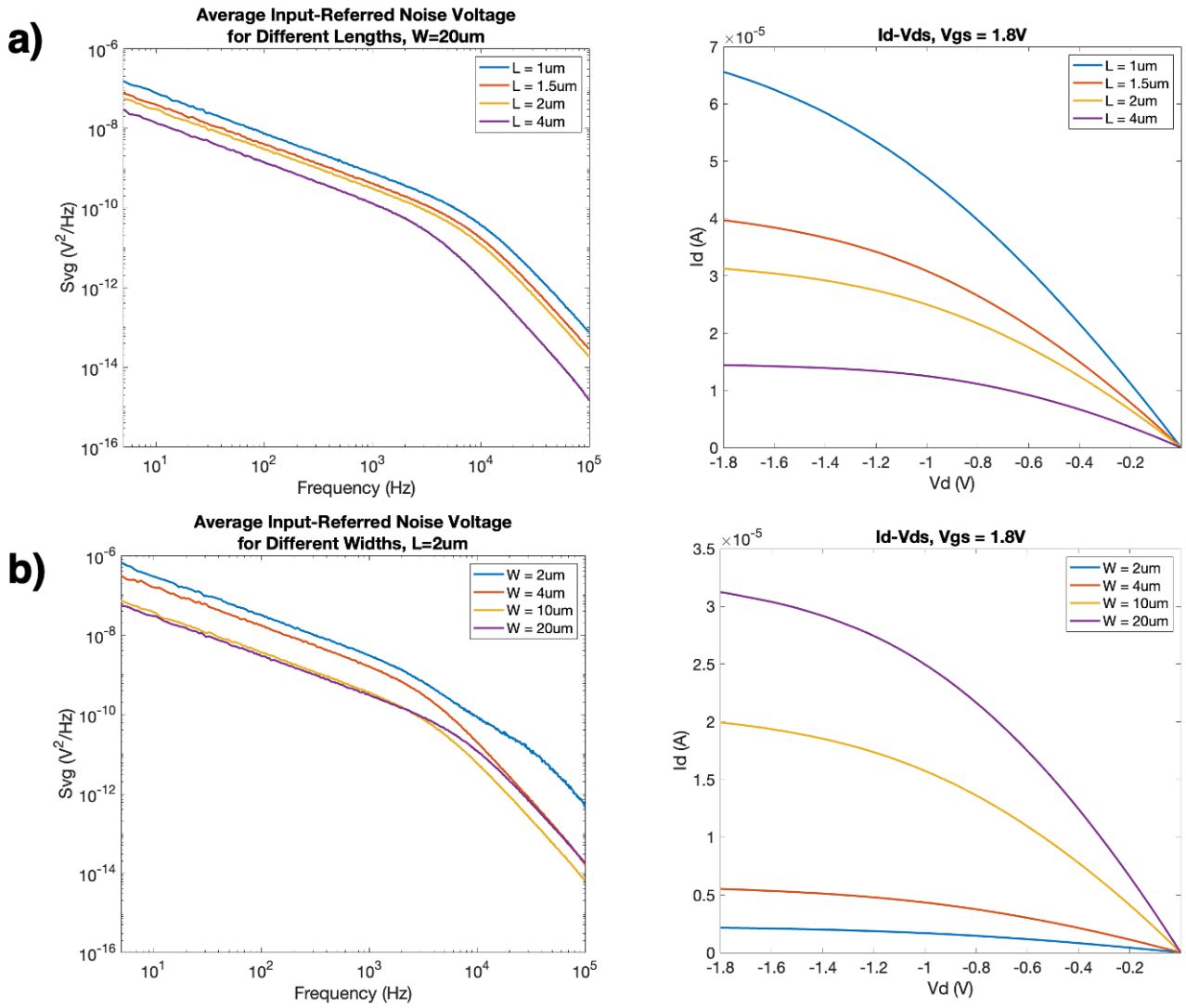

Figure 4.12. Input-referred voltage noise PSD (left) and I_D-V_{DS} (right) curves for PMOS CNFETs of varying channel (a) lengths (device width = 20μm) and (b) widths (device length = 2μm). Each curve represents the average measurement across 40 devices.

Different fabrication steps were omitted or altered to analyze their effects on noise. To understand the impact of RINSE, 3 types of PMOS CNFETs were measured: devices processed with 1) no RINSE, 2) room temperature RINSE, and 3) heated RINSE (60°C). Four die were fabricated, and an anneal was performed on 3 die after source/drain deposition. Room-temperature RINSE seems to slightly decrease *1/f* noise, while heated RINSE without an anneal step lowers device on-current and increases *1/f* noise by about 1 order of magnitude (Fig. 4.13).

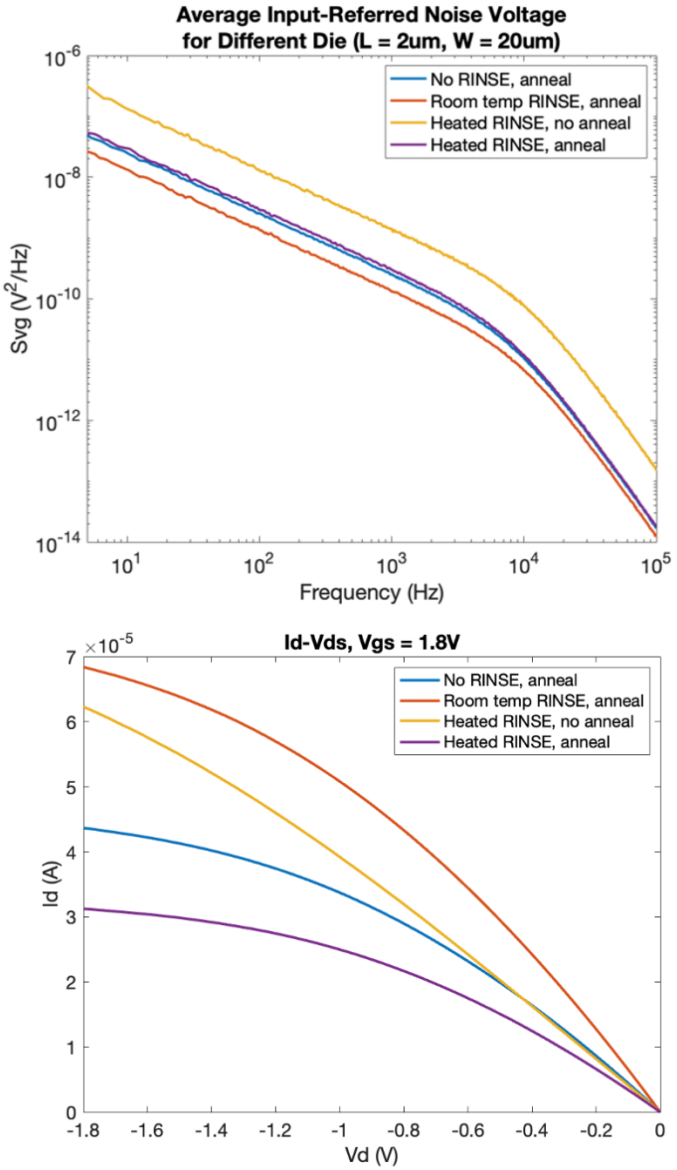

Figure 4.13. Input-referred voltage noise PSD (top) and I_D-V_{DS} (bottom) curves for PMOS CNFETs processed with different RINSE and anneal steps. Each curve represents the average measurement across ≥24 devices.

The effects of annealing and the timing of the anneal were also studied, with devices subjected to: 1) no anneal, 2) anneal after CNT deposition, 3) anneal after source/drain deposition. RINSE was performed on all devices in this experiment. These results show an anneal after source/drain deposition decreases noise by approximately 1 order of magnitude compared to devices that were not annealed. The timing of the anneal is significant, as devices that are annealed directly after

CNT deposition show greater *1/f* noise than those that are not annealed. Annealing after CNT deposition also degrades device on-current (Fig. 4.14).

Unpassivated and passivated (100nm SiO2) PMOS CNFETs were also measured. The difference in *1/f* noise between the two sets of devices appears minimal (Fig. 4.15).

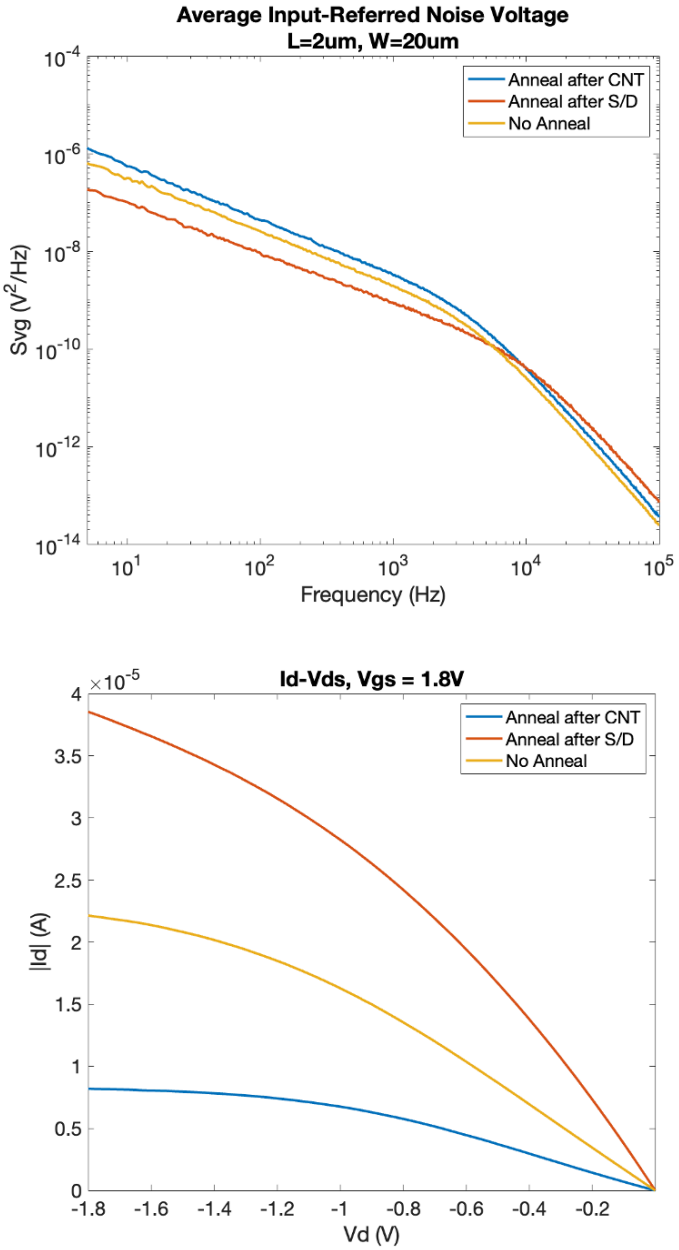

Figure 4.14. Input-referred voltage noise PSD (left) and I_D-V_{DS} (right) curves for PMOS CNFETs processed with different anneal timings. Each curve represents the average measurement across ≥26 devices.

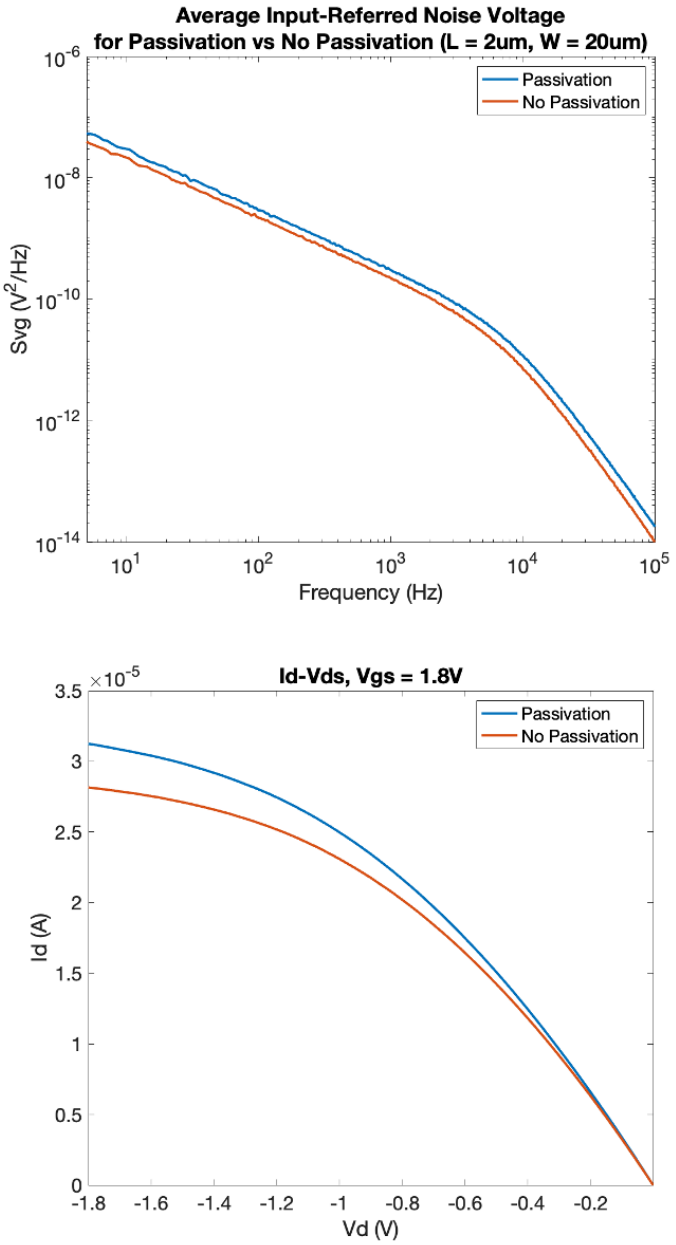

Figure 4.15. Input-referred voltage noise PSD (left) and I_D-V_{DS} (right) curves for PMOS CNFETs that were either unpassivated or passivated with 100nm of SiO_2. Each curve represents the average measurement across ≥35 devices.

When looking at different CNT solutions, the *1/f* noise of PMOS CNFETs fabricated with isoSOL-100 is about 2 orders of magnitude lower than those fabricated with s-Tetrazine copolymer

CNTs. These results emphasize the importance of the manufacturing process used to generate and sort CNTs, as it has a significant impact on both the CNT quality and 1/*f* noise (Fig. 4.16).

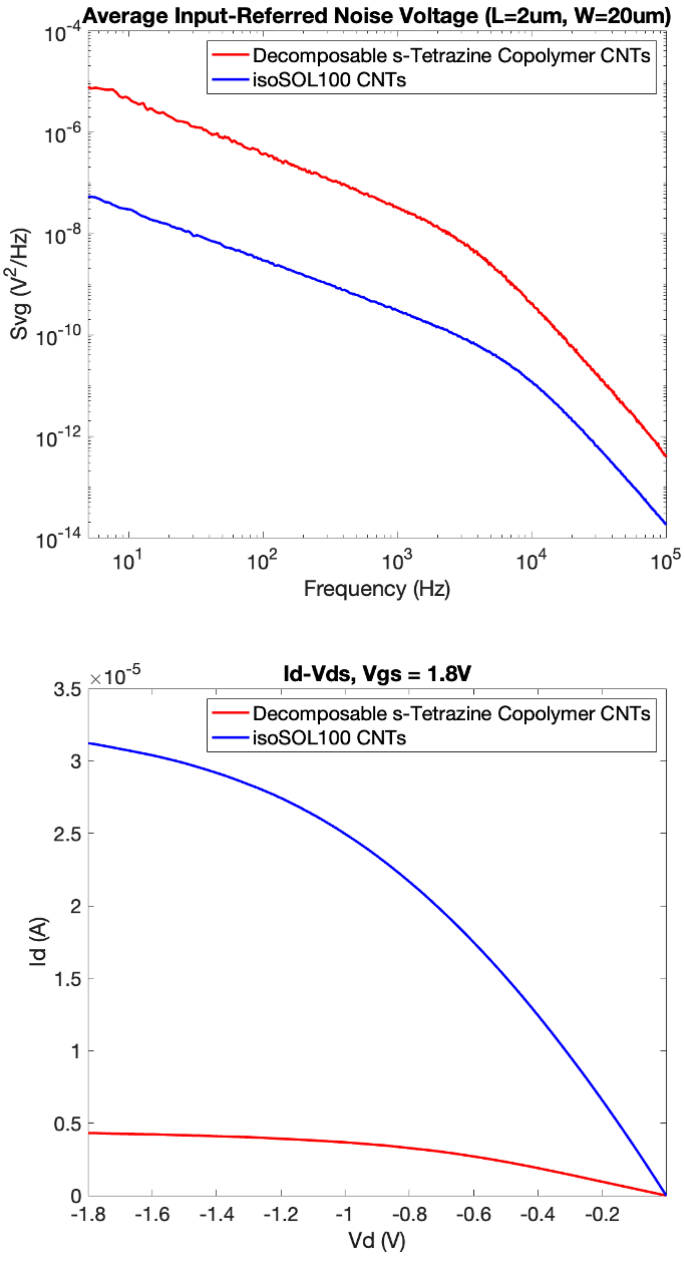

Figure 4.16. Input-referred voltage noise PSD (left) and I_D-V_{DS} (right) curves for PMOS CNFETs fabricated with 2 different CNT solutions. Each curve represents the average measurement across ≥25 devices.

CNFETs have recently been integrated into VLSI-compatible commercial fabrication facilities and foundries. PMOS CNFETs fabricated in an industry foundry are compared to those fabricated at MIT. Without any optimization of the industry CNFET process flow for noise, the industry CNFETs still show >1 order of magnitude lower noise when normalized for device area (Fig. 4.17).

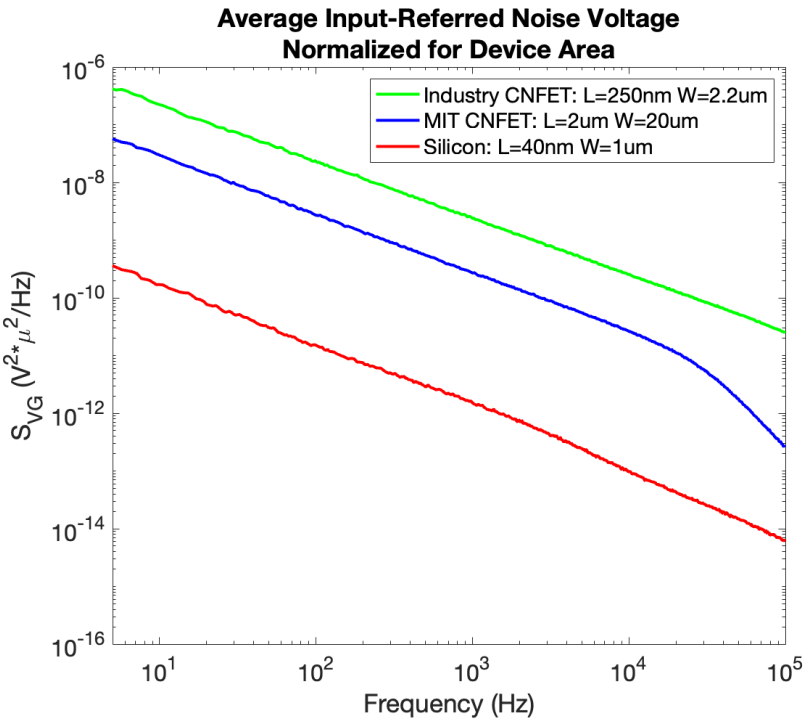

Figure 4.17. Input-referred voltage noise PSD normalized for device area for 2µm x 20µm PMOS CNFETs fabricated at MIT, 250nm x 2.2µm PMOS CNFETs fabricated in a commercial foundry, and 40nm x 1µm silicon FinFETs. Measurements are normalized to 1µm^2 area. Each curve represents the average measurement across ≥23 devices.

To understand how CNFETs compare to advanced silicon FETs, 40-nm technology node silicon FETs were measured. When normalized for device area, the *1/f* noise of industry CNFETs is about 2 orders of magnitude greater than that of the silicon FETs (Fig. 4.17).

4.6 Reducing *1/f* Noise in CNFET Circuits

Based on these experiments, there are several pathways that can be taken to decrease *1/f* noise in CNFETs. Removing excess polymer after CNT deposition through RINSE and annealing the CNFETs after source/drain deposition appear to be effective ways to lower noise. Fabricating CNFETs in a commercial foundry versus a shared fabrication facility also reduces noise, likely due to less process variability and fewer contaminates. Although the *1/f* noise in CNFETs fabricated in a commercial foundry is still about 2 orders of magnitude higher than that of silicon FETs, the process flow of CNFETs in industry has yet to be optimized for noise. By adding in an anneal step and performing further experiments, this noise will be reduced and could approach the noise of current silicon technologies.

In addition to optimizing the process flow, different circuit design techniques could also be employed to remove system noise. When considering the pipeline ADC mentioned in the previous section, a design technique known as digital chopping could be employed to remove the higher *1/f* noise contributed by CNFETs [Gulati 2001]. This is achieved by multiplying the input of the ADC by 1 and -1 in an alternate manner to modulate the input signal around the chopping frequency. The digital output is then demodulated by multiplying the digital output by 1 and -1 to demodulate the signal back to the baseband. In the process, the 1/f noise is modulated up to the chopping frequency, which is then low-pass filtered out by a digital filter.

4.7 Conclusion

CNFET analog circuits could leverage the benefits of CNTs and novel 3D circuit architectures to enable exciting new systems beyond the current state-of-the-art. From chips on which both the analog and digital circuitry are fabricated for optimal performance, to nanosystems where sensing

blocks are built directly on top of analog compute circuitry for enhanced data processing, developing robust analog circuitry with CNFETs could enable a wide range of applications. The work in this thesis shows analog and mixed-signal circuits can be successfully fabricated with CNFETs; however, there remain device characteristics, such as noise, which require further consideration before more advanced analog circuitry can be realized with this emerging technology. Additional research into optimizing CNFET fabrication and circuit design for these design considerations could bring this technology closer toward integration into current and future systems.

Chapter 5:
Beyond Computing – Carbon Nanotube Biosensor Chips for Point-of-Care Diagnostics

5.1 Limitations of Conventional Diagnostics

With the rise of personalized healthcare and the recent COVID-19 pandemic, the demand for devices that provide access to personal health markers has increased tremendously. This has resulted in the introduction of products like smartwatches, which connect to smartphone apps to seamlessly provide users with information about biometrics such as their heartrate or number of steps taken in a day, and increased use of at-home tests, such as lateral-flow tests for COVID-19 or the numerous "kits" that exist today to diagnose everything from food sensitivities to fertility.

However, despite this progress in personal health, significant limitations in rapid diagnostics and biomarker tracking still exist both at home and in a point-of-care setting. The commonly used rapid lateral flow assay, which exists for a range of applications from pregnancy to strep throat, has limited accuracy, is subject to human error in the readout process, and is difficult to multiplex [Wu 2020]. Additionally, these types of tests cannot provide information about the specific quantity of analyte present. Other same-day diagnostic methods, such as urine dipstick tests used for assessing urinary tract infections (UTIs), often offer limited information about a patient's disease state and cannot provide important information such as identification of the specific pathogen causing the disease (which is crucial for accurate treatment prescription).

There exists a need for health testing that can perform fast, accurate readout without the risk of human error. Emerging nanotechnologies have shown promise towards realizing these types of

diagnostics due to the numerous ways they can be functionalized for biomedical applications, their high sensitivity to their surrounding environment, and their ability to be integrated with both flexible and conventional electronics. Demonstrations range from wearables that can noninvasively track bioelectric signals and sweat hormones [Kabiri Ameri 2017; Parlak 2018] to multiplexed sensor arrays for cancer biomarkers [Zheng 2005]. However, commercially realizing nanomaterial-based biosensing platforms has remained elusive. Issues inherent to devices fabricated from new materials, such as yield and device-to-device variations, are a major obstacle to reliably producing results that can meet clinical standards.

5.2 Carbon Nanotubes for Healthcare Application

CNFETs are an emerging nanotechnology that show promise for both their energy-delay product (EDP) benefits [Hills 2018] and sensing capabilities [Liu 2015; Kong 2000], and they have recently been incorporated within commercial fabrication facilities and foundries [Bishop 2020]. Demonstrations of CNTs covalently bound to antibodies for biomarker sensing have shown consistent and measurable responses when exposed to target antigens. However, such demonstrations were not solid-state compatible or had a limited number of devices, making them impractical for real-world application [Lerner 2013; Liang 2020; Bhardwaj 2017; Shao 2021].

Here, we combine the 200 mm wafer-scale and VLSI-compatible foundry fabrication of CNFETs with the mature sensing modality of antibody-based targeted antigen binding to demonstrate a biosensing platform capable of rapidly detecting and identifying bacteria within model urine. VLSI integration enables the fabrication of hundreds of CNFET sensors on a single chip, which we demonstrate experimentally is essential for accurate pathogen detection and identification. Such massive multiplexed sensor integration realizes two significant benefits: (1) it

overcomes variations and failures inherent to functionalizing emerging nanotechnologies, and (2) this in turn enables reliable and robust detection and identification of multiple pathogens within a single chip.

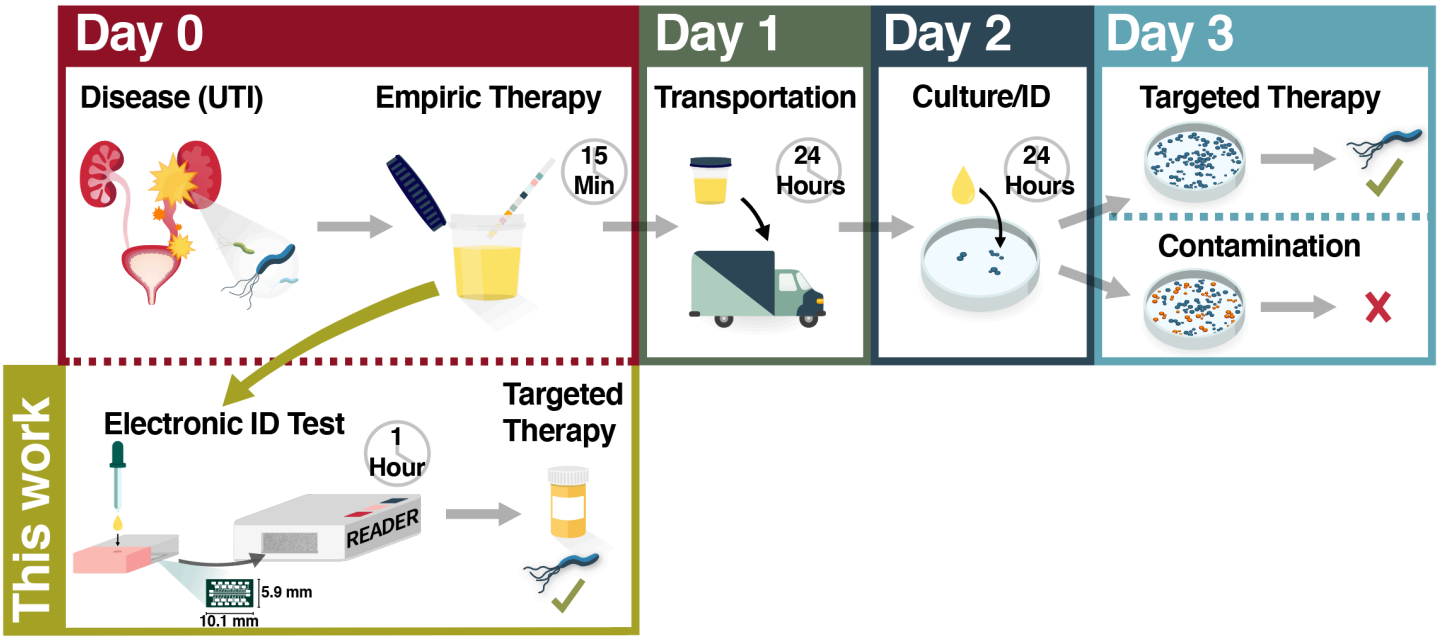

Figure 5.1. Application of our BioSensor chip versus today's conventional diagnostic process (example: UTI). Illustration shows how fully-electronic point-of-care test enables improved targeted therapy administered within 1 hour of sample acquisition, versus conventional testing today which requires multi-day workflows. Additional lab testing is still needed to perform antibiotic susceptibility testing, if required.

Fig. 5.1 depicts an example application of our BioSensor chip and the benefit of such a fully-electronic point-of-care diagnostic test. As illustrated in Fig. 5.1, today's conventional diagnostic process relies on empiric therapy (a clinical "educated guess") for initial treatment. However, such empiric therapy is often not optimal, as the infectious pathogen has not yet been identified. Conventional identification approaches today (such as culturing for single-colony purification) often take multiple days and still do not always result in a conclusive result. The major benefit of

realizing a fully-electronic point-of-care diagnostic test (such as the presented multiplexed CNFET BioSensor chip) is that – as we experimentally demonstrate – pathogen detection and identification can be completed within 1 hour of sample acquisition, enabling a more appropriate antibiotic therapy to be administered the same day of disease presentation.

5.3 CNFET BioSensor Fabrication

Fig. 5.2a-b displays the CNFET device structure and process flow of chip fabrication and functionalization. 200 mm CNFET wafers are fabricated in a foundry (SkyWater Technology Foundry), with each chip containing hundreds of identical CNFET sensors (pre-functionalization). Wafers are diced and individual chips are functionalized with target antibodies relevant to the desired application. Antibody-CNT binding is performed in a three-step process. First, chips are dispersed in 6 mM 1-pyrenebutanoic acid succinimidyl ester (PBASE) in dimethylformamide (DMF). To achieve multiplexing, different antibody solutions (50 μg/mL antibody in 10 mM phosphate-buffered saline, PBS) are separately applied to the four quadrants of the die to ensure four distinct sensor types. In this demonstration, the 4 functionalizations are: Pseudomonas aeruginosa monoclonal antibody, E. coli serotype O157 monoclonal antibody, Proteus mirabilis monoclonal antibody, and 10 mM PBS (as a control). The chips are incubated in a humid environment to prevent evaporation. Finally, chips are soaked in 0.01% Tween 20 in deionized water to reduce non-specific binding. In total, there are 128 sensors per functionalization, equaling 512 sensors per chip. The functionalization process is optimized to not increase the variability of the CNFETs (CNFET V_{TH} variability remains unchanged with functionalization, Fig. 5.2c).

To demonstrate our BioSensor chip's ability to detect three different bacteria, initial V_{GS} sweeps across all devices were performed with a custom handheld electronic reader. Chips were

then incubated for 1 hour in solutions containing either Pseudomonas aeruginosa, E. Coli, or Proteus mirabilis (common pathogenic bacteria, at concentrations similar to bacterial load in a common urinary tract infection, $200x10^3$ CFU/ml). Chips were dried gently with N_2 and post-exposure V_{GS} sweeps were performed. Each full-chip measurement is completed in less than 2 seconds.

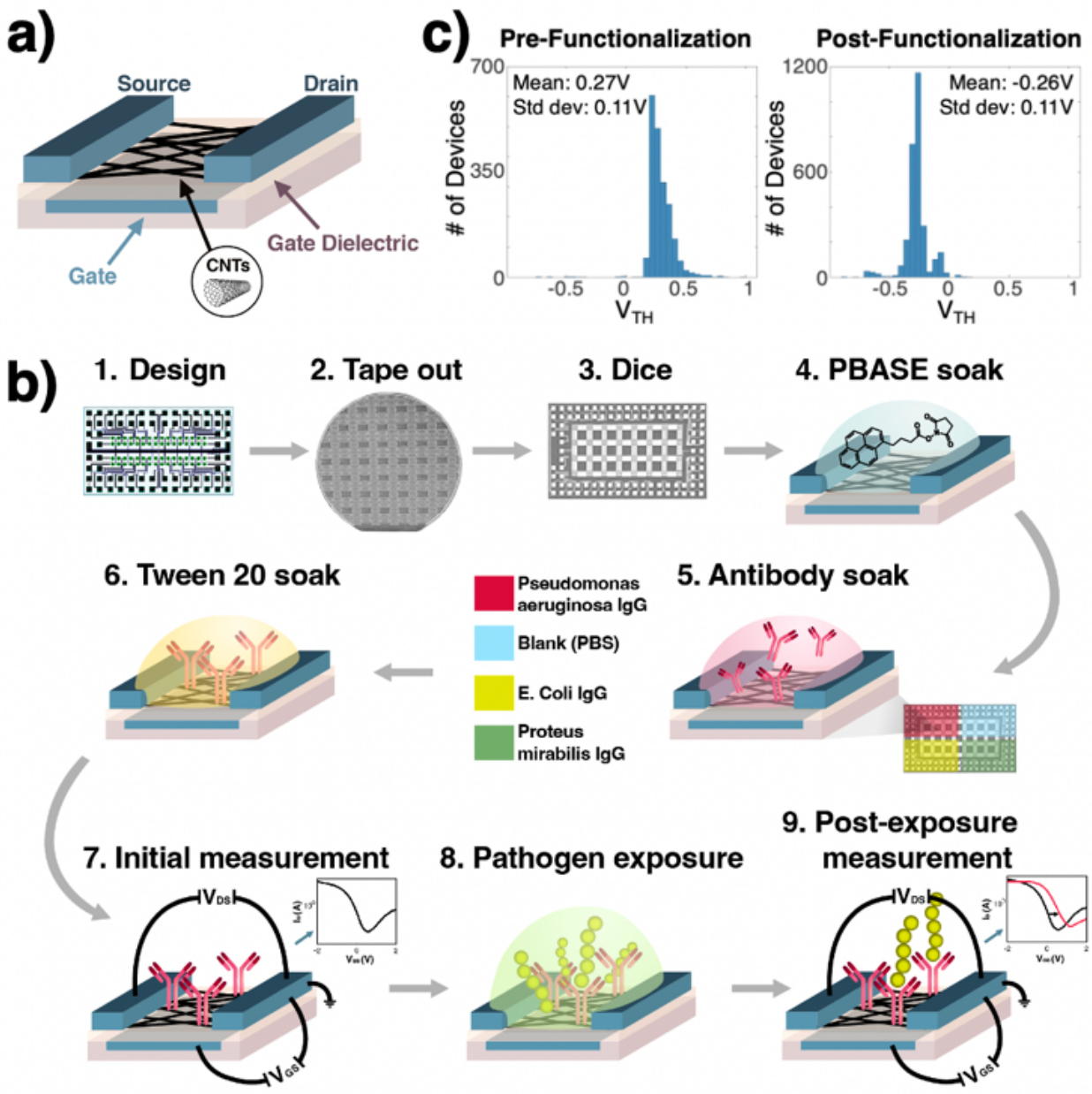

Figure 5.2. (a) CNFET schematic before antibody functionalization. (b) Process flow for fabricating and measuring BioSensor chips. Chip quadrants are functionalized with different antibodies to achieve multiplexing. (c) Histograms of CNFET V_{TH} distributions before (left) and after (right) antibody functionalization. The mean V_{TH} is 0.27V and -0.26V before and after antibody functionalization, respectively. The standard deviation of CNFET V_{TH} remains unchanged with functionalization at 0.11V.

5.4 CNFET BioSensor Experimental Results

BioSensor Chip Characterization

To test and characterize our Biosensor chips, we exposed multiple chips to each of the pathogenic bacteria. As illustrated in Fig. 5.3, exposure to a particular bacteria produces a significant V_{TH} shift only in the chip quadrant functionalized with the corresponding antibody for that bacteria. This shift is attributed to the antigen binding to the antibodies functionalizing the CNFETs. Chip quadrant functionalizations and plot color-coding are depicted in Fig. 5.3a. The specific pathogen each chip was exposed to is shown in Fig. 5.3b. I_D vs. V_{GS} measurements of the CNFET sensors in each chip quadrant are overlaid in Fig. 5.3c, showing the response of the sensors before and after exposure. The effect of targeted antigen binding on sensor V_{TH} can be further visualized in Fig. 5.3d, which displays histograms of device V_{TH} values for each quadrant before and after exposure, and Fig. 5.3e, which shows heatmaps of V_{TH} values and change across the entire chip. The significant V_{TH} shift that occurs only in the chip quadrant functionalized for the exposed pathogen indicates a measurable response to antibody-antigen binding.

The mechanism behind the V_{TH} shift is likely due to the negative electrostatic charge of bacteria cells [Bayer 1990]. This assumption is based on the positive V_{TH} shift in the PMOS FETs with antibodies corresponding to the exposed pathogen and the observation that device on-current appears unchanged by bacteria exposure and binding (indicating charge mobility is not affected by antigen binding).

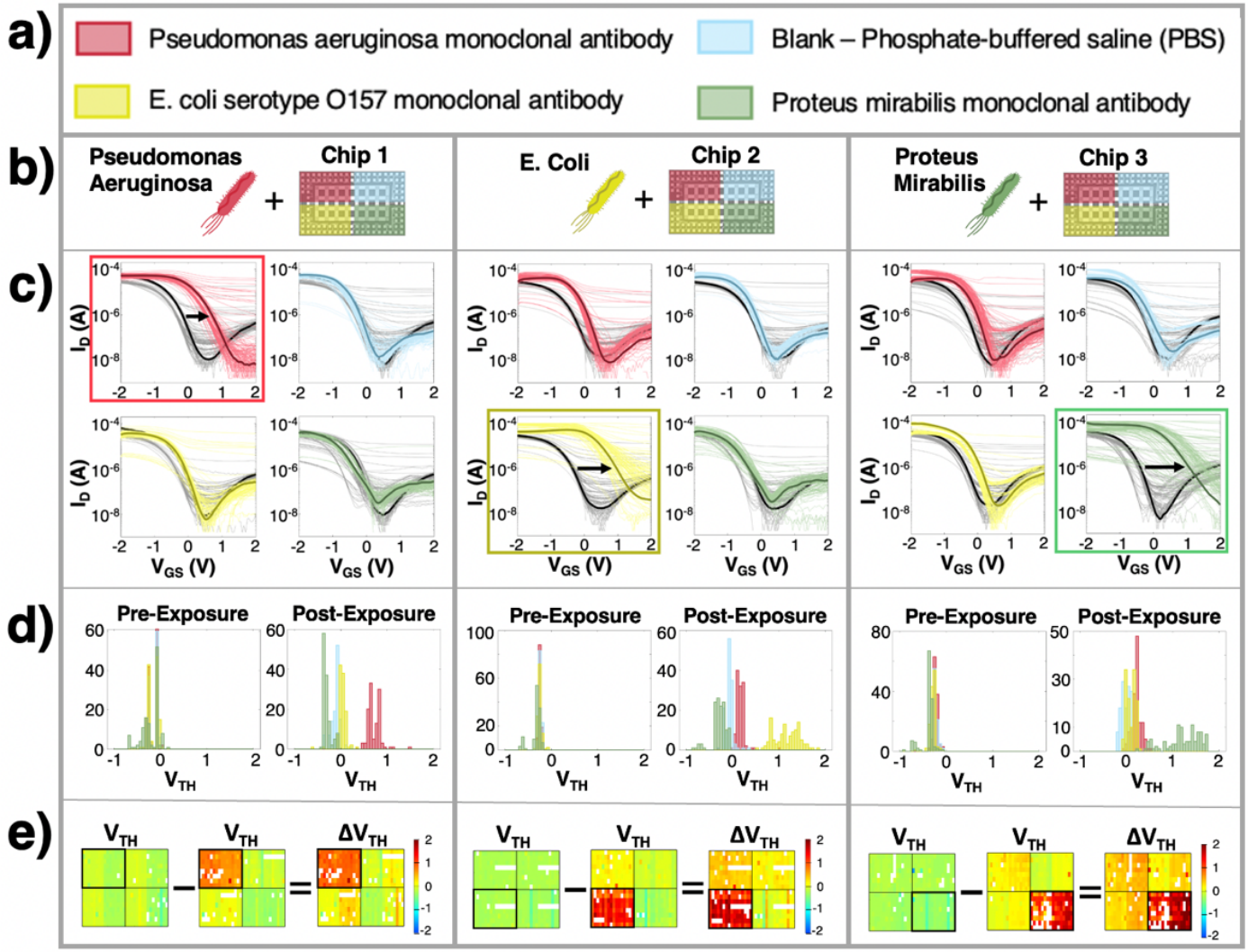

Figure 5.3. (a) Quadrant functionalization labels for chips in (b): testing setup for identifying 3 different pathogens with our BioSensor chips. Different chips are used for each experiment. Chips are colored to differentiate quadrants. Thus, each quadrant (e.g., color) represents a collection of 128 sensors all functionalized with the same antibody targeting the same bacteria. (c) I_D vs. V_{GS} characteristics of each chip before pathogen exposure (in black/gray) and post-exposure (in color), V_{DS}=-1.8V. Only the quadrant of the chip which has the matching antibody to the bacteria present exhibits a strong and statistically significant shift in I_D-V_{GS} characteristics, attributed to the antigen binding to the antibodies functionalizing the CNFETs. The effect of targeted antigen binding on sensor V_{TH} is illustrated in: (d) histograms of chip V_{TH} distributions, and (e) heatmaps of V_{TH} values and change across the entire chip, where each pixel represents one CNFET sensor (blank pixels represent broken sensors). Sensor quadrants are outlined for clarity.

Identification Blind Trials

Blind trials were conducted with additional Biosensor chips to test the platform's ability to identify unknown pathogens algorithmically, removing the risk of human error from pathogen exposure classification. The classification methodology is shown in Fig. 5.4a. Multiple experiments were used to characterize the V_{TH} change (ΔV_{TH}) after exposure when the pathogen is "absent" or "present." Ranges were established by finding the mean (μ) ± standard deviation (σ) of ΔV_{TH} for both "absent" and "present" conditions. The pathogen is considered present if the quadrant's $\mu \pm \sigma$ of ΔV_{TH} overlaps the "present" range and does not overlap the "absent" range, and vice versa. Quadrant classification is deemed "inconclusive" if $\mu \pm \sigma$ of ΔV_{TH} overlaps both or neither of the ranges. If any of the four quadrants are classified as inconclusive or multiple quadrants indicate pathogen presence, classification is unsuccessful.

In the blind trials, each chip is exposed to one of the pathogenic bacteria for which it is functionalized. The exposed pathogen is identified by calculating the $\mu \pm \sigma$ of ΔV_{TH} for each chip quadrant and applying the aforementioned methodology to determine if each quadrant's ΔV_{TH} range indicates pathogen presence, absence, or is inconclusive. The results of these experiments for 3 different chips are depicted in Fig. 5.4b-d. Although not used for classifying, scatter plots of each chip's ΔV_{TH} values organized by sensor functionalization are included to visualize the chips' response to pathogen exposure. In all cases the BioSensor chips are able to successfully detect and correctly identify the bacteria present.

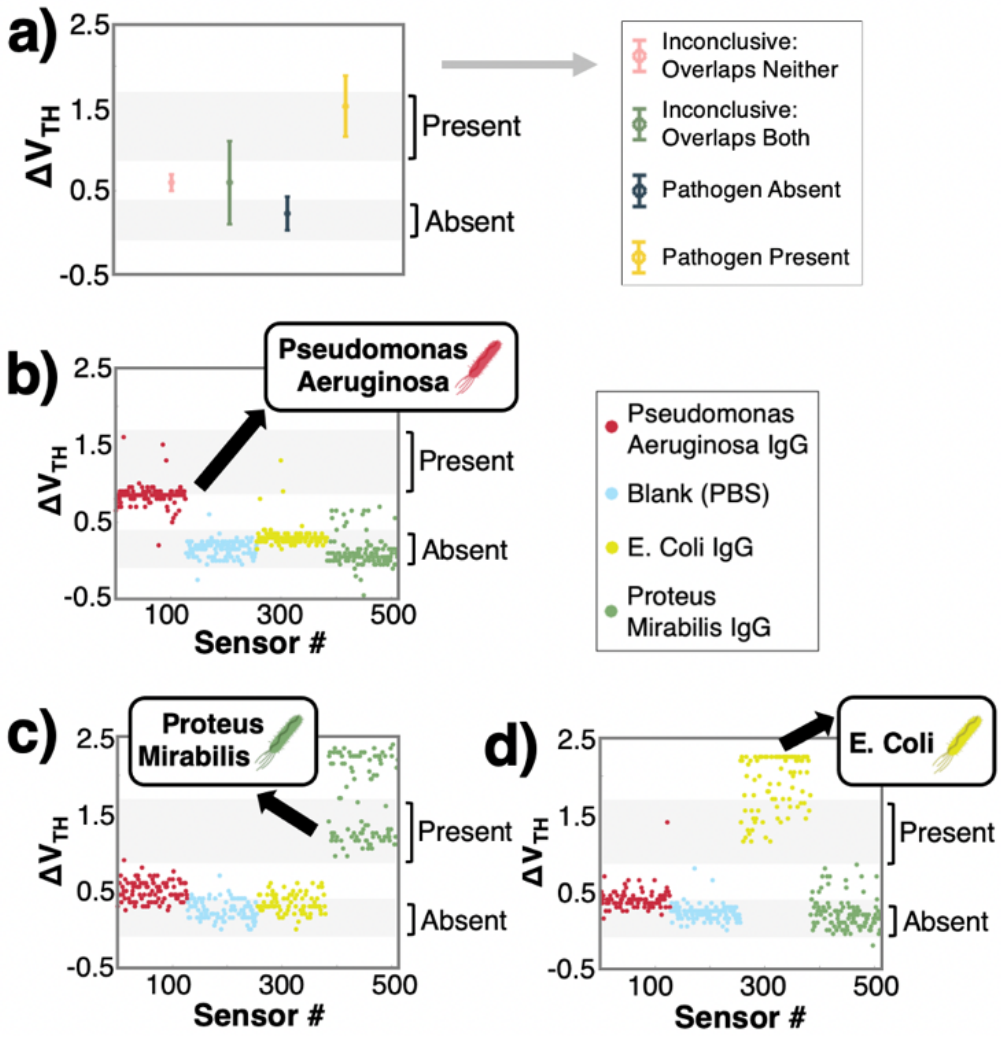

Figure 5.4. (a) Classification methodology for identifying pathogens using our BioSensor chips. Pathogen "absent" and "present" regions are defined as the mean (μ) ± standard deviation (σ) of ΔV_{TH} from multiple experiments, and the bars in this plot represent hypothetical μ±σ of ΔV_{TH} for each chip quadrant from an unknown exposure. If any quadrants are classified as inconclusive or multiple quadrants indicate bacteria presence, classification is unsuccessful. Results from successful blind trials using this methodology and scatter plots of each chip's ΔV_{TH} values, organized by sensor functionalization, are shown in: (b) chip #1, classified as Pseudomonas Aeruginosa, (c) chip #2, classified as Proteus Mirabilis, (d) and chip #3, classified as E. Coli.

Classification Accuracy vs. Scale

To demonstrate the importance of integrating many copies of identical sensors within a single chip, Monte Carlo simulations of chip pathogen classification were performed using different numbers of devices (Fig. 5.5). The number of sensors sampled (n) ranged from 2 to 128 per quadrant. 3000 simulations were run per sample size; for each simulation, classification was performed using n randomly selected sensors per quadrant. If the classification identified the wrong bacteria or was inconclusive, it was labeled unsuccessful. With the intended use of this technology being for a point-of-care setting, high accuracy is extremely important. Because of variations inherent to emerging nanotechnologies, antibody functionalization, and bacteria binding, integrating >95 sensors per functionalization is required to achieve >99.9% accuracy. This demonstrates the importance of the VLSI-compatible and wafer-scale fabrication of the CNFET-based biosensing technology.

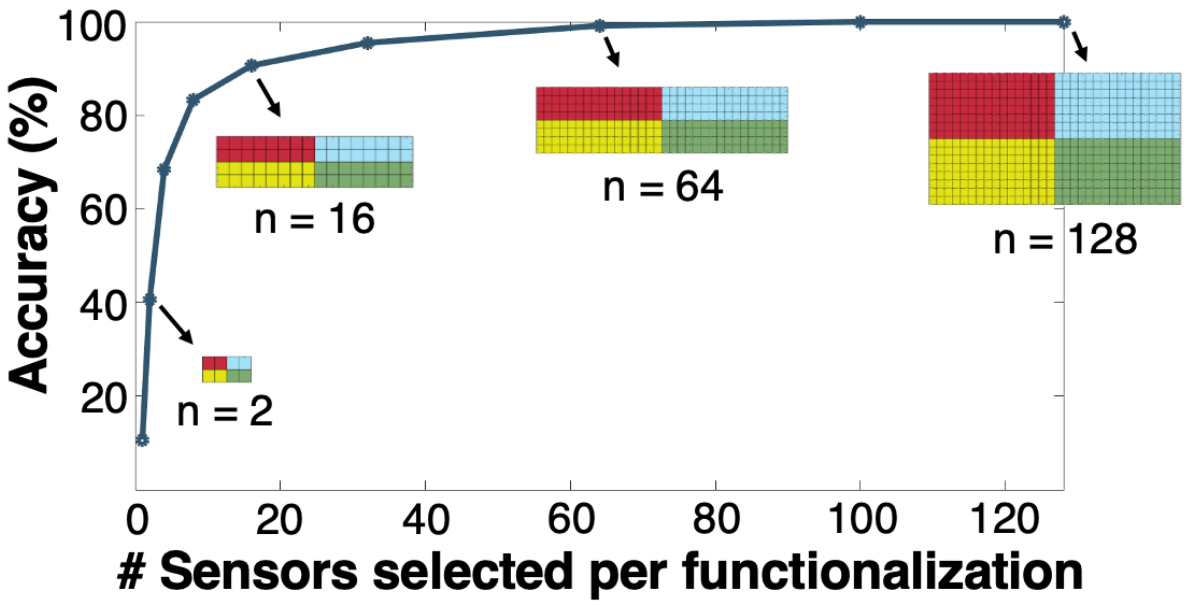

Figure 5.5. Effect of number of sensors on classification accuracy. Monte Carlo simulations of bacteria classification were performed using different sample sizes (*n*) of devices, sampled from experimentally measured chips. For each simulation, *n* devices per quadrant were randomly selected, and chip classification was recorded as either accurate or inaccurate/inconclusive. 3000 simulations were run per sample size and accuracy was averaged across runs. At n=64, classification accuracy is 99.1%. Accuracy of >99.9% is achieved when the number of sensors used per functionalization is >95.

5.5 Conclusion

We experimentally demonstrate a wafer-scale approach to integrating an emerging nanotechnology with a mature biosensing modality to create CNFET-antibody-based BioSensor chips that can perform clinically useful diagnostics. Their ability to accurately detect and identify pathogens is directly enabled by VLSI integration: by fabricating 100s of CNFET sensors on each chip, we show that through sensor redundancy this platform can overcome yield and variation issues inherent to emerging nanotechnologies and sensor processing. As a case-study, our CNFET BioSensor platform is used to detect and identify 3 different bacteria common to UTIs. However,

this platform is notably versatile, as it has the potential to be used for a variety of diseases simply by changing the antibodies functionalizing the CNFETs. With pathogen detection and identification being completed within 1 hour of sample acquisition, this work has the potential to improve patient care by reducing time to targeted treatment at the point of care.

Chapter 6:

Concluding Remarks

The rapid progression of technology over the past few decades has revolutionized all of our daily lives. In an age where we are connected more than ever and can access almost any information within seconds, it is hard to envision this progress ever coming to a halt. However, computing is currently facing serious challenges, including difficulty in continued scaling, diminishing returns in energy efficiency, bandwidth bottlenecks, and connectivity constraints. As the end of Moore's law becomes a greater reality, we are faced with a significant inflection point in technological development. In order to continue moving forward, we must look beyond what has worked in the past and begin to leverage less conventional materials and techniques.

Emerging nanotechnologies have shown great promise for future technology. As I demonstrate in this thesis, they can enable exciting new applications such as 3D circuit architectures, whereby device density and connectivity are significantly increased, and can be used to realize more sophisticated sensing platforms for healthcare applications. However, while nanomaterials have been the basis of academic research for decades, these technologies have yet to be proven commercially viable. This thesis uses CNTs as a case-study to propose an on-ramp for the adoption of emerging technologies into existing systems. We show advancement in state-of-the-art circuitry, successfully building the first analog and mixed-signal circuits built with CNFETs. By demonstrating the benefits and feasibility of building digital, analog, *and* mixed-signal circuits with CNFETs, we show a natural first step to integrating commercially fabricated CNFETs in circuits and systems today.

In order to realize the full benefits and applications of this technology, the adoption of CNFETs must be accompanied by further device characterization and optimization as well. *1/f* noise is still high in CNFETs compared to conventional silicon FETs, and continued research into optimized fabrication methods and circuit techniques is required to build high-performance CNFET-based analog and mixed-signal circuitry.

These advances across CNFET integration and device performance are essential for bringing CNT technology to a point of maturation in which novel application spaces can be realized outside of academic and research facilities. While emerging nanotechnologies provide hope of continuing Moore's law and advancements in computing, they also importantly provide real promise toward realizing new technologies *beyond* what is conventional today.

References

[Amer 2019] Amer, Aya G., Rebecca Ho, Gage Hills, Anantha P. Chandrakasan, and Max M. Shulaker. 2019. "29.8 SHARC: Self-Healing Analog with RRAM and CNFETs." In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, 470–72. IEEE.

[Appenzeller 2008] Appenzeller, J. 2008. "Carbon Nanotubes for High-Performance Electronics—Progress and Prospect." *Proceedings of the IEEE* 96 (2): 201–11. https://doi.org/10.1109/JPROC.2007.911051.

[Appenzeller 2007] Appenzeller, Joerg, Yu-Ming Lin, Joachim Knoch, Zhihong Chen, and Phaedon Avouris. 2007. "1/f Noise in Carbon Nanotube Devices—On the Impact of Contacts and Device Geometry." *IEEE Transactions on Nanotechnology* 6 (3): 368–73. https://doi.org/10.1109/TNANO.2007.892052.

[Banerjee 2001] Banerjee, K., S.J. Souri, P. Kapur, and K.C. Saraswat. 2001. "3-D ICs: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration." *Proceedings of the IEEE* 89 (5): 602–33. https://doi.org/10.1109/5.929647.

[Batude 2011] Batude, P., M. Vinet, B. Previtali, C. Tabone, C. Xu, J. Mazurier, O. Weber, et al. 2011. "Advances, Challenges and Opportunities in 3D CMOS Sequential Integration." In *2011 International Electron Devices Meeting*, 7.3.1-7.3.4. https://doi.org/10.1109/IEDM.2011.6131506.

[Bayer 1990] Bayer, Manfred E., and John L. Sloyer. 1990. "The Electrophoretic Mobility of Gram-Negative and Gram-Positive Bacteria: An Electrokinetic Analysis." *Microbiology* 136 (5): 867–74. https://doi.org/10.1099/00221287-136-5-867.

[Bhardwaj 2017] Bhardwaj, Jyoti, Sivaranjani Devarakonda, Suveen Kumar, and Jaesung Jang. 2017. "Development of a Paper-Based Electrochemical Immunosensor Using an Antibody-Single Walled Carbon Nanotubes Bio-Conjugate Modified Electrode for Label-Free Detection of Foodborne Pathogens." *Sensors and Actuators B: Chemical* 253 (December): 115–23. https://doi.org/10.1016/j.snb.2017.06.108.

[Bishop 2020] Bishop, Mindy D., Gage Hills, Tathagata Srimani, Christian Lau, Denis Murphy, Samuel Fuller, Jefford Humes, Anthony Ratkovich, Mark Nelson, and Max M. Shulaker. 2020. "Fabrication of Carbon Nanotube Field-Effect Transistors in Commercial Silicon Manufacturing

Facilities." *Nature Electronics* 3 (8): 492–501. https://doi.org/10.1038/s41928-020-0419-7.

[Bishop 2019] Bishop, Mindy D., H.-S. Philip Wong, Subhasish Mitra, and Max M. Shulaker. 2019. "Monolithic 3-D Integration." *IEEE Micro* 39 (6): 16–27. https://doi.org/10.1109/MM.2019.2942982.

[Chang 2014] Chang, Dong-Young, Carlos Muñoz, Denis Daly, Soon-Kyun Shin, Kevin Guay, Thomas Thurston, Hae-Seung Lee, Kush Gulati, and Matthew Straayer. 2014. "11.6 A 21mW 15b 48MS/s Zero-Crossing Pipeline ADC in 0.13µm CMOS with 74dB SNDR." In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 204–5. https://doi.org/10.1109/ISSCC.2014.6757401.

[Collins 2000] Collins, Philip G., M. S. Fuhrer, and A. Zettl. 2000. "1/f Noise in Carbon Nanotubes." *Applied Physics Letters* 76 (7): 894–96. https://doi.org/10.1063/1.125621.

[Dennard 1974] Dennard, Robert H., Fritz H. Gaensslen, V. Leo Rideout, Ernest Bassous, and Andre R. LeBlanc. 1974. "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions." *IEEE Journal of Solid-State Circuits* 9 (5): 256–68.

[Franklin 2012] Franklin, Aaron D., Mathieu Luisier, Shu-Jen Han, George Tulevski, Chris M. Breslin, Lynne Gignac, Mark S. Lundstrom, and Wilfried Haensch. 2012. "Sub-10 Nm Carbon Nanotube Transistor." *Nano Letters* 12 (2): 758–62. https://doi.org/10.1021/nl203701g.

[Geier 2015] Geier, Michael L., Julian J. McMorrow, Weichao Xu, Jian Zhu, Chris H. Kim, Tobin J. Marks, and Mark C. Hersam. 2015. "Solution-Processed Carbon Nanotube Thin-Film Complementary Static Random Access Memory." *Nature Nanotechnology* 10 (11): 944–48. https://doi.org/10.1038/nnano.2015.197.

[Gielen 2008] Gielen, G., P. De Wit, E. Maricau, J. Loeckx, J. Martín-Martínez, B. Kaczer, G. Groeseneken, R. Rodríguez, and M. Nafría. 2008. "Emerging Yield and Reliability Challenges in Nanometer CMOS Technologies." In *Proceedings of the Conference on Design, Automation and Test in*

Europe, 1322–27. DATE '08. New York, NY, USA: Association for Computing Machinery. https://doi.org/10.1145/1403375.1403694.

[Gulati 2001] Gulati, K., and Hae-Seung Lee. 2001. "A Low-Power Reconfigurable Analog-to-Digital Converter." *IEEE Journal of Solid-State Circuits* 36 (12): 1900–1911. https://doi.org/10.1109/4.972140.

[Ha 2015] Ha, Tae-Jun, Kevin Chen, Steven Chuang, Kin Man Yu, Daisuke Kiriya, and Ali Javey. 2015. "Highly Uniform and Stable N-Type Carbon Nanotube Transistors by Using Positively Charged Silicon Nitride Thin Films." *Nano Letters* 15 (1): 392–97. https://doi.org/10.1021/nl5037098.

[Han 2017] Han, Shu-Jen, Jianshi Tang, Bharat Kumar, Abram Falk, Damon Farmer, George Tulevski, Keith Jenkins, et al. 2017. "High-Speed Logic Integrated Circuits with Solution-Processed Self-Assembled Carbon Nanotubes." *Nature Nanotechnology* 12 (9): 861–65. https://doi.org/10.1038/nnano.2017.115.

[Hills 2018] Hills, Gage, Marie Garcia Bardon, Gerben Doornbos, Dmitry Yakimets, Pieter Schuddinck, Rogier Baert, Doyoung Jang, et al. 2018. "Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI." *IEEE Transactions on Nanotechnology* 17 (6): 1259–69. https://doi.org/10.1109/TNANO.2018.2871841.

[Hills 2015] Hills, Gage, Jie Zhang, Max Marcel Shulaker, Hai Wei, Chi-Shuen Lee, Arjun Balasingam, H.-S Philip Wong, and Subhasish Mitra. 2015. "Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 34 (7): 1082–95. https://doi.org/10.1109/TCAD.2015.2415492.

[Hills 2019] Hills, Gage, Christian Lau, Andrew Wright, Samuel Fuller, Mindy D. Bishop, Tathagata Srimani, Pritpal Kanhaiya, et al. 2019. "Modern Microprocessor Built from Complementary Carbon Nanotube Transistors." *Nature* 572 (7771): 595–602. https://doi.org/10.1038/s41586-019-1493-8.

[Hodges 2004] Hodges, David, Horace Jackson, and Resve Saleh. 2004. *Analysis and Design of Digital Integrated Circuits*. 3rd ed. New York, NY, USA: McGraw-Hill, Inc.

[Janousch 2007] Janousch, M., G. I. Meijer, U. Staub, B. Delley, S. F. Karg, and B. P. Andreasson. 2007. "Role of Oxygen Vacancies in Cr-Doped SrTiO3 for Resistance-Change Memory." *Advanced Materials* 19 (17): 2232–35. https://doi.org/10.1002/adma.200602915.

[Kabiri Ameri 2017] Kabiri Ameri, Shideh, Rebecca Ho, Hongwoo Jang, Li Tao, Youhua Wang, Liu Wang, David M. Schnyer, Deji Akinwande, and Nanshu Lu. 2017. "Graphene Electronic Tattoo Sensors." *ACS Nano* 11 (8): 7634–41. https://doi.org/10.1021/acsnano.7b02182.

[Karanicolas 1993] Karanicolas, A. N., Hae-Seung Lee, and K. L. Barcrania. 1993. "A 15-b 1-Msample/s Digitally Self-Calibrated Pipeline ADC." *IEEE Journal of Solid-State Circuits* 28 (12): 1207–15. https://doi.org/10.1109/4.261994.

[Kong 2000] Kong, Jing, Nathan R. Franklin, Chongwu Zhou, Michael G. Chapline, Shu Peng, Kyeongjae Cho, and Hongjie Dai. 2000. "Nanotube Molecular Wires as Chemical Sensors." *Science* 287 (5453): 622–25. https://doi.org/10.1126/science.287.5453.622.

[Kull 2018] Kull, Lukas, Danny Luu, Christian Menolfi, Matthias Brändli, Pier Andrea Francese, Thomas Morf, Marcel Kossel, Alessandro Cevrero, Ilter Ozkaya, and Thomas Toifl. 2018. "A 24–72-GS/s 8-b Time-Interleaved SAR ADC With 2.0–3.3-PJ/Conversion and >30 DB SNDR at Nyquist in 14-Nm CMOS FinFET." *IEEE Journal of Solid-State Circuits* 53 (12): 3508–16. https://doi.org/10.1109/JSSC.2018.2859757.

[Lau 2018] Lau, Christian, Tathagata Srimani, Mindy D. Bishop, Gage Hills, and Max M. Shulaker. 2018. "Tunable N-Type Doping of Carbon Nanotubes Through Engineered Atomic Layer Deposition HfOX Films." *ACS Nano*, October. https://doi.org/10.1021/acsnano.8b04208.

[Lee 2015] Lee, C.-, E. Pop, A. D. Franklin, W. Haensch, and H.- P. Wong. 2015. "A Compact Virtual-Source Model for Carbon Nanotube FETs in the Sub-10-Nm Regime—Part I: Intrinsic Elements." *IEEE Transactions on*

Electron Devices 62 (9): 3061–69. https://doi.org/10.1109/TED.2015.2457453.

[Lerner 2013] Lerner, Mitchell B., Jennifer Dailey, Brett R. Goldsmith, Dustin Brisson, and A. T. Charlie Johnson. 2013. "Detecting Lyme Disease Using Antibody-Functionalized Single-Walled Carbon Nanotube Transistors." *Biosensors and Bioelectronics* 45 (July): 163–67. https://doi.org/10.1016/j.bios.2013.01.035.

[Liang 2020] Liang, Yuqi, Mengmeng Xiao, Ding Wu, Yanxia Lin, Lijun Liu, Jianping He, Guojun Zhang, Lian-Mao Peng, and Zhiyong Zhang. 2020. "Wafer-Scale Uniform Carbon Nanotube Transistors for Ultrasensitive and Label-Free Detection of Disease Biomarkers." *ACS Nano* 14 (7): 8866–74. https://doi.org/10.1021/acsnano.0c03523.

[Liebmann 2016] Liebmann, Lars, Jia Zeng, Xuelian Zhu, Lei Yuan, Guillaume Bouche, and Jongwook Kye. 2016. "Overcoming Scaling Barriers through Design Technology CoOptimization." In *2016 IEEE Symposium on VLSI Technology*, 1–2. https://doi.org/10.1109/VLSIT.2016.7573398.

[Lin 2007] Lin, Yu-Ming, Joerg Appenzeller, Zhihong Chen, and Phaedon Avouris. 2007. "Electrical Transport and 1/f Noise in Semiconducting Carbon Nanotubes." *Physica E: Low-Dimensional Systems and Nanostructures* 37 (1): 72–77. https://doi.org/10.1016/j.physe.2006.07.008.

[Liu 2015] Liu, Sophie F., Lionel C. H. Moh, and Timothy M. Swager. 2015. "Single-Walled Carbon Nanotube–Metalloporphyrin Chemiresistive Gas Sensor Arrays for Volatile Organic Compounds." *Chemistry of Materials* 27 (10): 3560–63. https://doi.org/10.1021/acs.chemmater.5b00153.

[Miyahara 2013] Miyahara, Y., M. Sano, K. Koyama, T. Suzuki, K. Hamashita, and B. Song. 2013. "Adaptive Cancellation of Gain and Nonlinearity Errors in Pipelined ADCs." In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 282–83. https://doi.org/10.1109/ISSCC.2013.6487736.

[Moore 1965] Moore, Gordon E. 1965. "Cramming More Components onto Integrated Circuits." *Electronics* 38 (8).

[NanoIntegris] "NanoIntegris." n.d. Accessed December 21, 2018. http://nanointegris.com/.

[Nemirovsky 2011] Nemirovsky, Yael, Dan Corcos, Igor Brouk, Amikam Nemirovsky, and Samir Chaudhry. 2011. "1/f Noise in Advanced CMOS Transistors." *IEEE Instrumentation & Measurement Magazine* 14 (1): 14–22. https://doi.org/10.1109/MIM.2011.5704805.

[Panth 2013] Panth, Shreepad, Kambiz Samadi, Yang Du, and Sung Kyu Lim. 2013. "High-Density Integration of Functional Modules Using Monolithic 3D-IC Technology." In *2013 18th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 681–86. https://doi.org/10.1109/ASPDAC.2013.6509679.

[Parlak 2018] Parlak, Onur, Scott Tom Keene, Andrew Marais, Vincenzo F. Curto, and Alberto Salleo. 2018. "Molecularly Selective Nanoporous Membrane-Based Wearable Organic Electrochemical Device for Noninvasive Cortisol Sensing." *Science Advances* 4 (7): eaar2904.

[Rao 2001] C. Radhakrishna Rao. 2001. *Linear Statistical Inference and Its Applications, 2nd Edition*. Second edition. https://www.wiley.com/en-us/Linear+Statistical+Inference+and+its+Applications%2C+2nd+Edition-p-9780471218753.

[Razavi 2017] Razavi, Behzad. 2017. *Design of Analog CMOS Integrated Circuits*. Second edition. New York, NY: McGraw-Hill Education.

[Shahrjerdi 2013] Shahrjerdi, Davood, Aaron D. Franklin, Satoshi Oida, John A. Ott, George S. Tulevski, and Wilfried Haensch. 2013. "High-Performance Air-Stable n-Type Carbon Nanotube Transistors with Erbium Contacts." *ACS Nano* 7 (9): 8303–8. https://doi.org/10.1021/nn403935v.

[Shao 2021] Shao, Wenting, Michael R. Shurin, Sarah E. Wheeler, Xiaoyun He, and Alexander Star. 2021. "Rapid Detection of SARS-CoV-2 Antigens Using High-Purity Semiconducting Single-Walled Carbon Nanotube-Based Field-Effect Transistors." *ACS Applied Materials & Interfaces* 13 (8): 10321–27. https://doi.org/10.1021/acsami.0c22589.

[Shulaker 2014] Shulaker, M. M., J. Van Rethy, G. Hills, H. Wei, H. Chen, G. Gielen, H.-P. Wong, and S. Mitra. 2014. “Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs.” *IEEE Journal of Solid-State Circuits* 49 (1): 190–201. https://doi.org/10.1109/JSSC.2013.2282092.

[Shulaker 2013a] Shulaker, Max M., Gage Hills, Nishant Patil, Hai Wei, Hong-Yu Chen, H.-S. Philip Wong, and Subhasish Mitra. 2013. “Carbon Nanotube Computer.” *Nature* 501 (7468): 526–30. https://doi.org/10.1038/nature12502.

[Shulaker 2013b] Shulaker, M., J. Van Rethy, G. Hills, H. Chen, G. Gielen, H.- P. Wong, and S. Mitra. 2013. “Experimental Demonstration of a Fully Digital Capacitive Sensor Interface Built Entirely Using Carbon-Nanotube FETs.” In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, 112–13. https://doi.org/10.1109/ISSCC.2013.6487660.

[Shulaker 2017] Shulaker, Max M., Gage Hills, Rebecca S. Park, Roger T. Howe, Krishna Saraswat, H.-S. Philip Wong, and Subhasish Mitra. 2017. “Three-Dimensional Integration of Nanotechnologies for Computing and Data Storage on a Single Chip.” *Nature* 547 (7661): 74–78. https://doi.org/10.1038/nature22994.

[Suriyasena 2014] Suriyasena Liyanage, Luckshitha, Xiaoqing Xu, Greg Pitner, Zhenan Bao, and H.-S. Philip Wong. 2014. “VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-Function Metal Oxides.” *Nano Letters* 14 (4): 1884–90. https://doi.org/10.1021/nl404654j.

[Sze 2020] Sze, Vivienne, Yu-Hsin Chen, Tien-Ju Yang, and Joel S. Emer. 2020. “Advanced Technologies.” In *Efficient Processing of Deep Neural Networks*, edited by Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, and Joel S. Emer, 253–80. Synthesis Lectures on Computer Architecture. Cham: Springer International Publishing. https://doi.org/10.1007/978-3-031-01766-7_10.

[Tang 2018] Tang, Jianshi, Qing Cao, George Tulevski, Keith A. Jenkins, Luca Nela, Damon B. Farmer, and Shu-Jen Han. 2018. “Flexible CMOS Integrated Circuits Based on Carbon Nanotubes with Sub-10 Ns Stage Delays.” *Nature Electronics* 1 (3): 191–96. https://doi.org/10.1038/s41928-018-0038-8.

[Tulevski 2014] Tulevski, George S., Aaron D. Franklin, David Frank, Jose M. Lobez, Qing Cao, Hongsik Park, Ali Afzali, Shu-Jen Han, James B. Hannon, and Wilfried Haensch. 2014. “Toward High-Performance Digital Logic Technology with Carbon Nanotubes.” *ACS Nano* 8 (9): 8730–45. https://doi.org/10.1021/nn503627h.

[Villa 2014] Villa, Oreste, Daniel R. Johnson, Mike Oconnor, Evgeny Bolotin, David Nellans, Justin Luitjens, Nikolai Sakharnykh, et al. 2014. “Scaling the Power Wall: A Path to Exascale.” In *SC ’14: Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis*, 830–41. https://doi.org/10.1109/SC.2014.73.

[Weste 2010] Weste, Neil, and David Harris. 2010. *CMOS VLSI Design: A Circuits and Systems Perspective*. 4th ed. USA: Addison-Wesley Publishing Company.

[Wong 2012] Wong, H.-S. Philip, Heng-Yuan Lee, Shimeng Yu, Yu-Sheng Chen, Yi Wu, Pang-Shiu Chen, Byoungil Lee, Frederick T. Chen, and Ming-Jinn Tsai. 2012. “Metal–Oxide RRAM.” *Proceedings of the IEEE* 100 (6): 1951–70. https://doi.org/10.1109/JPROC.2012.2190369.

[Wu 2020] Wu, Yuhao, Yaofeng Zhou, Yuankui Leng, Weihua Lai, Xiaolin Huang, and Yonghua Xiong. 2020. “Emerging Design Strategies for Constructing Multiplex Lateral Flow Test Strip Sensors.” *Biosensors and Bioelectronics* 157 (June): 112168. https://doi.org/10.1016/j.bios.2020.112168.

[Wulf 1995] Wulf, Wm. A., and Sally A. McKee. 1995. “Hitting the Memory Wall: Implications of the Obvious.” *ACM SIGARCH Computer Architecture News* 23 (1): 20–24. https://doi.org/10.1145/216585.216588.

[Yang 2017] Yang, Yingjun, Li Ding, Jie Han, Zhiyong Zhang, and Lian-Mao Peng. 2017. “High-Performance Complementary Transistors and Medium-Scale Integrated Circuits Based on Carbon Nanotube Thin Films.” *ACS Nano* 11 (4): 4124–32. https://doi.org/10.1021/acsnano.7b00861.

[Zhang 2018] Zhang, Heng, Li Xiang, Yingjun Yang, Mengmeng Xiao, Jie Han, Li Ding, Zhiyong Zhang, Youfan Hu, and Lian-Mao Peng. 2018. “High-Performance Carbon Nanotube Complementary Electronics and Integrated Sensor Systems on Ultrathin Plastic Foil.” *ACS Nano* 12 (3): 2773–79. https://doi.org/10.1021/acsnano.7b09145.

[Zhang 2011] Zhang, Jialu, Chuan Wang, Yue Fu, Yuchi Che, and Chongwu Zhou. 2011. “Air-Stable Conversion of Separated Carbon Nanotube Thin-Film Transistors from p-Type to n-Type Using Atomic Layer Deposition of High-κ Oxide and Its Application in CMOS Logic Circuits.” *ACS Nano* 5 (4): 3284–92. https://doi.org/10.1021/nn2004298.

[Zhang 2009] Jie Zhang, N.P. Patil, and S. Mitra. 2009. “Probabilistic Analysis and Design of Metallic-Carbon-Nanotube-Tolerant Digital Logic Circuits.” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 28 (9): 1307–20. https://doi.org/10.1109/TCAD.2009.2023197.

[Zhang 2006] Zhang, Ting, Megan B. Nix, Bong-Young Yoo, Marc A. Deshusses, and Nosang V. Myung. 2006. “Electrochemically Functionalized Single-Walled Carbon Nanotube Gas Sensor.” *Electroanalysis* 18 (12): 1153–58. https://doi.org/10.1002/elan.200603527.

[Zheng 2005] Zheng, Gengfeng, Fernando Patolsky, Yi Cui, Wayne U. Wang, and Charles M. Lieber. 2005. “Multiplexed Electrical Detection of Cancer Markers with Nanowire Sensor Arrays.” *Nature Biotechnology* 23 (10): 1294–1301. https://doi.org/10.1038/nbt1138.