Power FETs in Switching Applications

by

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Abstract

A three-phase, mosfet inverter motor drive was designed and constructed to meet the requirements of a two-horsepower, size-constrained application. Paralleled power mosfets were successfully employed to provide circuit operation at currents greater than the capability of a single mosfet. The performance of the mosfet design was compared to that of a relatively conventional bipolar circuit, designed for the same application.

The power mosfet design was shown to have significant advantages over the bipolar design in terms of size. The mosfet design was twenty per cent smaller in size than the bipolar design. This very significant size advantage was achieved without penalties in the areas of cost or efficiencies. While the mosfet and bipolar designs were seen to have different efficiency profiles over a range of operating conditions, the overall efficiencies were found to be very similar - typically around 92%. Although cost was not regarded as a significant constraint in either design, it was shown that the cost of a mosfet design is not significantly worse than that of a bipolar design and may in fact be better. The relative reliability of the two circuits was impossible to compare because of the limited design experience with power mosfets.

Thesis Supervisor: Dr. John G. Kassakian

Title: Associate Professor of Electrical Engineering

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1. Introduction

The recent emergence of power mosfets [1,2,3] has given the circuit designer new options when designing power circuits. The traditional choice between power bipolar transistors and thyristors must be extended to include power mosfets. This is a significant extension of options as the characteristics and circuitry behavior of these new devices is substantially different from those of either of the other alternatives.

Currently, interest in the use of power mosfets seems to focus primarily on their high switching speed. This characteristic has been used to advantage in the design of high frequency switching regulators and other high speed circuits [4,5]. There is another substantial advantage of power mosfets - simplicity of drive. Because they are voltage-controlled devices requiring virtually no input current, the drive stage has to provide much less power than in conventional bipolar designs. Voltage drive waveforms are also in general much easier to synthesize then current drive waveforms. These two advantages should result in much simpler circuitry for designs employing power mosfets.

The following is a comparison of a conventional bipolar design and a power mosfet design for an inverter motor drive in a size-constrained application. The development of the mosfet design is described and the resulting design is compared with a conventional bipolar design in the areas of size, efficiency, cost and reliability.

1.1 Application

A need for a low-volume, light-weight inverter motor drive prompted this examination of power mosfet switching circuits as an alternative to conventional bipolar switching circuits in size-constrained, medium-power applications. The motor to be driven is a three-phase, two-horsepower, induction motor. This motor drives a pump, and the pumping application requires that minimum size and weight be primary design goals.

The power for the motor will come from a battery which will provide a stiff voltage source with low internal impedance. The battery voltage will vary between 300 and 50 volts during the pump operation.

During normal operation the motor drive will operate with a bus voltage of between 300 and 150 volts and provide a three-phase, 400 Hz drive to the motor. The fundamental component of the motor line-line voltage will be maintained at 100 Vrms and the normal line current will be 9.5 Arms at a rated load of 1645 watts. The fundamental component of the line-line voltage will be maintained at 100 Vrms by means of pulse width modulation. The pulse width modulation will be done at nine times the drive frequency using the subharmonic scheme [6].

When the bus voltage drops below 150 volts, it is no longer possible to maintain the motor line-line voltage at 100 Vrms, so the line-line voltage is allowed to drop linearly with the bus voltage. The frequency is also dropped linearly, maintaining constant volts/Hz to maintain the power delivered to the load. Variable frequency

drive is also provided to allow controlled start up and shut down. The drive frequency is allowed to range from 40 Hz to 400 Hz. Because the pulse width modulation provides between one and nine chops per cycle depending on the bus voltage, the switching frequency can vary from 40 Hz to 3600 Hz. A current limit is also provided at 16 amperes which will be allowed to chop at frequencies up to 10 kHz.

In summary the requirements of the switching stage are: it will operate with bus voltages between 50 and 300 volts, it will operate at switching speeds between 40 Hz and 10 kHz, and it will switch currents as large as 16 amperes. This is to be accomplished primarily with minimum size and as much as possible with maximum efficiency and minimum cost.

2. The Power Mosfet

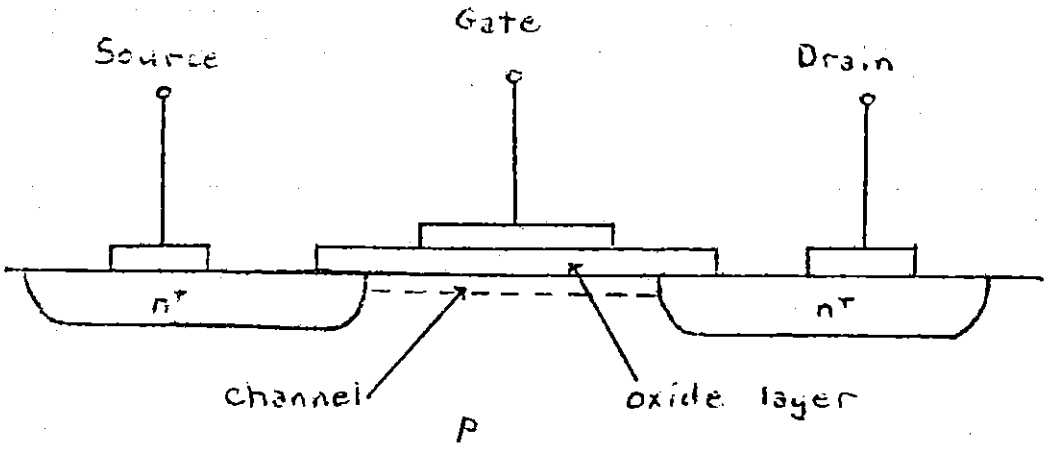
Until recently field-effect transistors were used exclusively in small-signal, low-current applications. Recent advances in technology have extended their use into the power field. Devices are now available with current ratings as high as 70 amperes and voltage ratings as high as 500 volts.

2.1 Mosfet Device Physics

Lower power mosfets typically use a lateral structure as shown in Fig. 1. The forward conductivity of the device is changes by modulating the conductivity of the channel electrostatically by means of the gate. The gate is electrically isolated from the channel by a thin, insulating, oxide layer. The voltage applied between the gate and the source changes the effective doping of the channel region which changes the forward drain-source resistance of the device.

Two major problems prevented the use of this structure as a power device. In order to conduct large currents the channel resistance must be very low to minimize device power dissipation. To do this the channel must be made very short. Initially, photolithography could not produce short enough channels. The second problem was the need to include a thick, lightly-doped N region in the current path. This region would provide the much larger breakdown voltage necessary for a power device. To insert this region in the lateral structure would require a large amount of chip area and make the device prohibitively large. A structure with vertical current flow was needed to allow this layer to be included beneath the surface of the device where it would not

Fig. 1. LMOS Mosfet Structure



take up valuable chip area. An additional advantage of a structure with vertical current flow, is that the drain and source contacts are on opposite sides of the wafer. This allows the use of even less area for a device with a given current rating.

The first commercial devices to overcome these problems were developed by Siliconix and had a V-groove structure (VMOS) as shown in Fig. 2. The problem of obtaining a short channel is solved by first etching V-grooves in the silicon wafer. The slope of the sides of the groove is fixed by the crystalline structure of silicon. The channel length is controlled by the difference in the diffusion depths of the N^+ and P layers. The difference between diffusion depths could be controlled more accurately than the width of surface structures. This structure also allowed vertical current flow and hence the subsurface, horizontal N_{epi} layer necessary for a higher voltage rating.

The other structure currently being used to produce power mosfet devices is the double-diffused structure (DMOS) shown in Fig. 3. This structure is something of a cross between the VMOS and LMOS structures. Improved photolithographic techniques have allowed the channel to be created on the surface as in the LMOS structure. The vertical current flow and the inclusion of the N_{epi} layer is accomplished as in the VMOS structure. Currently, DMOS allows somewhat higher packing densities and hence higher current devices. International Rectifier is the leading supplier of DMOS mosfets with their HEXFET® line.

Fig. 2. VMOS Mosfet Structure

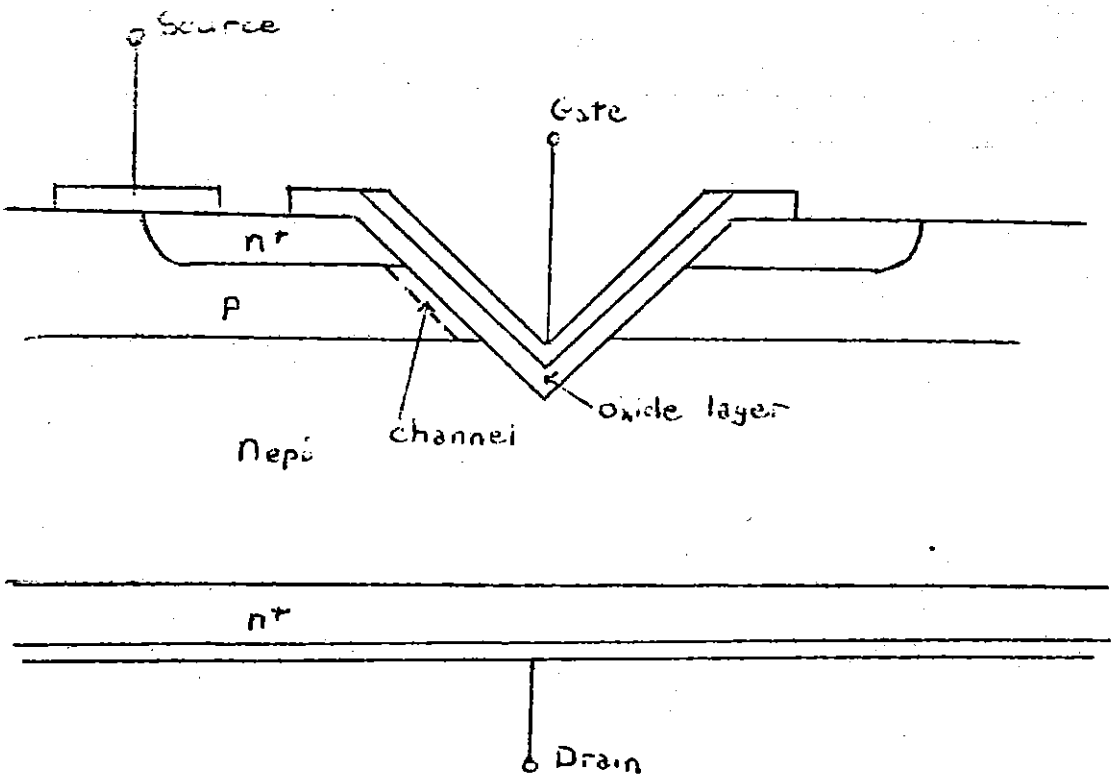
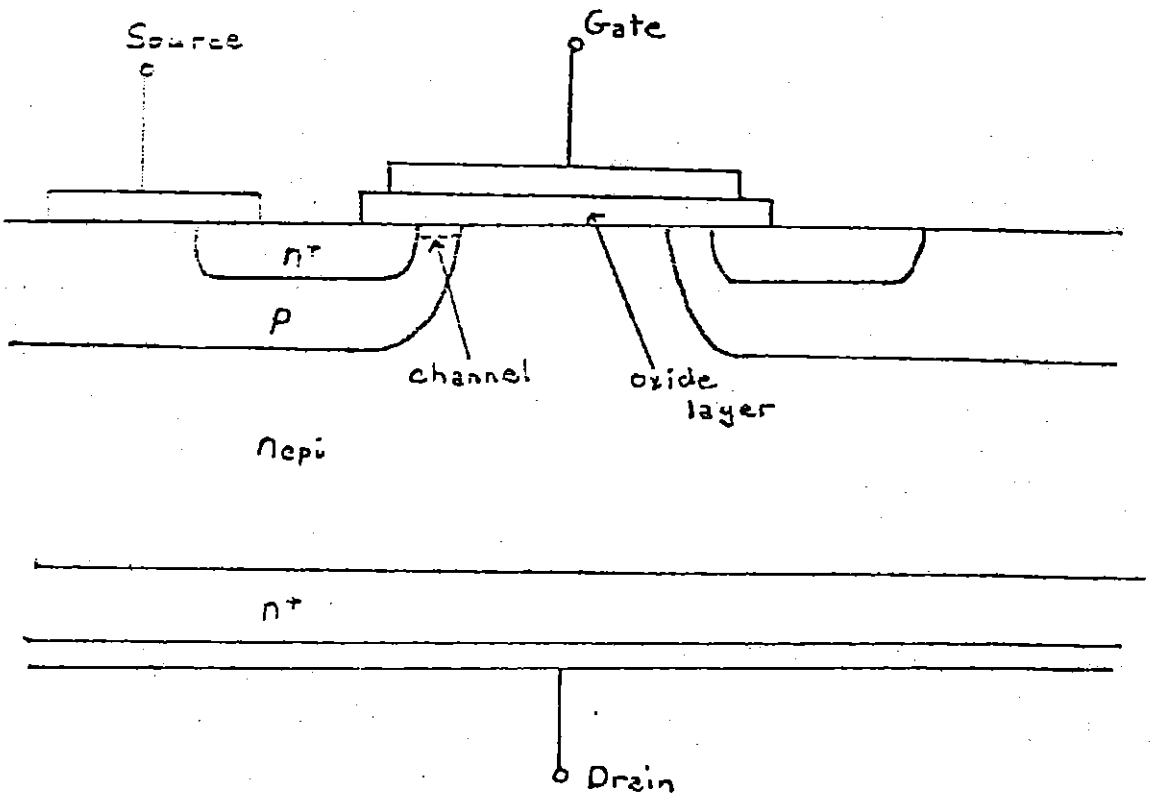


Fig. 3. DMOS Mosfet Structure

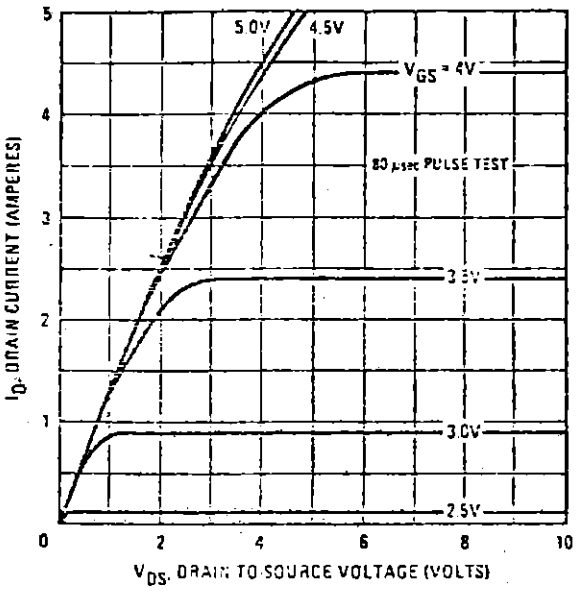


Inherent in each of the structures are parasitic elements. As can be seen from the diagrams, a NPN sequence of layers exists in the devices. It is possible under some circumstances to inject current into the P region and cause transistor action. More significant is the reverse diode formed by the P layer - N_{epi} layer junction. This diode allows reverse current flow from source to drain. This diode precludes the use of a single mosfet as an ac switch. The circuit behavior of these parasitic elements will be discussed in the next section.

2.2 Mosfet Circuit Behavior

Despite the difference in construction technologies, the terminal characteristics of DMOS mosfets and VMOS mosfets are virtually identical. The static output characteristics of a typical power mosfet are shown in Fig. 4. At any given gate voltage their are two main regions of operation. The first region is the constant resistance region. In this region the drain current is determined chiefly by the drain to source voltage. The second region is the constant current region. In this region the mosfet behaves as a constant current source. This results because electron velocity saturation in the channel prevent additional current from flowing. One should be careful not to confuse this use of the term saturation with its use when referring to bipolar transistors. In bipolar transistors saturation refers to the low voltage-drop, fully on condition, while in mosfets it refers to the high voltage-drop linear region. The slope of the V_{GS} - I_D curve in the constant resistance region is the "on resistance" of the device. This is an important parameter in power applications as it determines the on-state voltage-drop and power-loss in the mosfet.

Fig. 4. Power Mosfet Static Operating Characteristics



The static gate voltage versus drain current curve for a typical power mosfet is shown in Fig. 5. This curve reveals another significant characteristic of a mosfet - the gate threshold voltage $V_{GS}(th)$. Below this threshold voltage only the drain-source leakage current, I_{DSS}, flows. This current is relatively small, typically less than a milliampere. Above this voltage the relationship of gate voltage to drain current is initially a square law relationship which changes quickly to a linear relationship. This behavior can also be seen in the transconductance, g_{fs}, versus gate voltage curve (Fig. 6). The transconductance of a mosfet is the ratio of drain current to gate voltage and is the analogue of the beta of a bipolar transistor. As can be seen from the curve, the power mosfet exhibits a nearly constant transconductance over a wide range of drain currents. This feature is useful when power mosfets are used in linear circuits. The current gain of a power mosfet is essentially infinite. It is limited only by the gate leakage, I_{GSS}, which is typically on the order of nanoamperes.

The dynamic behavior of power mosfets is dominated by the interterminal capacitances. Because power mosfets are majority carrier devices their switching times are not limited by the minority carrier storage delay times seen in bipolar transistors. The primary limitation of switching speed is the speed at which the input capacitance, C_{iss}, can be charged and discharged. This allows the circuit designer to control switching speeds rather than the transistor designer as is the case in bipolar transistors. Using currently available power mosfets with relatively simple low-impedance drive circuits, switching speeds of a few tens of nanoseconds can readily be obtained. The gate to source or reverse transfer capacitance, C_{rss}, can greatly increase switching times,

Fig. 5. Power Mosfet Transfer Characteristics

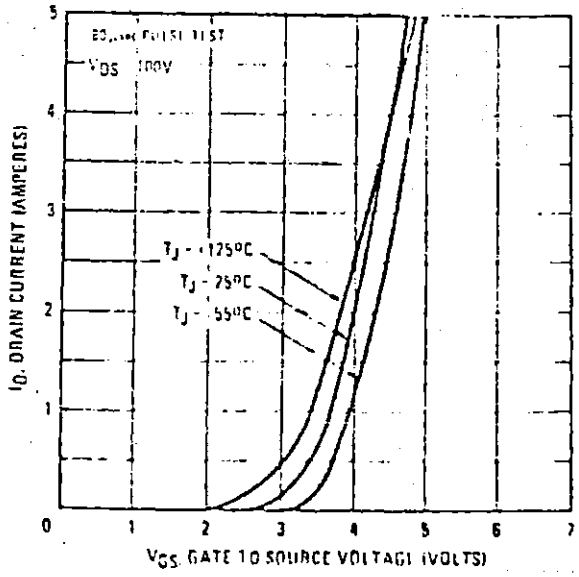
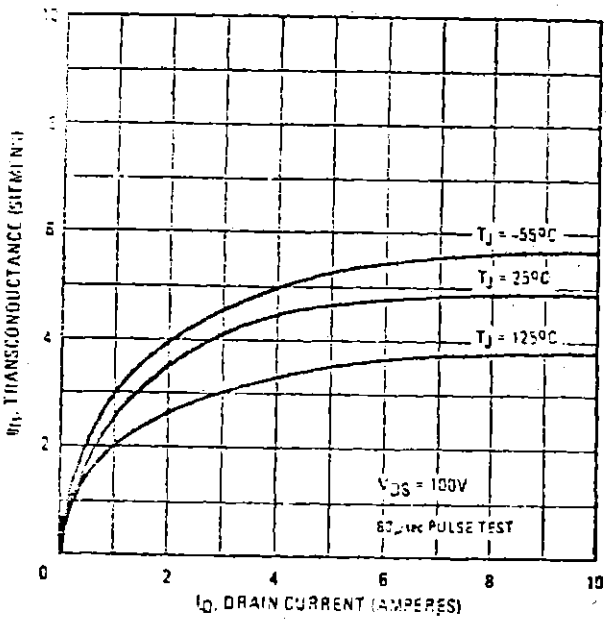


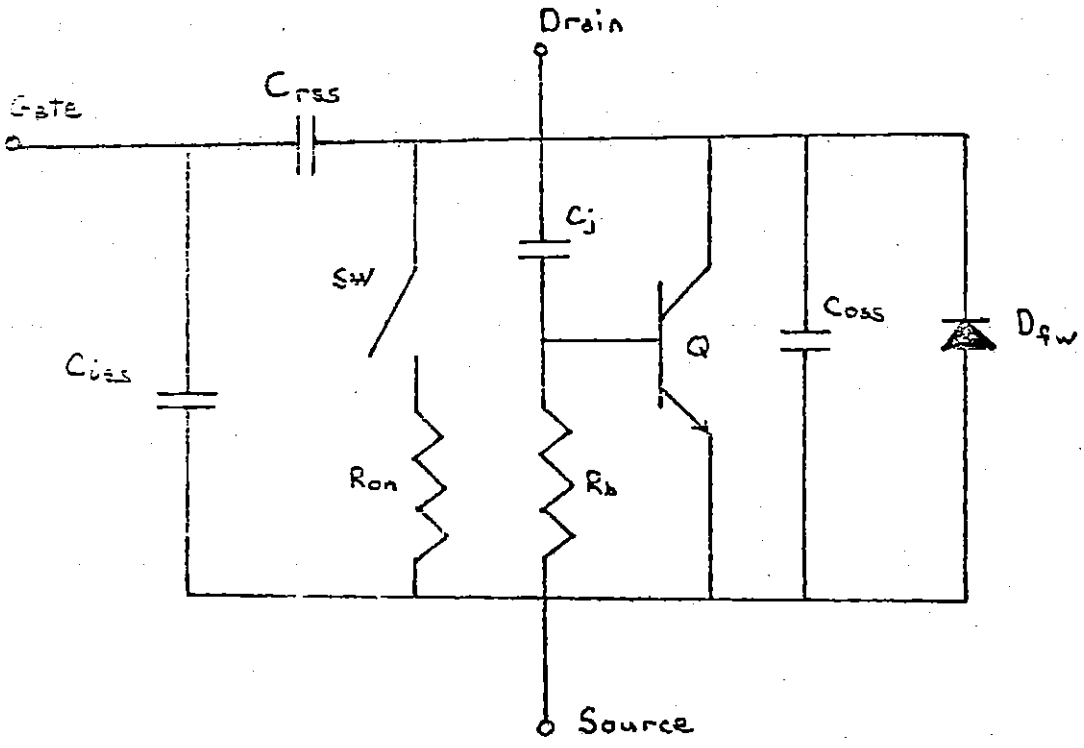
Fig. 6. Power Mosfet Transconductance Curves



acting as a Miller capacitance. The output capacitance, C_{oss}, can also be important in circuit behavior.

A circuit model of the mosfet which is useful for the analysis of switching circuits can be developed from the above discussion of terminal behavior and device physics (Fig. 7). This model consists of the interterminal capacitances, a switch, the "on" resistance and the parasitic diode and transistor mentioned previously. The resistor, R_b, from the base to the emitter of the transistor represents the spreading resistance of the P region and the capacitor, C_j, represents the P layer - N_{epi} layer junction capacitance. It can be seen that large slew rates of drain to source voltage can turn on the transistor. This causes current tails during switching and was observed in the testing of early devices. Recent designs seem to be much more immune to this behavior, and no transistor effects have been seen with drain to source voltage slew rates as high as 20,000 v/μs. The other parasitic component is the reverse "free wheeling" diode. Although the use of this diode in a circuit can save a part in some circuits, in many circuits the bad reverse recovery characteristics of this diode can lead to trouble. International Rectifier parts have shown reverse recoveries lasting several hundred nanoseconds and peak recovery currents as large as several times the forward current [7]. This diode can be designed out of the circuit by paralleling the mosfet with a diode having a lower forward drop and better reverse recovery characteristics. Because diodes with good reverse recovery characteristics typically have large forward drops, this is usually impossible. It is usually then necessary to block the mosfet internal diode with an additional series diode.

Fig. 7. Power Mosfet Circuit Model



The variation of characteristics with temperature can cause significant problems in power devices as they must operate over wide extremes of temperature. Power mosfets, however, are not greatly affected by temperature. The primary effect is that the on-resistance increases with temperature at the rate of approximately 0.7%/ ^{o}C. This positive temperature coefficient is responsible for the lack of secondary breakdown in power mosfets. It prevents the localized current hogging which leads to secondary breakdown in bipolar transistors. If a small area conducts more than its share of current the area heats up which results in a localized increase in resistance and hence a decrease in current. This temperature coefficient also has its disadvantages. If a power mosfet is inadequately heat sunk thermal runaway can occur. An increase in temperature will cause an increase in resistance which in turn causes an increase in power dissipation raising the temperature still more. The threshold voltage and transconductance are also slight functions of temperature.

Two other important parameters of a power mosfet are gate to source breakdown voltage, V_{GSS}, and drain to source breakdown voltage, V_{DSS}. Gate to source breakdown voltages are typically about 40 volts. Gate to source overvoltage results in a rapid degradation of the gate oxide layer. Initially this causes high gate leakage which will quickly degrade to a near short condition between gate and both drain and source. Circuits should incorporate some kind of protection from this breakdown and several mosfets come with internal zener diodes. Drain to source breakdown is less catastrophic and is essentially the same as reverse breakdown in power diodes. As long as the breakdown is not sustained and the power input is not excessive, permanent

damage will not occur.

Another failure mode is slow gate threshold voltage drift caused by residual ions in the gate oxide layer. Occasionally positive ions such as sodium may reside in the gate oxide after manufacture. A time-average positive gate voltage will cause these ions to slowly drift into the channel where they slowly change the doping level. This results in a slow reduction in the gate threshold voltage. Eventually a state may be reached where the mosfet cannot be turned off. Although this problem was observed in a few early samples, better process control seems to have eliminated this problem in currently available mosfets.

2.3 Comparison of Mosfet and Bipolar Transistors

Now that the major characteristics of power mosfets have been described it is useful to compare them with those of power bipolar transistors. Because of the fundamentally different operating principles there are several major differences between the two types of power transistors. Perhaps the most fundamental difference between mosfets and bipolar transistors is that the former are voltage controlled devices while the latter are current controlled devices. This can result in much simpler drive circuitry for the mosfets since voltage signals are in general easier to produce than current signals. The mosfet also has very low drive power since the device has virtually no input current.

A second major difference is that the mosfet is a majority carrier device while the bipolar transistor is a minority carrier device. This allows the mosfet to escape the problems of minority carrier storage delay time and hence generally allows much faster switching times. This allows a large reduction in switching losses or much higher practical switching speeds.

The efficiency gains resulting from low drive power and reduced switching losses are at least partially mitigated by the relatively large "on" state losses of power mosfets. When fully "on" a mosfet appears to the circuit as a resistor while a bipolar transistor appears as a voltage source with a relatively constant magnitude equal to the transistor's saturation voltage. As the current is increased, the mosfet "on" losses increase as the square of current while losses in the bipolar transistor increase only linearly with current. This generally results in larger "on" state losses for power mosfets as compared with bipolar transistors.

The last major difference between mosfets and bipolar transistors is their behavior over a range of temperatures. The "on" state resistance of a mosfet has a positive temperature coefficient while that of a bipolar transistor has a negative coefficient. This positive temperature coefficient in mosfets insures a relatively uniform current distribution, eliminating the possibility of "hot spot" formation which occurs in bipolar transistors and which can lead to secondary breakdown. This also means that mosfets inherently current share when paralleled. This eliminates the need for ballast resistors or careful parameter matching that is necessary when bipolar transistors are paralleled. The switching speeds of mosfets are also not affected by

temperature in contrast to bipolar transistors.

2.4 Currently Available Mosfets

The recent emergence of the power mosfet technology has been accompanied with a proliferation of product announcements. A summary of some of the currently available parts and their specifications is contained in Table 1.

Several things can be seen from Table 1. First of all there is currently available a wide variety of power mosfets from several manufacturers. Two manufacturers, Hitachi and Supertex, have announced complementary N and P channel devices. Because the P channel devices were impossible to obtain complementary circuits will not be considered in the following section. The three most important parameters for determining the performance of power mosfets in switching applications are drain to source breakdown voltage, "on" resistance, and input capacitance. A fairly typical device is one having a drain to source breakdown voltage of 400 volts, an "on" resistance of one ohm, and an input capacitance of about 1000 pF. Since a device of this type is made by three manufacturers, International Rectifier (IRF330), Siliconix (VN40000A), and Supertex (VN0450), it is a useful means of comparing manufacturers product lines. The differences in current ratings for these three devices appear to result from two factors - the packaging details for each manufacturer and their courage in specifying their parts. When sizing power mosfets for peak currents it is probably more useful to calculate power dissipation and use the manufacturer's thermal ratings to determine safety than to use the manufacturer's peak current specifications. Each of

the three manufacturers currently offers a significant advantage over the other two. International Rectifier offers by far the broadest product line, Supertex offers the most complete packaging line (TO-3, TO-39, TO-220, dice, and DIP packages), and Siliconix offers the lowest prices. Siliconix also seems to have the best thermal packaging. The Siliconix process also results in somewhat higher gate threshold voltages, which may or may not be an advantage in a given application.

Table I. Currently Available Power Mosfets

Part	IRF330	IRF331	IRF332	IRF333	IRF350	IRF351	IRF352
Source	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect
Process	DMOS	DMOS	DMOS	DMOS	DMOS	DMOS	DMOS
BV_{DSS}	400V	350V	400V	350V	400V	350V	400V
BV_{GSS}	±20V	±20V	±20V	±20V	±20V	±20V	±20V
I_{DSS}	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA
$I_D(cont)$	4.0A	4.0A	3.5A	3.5A	11A	11A	10A
$I_D(peak)$	8.0A	8.0A	7.0A	7.0A	25A	25A	20A
$R_{DS}(on)$	1.0Ω	1.0Ω	1.5Ω	1.5Ω	0.3Ω	0.3Ω	0.4Ω
$V_{GS}(th)$	1-3V	1-3V	1-3V	1-3V	1-3V	1-3V	1-3V
I_{GSS}	100nA	100nA	100nA	100nA	100nA	100nA	100nA
C_{iss}	1000pF	1000pF	1000pF	1000pF	4000pF	4000pF	4000pF
C_{oss}	300pF	300pF	300pF	300pF	600pF	300pF	300pF
C_{rss}	20pF	20pF	20pF	20pF	200pF	200pF	200pF
$R_{\theta JC}$	1.66°C/W	1.66°C/W	1.66°C/W	1.66°C/W	0.83°C/W	0.83°C/W	0.83°C/W
Cost	$28	$24	$26	$22	$85	$75	$80

Table II. Currently Available Power Mosfets (cont.)

Part	**IRF353**	**IRF430**	**IRF431**	**IRF432**	**IRF433**	**IRF230**	**IRF150**
Source	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect	Int Rect
Process	DMOS	DMOS	DMOS	DMOS	DMOS	DMOS	DMOS
BV_{DSS}	350V	500V	450V	500V	450V	200V	100V
BV_{GSS}	±20V	±20V	±20V	±20V	±20V	±20V	±20V
I_{DSS}	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA	1.0mA
$I_D(cont)$	10A	3.5A	3.5A	3.0A	3.0A	7.0A	28A
$I_D(peak)$	20A	7.0A	7.0A	6.0A	6.0A	15A	70A
$R_{DS}(on)$	0.4Ω	1.5Ω	1.5Ω	2.0Ω	2.0Ω	0.4Ω	0.055Ω
$V_{GS}(th)$	1-3V	1.5-3.5V	1.5-3.5V	1.5-3.5V	1.5-3.5V	1.5-3.5V	1.5-3.5V
I_{GSS}	100nA	100nA	100nA	100nA	100nA	100nA	100nA
C_{iss}	4000pF	900pF	900pF	900pF	900pF	1000pF	4000pF
C_{oss}	600pF	200pF	200pF	200pF	200pF	450pF	1500pF
C_{rss}	200pF	60pF	60pF	60pF	60pF	150pF	500pF
$R_{\theta JC}$	0.83°C/W	1.66°C/W	1.66°C/W	1.66°C/W	1.67°C/W	1.67°C/W	0.83°C/W
Cost	$70	$40	$28	$34	$24	NA	$75

Table III. Currently Available Power Mosfets (cont.)

Part	IRF130	2SK135	2SJ50*	VN4000A	VN4001A	VN4002A	VN0335
Source	Int Rect	Hitachi	Hitachi	Siliconix	Siliconix	Siliconix	Supertex
Process	DMOS	NA	NA	VMOS	VMOS	VMOS	VMOS
BV_{DSS}	100V	160V	-160V	400V	400V	400V	350V
BV_{GSS}	±20V	±14V	±14V	±20V	±20V	±20V	±20V
I_{DSS}	1.0mA	NA	NA	10mA	10mA	10mA	0.1mA
$I_D(cont)$	6.0A	7.0A	-7.0A	8.0A	8.0A	8.0A	4.0A
$I_D(peak)$	12.0A	7.0A	-7.0A	16.0A	16.0A	16.0A	NA
$R_{DS}(on)$	0.12Ω	1.6Ω	1.6Ω	1.0Ω	1.5Ω	7.0Ω	3.0Ω
$V_{GS}(th)$	1-3V	0-1.5V	-1.5-0V	3-5V	3-5V	3-5V	1-3V
I_{GSS}	100nA	NA	NA	100nA	100nA	100nA	NA
C_{iss}	1000pF	600pF	500pF	800pF	800pF	800pF	700pF
C_{oss}	500pF	350pF	400pF	115pF	115pF	115pF	500pF
C_{rss}	100pF	10pF	40pF	30pF	30pF	30pF	25pF
$R_{\theta JC}$	1.67°C/W	0.8°C/W	0.8°C/W	1.17°C/W	1.17°C/W	1.17°C/W	NA
Cost	$18	NA	NA	NA	NA	NA	$21

* P-channel device.

NA Information not available

Table IV. Currently Available Power Mosfets (cont.)

Part	VN0435	VN0440	VN0445	VN0450	VN0345	VN0340	VP0109*
Source	Supertex	Supertex	Supertex	Supertex	Supertex	Supertex	Supertex
Process	VMOS	VMOS	VMOS	VMOS	VMOS	VMOS	VMOS
BV_{DSS}	350V	400V	450V	500V	450V	400V	-90V
BV_{GSS}	±20V	±20V	±20V	±20V	±20V	±20V	±20V
I_{DSS}	250μA	250μA	250μA	250μA	100μA	100μA	-10μA
$I_D(cont)$	8.0A	8.0A	8.0A	8.0A	4.0A	4.0A	-1.0A
$I_D(peak)$	NA	NA	NA	NA	NA	NA	NA
$R_{DS}(on)$	0.8Ω	0.8Ω	0.8Ω	0.8Ω	3.0Ω	3.0Ω	9.0Ω
$V_{GS}(th)$	1-3V	1-3V	1-3V	1-3V	1-3V	1-3V	-1.5- -3.5V
I_{GSS}	250nA	250nA	250nA	250nA	100nA	100nA	100nA
C_{iss}	2000pF	2000pF	2000pF	2000pF	700pF	700pF	50pF
C_{oss}	1500pF	1500pF	1500pF	1500pF	500pF	500pF	50pF
C_{rss}	75pF	75pF	75pF	75pF	25pF	25pF	10pF
$R_{\theta JC}$	NA	NA	NA	NA	NA	NA	NA
Cost	NA	NA	NA	NA	$30	$24	$9

* P-channel device.

NA Information Not Available

3. Mosfet Drive Design

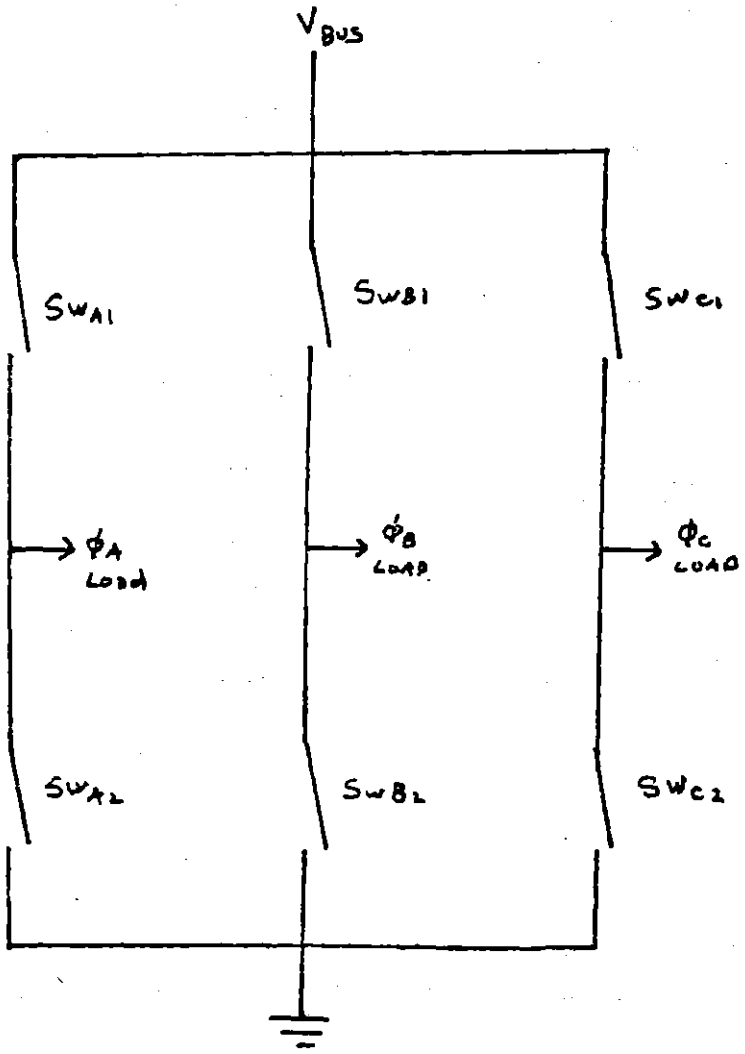
In order to use the mosfets in the application it is necessary to develop a drive design. Several steps are necessary in order to arrive at the final design. The initial steps are the selection of the topology or topologies to be examined and the particular power devices to be used. Then the initial design or designs can be built and unforeseen problems can be corrected. Finally, once a working design exists, the design can be analyzed and optimized.

3.1 Topology Selection

The basic topology was selected to be the bridge topology shown in Fig.8 because it seems to accomplish dc-ac inversion with the fewest parts. Although bipolar drive topologies can certainly be modified to drive power mosfets, the use of these circuits will almost certainly not take advantage of the unique characteristics of the power mosfet. Basically to switch a mosfet on and off it is necessary to charge and discharge its input capacitance. The switching speed is determined by how fast these charges and discharges can be accomplished. Several topologies were examined which accomplished the task of driving a bridged pair of mosfets. Complementary topologies were not examined because P-channel mosfets are unavailable.

When bridge circuits are designed using non-complementary devices, one of the largest obstacles to be overcome is the fact that the upper corner drive must float up and down with the output voltage. Five basic schemes were developed to provide this floating upper corner drive.

Fig. 8. Basic Bridge Topology



The first topology (Fig. 9) little more than a bipolar drive topology adapted to power mosfets. It utilizes a floating, low-level power supply to provide the power source for the floating upper corner drive. The upper corner drive signal is coupled in using an optoisolator, and then buffered in order to drive the mosfet input capacitance. The lower corner is simply driven directly through a buffer. Although this topology is very simple and the number of parts is small, its use in a three phase system requires three floating low-voltage power supplies in addition to the non-floating supply. This imposes a tremendous size penalty on the power supply, so basically the simplicity in the drive circuit has been obtained by imposing a complex structure on the power supply.

The second drive topology (Fig. 10) uses a transformer coupled upper corner drive. For some applications this works very well. No floating supplies are needed and the drive circuit is very simple. The biggest drawback to this topology is the frequency limitation of the transformer. In order to have the fast rise and fall times on the upper corner gate drive signal necessary for low switching losses, the transformer must have good high frequency response. To achieve switching times on the order of several hundred nanoseconds, it is necessary to have a transformer with frequency response out to 5MHz. This extended high frequency response requires very low leakage inductance. This can be accomplished with special wire and winding techniques. Low frequency response, however, is more difficult to achieve. To achieve extended low frequency response it is necessary to minimize the ratio of self inductance to series resistance. A small transformer with extended low frequency response is an

Fig. 9. Drive Topology I

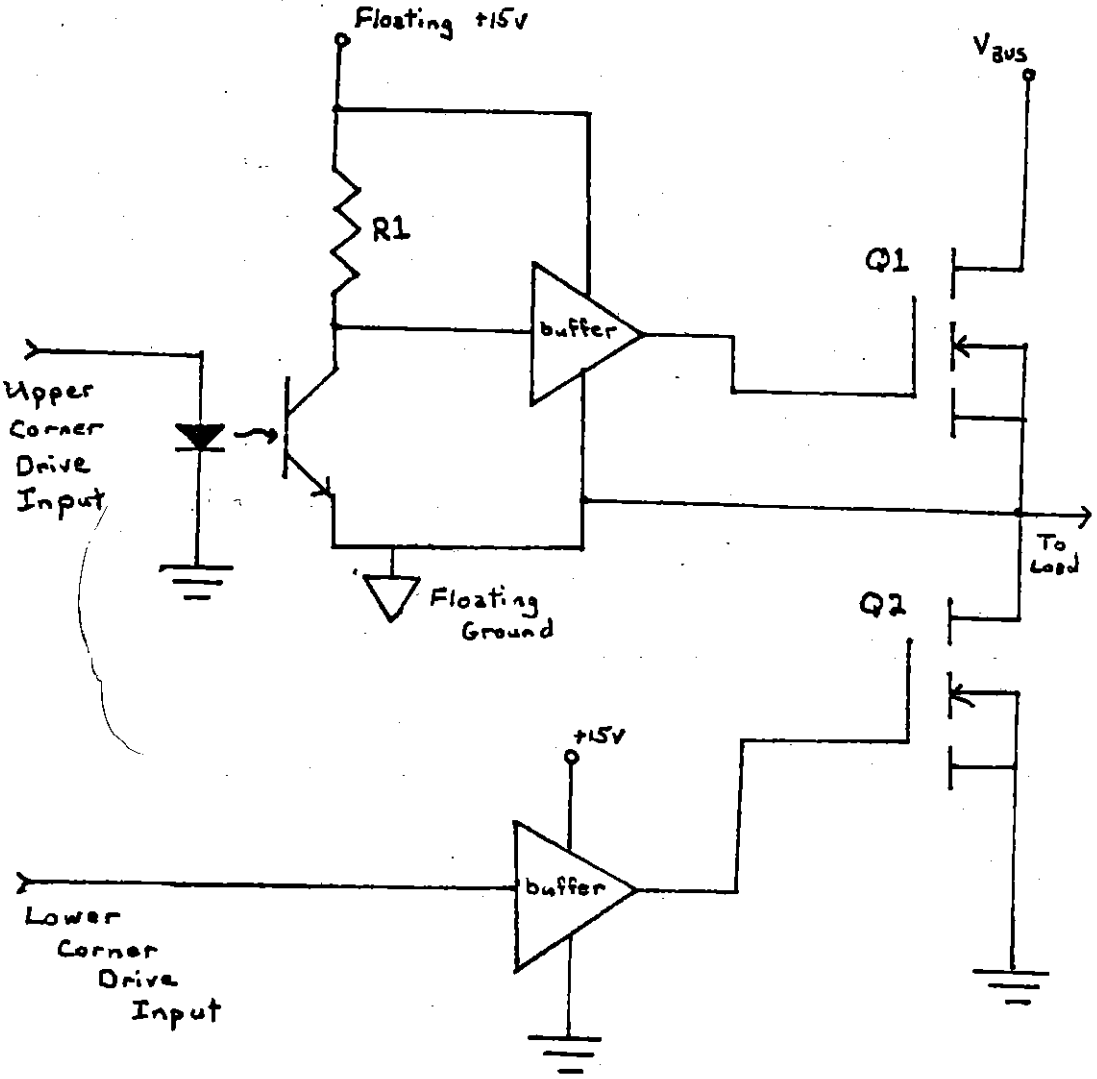
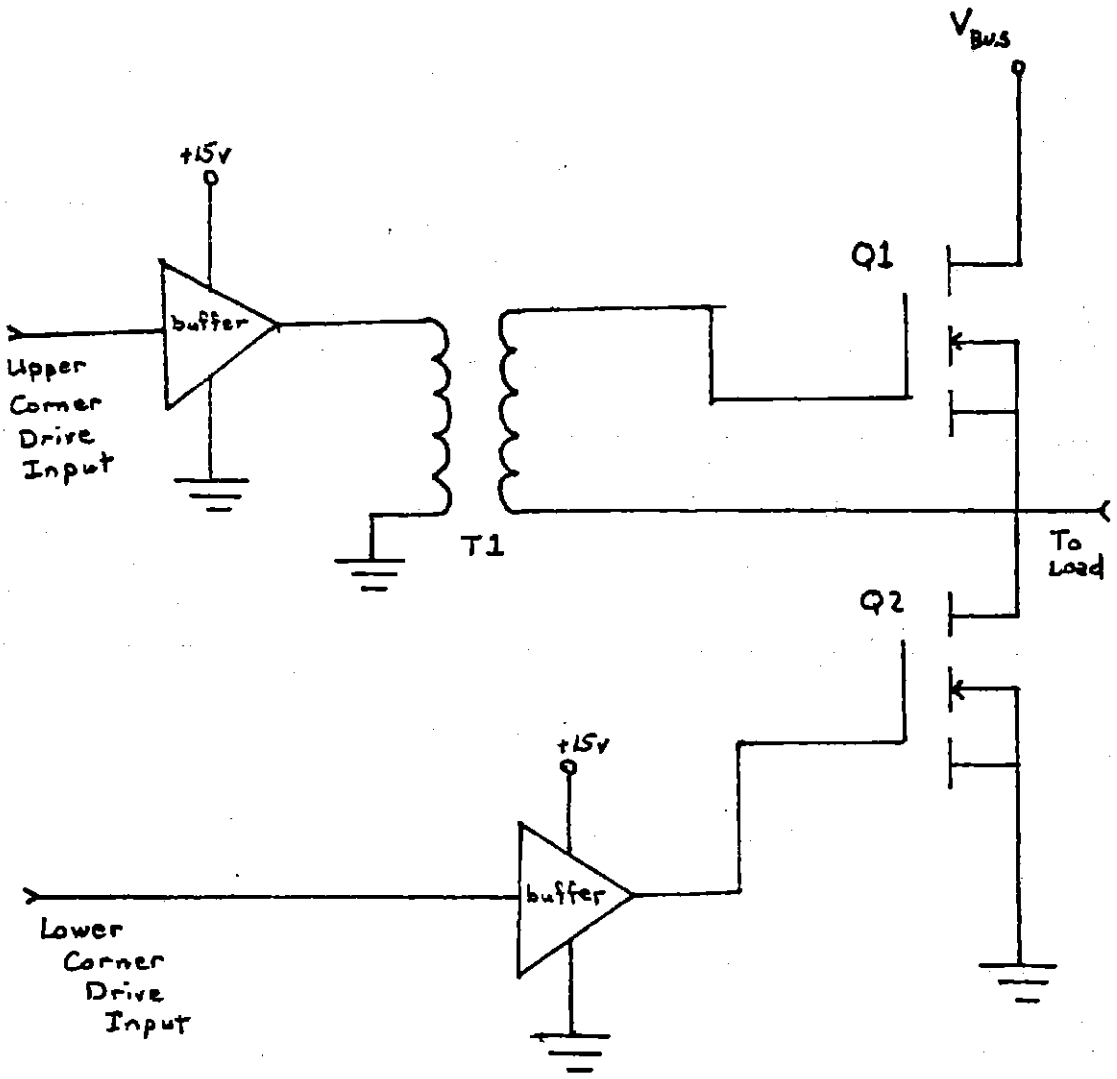


Fig. 10. Drive Topology II



impossibility. Either the self-inductance is made large with a large amount of iron or the series resistance is made small with a large amount of copper or both. As the transformer gets larger it also becomes more difficult to achieve the low leakage inductance necessary for high frequency response. So while the transformer drive topology is attractive for many applications, for applications requiring low frequency switching capability, a substantial size penalty must be paid to fit in a transformer with the required frequency response.

In the third topology (Fig. 12) inductive ring up is used to charge the upper corner input capacitance. To examine this one can model the upper corner charging circuit as shown in Fig. 13. In this circuit model, C_{IN} is the input capacitance of mosfet Q1, SW1 is mosfet Q3, C_{OUT} is the output capacitance of mosfet Q3, and $V_{LOAD}(t)$ is the output voltage which slews from 0 volts to V_{RAIL} during the switching transient. The energy stored in the inductor must supply the energy finally stored in the input capacitance, $1/2\ C_{IN}V^2_{FINAL}$, and the energy stored in the output capacitance, $1/2\ C_{OUT}V^2_{RAIL}$, plus it must supply energy to negate the energy pumped back from the output, $1/2\ C_{OUT}V^2_{RAIL}$. The energy balance to size the inductor is then:

$$1/2\ LI^2 = 1/2\ C_{OUT}V^2_{RAIL} + 1/2\ C_{IN}V^2_{RAIL} + 1/2\ C_{IN}V^2_{FINAL} + \text{SAFETY MARGIN.}$$

One can define the time constant, $\tau = L/R$, which determines the recovery time of the circuit. The peak current is determined by the size of the resistor: $I = V_{LOW}/R$. Using these expressions in the above equation yields the following equation.

Fig. 11. Drive Topology III

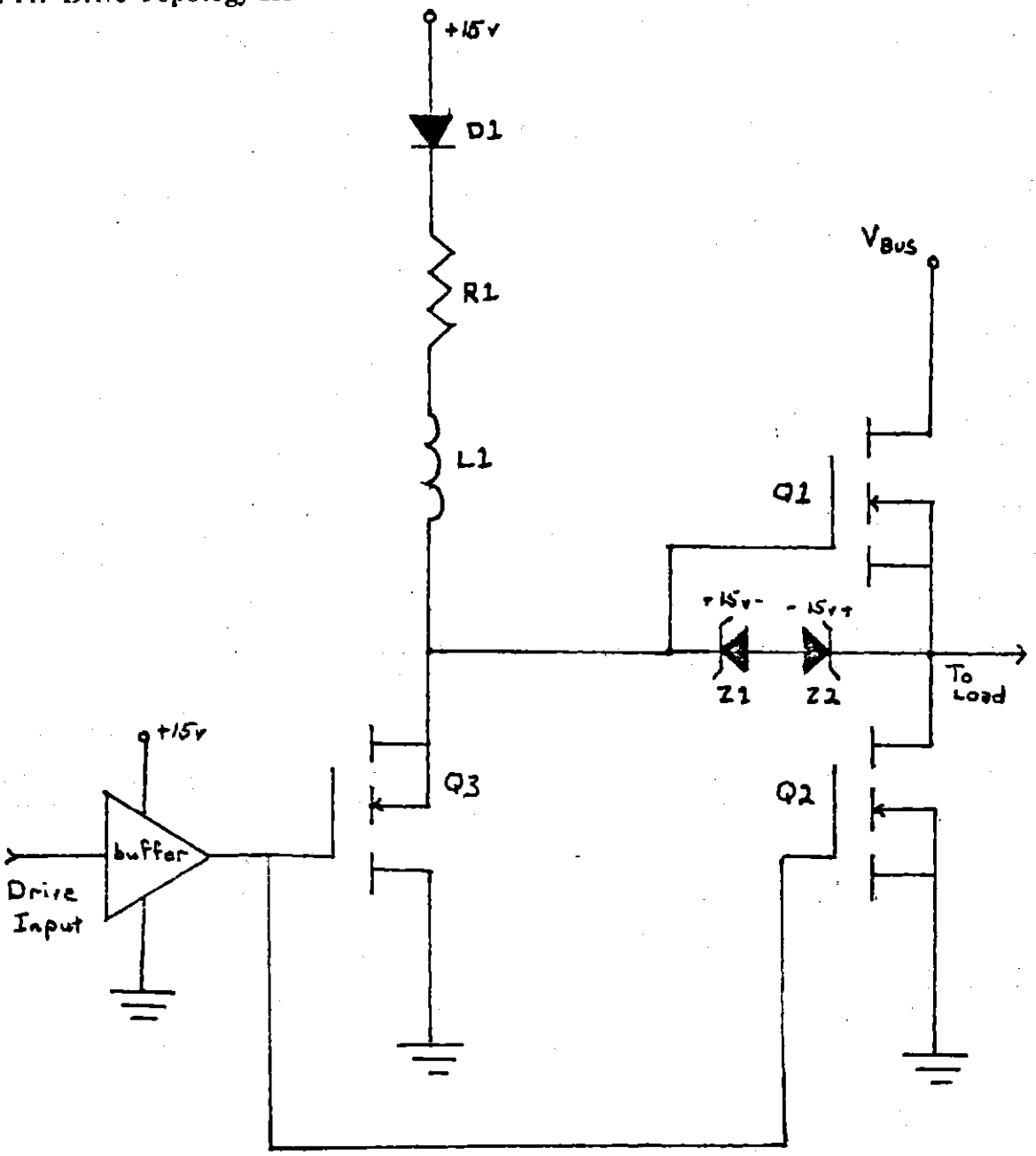
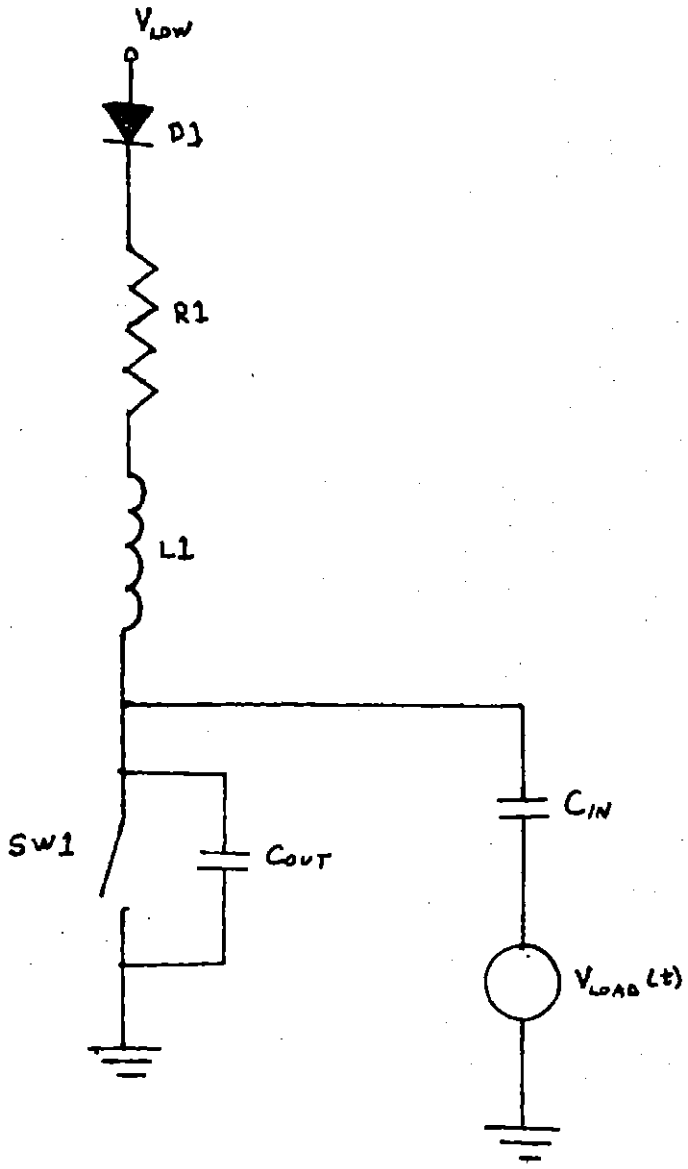


Fig. 12. Upper Corner Charging Circuit Model

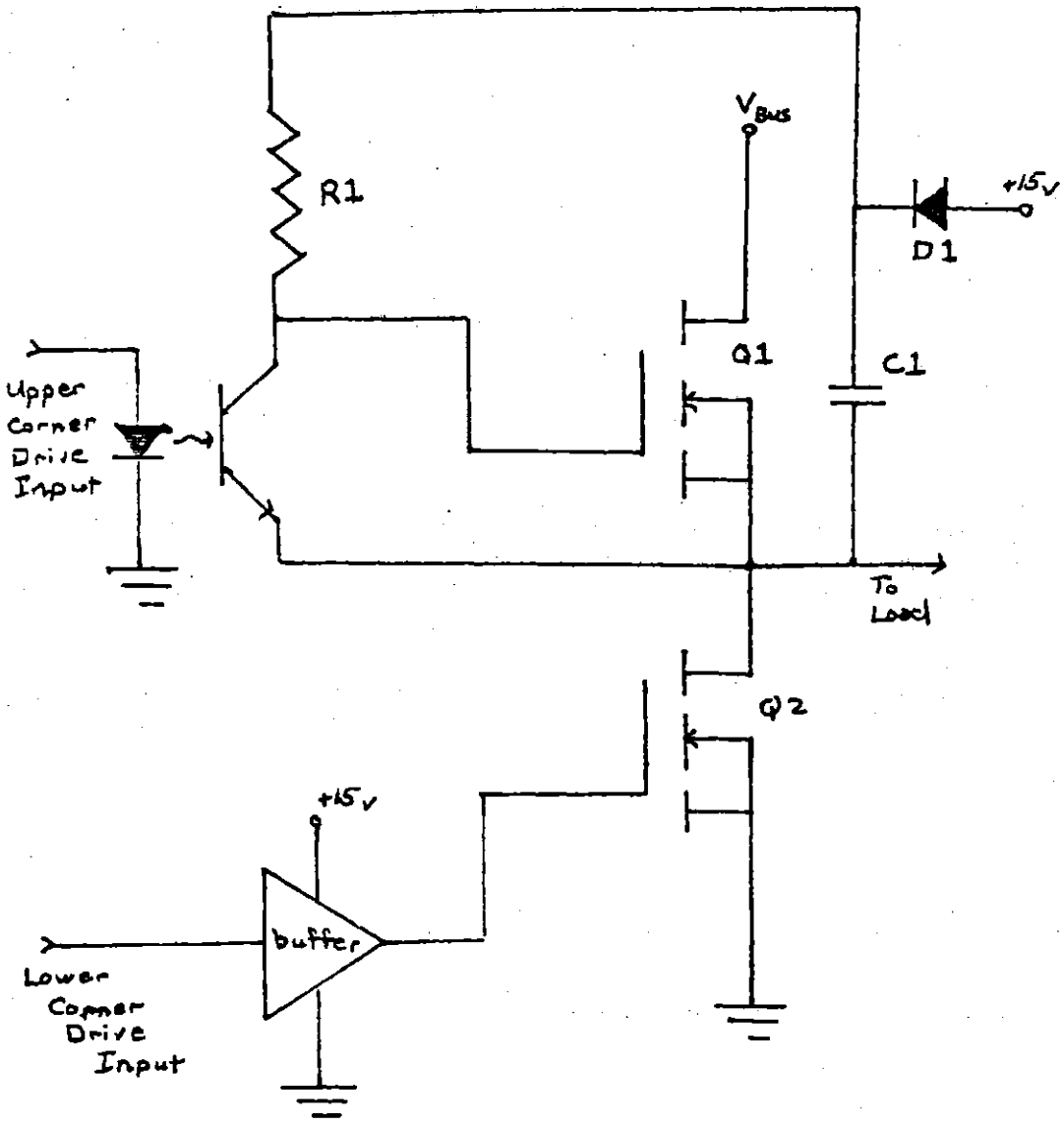


$$1/2\ V_{LOW}^2\tau^2/L = 1/2\ C_{OUT}V_{RAIL}^2 + 1/2\ C_{IN}V_{RAIL}^2 + 1/2\ C_{IN}V_{FINAL}^2$$
$$+ \text{SAFETY MARGIN}$$

As an example suppose a circuit has the following parameters: C_{IN} = 1500 pF, C_{OUT} = 200 pF, V_{RAIL} = 300 v, V_{FINAL} = 15 v, V_{LOW} = 15 v. Assume a safety margin of 50% is desired and a recovery time of 50 μs is desired. The above equation then yields the following component values: R = 48 Ω , L = 2.4 mH. The zener diode, Z1, shown in Fig. 10, clamps the final gate voltage of mosfet Q1 at 15 volts. The excess energy in the inductor is dissipated in this diode. This drive scheme has two major problems. First the power dissipation in the resistor is relatively large. In the example above, assuming a 50% duty cycle, the power dissipation would be 2.4 watts. Also once the mosfet input capacitor is charged, it has no source of refresh. At low frequencies this may become a problem as the charge slowly leaks off the gate capacitance. This could be remedied by paralleling the input capacitance with a larger capacitor but this causes a corresponding increase in the energy that must be stored in the inductor.

The fourth topology, Fig. 13, uses a floating capacitor, C1, as a floating supply to charge the upper corner mosfet input capacitance. When mosfets Q2 and Q3 are "on", capacitor C1 is charged to 15 volts from the low level supply and the gate of Q1 is held at ground. When Q2 and Q3 are turned off, capacitor C1 acts as a voltage source floating with the output voltage, and charges the input capacitance of Q1 to 15 volts through the resistor R. The upper corner switching speed is limited by the time constant RC_{IN}. If R is made small in order to enhance switching speed, the power it dissipates when Q3 is "on" becomes excessive. A somewhat improved version of this

Fig. 13. Drive Topology IV



topology is shown in Fig. 14. In this topology the source impedance for charging the gate capacitance of the upper corner mosfet has been greatly reduced by using Q4 as an emitter follower. The diode, D1, insures that a low impedance discharge path remains for the upper corner gate charge. One advantage of this topology is the ability to sustain leakage from the gate capacitance for long periods of time by using C1 as a charge reservoir. If a longer holdup time is desired, the size of C1 can simply be increased. This design does have two possible disadvantages. First there is no provision made for having both the upper and lower corners turned off at the same time. This could be a problem in some applications depending on the control strategy. Another disadvantage is that the mosfet Q3 is an additional high voltage component. Although the average current in Q3 is small, it must withstand a voltage equal to the sum of the bus voltage and the low level supply.

The fifth topology (Fig. 15) is a variation on the preceding one. A capacitor, C, is again used to provide a floating charge source for the upper corner gate drive. An optoisolator, Q3, is used to couple in the upper corner drive. This has a definite advantage over the previous design. The floating upper corner in this design is much better isolated from the rest of the circuitry and hence can be switched off simultaneously with the lower corner. A significant disadvantage of this design is the slow speeds at which optoisolators are able to switch, especially into capacitive loads. Currently available optoisolators can switch as fast as 10 μs and source as much as 150 mA. This would result in extremely slow upper corner switching times and large switching losses. A more practical version of this topology is shown in Fig. 16. In this

Fig. 14. Improved Version of Drive Topology IV

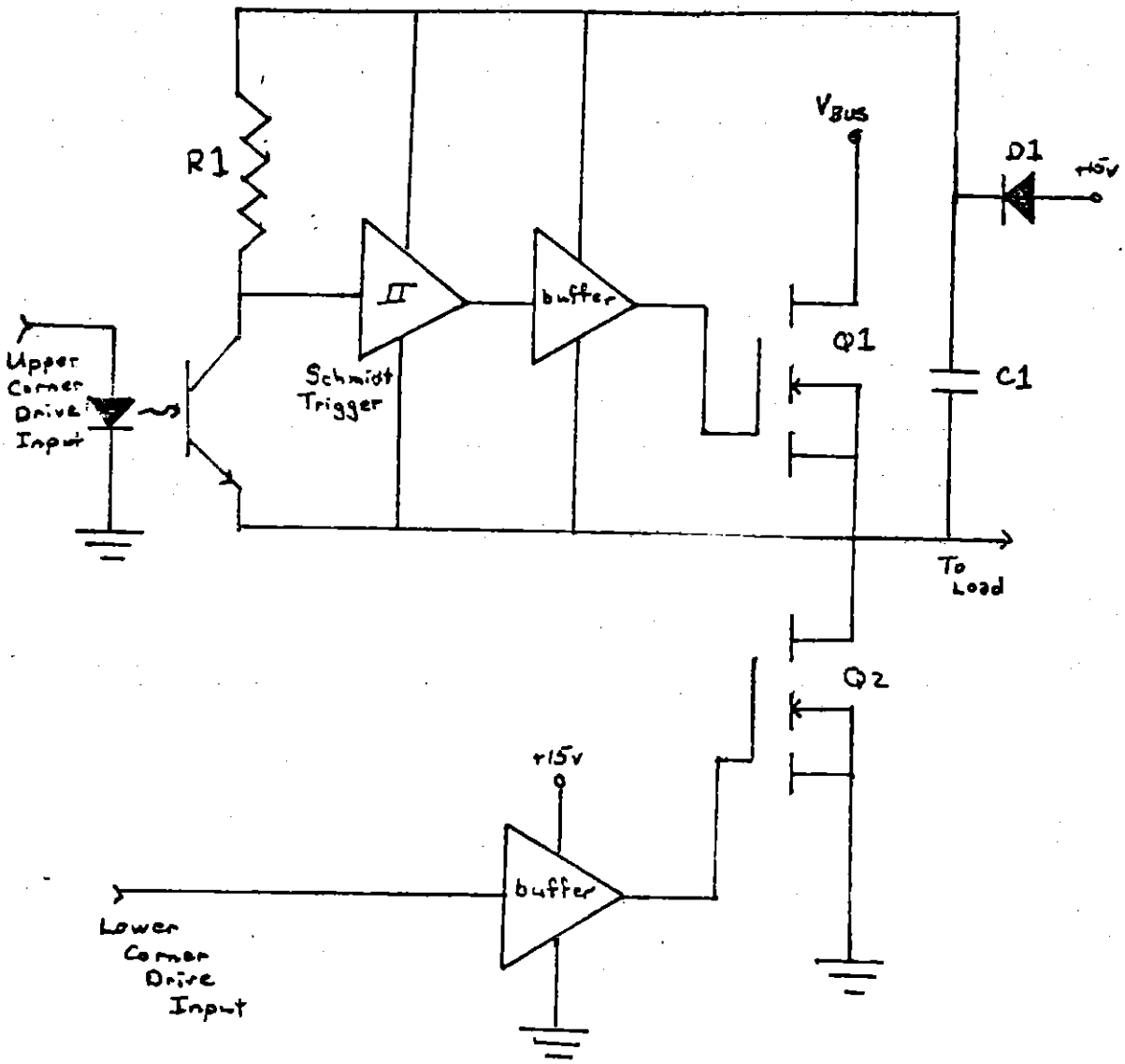


Fig. 15. Drive Topology V

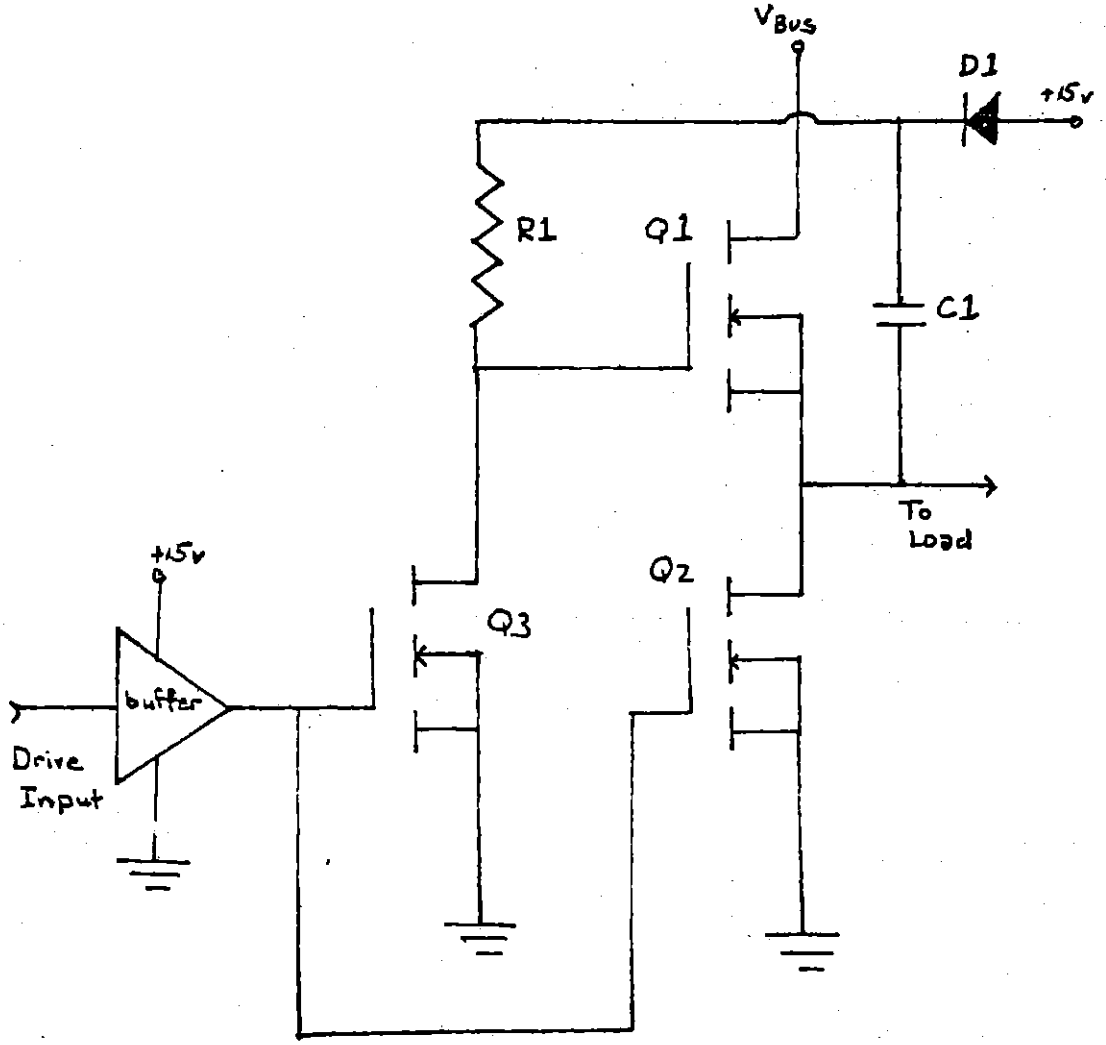
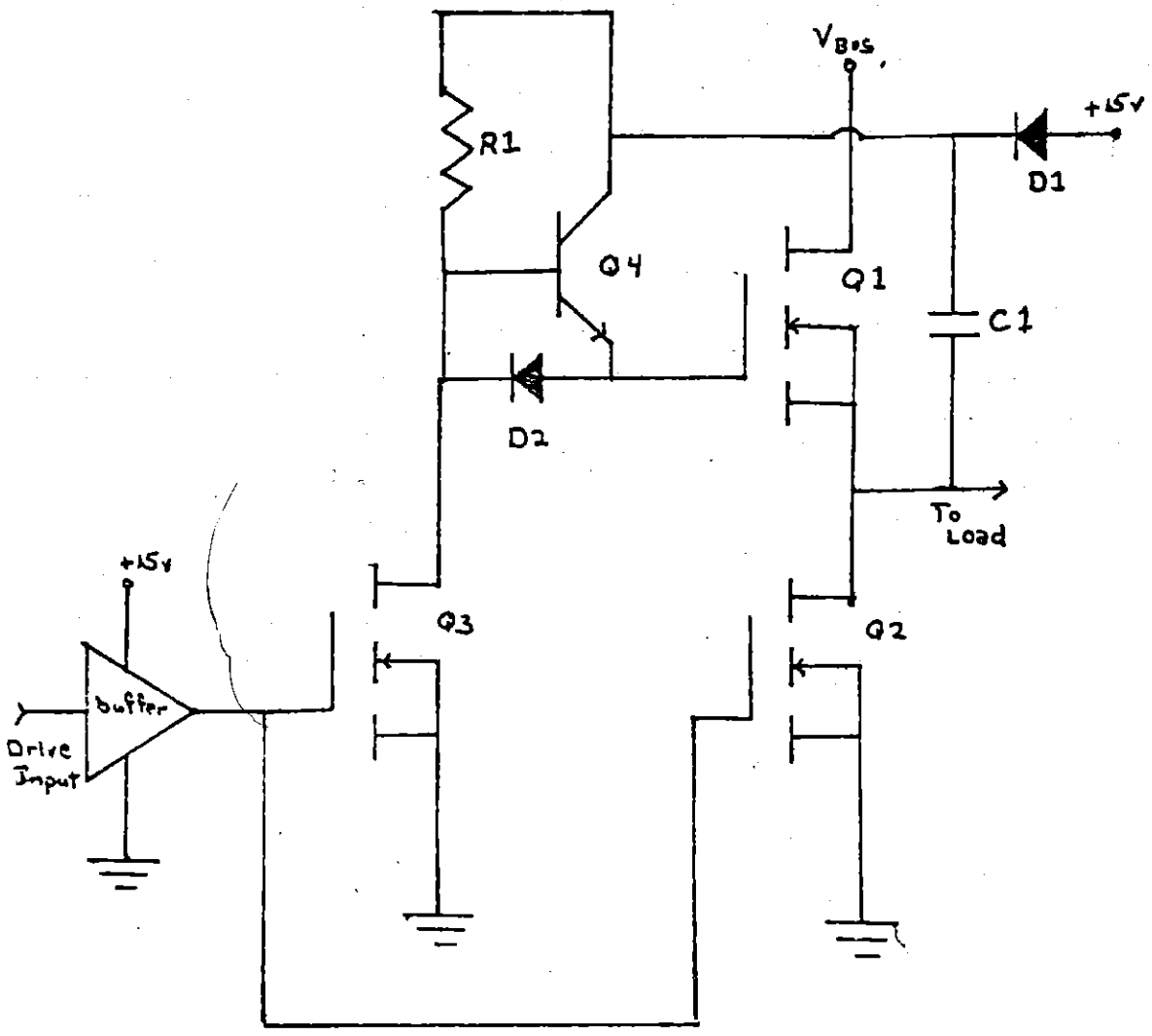


Fig. 16. Improved Version of Drive Topology V



circuit the switching speed is greatly enhance by using a CMOS Schmidt trigger and CMOS buffer. The combination of these two devices will supply very fast switching gate drive to the upper corner mosfet. The CMOS chips are necessary to limit the steady state drain on the capacitor, which is acting as their power supply. The price to be paid for this improved switching is the delay introduced by the Schmidt trigger and the added circuit complexity. Using available parts the delay could be kept as low as about 2 μs.

The major constraints in deciding among these topologies were the necessity to have a small size and the necessity to switch at low frequencies. These constraints eliminated the first three topologies. Because space was at a premium and the ability to simultaneously shut off both upper and lower corners was not necessary, the fourth topology was selected for development over the fifth topology.

3.2 Power Device Selection

After the basic topology has been decided upon the next task to be accomplished is the selection of a power device. The application provides constraints which dictate which devices may be used.

Several constraints on device characteristics are imposed by the application. Since the circuit must operate off bus voltages of between 300 and 50 volts, devices with a breakdown voltage of over 300 volts should be used. Practically using 400 volt devices is prudent as it allows protection against voltage ring up which may be caused by bus inductance. The peak load in this application is 1645 watts and the induction

motor is designed to operate with a line-line drive voltage of 100 Vrms. In a three phase system to deliver 1645 watts a line current of 9.5 Arms is required or a peak line current of 13.4 Amps. Allowing a 20% overload for current limit results in a worst case peak current of 16 Amps. The other application constraint is that the heat sink capability and operating environment require the minimum junction temperature with a case temperature of 70°C.

From Tables I-IV, it can be seen that the International Rectifier part, IRF350, is the part best suited for this application. If the assumption that most of the power dissipation in the power mosfet is "on" state losses, the power dissipated in an IRF350 in this application can be calculated.

In calculating power dissipation one must use the fact that the "on" resistance increases with temperature at the rate of 0.7%/°C. Thus the power equation for the mosfet is:

$$P = I_{RMS}^2 R_{ON}(25^oC)e^{0.007(T-25)}$$

Assuming a case temperature of 70°C and knowing the case-junction thermal resistance $R_{\theta JC}$ reduces this equation to one unknown:

$$P = I_{RMS}^2 R_{ON}(25^oC)e^{0.007(R_{\theta JC}P+70-25)}$$

For the IRF350 in this application the parameters are: I_{RMS} = 9.5 Amps, $R_{ON}(25^oC)$ = .3Ω, and $R_{\theta JC}$ = .83°C/watt. Using these values the power is found to be 54.8 watts indicating a junction temperature of 115°C. This is well within the manufacturer's

maximum rating of 150°C. The lack of availability of the IRF350 prompted examination of other alternatives.

Since there are no available 400 volt devices with larger current capabilities than the IRF350 it was necessary to examine paralleling devices. Two devices seemed to be appropriate for the application, International Rectifier's IRF330 and Siliconix's VN4000A. A pair of either of these devices should approximately equal the performance of the IRF350 and the dissipation would be divided between two TO-3 packages.

The chief concern when paralleling power devices is how well they current share. Current sharing must be examined both statically and dynamically. Static sharing determines how well the devices share under steady state conditions and dynamic sharing determines how well they share during switching.

Static current sharing is determined by the "on" resistances of the power mosfets. The positive temperature coefficient of the mosfet helps keep the current fairly balanced. The mosfet with the lowest "on" resistance draws more current and dissipates more power. This heats up this mosfet more which causes its resistance to increase which reduces the imbalance. The static current balance in two parallel mosfets can be found by solving four non-linear equations. The equations representing power dissipation are:

$$P_1 = I_1^2 R_{ON1}(25^oC)e^{0.007(T_{CASE}+R_{\theta JC}P_1-25)}$$

$$P_2 = I_2^2 R_{ON2}(25^oC)e^{0.007(T_{CASE}+R_{\theta JC}P_2-25)}$$

The voltage balance and current constraint equations are:

$$I_1 + I_2 = I_{TOTAL}$$

$$I_1 R_{ON1}(25^oC)e^{0.007(T_{CASE}+R_{\theta JC}P_1-25)} = I_2 R_{ON2}(25^oC)e^{0.007(T_{CASE}+R_{\theta JC}P_2-25)}$$

The worst case current sharing can be found by substituting in the lowest and highest possible values for R_{ON1} and R_{ON2} and solving.

The testing of 30 IRF330 devices showed $R_{ON}(25^oC)$ values ranging from 0.625 Ω to 1 Ω. The parameters for determining the worst case current sharing for a pair of IRF330s are $R_{ON1}(25^oC)$ = 0.625 Ω, $R_{ON2}(25^oC)$ = 1.0 Ω, $R_{\theta JC}$ = 1.67°C/watt, T_{CASE} = 70 °C, and I_{TOTAL} = 9.5 Arms. Using these values in the above formulas yield the following values.

	Current	Power	Junction Temperature	"On" Voltage
mosfet 1	5.5 A	43.6 W	143°C	7.95 V
mosfet 2	4.0 A	31.8 W	124°C	7.95 V

Although no VN4000As were available for testing, it was assumed their "on" resistance range would be the same as that of the IRF330s. The parameters used for calculating worst case current sharing for the VN4000As are $R_{ON1}(25^oC)$ = 0.625 Ω, $R_{ON2}(25^oC)$ = 1.0 Ω, $R_{\theta JC}$ = 1.17°C/watt, T_{CASE} = 70°C, and I_{TOTAL} = 9.5 Arms.

Using these parameters the following worst case sharing data was found.

	Current	Power	Junction Temperature	"On" Voltage
mosfet 1	5.65 A	37.1 W	113°C	6.5 V
mosfet 2	3.85 A	24.9 W	99°C	6.5 V

As can be seen from the numbers shown above, the current imbalance is not severe. For a ±23% variation in "on" resistance, the current variation was reduced to ±16% for the IRF330 and to ±19% for the VN4000A. This reduction in variation is a result of the positive temperature coefficient of the "on" resistance. Although the junction temperatures are higher than those for the IRF350 they are still within the manufacturers specifications - 150°C for the IRF330 and 175°C for the VN4000A.

Although the VN4000A seems to be a superior device on the basis of the above thermal behavior, its lack of availability caused the use of the IRF330 in the circuit development. At least from the information given on the manufacturers' data sheets, the VN4000A should be similar enough to the IRF330 to allow direct replacement when they become available. This should result in a performance improvement.

Dynamic current sharing is determined by how closely the paralleled devices track during switching. The big problem here is making the devices switch at the same time. Obviously if one device switches off first, the other device will pick up the total

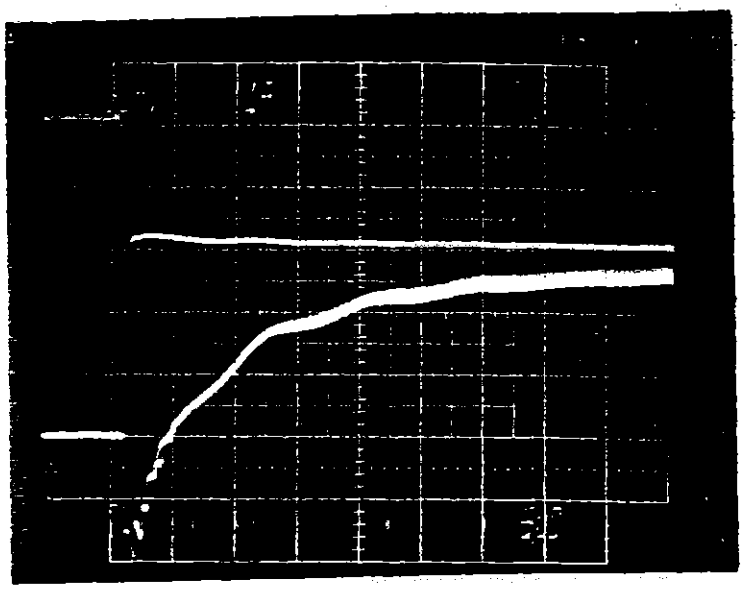
current until it switches off. Because the speed of switching of the mosfets is very fast, these current unbalances should not be a problem. Typically, slight unbalances of about 50nsec in length were observed during paralleled switching. These differences in switching times are caused by variations in gate threshold voltages. Typical paralleled turn-on and turn-off photos are shown in Fig. 17.

3.3 Circuit Implementation

Once the circuit topology and power devices to be used were selected, the circuit shown in Fig. 18 was constructed and operated. Components were not optimal, but were selected to be safe. Buffering of the drive signal was accomplished with the MMH0026. This is a bipolar clock driver with active pull-up and pull-down. It is designed to drive capacitive loads and seemed well suited to the task of driving the mosfet input capacitance. When operating the circuit, several problems quickly showed up.

The first problem seen was the need for protection from gate to source breakdown. It was very easy to accidently exceed the ±20 V absolute maximum rating and ruin a device. To prevent this problem, three zener diodes were added, Z1,Z2, and Z3, as shown in Fig. 19. The additional reverse zener was needed to protect the upper corner mosfet in order to prevent Q3 from sharing the lower corner current with Q2. Since the normal "on" voltage of Q2 can be as high as 8 volts, without the upper corner

Fig. 17. Current Sharing in Paralleled Mosfets

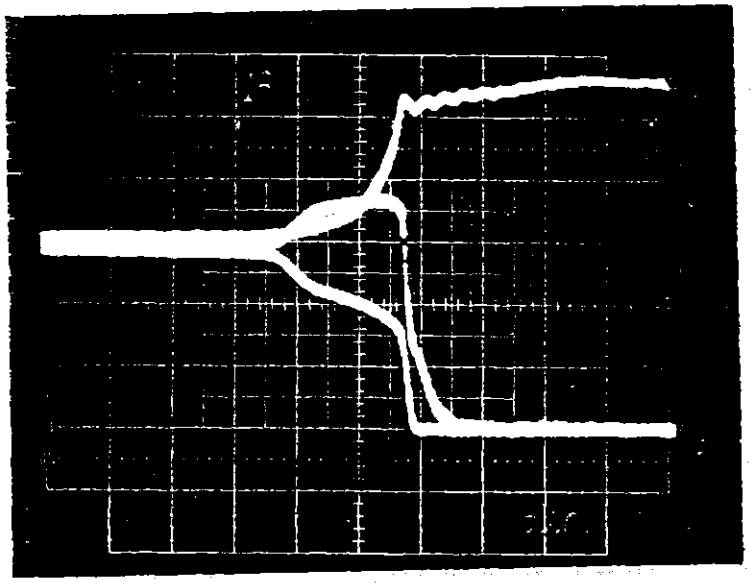


V_{DS1} 50v/div

I_{DA} & I_{DB}

2A/div

5μs/div



V_{DS1} 50v/div

I_{DA} & I_{DB}

2A/div

500ns/div

Fig. 18. Initial Drive Circuit

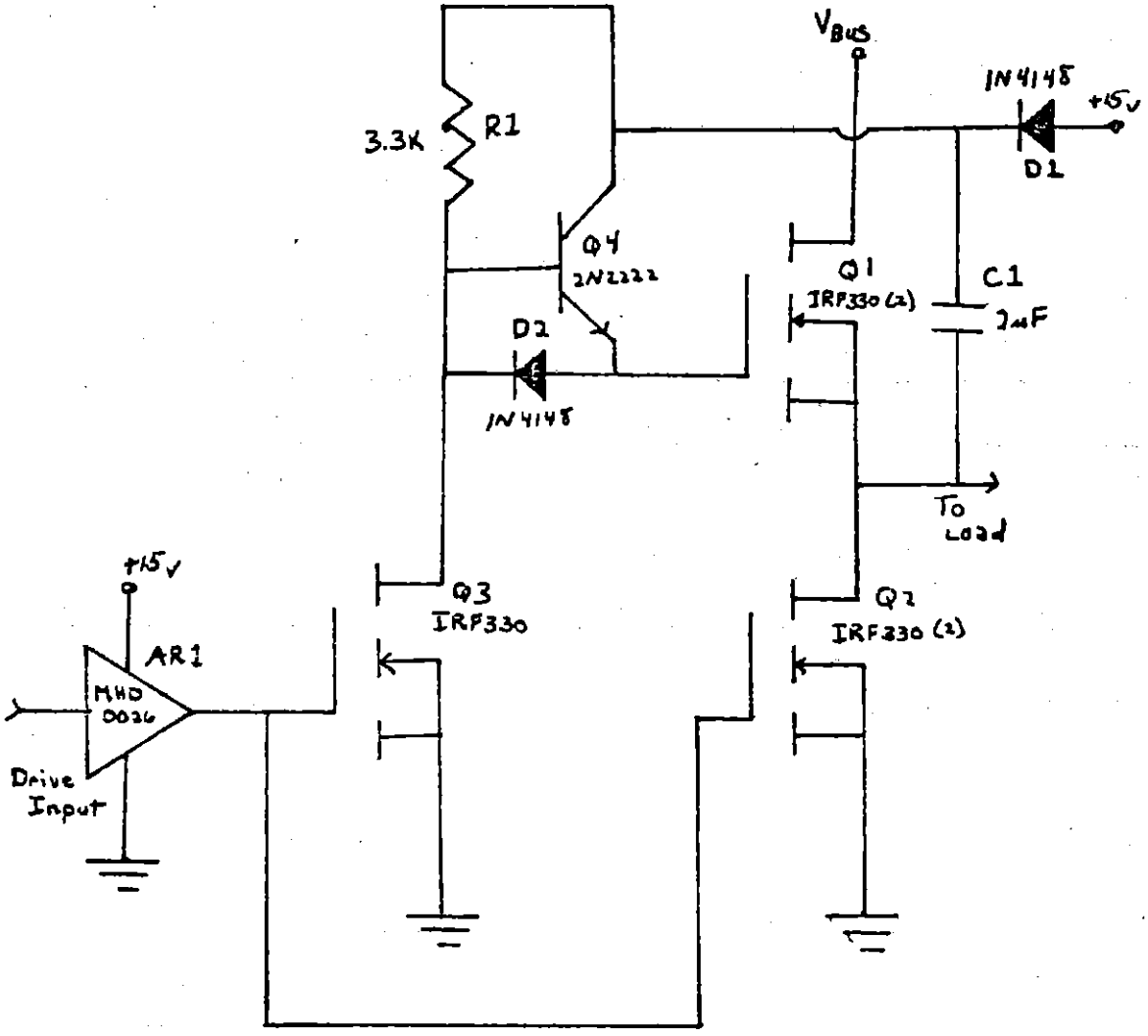
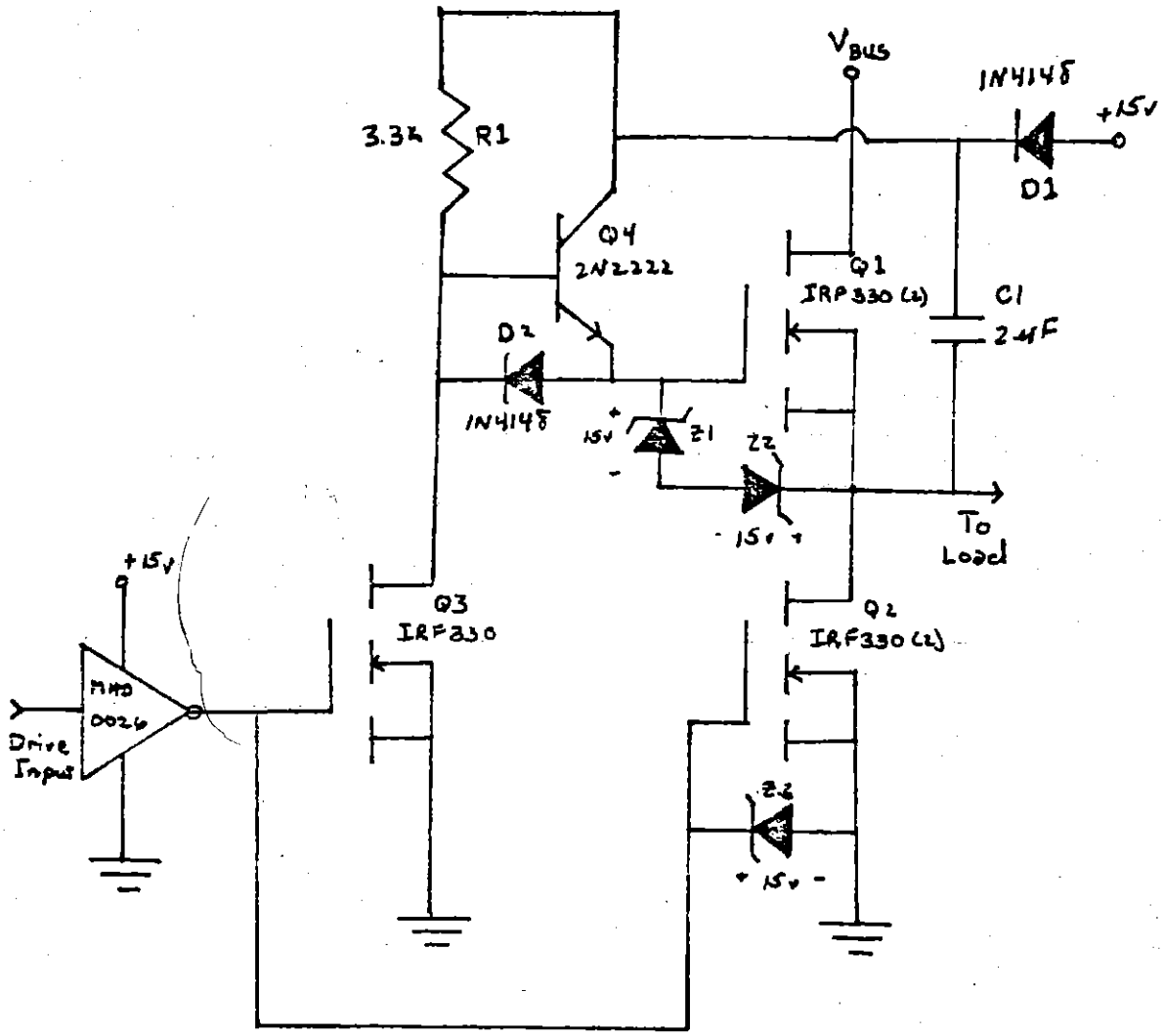


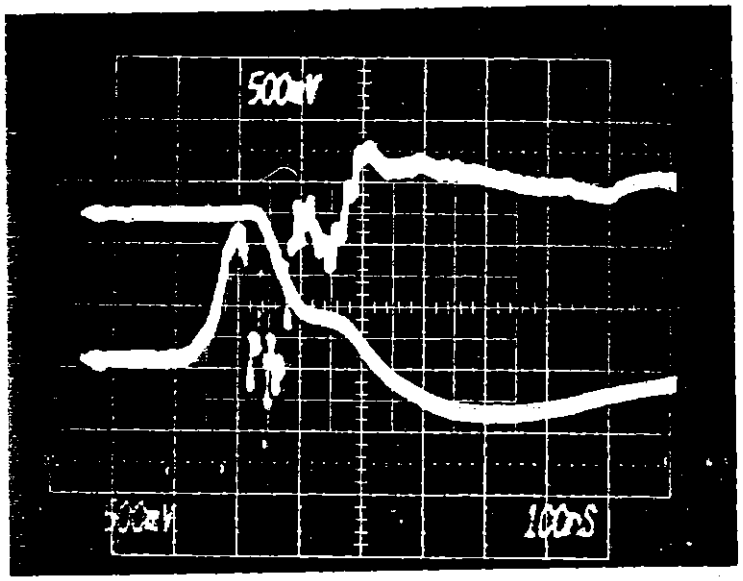
Fig. 19. Drive Circuit with Zener Gate Protection



reverse zener diode, Z2, significant current would flow through Q3, which is also "on" when Q2 is "on".

The second problem was the "shoot through" current caused by a delay in upper corner switching. This delay was caused by the Q3 switching time. If Q1 is "on" and then Q2 and Q3 both switch on, both Q1 and Q2 are "on" while Q3 is switching. This overlap in gate drives (Fig. 20) caused a very large "shoot through" current - about 20 amperes with a bus voltage of only 75 volts. Two schemes were examined to solve this problem. The first scheme was to use a resistor, R2, to slow down the turn-on of the lower corner mosfet, Q2 (Fig. 21). The result of this solution is shown in Fig. 22. While the gate drives no longer show overlap, the slow turn-on of the lower corner could result in problems, especially during pulse width modulation. During pulse width modulation, Q2 might be required to turn on and pick up a large forward current from the upper corner free wheeling diode. The very slow turn-on of the lower corner mosfet will cause it to remain saturated until the gate voltage reaches a value sufficient to support the entire load current. This behavior will greatly increase switching losses. The second solution to the problem was to use a delay network and buffer to create a fast-rising gate signal delayed by approximately 200 ns (Fig. 23). The input drive, Q5 and Q6, is designed to insure the low threshold voltage of the MMH0026 (0.2 volts) is not exceeded. The delay network is composed of R2 and C2 and the zeners, Z5 and Z6, insure that the buffer input voltages do not exceed the rated

Fig. 20. Overlapping Gate Drives



V_{GS2} 5v/div

V_{GS1} 5v/div

Fig. 21. Drive Circuit with Resistive Lower Corner Delay

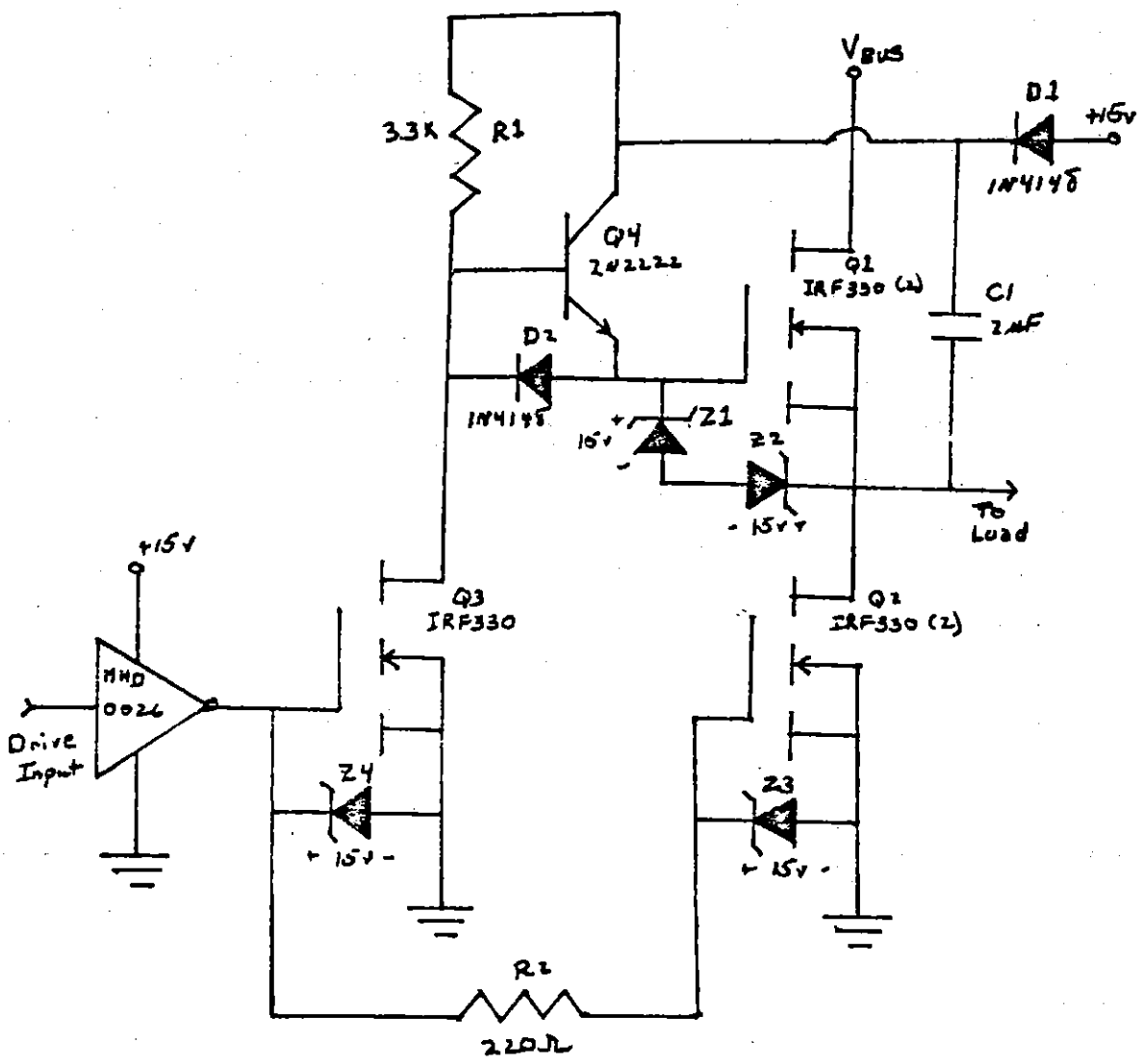
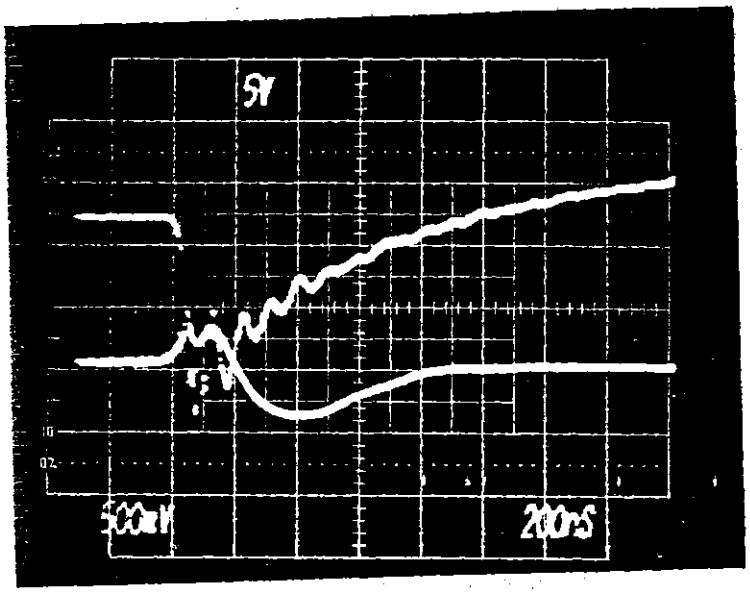


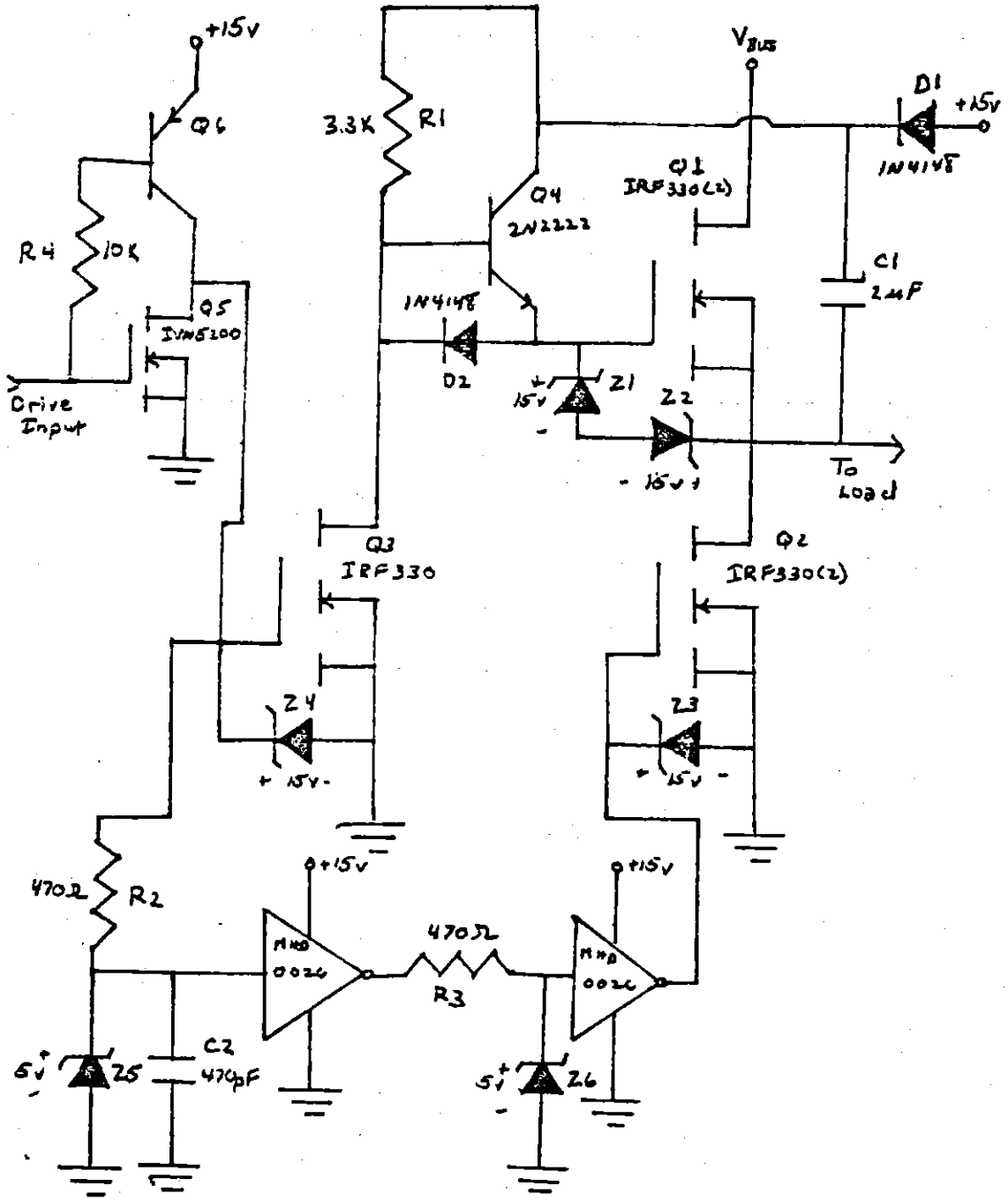
Fig. 22. Gate Drives with Resistive Lower Corner Delay



V_{GS2} 5v/div

V_{GS1} 5v/div

Fig. 23. Drive Circuit with Buffered Lower Corner Delay

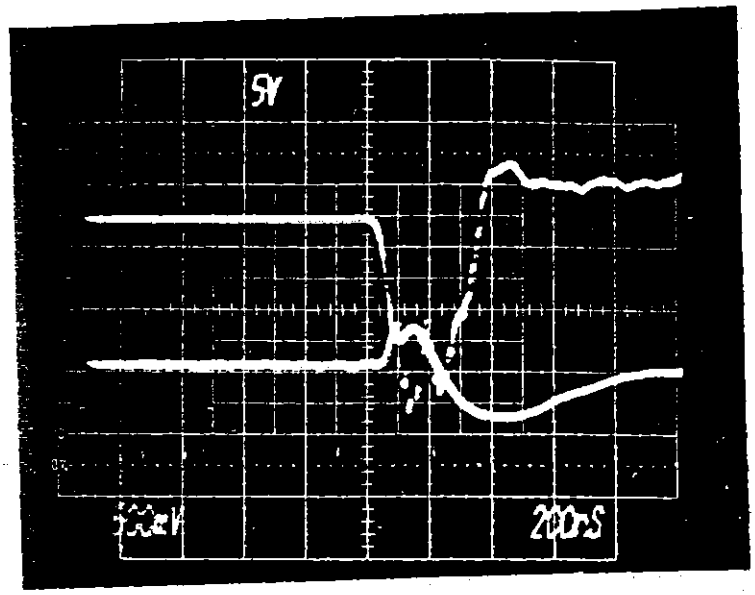


maximum. This scheme worked quite well as can be seen in Fig. 24.

The third and largest problem was caused by the reverse recovery of the mosfets' internal free wheeling diodes. When pulse width modulating into an inductive load, it sometimes happens that a mosfet will free-wheel current during its entire "on" period (Fig. 25). When this corner turns off and the other corner turns on, the other corner must conduct not only the load current but also the reverse recovery current needed to clear the free-wheeling diode of stored charge. While this charge is being cleared, the voltage drop across the diode remains low, so the other corner is faced with exceptionally large currents and the full bus voltage (Fig. 26). Because of this it is desirable to have diodes which recover quickly with small reverse recovery currents. The diodes internal to the IRF330 mosfet are not particularly good in this regard. Typical reverse recovery time of 300 ns and peak recovery currents of 10 Amps have been observed for the IRF330. International Rectifier has indicated that the reverse recovery can get much worse than that, especially at elevated temperatures [7]. To solve this problem, blocking diodes, D3 and D4, were installed to block the mosfet internal diodes and new free-wheeling diodes, D4 and D5, were installed (Fig. 27). These new diodes were International Rectifier 6FL60 devices

with a reverse recovery time of under 200 nsec and a peak recovery current of 4.0 amperes. The improvement can be seen in Fig. 28.

Fig. 24. Gate Drives with Buffered Lower Corner Delay



V_{GS2} 5v/div

V_{GS1} 5v/div

Fig. 25. Reverse Recovery During Pulse Width Modulation

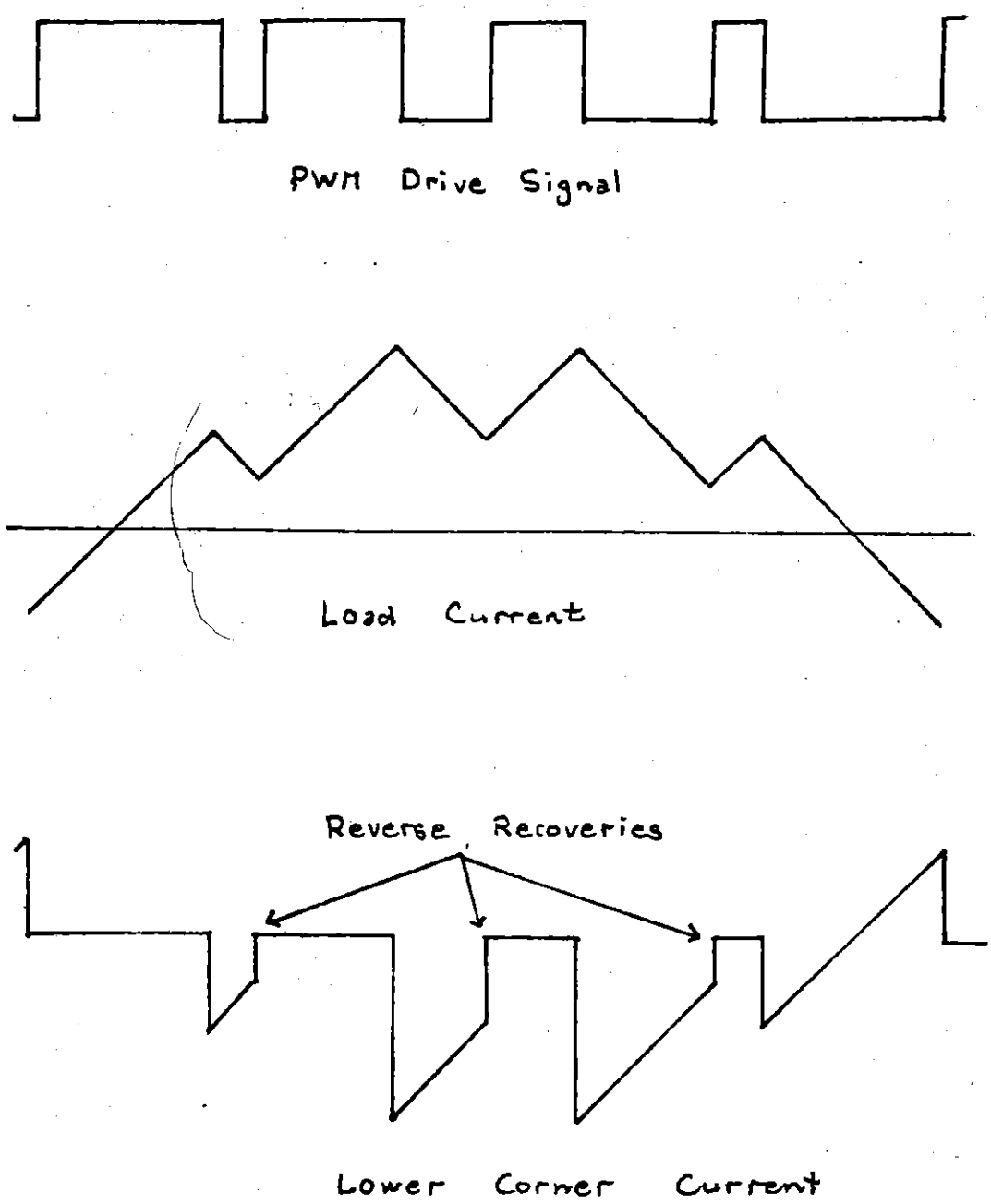
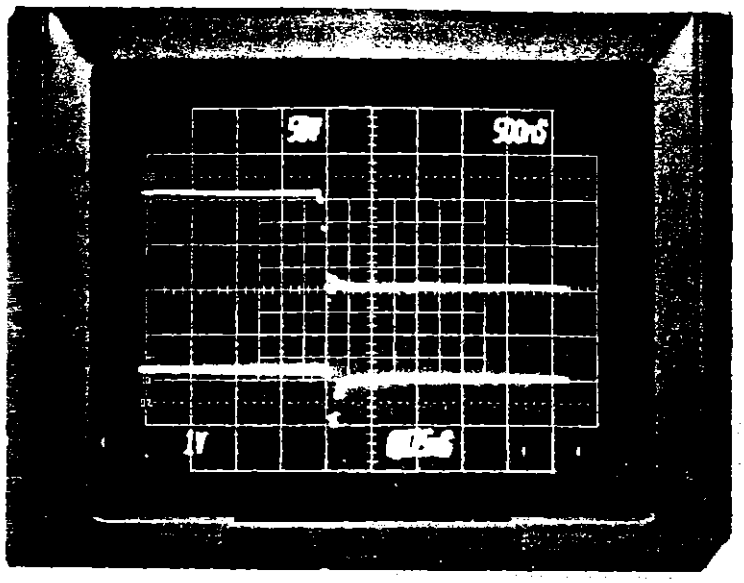


Fig. 26. Reverse Recovery with Internal Diode



V_{DS2} 50V/div

I_{FD1} 10A/div

Fig. 27. Drive Circuit with External Free-Wheeling Diode

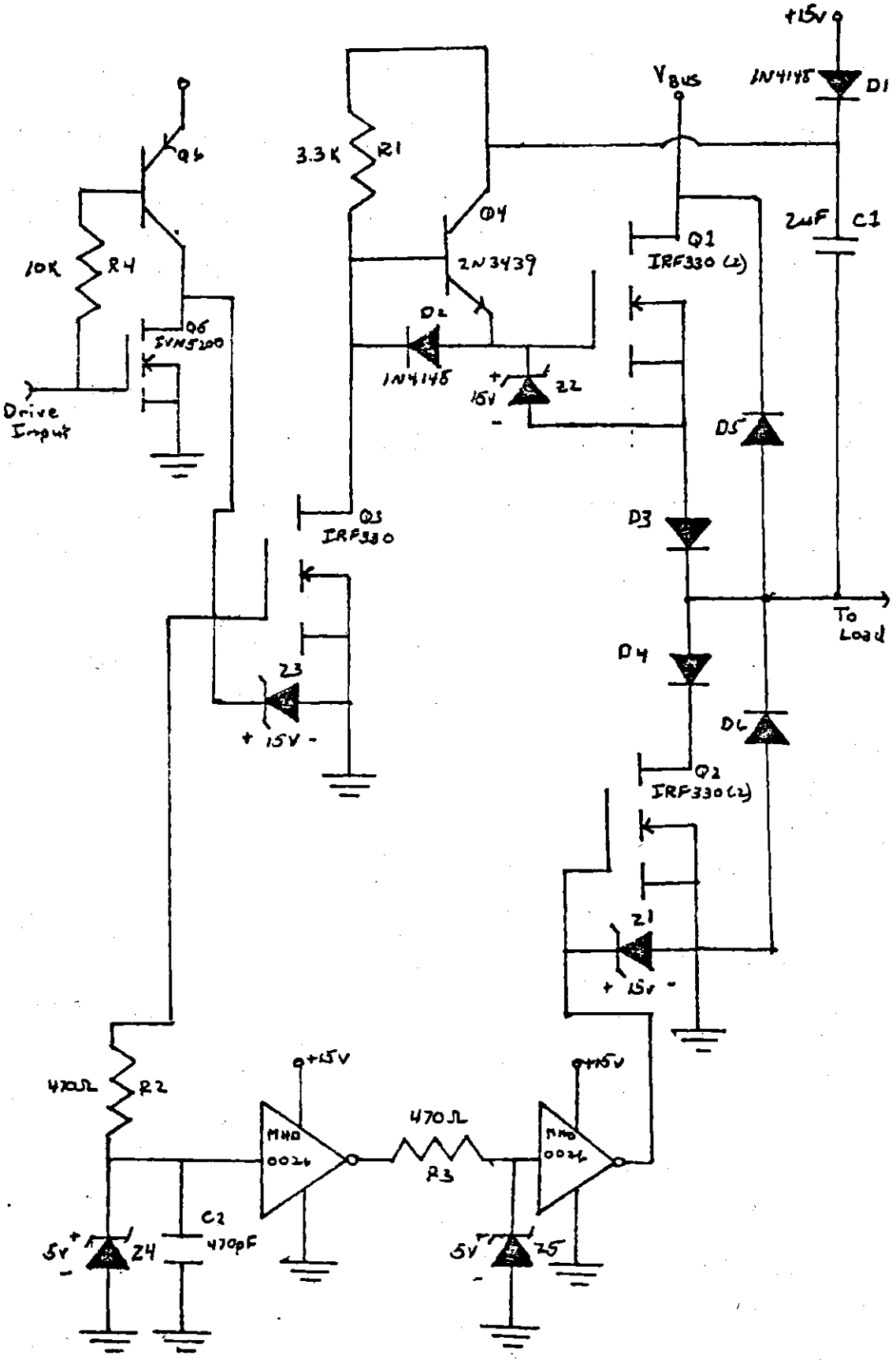
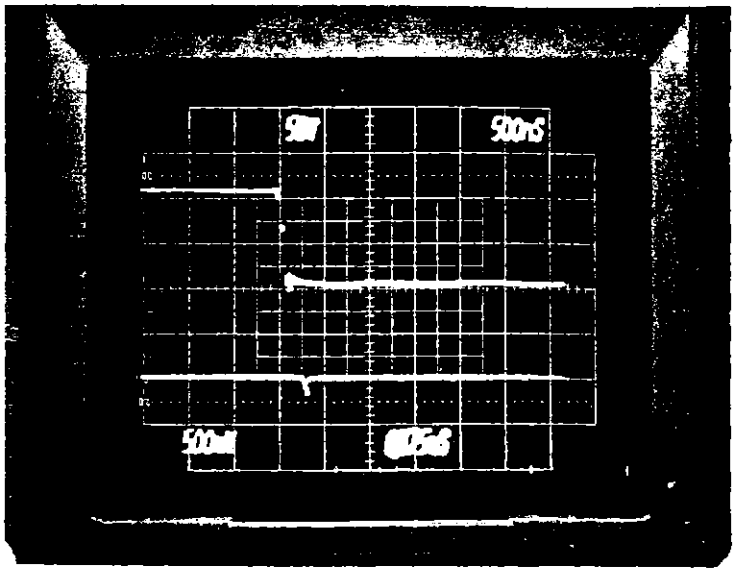


Fig. 28. Reverse Recovery with External Diode



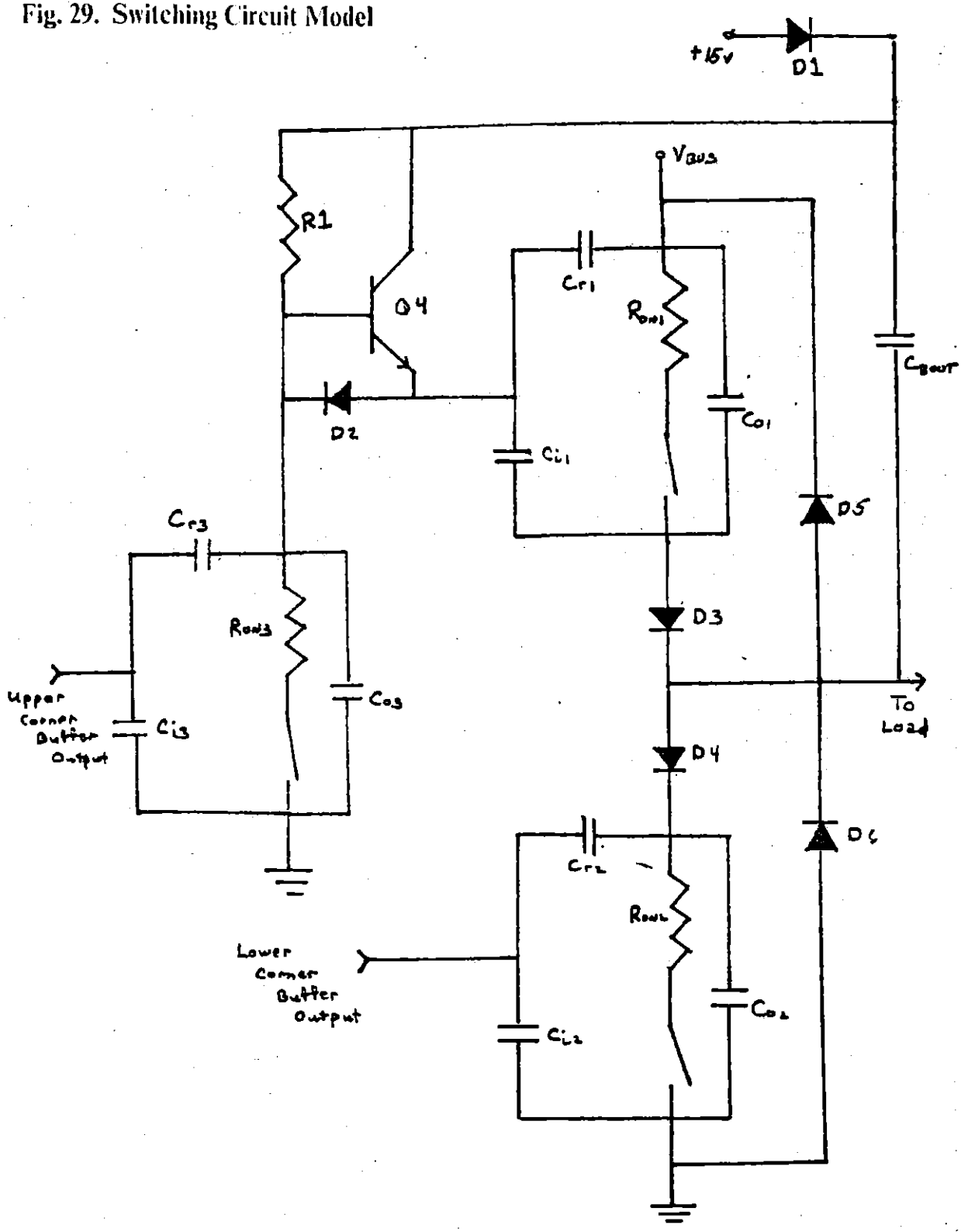
V_{DS2} 50v/div

I_{FW1} 5A/div

3.4 Circuit Analysis

The working circuit can now be analyzed to allow improved performance and to check the basic assumption made throughout the design - that the power mosfets would switch fast enough (several hundred nanoseconds or less) to make switching losses negligible. A switching circuit model of the final design is shown in Fig. 29. As can be seen from this model, the lower corner switching behavior is relatively simple. The switching speed is determined by the time constant created by the output resistance of the buffer and the effective input capacitance formed by C_{i2} and C_{r2}. Because the output impedance of the buffer used is very low ($<10\Omega$) this time constant is very small. Lower corner switching is therefore always very fast, typically under 100 nanoseconds. The upper corner switching is somewhat more complicated. Upper corner turn-off is relatively simple. The mosfet input capacitance, C_{i1} is simply discharged through the mosfet, Q3. This happens very quickly due to the low "on" resistance of the mosfet, so upper corner turn-off is very fast. Upper corner turn-on is somewhat more complicated. Two main situations exist for upper corner turn-on - either there is an inductive load and positive current flowing in the lower corner mosfet or there is not. The latter situation happens when there is a resistive load or when there is an inductive load but the current is "free-wheeling" in the lower corner prior to upper corner turn-on. When there is positive current flowing in the lower corner and the lower corner turns off, the inductance maintains the current flow, charging up the

Fig. 29. Switching Circuit Model



lower corner output capacittance, C_{o2}, to the bus voltage. When the output voltage reaches the bus voltage, the upper corner "free-wheeling" diode picks up the current. Meanwhile, the driver mosfet, Q3, has turned off and the upper corner drive circuit is trying to turn on the upper corner mosfet. To accomplish this it must charge the output capacitance of the driver mosfet, C_{o3}, to the bus voltage plus fifteen volts and the input capacitance of the upper corner mosfet, C_{i1}, to fifteen volts. This charging time is controlled by the time constant shown below.

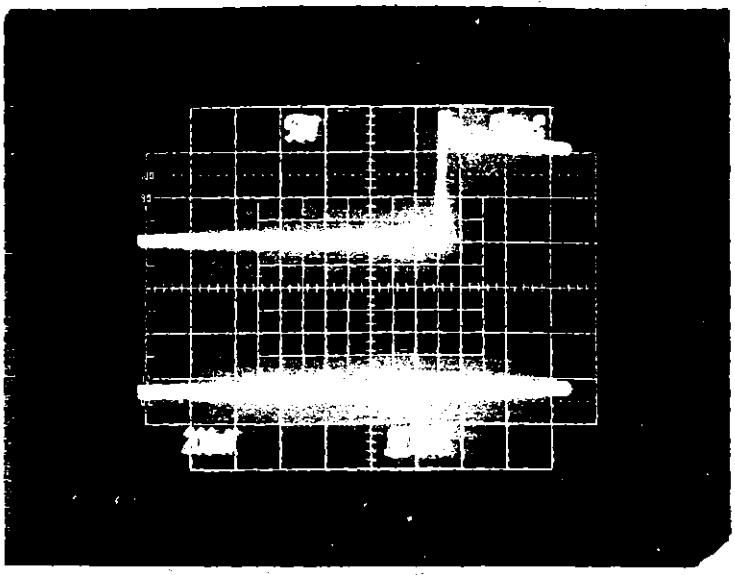
$$\tau = R1(C_{o3} + C_{i1}/\beta)$$

As can be seen from this equation, the output capacitance of the driver mosfet actually dominates the time constant. For the values of components selected previously, this time constant is 600 nanoseconds. The actual output switching is much faster, since it takes place as the gate voltage crosses the threshold voltage. When there is no inductive "kick-back" to ring up the output voltage the switching is much slower. Here again the driver mosfet output capacitance is the limiting factor. Under these conditions the bootstrap capacitor, C_{BOOT}, acts as a floating fifteen volt voltage source. The driver mosfet output capacitance, C_{o3}, is then effectively being charged by a constant current source with a magnitude of 15V/R1. The switching time is then determined by the charging time of the output capacitor, which is found from the equation below.

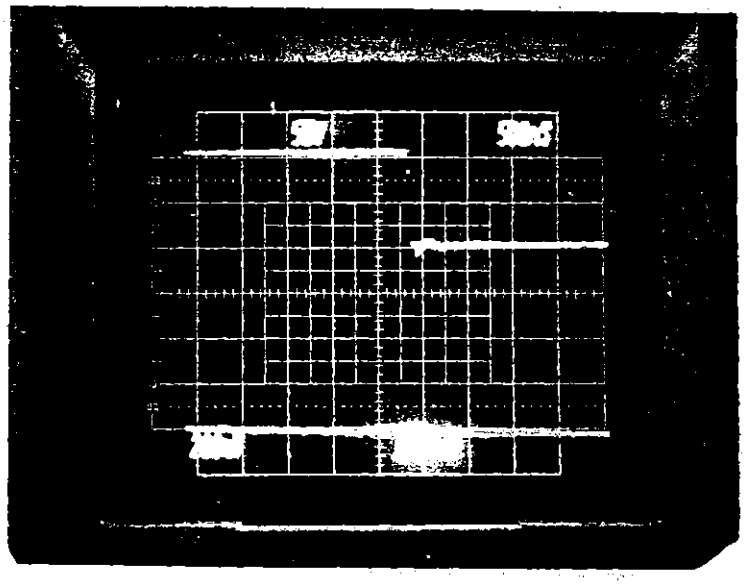
$$t_{switch} = C_{o3}V_{BUS}R1/15V$$

With a bus voltage of 300 volts, a worst-case output capacitance of 300 pF, and a resistance of 3300 Ω, this equation results in a switching time of 20 μs. This was considered unacceptably long, so the value of resistor, R1, was reduced to 330 Ω. This results in a worst-case switching time of 2 μs, and the switching time is only this slow during a "free-wheeling" upper corner turn-on. The change in this resistor value increases the driver low-level power consumption to 0.34 watts per phase. Typical switching waveforms are shown in Fig. 30 (inductive "kick-back" switching) and in Fig. 31 ("free-wheeling" switching). As expected, the "free-wheeling" upper corner turn-on is significantly slower than the other transitions. The load current in each of these photographs appears constant because at these fast time-scales the inductance of the load causes it to act like a cuurrent source.

Fig. 30. Inductive Kick-back Switching Waveforms

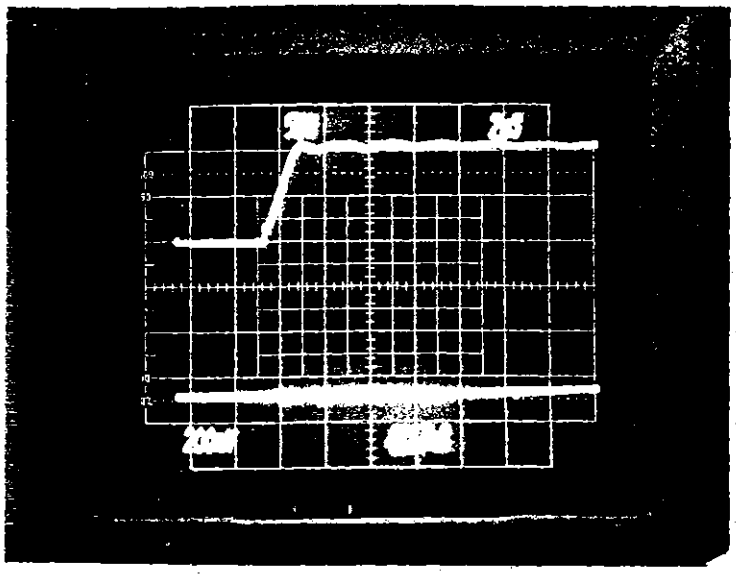


Upper Corner Turn-On



Lower Corner Turn-On

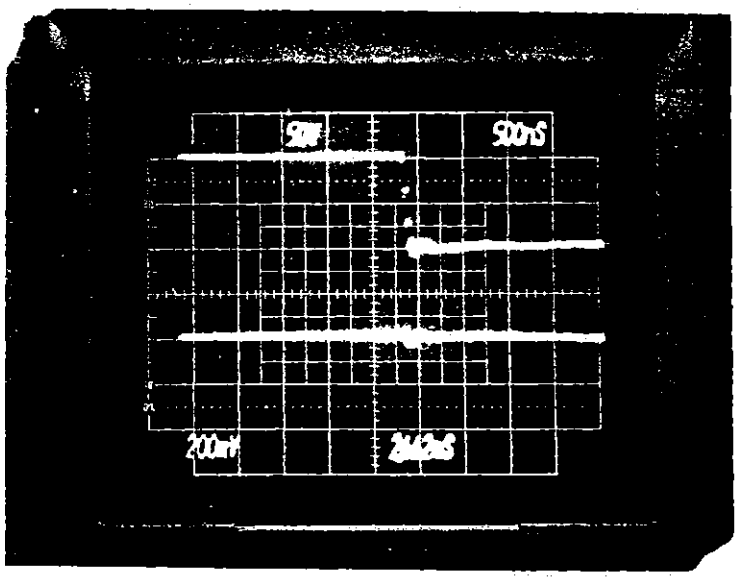
Fig. 31. Free-wheeling Switching Waveforms



VOUT

IOUT

Upper Corner Turn-On



VOUT

IOUT

Lower Corner Turn-On

4. Mosfet and Bipolar Circuit Comparison

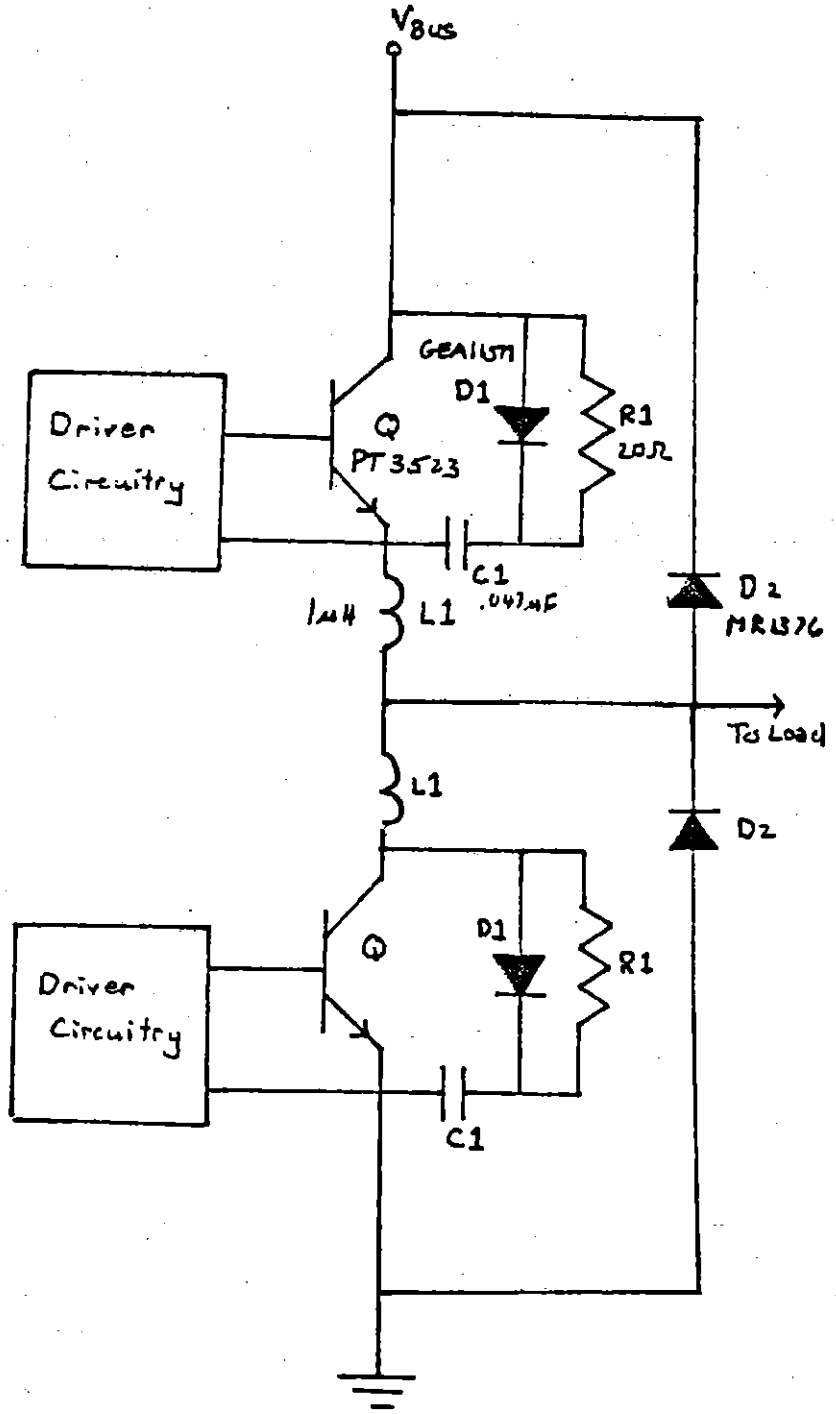
Now that the mosfet inverter circuit has been developed and analyzed, it is useful to compare it with a bipolar inverter circuit designed to accomplish the same task. While the bipolar circuit design will not be analyzed in as much detail as the mosfet design, its basic operation will be described and then its performance will be compared with that of the mosfet design in the areas of size, efficiency, reliability and cost.

4.1 The Bipolar Circuit

The basic bipolar topology is a bridge topology with parallel and series snubbers (Fig. 32). The parallel snubber is a polarized snubber consisting of R1,D1, and C1. Its purpose is to modify the turn-off behavior of the transistor to prevent secondary breakdown. The series snubber, L1, acts to limit the current spike conducted during turn-on. This current spike consists of the complementary parallel snubber charging current, the self snubber discharge current and the complementary free wheeling diode reverse recovery current in addition to the normal load current. The resistor, R1, controls the magnitude of the self snubber discharge current, dissipates the snubber energy, and determines the recovery time of the snubber.

Operation with a 300 volt bus dictated the use of 400 volt transistors. In order to avoid secondary breakdown when switching 16 amperes, the smallest snubber capacitor that could be used is 0.047 μF. Ideally the series snubber, L1, should be large

Fig. 32. Bipolar Transistor Topology

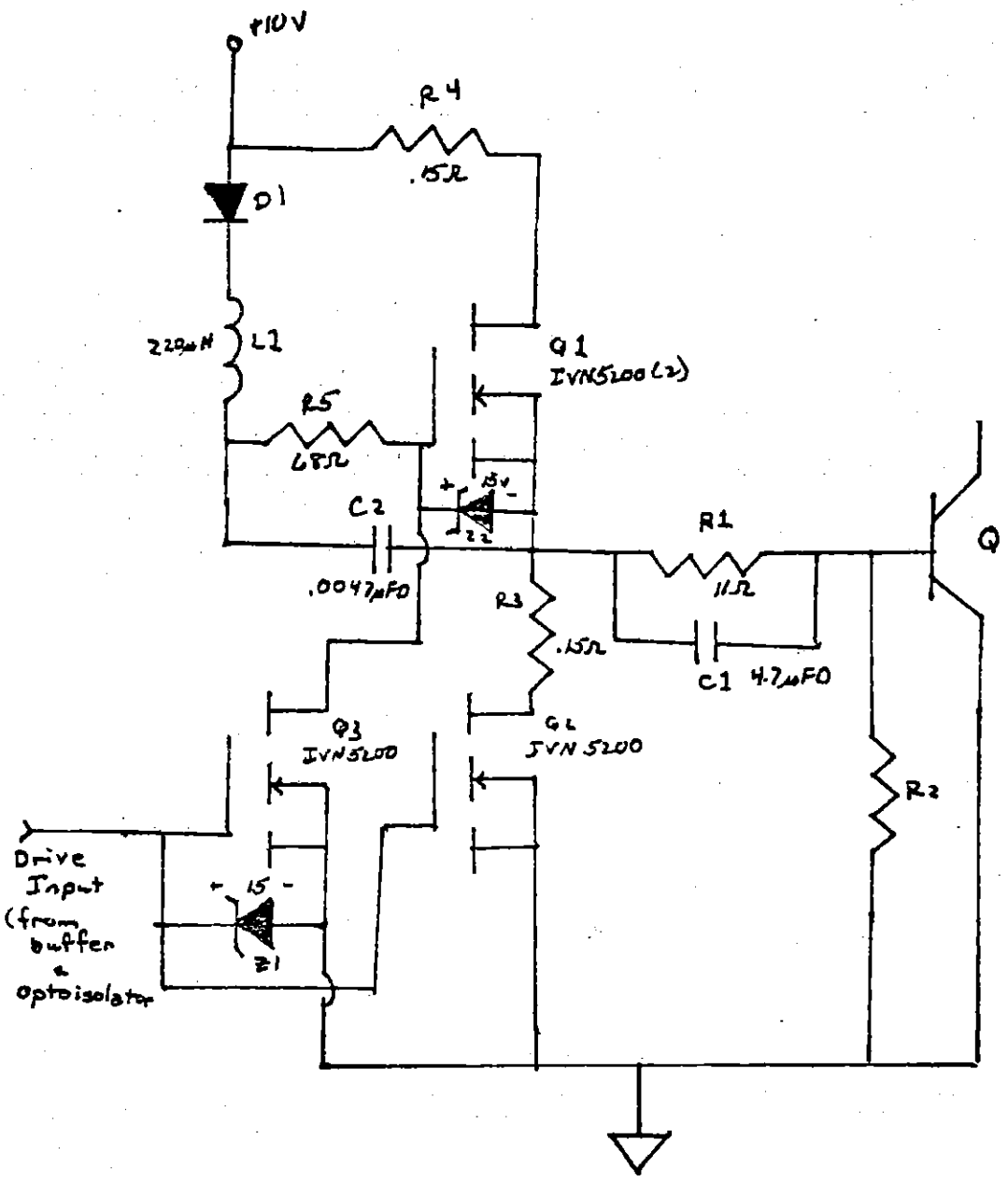


since this would reduce the turn-on current spike. A large inductance, however, results in voltage ring-up during turn off. The series inductance was selected at a compromise value of 1μH. This value of inductance causes a voltage ring-up of 73 volts at 16 amperes and limits the complementary parallel snubber charging current to 32 amperes. In order to provide safe parallel snubber recovery and the current limit peak switching frequency of 10 kHz, the snubber resistor, R1, was selected to be 20 Ω. This limits the self snubber discharge current to 18.2 amperes. The free wheeling diode reverse recovery current could be as high as 15 amperes. These numbers indicate that the transistor must conduct a current spike of as high as 72 amperes during turn on. On this basis, the Power Tech transistor, PT3523, was selected.

The drive circuitry, Fig. 33, is a relatively standard design. Small power mosfets, Q1-5, have been used to provide fast current switches with easy drive. A speed-up capacitor, C1, has been added to provide the base current spike necessary during turn-on. Each corner is optically isolated and each of the three upper corners requires a separate floating 10 volt supply.

The losses in this bipolar design occur in several places. There are two main types of losses - steady state losses and switching losses. The steady state losses occur in two places - the transistor "on" losses and the drive losses. The drive losses are caused by the continuous base current that must flow to keep the transistor saturated. Assuming a worst case saturation beta of 26 at a current of 16 amperes, the base drive

Fig. 33. Bipolar Drive Circuitry



was selected to be 0.7 amperes. This results in a continuous drive loss of 7 watts per phase. The "on" loss is the loss due to the saturation voltage drop of the transistor. The transistor has a saturation voltage drop of 0.2 volts. With a 9.5 Arms load current flowing, this results in an "on" loss of 1.9 watts per phase. The switching losses in the bipolar design are very significant. Using the drive scheme described above the switching time for the transistor can be as long as 3 μs. The switching loss can be calculated using the formula below.

$$P_{switch} = V_{BUS} I_{LOAD} f_{switch} t_{switch} / 3$$

At a frequency of 3600 Hz, with a switching time of 3 μs, a bus voltage of 300 volts and a load current of 9.5 Arms the switching losses for one phase would be 5.1 watts. The last major power loss is the power lost in the snubber resistor. This power can be calculated as shown below.

$$P_{snubber} = C_{snubber}(V_{BUS} + V_{RING})^2 f_{switch}$$

With a snubber capacitor of 0.047 μF, a bus voltage of 300 volts, a ring-up voltage of 73 volts and a switching frequency of 3600 Hz the snubber losses are 23.5 watts. Under the above conditions, the total losses for this design are 37.5 watts per phase.

4.2 Performance Comparison

The bipolar inverter circuit and the mosfet inverter circuit described above both accomplish the same task. To decide what the relative advantages and disadvantages of the two circuits are they can be compared in the areas of size, efficiency, cost, and reliability.

The physical sizes of the bipolar circuit and the mosfet circuit are tabulated in Tables V and VI respectively. As can be seen from these tables, the mosfet circuitry is significantly smaller. This is the result of two main factors. First of all, snubbers are not necessary for the safe operation of the mosfet circuit. This results in very substantial size savings since the snubber resistor and capacitor are very large. A second reason for the mosfet circuit being smaller is thatt the components in the mosfet driver are very small and do not have to be able to dissipate much power. The bipolar driver, in contrast, has several large power resistors and the large speed-up capacitor. The size advantage demonstrated here does not even take into account the fact that the bipolar design requires a significantly larger low level power supply. It can be seen from the tables that the mosfet design has in fact provided the significant reduction in size that had been desired.

Table V. Bipolar Circuit Size

FET, IVN5200	30@ .1075 in^2	3.225 in^2
Buffer, DS0026	3@ .1075 in^2	.323 in^2
15V zener, 1N965	18@ .018 in^2	.364 in^2
5V zener, 1N751	6@ .018 in^2	.108 in^2
4.7μF capacitor, 20V	6@ .683 in^2	4.098 in^2
0.1μF capacitor, 20V	12@ .82 in^2	.982 in^2
.15Ω resistor, 1 Watt	12@ .141 in^2	1.692 in^2
11Ω resistor, 12.5 Watts	6@ .859 in^2	5.154 in^2
20Ω resistor, 50 Watts	6@ 1.514 in^2	9.084 in^2
0.47μF capacitor, 400V polycarbonate	6@ .365 in^2	2.190 in^2
Diode, 6FL60	12@ .15 in^2	1.800 in^2
Transistor, PT3523	6@ .244 in^2	1.464 in^2
Subtotal		30.486 in^2
50% overhead		15.243 in^2
Total		45.727 in^2

Table VI. Mosfet Circuit Size

FET, IVN5200	3@ .1075 in^2	.323 in^2
Buffer, DS0026	3@ .108 in^2	.323 in^2
Transistor, 2N3439	3@ .1075 in^2	.323 in^2
Transistor, 2N3905	3@ .065 in^2	.195 in^2
15V zener, 1N965	9@ .018 in^2	.162 in^2
5V zener, 1N751	6@ .018 in^2	.108 in^2
Resistors, 1/4 Watt	12@ ..027 in^2	.324 in^2
Capacitor, 470pF	3@ .017 in^2	.051 in^2
Diode, 6FL60	12@ .15 in^2	1.800 in^2
Mosfet, IRF330	15@ 1.328 in^2	19.920 in^2
Subtotal		23.529 in^2
50% overhead		11.765 in^2
Total		35.294 in^2

A comparison of the losses and efficiency of the two circuits reveals several important differences. The power losses for the mosfet circuit can be determined as shown below.

$$P_{mosfet} = (1\text{-}k)P_{on} + kP_{fw} + P_{drive} + 2f_{switch}V_{BUS}Q_{switch}$$

In the above equation k is the fraction of time the current "free wheels", P_{on} is the "on" loss of the mosfets, P_{drive} is the power consumed in the drive, P_{fw} is the power dissipated in the "free wheeling" diode, and Q_{switch} is the effective switching charge.

$$Q_{switch} = I_{LOAD}t_{switch}/6$$

For the bipolar transistor the losses can be calculated from the following equation.

$$P_{bipolar} = (1\text{-}k)P_{on} + kP_{fw} + P_{drive} + 2f_{switch}V_{BUS}Q_{switch}$$
$$+ f_{switch}C_{snubber}(V_{BUS} + V_{RING})^2$$

The "free-wheeling" diode loss can be calculated assuming a forward drop of 1.5 volts. With a current of 9.5 Arms, this yields a loss of 12.8 watts. For the mosfet design the drive loss is 0.34 watts and in the bipolar design this loss is 8.0 watts. Assuming a 300 ns worst-case switching time for the mosfet circuit and a 3 μs worst-case switching time for the bipolar circuit, one can calculate a switching charge of 0.475 μC for the mosfet circuit and 4.75 μC for the bipolar circuit. The "on" losses for the mosfet circuit are 75.4 watts if the worst case selection of 2 IRF330s is assumed but can be as low as 54.8

watts for a single IRF350. In the following analysis it is assumed 2 IRF330s are being used. The "on" losses for the bipolar circuit are 1.9 watts.

The losses and efficiencies of the two circuits vary as the operating conditions vary. The efficiencies of the two circuits are compared below at three typical operating states. In the first state the bus voltage is 300 volts, the bus current is 9.5 Arms, the switching frequency is 3600 Hz, and the current is "free-wheeling" 50 per cent of the time. Under these conditions the mosfet circuit's losses are 45.2 watts per phase and the bipolar circuit's losses are 49.6 watts per phase. The corresponding efficiencies, assuming a load of 1645 watts, are 92.4% for the mosfet circuit and 91.7% for the bipolar circuit. This is probably the most typical operating condition for this application. A second operating state would have a bus voltage of 150 volts, a switching frequency of 400 Hz, a load current of 9.5 Arms and very little "free-wheeling" current flow. Under these conditions the mosfet circuit's losses would be 75.5 watts and the bipolar circuit's losses would be 11.1 watts. The corresponding efficiencies are 87.9% for the mosfet circuit and 98.0% for the bipolar circuit. A third operating condition would be that of current limit. Here one might find a bus voltage of 300 volts, a current of 11.0 Arms, a switching frequency of 8000 Hz and "free-wheeling" current 80 per cent of the time. Under these conditions the power losses are 27.4 watts for the mosfet circuit and 131.8 watts for the bipolar circuit. The corresponding efficiencies are 95.2% and 80.6%.

Several things can be noted from the above calculations. The most obvious fact is that the mosfet circuit operates better at high frequencies and the bipolar circuit operates better at low frequencies. This is as expected because the bipolar circuit's losses are dominated by switching losses while the mosfet circuit's losses are dominated by "on" losses. A second characteristic is that the mosfet circuit's efficiency improves as the amount of time the current "free-wheels" increases. This is due to the much lower forward drop of the "free-wheeling" diode as compared to the mosfet.

The parts cost for the bipolar circuit and the mosfet circuit are summarized in Tables VII and VIII. Although the cost of the bipolar circuit is very high, this is primarily due to attempts to reduce the circuit size. A somewhat larger snubber would allow the use of much cheaper transistors. Also, a somewhat larger, but much cheaper bipolar drive circuit could have been built by replacing the IVN5200 mosfets with small power transistors. Because small size was the primary design goal, these modifications were not implemented. In a less size-constrained application, these changes would probably be made. If these changes were made, the bipolar design would probably be cheaper than the mosfet design as a result of the expense of the power mosfets. It is unlikely if the percentage cost differential would be large owing to the relatively large cost of the bipolar drive components.

Table VII. Bipolar Circuit Cost

FET, IVN5200	30@ $7.40	$220.00
Buffer, DS0026	3@ $7.00	$21.00
15V zener, 1N965	18@ $.54	$9.72
5V zener, 1N751	6@ $.41	$2.46
4.7μF capacitor, 20V	6@ $.80	$4.80
0.1μF capacitor, 20V	12@ $.78	$9.36
.15Ω resistor, 1 Watt	12@ $1.23	$14.76
11Ω resistor, 12.5 Watts	6@ $2.57	$15.42
20Ω resistor, 50 Watts	6@ $3.15	$18.90
0.47μF capacitor, 400V polycarbonate	6@ $9.47	$56.82
Diode, 6FL60	12@ $8.12	$97.44
Transistor, PT3523	6@ $149.00	$894.00
Total		$1366.68

Table VIII. Mosfet Circuit Size

FET, IVN5200	3@ $7.40	$22.20
Buffer, DS0026	3@ $7.00	$21.00
Transistor, 2N3439	3@ $1.65	$4.95
Transistor, 2N3905	3@ $.50	$1.50
15V zener, 1N965	9@ $.54	$4.86
5V zener, 1N751	6@ $.41	$2.46
Resistors, 1/4 Watt	12@ $.38	$4.56
Capacitor, 470pF	3@ $.75	$2.25
Diode, 6FL60	12@ $8.12	$97.44
Mosfet, IRF330	15@ $28.00	$420.00
Total		$581.22

Because of the limited experience with the operation of these two circuits it is difficult to say anything substantive about the reliability of the two circuits. Although both bipolar transistors and power mosfets have weaknesses, the circuit designs take these into account and should protect the devices from overvoltage in the power mosfet circuit and secondary breakdown in the bipolar transistor circuit. Due to their recent development, little is known about the long-term reliability of power mosfets. The smaller number of parts in the mosfet circuit should lend somewhat of a reliability advantage to that circuit, but this is mitigated by the lack of experience with power mosfet circuits.

5. Summary and Conclusions

A working, three-phase, mosfet inverter has been designed and constructed to meet the requirements of the application described in the first chapter. Paralleled power mosfets have been successfully employed to provide circuit operation at currents larger than the capability of a single mosfet. The performance of the mosfet design was compared with that of a relatively conventional bipolar circuit, designed for the same application.

Several interesting observations resulted from this comparison. First, the necessity of low frequency operation enabled the mosfet design to successfully compete with a bipolar design in terms of size. At higher frequencies a transformer-coupled, porportional-base-drive topology would have made possible a very small bipolar design. As the frequency of operation becomes very low, however, the efficiency of the power mosfet design becomes much worse than that of the bipolar design. At operating frequencies between several hundred Hertz and several thousand Hertz the mosfet design has the largest advantag. At these frequencies, the efficiency of the mosfet design is equal to that of the bipolar design and the size advantage of the mosfet design is significant.

Another significant advantage of the mosfet design over the bipolar design is in the area of low-level power supply requirements. The bipolar design required three floating ten volt, eight watt supplies and a non-floating ten volt, 24 watt supply. The mosfet design requires only a non-floating supply and consumes less than two watts. The bulk of the power is consumed by the buffer used to interface with the low-power control circuits.

A cost comparison of the two designs reveals that although mosfets are more expensive than bipolar transistors, the cost of the associated drive components renders this difference insignificant. In fact, if efforts are made to reduce the size of the bipolar design as were made in the design presented above, the resulting bipolar design can be significantly more expensive than the mosfet design. Little can be said about the relative reliability of the two designs until more experience with mosfet designs is obtained.

In conclusion, the power mosfet design offers a significant advantage over a bipolar transistor design in a size-constrained, low-frequency, medium-power application. This size advantage comes with little or no penalty in the areas of cost and efficiency. The relative reliability of the two designs is still uncertain due to the recent advent of power mosfets.

Several areas of future research have been indicated by the above work. Two particularly stand out. Furthur development of the opticall-isolated drive topology, Topology V, would be very interesting as this drive design seemed very competitive with the drive actually developed. Also research into improving the characteristics of the internal "free-wheeling" diode in the power mosfets would be very important as it would greatly increase their utility in power switching applications. In general much work remains to be done in exploring the applicationsof power mosfets in switching applications. Their differences from bipolar transistors promise the possibility of their use in a wide range of applications.

6. References

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