A MEMS-Based Precision Operational Amplifier

by

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Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

Masters of Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2004

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Abstract

Two main difficulties for amplifiers that attempt to make precision DC measurements are the inherent low-frequency noise of the amplifier and the leakage current of the amplifier input stage. This thesis presents a novel fully integrated operational amplifier design that addresses both measurement limitations by using a fully differential mechanical transductor input stage, fabricated using SOI-MEMS technology.

The input stage of the amplifier is a MEMS structure that provides a variable capacitance to transduce a low-frequency input voltage into a high-frequency AC current. This up-modulation of the input signal is exploited to reduce offsets and low-frequency noise, and the dielectric isolation of the MEMS structure provides high input impedance and low leakage currents.

To function, the MEMS-based amplifier includes two co-dependent feedback loops. The 'drive loop' utilizes closed-loop control to vibrate the MEMS structure at its mechanical resonant frequency to produce a modulating capacitance. The 'sense loop' senses the up-modulated signal from the MEMS structure, and provides gain and demodulation to this signal. Global feedback around the sense loop allows for accurate measurement of the input voltage.

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Contents

Chapter 1

Introduction

1.1 Design Objectives

The goal of this thesis is to design an amplifier that can accurately measure small differential voltages and provide a single-ended output. The MEMS-based amplifier designed in this work may be used either as an instrumentation amplifier for true differential input voltage measurements, or in a feedback configuration as an operational amplifier, as illustrated in Figure 1-1.

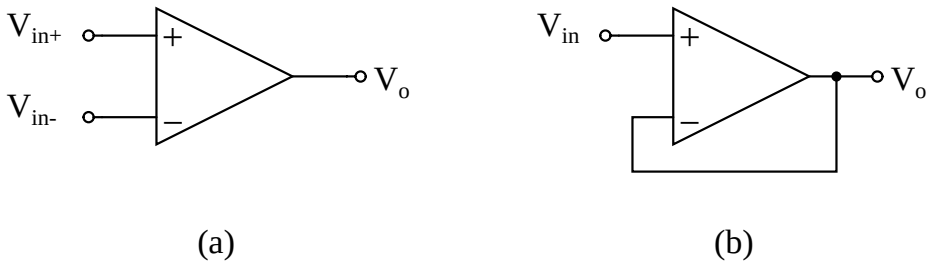

Figure 1-1: The MEMS-based amplifier may be configured as an instrumentation amplifier (a) or an operational amplifier (b).

Desirable characteristics for a precision amplifier include the following. The amplifier should have a large input common-mode voltage range, so that it can measure small voltage differences riding on arbitrary common-mode voltages. The amplifier gain ought to be independent of this common-mode voltage at the input, so it

must have a large common-mode rejection ratio. The gain of the amplifier should be well-known and consistent to provide reliable and accurate amplification to its input voltages. It is also desirable for the amplifier to have minimum leakage current, offset, and drift. The leakage currents of an amplifier generally provide bias to its input stage, and the amplifier offset voltage is defined as the differential input voltage that must be applied to drive the amplifier output to zero. Both can introduce an error between the input voltage and its measurement, and this error may change with temperature. In addition, the inherent noise of the amplifier limits the minimum detectable signal, so the amplifier should be as low-noise as possible. Ideally, the amplifier also ought to have large bandwidth, so it can measure signals with high frequency content.

As with all designs, trade-offs must be made among the amplifier qualities to accomodate the performance requirements of a particular application, and the key trade-off for the MEMS-based amplifier lies in its bandwidth. In exchange for low offset and leakage current, the intended bandwidth of the MEMS-based amplifier is about 1.5kHz. Thus, this amplifier is suited for precision measurements of signals with low-frequency content. Target applications include physical sensors such as thermocouples, pH meters, and strain gauges, which have measurement variables that change slowly due to the nature of their inherent physical and chemical mechanisms.

The available supply voltages for the MEMS-based amplifier are 0, 5, and 10V, and it is desired that the amplifier uses less than 4mA of total current to function. The amplifier should also function over a temperature range from -40°C to 105°C. The design specifications for the MEMS-based amplifier are summarized in Table 1.1.

1.2 Design Challenges

Amplifiers that attempt to make precision low-frequency measurements face two primary difficulties [1]. One problem is the inherent noise of the amplifier interfering with measurements. The other issue is the leakage current of the amplifier, which limits the resolution of small input signals.

Key Specifications	
Common-Mode Range	$\pm$100V
CMRR	$>$ 100dB
Gain Error ($A_v = 1$)	0.001
Gain Non-linearity ($A_v = 1$)	5ppm
Input-referred offset	$< 20\mu$V
Input-referred drift	< 50nV/°C
Input-referred noise	3μV RMS, 10Hz
Input leakage current (DC)	$<$ 10pA
Available suppy voltages	0V, 5V, 10V
Total Supply Current	$<$ 4mA
Temperature Range	-40 – 105°C

Table 1.1: Target design specifications for the MEMS-based amplifier.

1.2.1 Noise

The currents and voltages of the devices in an amplifier experience random variations about their average values. These random variations are referred to as noise, and are caused by different physical factors affecting the movement of electrons [2]. Thermal noise is due to the random thermal motion of electrons and depends on the absolute temperature. Shot noise occurs because the passage of an electron across a potential energy barrier is a random event, and depends on the DC bias current. Flicker or $1/f$ noise is due to crystalline defects in a device which randomly trap and release carriers.

While the spectral densities of thermal and shot noise are white and broadband, the spectral density of flicker noise is inversely proportional to frequency. The noise spectral density of an amplifier with thermal, shot, and flicker noise components is illustrated in Figure 1-2. The frequency f_n, where the flicker noise and white noise contributions are equal, is called the noise corner frequency. Due to the frequency characteristic of flicker noise, small low-frequency input voltages are quickly overwhelmed.

However, observing Figure 1-2, it can be noted that for the same measurement bandwidth, low-frequency measurements are affected by much more noise than measurements of signals above the noise corner frequency. This suggests that one possible

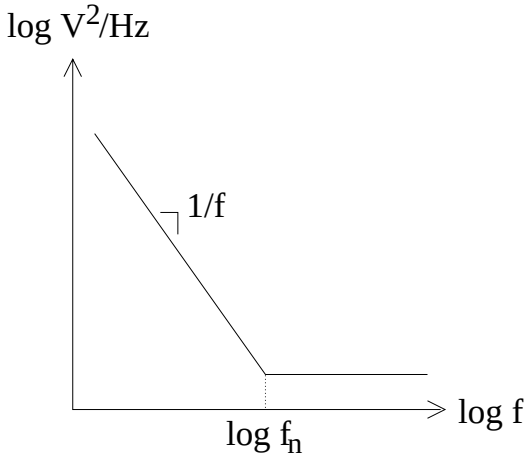

Figure 1-2: Noise spectral density as a function of frequency of an amplifier with thermal, shot, and flicker noise.

low-noise DC measurement technique is to translate the signal to a higher frequency before amplifying it with an inherently noisy circuit.

1.2.2 Leakage Current

Another error source that is of concern is the bias currents of the amplifier inducing offsets and noise. These bias currents are particularly problematic in the measurement of small voltage signals with a large source resistance, as illustrated in Figure 1-3. Typical leakage currents for amplifiers with MOSFET, JFET, and bipolar input stages are discussed in [1].

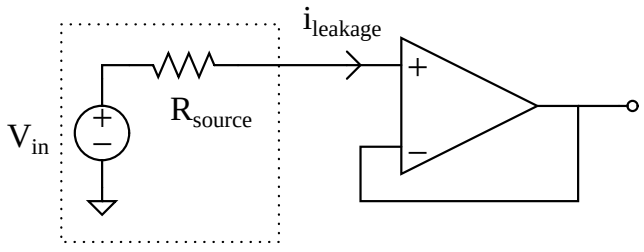

Figure 1-3: Effect of leakage current on an input signal with a large source resistance.

1.3 Principle of Operation

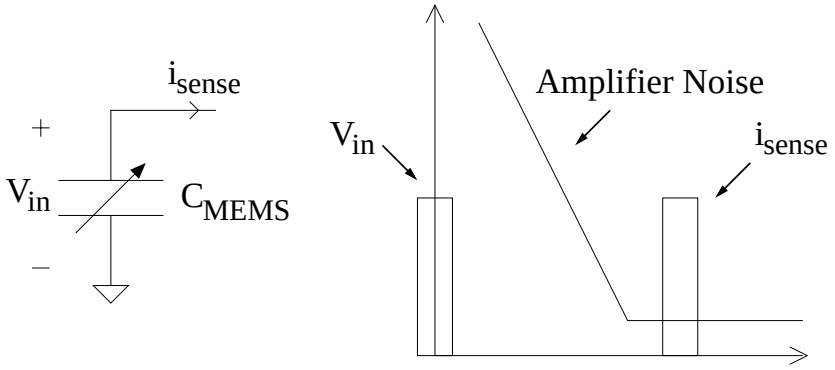

Figure 1-4: Principle of operation.

Both measurement difficulties are addressed by utilizing a MEMS-based input stage that acts as a capacitive transducer [1], [3]. The principle of operation is illustrated in Figure 1-4. The MEMS structure is essentially two capacitor plates, one of which can move to vary the overlap area. The MEMS structure varies this overlap to produce a sinusoidally varying capacitance:

$$C(t) = C_m \sin(\omega_m t).$$

A DC voltage on such a capacitor creates a current signal, i_{sense}:

$$i_{sense} = C_{\text{MEMS}} \frac{dV_{in}}{dt} + V_{in} \frac{dC_{\text{MEMS}}}{dt} = 0 + V_{in}(C_m \omega_m \cos(\omega_m t)).$$

This induced current is at the frequency of the capacitance modulation, and its amplitude is proportional to the input voltage. Thus, the MEMS structure effectively provides amplitude modulation. If the frequency of modulation ω_m is above the $1/f$ corner frequency of the amplifier noise, and if the input signal is sufficiently bandlimited, the input signal and the low-frequency noise of the amplifier do not share bandwidth. The AC sense current can be amplified and demodulated back to DC, and the resulting output is a noise-reduced DC measurement of the input.

The fundamental concept of this design is to up-modulate the input before noise

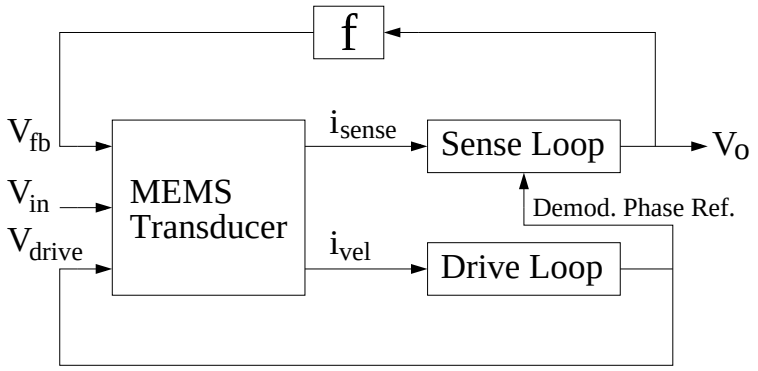

Figure 1-5: System overview.

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is added to the signal. Therefore, the up-modulator itself should not have inherent noise. In theory, capacitors are noiseless systems, so the up-modulation of the input voltage does not introduce noise into the signal bandwidth.

Furthermore, as a fundamentally capacitive technique, no DC current should be drawn from the input voltage source. The MEMS structure also has dielectric isolation trenches so that its capacitive plates have extremely low leakage currents over a wide range of temperatures, and a fully differential transducer further reduces the current drawn from the input source. Although the input bandwidth is constrained, this amplifier is well suited for low-frequency precision measurement applications.

1.4 System Overview

An overview of the MEMS-based amplifier system is illustrated in Figure 1-5. To function, the MEMS-based amplifier uses two co-dependent feedback loops [4]. The 'drive loop' utilizes closed-loop control to vibrate the MEMS structure at a constant frequency to produce a time-varying capacitance. The rate of capacitance modulation is measured through a velocity current signal, and the drive loop controls the vibration of the MEMS structure accordingly. The time-varying capacitance allows the MEMS structure to transduce a DC input voltage into an AC current. The 'sense loop' picks-off this up-modulated sense current from the MEMS structure, and provides gain and

demodulation to this signal. The output of the sense loop is fed back to the MEMS transducer to provide accurate gain to the input.

1.5 Thesis Outline

Chapter 2 is an overview of the MEMS sensor. It discusses the structure of the MEMS transducer to provide a variable capacitance and to interact with the drive and sense loops. The mechanical and simulation models used to estimate the behavior of the MEMS structure are presented, and the design specifications for the MEMS transducer are calculated.

Chapter 3 discusses the drive loop. The need for closed-loop control of the capacitance modulation is motivated and the feedback loop is analyzed. Other design considerations of the drive loop are introduced, and the circuits implementing the drive loop signal chain are presented. The chapter concludes with simulated results showing agreement with theory.

Chapter 4 details the sense loop. The need for feedback in the sense loop is motivated, and the open loop transfer function of the sense loop is analyzed to estimate the closed-loop behaviour of the system. Design considerations for the noise and offset performance of the overall system are discussed, and the design of the sense loop signal chain is presented. The noise and offset of the system are then analyzed, followed by simulated results to confirm the calculations.

Chapter 5 summarizes the design efforts of this thesis, and concludes with a discussion of future work and potential design improvements.

Chapter 2

MEMS Transducer

2.1 Motivation

The MEMS transducer is the input stage of the MEMS-based amplifier. It serves as a mechanical transconductor that transduces the low-frequency voltage input into a high-frequency current signal to achieve lower noise and offset performance for the overall amplifier. The following sections describe the design of the MEMS structure to function as such a transducer and to provide the desired inputs and outputs for the drive and sense loops. A mechanical model of the MEMS structure is also presented, and this chapter concludes with the behavioral model of the transducer used in the simulation of the MEMS-based amplifier.

2.2 Structure Design

2.2.1 Overlap Area Modulation

The MEMS structure creates a modulating capacitance by varying the overlap area between two capacitor plates, as illustrated in Figure 2-1. One plate is mechanically fixed, and the other is free to displace. The amount of overlap is represented by x, the height of the plates is h, and the gap between the plates is g. The capacitance of the MEMS structure is

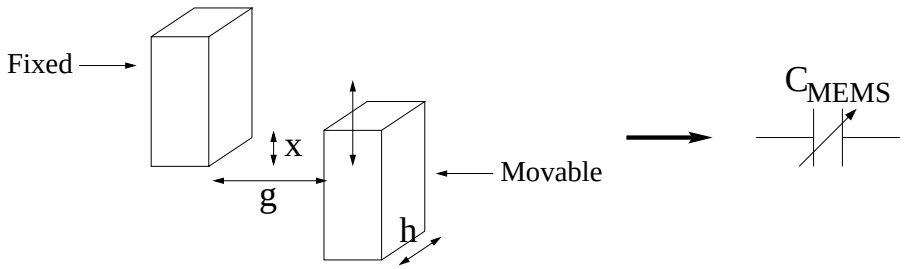

Figure 2-1: Modulating the capacitance by varying the overlap area.

$$C_{\text{MEMS}} = \frac{\epsilon_o h}{g} x,$$

where x is a time-varying quantity:

$$x = x_o + x_m \sin(\omega_m t).$$

The MEMS capacitance can be expressed as

$$C_{\text{MEMS}} = \frac{\epsilon_o h}{g} x_o + \frac{\epsilon_o h}{g} x_m \sin(\omega_m t) = C_o + C_m \sin(\omega_m t),$$

where C_o represents the static capacitance of the MEMS structure, and C_m is the magnitude of the capacitance modulation.

The MEMS transducer consists of a series of fixed plates that interact with one common moving beam. As discussed in Section 1.4, for the two feedback loops, the MEMS transducer must have four input/output plates. The sense loop must have plates for the input voltages, and plates for the feedback voltages. The up-modulated current signal is picked-off from the moving beam. The drive loop must have plates to apply electrostatic forces to move the beam, and plates to measure the velocity of the movement.

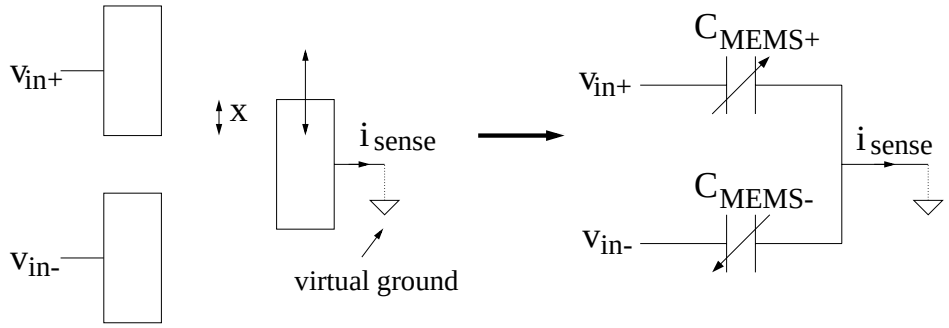

Figure 2-2: Input capacitor plates of the MEMS transducer.

2.2.2 Input Plates

The pair of plates to accomodate differential input voltages for the sense loop is illustrated in Figure 2-2. The two plates connected to the input voltages are mechanically fixed, and the moving beam is assumed to be biased at a virtual ground. The two fixed plates see the same magnitude of capacitance modulation but with opposite phases:

$$C_{\text{MEMS+}} = C_o + C_m \sin(\omega_m t)$$

$$C_{\text{MEMS-}} = C_o - C_m \sin(\omega_m t).$$

The induced signal current on the moving beam is given by

$$\begin{aligned} i_{sense} &= v_{in+}\frac{dC_{\text{MEMS+}}}{dt} + v_{in-}\frac{dC_{\text{MEMS-}}}{dt} \\ &= (v_{in+} - v_{in-})C_m\omega_m \sin(\omega_m t). \end{aligned}$$

Thus, the MEMS transducer rejects the common mode component of the input voltages, and amplitude-modulates the differential component to the capacitance modulation frequency. In practice, the common mode suppression is limited to the matching of the modulation capacitances, which is approximately -60dB [5].

2.2.3 Feedback Plates

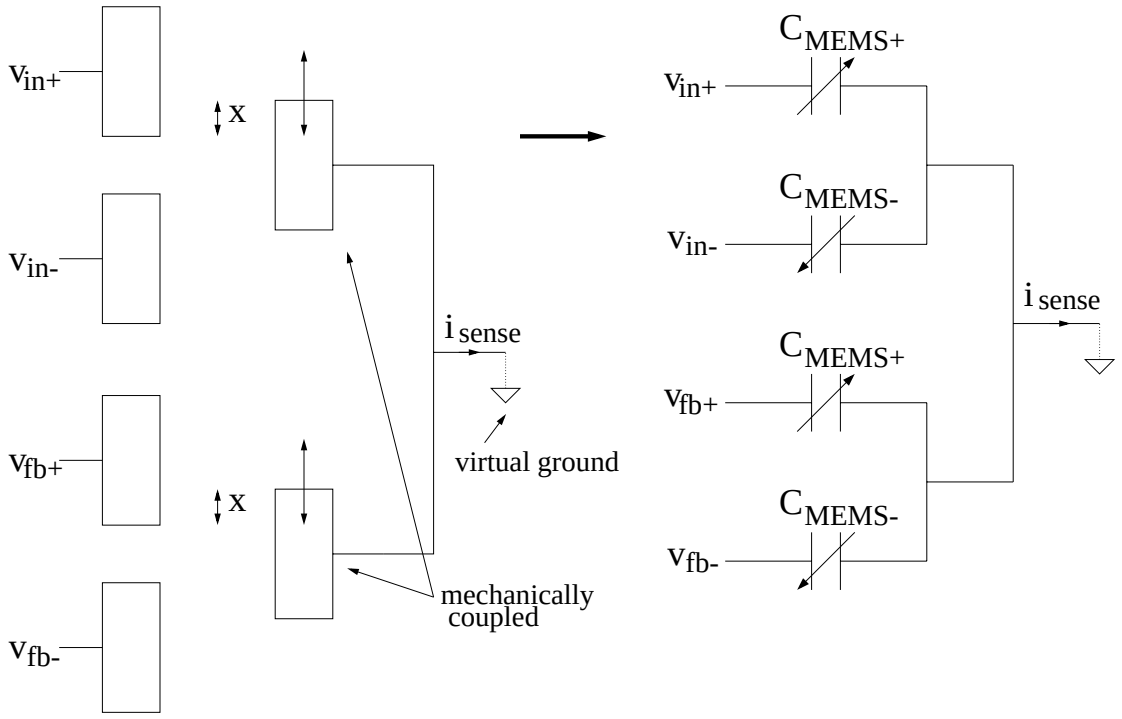

Figure 2-3: Input and feedback capacitor plates of the MEMS transducer.

Feedback in the MEMS-based amplifier can be accomplished by feeding the output of the sense loop back to one of the input plates, as a classic operational amplifier feedback topology. Alternatively, for an instrumentation amplifier topology with true differential inputs, the output may be connected to one of the feedback plates, which are an additional pair of fixed capacitor plates interacting with the moving beam, as illustrated in Figure 2-3. The induced current on the moving beam is now

$$i_{sense} = ((v_{in+} - v_{in-}) + (v_{fb+} - v_{fb-}))\, C_m \omega_m \sin(\omega_m t).$$

Such a feedback configuration allows for complete isolation of the input terminals, and the input common-mode voltage range is no longer constrained by the supply rails of the amplifier, but is limited instead by the breakdown voltage of the isolation trenches [1].

2.2.4 Force Drive Plates

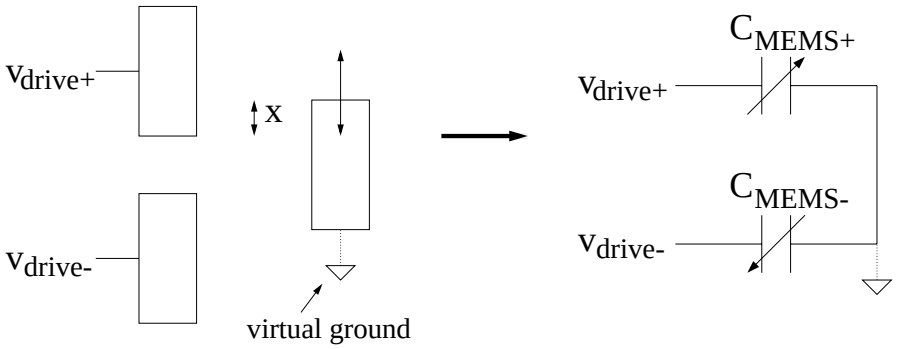

Figure 2-4: Capacitor plates for the electrostatic force drive of the MEMS transducer.

The moving beam of the MEMS structure is actuated by electrostatic forces induced by applied voltages, as illustrated in Figure 2-4. For voltages V_{drive+} and V_{drive-} on the fixed plates, the attractive force acting on the moving beam is given by the gradient of the energy stored. The two MEMS capacitances are

$$\begin{aligned} C_{\text{MEMS+}} &= \frac{\epsilon_o h}{g} x = \frac{\epsilon_o h}{g}(x_o + x_m \sin(\omega_m t)) \\ C_{\text{MEMS-}} &= \frac{\epsilon_o h}{g}(x_o - x_m \sin(\omega_m t)) = \frac{\epsilon_o h}{g}(2x_o - x). \end{aligned}$$

Thus, assuming that the moving beam is at a virtual ground of 0V, the force experienced by the beam is

$$\vec{F} = -\vec{\nabla}(\frac{1}{2} C_{\text{MEMS+}} V_{drive+}^2 + \frac{1}{2} C_{\text{MEMS-}} V_{drive-}^2).$$

Because only one direction of movement is possible, the energy gradient simply reduces to

$$\begin{aligned}\vec{F} &= -\frac{\partial}{\partial x}(\frac{1}{2}C_{\text{MEMS}+}V_{drive+}^2 + \frac{1}{2}C_{\text{MEMS}-}V_{drive-}^2)\hat{x} \\ &= -\frac{1}{2}\frac{\epsilon_o h}{g}(V_{drive+}^2 - V_{drive-}^2)\hat{x}.\end{aligned}$$

For a square wave voltage drive between E_o and 0, the induced force is also a square wave between

$$\vec{F} = \pm\frac{1}{2}\frac{\epsilon_o h}{g}E_o^2\hat{x}.$$

2.2.5 Velocity Pick-Off Plates

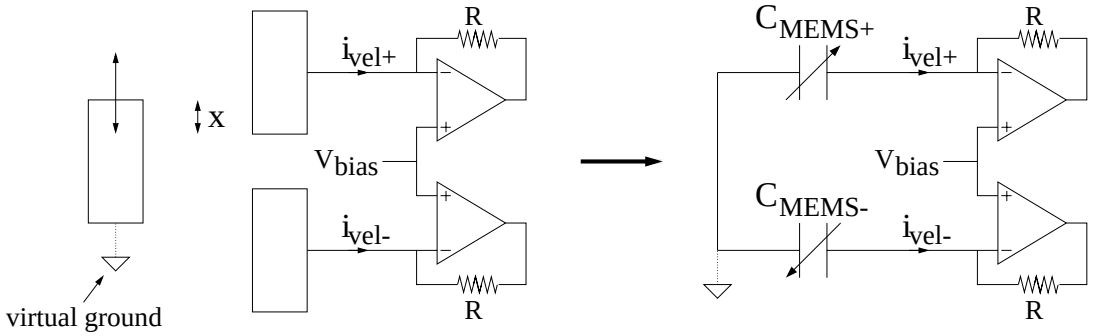

Figure 2-5: Capacitor plates for measuring the velocity of the moving beam of the MEMS transducer.

The velocity of the moving beam is measured through another set of fixed plates, illustrated in Figure 2-5. Transresistance amplifiers bias the fixed plates at V_{bias}. The displacement of the moving beam induces current signals on the fixed plates:

$$\begin{aligned}i_{vel+} &= V_{bias}\frac{dC_{\text{MEMS}+}}{dt} = V_{bias}\frac{\epsilon_o h}{g}\frac{dx}{dt} \\ i_{vel-} &= V_{bias}\frac{dC_{\text{MEMS}-}}{dt} = -V_{bias}\frac{\epsilon_o h}{g}\frac{dx}{dt},\end{aligned}$$

assuming that the moving beam is at a virtual ground of 0V. The currents are proportional to the velocity of the moving plate, as desired.

2.2.6 Fully Differential Transducer

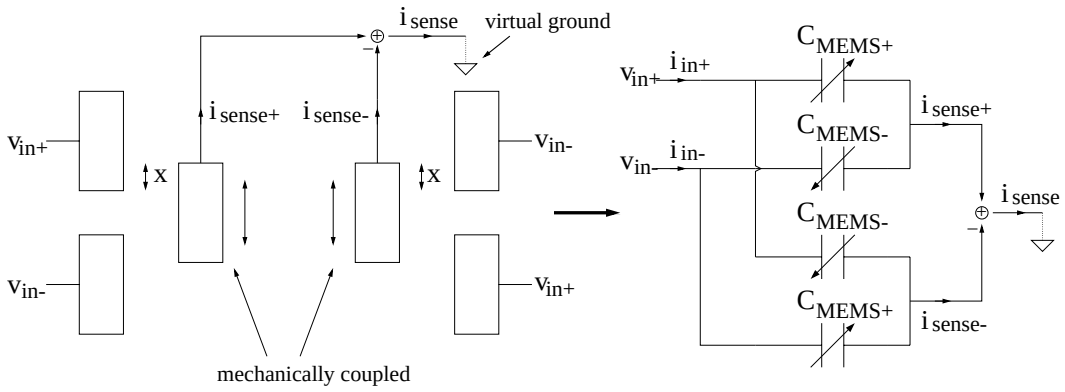

Figure 2-6: Fully differential transducer to eliminate dynamic current drawn from the source.

The input voltage is sensed capacitively, which implies that no DC current should be drawn from the input source. However, because the input capacitor is time-varying, the source must supply an AC current in order to maintain the voltage at the input plates as the MEMS capacitance modulates. To eliminate this dynamic current, the net input capacitance seen by the source should appear static. This is accomplished by the fully differential transducer shown in Figure 2-6. Each voltage source now sees two capacitors modulating out of phase in parallel:

$$\begin{aligned} C_{in+} = C_{in-} &= C_{\text{MEMS}+} + C_{\text{MEMS}-} \\ &= (C_o + C_m \sin(\omega_m t)) + (C_o - C_m \sin(\omega_m t)) = 2C_o. \end{aligned}$$

The sense current is now given by

$$\begin{aligned} i_{sense+} &= v_{in+}\frac{dC_{\text{MEMS}+}}{dt} + v_{in-}\frac{dC_{\text{MEMS}-}}{dt} = (v_{in+} - v_{in-})C_m\omega_m \sin(\omega_m t) \\ i_{sense-} &= v_{in+}\frac{dC_{\text{MEMS}-}}{dt} + v_{in-}\frac{dC_{\text{MEMS}+}}{dt} = -(v_{in+} - v_{in-})C_m\omega_m \sin(\omega_m t) \\ i_{sense} &= i_{sense+} - i_{sense-} = 2(v_{in+} - v_{in-})C_m\omega_m \sin(\omega_m t). \end{aligned}$$

The current drawn from each of the inputs is

$$\begin{aligned} i_{in+} &= v_{in+}\frac{dC_{\text{MEMS+}}}{dt} + v_{in+}\frac{dC_{\text{MEMS-}}}{dt} = 2v_{in+}\frac{dC_o}{dt} = 0 \\ i_{in-} &= v_{in-}\frac{dC_{\text{MEMS-}}}{dt} + v_{in-}\frac{dC_{\text{MEMS+}}}{dt} = 2v_{in-}\frac{dC_o}{dt} = 0, \end{aligned}$$

as desired. In practice, the dynamic current drawn from the source is limited by the matching of the MEMS capacitances, which suppresses this current by three orders of magnitude. Another advantage of the fully differential transducer is the rejection of unwanted common mode voltages in the signal chain, such as clock feedthrough. This will be discussed in further detail in Chapter 4.

2.2.7 Complete MEMS Structure

The complete fully differential MEMS transducer is shown in Figure 2-7. The shaded areas represent the moving beam, and the non-shaded areas are the fixed plates. The fixed plates have multiple fingers overlapping with the moving beam, which effectively create parallel capacitances to increase the total modulating capacitance. The capacitance C_{MEMS} of the previous analysis can be considered the capacitance between one finger of the fixed plate with the moving beam, so for N fingers, the effective capacitance simply scales to NC_{MEMS}. The input, feedback, drive, and velocity pick-off plates have N_{input}, N_{fb}, N_{drive}, and N_{vel} fingers, respectively.

The bottom half of the MEMS structure is used by the drive loop to apply the electrostatic forces that vibrate the moving beam and to measure the resulting beam velocity. The moving beam in the bottom half of the transducer is mechanically coupled to the two moving beams in the upper half so that all three beams vibrate together. The vibration of the upper two moving beams transduces the input and feedback voltages into a differential AC sense current.

The sense loop detects this current signal, and amplifies and demodulates it. Since the frequency of vibration and the frequency of up-modulation are the same, the phase reference for the demodulator can be derived from the force signal in the drive loop.

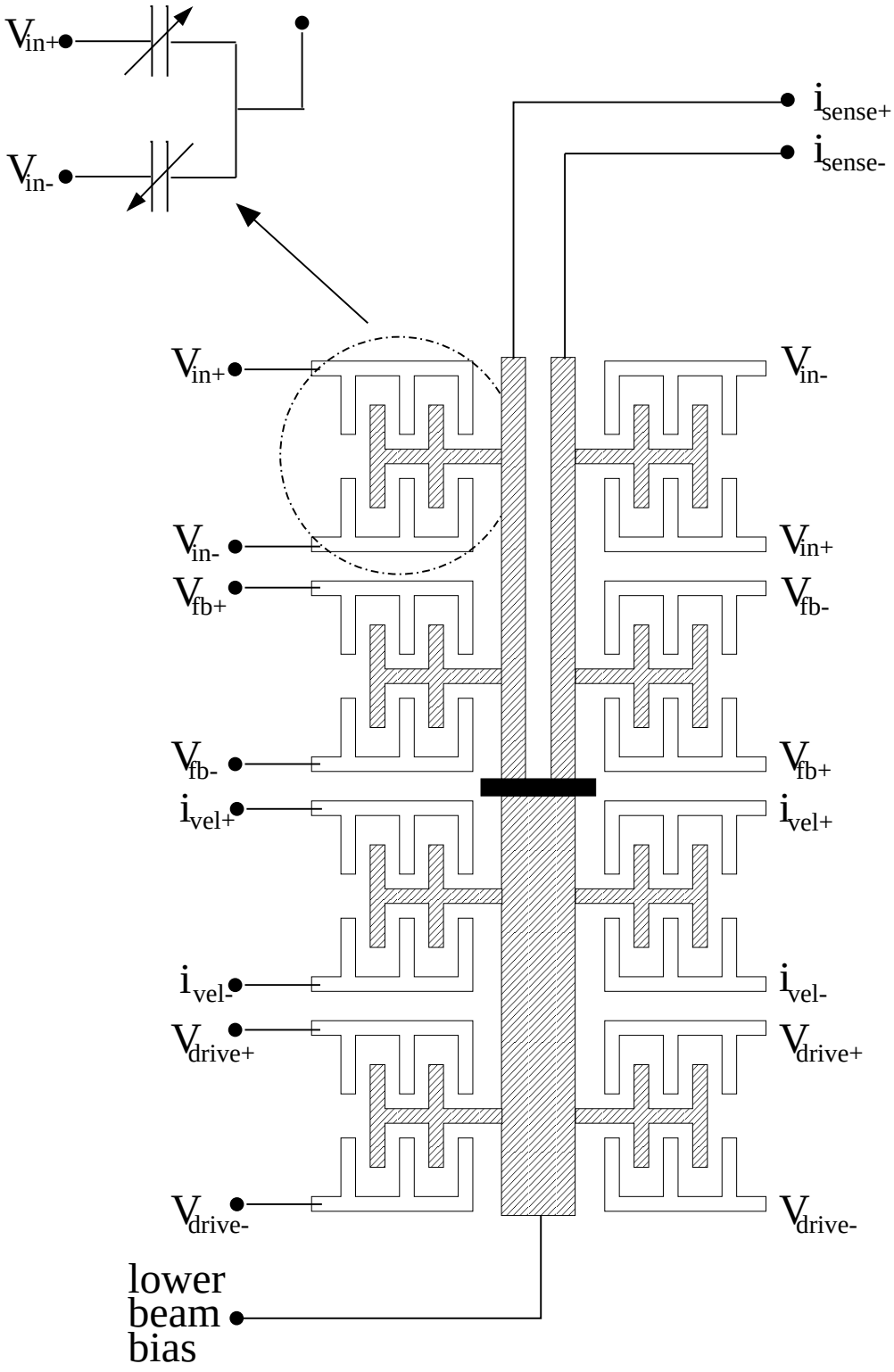

Figure 2-7: Complete MEMS transducer.

Although the three moving beams are mechanically coupled so they maintain phase coherency, they are electrically isolated from each other and can be biased to independent voltages. The moving beam in the bottom half of the structure should be biased to maximize both the electrostatic force drive and the induced velocity current signal. The square-wave drive voltages to actuate the MEMS beam are 0V and 10V, and the magnitude of the resulting electrostatic forces are maximum when the moving beam is biased to either 0V or 10V. The velocity plates are biased at 1.5V, so the bottom moving beam is chosen to be biased at 10V for a larger induced velocity current signal. The two moving beams in the upper half of the MEMS transducer must be biased to be in the linear range of the first sense loop circuit.

2.2.8 Parasitic Capacitance

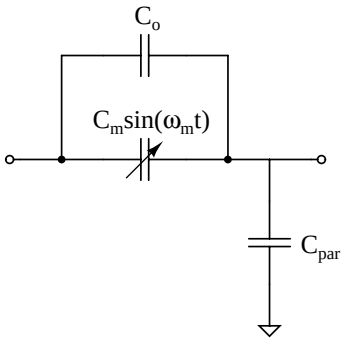

Figure 2-8: Model of the MEMS structure capacitances.

In addition to the static and modulating capacitances of the MEMS structure, there is also a parasitic capacitance to ground at the output terminals of the MEMS transducer, due to the capacitance of the dielectric isolation trenches and other process details [1]. This is illustrated in Figure 2-8. The parasitic capacitance C_{par} is about 1pF for the structures used in this SOI process.

2.2.9 Input Common-Mode Voltage Range

Observing Figure 2-7, it can be seen that the interleaving of the fixed and moving fingers of the transducer create other capacitances besides the primary overlap

capacitance. While one edge of the moving fingers forms a overlap-modulated capacitance with the fixed plate, its perpendicular edge simultaneously forms a small gap-modulated capacitance. This small but non-zero capacitance also stores energy and creates a force gradient perpendicular to the desired direction of motion which can potentially collapse the moving beam towards the fixed fingers. Thus, the presence of these secondary capacitances limit the input common-mode voltage range of the MEMS structure. In addition, the dielectric isolation trenches include nitride films that break down beyond their maximum supportable electric fields. This also presents an upper limit on the common-mode voltage range. With appropriate design, the transducer can stand-off a common-mode voltage up to about 200V [1].

2.3 MEMS Frequency Response

The displacement of the moving beam resulting from an arbitrary electrostatic force drive can be approximately modeled as a simple mass-spring-damper system:

$$F = m\ddot{x} + b\dot{x} + kx,$$

where m, b, and k represent, respectively, the effective mass, damping, and restoring-force constants of the MEMS structure. The transfer function can be represented in the frequency domain via a Laplace transform:

$$\frac{X}{F}(s) = \frac{1}{ms^2 + bs + k}.$$

The nature of overlap area modulation results in a system with very little damping, and the transducer is expected to have a high quality factor of about 450, with the frequency of resonance at roughly 15kHz [1]. Figure 2-9 illustrates the anticipated frequency response.

Because the transduced sense current from the MEMS structure is proportional to its change in capacitance, a large displacement improves the magnitude of the signal.

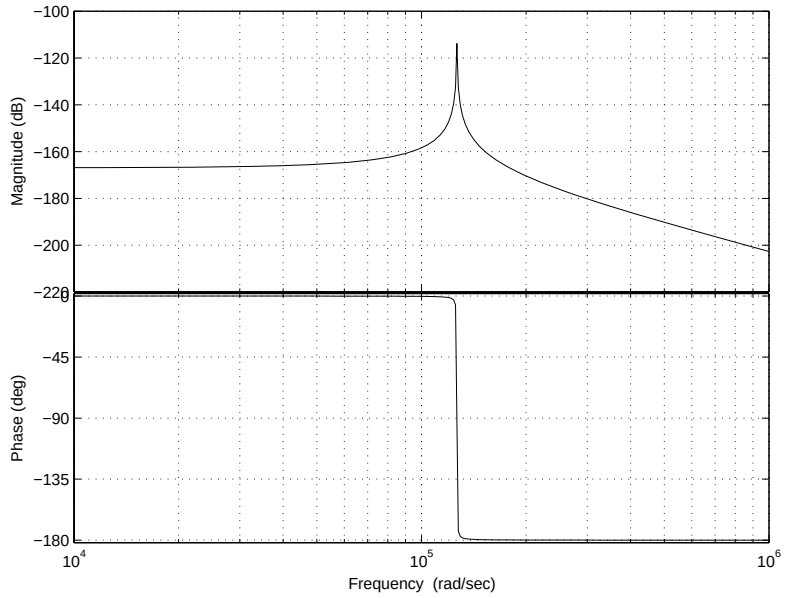

Figure 2-9: Ideal force-to-displacement frequency response of the MEMS transducer.

However, large voltages necessary to actuate large force drives can capacitively couple into the sense loop through stray parasitics, interfering with the sensing of small signals. Therefore, to optimize the sensitivity of the MEMS-based amplifier, it is desirable to vibrate the moving beam at its mechanical resonant frequency, where its displacement is maximum for a given amplitude of voltage drive.

2.4 ADICE Model For MEMS Transducer

Figure 2-10 illustrates the behavioral model for the MEMS transducer initially developed by [1] for simulation in ADICE. The ADICE symbol of this model is shown in Figure 2-11. The parameters for the MEMS transducer were modified for use in this thesis, and the values used are listed in Table 2.1. Using these values, the specifications for the MEMS transducer are calculated from the equations derived in the previous sections, and summarized in Table 2.2. The calculated values for i_{vel}, x_m, and C_m assumed that the MEMS structure is vibrating at its mechanical resonant frequency.

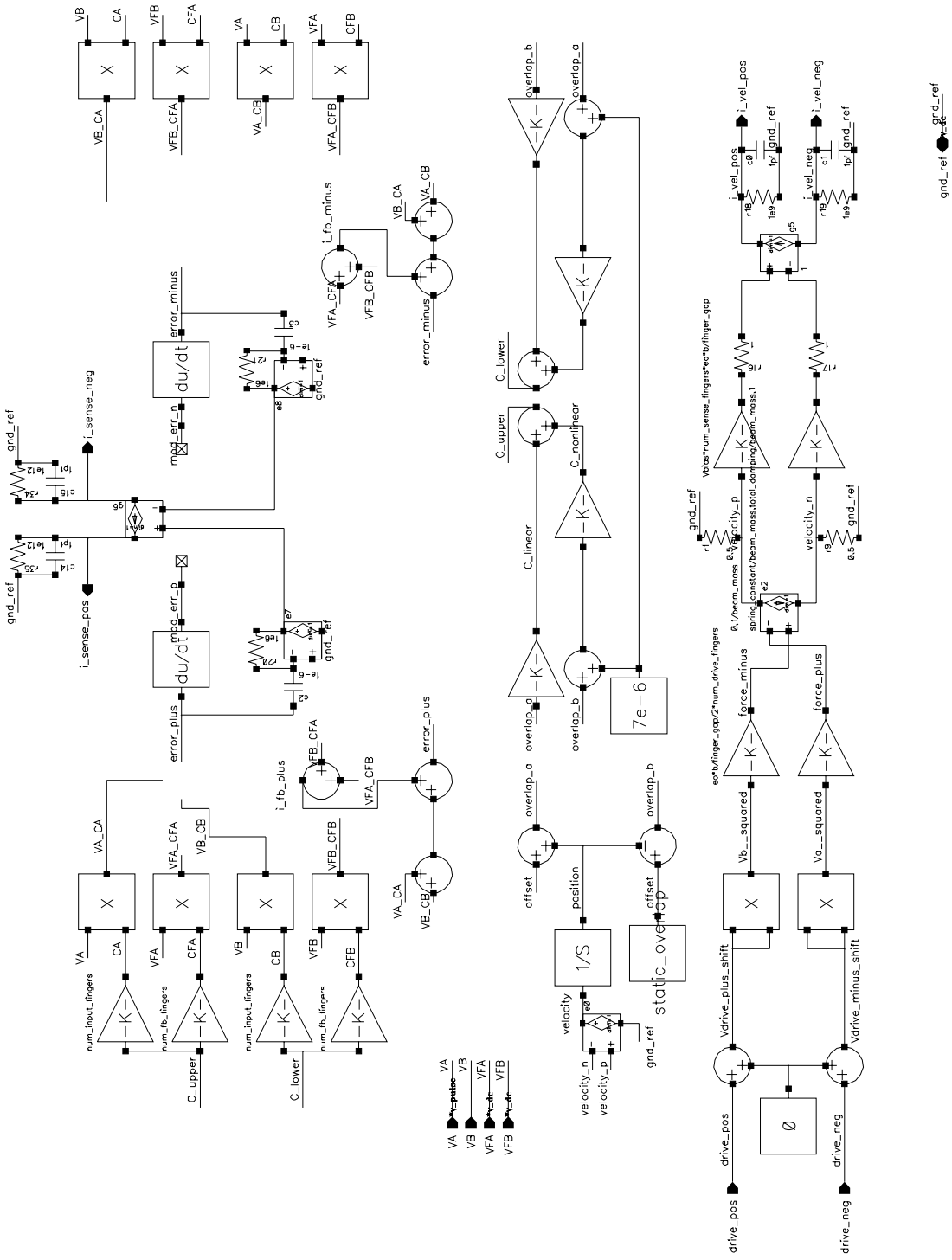

Figure 2-10: ADICE model for the MEMS transducer.

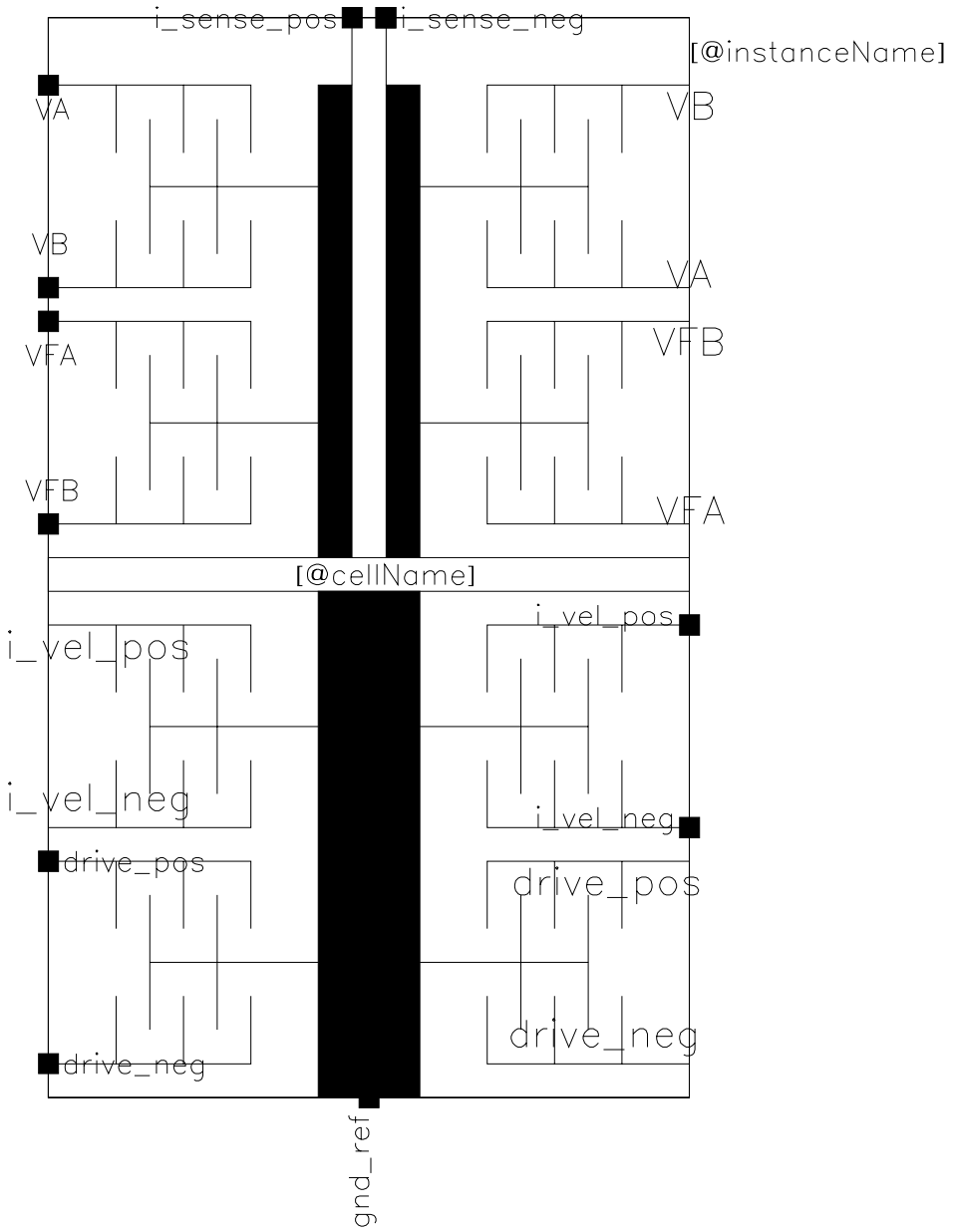

Figure 2-11: ADICE symbol for the MEMS transducer.

Parameters	Values
ϵ_o	8.85 pF/m
h	16.5μm
g	2μm
x_o	8μm
N_{input}	440
N_{fb}	440
N_{drive}	100
N_{vel}	120
m	5.6×10^{-9} kg
β	1.587×10^{-6} kg/s
k	50 N/m

Table 2.1: Parameter values for the MEMS transducer design.

Specifications	Values
f_{res}	15kHz
i_{vel}	$\pm$20nA
x_m	$\pm$ 3.1μm
C_m	$\pm$ 100fF
C_o	260fF
C_{par}	1pF

Table 2.2: Specifications for the MEMS transducer.

Chapter 3

Drive Loop

3.1 Motivation

The purpose of the drive loop is to vibrate the movable beam of the MEMS transducer to produce a sinusoidally varying capacitance. Due to the high quality factor of the MEMS structure, it is advantageous to vibrate the moving beam at its mechanical resonant frequency to yield the largest sense current from the transducer for a given voltage drive. Thus, maximum displacement results in improved signal-to-noise ratio for the overall MEMS-based amplifier system.

Care must be taken to maintain vibration at resonance. The frequency of the resonant peak illustrated in Figure 2-9 can shift with process variations and temperature. Consequently, a fixed-frequency drive can severely degrade the sensitivity of the amplifier and result in poor noise performance. To address this problem, a robust approach is needed to ensure that the moving structure will consistently vibrate at its mechanical resonance. This robustness is achieved through closed-loop control. Because the applied force drive and beam velocity are in phase at resonance, it is possible to place the transducer in a feedback loop with a nonlinear element to form a self-exciting oscillator that drives itself to maintain constant-amplitude oscillations at the desired vibration frequency.

3.2 Overview

A simplified overview of the drive loop electronics is illustrated in Figure 3-1, and the block diagram for the drive loop is shown in Figure 3-2. The circuits are shown here as single-ended for simplicity, although in actuality the entire signal chain and all amplifiers in the drive loop are fully differential. The velocity signal current from the MEMS structure, produced by the modulating capacitance of the transducer, is converted into a voltage by the transresistance amplifier, and an intermediate gain stage provides additional amplification. The high-pass filter suppresses any DC offsets before the comparator converts the signal into a square-wave voltage drive. This square-wave voltage drive from the comparator applied on the fixed drive plates of the transducer induces an electrostatic force, and the amplitude and frequency of the force drive determine the displacement of the moving beam of the MEMS structure. The beam velocity is converted to a current by additional fixed plates of the transducer.

The presence of a comparator (a nonlinear element) in the feedback path of the drive loop makes direct application of linear analysis techniques difficult. However, describing functions provide a method to treat nonlinear elements such that traditional LTI stability analysis may be applied.

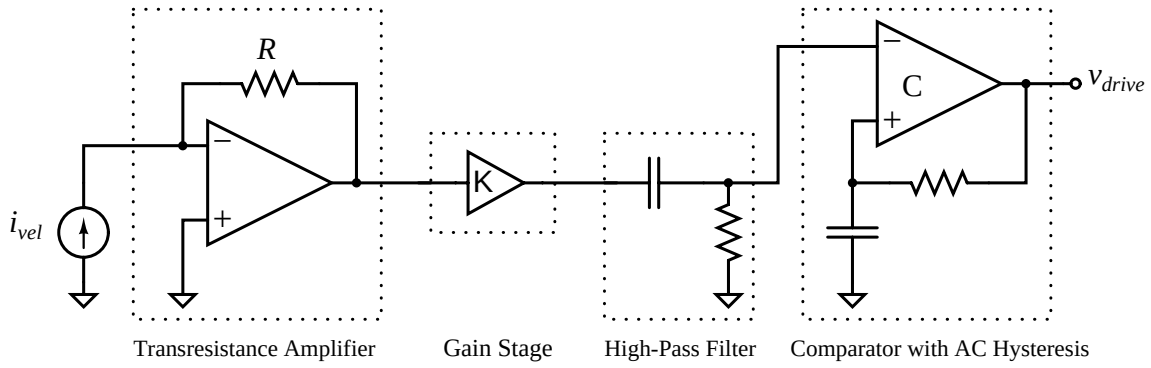

Figure 3-1: Simplified overview of drive loop.

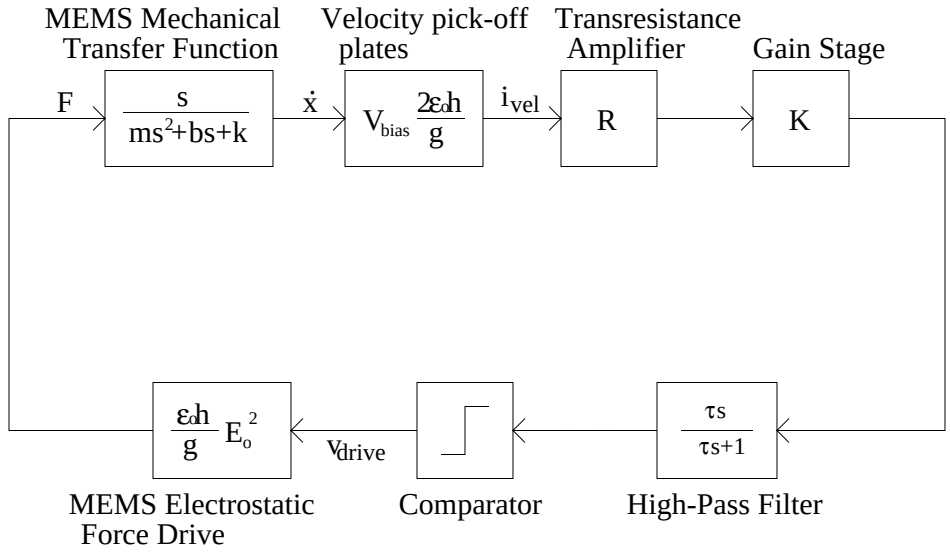

Figure 3-2: Block diagram for drive loop feedback.

3.3 Describing Function Analysis

Describing function analysis assumes that the overall loop transmission is sufficiently low-pass in nature so that the effective gain of the nonlinear element is well approximated by the fundamental component of its output, which can depend on both the frequency and amplitude of the input, divided by its input amplitude [6]. For a comparator without hysteresis, its describing function is simply

$$G_D(E) = \frac{4}{\pi}\frac{E_o}{E},$$

where E is the amplitude of the input of the comparator, and E_o is the amplitude of the square-wave output of the comparator. Intuitively, the high-Q bandpass nature of the transducer attenuates the harmonics of the square wave drive to yield the desired sinusoidal displacement of the beam, in line with the describing function approximation.

Observing Figure 3-2, the open-loop transfer function of the drive loop is

$$L(s) = \left(s\frac{X}{F}(s)\right)\left(V_{bias}\frac{2\epsilon_0 h}{g}\right)(R)(K)\left(\frac{4}{\pi}\frac{E_o}{E}\right)\left(E_o^2\frac{\epsilon_0 h}{g}\right).$$

Constant-amplitude oscillations are possible when the system poles are on the $j\omega$-axis; this occurs when the two following conditions are satisfied:

$$|L(j\omega)| = 1$$

$$\angle L(j\omega) = 0.$$

If the transresistance amplifier, gain stage, high-pass filter, and comparator contribute negligible phase shift, the net loop transfer function phase is zero only at the resonant frequency of the transducer, when the velocity of the beam is linearly related to the drive force. Thus, this frequency is the self-oscillation frequency of the drive loop, and the magnitude of the loop transfer function is unity when the amplitude of oscillations into the comparator is

$$E = \left(\frac{1}{\beta}\right)\left(V_{bias}\frac{2\epsilon_0 h}{g}\right)(R)\,(K)\left(\frac{4E_o}{\pi}\right)\left(E_o^2\frac{\epsilon_0 h}{g}\right).$$

This analysis indicates that poles on the $j\omega$-axis are possible. However, in order to maintain constant-amplitude oscillations, the system poles must be able to remain on the $j\omega$-axis under perturbations. Observation of the root locus of the open-loop drive transfer function, illustrated in Figure 3-3, indicates that this is true. Intuitively, the comparator acts as a variable gain element depending on the amplitude of oscillations: if the amplitude of oscillations is small, the effective gain from the comparator is large, and vice versa. If the system poles of the drive loop drift into the right-half plane, resulting in exponentially increasing amplitude of oscillations, the effective gain of the comparator decreases. The root locus indicates that a decrease in the loop transmission gain pulls the system poles towards the left-half plane, back towards the $j\omega$-axis. Conversely, if the poles on the $j\omega$-axis drift into the left-half plane, causing exponentially decreasing amplitude of oscillations, the effective gain of the comparator increases, pulling the poles towards the right-half plane. Therefore, the drive loop is capable of sustaining constant-amplitude oscillations at the mechanical resonance of the MEMS transducer.

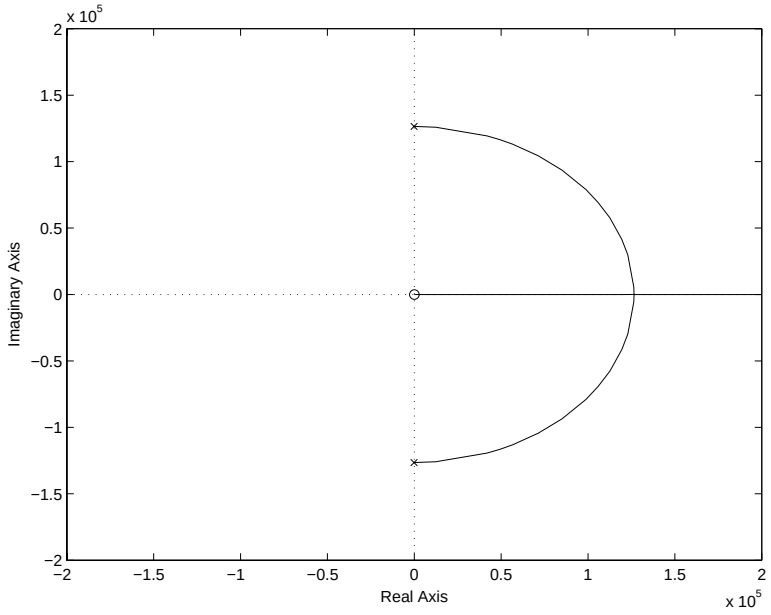

Figure 3-3: Root locus for the drive loop transfer function.

3.4 Design Considerations

3.4.1 Phase Shift at Resonance

In reality, however, the transresistance amplifier, gain stage, and comparator, although designed for wide bandwidths, contribute small negative phase shifts at the resonant frequency of the MEMS transducer due to their finite bandwidths. The high-pass filter can be designed to provide positive phase shift for cancellation, but precise cancellation of phase shifts is not practical over a -40 to 105°C temperature range, and a phase error between one and five degrees is expected. Therefore, the oscillation frequency of the drive loop is not precisely at the resonant peak of the transducer, and the displacement of the beam is less than maximum. Nonetheless, due to the high-Q nature of the mechanical transfer function, a 20° phase error from resonance results in less than 5% loss in beam displacement, so a small phase error does not significantly decrease the transduced AC sense current. However, phase shift from resonance results in signal loss in the sense loop as it is demodulated. This is analyzed in Chapter 4.

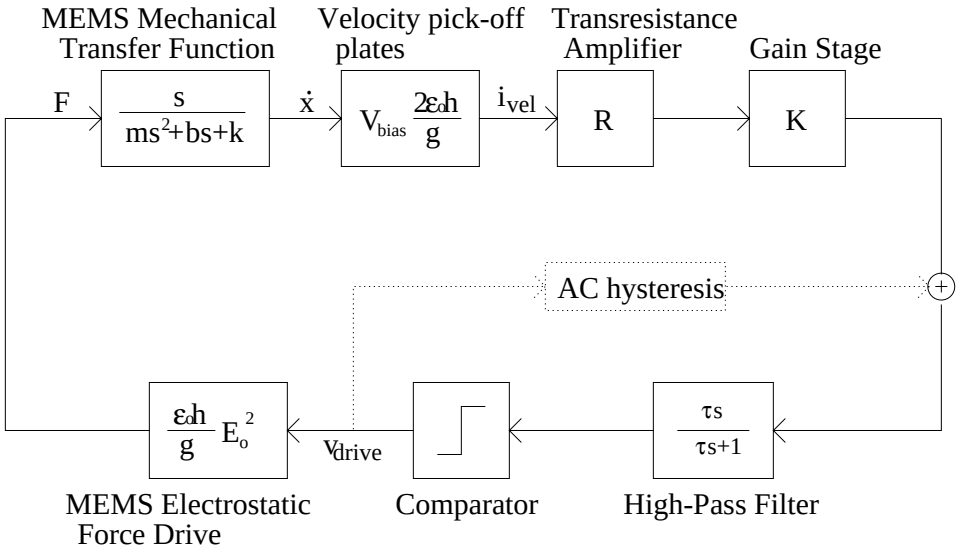

Figure 3-4: Drive loop block diagram with AC hysteresis.

3.4.2 AC Hysteresis

In practice, the presence of parasitic paths coupling force and velocity nodes in the drive loop can result in unwanted high-frequency oscillations. In addition, noise at the input of the comparator can potentially cause multiple transitions near the comparator threshold. Both problems are addressed by adding a small amount of positive capacitive feedback around the comparator, as indicated in Figure 3-4. This creates a 'blanking' interval such that once the comparator changes state, it cannot make another transition for a fixed amount of time. The effect of the AC hysteresis is illustrated conceptually in Figure 3-5. The time constant of the AC hysteresis is set to be faster than the period of the resonant frequency so that it does not contribute phase shift at the target oscillation frequency of the feedback loop, and the describing function of the comparator remains unchanged.

Another design concern is the presence of higher order resonant modal frequencies of the MEMS structure, which can also potentially form stable limit cycles. However, the nature of the force drive and velocity pick-off cannot support many of these mechanical modes, so these modes can never be excited into a self-sustaining oscillation. In addition, the other resonant modes are at frequencies much higher than the fun-

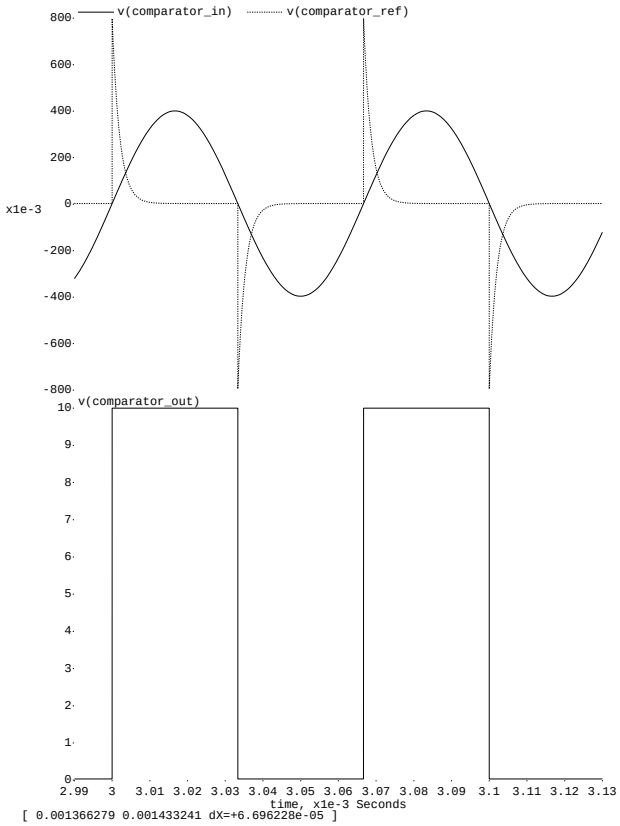

Figure 3-5: Conceptual effect of AC hysteresis.

damental resonance, so the modes that can plausibly be realized by the force drive are prevented by the blanking interval of the AC hysteresis.

3.4.3 Drive Loop Start-up

At initial power-up, the MEMS beam is stationary, and the output of the comparator is in an arbitrary initial state. The comparator cannot transition unless the beam moves, and the beam cannot move unless the comparator transitions. Although the describing function analysis demonstrates that the drive loop is capable of sustaining constant-amplitude oscillations, the system must be perturbed at start-up to push the system towards oscillation. This initial perturbation is provided by the inherent noise in the drive loop circuits, which is dominated by the 2MΩ load of the transresistance amplifier. This noise is amplified by the subsequent gain stage, and its rms amplitude must be able to overcome offsets at the input of the comparator to instigate progress

towards steady-state oscillation. The high-pass filter suppresses the offsets of the transresistance amplifier and the gain stage to aid this noise-induced start-up.

However, the high-pass filter uses a nonlinear resistor, the resistance of which is sensitive to large voltage swings. Although the gain of the intermediate gain stage must be large during start-up to sufficiently amplify the noise to overcome the comparator offset, it is desirable that this gain is much less during the steady state operation of the drive loop. Therefore, the gain stage was designed to have a switch that controls the amount of gain.

3.5 Drive Loop Circuits

The circuits used in the drive loop were borrowed from a gyroscope prototype from Analog Devices. This section analyzes these circuits with a few modifications to demonstrate feasibility for this system. The velocity current from the MEMS transducer is picked-off differentially by a fully differential transresistance amplifier, and a switched gain stage provides additional gain. This stage has higher gain when the drive loop is first turned on to amplify noise to induce start-up, but is manually switched to a lower gain when the MEMS beam is oscillating with a constant amplitude. The lower gain state is desirable during steady state operation to remain in the linear range of the nonlinear resistor used in the high-pass filter which follows the switched gain stage. The high-pass filter suppresses DC offsets from the transresistance amplifier and the gain stage to avoid large offsets at the input of the comparator. The comparator is comprised of two stages. The high-gain/latching stage converts the output of the high-pass filter into a 0-5V square-wave, and the level translator converts the 0-5V square-wave into a 0-10V square-wave to drive the MEMS transducer. These two stages together effectively form a 0-10V comparator. Capacitive feedback from the output of the high-gain/latching stage to the output of the switched gain stage creates an AC hysteresis interval.

All the power supply rails for the drive loop circuits are 5V and 0V, except for the level translator, which are 10V and 0V. The primary motivation for this is that

the circuits borrowed from the gyro prototype operated at 0V and 5V. By using the intended supply rails, the minimum device length did not need to be increased to accomodate larger breakdown voltages. In addition, a 10V transition into the hysteresis feedback capacitors results in a larger peak voltage into the high-pass filter, which can potentially cause the LFET resistance to change nonlinearly. Thus, the output of the high-gain/latching stage was used for hysteretic feedback instead of the output of the level translator.

Table **??** summarizes of the key specifications for each circuit block. The phase margin Φ_m is not relevent for the preamplifier and the source follower, which are open loop. The noise spectral densities of the amplifiers listed in the table are at 15kHz for the preamplifier and the demodulator op amp, and at 1Hz for the source follower buffer and the difference op amp.

3.5.1 Transresistance Amplifier

The transresistance amplifier has an open loop differential gain of about 6400, a unity-gain crossover frequency at roughly 6MHz, and a phase margin of 65°. The schematic is illustrated in Figure 3-6, and its frequency response is shown in Figure 3-7. The transresistance amplifier is shown with its load in Figure 3-8.

The basic topology consists of two gain stages with Miller compensation for closed-loop stability. The first stage is a PMOS differential pair with resistive loading to avoid common-mode feedback, and the second stage utilizes an NPN differential pair with PMOS current source loads for high gain. The diode provides DC level-shifting. Emitter followers buffer the output so the resistors needed to detect the output common-mode level avoid loading the high impedance node. A high-gain differential amplifier compares the output common-mode voltage with a reference (1.5V), and servos the current sources of the second gain stage until the output common-mode voltage is equal to the reference. The transresistance amplifier uses a total of 200μA of current.

The common-mode reference voltage, and thus the common-mode voltage of the transresistance amplifier output, is equal to 1.5V. Because there is no DC current through the transresistance load from the MEMS structure, the DC common-mode

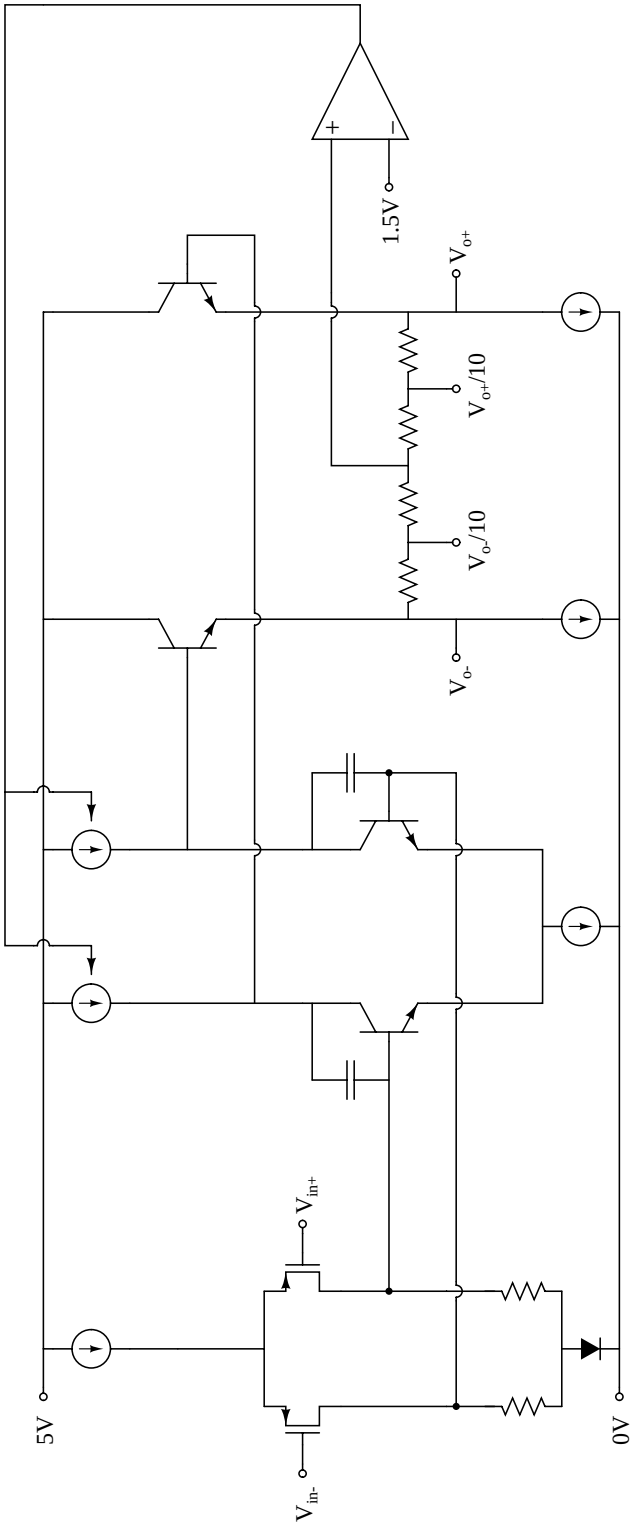

Figure 3-6: Transresistance amplifier.

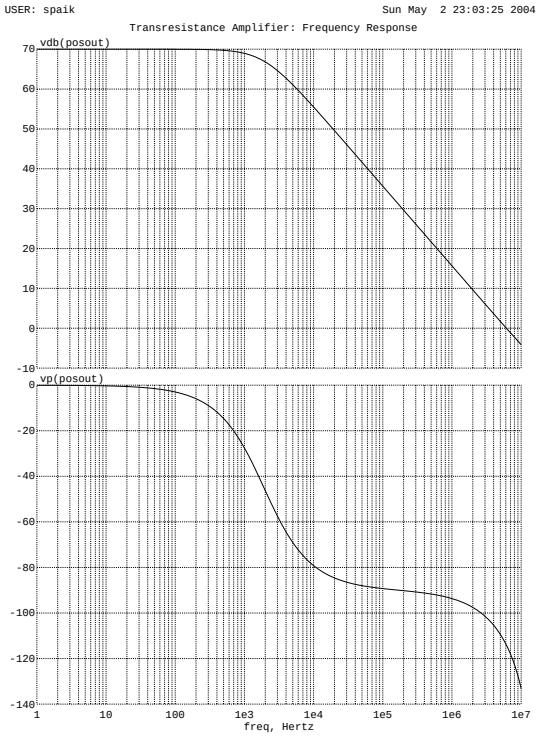

Figure 3-7: Frequency response of transresistance amplifier.

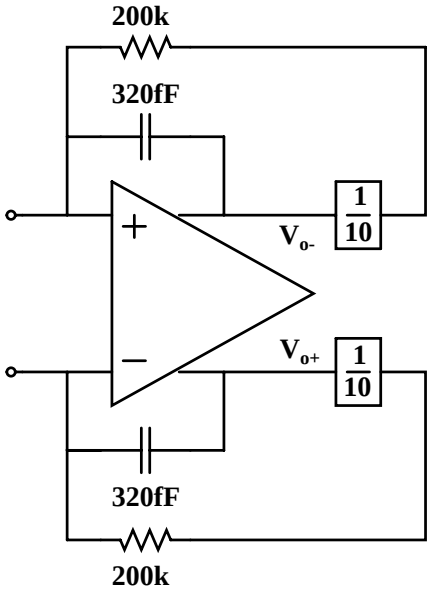

Figure 3-8: Transresistance amplifier with load.

voltage of the transresistance amplifier input is also 1.5V. This sets the bias voltage on the velocity pick-off plates of the transducer.

The transresistance load for the amplifier is desired to be 2MΩ. Due to non-linearity issues experienced with using an LFET in triode here, a thin-film resistor was used instead. However, such a large resistance would require enormous area, so the output of the amplifier was attenuated by a factor of ten before feeding back to the input. With a 200kΩ resistor, the effective load appears to be 2MΩ, as desired.

It should be noted that achieving a 2MΩ resistance with a 200kΩ resistor and a feedback attenuation of ten results in ten times more noise than using a 2MΩ resistor without feedback attenuation. The increased noise helps motivate start-up, but the presence of noise in the signal chain can cause double-triggering at the input of the comparator. This is prevented with AC hysteresis.

The capacitive loading of the MEMS transducer at the input of the transresistance amplifier with the 2MΩ effective load places a low-frequency pole in the forward path of the amplifier, degrading amplifier stability. A 320fF capacitor placed from the unattenuated output of the amplifier to the input provides lead compensation (placing the capacitor directly in parallel with the 200kΩ resistor requires a larger capacitor value for the same zero location) to aid stability. The resulting phase shift at 15kHz, the MEMS resonant frequency, is

$$\arctan\left((2\text{M}\Omega)(320\text{fF})(2\pi)(15\text{kHz})\right) = -3.45^\circ.$$

The magnitude of velocity signal current from the MEMS structure is 20nA. Thus, each output of the transresistance amplifier has an amplitude of

$$(\pm 20\text{nA})(2\text{M}\Omega) = \pm 40\text{mV}.$$

3.5.2 Switched Gain Stage

The switched gain stage, shown in Figure 3-9, is a resistively loaded differential amplifier with emitter degeneration in parallel with a switch, for a differential gain of

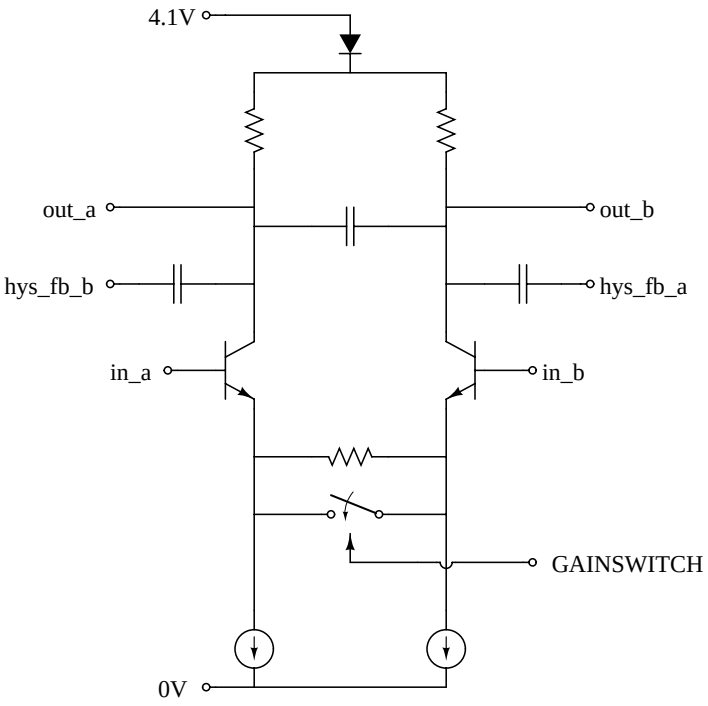

Figure 3-9: Switched gain stage.

about 30 when GAINSWITCH is high, and a gain of about 6 when GAINSWITCH is low. A shunt capacitor between the two outputs provides bandlimiting, and two additional inputs capacitively coupling into the output nodes allow for AC hysteresis feedback to prevent the comparator from double triggering. An external reference voltage of 4.1V to power this stage is used to ensure a low impedance power supply, which is important because of transients due to the AC hysteresis feedback. This stage uses a total of 35μA of current.

Nominally, the hysteresis feedback nodes are low impedance, so the capacitors form a low-pass filter with a corner frequency at 200kHz. When the comparator transitions, the step change in voltage sees a capacitive divider into the output nodes

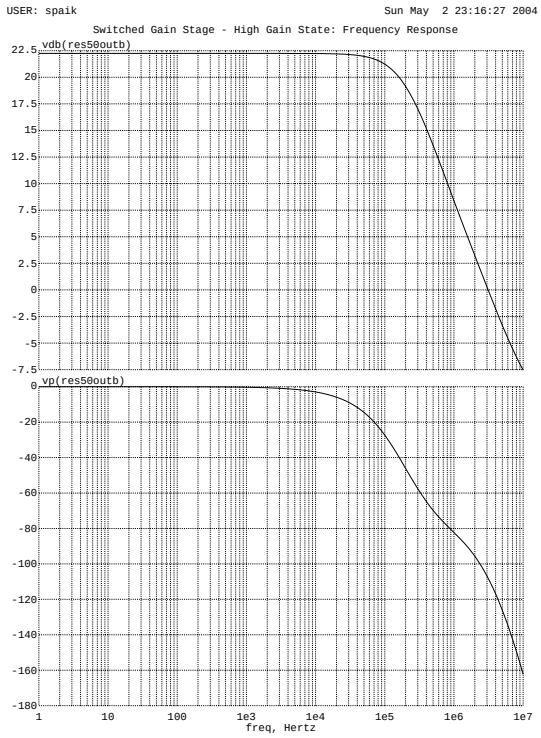

Figure 3-10: Frequency response of switched gain stage in its high gain state.

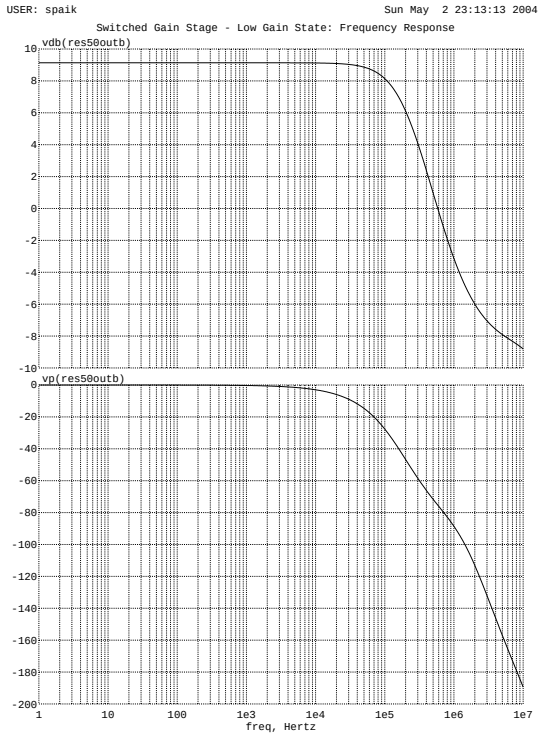

Figure 3-11: Frequency response of switched gain stage in its low gain stage.

of the switched gain stage. This step change propagates through the high-pass filter to the comparator inputs, and pulls the the higher input of the comparator even higher, and the lower input even lower. The capacitors and the load resistors of the switched gain stage set the time constant of the decay of this AC hysteresis.

The frequency response in both gain states is illustrated in Figures 3-10 and 3-11. The switched gain stage is in its low gain stage during steady state operation of the drive loop, and the differential signal output of this stage is

$$(\pm 40\text{mV})(6) = \pm 240\text{mV}$$

on top of the DC common-mode voltage of

$$4.1\text{V} - 0.6\text{V} - (90\text{k}\Omega)(8.8\mu\text{A}) = 2.7\text{V}.$$

The phase shift introduced at the MEMS resonant frequency is

$$\arctan\left(\frac{15\text{kHz}}{200\text{kHz}}\right) = -4.3^\circ.$$

3.5.3 High-Pass Filter

The high-pass filter in Figure 3-12 consists simply of a capacitor and a resistor. It should suppress DC offsets, but avoid attenuating the 15kHz signal from the MEMS transducer. The large resistance necessary for a sufficiently low-frequency pole would require a thin-film resistor that takes up an unreasonably large area. Instead, an LFET is operated in its triode region. The four diode-connected transistors in parallel on the left set up the gate-to-source bias of the two transistors on the right, which have a much longer length than the diode-connected transistors. Hence these two transistors are called long FETs, or LFETs, and are guarenteed to operate in the triode region for a resistance of roughly 10MΩ. This LFET biasing uses about 3.4μA of current. With a 7.5pF capacitor, the high-pass filter has a zero at the origin and a pole at 2.1kHz. Its frequency response is illustrated in Figure 3-13. The diode-

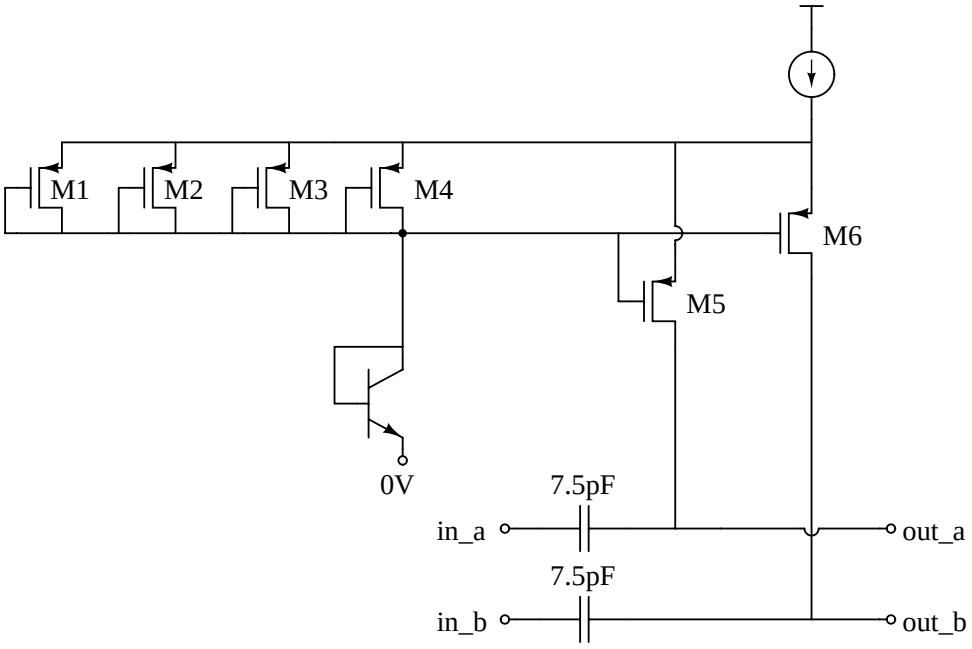

Figure 3-12: High-pass filter.

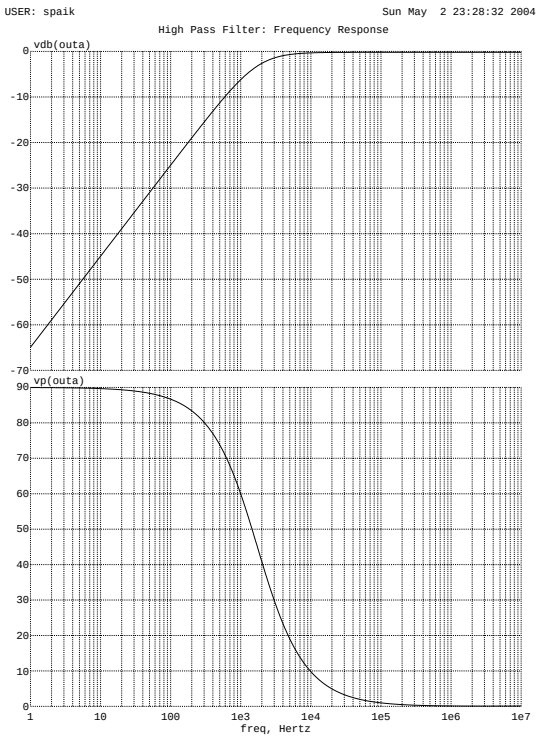

Figure 3-13: Frequency response of the high-pass filter.

connected NPN transistor provides level-shifting to bias the output voltage of the high-pass filter to be in the high-gain input range of the following stage. The DC common-mode voltage at the output of the high-pass filter is about 2V. The gain and phase shift at 15kHz are

$$\left| \frac{j(2\pi)(15\text{kHz})(10\text{M}\Omega)(7.5\text{pF})}{1 + j(2\pi)(15\text{kHz})(10\text{M}\Omega)(7.5\text{pF})} \right| = 0.99,$$

$$90^\circ - \arctan\left(\frac{15\text{kHz}}{2.1\text{kHz}}\right) = 8^\circ.$$

3.5.4 High-Gain/Latching Stage

The high-gain/latching stage is illustrated in Figure 3-14. The NMOS source-follower input stage of this stage avoids loading the high-pass filter that precedes it. NPN and PNP differential gain stages with resistive loads provide a high gain of about 2000 (and common-mode feedback is conveniently not needed), and the positive feedback of the proceeding latching stage provides rail-to-rail squaring of the input signal. Inverters at the output provide buffering to drive the level translator stage. This stage uses 780μA of bias current.

The DIS input, when high, steals away bias current from the PMOS differential-pair gain stage, turning it off. The latching stage can then be externally driven from inputs RD1 and RD2; this provides a means of testing the drive loop circuitry open-loop.

The frequency response of the two high-gain stages is shown in Figure 3-15. Its -3dB bandwidth is 270kHz, which is consistent with its -3° of phase shift at 15kHz.

3.5.5 Level Translator

Whereas the supply rails of the preceding circuits were 5V and ground, the supply rails of the level translator stage are 10V and ground. Referring to Figure 3-16, the NMOS input transistors accept the 0 and 5V output of the previous stage, and the cross-coupled PMOS load latches it to 0 and 10V. Inverters at the output provide

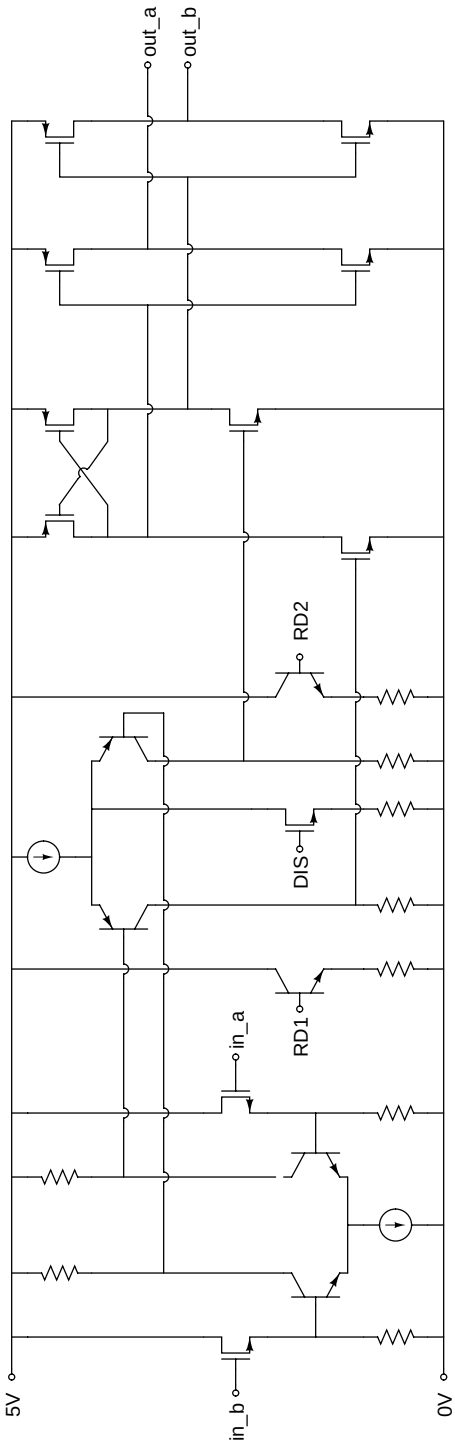

Figure 3-14: High gain/latching stage.

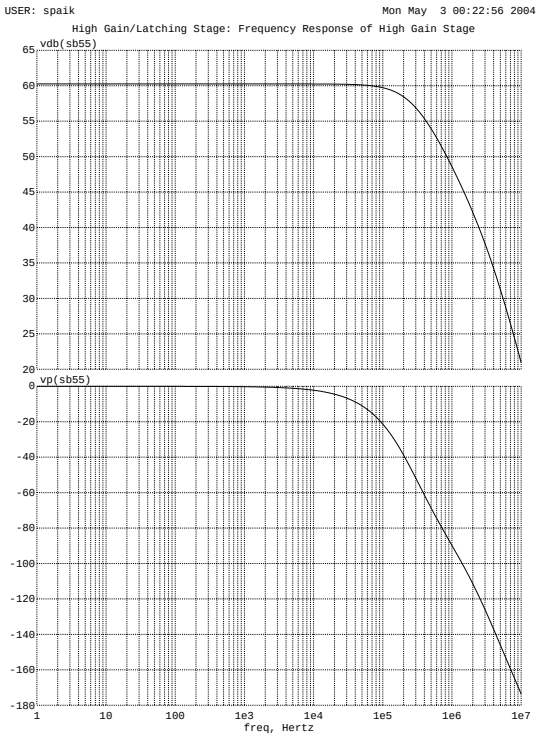

Figure 3-15: Frequency response of the high-gain stage without the latching stage.

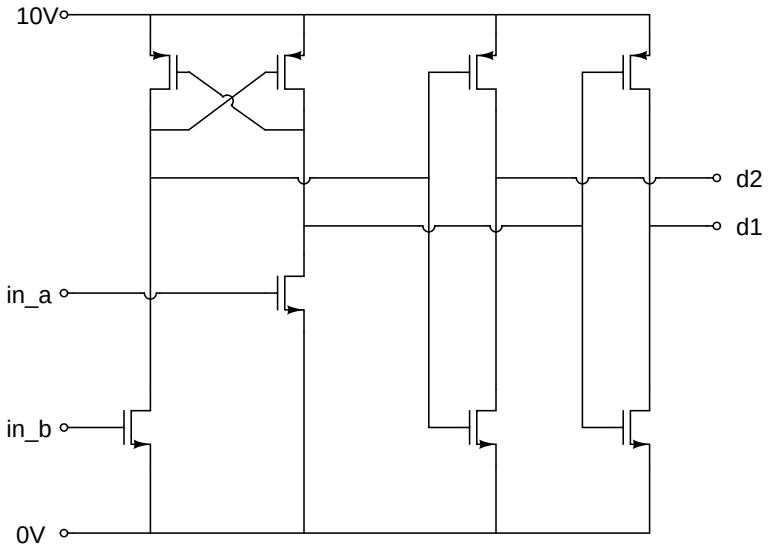

Figure 3-16: Level translator.

buffering to drive the capacitive load of the MEMS transducer force drive plates. A 0V and 10V square-wave drive induces 365nN of electrostatic force.

3.6 Simulation Results

Figure 3-17 illustrates the drive loop signal chain in feedback with the MEMS transducer. The simulated drive loop signal waveforms in steady-state are shown in Figure 3-19. The variables $i(v0)$, vel_transr, vel_gain, vel_hpf, vel_higain, and vel_drive represent, respectively, the velocity current from the MEMS transducer, the output of the transresistance amplifier, the output of the switched gain stage, the output of the high-pass filter, the output of the high-gain/latching stage, and the output of the level translator. The simulated frequency of the square wave driving the MEMS transducer is about 14.94kHz, and the phase shift between the velocity current and the output of the level translator is about -4.3°. Figure 3-18 shows the velocity current signal and the output of the transresistance amplifier during start-up. The number of cycles to reach equiblibrium is roughly equal to the quality factor of the system, and the simulated start-up takes about 15ms to reach the maximum, steady-state amplitudes of the signals.

3.7 Summary

The function of the drive loop in the MEMS-based amplifier system is to vibrate the movable beam of the MEMS structure. This creates the modulating capacitance which transduces the low-frequency input voltage into a high-frequency current signal. The mechanical frequency response of the MEMS structure is underdamped, and the beam should be vibrated at its mechanical resonance to maximize the signal-to-noise ratio of the system. Closed-loop control to robustly vibrate the beam for optimum system performance was analyzed with the aid of describing functions. The circuits used in the drive loop were borrowed from an ADI gyro sensor and modified to function in this application.

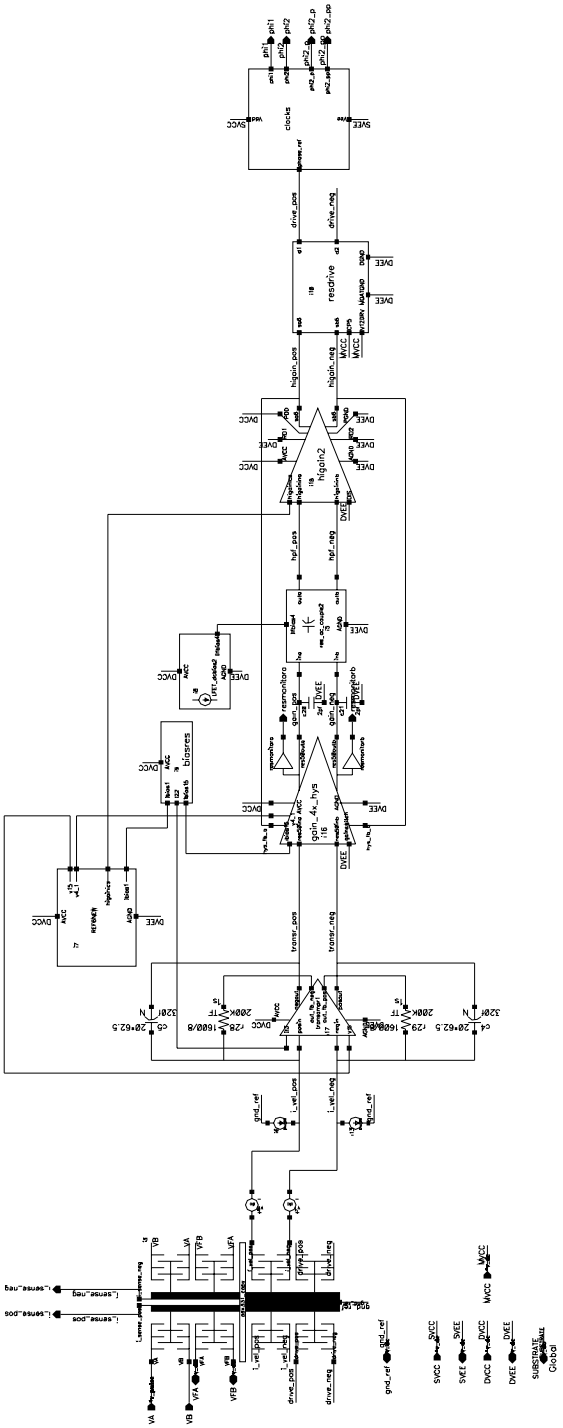

Figure 3-17: Drive loop in feedback with the MEMS transducer.

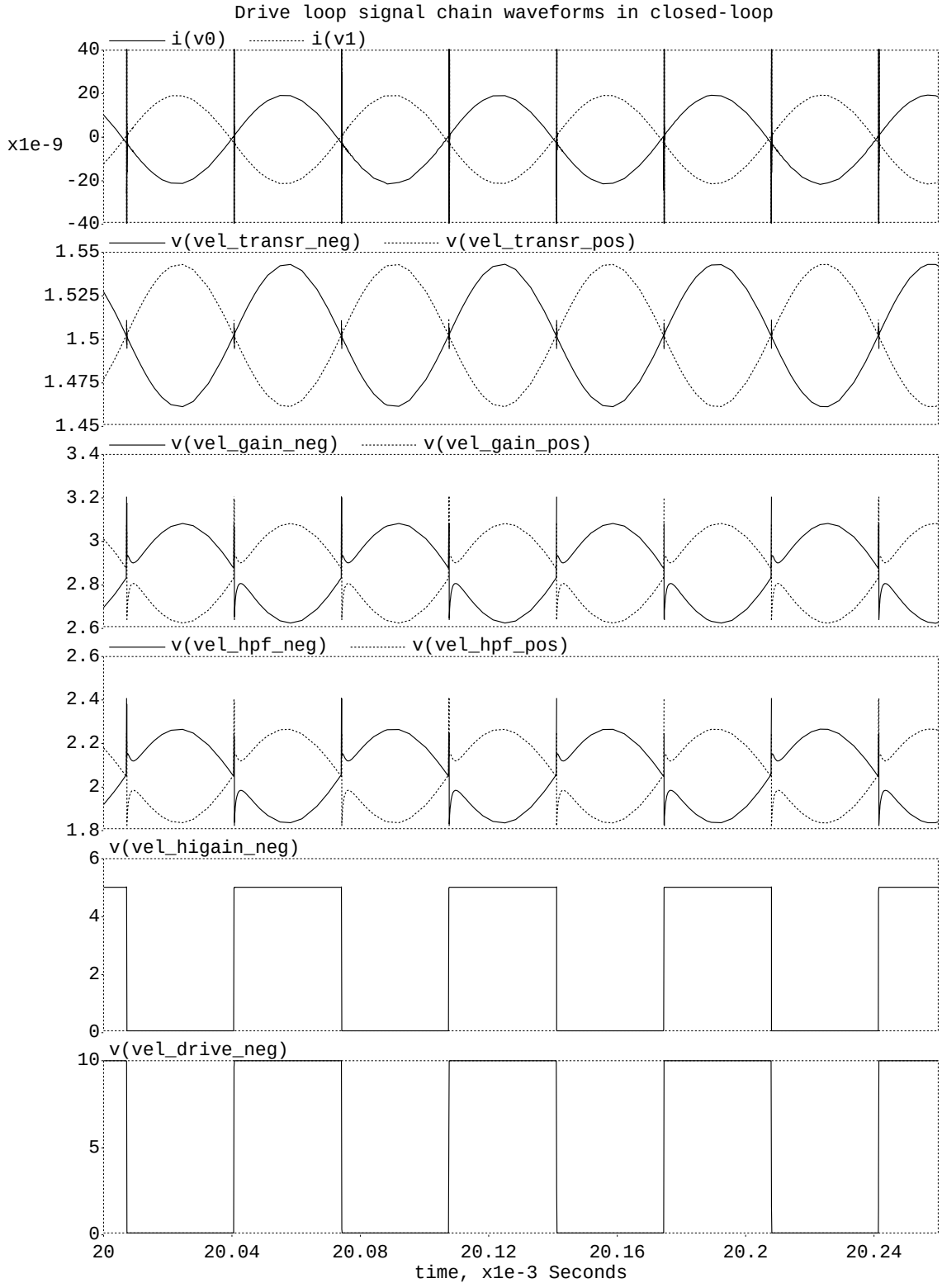

Figure 3-18: Drive loop simulation: steady-state resonance.

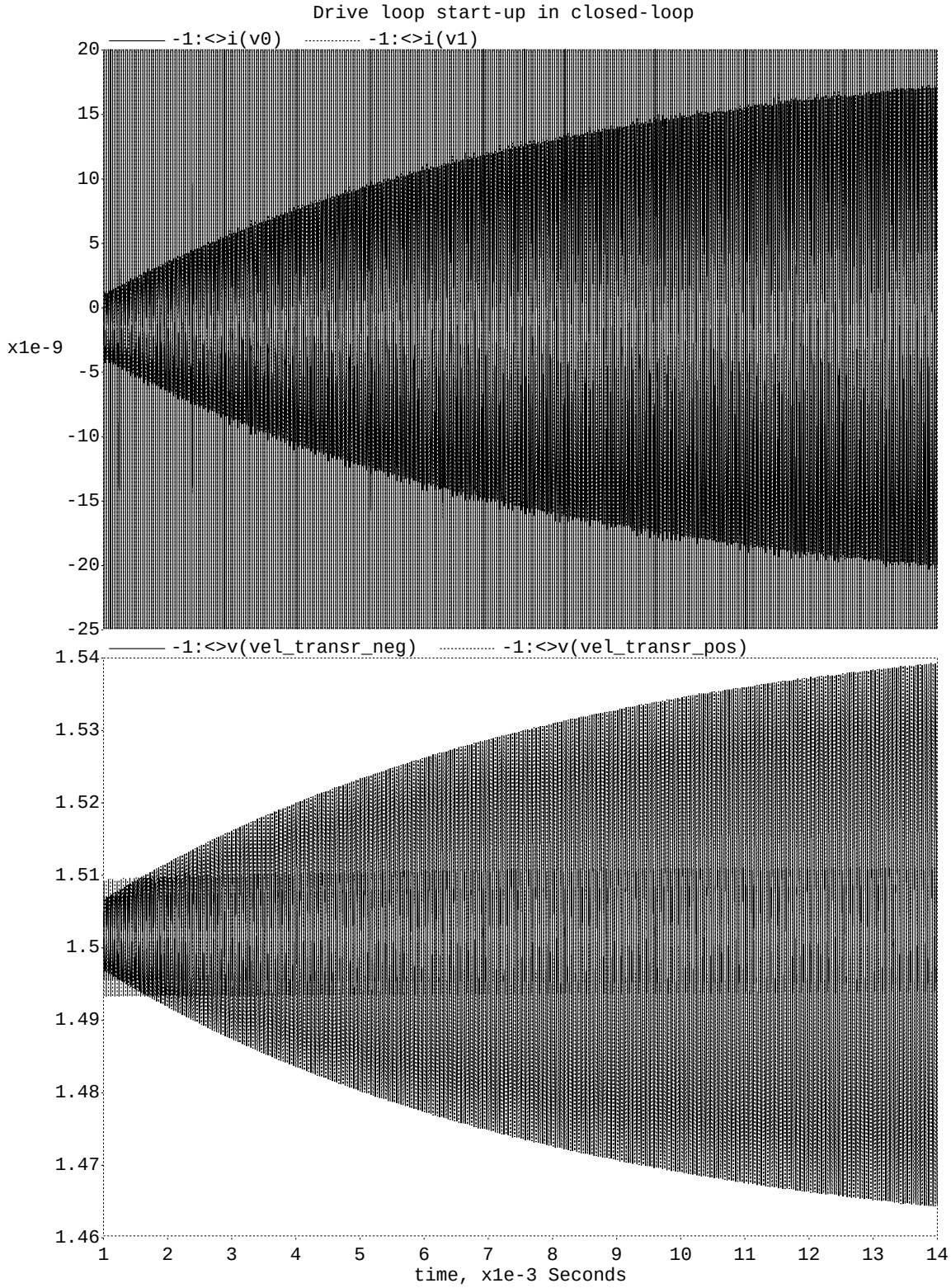

Figure 3-19: Drive loop simulation: start-up transients.

Chapter 4

Sense Loop

4.1 Motivation

The basic function of the sense loop is illustrated in Figure 4-1. The differential input voltage is transduced into an AC current by the MEMS transducer, and the purpose of the sense loop is to provide gain and demodulation to this sense current, for a low-frequency output corresponding to the low-frequency input. The capacitance C_{in} represents the input capacitance of the preamplifier.

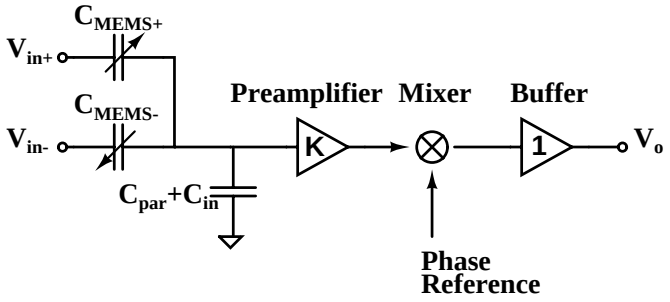

Figure 4-1: Basic function of the sense loop.

As an open loop amplifier, the sense current amplitude, and thus overall gain of the input voltage signal, depends on the magnitude of the capacitance modulation, in addition to other potentially variable gain elements in the sense loop signal path. While the modulating capacitances of the MEMS transducer are capable of matching

to 0.1%, their absolute values can vary as much as 20%. Furthermore, the amount of capacitance modulation also depends on the viscosity of air between the capacitive plates, which changes with temperature. To provide consistent and predictable gain to the input signal over temperature and process variations, global feedback from the output of the sense loop to the MEMS transducer maintains a robust closed-loop gain over variations in the forward-path gain. The use of feedback trades 20% variations in open loop gain for 20% variations in closed-loop bandwidth, which for the purpose of the MEMS-based amplifier is an acceptable trade-off. Including an integrator in the signal path allows zero steady-state error in the measurement. As discussed earlier, the MEMS-based amplifier may be configured as either an operational amplifier, with the output feeding back to one of the input plates, as illustrated in Figure 4-2, or as an instrumentation amplifier, with the output feeding back to additional fixed capacitor plates for a true differential input and complete isolation of the input terminals.

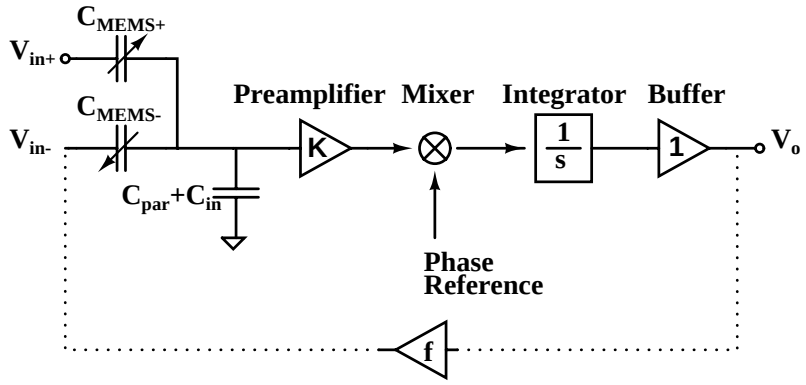

Figure 4-2: Sense loop with global feedback and integrator for zero steady state error.

4.2 Overview

If the AC sense current of the MEMS transducer were demodulated immediately, and if the demodulation process did not add additional noise sharing bandwidth with the input signal, then the demodulated output would result in a low-noise measurement of

the input, and all would be well. However, nonidealities in the demodulation generally increase the noise level in the signal bandwidth, defeating the benefits achieved by the MEMS transducer. Therefore, it is practical to preamplify the sense current before it is demodulated, to boost its signal magnitude relative to the additional noise to be introduced. Thus, the preamplifier must be designed carefully to add minimum noise in the bandwidth of the up-modulated signal.

Since the output terminal of the MEMS transducer connecting to the input of the sense loop is a capacitive node, the DC bias must be well-controlled to remain within the linear region of the preamplifier. This can be achieved by reset switches, with resets occuring each clock cycle of the demodulator phase reference. Integrated switches have the advantage of excellent matching as well as a fast recovery time to common-mode transients at the input node. However, the loop is no longer in the continuous time domain, and as with any sampled-data system, there will be aliased kT/C noise, in addition to charge injection offsets as the switches open. Both can be rejected with an appropriate correlated double sampling (CDS) clocking scheme.

The CDS circuit used in the sense loop is illustrated in Figure 4-3. For simplicity, the sense loop signal chain is shown here as single-ended, although the actual signal chain is fully differential. As its name indicates, CDS samples the noise and offset of an amplifier twice during each clock period. During ϕ_2, the signal path of the demodulator is disconnected, the input node of the preamplifier can be reset, and the charge injection and kT/C noise of the reset switches settle onto C_s, while the DC offset of the demodulator op amp is sampled onto C_h. During ϕ_1, C_h presents an offset-reduced summing junction while the signal sees a gain of $-C_s/C_f$.

An advantage of this particular topology is that it simultaneously provides demodulation and integration to the up-modulated signal. To gain intuition for how this stage functions as both a demodulator and an integrator, Figure 4-4 illustrates the signal phasing relative to the demodulator clock. The amplitude of the preamplifier output is proportional to the DC input voltage. The switches are phased such that the peak-to-peak amplitude is unwrapped during ϕ_1 and accumulated during ϕ_2. Therefore, the slope of the average value of the CDS output is proportional to twice

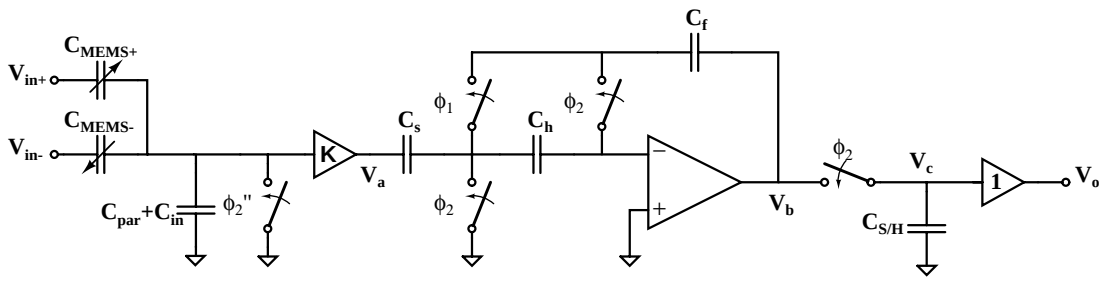

Figure 4-3: Sense loop with input reset switch and CDS dual demodulator/integrator.

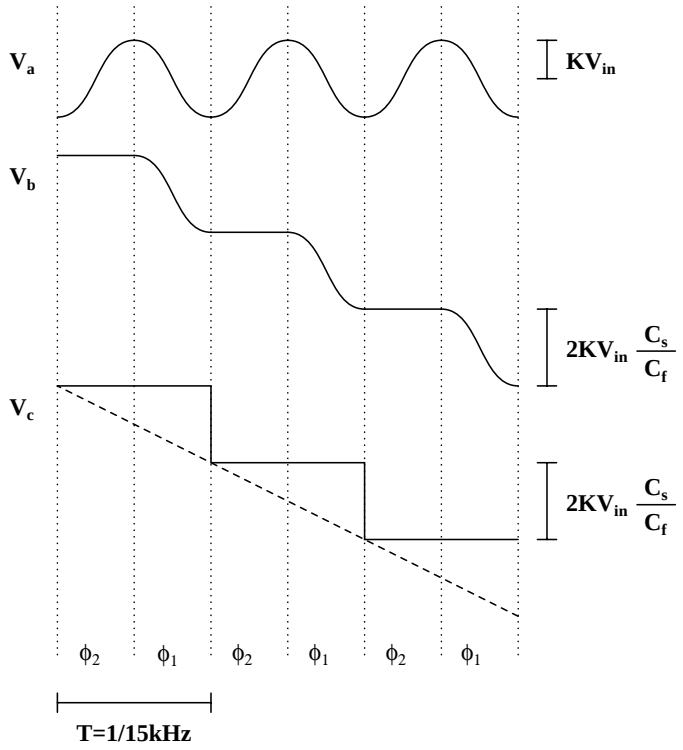

Figure 4-4: Phasing for the CDS demodulator/integrator.

the magnitude of the DC input voltage. Thus, the sinusoidal sense current signal is demodulated back to DC and this DC value is integrated. A mathematical derivation of the transfer function for the CDS integrating demodulator is given in Section 4.4.

This CDS topology also effectively squares the DC gain of the demodulator op amp [7]. The intuition for this is as follows. If the offset of the op amp were perfectly sampled onto C_h, assuming no charge injection of the demodulator switches, C_h would produce an ideal virtual summing junction for the signal during ϕ_2. The open loop DC gain of the op amp would then appear to be infinite. However, the offset of the op amp can be sampled onto C_h only as accurately as its DC open loop gain. Therefore, during ϕ_2, the virtual summing junction has an offset that is smaller than the offset of the op amp by a factor of the DC open loop gain of the op amp. This offset reduction effectively squares the apparent DC open loop gain of the demodulator op amp.

4.3 Design Considerations

4.3.1 Clocking

Because the drive frequency of the MEMS transducer and the frequency of up-modulation are the same, the output of the comparator in the drive loop can serve as the phase reference for demodulation in the sense loop. At resonance, the AC sense current from the MEMS transducer is in phase with the beam velocity. This current signal is then integrated by the capacitance at the input of the preamplifier, and the signal at the preamplifier output is in phase with the beam displacement and in quadrature with the comparator output. This generates the clocking waveforms relative to the signal to be demodulated as illustrated in Figure 4-4, and the AC sense current is demodulated and integrated as desired.

The importance of maintaining beam displacement at resonance, where the AC sense signal and the electrostatic drive are exactly in phase, can be seen here. Deviation from resonance degrades the sense loop signal in two ways: the displacement of the beam, and therefore the magnitude of the transduced AC current, is less than

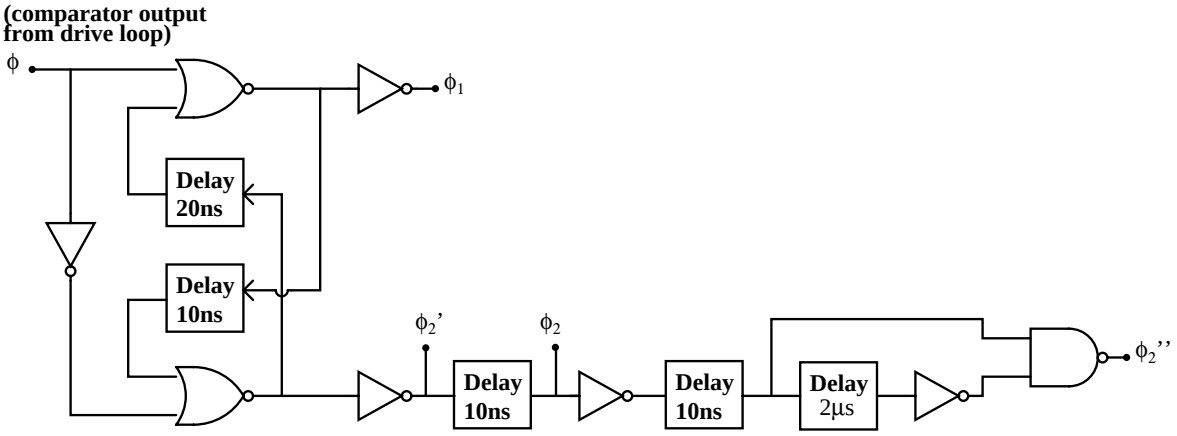

Figure 4-5: Circuit for demodulator clock synthesis.

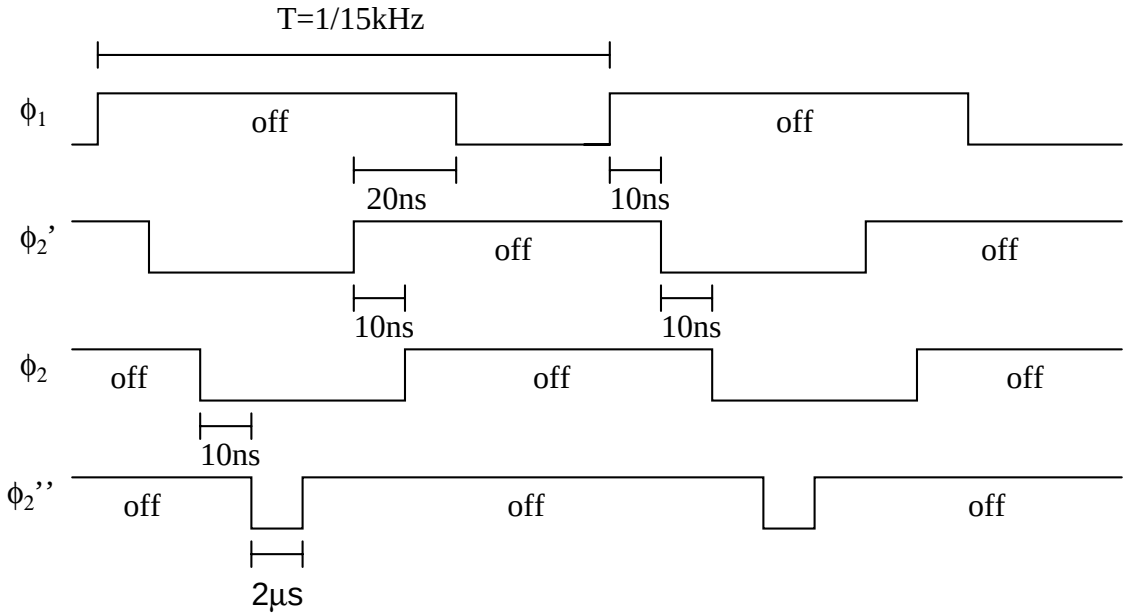

Figure 4-6: Timing waveforms for demodulator clocks (not to scale).

maximum, and the phase difference between the up-modulated sense signal and the demodulator phase reference results in a loss in gain at demodulation.

The CDS circuit requires that the clocks ϕ_1 and ϕ_2 do not overlap. Furthermore, at the end of ϕ_2, it is desirable to open the switch sampling the demodulator output V_b onto the capacitor $C_{S/H}$ slightly before the switches sampling the offset of the demodulator op amp onto C_h are turned off, so that the charge injection of these switches do not affect the sampled voltage. Thus, the output sample-and-hold switch phase is similar to ϕ_2 but is slightly advanced in time, and will be referred to as ϕ_2'. In addition, the input node of the preamplifier should be shorted briefly during ϕ_2 to the desired input bias voltage, when the signal path of the sense loop has been disconnected. The phase of the reset switch will be referred to as ϕ_2''. The circuit used to generate the desired non-overlapping and delayed clocks was adapted from [2] and is shown in Figure 4-5, and the resulting clock waveforms are illustrated in Figure 4-6.

4.3.2 Noise

If the settling time constants associated with C_s and C_h are fast relative to the duration of ϕ_2, the sense signal is unaffected by the charge injection and kT/C noise of the reset switch and the DC offset of the demodulator op amp. Similarly, low-frequency noise at the output of the preamplifier and at the input of the demodulator op amp are also suppressed by the inherent DC rejection of CDS, indicating that the noise of both amplifiers is essentially high-pass filtered [7]. The MEMS transducer up-modulates the DC input voltage into a frequency region of low noise so that the signal avoids sharing bandwidth with low-frequency noise. The CDS demodulator suppresses low-frequency noise as it maps the AC sense current signal back to DC to produce a noise-reduced DC measurement.

However, as a sampled-data system, noise is expected to be aliased if the sampling frequency is less than twice the noise bandwidth. As can be seen from Figure 4-7, while inputs into the demodulator at the even harmonics of the clock frequency do not change the CDS integrator output over one clock period, the odd harmonics are

demodulated with the sense current signal from the MEMS transducer. Similarly, it can also be seen that odd harmonic signals at the input of the demodulator op amp are also folded into DC. Although the CDS integrator suppresses DC offsets and low-frequency noise of the preamplifier and demodulator op amp, broadband thermal noise at the odd harmonics of the clock frequency add noise to the demodulated signal measurement. Therefore, both the preamplifier and the demodulator op amp must be sufficiently bandlimited to reduce this noise aliasing.

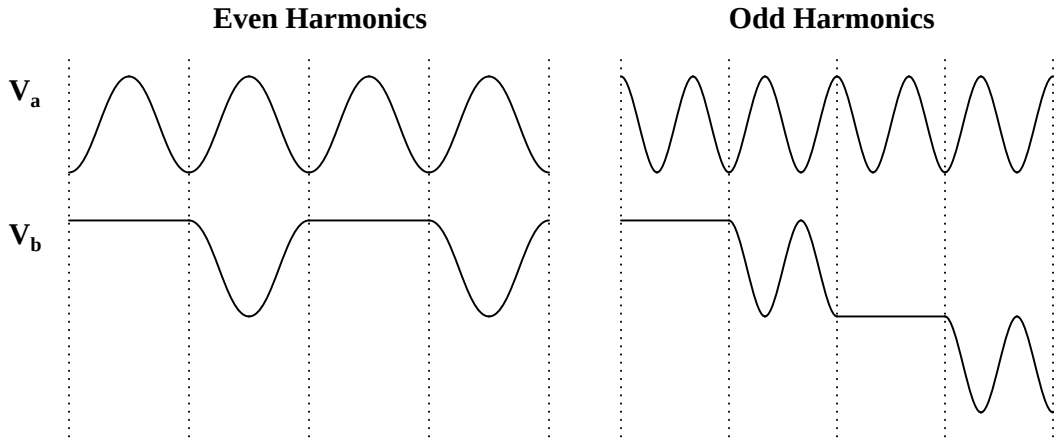

Figure 4-7: Noise aliasing of the CDS integrating demodulator.

4.3.3 Drive Feedthrough

The large voltages needed to actuate the MEMS beam can parasitically couple into the input node of the sense loop through stray capacitances, as illustrated in Figure 4-8. This feedthrough component is in phase with the demodulator clock and in quadrature with the AC sense signal, and is ideally rejected by the CDS demodulator. However, the finite bandwidth of the preamplifier causes phase shift at the modulation frequency, and a fraction of this feedthrough term is demodulated and appears as an offset error at the output. C_{stray} is expected to be much smaller than C_{in}, but the actuation voltages are typically much larger than the sense voltages, so this quadrature offset can be significant. Phase shift introduced by the preamplifier also

attenuates the sense signal as it is demodulated, resulting in a two-fold degradation of the input-referred offset. Heavily bandlimiting the preamplifier also prevents the charge injection and kT/C noise of the reset switch from settling. Therefore, there is a direct trade-off between noise and offset performance.

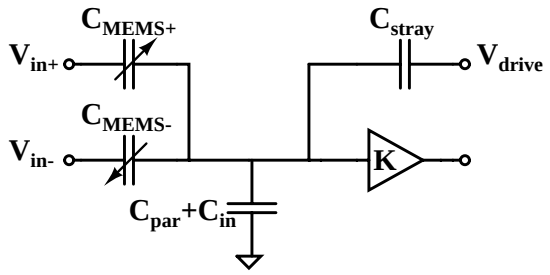

Figure 4-8: Sense node with drive feedthrough.

4.3.4 Charge Injection

Each switch in the sense loop is actually a PMOS transistor. For each switch to turn off, the charge stored in the channel of the device while it was on must flow out of its drain and source junctions [2]. Charges injected into the circuit as the switches turn off result in offsets. The channel charge of each switch is approximately

$$Q_{CH} = WLC_{ox}(V_{switch} - V_{Tp}),$$

where V_{switch} represents the gate drive of the switch and V_{Tp} is the threshold voltage for the PMOS device. To minimize the offsets due to charge injection, it is desirable to size the switches as small as possible. However, the switches also have a non-zero channel resistance which is inversely proportional to the width of the switch:

$$r_{ds} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{Tp})}.$$

In addition to the phase shift from the preamplifier, the on-resistance of the switches also introduces phase shift to the sense signal and the quadrature feedthrough as they

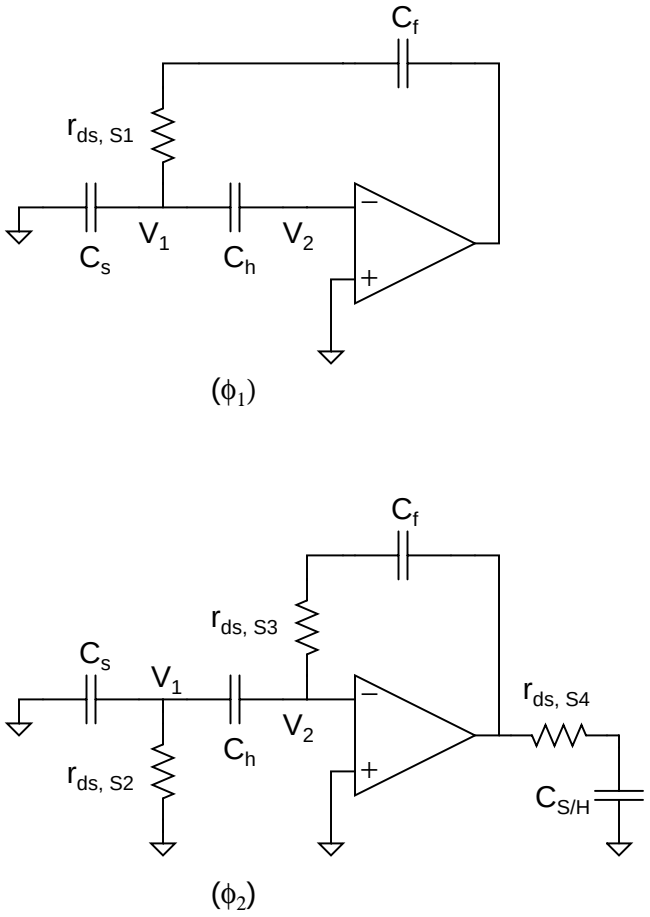

Figure 4-9: On-resistance of the demodulator switches.

are demodulated. This is illustrated in Figure 4-9. During ϕ_1, the on-resistance of switch S1 causes the signal to see a gain transfer function of

$$-\frac{r_{ds}+\frac{1}{C_f s}}{\frac{1}{C_s s}} = -\frac{C_s}{C_f}(r_{ds}C_f s + 1),$$

which is equal to C_s/C_f for zero on-resistance. The resulting phase shift at the up-modulation frequency of 15kHz is

$$\gamma = \arctan(r_{ds}C_f(2\pi)(15\text{kHz})),$$

which is positive and can be used to cancel the negative phase shift introduced by the preamplifier. Thus, there is a direct trade-off between charge injection and drive

feedthrough offsets. In addition, during the autozero phase ϕ_2, the on-resistance of switch S2 creates a settling time constant for the charge injection and kT/C noise of the reset switch. One side of the feedback capacitor C_f moves between node v_1 and v_2, and if the voltages at the two nodes are different, the change in voltage must settle onto C_f through the switch resistance. The sampling of the output of the demodulator onto capacitor $C_{S/H}$ must also settle through the switch resistance of S4. These switches must be sized appropriately to ensure sufficient settling during their switch phases.

4.4 Closed-Loop Stability Analysis

The target closed-loop bandwidth of the sense loop is 1.5kHz. However, because of the up-modulation of the input signal, the sense loop is not a linear time-invariant system, so traditional feedback analysis cannot be applied. Nevertheless, previous work has confirmed that the output step response is well-predicted by the effective loop transfer function seen by the DC input voltage [1].

The sense loop transfer function is found referring to Figure 4-3. First, the non-inverting input voltage sees a capacitive divider:

$$\begin{aligned} v_{in+}\left(\frac{C_{\text{MEMS+}}}{C_{\text{MEMS+}}+C_{\text{MEMS-}}+C_{par}+C_{in}}\right) &= v_{in+}\left(\frac{C_o+C_m\sin(\omega_m t)}{2C_o+C_{par}+C_{in}}\right) \\ &\approx v_{in+}\left(\frac{C_o}{C_{par}+C_{in}}+\frac{C_m\sin(\omega_m t)}{C_{par}+C_{in}}\right), \end{aligned}$$

where it is assumed that $2C_o \ll C_{par}+C_{in}$. The first term represents a DC component due to the static capacitance of the MEMS transducer, and the second term is the up-modulated component due to the modulating capacitance. Equivalently, the second term is also the AC sense current integrated by the capacitance $C_{par}+C_{in}$. The DC component is rejected by the CDS demodulator, so only the up-modulated component is of interest.

In addition, nonidealities in the drive loop can result in a modulation frequency

that is not precisely the mechanical resonant frequency of the MEMS transducer. This causes a small phase shift, represented by φ, between the beam velocity and the drive voltage, which also serves as the demodulator phase reference. Because the AC sense current is in phase with the beam velocity, this phase shift will attenuate the sense signal as it is demodulated. Thus, the effective gain of the MEMS capacitive divider is

$$\frac{C_m \sin(\omega_m t)}{C_{par} + C_{in}} \cos\varphi.$$

It was stated previously that $\varphi = -4.3°$, so $\cos\varphi = 0.9972 \approx 1$.

This AC term is amplified by the gain of the preamplifier at the modulation frequency, which is denoted by K. The bandwidth of the preamplifier also introduces phase shift θ at the modulation frequency which also decreases the gain of the sense loop signal at the demodulator. Therefore, the effective gain of the preamplifier is

$$K \cos\theta.$$

The phase shifts from the MEMS transducer and the preamplifier provide a net phase shift of $\varphi + \theta$ to the signal, so the net effective gain is

$$\left(\frac{C_m \sin(\omega_m t)}{C_{par} + C_{in}}\right)(K)\cos(\varphi + \theta).$$

Referring to Figure 4-3, the difference equation of the CDS integrating demodulator is given by

$$v_c[n-1] - v_c[n] = \frac{C_s}{C_f}(v_a[n - \frac{1}{2}] - v_a[n-1]),$$

where the discrete time samples are related to their corresponding continuous time signals by $v[n] = v(nT)$, and T is the demodulator clock period. The Z-transform of this difference equation is

$$\frac{V_c}{V_a}(z) = \frac{C_s}{C_h}\frac{z^{-1/2} - z^{-1}}{z^{-1} - 1}.$$

Substituting $z = e^{j\omega T}$ yields the discrete-time frequency response:

$$\frac{V_c}{V_a}(e^{j\omega T}) = -\frac{C_s}{C_f}e^{j\omega T/4}\frac{\sin(\omega T/4)}{\sin(\omega T/2)}.$$

Because the behaviour of interest of the CDS integrator is for a low-frequency input that has been up-modulated, this expression can be simplified by noting that $\omega = \omega_m + \omega_s$, where ω_m is the resonant frequency of the MEMS structure and ω_s is the frequency of the input voltage signal. Using the fact that $\omega_m T = 2\pi$ and assuming that the input signal has been appropriately bandlimited so that $\omega_s \ll \omega_m$, this transfer function becomes

$$\begin{aligned}
\frac{V_a}{V_c} &= -\frac{C_s}{C_f}e^{-j(\omega_m+\omega_s)T/4}\frac{\sin((\omega_m+\omega_s)T/4)}{\sin((\omega_m+\omega_s)T/2)} \\
&= -\frac{C_s}{C_f}e^{-j\omega_m T/4}e^{-j\omega_s T/4}\frac{\sin(\omega_m T/4)\cos(\omega_s T/4) + \cos(\omega_m T/4)\sin(\omega_s T/4)}{\sin(\omega_m T/2)\cos(\omega_s T/2) + \cos(\omega_m T/2)\sin(\omega_s T/2)} \\
&= -\frac{C_s}{C_f}\frac{e^{-j\omega_s T/4}}{j}\frac{\cos(\omega_s T/4)}{\sin(\omega_s T/2)} \\
&\approx -\frac{C_s}{C_f}\frac{1}{j}\frac{1}{\omega_s T/2} \\
&= -\frac{C_s}{C_f}\frac{2}{T}\frac{1}{j\omega_s}.
\end{aligned}$$

Therefore, the effective transfer function seen by the input signal is

$$\frac{V_a}{V_c}(s) = \frac{C_s}{C_f}\frac{2}{T}\frac{1}{s}$$

in agreement with the intuition given previously. It is assumed that the fully differential signal chain is appropriately connected for global negative feedback, and that the forward loop transfer function is non-inverting.

In the above derivation, by assuming that $\omega_s \ll \omega_m$, the term $e^{-j\omega_s T/4}$ was approximated as one. Including this term in the transfer function gives

$$\frac{V_a}{V_c}(s) = \frac{C_s}{C_f}\frac{2}{T}\frac{1}{s}\ e^{-sT/4}.$$

This quarter-cycle time delay reflects the fact that a quarter-cycle shift in the sense signal would result in no output at the integrating demodulator.

It should also be noted that the CDS integrator cannot truly provide infinite gain to the demodulated signal. The finite DC gain of the demodulator op amp, represented by A_o, shifts the actual integrator pole into the left-half plane:

$$\frac{V_a}{V_c}(s) = \frac{A_o^2}{1 + A_o^2\frac{C_f}{C_s}\frac{T}{2}s}\ e^{-sT/4},$$

where the effective DC gain of the CDS integrator is A_o^2 due to the nature of the offset sampling.

As discussed previously, the non-zero on-resistance of the demodulator switches introduces a phase shift γ to the sense signal as it is demodulated:

$$\gamma = \arctan(r_{ds}C_f(2\pi)(15\text{kHz})).$$

This phase shift sums with the phase shifts from the MEMS transducer and the preamplifier.

It can be assumed that the output buffer has unity gain and a bandwidth much greater than 1.5kHz, so that it contributes negligible dynamics at the frequencies of interest. The output voltage can be attenuated for feedback, and connected to the MEMS capacitor plates. The feedback voltage sees the same capacitive divider as the input voltage, but with a modulating capacitance that is of opposite phase.

The block diagram for the sense loop is shown in Figure 4-10. The effective loop transfer function seen by the low-frequency input voltage is approximately

$$
\begin{aligned}
L(s) &= \left(\frac{C_m}{C_{par}+C_{in}}\right)(K)(\cos(\varphi+\theta+\gamma))\left(\frac{A_o^2}{1+A_o^2\frac{C_f}{C_s}\frac{T}{2}s}\ e^{-sT/4}\right) \\
&\approx \left(\frac{C_m}{C_{par}+C_{in}}\right)(K)(\cos(\varphi+\theta+\gamma))\left(\frac{C_s}{C_f}\frac{2}{T}\frac{1}{s}\ e^{-sT/4}\right).
\end{aligned}
$$

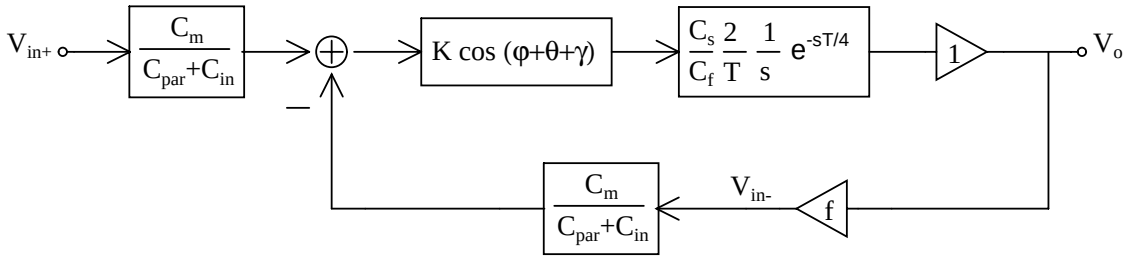

Figure 4-10: Block diagram for sense loop feedback.

The unity gain crossover frequency, and thus the closed-loop bandwidth of the sense loop, is well-approximated by

$$
\omega_c = \left(\frac{C_m}{C_{par}+C_{in}}\right)(K)(\cos(\varphi+\theta+\gamma))\left(\frac{C_s}{C_f}\frac{2}{T}\right).
$$

It was stated previously that the magnitude of the modulating capacitance C_m is 100fF, the output trench capacitance of the MEMS structure C_{par} is 1pF, and the phase error of the drive loop from resonance is $+4.3°$. The preamplifier has an input capacitance C_{in} of roughly 1pF, a gain of about 200, and a bandwidth of 250kHz. The resulting phase shift at the modulation frequency is

$$
\theta = -\arctan\left(\frac{f_m}{f_{BW}}\right) = -\arctan\left(\frac{15\text{kHz}}{250\text{kHz}}\right) = -3.4°.
$$

To achieve the target crossover frequency of 1.5kHz, the gain of the demodulator during ϕ_1 must be

$$\begin{aligned}\frac{C_s}{C_f} &= \omega_c\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K(\cos(\varphi+\theta+\gamma))}\right)\left(\frac{T}{2}\right)\\ &\approx (2\pi)(1.5\text{kHz})\left(\frac{100\text{fF}}{1\text{pF}+1\text{pF}}\right)\left(\frac{1}{200}\right)\left(\frac{1}{15\text{kHz}}\right)\left(\frac{1}{2}\right)\\ &\approx \frac{1}{32}.\end{aligned}$$

Accordingly, C_s and C_f were chosen to be 1pF and 32pF, respectively. The phase margin is

$$\phi_{\text{PM}} = 180 + \angle L(j\omega_c) = 180 - 90 - 2\pi\left(\frac{1.5\text{kHz}}{15\text{kHz}}\right)\left(\frac{1}{4}\right)\frac{180}{\pi} = 81^\circ.$$

The on-resistance of the demodulator switches is about 20kΩ, so the phase shift introduced by the demodulator to the sense signal is

$$\gamma = \arctan(r_{ds}C_f(2\pi)(15\text{kHz})) = \arctan((20\text{k}\Omega)(32\text{pF})(2\pi)(15\text{kHz})) = 3.45^\circ.$$

Figures 4-11 and 4-12 illustrate the predicted open loop frequency and closed-loop step responses of the sense loop for unity gain feedback based on the effective loop transfer function derived. For a ±20% variation in C_m, the open loop crossover frequency varies by ±20%, which causes negligible change in the phase margin. The closed-loop gain changes by less than 0.1ppm and exhibits no overshoot, which is consistent with a system with about 80° of phase margin. The rise times range from about 180μs to 280μs, which corresponds well with a system with a 1.2 to 1.8kHz bandwidth. With feedback, variations in the open loop gain are traded-off for variations in the closed-loop bandwidth, and the accuracy of the closed-loop gain depends instead on the matching of the feedback resistors (if used) and the matching of the modulating capacitance values.

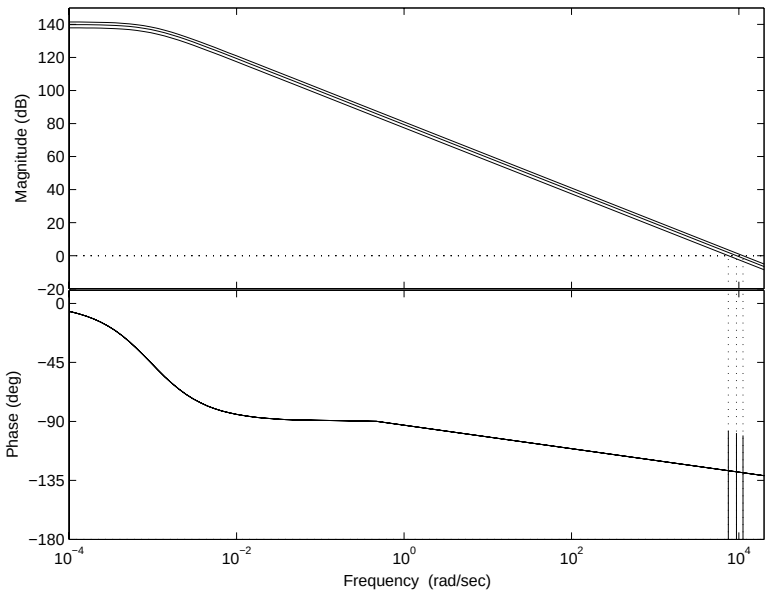

Figure 4-11: Open loop frequency response of sense loop transfer function.

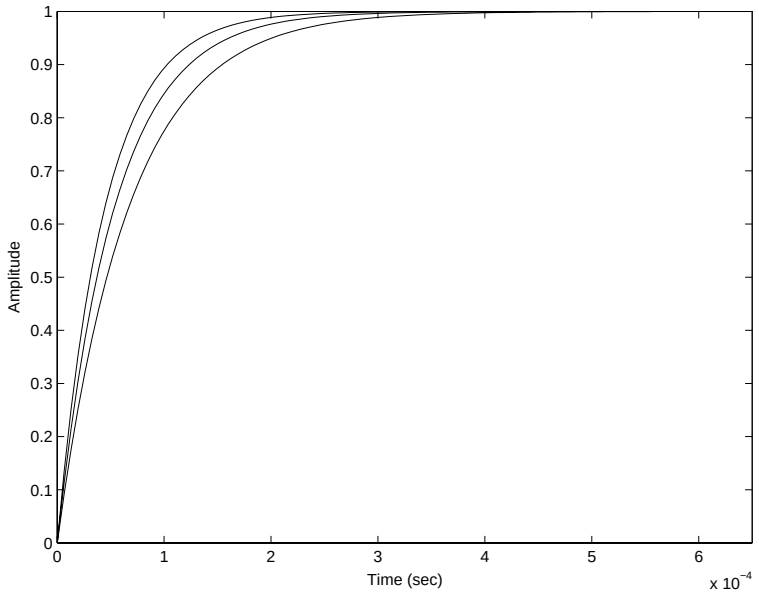

Figure 4-12: Time domain step response of sense loop transfer function in unity gain feedback.

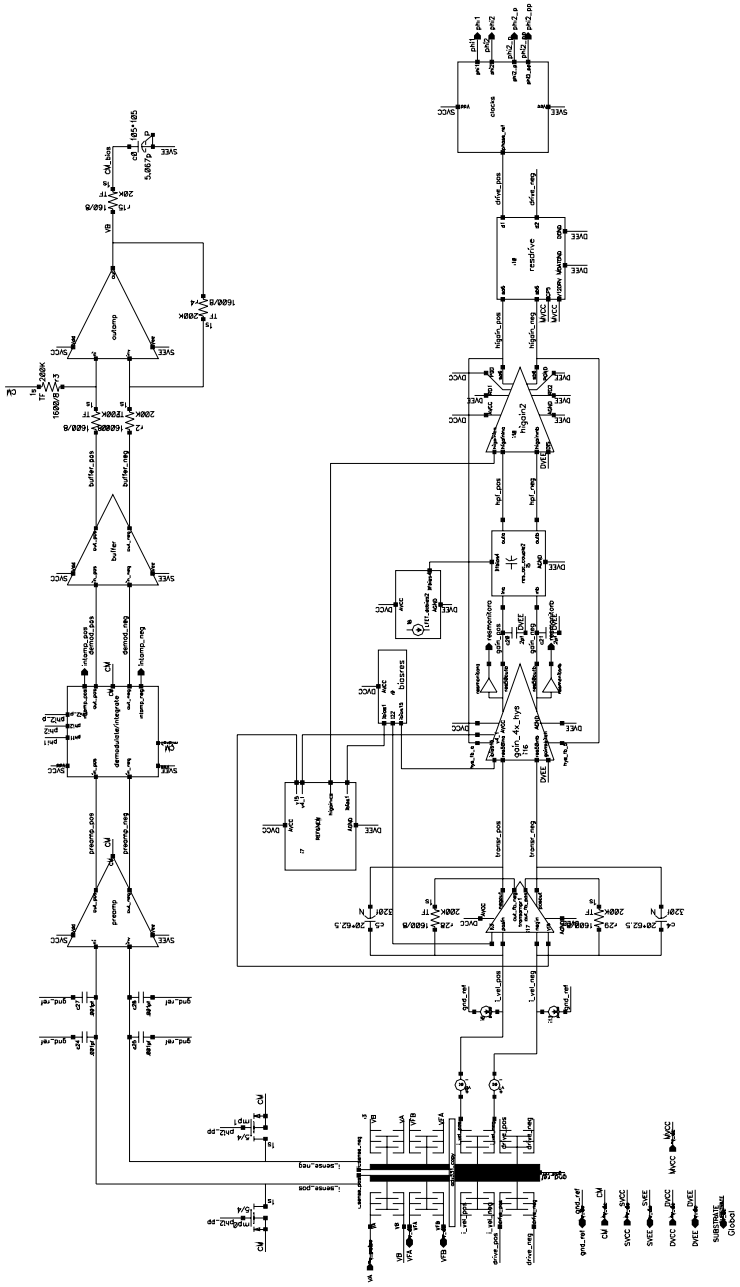

Figure 4-13: MEMS-based amplifier system with the MEMS transducer, drive loop, and sense loop.

	Preamplifer	Demod. Op Amp	SF Buffer	Diff. Op Amp
Gain	200	1000	0.98	500
BW/X-Over	250kHz	3.6MHz	37MHz	2.5MHz
Φ_m	N/A	87°	N/A	82°
Noise	4.9 $\frac{\text{nV}}{\sqrt{\text{Hz}}}$	6.3$\frac{\text{nV}}{\sqrt{\text{Hz}}}$	45$\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$	7$\frac{\mu\text{V}}{\sqrt{\text{Hz}}}$
Input Swing	1.4–7.0V	0.1–7.6V	0–7.8V	0.1–7.9V
Output Swing	3.2–8.8V	1.3–8V	1.7–9.6V	0.1–9.7V
Current	300μA	360μA	170μA	270μA

Table 4.1: Summary of specifications for circuit blocks in the sense loop.

4.5 Sense Loop Circuits

Figure 4-13 shows the sense loop signal chain with the MEMS transducer and the drive loop. The AC sense current from the MEMS beam is detected and amplified by a preamplifier, and then simultaneously demodulated and integrated by the CDS switched-capacitor circuit. A source follower buffers the output of the demodulating integrator into a difference amplifier which converts the differential signal into a single-ended output and can drive the input or feedback plates of the MEMS transducer. Table 4.1 summarizes of the key specifications for each circuit block. The phase margin Φ_m is not relevent for the preamplifier and the source follower, which are open loop. The noise spectral densities of the amplifiers listed in the table are at 15kHz for the preamplifier and the demodulator op amp, and at 1Hz for the source follower buffer and the difference op amp.

4.5.1 Low-Noise Preamplifier

The preamplifier, shown in Figure 4-14, is essentially a fully differential folded-cascode with common-mode feedback and constant-g_m current biasing. The folded-cascode amplifier consists of a PMOS input stage (MP0 and MP1) and NPN common-base stage (QN0 and QN1). PMOS source followers (MP18 and MP19) buffer the output for low output impedance. The 400kΩ shunt resistors (R2 and R3) dominate the load and provide a differential gain of 200, and capacitors at the high impedance node (C0

and C1) bandlimit the frequency response to 250kHz. The frequency response for one of the differential outputs is shown in Figure 4-15. The preamplifier uses 300μA of current, and has an input swing from 1.4V to 7.0V. Thus, the high impedance node between the MEMS beam and the preamplifier may be biased to any voltage inside this range. The preamplifier has an output swing of 3.2 to 8.8V.

Common-mode feedback is implemented by a PMOS differential pair (MP5 and MP6), which compares the output common-mode voltage level with a reference (CM), and QN4 servos the currents through QN2 and QN3 until the output common-mode voltage is equal to the reference. Because the currents through QN2 and QN3 are about 5 times larger than the current through QN4, QN5 is used to reduce systematic offset due to base currents. The base of QN5 is also used to bias the common-base stage of the cascode.

The current reference for the preamplifier is generated by a constant-g_m bias circuit, implemented by MN0, MN1, MP23, and MP24. This topology of back-to-back PMOS and NMOS current mirrors result in transconductances that are determined exclusively by the degeneration resistor R9 and the relative geometries of the transistors, independent of temperature, assuming that the Early effect is negligible [2]. By referencing all current sources with this bias network, the transconductances of all transistors in the preamplifier, and thus also the preamplifier gain, remain constant over temperature. MN2, MN3, MP15, and MP16 provide cascoding to reduce Early effect in the bias network, and MP22 ensures start-up, so that the inherent positive feedback latches in the desired direction.

As the front-end amplifier of the sense loop, the added noise of the preamplifier is critical in the overall noise performance of the MEMS-based amplifier. Thus, the preamplifier must be designed to be as low-noise as possible. The preamplifier was chosen to be open loop, to avoid voltage noise up-mixing into the sense current bandwidth, which is an inherent problem with feedback amplifiers that have a modulating impedance connected to its input terminals [3].

The input transistors were chosen to be PMOS. Although NMOS devices have lower thermal noise than their PMOS counterparts due to the larger mobility of

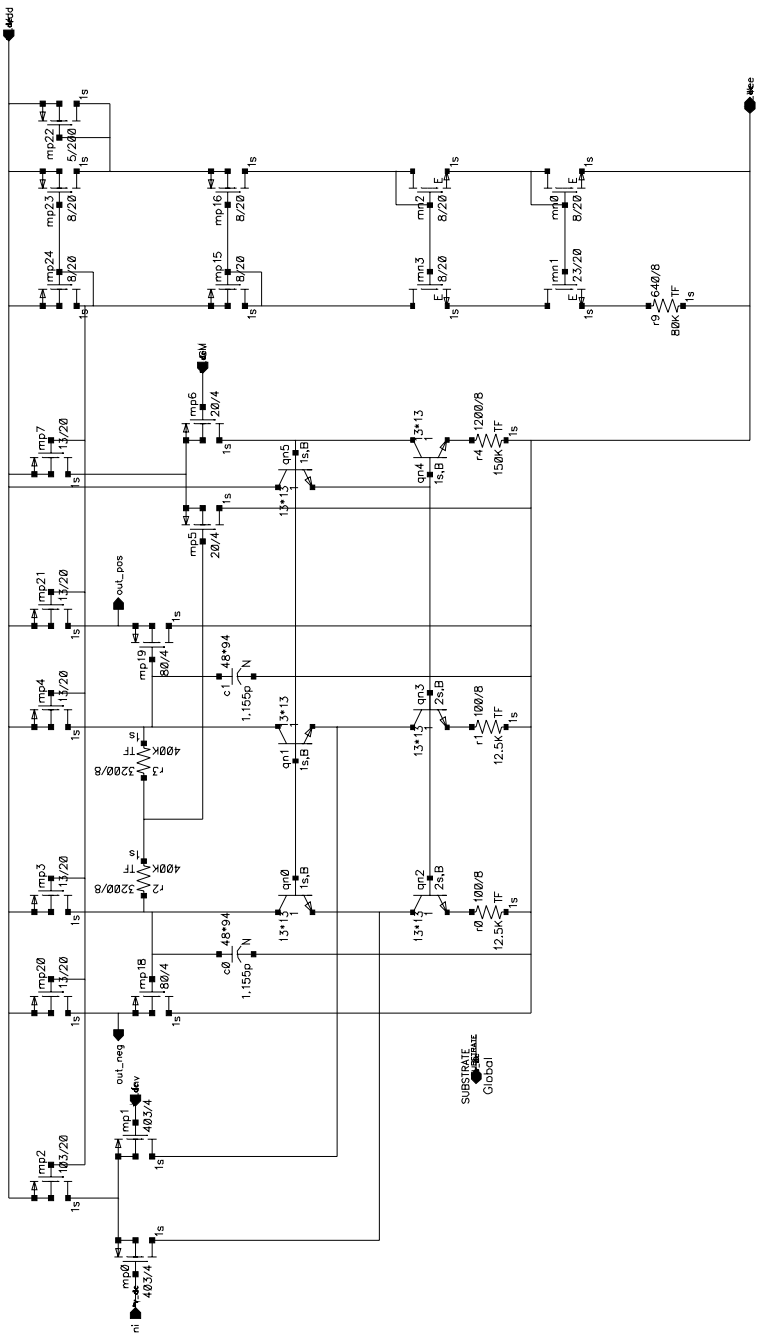

Figure 4-14: Low-noise preamplifier.

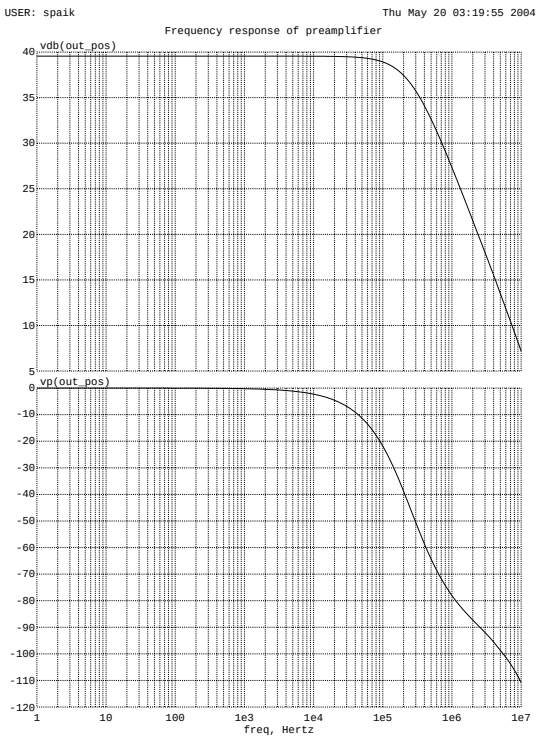

Figure 4-15: Preamplifier frequency response.

electrons, their noise corners are also at higher frequencies. Thus, PMOS devices were found to have less noise at 15kHz. The transconductances of the input transistors should be as large as possible to decrease the input-referred noise of the preamplifier. Thus, MP0 and MP1 are wide and biased with large drain currents. However, a wide transistor also increases the input capacitance of the pre-amplifier, attenuating the AC signal current from the MEMS beam. Therefore, for a fixed amount of power, there is an optimum width to maximize the signal-to-noise ratio. The optimum trade-off was estimated to occur when the input capacitance of the pre-amplifier is equal to the output capacitance of the MEMS beam, which is about 1pF, and the input transistors were sized accordingly.

To minimize the noise contribution of the bipolar current sources QN2 and QN3, it was necessary to heavily degenerate them to reduce their effective transconductances. Similarly, the PMOS current sources MP3 and MP20 were designed to have long lengths to decrease their transconductances, and thus their noise contribution at the

output. The trade-off is reduced head-room as this increases their saturation voltages. Because the sense loop utilizes feedback, the preamplifier will not need to have large output swing in steady state due to the large gain of the demodulating integrator proceeding it. As a cautionary design measure, however, the preamplifier should be designed with some output headroom to accomodate changes in the output voltage due to mismatches in the input differential pair transistors, or voltage offsets due to charge injection of the reset switches. For an estimated charge injection of 15mV from the reset switch, the output of the preamplifier must have at least a $(15\text{mV})(200) = 3\text{V}$ swing at the output.

Because the current through the common-base leg of the folded-cascode does not affect gain, the bias currents were chosen to be small, to decrease the collector and drain current noise of transistors MP3 and MP4, and therefore their noise contributions at the output. The noise spectral density at 15kHz referred to the input of the preamplifier was simulated to be about $4.9\text{nV}/\sqrt{\text{Hz}}$ for a single input side.

4.5.2 CDS Integrating Demodulator

Switches

Figure 4-16 shows the switches and op amp that make up the CDS integrating demodulator. All switches are PMOS, instead of NMOS, because the substrate of a PMOS may be tied to its source, for a smaller threshold voltage, and thus a smaller channel resistance for the same gate drive, than the NMOS. The on-resistance of the demodulator switches MP0, MP1, MP2, MP3, MP4, and MP5 introduce additional undesired phase shift to the AC sense signal and the quadrature offset. Thus, these switches are not minimum-sized to reduce their channel resistance when turned on, at the cost of increased charge-injection. Because the terminals of these switches remain close to zero volts, the gate drive of these switches can afford to be decreased, to reduce charge injection and gate drive feed-through. With a width of 17.6μm and a gate drive of 5$\pm$1.5V, the maximum on-resistance is simulated to be 20kΩ. MP12 and MP13 must have a gate drive of 5$\pm$5V because their terminals see the entire span of

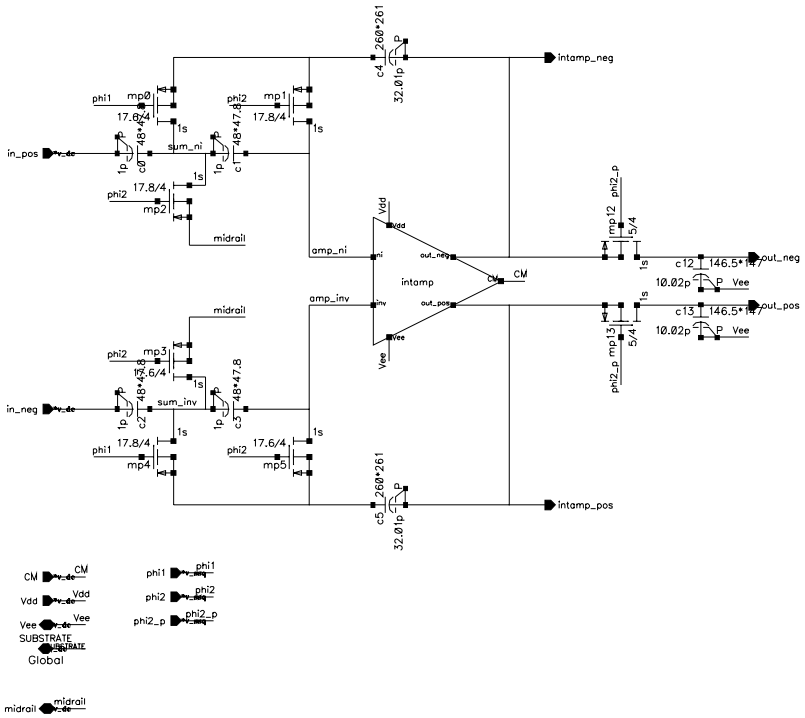

Figure 4-16: CDS integrating demodulator.

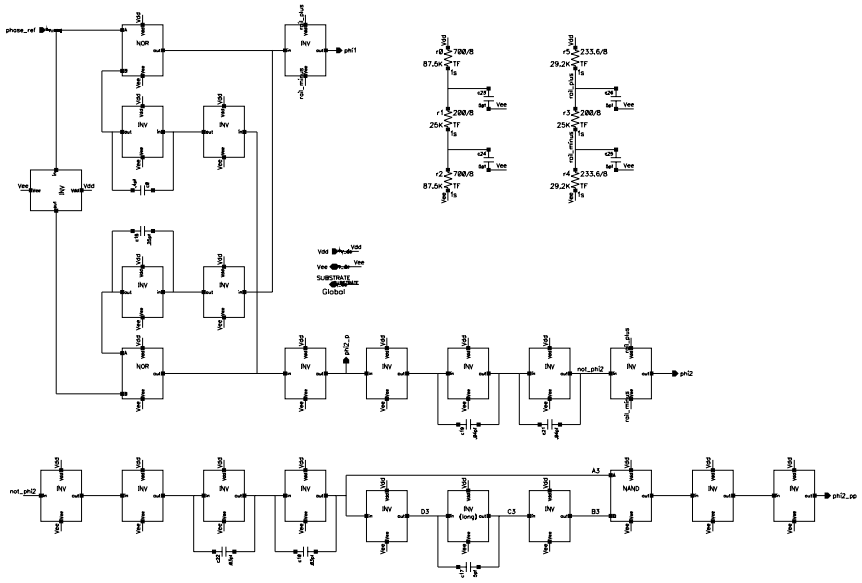

Figure 4-17: Switch drives for the CDS integrating demodulator.

the output swing, and can also be minimum-sized since their on-resistance of 25kΩ allows for sufficient settling onto $C_{S/H}$ during the half-cycle.

Clocks

The clock implementation for the switch drives must guarantee one set of non-overlapping clocks for the CDS scheme. It is also necessary to generate ϕ_2', which is time-advanced in phase relative to ϕ_2, and to generate ϕ_2'', which turns on after ϕ_2 but is only on briefly (2μs). It should be noted that because the switches are PMOS, the switches are turned on when the gate drive is low, and turned off when the gate drive is high. The feedback logic circuit shown in Figure 4-17 ensures that ϕ_1 and ϕ_2' do not overlap. A series of capacitively loaded inverters make ϕ_2 a time-delayed version of ϕ_2', as desired. More capacitively loaded inverters delay the turn-on of ϕ_2'', and logic with an additional time delay and a NAND gate establish the duration of the turn-on time of ϕ_2''. Reduced gate drives for ϕ_1 and ϕ_2 are implemented by resistively dividing down the supply rail voltages seen by the inverters. The inverters and nor gates use minimum-sized NMOS with PMOS pull-ups sized for equal pull-down and pull-up drive capability. Because the delay between ϕ_2 and ϕ_2'' is particularly long, one inverter with a long length is used to avoid using a large capacitor to achieve the delay.

Integrator Op Amp

The op amp used in the demodulator is shown in Figure 4-18. The thermal noise of this amplifier is also aliased into the sense signal bandwidth, so the design of this amplifier must also be low-noise and appropriately bandlimited. This topology is similar to the pre-amplifier. A PMOS input stage (MP1 and MP2) followed by an NPN common-base stage (QN0 and QN1) form a folded-cascode. To avoid loading the high-impedance output node with resistors necessary for common-mode feedback, the output is first buffered by emitter followers (QN4 and QN5) to maintain a high differential gain of greater than 1000 over the output swing range. Capacitors C2 and C3 provide dominant pole compensation for a crossover frequency of 3.6MHz,

and phase margin of 87°. These capacitors also aid the stability of the common-mode feedback loop. The open loop frequency response is shown in Figure 4-19. This op amp uses 360μA of current, has an input swing of 0.1V to 7.6V, and an output swing from 1.3V to 8V. Since this op amp is used in feedback, its input terminals should not move very much. However, charge injection of the demodulator switches can change the common-mode input voltage, so the op amp should be designed with some input headroom to remain in its high-gain region. Referring to Figure 4-22, because the output of the difference amplifier following the demodulator is

$$5\text{V} + V_+ - V_-,$$

the output of the integrator op amp, as well as the source follower buffer proceeding it, only needs to swing 5±2.5V for the output of the sense loop to swing the full 0 to 10V scale.

The output of the op amp is at its high-impedance node, instead of at the output of the emitter followers for a lower output resistance. This is due to the capacitors the op amp must drive in its feedback path as well as the sample-and-hold capacitor at the output. If the output of the op amp were at the output of the emitter followers, the large capacitance at the output of the amplifier would result in an additional low-frequency pole in the forward path of the op amp, which would degrade stability. Instead, because the output of the op amp is at its high-impedance node, added capacitance at that node serves to lower the dominant pole location and the crossover frequency, improving stability. During ϕ_2 when the op amp is driving $C_f = 32\text{pF}$ and $C_{S/H} = 10\text{pF}$, the capacitance at the high-impedance node increases by a factor of

$$\frac{10\text{pF} + 32\text{pF} + 10\text{pF}}{10\text{pF}} \approx 5.2,$$

for a closed-loop bandwidth of about 690kHz, which is the bandwidth used for the noise aliasing calculations. The noise spectral density at 15kHz referred to the input of the integrator op amp was simulated to be 6.3nV/$\sqrt{\text{Hz}}$ for a single input side.

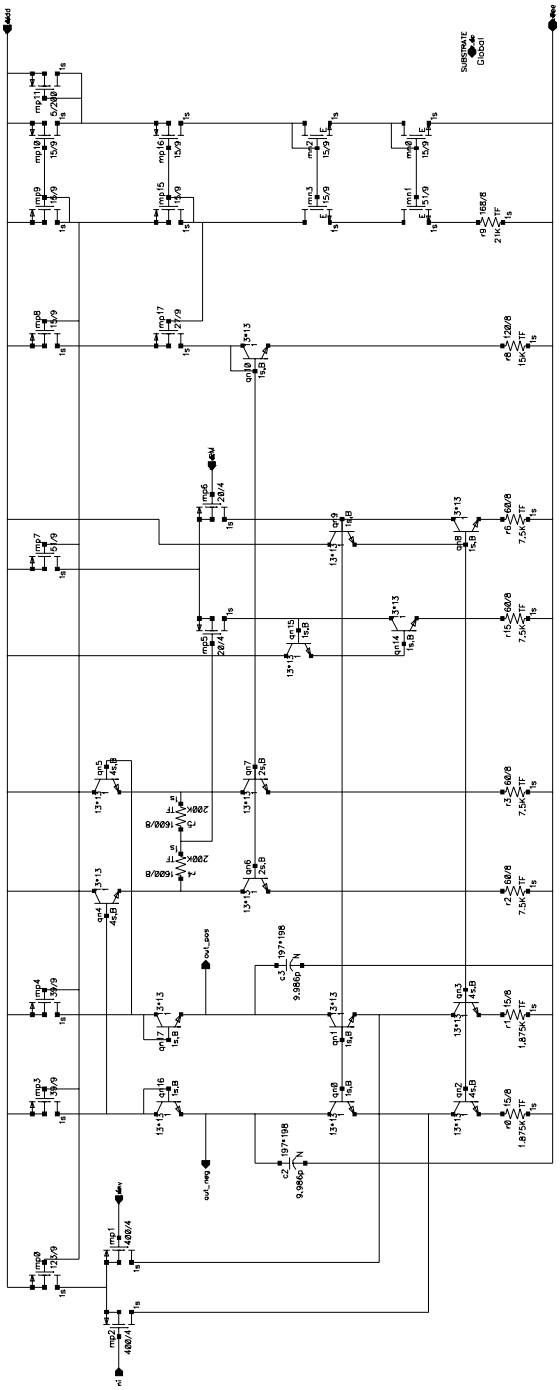

Figure 4-18: Op amp used in integrating demodulator.

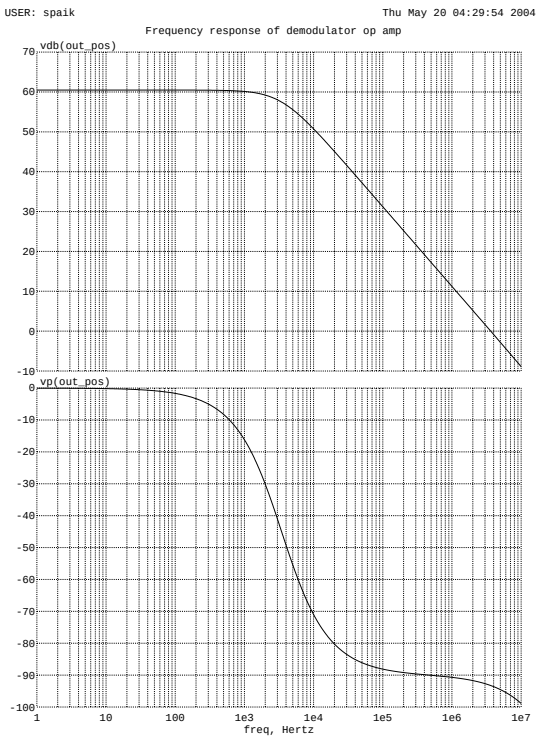

Figure 4-19: Demodulator op amp open loop frequency response.

4.5.3 Source Follower Buffer

The source follower together with an op amp configured as a difference amplifier serve as the output buffer which converts the differential sense signal into a single-ended output. The source follower simply functions to avoid loading the capacitor $C_{S/H}$ at the output of the integrating demodulator with the resistors of the difference amplifier. It must also provide enough current to drive a 5V difference into the difference amplifier. The circuit is illustrated in Figure 4-20, and its frequency response is shown Figure 4-21. The gain is 0.98, and the bandwidth is about 37MHz. The noise of the stages following the demodulator is not aliased so the bandwidth of this buffer does not need to be limited. The sense loop signal is at DC when it reaches this stage, so its low-frequency noise, which represents the offset drift of the overall system, is of interest, and the buffer has $45\mu\text{V}/\sqrt{\text{Hz}}$ of noise at 1Hz. The input can swing from 0V to 7.8V, the output can swing from 1.7V to 9.6V, and this stage uses a total of 170μA of current.

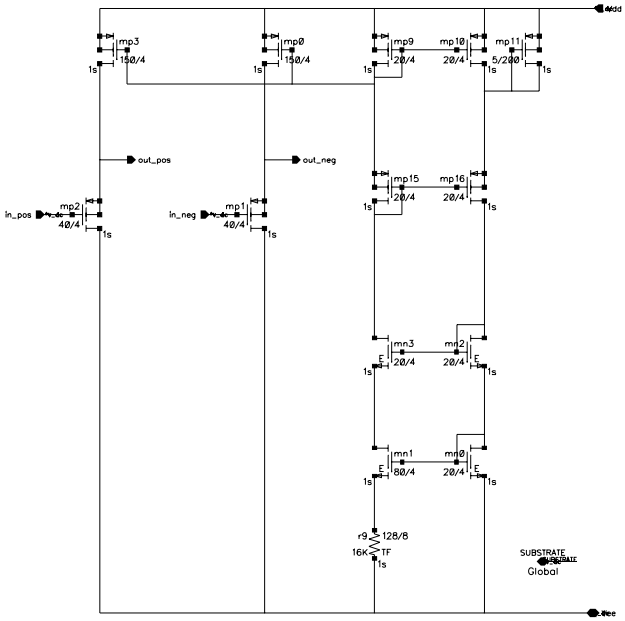

Figure 4-20: Source follower buffer.

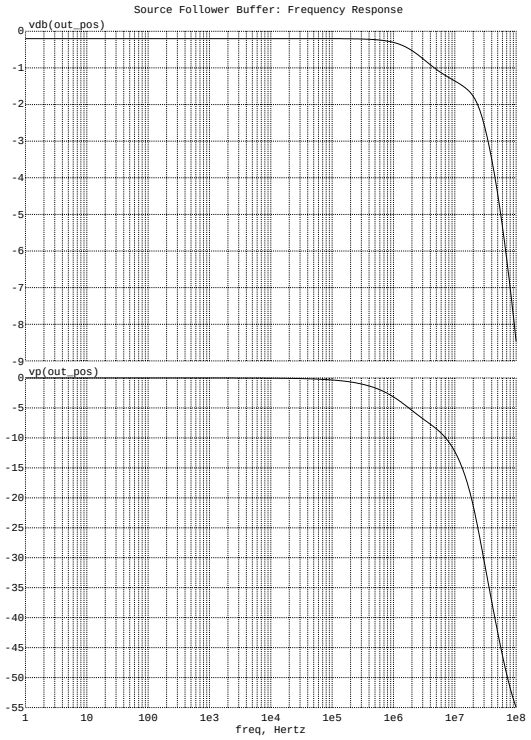

Figure 4-21: Source follower frequency response.

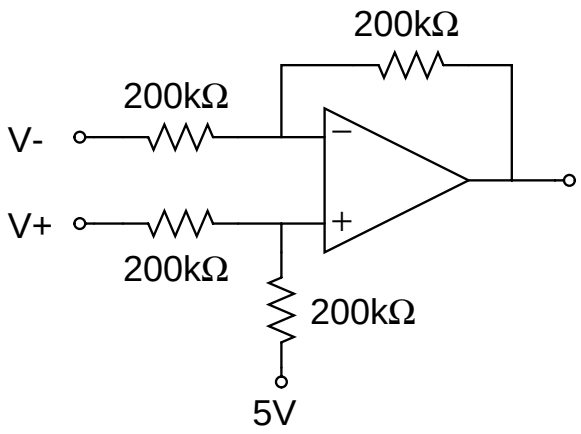

Figure 4-22: Difference amplifier.

4.5.4 Difference Amplifier

The difference amplifier is shown in Figure 4-22, which simply takes the difference between its two input voltages and provides a single-ended output. The op amp used in the difference amplifier is shown in Figure 4-23. The op amp topology is essentially a PMOS differential pair with an NPN current mirror load, NMOS source follower for buffering, and a NMOS common source amplifier for additional gain. Since the amplifier has two gain stages, and consequently two dominant poles, Miller compensation is employed to establish a low-frequency pole at the output of the first gain stage to dominate the unity crossover frequency. The capacitive feedback around the second gain stage lowers the effective output impedance of the amplifier and moves the second pole to a higher frequency. A resistor (r7) in the compensation network introduces a zero in the feedback admittance to aid stability. A small amount of degeneration in the current mirror helps reduce the the input-referred offset drift of the bipolar transistors, and also boosts slightly the output resistance. Transistors MN0 and MN2 balance the loading on the current mirror. The output of the op amp drives the input or feedback plates of the MEMS transducer, so it must have adequate output current. The output transistors are also designed to be wide to decrease the saturation voltage of the devices for rail-to-rail output swing within 300mV of the supply voltages. Because of the feedback of the difference amplifier and the high

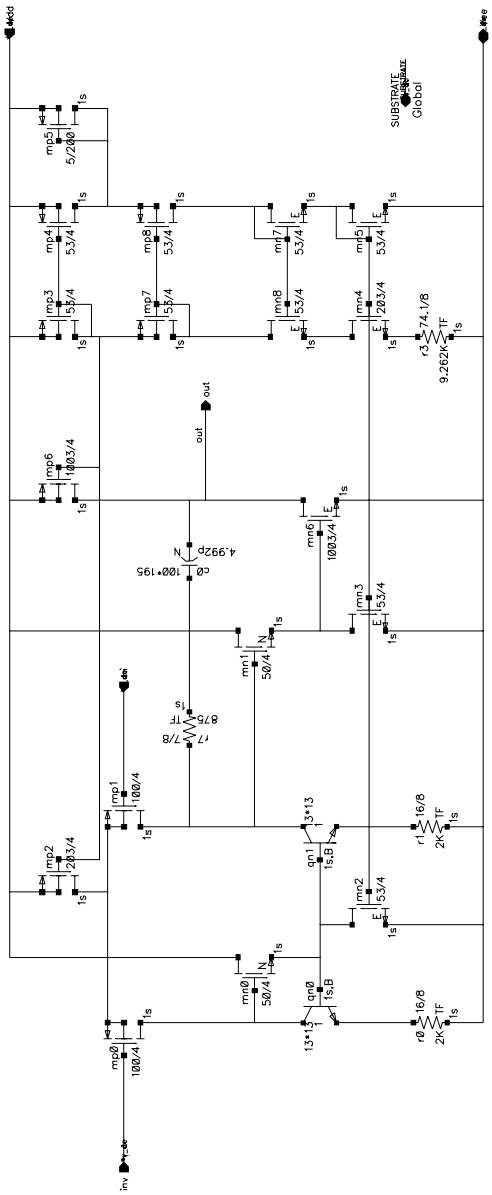

Figure 4-23: Op amp used in difference amplifier.

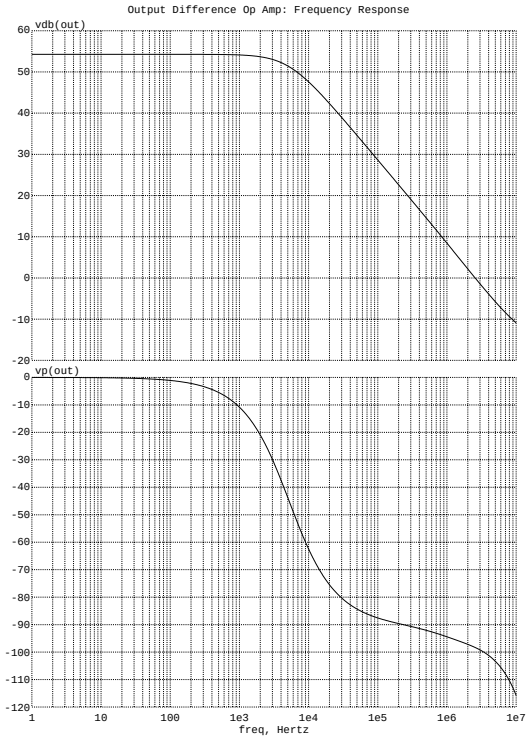

Figure 4-24: Frequency response for op amp used in difference amplifier.

open loop gain of the op amp, its input terminals do not move very much, so its input voltage range does not matter. Nonetheless, it was found to be from 0.1V to 7.9V. The op amp has an open loop gain of about 500, and crosses unity gain at 2.5MHz with a phase margin of 82°. The noise spectral density at 1 Hz referred to the input of this op amp was found to be $7\mu\text{V}/\sqrt{\text{Hz}}$. It also uses 270μA of current.

4.6 Noise Analysis

4.6.1 Amplifier Noise

Figure 4-25 shows the three sources of noise in the sense loop due to each of the amplifiers. The input-referred noise of the preamplifier, demodulator op amp, and output buffer are represented by v_{n1}, v_{n2}, and v_{n3}, respectively. The task is to determine the input-referred noise of the overall sense loop.

The preamplifier noise is amplified by the preamplifier gain, and the thermal noise

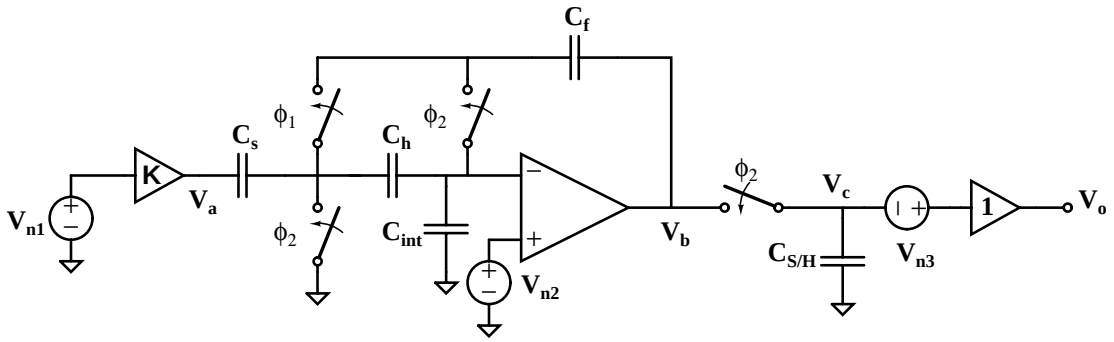

Figure 4-25: Sense loop signal chain for noise analysis.

at the odd harmonics of the clock frequency are demodulated to DC. Therefore, the noise at the output of the sense loop in the bandwidth of the DC output voltage is given by

$$v_{no1} = v_{n1}|_{\omega_m}(K)\left(\frac{C_s}{C_f}\frac{2}{T}\frac{1}{s}\right)\sqrt{2N_1},$$

where $v_{n1}|_{\omega_m}$ is the noise of the preamplifier at the modulation frequency in volts/$\sqrt{\text{Hz}}$, and N_1 is the number of odd harmonics of the modulation frequency less than the preamplifier bandwidth. The thermal noise at these frequencies is assumed to be constant since the modulation frequency is above the noise corner frequency of the preamplifier, and the noise adds in a root-mean-square fashion because the thermal noise at the different frequencies are uncorrelated. The factor of $\sqrt{2}$ accounts for the fully differential signal chain with two statistically independent paths for the noise.

As found previously, the magnitude of the sense loop signal gain is given by

$$\begin{aligned} G_{sense} &= \left(\frac{C_m}{C_{par}+C_{in}}\right)(K)(\cos(\varphi+\theta+\gamma))\left(\frac{A_o^2}{1+A_o^2\frac{C_f}{C_s}\frac{T}{2}s}\right) \\ &\approx \left(\frac{C_m}{C_{par}+C_{in}}\right)(K)\left(\frac{C_s}{C_f}\frac{2}{T}\frac{1}{s}\right). \end{aligned}$$

To find the input-referred noise due to the preamplifier, the preamplifier contribution to the output noise is divided by this gain:

$$v_{ni1} = \frac{v_{no1}}{G_{sense}} = v_{n1}|_{\omega_m} \left(\frac{C_{par} + C_{in}}{C_m} \right) (\sqrt{2N_1}).$$

The noise at the input of the preamplifier at 15kHz was simulated to be $4.9\text{nV}/\sqrt{\text{Hz}}$. Since the bandwidth of the preamplifier is 250kHz, there are $N_1 = 8$ odd harmonics of 15kHz less than 250kHz. A number of odd harmonics are aliased into the sense signal bandwidth, but the wide bandwidth of the preamplifier is necessary to sufficiently suppress the drive feedthrough offset and allow the charge injection offsets of the reset switch to settle. The input-referred noise due to the preamplifier is

$$v_{ni1} = (4.9\text{nV}/\sqrt{\text{Hz}}) \left(\frac{1\text{pF} + 1\text{pF}}{100\text{fF}} \right) \sqrt{16} = 392\text{nV}/\sqrt{\text{Hz}}.$$

Neglecting C_{int}, the noise of the integrator op amp sees a gain of $1 + \frac{C_h}{C_f}$ during ϕ_2, and a gain of $1 + \frac{C_s}{C_f}$ during ϕ_1. If $C_h = C_s$, then the gains of the noise during the two phases are the same, and the odd harmonics of the thermal noise are not folded into DC. However, the integrator op amp has an input capacitance, represented by C_{int}. The gain during ϕ_2 is now

$$\alpha_2 = 1 + \frac{C_{int} + C_h}{C_f},$$

and the gain during ϕ_1 is

$$\alpha_1 = \left(1 + \frac{C_{int}}{C_h} \right) \left(1 + \frac{C_s}{C_f} \right) + \frac{C_{int}}{C_f}.$$

Thus, the aliased noise at the output of the sense loop due to the integrator op amp is given by

$$v_{no2} = v_{n2}|_{\omega_m} (\alpha_1 - \alpha_2) \frac{2}{T} \frac{1}{s} \sqrt{2N_2},$$

where $v_{n2}|_{\omega_m}$ is the noise of the integrator op amp at the modulation frequency in

volts/$\sqrt{\text{Hz}}$, and N_2 is the number of odd harmonics of the modulation frequency less than the integrator op amp bandwidth. The input-referred noise due to the integrator amplifier is thus

$$\begin{aligned} v_{ni2} &= \frac{v_{no2}}{G_{sense}} \\ &= v_{n2}|_{\omega_m} \left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)(\alpha_1-\alpha_2)\left(\frac{C_f}{C_s}\right)(\sqrt{2N_2}). \end{aligned}$$

The integrator op amp was designed so that its input capacitance, C_{int}, is 1pF:

$$\begin{aligned} \alpha_1-\alpha_2 &= \left(1+\frac{C_{int}}{C_h}\right)\left(1+\frac{C_s}{C_f}\right)+\frac{C_{int}}{C_f}-\left(1+\frac{C_{int}+C_h}{C_f}\right) \\ &= \left(1+\frac{1\text{pF}}{1\text{pF}}\right)\left(1+\frac{1\text{pF}}{32\text{pF}}\right)+\frac{1\text{pF}}{32\text{pF}}-\left(1+\frac{1\text{pF}+1\text{pF}}{32\text{pF}}\right) \\ &= 1.03. \end{aligned}$$

The op amp input noise at 15kHz was simulated to be 6.3nV/$\sqrt{\text{Hz}}$. Its closed-loop bandwidth is about 690kHz, so $N_2 = 23$:

$$\begin{aligned} v_{ni2} &= (6.3\text{nV}/\sqrt{\text{Hz}})\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)(1.03)\left(\frac{32\text{pF}}{1\text{pF}}\right)(\sqrt{46}) \\ &= 99\text{nV}/\sqrt{\text{Hz}}. \end{aligned}$$

The sense signal is demodulated when it reaches the output buffer. Thus, the noise contribution of the output buffer is simply its low-frequency $1/f$ noise, which causes offset drift. At 1Hz, the noise at the input of the buffer is

$$\sqrt{(45\mu\text{V}/\sqrt{\text{Hz}})^2+(7\mu\text{V}/\sqrt{\text{Hz}})^2} \approx 45\mu\text{V}/\sqrt{\text{Hz}},$$

and the resulting noise at the output is

$$v_{no3} = v_{n3}|_{DC}(\sqrt{2}) \approx (45\mu\text{V}/\sqrt{\text{Hz}})(\sqrt{2}) = 64\mu\text{V}/\sqrt{\text{Hz}}.$$

Although the sense signal shares bandwidth with the $1/f$ noise of the output buffer, the signal has been amplified by previous stages so that the noise magnitude relative to the signal is small. Referred to the input, the noise contribution of the output buffer is

$$\begin{aligned} v_{ni3} &= \frac{v_{no2}}{G_{sense}} \\ &= v_{n3}|_{DC}\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{C_f}{C_s}\frac{T}{2}s\right), \end{aligned}$$

which approaches zero in steady state due to the infinite gain of the integrating demodulator. However, as discussed before, the actual DC gain of the integrator is finite:

$$\begin{aligned} v_{ni3} &= v_{n3}|_{DC}\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{1+A_o^2\frac{C_f}{C_s}\frac{T}{2}s}{A_o^2}\right) \\ &= v_{n3}|_{DC}\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{1}{A_o^2}\right) \\ &= 64\mu\text{V}\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{1}{10^6}\right) \\ &= 6.4\text{pV}/\sqrt{\text{Hz}}. \end{aligned}$$

Because the noise contributions of the three sense loop amplifiers are uncorrelated, the input-referred noise of the sense loop is the rms sum of the input-referred noise of the three amplifiers:

$$v_{ni,ckts} = \sqrt{v_{ni1}^2 + v_{ni2}^2 + v_{ni3}^2}$$

$$= \sqrt{(392\text{nV}/\sqrt{\text{Hz}})^2 + (99\text{nV}/\sqrt{\text{Hz}})^2 + (6.4\text{pV}/\sqrt{\text{Hz}})^2}$$
$$= 404\text{nV}/\sqrt{\text{Hz}}.$$

The rms noise power of the input-referred noise in a 10Hz bandwidth is thus

$$v_{ni,ckts\,(rms)} = (404\text{nV}/\sqrt{\text{Hz}})(\sqrt{10}) = 1.28\mu\text{V}.$$

4.6.2 kT/C Noise

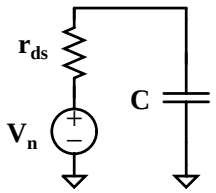

Figure 4-26: Noise of a switch in the on state.

A PMOS switch in the on state has a non-zero channel resistance that has thermal noise, as illustrated in Figure 4-26 [8]. The spectral density of this noise is

$$v_n^2(f) = 4kTr_{ds} \quad (\text{V}^2/\text{Hz}),$$

where k is Boltzmann's constant, T is the absolute temperature, and r_{ds} is the on-resistance of the switch. If the switch is sampling a voltage onto a capacitor, the switch noise is also sampled and held on the sampling capacitor when the switch turns off. Integrating the noise spectral density over the bandwidth of the low-pass filter formed by r_{ds} and C, the rms noise power of the sampled noise is

$$v_{n\,(rms)} = \sqrt{\frac{kT}{C}},$$

which turns out to be independent of the switch resistance. This represents the error between the voltage that was being sampled and the actual voltage held on

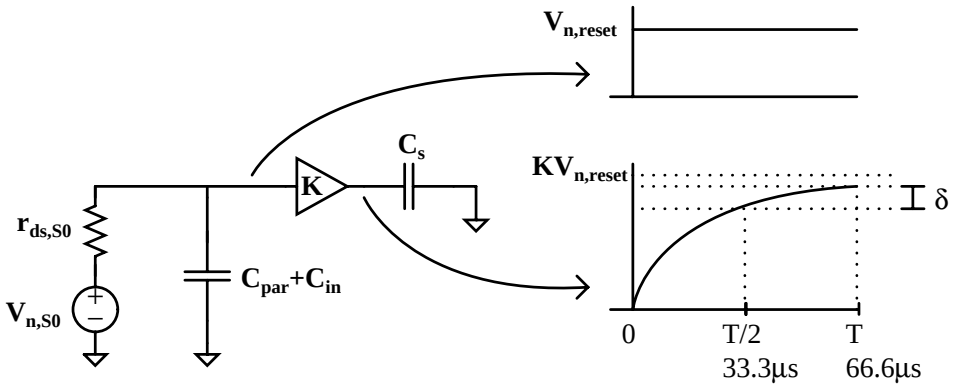

Figure 4-27: Sample noised of the reset switch.

the sampling capacitor due to the switch noise. The kT/C noise of the reset and demodulator switches result in offsets at the output of the sense loop.

Figure 4-27 illustrates the effect of kT/C noise of the reset switch. The noise is sampled onto the capacitance at the input node of the preamplifier:

$$v_{n,S0\,(rms)} = \sqrt{\frac{kT}{C_{par} + C_{in}}} = \sqrt{\frac{(1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}})(300\mathrm{K})}{1\mathrm{pF} + 1\mathrm{pF}}} = 45.5\mu\mathrm{V}.$$

As with the charge injection analysis, the preamplifier amplifies and stores this voltage onto the capacitor C_s. This sampled noise voltage was assumed to appear as a step at the input of the preamplifier to analyze the worst case offset. The offset due to the residual settling of such a step due to the finite bandwidth of the preamplifier is given by

$$\begin{aligned} \delta &= v_{n,S0\,(rms)}\ (K)[(1 - \exp(-2\pi f_{\mathrm{BW}} \cdot T)) - (1 - \exp(-2\pi f_{\mathrm{BW}} \cdot T/2))] \\ &= v_{n,S0\,(rms)}\ (K)(\exp(-2\pi f_{\mathrm{BW}} \cdot T/2) - \exp(-2\pi f_{\mathrm{BW}} \cdot T)), \end{aligned}$$

where f_{BW} is the bandwidth of the preamplifier. Referred to the input, δ is divided by the sense loop gain preceding it. However, although the sense loop is fully differential, the sampled noise of the two reset switches at the differential inputs of the preamplifier are uncorrelated. Thus, instead of suppression due to the matching of the switches,

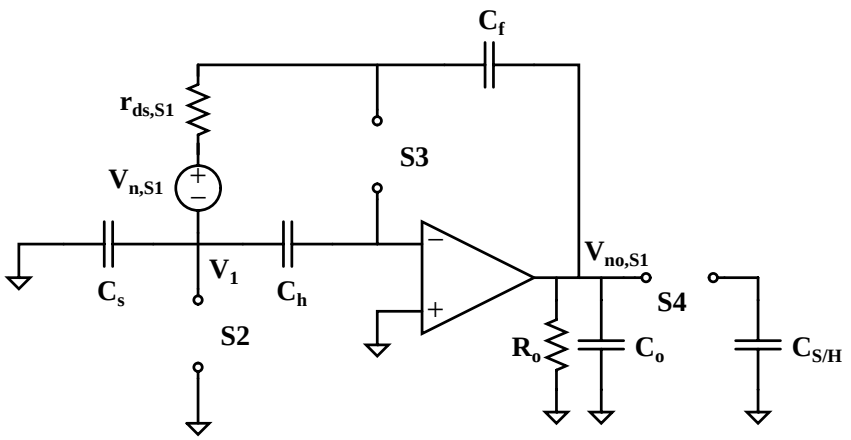

Figure 4-28: Sampled noise of switch S1.

the two uncorrelated noise paths increase the noise by a factor of $\sqrt{2}$:

$$\begin{aligned}
v_{ni,S0\,(rms)} &= \delta\left(\frac{1}{K}\right)\left(\frac{C_{par}+C_{in}}{C_m}\right)(\sqrt{2}) \\
&= v_{n,S0\,(rms)}(\exp(-2\pi f_{\mathrm{BW}}\cdot T/2)-\exp(-2\pi f_{\mathrm{BW}}\cdot T))\left(\frac{C_{par}+C_{in}}{C_m}\right)(\sqrt{2}) \\
&= 45.5\mu\mathrm{V}(\exp(-2\pi\times 250\mathrm{kHz}\times 33.3\mu\mathrm{s}) \\
&\quad -\exp(-2\pi\times 250\mathrm{kHz}\times 66.6\mu\mathrm{s}))\left(\frac{1\mathrm{pF}+1\mathrm{pF}}{100\mathrm{fF}}\right)(\sqrt{2}) \\
&= 2.5\times 10^{-26}\mathrm{V}\approx 0.
\end{aligned}$$

Figure 4-28 illustrates the switch noise during ϕ_1, where R_o and C_o represent the output resistance and capacitance of the demodulator op amp. To determine the sampled noise of switch S1, it is necessary to determine the transfer function seen by the noise to the output, $v_{no,S1}$, which will be defined as $H(s)$. With switch S1 closed, the feedback around the op amp, neglecting its offset, forces the inverting terminal to be virtual ground and prevents the charge in capacitor C_h from changing. Thus, the node v_1 is also at virtual ground, and the switch resistance forms a bandpass filter with C_f, C_o, and R_o. The noise transfer function is

$$\begin{aligned} H(s) &= \frac{R_o||\frac{1}{C_o s}}{R_o||\frac{1}{C_o s} + r_{ds} + \frac{1}{C_f s}} \\ &= \frac{R_o C_f s}{1 + (R_o C_o + R_o C_f + r_{ds} C_f)s + r_{ds} R_o C_f C_o s^2}. \end{aligned}$$

Assuming $R_o \gg r_{ds}$ and $C_f \gg C_o$, the transfer function $H(s)$ has two widely spaced poles with time constants $R_o(C_f + C_o)$ and $r_{ds}\frac{C_f C_o}{C_f + C_o}$. Thus the noise transfer function may be approximated as

$$\begin{aligned} H(s) &\approx \frac{R_o C_f s}{(1 + R_o(C_f + C_o)s)(1 + r_{ds}\frac{C_f C_o}{C_f + C_o} s)} \\ &= \frac{R_o C_f s}{1 + (R_o C_o + R_o C_f + r_{ds}\frac{C_f C_o}{C_f + C_o})s + r_{ds} R_o C_f C_o s^2}, \end{aligned}$$

which approaches the exact noise transfer function if $C_f \gg C_o$, as assumed. To find the rms sampled noise voltage at the output of the demodulator integrator, the noise spectral density $v_{n,S1}$ filtered by the noise transfer function should be integrated over frequency:

$$v^2_{no,S1\,(rms)} = \int_0^\infty v^2_{n,S1}\,|H(j\omega)|^2\,d\omega.$$

However, only the noise in the bandwidth of the sense signal is of interest, and this analysis assumes that all of the thermal noise in the noise bandwidth appears at the output. Due to the phasing of the switches, the odd harmonics of the switching frequency inside the bandpass of the noise transfer function are mapped to DC and integrated with the sense signal, but the even harmonics are not, in a manner similar to the aliasing of the preamplifier and demodulator op amp noise. The on-resistance of the switch is

$$r_{ds} = \frac{1}{\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{Tp})} = \frac{1}{(14\mu\text{A/V}^2)\frac{17.6\mu\text{m}}{4\mu\text{m}}(1.5\text{V} - 0.8\text{V})} \approx 20\text{k}\Omega.$$

Thus the spectral density of the thermal noise is

$$v_{n,S1} = \sqrt{4kTr_{ds}} = \sqrt{4(1.38 \times 10^{-23}\,\mathrm{J\,K^{-1}})(300\mathrm{K})(20\mathrm{k}\Omega)} = 18\mathrm{nV}/\sqrt{\mathrm{Hz}},$$

The output resistance R_o of the op amp is about 4.9MΩ, and the output capacitance C_o is 10pF. Thus, the two poles of the noise transfer function are at $1/(2\pi R_o(C_f + C_o)) = 520\mathrm{Hz}$ and $1/(2\pi r_{ds}\frac{C_f C_o}{C_f+C_o}) = 900\mathrm{kHz}$, and there are $N_{S1} = 30$ odd harmonics of 15kHz inside this bandpass bandwidth. However, the bandwidth of the op amp is 690kHz, which bandlimits the amount of noise aliasing to $N_{S1} = 23$. Thus, the noise at the output in the sense signal bandwidth is given by

$$v_{no,S1} = v_{n,S1}\left(\frac{2}{Ts}\right)(\sqrt{N_{S1}})(\sqrt{2}),$$

The input-referred noise is

$$\begin{aligned} v_{ni,S1} &= \frac{v_{no,S1}}{G_{sense}} \\ &= v_{n,S1}\left(\frac{2}{Ts}\right)\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{C_f}{C_s}\right)\left(\frac{Ts}{2}\right)(\sqrt{N_{S1}})(\sqrt{2}) \\ &= 18\mathrm{nV}/\sqrt{\mathrm{Hz}}\left(\frac{1\mathrm{pF}+1\mathrm{pF}}{100\mathrm{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{32\mathrm{pF}}{1\mathrm{pF}}\right)(\sqrt{23})(\sqrt{2}) \\ &= 390\mathrm{nV}/\sqrt{\mathrm{Hz}}, \end{aligned}$$

and in a 10Hz bandwidth, the rms noise power is

$$v_{ni,S1\,(rms)} = (v_{ni,S1})(\sqrt{10\mathrm{Hz}}) = (390\mathrm{nV}/\sqrt{\mathrm{Hz}})(\sqrt{10\mathrm{Hz}}) = 1.2\mu\mathrm{V}.$$

Figure 4-29 illustrates the switch noise during ϕ_2 due to switch S2. Once again, it can be assumed that the op amp forces its inverting terminal to be virtual ground, and the switch noise sees the capacitance $C_s + C_h$ in series with its on-resistance. The noise of this switch sees a gain of C_h/C_f, and the odd harmonics of the switching frequency inside the noise bandwidth are unwrapped during ϕ_2, and accumulated

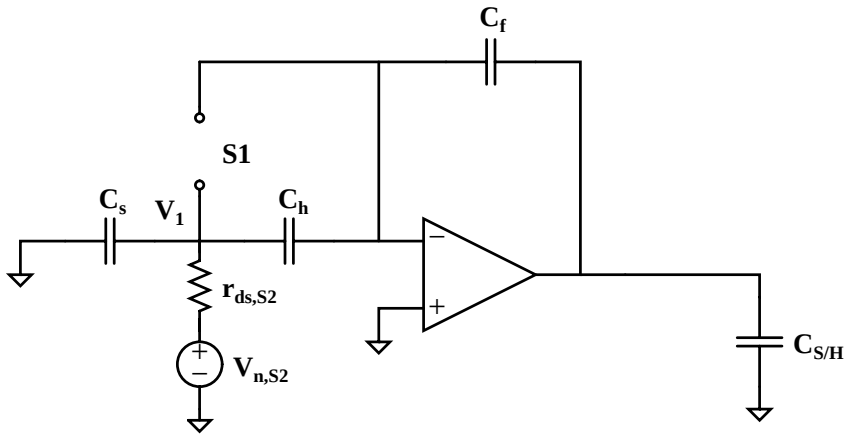

Figure 4-29: Sampled noise of switch S2.

during ϕ_1. Thus, these harmonics are demodulated and integrated, and contribute noise in the bandwidth of the sense signal. Switch S2 has the same gate drive and dimensions as switch S1, thus their on-resistance and thermal noise spectral density are the same. The noise bandwidth is

$$\frac{1}{2\pi}\frac{1}{r_{ds}(C_s+C_h)} = \frac{1}{(2\pi)(20\text{k}\Omega)(1\text{pF}+1\text{pF})} = 4\text{MHz},$$

and there are $N_{S2} = 132$ odd harmonics of 15kHz inside this bandwidth. However, once again the op amp bandwidth of 690kHz bandlimits the frequency response instead, and $N_{S2} = 23$. The noise at the output is

$$v_{no,S2} = v_{n,S2}\left(\frac{C_h}{C_f}\right)\left(\frac{2}{Ts}\right)(\sqrt{N_{S2}})(\sqrt{2}).$$

The input-referred noise is

$$\begin{aligned} v_{ni,S2} &= \frac{v_{no,S2}}{G_{sense}} \\ &= v_{n,S2}\left(\frac{C_h}{C_f}\right)\left(\frac{2}{Ts}\right)\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{C_f}{C_s}\right)\left(\frac{Ts}{2}\right)(\sqrt{N_{S1}})(\sqrt{2}) \end{aligned}$$

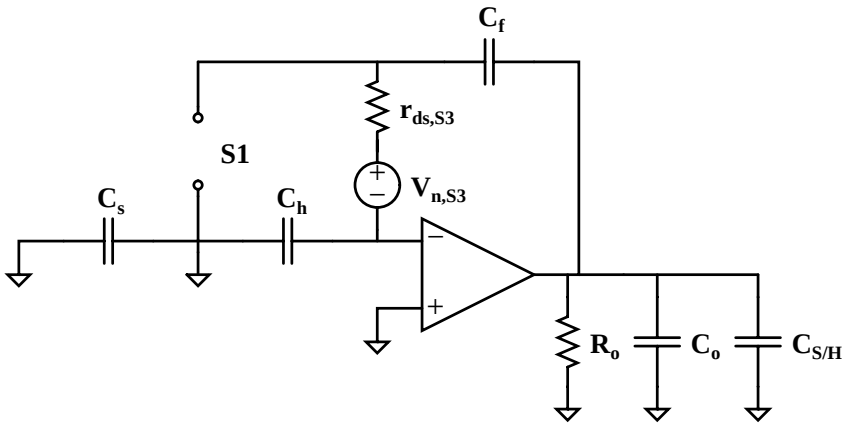

Figure 4-30: Sampled noise of switch S3.

$$
\begin{aligned}
&= 18\text{nV}/\sqrt{\text{Hz}}\left(\frac{1\text{pF}}{32\text{pF}}\right)\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{32\text{pF}}{1\text{pF}}\right)(\sqrt{23})(\sqrt{2}) \\
&= 12.2\text{nV}/\sqrt{\text{Hz}},
\end{aligned}
$$

and in a 10Hz bandwidth, the rms noise power is

$$v_{ni,S2\,(rms)} = (v_{ni,S2})(\sqrt{10\text{Hz}}) = (8.4\text{nV}/\sqrt{\text{Hz}})(\sqrt{10\text{Hz}}) = 26.7\text{nV}.$$

In addition, the switch noise is sampled onto the node v_1. This creates an offset at the signal summing junction during ϕ_1, which DC shifts the output without changing the charge stored on C_f. During ϕ_2, node v_1 is reset again, and the output DC shifts back when switch S3 closes, neglecting time-variation in the op amp offset. The output is sampled onto capacitor $C_{S/H}$ during ϕ_2, so a DC offset at node v_1 during ϕ_1 does not affect the sampled output of the demodulator.

Figure 4-30 illustrates the switch noise during ϕ_2 due to switch S3. Similar to the analysis of the noise of switch S1, the op amp forces its inverting terminal to be virtual ground, and the noise transfer function is determined by the channel resistance of S3, the feedback capacitor C_f, and the output impedance of the op amp, $R_o||\frac{1}{C_o s}$. The odd harmonics of the noise less inside this bandpass filter are aliased into the sense signal bandwidth. Switch S3 has the same gate drive and dimensions as switch S1, and its switch noise sees the same capacitance, so their on-resistance, thermal noise

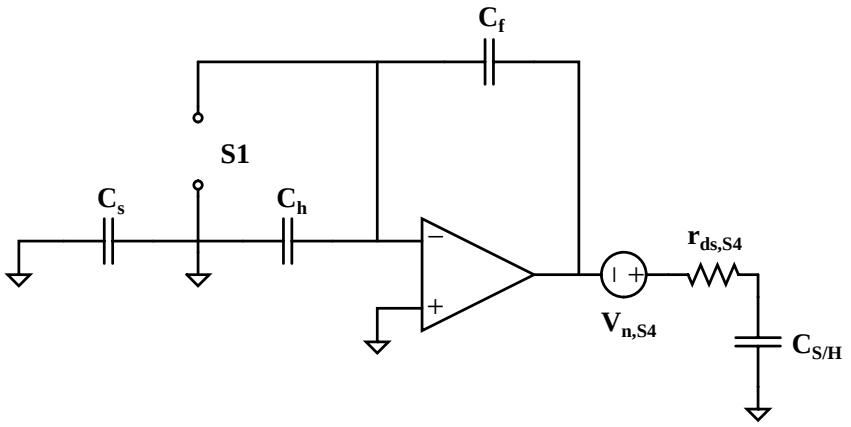

Figure 4-31: Sampled noise of switch S4.

spectral density, and noise bandwidth are the same. Therefore,

$$v_{ni,S3} = v_{ni,S1} = 390\text{nV}/\sqrt{\text{Hz}},$$

and in a 10Hz bandwidth, the rms noise power is

$$v_{ni,S3\,(rms)} = v_{ni,S1\,(rms)} = 1.2\mu\text{V}.$$

Figure 4-31 illustrates the switch noise during ϕ_2 due to switch S4. The feedback around the demodulator op amp forces its output to be constant in the absence of time-varying signals at its input. Thus, the switch noise is sampled onto capacitor $C_{S/H}$, and the noise at the output is

$$v_{no,S4\,(rms)} = v_{n,S4\,(rms)} = \sqrt{\frac{kT}{C_{S/H}}} = \sqrt{\frac{(1.38\times10^{-23}\,\text{J K}^{-1})(300\text{K})}{10\text{pF}}} = 20.3\mu\text{V}.$$

Because this noise represents an offset error between the voltage being sampled and the actual sampled voltage and is resampled onto $C_{S/H}$ each cycle, the input-referred noise is divided by the DC gain of the demodulating integrator, and the noise is

$$\begin{aligned} v_{ni,S4\,(rms)} &= \frac{v_{no,S4\,(rms)}}{G_{sense}} \\ &= v_{n,S4\,(rms)} \left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{1}{A_o^2}\right)\sqrt{2} \\ &= 20.3\mu\text{V}\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{1}{10^6}\right)\sqrt{2} \\ &= 2.9\text{pV}/\sqrt{\text{Hz}}. \end{aligned}$$

In a 10Hz bandwidth, the rms noise power is

$$v_{ni,S4\,(rms)} = (v_{ni,S4})(\sqrt{10\text{Hz}}) = (2.9\text{pV}/\sqrt{\text{Hz}})(\sqrt{10\text{Hz}}) = 9.2\text{pV}.$$

The total noise power due to the noise of the switches is the rms sum:

$$\begin{aligned} v_{ni,sw\,(rms)} &= \sqrt{v_{ni,S0\,(rms)}^2 + v_{ni,S1\,(rms)}^2 + v_{ni,S2\,(rms)}^2 + v_{ni,S3\,(rms)}^2 + v_{ni,S4\,(rms)}^2} \\ &= \sqrt{0^2 + (1.2\mu\text{V})^2 + (38.2\text{nV})^2 + (1.2\mu\text{V})^2 + (2.9\text{pV})^2} \\ &= 1.69\mu\text{V}. \end{aligned}$$

The noise due to the amplifiers and the noise due to the switches are also uncorrelated, so the total input-referred noise of the sense loop, and thereby the MEMS-based amplifier, is

$$v_{ni\,(rms)} = \sqrt{v_{ni,ckts\,(rms)}^2 + v_{ni,sw\,(rms)}^2} = \sqrt{(1.28\mu\text{V})^2 + (1.69\mu\text{V})^2} = 2.1\mu\text{V}.$$

4.7 Offset Analysis

4.7.1 Feedthrough

As discussed earlier, the drive voltages used to apply electrostatic forces on the MEMS transducer can feed into the sense loop through stray capacitances, as illustrated in

Figure 4-8. The peak-to-peak amplitude of the drive voltages is 10V, and assuming a stray capacitance of 1fF, the amplitude of the feedthrough signal at the input of the sense loop is

$$\begin{aligned} v_{feed} &= V_{drive}\left(\frac{C_{stray}}{C_{stray}+C_{par}+C_{in}}\right) \\ &\approx V_{drive}\left(\frac{C_{stray}}{C_{par}+C_{in}}\right) \\ &= 10\text{V}\left(\frac{1\text{fF}}{1\text{fF}+1\text{pF}+1\text{pF}}\right) \quad (\text{peak}-\text{to}-\text{peak}) \\ &= 5\text{mV} \quad (\text{peak}-\text{to}-\text{peak}) \\ &= \pm 2.5\text{mV}. \end{aligned}$$

If the drive loop is ideally operating at the mechanical resonance of the MEMS transducer, v_{feed} is in phase with the beam velocity. The AC sense current signal from the MEMS transducer is also in phase with the beam velocity, but is integrated by the capacitance at the input node of the sense loop. Thus, the sense signal at the output of the preamplifier is in phase with the beam displacement. Because the sense and feedthrough signals are in quadrature, the feedthrough signal is ideally rejected as the sense signal is demodulated.

Two factors prevent perfect quadrature suppression. The preamplifier bandwidth and on-resistance of the demodulator switch during ϕ_1 introduces phase shift to both the sense and feedthrough signals, which results in a loss in the sense signal gain at the demodulator, and causes a portion of the feedthrough to be demodulated into a DC voltage. In addition, the drive loop does not operate exactly at resonance, and there is a phase shift φ between the MEMS transducer drive voltage and beam velocity. The feedthrough signal is in phase with the drive voltage, which also clocks the demodulator, so the feedthrough offset is unchanged. However, the drive loop phase error φ results in additional loss in gain for the demodulated sense signal, which effectively increases the input-referred offset.

The feedthrough signal sees a similar loop transfer function as the sense signal.

The gain of the preamplifier is the same, since the sense and feedthrough signals are at the same frequency, although the phase shifts θ of the preamplifier and γ of the on-resistance of the demodulator switches act to increase the gain of the feedthrough signal at the demodulator, instead of decreasing it. The feedthrough signal is then demodulated and integrated in the same manner as the sense signal. The magnitude of the feedthrough signal gain is thus

$$G_{feed} = (K \sin(\theta + \gamma)) \left(\frac{C_s}{C_f} \frac{2}{T} \frac{1}{s} \right).$$

With careful layout, it can also be assumed that the feedthrough signal enters symmetrically into the differential signal chain of the sense loop. The common-mode rejection of the differential output of the sense loop is assumed to provide additional suppression by a factor of 100 [5]. Referred to the input, the total input-referred feedthrough offset is estimated to be

$$\begin{aligned} v_{os,feed} &= v_{feed} \left(\frac{G_{feed}}{G_{sense}} \right) \left(\frac{1}{100} \right) \\ &= v_{feed} \left(\frac{C_{par} + C_{in}}{C_m} \right) \left(\frac{\sin(\theta + \gamma)}{\cos(\varphi + \theta + \gamma)} \right) \left(\frac{1}{100} \right) \\ &= (2.5\text{mV}) \left(\frac{1\text{pF} + 1\text{pF}}{100\text{fF}} \right) \left(\frac{\sin(-3.4^\circ + 3.45^\circ)}{\cos(4.3^\circ - 3.4^\circ + 3.45^\circ)} \right) \left(\frac{1}{100} \right) \\ &= 0.44\mu\text{V}. \end{aligned}$$

4.7.2 Charge Injection

As a rough first-order estimation of the effects of charge injection, the following analysis assumed that the channel charge splits evenly between the drain and the source of the switch. Because the gate-to-source and gate-to-drain capacitances were on the order of 0.1fF, the offset due to the gate drive feedthrough via the overlap capacitances were much smaller than the charge injection offsets, and thus the gate drive feedthrough was ignored.

Figure 4-32 illustrates the effect of charge injection due to the reset switch. The

reset switch, S0, opens during ϕ_2. It is minimum-sized to minimize its channel charge, and has a 5±5V gate drive:

$$Q_{CH0} = WLC_{ox}(V_{switch} - V_{Tp}) = (5\mu\text{m})(4\mu\text{m})(710\mu\text{F/m}^2)(5\text{V} - 0.8\text{V}) = 60\text{fC}.$$

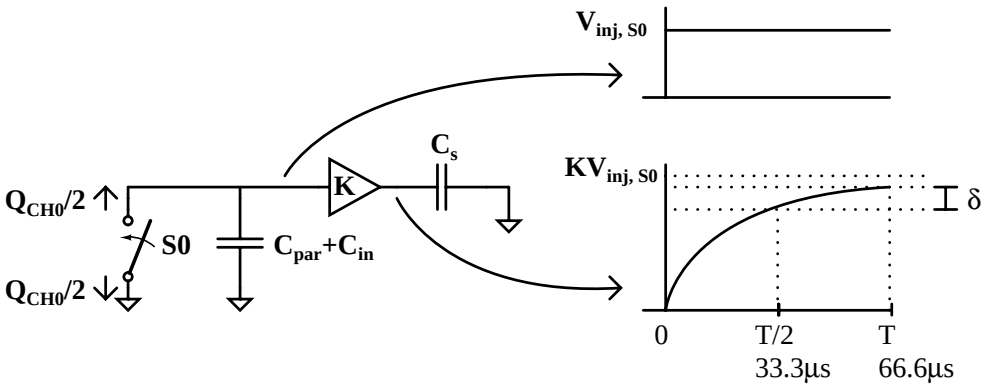

Figure 4-32: Charge injection of reset switch.

Half of this charge is transferred to the capacitance at the input node of the preamplifier when S0 opens:

$$V_{inj,S0} = \frac{Q_{CH0}}{2}\left(\frac{1}{C_{par} + C_{in}}\right) = \frac{60\text{fC}}{2}\left(\frac{1}{1\text{pF} + 1\text{pF}}\right) = 15.0\text{mV}.$$

The preamplifier sees a step increase of 15mV at its input when the reset switch opens, which is amplified and stored onto the capacitor C_s. If this change in voltage due to the charge injection of the reset switch settles completely during ϕ_2, then the sense loop signal is unaffected by it during ϕ_1. However, the finite bandwidth of the preamplifier results in a settling time constant (the preamplifier has a very low output resistance, so the time constant associated with C_s is negligible), and the residual settling of $V_{inj,S0}$ onto C_s during ϕ_1, represented by δ, results in an offset:

$$\begin{aligned}\delta &= V_{inj,S0}\ (K)[(1-\exp(-2\pi f_{\mathrm{BW}}\cdot T))-(1-\exp(-2\pi f_{\mathrm{BW}}\cdot T/2))] \\ &= V_{inj,S0}\ (K)(\exp(-2\pi f_{\mathrm{BW}}\cdot T/2)-\exp(-2\pi f_{\mathrm{BW}}\cdot T))\end{aligned}$$

To find the input-referred offset, δ is divided by the sense loop gain preceding it. Furthermore, the sense loop is fully differential, and systematic offsets due to charge injection are correlated. The two reset switches at the differential inputs of the preamplifier are assumed to match to 1% from an analysis of process matching [5], and thus the differential output provides an extra factor of 100 in offset suppression:

$$\begin{aligned}V_{os,S0} &= \delta\left(\frac{1}{K}\right)\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{100}\right) \\ &= V_{inj,S0}(\exp(-2\pi f_{\mathrm{BW}}\cdot T/2)-\exp(-2\pi f_{\mathrm{BW}}\cdot T))\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{100}\right)\end{aligned}$$

The bandwidth of the preamplifier is 250kHz, and ϕ_2 and ϕ_1 are both $\mathrm{T}/2 = 1/30\mathrm{kHz} \approx 33.3\mu\mathrm{s}$ long, so

$$\begin{aligned}V_{os,S0} &= 15\mathrm{mV}(\exp(-2\pi\times 250\mathrm{kHz}\times 33.3\mu\mathrm{s}) \\ &\quad -\exp(-2\pi\times 250\mathrm{kHz}\times 66.6\mu\mathrm{s}))\left(\frac{1\mathrm{pF}+1\mathrm{pF}}{100\mathrm{fF}}\right)\left(\frac{1}{100}\right) \\ &= 6\times 10^{-26}\mathrm{V}\approx 0.\end{aligned}$$

Figure 4-33 illustrates the charge injection due to the switch S1 turning off during ϕ_1. Because the ϕ_1 and ϕ_2 clocks are non-overlapping, the other switches in the demodulator are still off when S1 opens. Switch S1 is not minimum-sized to reduce its on-resistance, which increases its channel charge. In addition, because both terminals of the switch are close to virtual ground, the gate drive of this switch can be reduced to 5±1.5V. The channel charge for S1 is given by

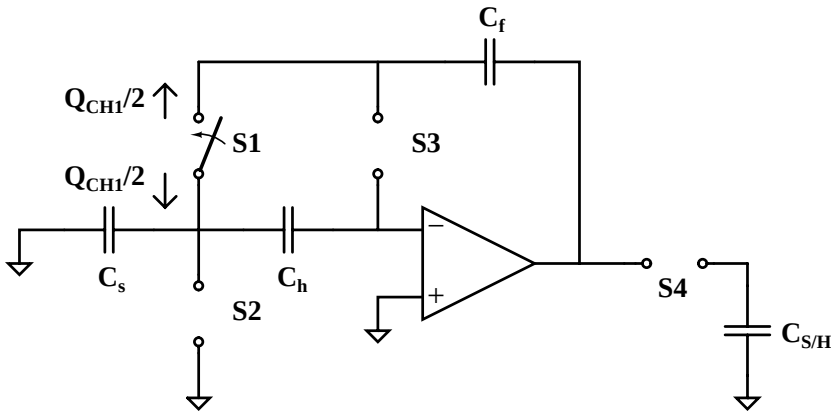

Figure 4-33: Charge injection of switch S1.

$$Q_{CH1} = WLC_{ox}V_{switch} = (17.6\mu\text{m})(4\mu\text{m})(710\mu\text{F/m}^2)(1.5\text{V} - 0.8\text{V}) = 35\text{fC}.$$

Half of its channel charge falls on C_s, which creates an offset at the virtual summing junction of the integrating demodulator. However, in the following phase ϕ_2, switch S2 immediately resets this node back to virtual ground, so this portion of the charge injection does not cause an offset in the sense loop. The other half of its channel charge accumulates on C_f. This occurs each cycle, so the average value of the offset is essentially integrated with the demodulated sense signal:

$$\begin{aligned} V_{inj,S1} &= \frac{Q_{CH1}}{2}\left(\frac{1}{C_f}\right)\left(\frac{1}{T}\frac{1}{s}\right) = \frac{35\text{fC}}{2}\left(\frac{1}{32\text{pF}}\right)\left(\frac{1}{T}\frac{1}{s}\right) \\ &= 0.55\text{mV}\left(\frac{1}{T}\frac{1}{s}\right). \end{aligned}$$

Dividing this by the sense loop gain refers the offset to the input, and once again assuming 1% matching of the switches in the differential signal chain:

$$V_{os,S1} = \frac{V_{inj,S1}}{G_{sense}} = \frac{Q_{CH1}}{2}\frac{1}{C_f}\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{C_f}{C_s}\right)\left(\frac{1}{2}\right)\left(\frac{1}{100}\right)$$

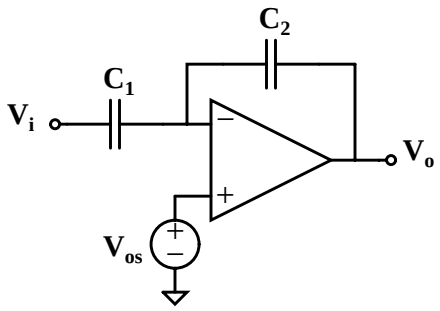

Figure 4-34: Effect of offset voltage at the summing junction of a capacitive gain circuit.

$$\begin{aligned} &= 0.55\text{mV}\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{32\text{pF}}{1\text{pF}}\right)\left(\frac{1}{2}\right)\left(\frac{1}{100}\right) \\ &= 8.8\mu\text{V}. \end{aligned}$$

Before the charge injection offsets of switches S2 and S3 are calculated, it is instructive to examine the effect of an offset voltage at the summing junction for a capacitive gain circuit, illustrated in Figure 4-34. The output voltage for such a gain configuration is given by

$$\frac{dv_o}{dt} = -\frac{C_1}{C_2}\frac{dv_{in}}{dt} + \left(1+\frac{C_1}{C_2}\right)\frac{dv_{os}}{dt}.$$

Thus, the offset voltage of the op amp only sees a voltage gain if it is time-varying. A DC offset voltage at the summing junction does not change the charge on the feedback capacitor C_2. The offset only shifts the output by its DC value, without seeing a voltage gain. This architecture is an auto-zero, so this makes sense.

Figure 4-35 illustrates the charge injection due to switches S2 and S3 turning off during ϕ_2. The demodulator output sample-and-hold switch turns off slightly before S2 and S3 turn off, and due to non-overlapping clocks, switch S1 is still open. Switches S2 and S3 are also not minimum-sized to reduce their on-resistance, and also can have reduced gate drives because both switch terminals are close to virtual ground. Thus, both switches have the same channel charge as S1:

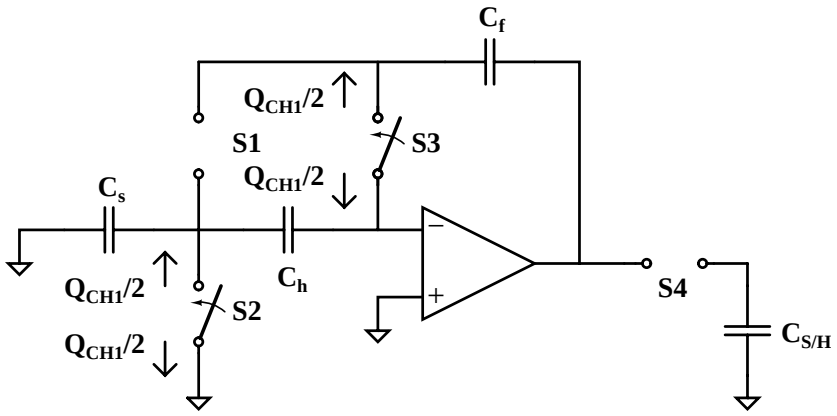

Figure 4-35: Charge injection of switches S2 and S3.

$$Q_{CH1} = Q_{CH2} = Q_{CH3} = 35\text{fC}.$$

Half of the channel charge of S2 settles onto C_s, resulting in an offset at the effective summing junction of the demodulating integrator:

$$V_{inj,S2} = \frac{Q_{CH2}}{2}\left(\frac{1}{C_s}\right) = \frac{35\text{fC}}{2}\left(\frac{1}{1\text{pF}}\right) = 17.5\text{mV}.$$

When switch S1 closes for the following phase ϕ_1, the output of the demodulating integrator is DC shifted by this offset voltage. However, this node is reset to virtual ground again when switch S1 opens and S2 closes again for ϕ_2. Also during ϕ_2, S3 closes, and the output of the demodulating integrator is shifted back to its previous value, neglecting time-variations in the op amp offset. Because the output of the demodulator is sampled onto capacitor $C_{S/H}$ during ϕ_2, the offset during ϕ_1 due to this charge injection does not affect the sampled demodulator output. Similarly, half of the channel charge of S3 also results in an offset at the CDS summing junction, but the sampled demodulator output is unaffected.

The other half of the channel charge of S3 is accumulated onto C_f each cycle, and the resulting offset is integrated with the demodulated sense signal in a manner similar to the charge injection of S1:

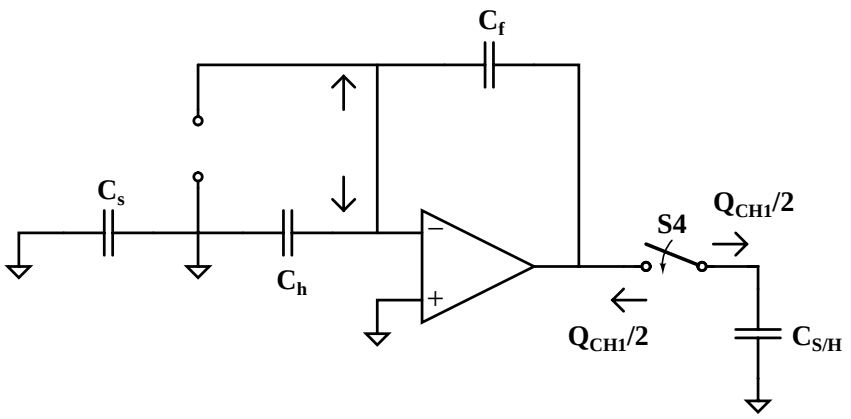

Figure 4-36: Charge injection of switch S4.

$$V_{inj,S3} = \frac{Q_{CH3}}{2}\left(\frac{1}{C_f}\right)\left(\frac{1}{T}\frac{1}{s}\right) = \frac{35\text{fC}}{2}\left(\frac{1}{32\text{pF}}\right)\left(\frac{1}{T}\frac{1}{s}\right) = 0.55\text{mV}\left(\frac{1}{T}\frac{1}{s}\right),$$

and the input-referred offset is

$$\begin{aligned} V_{os,S3} &= \frac{V_{inj,S3,b}}{G_{sense}} = \frac{Q_{CH3}}{2}\left(\frac{1}{C_f}\right)\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{C_f}{C_s}\right)\left(\frac{1}{2}\right)\left(\frac{1}{100}\right) \\ &= 0.55\text{mV}\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{32\text{pF}}{1\text{pF}}\right)\left(\frac{1}{2}\right)\left(\frac{1}{100}\right) \\ &= 8.8\mu\text{V}. \end{aligned}$$

Figure 4-36 illustrates the charge injection due to switch S4, which turns off during ϕ_2 just before switches S2 and S3 turn off. The on-resistance of this switch is less critical, so it is minimum-sized. The voltages at the switch terminals can potentially span 0 to 10V, so the switch gate drive must be full-scale. The resulting channel charge of S4 is

$$Q_{CH4} = WLC_{ox}V_{switch} = (5\mu\text{m})(4\mu\text{m})(710\mu\text{F/m}^2)(5\text{V} - 0.8\text{V}) = 60\text{fC}.$$

The half of this channel charge which is directed towards the output of the demodu-

lating integrator is absorbed by the op amp and does not settle on C_f. The other half of the channel charge settles onto $C_{S/H}$, but the voltage on this capacitor is resampled every cycle. Thus, the charge injection offset is not accumulated with the signal, and when referred to the input, is divided by the DC gain of the demodulating integrator. The change in the output voltage due to this charge injection is

$$V_{inj,S4} = \frac{Q_{CH4}}{2}\left(\frac{1}{C_{S/H}}\right) = \frac{60\text{fC}}{2}\left(\frac{1}{10\text{pF}}\right) = 3.0\text{mV},$$

and the corresponding input-referred offset is

$$\begin{aligned} V_{os,S4} &= \frac{V_{inj,S4}}{G_{sense}} \\ &= V_{inj,S4}\left(\frac{C_{par}+C_{in}}{C_m}\right)\left(\frac{1}{K}\right)\left(\frac{1}{A_o^2}\right)\left(\frac{1}{100}\right) \\ &= 3.0\text{mV}\left(\frac{1\text{pF}+1\text{pF}}{100\text{fF}}\right)\left(\frac{1}{200}\right)\left(\frac{1}{10^6}\right)\left(\frac{1}{100}\right) \\ &= 3\text{pV}. \end{aligned}$$

The total offset due to charge injection is the sum total of each of the charge injection offsets and the drive feedthrough offset:

$$\begin{aligned} v_{os,qinj} &= V_{os,S0} + V_{os,S1} + V_{os,S2} + V_{os,S3} + V_{os,S4} \\ &= 0 + 8.8\mu\text{V} + 8.8\mu\text{V} + 3\text{pV} \\ &= 17.6\mu\text{V}. \end{aligned}$$

The total offset of the sense loop is the sum of the charge injection offset and the drive feedthrough offset:

$$v_{os} = v_{os,feed} + v_{os,qinj} = 0.44\mu\text{V} + 17.6\mu\text{V} = 18.0\mu\text{V}.$$

4.8 Common-Mode Rejection Ratio

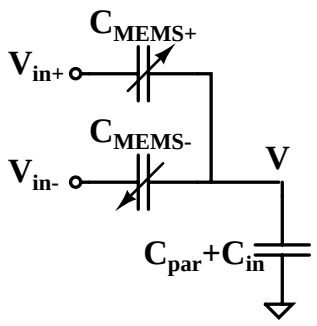

Figure 4-37: Up-modulation of the input voltages by the MEMS transducer.

Figure 4-37 illustrates the capacitive divider seen by the input voltages of the MEMS transducer. It was seen in Chapter 2 that the AC sense current from the moving beam is proportional to the difference between the two input voltages. However, this assumed that the magnitude of the modulating capacitances were equal, but these capacitances only match to 0.1%. Let

$$\begin{aligned} C_{\text{MEMS}+} &= C_o + C_{m+}\sin(\omega_m t), \\ C_{\text{MEMS}-} &= C_o - C_{m-}\sin(\omega_m t), \\ v_{in+} &= v_{cm} + \frac{1}{2}v_{id}, \\ v_{in-} &= v_{cm} - \frac{1}{2}v_{id}. \end{aligned}$$

The voltage at the input of the preamplifier is given by

$$\begin{aligned} v &= \frac{v_{in+}C_{\text{MEMS}+} + v_{in-}C_{\text{MEMS}-}}{C_{\text{MEMS}+} + C_{\text{MEMS}-} + C_{par} + C_{in}} \\ &= \frac{v_{in+}(C_o + C_{m+}\sin(\omega_m t)) + v_{in-}(C_o - C_{m-}\sin(\omega_m t))}{2C_o + (C_{m+} - C + m-) + C_{par} + C_{in}} \\ &\approx \frac{v_{in+}(C_o + C_{m+}\sin(\omega_m t)) + v_{in-}(C_o - C_{m-}\sin(\omega_m t))}{C_{par} + C_{in}} \end{aligned}$$

$$
\begin{aligned}
&= (v_{in+} + v_{in-}) \left(\frac{C_o}{C_{par} + C_{in}} \right) + \left(\frac{v_{in+} C_{m+} - v_{in-} C_{m-}}{C_{par} + C_{in}} \right) \sin(\omega_m t) \\
&= (2v_{cm}) \left(\frac{C_o}{C_{par} + C_{in}} \right) + \left(\frac{v_{cm}(C_{m+} - C_{m-}) + \frac{1}{2} v_{id}(C_{m+} + C_{m-})}{C_{par} + C_{in}} \right) \sin(\omega_m t),
\end{aligned}
$$

where it is assumed that $2C_o + C_{m+} - C_{m-} \ll C_{par} + C_{in}$. If the modulating capacitances are perfectly matched, then only the differential component of the input voltages is up-modulated, and the common-mode component remains at DC and is rejected by the CDS demodulator. However, a mismatch in the magnitude of the modulating capacitances causes a fraction of the common-mode component to also be up-modulated . This common-mode component is amplified, demodulated, and integrated with the differential component, and the ratio of the gain of the differential component to the gain of the common-mode component is given by

$$
\frac{a_{vd}}{a_{cm}} = \frac{C_{m+} + C_{m-}}{C_{m+} - C_{m-}}.
$$

Thus, the common-mode rejection ratio of the system is limited by the matching of the MEMS capacitances, which is about 60dB.

To improve the CMRR of the system, a bootstrapping trick is shown in Figure 4-38, which takes advantage of the global feedback of the sense loop. The input node of the preamplifier is biased with the output of the sense loop, instead of a constant voltage reference. Feedback forces $v_{in+} \approx v_{in-}$, so the common-mode voltage across the MEMS capacitors is greatly reduced. Correspondingly, the up-modulated common-mode component is also reduced, and the CMRR of the system is increased. The trade-off is that the input common-mode range is now equal to the input common-mode range of the preamplifier, instead of the dielectric breakdown voltage of the isolation trenches, which is an order of magnitude much larger.

4.9 Simulation Results

Figure 4-39 shows the simulated waveforms of the MEMS-based amplifier system in unity gain feedback for an input voltage step. The variables v_a, $v(i_{sense})$, v_{preamp},

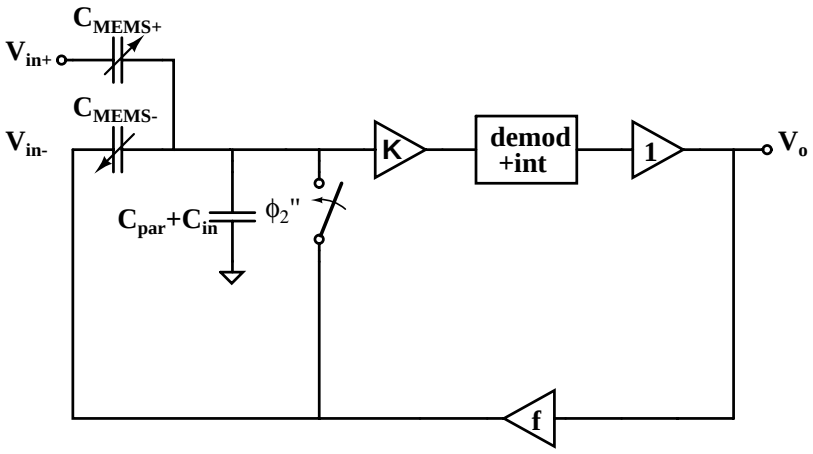

Figure 4-38: Bootstrapping the common-mode voltage across the MEMS transducer.

v_{intamp}, v_{demod}, and v_b represent, respectively, the system input voltage, the input voltage of the preamplifier, the output of the preamplifier, the output of the demodulator before the sample-and-hold capacitor, the sampled output of the demodulator, and the output. It should be noted that a 1% mismatch was added to the widths of the demodulator switches to simulate the charge injection offset. With perfectly matched switches, the system offset was simulated to be only 5μV. The differential output of the comparator was also coupled into the inputs of the preamplifier with a 1fF capacitance to simulated the drive feedthrough. The summing of the sense signal and quadrature error is why the preamplifier input voltage waveform is not sinusoidal.

The input of the preamplifier is periodically reset to a bias voltage of 5V, and the $v(i_{sense})$ waveform indicates a charge injection of 8mV, only half of what was predicted in the calculations above. The discrete output v_b has a rise time of roughly 230μs, which is consistent with a 1.5kHz bandwidth system. At the beginning of the step response, the output of the preamplifier saturates, due to the large error signal. The output swing of the preamplifier is effectively a slew-rate limiter.

Figure 4-40 shows the sense loop waveforms in steady state. It should be noted that as a sampled-data system, the output has a voltage ripple at the clock frequency of 15kHz which should be either low-pass filtered or sampled with an analog-to-digital converter with a correlated system clock. The average value of the output indicates

a system offset of 20μV, which is within 10% of the hand-calculated value. ADICE is not capable of simulating the noise folding of switched-capacitor circuits, so although the noise of the individual circuit blocks were simulated, the noise of the overall system including aliasing could only be calculated based on the simulated noise of each of the circuits.

Figure 4-41 shows the simulated step response of the MEMS-based amplifier system in unity gain feedback with common-mode bootstrapping. All the waveforms remain similar, except the $v(i_{sense})$ waveform, which increases with the output voltage. In steady state, when the output v_b is equal to the input v_a, there is very little common-mode voltage across the modulating capacitance. Thus, the amount of common-mode up-modulation is expected to be much less, and the common-mode rejection of the system is effectively increased. The output once again has a rise time of roughly 230μs, and a system offset of 19μV.

4.10 Summary

The sense loop picks-off the AC sense current from the MEMS beam, amplifies it, and demodulates it back to DC, while adding as little noise into the sense signal bandwidth as possible. Global feedback around the sense loop buys robustness in gain to the significant variations in the absolute magnitudes of the modulating capacitances, and an integrator in the sense loop allows zero steady-state error for an input voltage step. The input-referred noise was calculated to be 2.12μV (rms), based on the noise simulation of the individual amplifiers, but a system noise simulation was not possible. The simulated step response was consistent with a 1.5kHz bandwidth system, and the simulated input-referred offset was 20μV, which agreed well with the calculated offset of 18μV.

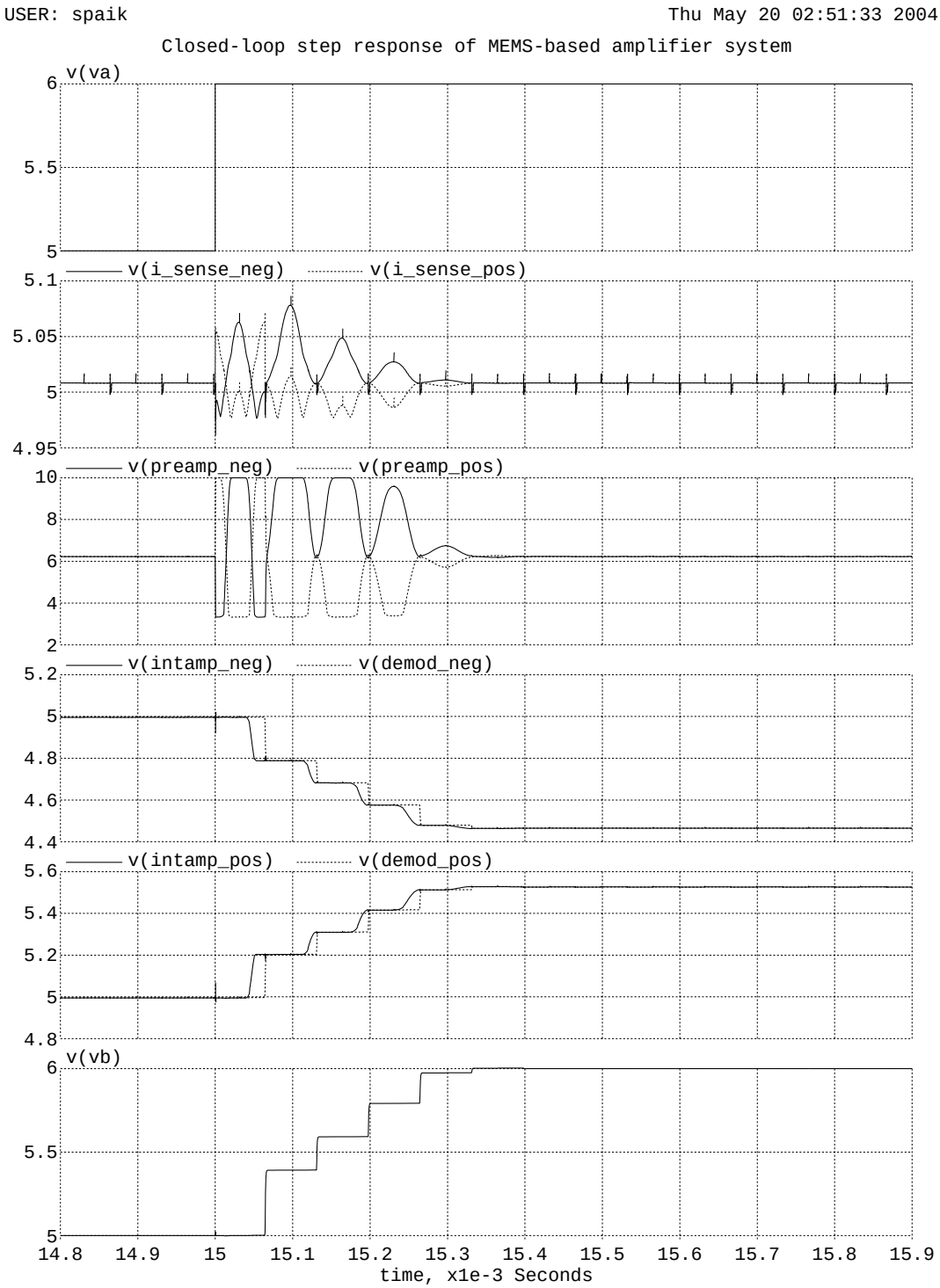

Figure 4-39: Step response of MEMS-based amplifier.

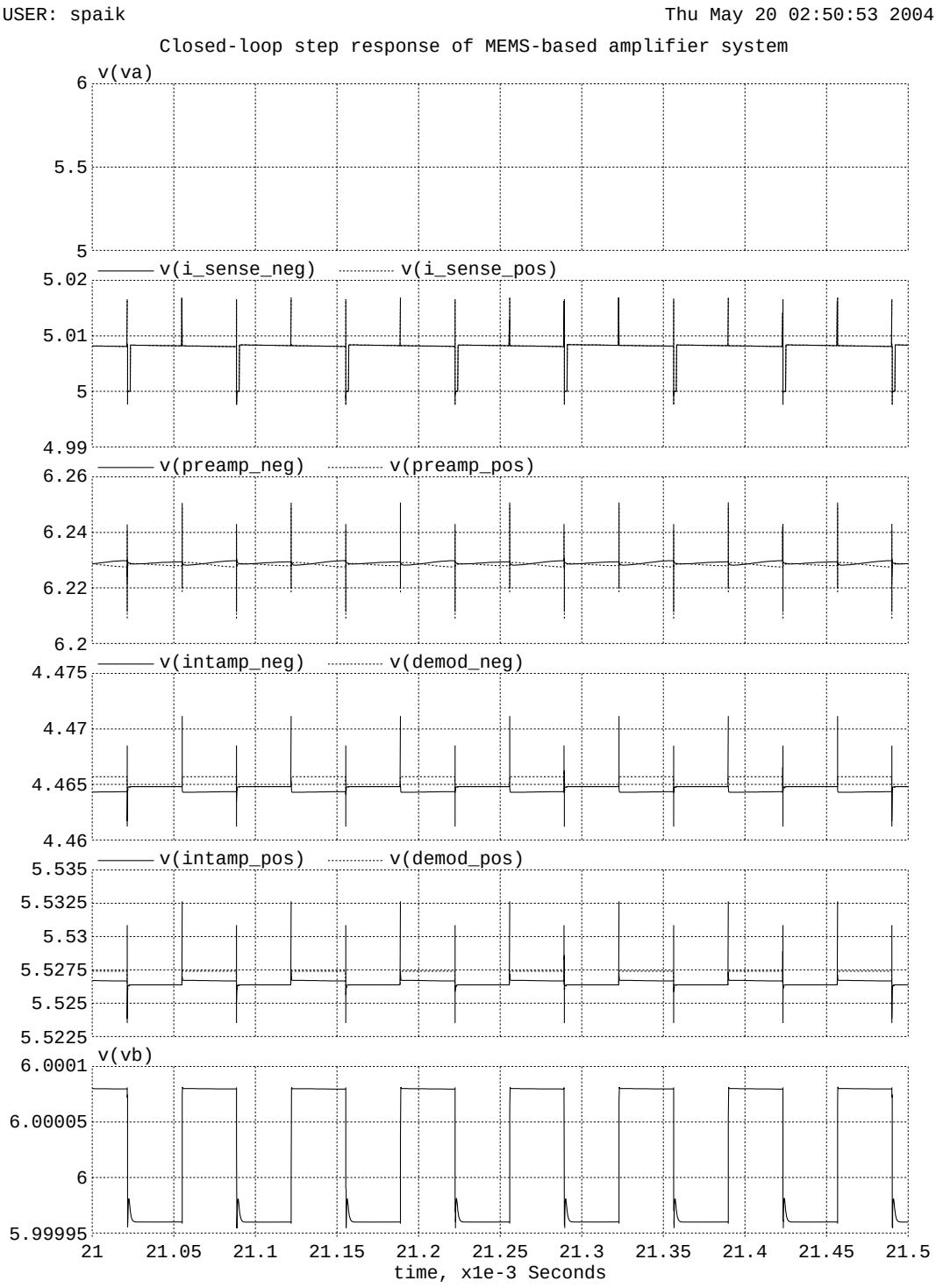

Figure 4-40: Step response of MEMS-based amplifier in steady state.

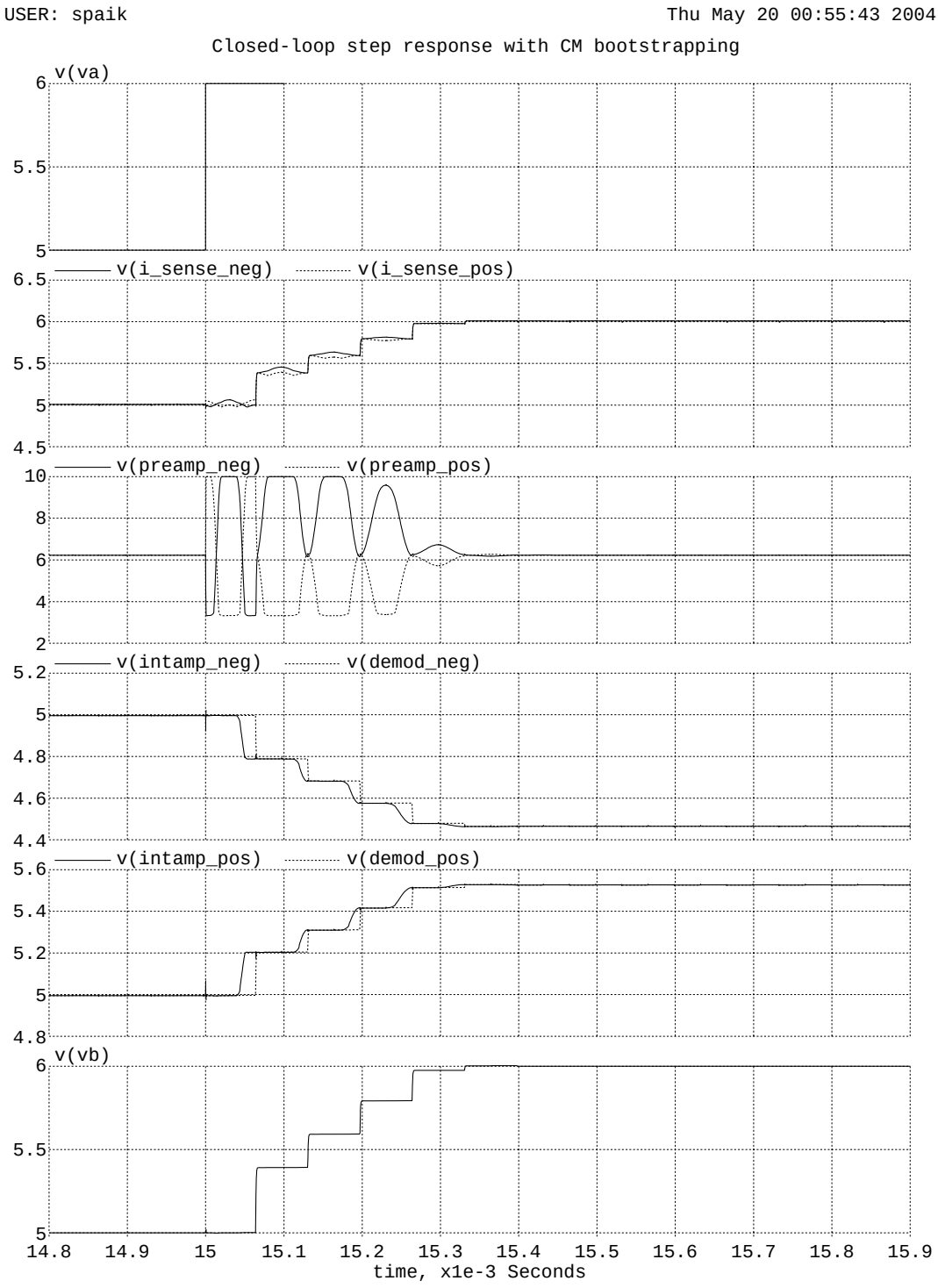

Figure 4-41: Step response of MEMS-based amplifier with common-mode bootstrapping.

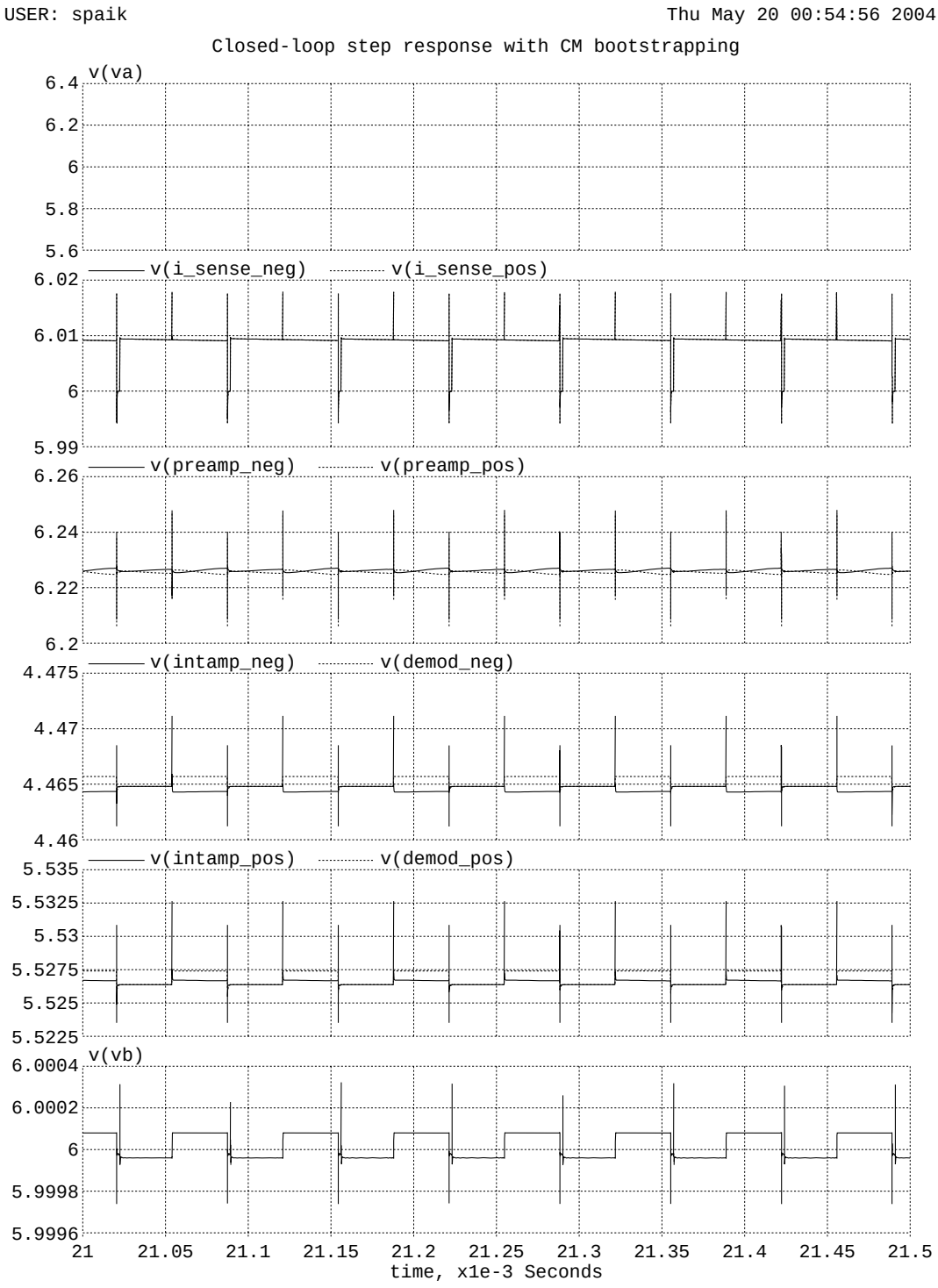

Figure 4-42: Step response of MEMS-based amplifier with common-mode bootstrapping in steady state.

Chapter 5

Conclusions

5.1 Design Summary

A novel amplifier utilizing a MEMS transducer input stage addresses the measurement limitations of existing amplifier topologies. Capacitive sensing of the signal, made possible by the MEMS, circumvents low-frequency noise through up-modulation, and facilitates very low leakage currents with capacitive sensing and dielectric isolation trenches. Two co-dependent feedback loops around the MEMS transducer were designed and analyzed.

The drive loop applies electrostatic voltage drive to sinusoidally vibrate the MEMS transducer beam to create a modulating capacitance. The resonant peaking of the MEMS transducer frequency response makes it desirable to vibrate the moving beam at the frequency of this peak to yield the maximum AC sense current for a fixed drive voltage. Feedback control of the capacitance modulation frequency is made possible by the linear relationship between the drive force and the transducer beam velocity at its desired frequency of vibration. The MEMS transducer may be coupled with a nonlinear element to form a self-exciting oscillator that maintains constant-amplitude oscillations at the resonant frequency of the MEMS structure, and this feedback loop was analyzed. While an open-loop solution using a fixed-frequency oscillator to drive the beam would severely compromise sensitivity and performance as the resonant peak shifts with temperature and process variations, the closed-loop design is guaranteed

to consistently vibrate the beam at its resonance, maintaining the maximum signal-to-noise ratio of the amplifier. Circuitry from a gyroscope prototype from Analog Devices was adapted for this application, and analysis and simulations demonstrated closed-loop oscillations very close to the mechanical resonant frequency.

The drive loop enables the DC input voltage to be transduced into an AC sense current, and the sense loop detects this up-modulated signal, and provides gain and demodulation for a low-noise DC output. However, the gain and demodulator circuits must not add noise into the signal bandwidth to win the benefits of up-modulation, but there was a direct trade-off between noise and offset performance. The sense loop circuits were designed and analyzed carefully with these considerations. In addition, the open-loop gain of the sense loop is sensitive to the absolute value of the modulating capacitances of the MEMS, which also change significantly with temperature and process variations, although their relative values match to 60dB. Accurate amplification of the input voltage is made possible by global feedback, which maintains a relatively constant gain despite variations in the modulating capacitance and other elements that affect the forward path gain of the sense loop. Although the sense loop is not strictly a linear time-invariant system, the open-loop transfer function was approximated, and the stability calculations and simulated transients agreed well. It was also discussed that the relative matching of the modulating capacitances limits the common-mode rejection ratio of the MEMS-based amplifier. A common-mode bootstrapping trick exploiting the global feedback of the sense loop improves this CMRR, but the common-mode voltage range of the input is limited by the linear input range of the sense loop preamplifier.

5.2 Future Work and Design Improvement

The next immediate step for this project would be the layout, fabrication, and evaluation of the MEMS transducer and circuitry for the drive and sense loops. Predicted and simulated performance agreed well, although simulated verification of certain specifications such as noise were not possible with Adice. In addition, a major as-

sumption of this work is that the MEMS structure, as a capacitor, is a noiseless system. Thus, the input voltage is up-modulated noiselessly before it is summed with low-frequency noise. However, the surface of the MEMS plates can potentially trap and release electrons in a manner similar to MOS devices, adding inherent $1/f$ noise in the signal bandwidth. The evaluation of a working amplifier prototype would help determine the fundamental performance limit of a MEMS-based design.

Although the CMRR of the MEMS-based amplifier was improved using a common-mode bootstrap to bias the capacitive output node of the MEMS transducer beam, the input voltage range has been severely constrained to equal the linear input range of the sense loop preamplifier. The MEMS transducer itself is capable of withstanding up to 200V of common-mode voltage, so to fully utilize this wide input range, trim techniques for the MEMS structure should be investigated to improve the matching of the modulating capacitances.

Two other key areas of improvement for this MEMS-based amplifier design are in the noise and offset specifications. One way to decrease the input-referred offset, which is mostly due to charge injection of the demodulator switches, is to increase the preamplifier gain. However, charge injection of the reset switches can potentially cause the output of a high gain stage to saturation. The capacitive node at the output of the transducer can be biased by other means than reset switches, and alternative methods are discussed in [1]. Then, a CDS scheme would not be necessary, and the demodulation of the sense signal may be done in the continuous time domain, also eliminating the increase of noise in the sense signal bandwidth due to aliasing. However, as discussed in [1], the other node biasing schemes have their own set of issues, so there is always a trade-off. To fundamentally improve the noise and offset performance of the system, the MEMS transducer must improve its inherent signal attention of $\frac{C_m}{C_{par}} = \frac{100\text{fF}}{1\text{pF}} = \frac{1}{10}$.

The largest component of the charge injection offset is due to the demodulator switches S1 and S3. This is because charge injected onto the feedback capacitor C_f cannot be differentiated from the charge transfer due to the sense signal at the input of the demodulator. To decrease the effect of this charge injection, the sense signal

gain can be boosted by increasing the capacitor C_s. This increases the open loop transfer function of the sense loop which can quickly degrade phase margin due to the time-delay of the switched-capacitor circuits, and the MEMS-based amplifier may no longer be unity-gain stable. However, typical micro-volt sensors are generally not be used in unity gain, so specifying a minimum closed-loop gain may be an acceptable trade-off for an improved offset specification.

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