THE DESIGN OF AN APPLICATION SPECIFIC INTERFACE DRIVER FOR A HIGH CAPACITIVE LOAD

by

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ALICE I. BIBER

Submitted to the Department of Electrical Engineering and Computer Science on August 28, 1989 in partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering and Computer Science.

ABSTRACT

Unique driver types are required to drive high capacitance loads such as those found in memory subsystems. These drivers are designed specifically to charge and discharge moderate capacitances and drive transmission lines. The driver discussed in this report is intended to drive the receiver networks seen in typical memory subsystems. Matching the output impedance of the driver to the transmission line load improves the overall performance of the system.

Typical drivers have fixed output impedances and cannot match a wide variety of load impedances. Therefore, the performance is reduced to allow the reflections to die out. With an impedance matching scheme, the reflections will be damped out more quickly and net performance will increase. The goal of this thesis is to analyze and design a driver to drive high capacitance and transmission line loads with improved performance over previous drivers.

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Dedication

To MIT Women’s Athletics (particularly the Ice Hockey and Soccer Teams).

I’d have never made it without you.
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1. Introduction

Unique driver types are required to drive high capacitance loads such as those found in memory subsystems. These drivers are designed specifically to charge and discharge moderate capacitances and drive transmission lines. The driver discussed in this report is intended to drive the receiver networks seen in typical memory subsystems. Matching the output impedance of the driver to the transmission line load improves the overall performance of the system.

Typical drivers have fixed output impedances and cannot match a wide variety of load impedances. Therefore, the performance is reduced to allow the reflections to die out. With an impedance matching scheme, the reflections will be damped out more quickly and net performance will increase. The goal of this thesis is to analyze and design a driver to drive high capacitance and transmission line loads with improved performance over previous drivers.

1.1 Background

Memory chips used by modern computer systems need to be organized so that they can be accessed easily and quickly. To do this, "smart" memory cards have been developed. These cards allow the system to efficiently access many memory modules. Also, these memory cards have control logic that allows the data read and write to be very fast. Redundancy and extended error correction improve the reliability of the card.

Memory cards are divided into two major sections: the memory modules and the control logic. Usually, the modules are organized in an array which is then subdivided into any number of memory banks. These divisions allow the access time to the data in the memory chips to be faster.
processor does not spend as much time waiting for data. Thus, overall response time of the system is improved.

The overall performance of memory subsystems is becoming increasingly limited by the signal transmission times as memory chip and control logic technologies evolve. Previously, bipolar buffers and control logic were used to drive memory signals. Designing a specific driver to drive memory signals is one way of attempting to reduce signal transmission times and improve memory system performance. A more application specific driver considers the memory system as part of the load and the design involves the entire system not just the driver.

A typical memory subsystem requires two major drivers: the system bus and the memory bus. These drivers are used to drive signals to the load efficiently and quickly. Drivers to such bus systems provide three states: low, high and high impedance. Certain drivers also convert voltage levels used by memory chips typically designed in CMOS technologies and those used by system logic which may be designed in transistor transistor logic (TTL) or emitter coupled logic (ECL). The drivers in this design are for mid-range to low-end systems which use CMOS technology.

There are two possible configurations where such application specific drivers are used: the system to memory card bus and the memory logic to memory array bus on a card. The design could improve performance in either configuration.

1.2 Motivation

The motivation for this project comes from the designers of “smart” memory cards used in many of IBM’s mid to low end systems. The “smart” memory cards include large amounts of logic circuitry designed to correct and detect errors in the data, refresh data when necessary, run diagnostic testing and interleave the memory banks. The designers have to deal with a large number of restrictions because of the drivers used on these memory cards. The memory subsystems being designed are expandable systems to suit the needs of many different customers. For example, a customer who does not need many memory cards will buy a system with perhaps 4 or 5 different cards including
processor cards, Input/Output (I/O) cards and memory cards. A customer who needs lots of memory because of the programs running in the system may purchase 12 cards instead of just 4 or 5. This customer may have 8 memory cards in the subsystem yet the same driver from the processor must drive this bus. The impedance that the driver sees is different in each case due to the loading of the transmission lines which comprise the system bus. Hence, an impedance matching driver would be useful in this configuration.

The driver's requirements restrict the functionality of the card by using many Input/Output (I/O) pins. Multiple drivers are needed to drive the signal to the receiver network because of the large capacitive load (in both the lightly loaded and heavily loaded configurations). More signal "drive" is needed to charge and discharge the capacitive load at the appropriate speed. If, however, the resistance of the driver does not match the transmission line impedance, reflections cause the time delay to be much larger. Due to the larger drive current, these reflections tend to be very large and in some cases, cause inappropriate switching of the receivers at the end of the transmission line. When too many drivers switch at the same time, the coupling between the lines may cause a quiet line to switch logic levels. Hence, there is a restriction on the number of drivers switching simultaneously.

The designers would like to minimize the reflections due to mismatch in the transmission lines. To a certain extent, the driver can reduce reflections but solving the whole problem requires an analysis of the entire network. Improving the overall performance is the primary goal of this project and designing a driver specific to memory cards is a result of this system analysis. However, as with any specific driver design, the new restrictions on the use of this driver and the improved performance are trade-offs that the system designer must consider during the design.

1.3 Previous Attempts

Most driver designers consider four things when designing drivers: delay, output impedance and the first derivatives of the pull-up and pull-down current (di/dt) and output voltage (dv/dt) which establish the amount of noise generated by the driver in the system. Since noise and delay are high priori-
ties, the impedance is not considered a high priority. This impedance mismatch can make a memory driver very good or adequate. Therefore, in addition to driving a high capacitively loaded net, the driver design will emphasize impedance matching in order to improve its performance in most configurations.

Matching the transmission line is not a new concept. Many of the CMOS drivers already in existence try to match a transmission line of a certain impedance by placing a pull up or pull down resistor in series with the driver output devices. A family of drivers with different output impedances are offered to match different transmission lines. However, when using expandable and configurable systems selecting a different driver is no longer an option. Also, in an attempt to minimize the number of different parts, a self-adjusting output impedance matching driver seems useful.

The driver chosen for the lightly loaded net must also work for the heavily loaded net. Since each transmission line is loaded with a different distributed capacitance depending on the configuration, the effective impedance of such a transmission line varies between configurations. Thus, the driver's output impedance will not match in each configuration. This driver design attempts to match the transmission line impedance with the output impedance of the driver through an impedance matching scheme. This scheme will reduce mismatch of the impedances and allow for some flexibility in modifying the system to provide better overall performance.

The basic reason for a more specific driver design is that typically finding the right output impedance for a particular net, having this particular output impedance driver and making this driver work well even as the configuration of the system changes is extremely difficult. Also, because of the capacitive load, often multiple drivers are used to transmit one signal to the entire array. With a variable output impedance design, the need for additional drivers could be eliminated or reduced. Reducing the number of drivers will reduce the I/O pin count where constraints are always tight. Also, it may be advantageous by reducing the number of modules needed on a memory card. In general, the performance of the memory system will be improved by optimizing the network.
1.4 Thesis Organization

This thesis will present a new perspective on driver design. The research considers the customer (memory card designers) perspective before the traditional perspectives. Though this design may not be optimal in some cases, this particular circuit provides a new means of improving system performance. This first section provides the background necessary to understand the problem. The second section, 2, "Methodology" on page 7, outlines the goals and considerations of the design. The following four sections describe the assumptions, analysis and design iterations. These four sections include the transmission line model, the driver design, the feedback design and the control circuitry design. The last two sections, 7, "Results" on page 45 and 8, "Conclusions" on page 56 describe results from actual network simulations and the conclusions drawn from these simulations. These sections also include the restrictions placed on the design and designer as well as suggestions for improvement and buildability. This last section includes future goals of this project.
2. Methodology

2.1 Literature Search

A literature search on drivers was conducted but this topic is not covered extensively. However, other topics such as SRAMs, receivers and bipolar drivers are useful in determining an approach to this particular problem. The articles on driver design and impedance matching are useful in understanding the complexity of the problem. Other articles such as the "VLSI Performance Compensation for Off-Chip Drivers and Clock Generation"\(^1\) contribute to the idea of an impedance matching driver and the partial implementation of such a matching circuit. Since only one article in particular addresses the driving of a transmission line with a CMOS driver, ideas are pieced together from other articles. Most of these articles are found in IEEE Journal of Solid State Circuits and the IEEE Custom Integrated Circuits Conference. Other references include texts on CMOS design, transmission line concepts and analog design.

The articles used can be broken down into four categories. The first category is the off-chip driver itself. The basic design including the predriver stage and the output stage are shown in many off-chip driver (OCD) articles. The variable output resistance scheme using a parallel linkage of devices has been seen extensively, although not with this purpose: to match the output impedance. Several of the

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articles pertain to driving different transmission lines, the termination techniques and the performance. These articles were useful in understanding the load of the driver and attempting to optimize the performance. The next category was the amplifier/comparator needed to measure whether the load was matched to the output impedance of the driver. The amplifiers used in other technologies such as BiCMOS and ECL provided useful topologies that were converted to pure CMOS for this particular design. The last category would be noise, used to analyze the overall performance of the system. These articles provided the background for the comparison of the driver to other existing drivers.

2.2 Special Considerations

The goals of this thesis project are to analyze the network of a memory subsystem and to improve the performance of the network by improving or changing both the network and the driver design. In the end, the performance of the memory subsystem is most important. In order to improve upon its performance, the system and memory bus specifications must be analyzed and the driver must be designed to better meet these requirements.

Designing a more specific driver for a memory subsystem includes the following considerations:

- simultaneous switching
- output impedance matching
- output noise tolerance
- speed (delay time)
- power dissipation
- area
- effects of process, temperature and voltage variation

Some of these considerations can be emphasized more than others depending on the driver design. Since most of the topics are related in some way, there are some trade-offs to be analyzed. In order to analyze the trade-offs properly, one must consider the system as a whole first then break it down into parts, considering the trade-offs of each part then combining all the pieces of the puzzle for the final design.

Most of the articles found in the literature search pertain to bipolar drivers and lightly loaded nets; these articles are therefore not very applicable. Since the overall performance is limited by a combina-
tion of elements, the project turned towards system optimization rather than driver design. In looking at the system, there are many degrees of freedom that contribute to improving the performance of the subsystem.

The design of an impedance matching circuit to complement a driver already in existence is not feasible since most drivers have only one output impedance. Therefore, designing a whole new driver along with the impedance matching circuit would maximize the performance of the subsystem. The concept is simple; the implementation is much more difficult. Few changes are necessary to produce such a circuit on an actual chip; such changes are discussed in 7, "Results" on page 45.

2.3 Impedance Matching Algorithm

The technology used for this design is a mature, high performance, 1.0 μm, 5 volt, CMOS technology. The basic idea behind the impedance matching algorithm is to measure the voltage at the output of the driver. The transmission line initially looks like a pure resistor (to the incident voltage wave) and therefore, there is a resistive divider between the output impedance of the driver and the transmission line. The incident wave divides across a voltage divider until a reflection is sent back from the far end of the transmission line. If the voltage at the output of the driver is exactly half the voltage swing then the driver output impedance matches the transmission line being driven. However, if the voltage is high or low, the output impedance needs to be changed accordingly. Rematching each time a signal is sent out is not possible because of the technology's speed and the load the driver is driving. The time required to measure the voltage, latch the binary output of the comparator and reset the output impedance is much longer than the time required for the signal to propagate to the load. Therefore, the matching would have to occur upon power-up and be stored in memory.
The Successive Approximation Scheme also used in analog to digital converters is an appropriate choice.² The scheme involves setting a bit, measuring the result and resetting or leaving the bit. Accurate analog to digital converters use this technique with a string of resistors or capacitors. In this case, the scheme requires a voltage comparator and several storage devices or latches to remember the status for that particular driver. The basic block diagram of such a system is shown in Figure 1 on page 11. The driver consists of the predrive and output stages. The load is a transmission line and the receivers are at the far end of the load. The comparator feeds back information to the latches and the output stage of the driver to determine what the impedance is. The output stage sets the impedance of the driver by turning on or off several bits.

The number of bits is determined by the range of resistances needed within the area constraint. Three bits allow eight different output impedance values to be used but keep driver area inputs to a minimum. The specifics of implementation will be covered in subsequent chapters.

2.4 System Description

A mid to low end system consists of two major parts: the processor (or system itself) and the appendages (or the auxiliary parts). Included in the auxiliary parts are the memory cards the system uses, perhaps a printer or a modem, and any other plug-in accessories to the system. The following block diagram, Figure 2 on page 12, illustrates the division between processor and its appendages.

Drivers in this configuration transmit signals through the transmission lines to the accessories. However, the accessories also need drivers to send signals to the processor. Depending on the configuration of the system, the impedance seen by one driver could be different from the impedance seen by another driver. Hence, an impedance matching driver could be useful. For example, in Figure 2

Figure 1. Block diagram of impedance matching scheme

on page 12 the printer and memory card two would see the characteristic impedance of the line where the hard drive and memory card one would see a more heavily loaded line.

There is another configuration: on the memory card itself. Typical memory cards contain two major divisions: the logic and the memory. The logic is used to access the memory in an organized fashion, to provide control functions, to provide error correction capabilities and direct memory addressing capabilities, all to improve the response time of the memory card. Each memory card's memory chips are organized in an array manner. Within this array, they are divided into any number of "memory banks" as seen in Figure 3 on page 13. A memory bank is a smaller group of modules also accessed in an array fashion. The logic modules are beneath the array of memory modules. The

2. Methodology

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memory banks do not have to be split directly down the middle, although traditionally, banks have been split in this manner.

Drivers used in this type of a configuration drive signals from the logic modules to the array modules. Typically, the signals are driven to 10 or 20 modules at a time. A typical card has between 40 and 80 modules on it. The transmission lines are from the logic driver to the array’s edge and from the array’s edge to each individual module that needs to be accessed. However, there are some simplifying assumptions which will be addressed in 3, “Bus Analysis” on page 15.
Figure 3. Memory modules on a memory card. Each card is divided into banks consisting of memory modules.
Both configurations require that the transmission line load be driven properly and with the correct termination. Otherwise, the reflections must settle out before the signal is assumed valid thus increasing the signal delay time. Depending on the load and the driver, this delay can be very long. Attempting to minimize this time is a primary goal and will improve the driver's overall performance.
3. Bus Analysis

3.1 Transmission Line Theory

Interconnections between the processor and the accessories of the system can be accurately modeled as transmission lines provided that the rise time of the signal and the propagation delay time of the signal are of similar magnitudes. Since in this analysis, the rise time and propagation delay time are similar, transmission lines are used to model the interconnections. However, with the use of transmission lines, there are a few assumptions made. The transmission lines are assumed to be lossless since in this case, this model is adequate. The resistance of the conductors is assumed to be negligible compared to the input and output resistance of the circuitry. Secondly, the dielectric properties of the insulators are assumed to be good. The phase distortion and bandwidth limitations are therefore considered negligible. In other words, technically, the transmission lines are assumed to be "ideal". With these simplifying assumptions, the transmission line models break down into three parameters: the characteristic impedance, $Z_o$, the time delay, $T_d$ and length.

The characteristic impedance is defined in terms of a distributed inductance and a distributed capacitance. For any length of transmission line where these two distributed parameters are constant, the impedance is equivalent to $Z_o$. The relationship also describes the transient voltage and transient current on the transmission line.

$$Z_o = \frac{v}{i} = \sqrt{\frac{L_o}{C_o}}$$

(1)
where $L_o = \text{inductance per unit length}$, $C_o = \text{capacitance per unit length}$, $Z_o$ is in ohms, $L_o$ is in Henrys and $C_o$ is in Farads.

Propagation delay or time delay, $T_d$ in time per length is also a function of both $L_o$ and $C_o$ as seen in the following formula.

$$T_d = \sqrt{L_o \times C_o}$$ (2)

These equations are only valid when the transmission line is considered lossless. In this case, there is no series resistance and no parallel conductance to allow power to be dissipated. Due to the original assumptions made, the more complicated formulae of lossy transmission lines will not be used here.\(^3\)

Whenever there is a discontinuity in the transmission line impedance, there will be a reflection. These reflections cause voltages on the transmission line to double when the load at the end of the transmission line is an open circuit or an approximation thereof. The settling time of a transmission line voltage to a certain value can be very long because of multiple reflections. When reflections are properly damped using termination techniques, the settling times are much shorter.

There are two types of termination techniques commonly used in damping or preventing reflections: series and parallel. As the names imply, the resistance either goes in series with the transmission line load or in parallel with the load. There are several advantages and disadvantages to each technique. The parallel termination technique and the series termination technique are shown in Figure 4 on page 17.

Parallel termination requires putting a resistor in parallel with the receiver at the receiving (or far) end of the transmission line. The initial voltage swing at the termination is the sum of the incident and

Figure 4. Termination techniques. Series and parallel termination techniques involve the placement of the termination resistor either in series or in parallel with the load.

reflected waves. Therefore, if the line is well matched, the initial voltage swing will be a delayed incident wave as shown in Figure 5 on page 18.

Series termination requires a resistance between the driver and the transmission line with no termination at the far end. Here, the initial waveform at the receiving end (provided that the receiving end is sufficiently far away from the driving end) will be doubled as soon as the incident waveform arrives (see Figure 5 on page 18). The waveform at the beginning of the transmission line (or near end) takes on a step form. The step lasts two time delays then the full voltage swing is seen. The voltage divider action of the resistor and the transmission line's characteristic impedance, which initially looks
Figure 5. Waveforms of different termination techniques. Series and parallel termination waveforms are distinctly different.

like a resistor, cause the step in voltage to occur. This step feature will be exploited by the impedance matching circuitry in this design.

The size of the reflected wave depends on the load. The reflection coefficient is the typical measurement that helps determine the size of the reflected wave. The reflection coefficient is defined as:

\[ \rho = \frac{Z_L \times Z_o}{Z_L + Z_o} \]  

(3)

where \( Z_L \) is the equivalent impedance that causes the reflection.
Series terminated nets are "first reflection" nets. The receivers switch as a result of the reflected waveform. The delay time in the first receiver would be $2 \times T_d$ (at worst case). With parallel terminated nets, also called "first incident" nets the switching occurs due to the incident waveform. Thus, the delay is only a $T_d$ (at worst case). Therefore, for the fastest systems series terminated lines are unacceptable.

The parallel termination technique's main advantage is that the reflection is dampened out at the load if the parallel resistor is matched to the transmission line. The settling time of the transient voltage in this case would be approximately one delay time of the transmission line. However, the driving source of this transmission line must have a very low impedance. Obtaining a sufficiently low drive impedance is difficult in CMOS. Therefore, series termination is sometimes more practical.

In series termination, the reflections due to the load are not dampened out until they arrive at the source. The settling time of the circuit is $2 \times T_d$ of the transmission line. However, the proper output impedance of the driver does not have to be as low. The trade-offs here are the delay time vs. the output impedance of the driver. Another advantage of the series termination is that the termination does not depend on the load. Any type of load can be on the end, but if the series resistance matches the transmission line, the reflection will be dampened out as much as possible. A disadvantage is that if the transmission line is long enough and has enough discontinuities, the output voltage can look like a staircase instead of a smooth transition. For certain types of circuits, such as clock circuits, this staircase waveform is unacceptable. However, the processor and memory busses can be analyzed to determine which termination technique to use.

The processor and memory busses can be modeled in a similar way. Basically, the model is a driver driving one transmission line which is connected to another transmission line of lower impedance. This transmission line is of lower impedance because of the distributed capacitance hanging off of it.
3.2 Memory Bus

Signal paths are modeled as transmission lines because ideal conductors do not really exist. However, when these transmission lines become short compared with the rise time, the response looks as if the transmission line load were just a lumped load. Thus, the model of the memory array can be made much simpler. The array, as shown in Figure 6 on page 21, can be modeled as another transmission line of lower characteristic impedance.

This figure can be separated into two portions: the longer transmission line and the capacitively loaded transmission line. The model has two transmission lines each with a different characteristic impedance. The characteristic impedance for the loaded transmission line depends on the load. The new impedance, \( Z'_o \), is the old \( Z_o \) modified by the distributed capacitance, \( C_D \). The following equations show the relationships.

\[
Z'_o = \sqrt{\frac{L_o}{C_o + C_D}} = \sqrt{\frac{L_o}{C_o}} \cdot \sqrt{\frac{C_o}{C_o + C_D}} = \sqrt{\frac{L_o}{C_o}} \cdot \frac{1}{\sqrt{1 + \frac{C_D}{C_o}}} = Z_o \cdot \frac{1}{\sqrt{1 + \frac{C_D}{C_o}}} \tag{4}
\]

where \( C_D \) is the capacitive load, \( C_L \), divided by the length \( \ell \).

Reflections due to the source and the load are not the only reflections in this system. The impedance mismatch caused by the capacitive loading will also contribute to some reflections. The only way to solve the problem completely would be to match the transmission line impedance at every junction. However, such matching would be equivalent to having just one transmission line. Matching at every junction is very difficult because of the complexity involved although many high performance bipolar systems do match at every junction. The next best thing is to try to reduce the reflections that occur at each junction.

In attempting to reduce these reflections, the impedance of the initial transmission line must be considered. Looking at a memory card, there are two types of wiring: microstrip and stripline. Both of
Figure 6. Transmission line model of a card net. The shorter transmission line stubs and the capacitive loads can be modeled as another transmission line of a lower characteristic impedance.

The wiring impedances depend inversely on the square root of the dielectric constant, $\varepsilon_r$, and also inversely on the width and thickness of the trace. Microstrips also depend on the thickness of the dielectric beneath the conductive strip. Figure 7 on page 22 shows the microstrip and the stripline.

Making the microstrip or the stripline wider reduces the impedance. Widening the lines is not always practical since minimum width lines use the least amount of area. Within the array portion of the memory card, minimum width lines are imperative because the capacitive loading already reduces the impedance to a large mismatch. However, for the lines from the logic modules to the edge of the array, wider lines should be used to try to decrease the mismatch between the two transmission lines.
Figure 7. Microstrip and stripline memory card wiring. Memory card wiring impedance depends on the type of wiring used. Usually both types of wiring are used on one memory card.

Using a sample connection of memory modules and sample lengths, a test load network is obtained. This network is used in the initial design and test phase. An actual net model is used later to measure performance of this driver vs. other drivers. In the test model, the line mismatch is greater than 3 to 1 causing some very large, undesirable reflections that reduce the performance of the memory system.

Assuming the width of the conducting line between the memory control logic and the array edge can be increased, a new driver output impedance must be made to match this new impedance. Here, an impedance matching circuit would be useful. The designer does not need to know prior to manufacturing how wide the transmission line will be since the impedance matching circuit will measure the
impedance and match to it. Also, as mentioned before, the impedance of the line could be different depending on the configuration of the system.

3.3 Processor Bus

The analogies to the memory bus are easily seen. The transmission line has capacitive loads and the signals need to be driven to a variety of destinations. Therefore, the model and procedure is parallel to the memory bus analysis. The line lengths and capacitance values differ slightly causing the impedance of the line to change. However, basically the analysis is the same and the outcome is also the same.
4. Driver Design

4.1 Predriver Stage

The drivers needed for busses in a memory subsystem are three state drivers. The three states produced are low, high and high impedance. When one driver is driving the bus, no other driver should be driving the bus high or low; any other drivers must be in a high impedance state. Such drivers usually have a data input, an enable, and an output.

The drivers usually consist of two stages: the predrive and the output. The predrive is used to gate the enable signal with the input signal yet still allow the output stage to provide a high impedance signal. The predrive requires a NAND gate, a NOR gate and an inverter. Basically, the data input and the enable are NANDed and fed to the output stage of the driver. The data input and the negative of the enable are NORed and also fed to the output stage. Figure 8 on page 25 shows a block diagram of the predriver stage.

The sizes of the predrive devices depend heavily on the amount of loading seen. Since MOS devices have gate to source and gate to drain capacitance which depend mainly on the width of the device, the loading depends on the width of the devices. The larger the devices the more current is available to charge or discharge the capacitors. However, being as fast as possible is not always a good idea since there are several other considerations. First, noise is a consideration. The faster and larger devices tend to produce more noise since their change in current vs. time (di/dt) is large. Secondly, area is a consideration. The larger devices obviously use more chip area. However, due to the large
Figure 8. The predriver stage. The predriver stage regulates the output transition rate by the size of its devices. It also allows the third state of high impedance to be produced by the driver.

currents and small resistances needed in the output stage the devices in the output stage need to be large.

4.2 Output Stage

Normal output stages are required to provide current for the load. Other considerations are driver impedance variation and impedance values. The output stage of the driver is used by the feedback circuitry to match the impedance of the transmission line. There are several ways of varying the output impedance of a driver.
Under normal circumstances, the output stage of a driver has a resistor in both the pull up and pull down portion of the circuit to match the output impedance. This resistor, however, is not easily varied. One option would be to add an array of resistors or a resistor string as seen in many analog to digital converters. Making resistors in a CMOS process is more costly than making transistors. However, CMOS transistors can be used as resistors. One exploitation of this idea would be to vary the gate to source voltage thereby causing the current through the transistor to vary. By Ohm's law, the resistance would vary also. However, varying the gate-source voltage requires a low impedance external source which adds complexity. Another idea would be to have several MOS transistors in parallel, and turn them on or off, as necessary as in Figure 9 on page 27. This type of output stage would allow a similar freedom to the resistor arrays but using transistors to provide the required resistances.

This type of architecture has been used in driver designs before but not to intentionally vary the output impedance. The each leg of the output stage requires two transistors, one of which is used as a switch to turn on (or off) the leg, the other to set the impedance. The resistance of MOS transistors is inversely proportional to the current, and therefore, proportional to the length over the width. Therefore, the longer the device is, the higher its resistance will be.

All the fingers or legs have two MOS transistors so that they can be turned on and off except the first finger. The first finger is always on so that there is always an output. With only the first finger on, the output resistance is the highest. When another finger is turned on, its resistance goes in parallel.

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with this resistance causing the overall resistance to decrease. The basic idea behind the successive approximation scheme is to turn on a finger, measure the voltage, then decide whether to keep the finger on or turn it off. However, instead of turning on the most significant bit first then continuing as the scheme says, the smallest resistance will be turned on first. So, in addition to the largest resistor, there is a small resistor in parallel. The comparator divides the possible resistances into two sections: high and low. This process is repeated again to divide the remaining portion into two sections also. After the third time, the resistance should approximately match the transmission line impedance. In this way, the impedance matching scheme can match to 8 different resistances by
sending out just three pulses (the pull up portion is matched on an up transition and the pull down portion is matched on a down transition).

4.2.1 Special Consideration

Special consideration is given to the drivers of row address select (RAS) lines on a memory card. RAS lines should not be activated unless the start of a refresh or read cycle is imminent. To avoid this problem, certain signal timings are very important. The array modules will not enter obscure test modes if the RAS lines are activated while the CAS lines and output enable lines are inactive. Please refer to 6.5, "Restrictions" on page 43 for more restrictions.

4.2.2 Resistance Values

Typical impedance values range from 20 to 100 ohms. This range would allow the designer to use this driver in almost all situations without having to worry about the impedance. So, with three bits, there will be eight different resistances. However, the weighting of the fingers determines the spread of the resistances. Since the existing drivers have impedances of 20, 40, and 80 ohms, these are some of the impedance values that this driver output stage should have. Making a binary weighted output stage concentrates the impedances on the lower end too much. There would only be 2 impedances above 45 ohms. Using resistors of 90, 180, 90 and 45 ohms respectively, the output impedance values would be 90, 60, 45, 36, 30, 26, 22.5 and 20 ohms. The one finger that is always on sets the highest impedance. Since process variations will change the resistances of the MOS devices, the highest impedance should be set around 100 ohms. Realistically, the highest impedance seen by the driver should be about 85 ohms. With all the fingers turned on, the impedance should be at its lowest of about 20 ohms. However, getting down to this low impedance requires incredibly large devices. Therefore, the sizes were chosen so that resistances range from 32 ohms to 100 ohms in a nominal process.

As process conditions vary to the extremes, the device sizes chosen do not yield the same resistance values but since this circuitry exploits feedback the matching scheme still works. Obviously, if all the fingers are off then the output impedance is the highest possible resistance. Conversely, if all the
fingers are on, the output impedance is the lowest possible resistance. The actual resistances will vary somewhat with process conditions. The scheme has been proven to work well under nominal test case conditions.

To set the resistance of the devices, the output node is tied to \( \frac{VDD}{2} \) and the current is analyzed. Using Ohm’s law, a target current is obtained for each finger such that the resistance of the finger corresponds to the target resistance. The target resistance values are the following: 100, 400, 200 and 75 ohms. These resistances provide output impedances in the range of 100 to 32 ohms as seen in the following table.

<table>
<thead>
<tr>
<th>Finger 1</th>
<th>Finger 2</th>
<th>Finger 3</th>
<th>Finger 4</th>
<th>Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>100 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>80 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>66.7 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>57.1 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>42.9 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>38.7 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>35.3 Ohms</td>
</tr>
<tr>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>32.2 Ohms</td>
</tr>
</tbody>
</table>

4. Driver Design 29
The response at the output of the driver ideally would be a staircase voltage with only one step. However, due to imperfections (non ideal circuit components, noise etc.), the voltage waveform is not just an ideal step: there are several 'glitches' and reflections due to capacitances at the end of the line. Although these capacitances are not large, the reflections (as seen at the output of the driver) may be quite large. Therefore, the timing of the feedback circuitry is critical to make this system function properly. If, for example, the timing is too late (or too early), the voltage measurement of the feedback circuit will cause the output stage of the driver to incorrectly match the transmission line. As the mismatch increases, the over and undershoot of the waveform as seen by the memory modules can exceed the specified limits. Even though there are protect structures at the receiver end to attempt to minimize damage to the module, such large over and undershoot waveforms should not be sent to the receiver repeatedly.

Large but reasonable overshoots to the receiver mechanism should not be a problem if they do not occur frequently. In order to match to the transmission line, there will be some large overshoots but if the timing is done correctly, these overshoots will occur once or twice during power-up only. After the output stage impedance matches the transmission line impedance, the overshoots should be within the specifications for the receivers. The timing of the feedback circuitry will prevent the overshoots from becoming a major problem.
5. Feedback Circuit Design

5.1 Requirements

For the successive approximation scheme to work in matching the impedance of the transmission line, the voltage on the line at the output of the driver must be measured and compared to half the voltage swing. A comparator is used to compare the output voltage to the reference voltage. After the voltage is measured, a memory device such as a latch must be set to remember which fingers of the output stage to use. There must be three latches for the pull up stage of the driver and three latches for the pull down stage of the driver. The impedance matching scheme is controlled by a 'black box' controller. The requirements of this black box are detailed in 6, "Control Circuitry" on page 40.

As with any MOS comparator or amplifier, offset voltage is a concern. However, in this situation, the differential input voltage is large enough to overcome the offset voltage and therefore, no offset cancellation scheme is considered. If the differential input voltage were on the order of the offset voltage (of about 10 mv) then such a cancellation scheme must be used.

5.2 Implementation

The feedback circuitry involves comparing two voltages and storing the result in binary form (i.e. either a one or a zero). The scheme requires six latches and a comparator. There are several ways of implementing the latches and the comparator in CMOS technology but some implementations are
more practical to the particular situation than others. Only three different circuits were considered: the cross-coupled latch, the CMOS sense amp, and the separate amplifier and latch.

5.2.1 Cross-Coupled Latch

One idea is to have the comparator and the latch in the same circuit as shown in Figure 10 on page 33 called the cross-coupled latch. Basically, this circuit is set up as a differential pair of MOS transistors with a biasing current source, a reset transistor and the cross-coupling to provide the latch. A differential input stage is chosen because most comparators are designed with such an input stage to keep the input impedance high, to provide a symmetrical input stage and to provide initial gain. The cross-coupling provides the feedback to set the latch. If this differential configuration does not provide enough gain for the latch to trigger valid voltage levels, another stage (a basic inverter) can be added to provide the extra gain necessary. Although this extra stage may be necessary in order to build such a comparator, the extra delay time puts more restrictions on the use of this feedback circuit. The major problem with this implementation (i.e. the comparator and the latch together) is that six comparators would be necessary and five would be idle at any given time.

5.2.2 CMOS Sense Amp

Another idea is a CMOS sense amp type comparator. In CMOS memories, sense amps are used to detect voltages of 50 to 100 millivolts between two bit lines in a memory array. The sense amp detect this signal and restore the voltage on the storage capacitor to the full logical potential of 0 or 1. The sense amp design is similar to the design discussed above except that there are basically two cross-coupled inverters which function as both the comparator and the latch. As shown in Figure 11 on page 34, this requires accurate and complex clocking.

This particular sense amp requires particularly complex timing. The pull down of the n transistor should be slow then fast. The p device must be pulled up after the n device is pulled down. Also, the strobe signal must zero out the latch right before sensing the voltage. Due to the many clocks involved and the similar problem of too many comparators for one circuit, this idea is abandoned
Figure 10. Cross-coupled latch. This idea used a differential pair and positive feedback to make a comparator and a latch, all in one.

also. A simpler topology of just a comparator connecting to 6 different latches seemed more appropriate.

5.2.3 Separate Comparator and Latch

This circuit in Figure 12 on page 35 uses a differential input, a bias transistor and two transistors as loads. This circuit is a simple single stage sense amp configuration; it detects small voltages and forces the output to a one or a zero. The gain of the differential circuit is $g_mR_L$. However, the output is single ended only so the gain is divided by two. Another stage following this input stage is necessary to get the voltage level shifted to valid logic levels. The gain of the input stage is about 10 and the
Figure 11. CMOS sense amplifier. This sense amplifier is similar to the cross-coupled latch, but it requires accurate clocking for proper operation.

delay time on the test circuit under nominal conditions is 2 ns. As seen in Figure 12 on page 35, the reference voltage and the bias voltage are produced by a simple voltage divider using diode connected transistors. These bias strings are turned on with a signal called TEST from the controller to prevent the circuit from drawing current (and therefore dissipating power) during normal operation. The output of the comparator feeds all six latches.

The amount of current in the circuit and the gain of the circuit are trade-offs. More current gives less gain because of the relationship between $g_m$, $R_L$, and the current. Out of a differential stage, the gain should be about 20, however, since the output is not differential half the gain is 'thrown away'. A
gain of 10 is acceptable and produces reasonable results. While more current would drive capacitance faster and therefore reduce the delay time of the comparator, increasing current involves decreasing the gain and makes it more difficult for the second stage to level shift the output. If more current is necessary, another stage of gain may be necessary too, because the output signal of the comparator may not be able to reach the valid logic levels for the latches.

These latches use positive feedback of two inverters to be set. The inverters are cascaded and the signal is fed back to the original inverter as shown in Figure 13 on page 36. The initial problem is where to set the unity gain points of the inverters to make the latch operate quickly and cleanly.

With the time needed for the comparator to pull down to 0.8 volts or the most positive down level
Figure 13. Latch design. This circuit is a positive feedback latch consisting of 2 inverters.

(MPDL) and to pull up to 2.4 volts or the least positive up level (LPUL) equal, the first inverter should be centered around half the voltage swing of 0.8 to 2.4 volts. The latches for the N pull down stage need to pull up quickly so the unity gain point for this first inverter is 1.2 volts. The latches for the P pull up stage need to pull down quickly so their unity gain point is slightly higher at 1.67 volts. The second inverter's unity gain point is set to 2.7 volts because pulling down takes longer than pulling up.
5.2.4 Timing

A strobe signal is used to time the setting of the latches. The timing of this strobe signal is critical to the proper operation of the feedback circuitry since if the signal is too early or too late, the wrong output of the comparator may be read by the latch causing the output stage of the driver to have an impedance mismatch. Since this timing is so critical, an on chip clock generation circuit was necessary (Figure 14 on page 38). Assuming that several signals from the control box as discussed in 6, "Control Circuitry" on page 40 are present, a short strobe signal can be generated with minimal circuitry. The 'CLK' signal is fed through a slow inverter and to a NAND gate simultaneously. The output of the slow inverter is also fed to this gate thereby forming a circuit more commonly known as a 'oneshot', in Figure 14 on page 38. The output of the oneshot, called 'CCOUT', is fed through an NAND gate with a control signal from the control logic to tell which strobe signal should be on.

5.3 Design Points

This design is practical because it requires only one comparator. The other designs would have had most of the comparators idle most of the time. This design also requires less clock signals than the CMOS sense amp. Even though this circuit has six different strobe signals, the STRB timings are generated by one oneshot, therefore, the clock generation for this circuit is not too difficult. One other advantage is that there are only two stages to the comparator making the comparator very fast. Speed is a key issue because the step in the voltage at the output of the driver is present for only twice the delay time of the transmission line. If the transmission line is short, the step will not be present long enough for the comparator to react to it. Such problems present some restrictions in the use of the driver.

Some other issues include whether the design is feasible for a non-nominal process. This design is pushing the technology to the edge of its limit in terms of speed and noise. If the transmission line were slightly shorter then the time of the step would be too short to allow the latches to set. The output impedance of the driver would be in the lowest impedance state because the latches would set
Figure 14. One shot timing generation circuit. This one shot circuitry generates the pulse necessary to strobe the pass gate.

to this state. Since the devices are so large yet the lengths as small as possible, this circuit is very susceptible to process channel length variation. However, these are some of the trade-offs made in design and they cause some of the restrictions on the driver.

5.4 Constraints

In order to build this design in reality, several changes are necessary. First, the output impedance range should be smaller. Then, the device sizes will vary less and the sizes can be smaller. Some minor changes are also necessary to do a feasible layout because area is such an important consider-
ation in these types of circuits. For example, another gain stage might be necessary in the comparator. This added stage would increase the reliability of the circuit and decrease the variation due to process but would imply a greater restriction on the transmission line length. Decreasing the speed of the circuit would also help by decreasing the total area needed. Also, decreasing the transition times of the driver's predrive and output stages would help reduce the noise generated due to such fast transitions. In general, it is better to drive circuits as slowly as possible to reduce coupling, di/dt and dv/dt noise. However, decreasing the transition times significantly reduces the amount of time that the plateau is visible, and therefore, the comparator needs to be even faster.
6. Control Circuitry

6.1 Black Box Requirements

This black box is the master controller of the whole scheme. The controller sends out test voltage pulses and when the matching is complete turns the feedback circuitry off. The black box’s entire job is to carry out the successive approximation scheme of impedance matching the output stage of the driver to the transmission line load. The black box is the interface between the system and the driver and is intended to be transparent to the system. However, there is one signal required from the system: the ‘TEST’ signal. A certain delay time is necessary so that power up can occur; the circuit may not immediately begin because VDD may not be ready. Once the voltages are ready the system needs to put out a signal to the control logic. The control logic can then enter its sequence and begin to match the impedance.

6.2 Control Sequence

First, the controller receives a signal from the system called ‘TEST’. This signal initiates a finite state machine (FSM) which sequences the appropriate signals. When the sequence is complete, a ‘DONE’ signal is sent to the system. The FSM first powers up the bias strings of the comparator using the ‘TEST’ signal. This signal must be held high until all the comparisons are done. The ‘RESET’ and ‘RESETB’ signals are used to reset the latches and set up initial conditions on the latches. The ‘CNTRLx’ (x = 1,2,⋯6) signal and the ‘CLK’ signal are used to generate the ‘STRBx’ (x = 1,2,⋯6) signal in the one shot circuitry. The ‘SETNx’ (x = 1,2,3) and ‘SETPx’ (x = 4,5,6) signals set the
latches to the appropriate state at the appropriate time (as seen in Figure 15 on page 42). The ‘INPUT’ signal and the ‘ENABLE’ signal provide the output stage and the load with the test waveform.

The CNTRLx signals are used to sequence through the pass gates between the output of the comparator (OUTI) and the input nodes of the latches (NINV1). The CLK signal allows the oneshot to produce the STRBx timings needed for these pass gates. The SETNx and SETPx signals are needed to set a particular finger on just prior to the comparison of the output voltage with the reference voltage. The successive approximation scheme requires that a finger be turned on, the voltage measured and the latch determines whether determines whether the finger should stay on, or be turned off. This sequence of events that will make this impedance matching scheme work.

6.3 Required Timings

The required timings sequence of timings are shown in Figure 15 on page 42. The signals which generate the test waveforms are the data input (‘INPUT’) and the enable (‘ENABLE’) signals. Without these signals, there would be no output voltage to compare with the reference voltage. The next most important signals are the TEST and CLK signals. The TEST signal allows the bias string to become active. After the matching is complete, this signal turns off the biasing of the comparator and there is no further power consumption from the bias circuitry. The CLK signal needs to be timed properly such that the STRBx signals arrive at their destinations (the pass gates) cleanly and quickly. The CNTRLx, SETNx and SETPx signals just determine which latch is being used. This sequencing through all six fingers allows the six latches to be set and the impedance matching scheme to work.
Figure 15. Control circuitry critical timing
6.4 Critical Timings

Critical timings are generated on chip with the one shot circuitry such that there are only a few timing considerations. The STRBx signal is generated by a oneshot because this signal is the only critical timing. All other timings are not as critical. The STRBx signal must come when the comparator output (OUT1) has reached its valid level. The total delay between the output of the driver voltage (hitting the plateau) and the OUT1 node (reaching a valid level) is two nanoseconds or less under nominal process conditions. The STRBx signal should be turning on the pass gate two nanoseconds after the plateau at the driver output. This timing is critical because the pass gate determines the setting time of the latch. However, the start of this pass gate timing is not as critical as the end. The latch will set to whatever binary value corresponds to the voltage last seen by the node NINV1. The STRBx signal can not be too long or the latches will set incorrectly. The OUT1 signal may change polarity due to the reflections of the capacitive load. The length of the STRBx signal is controlled by the size of the slow inverter in the oneshot. The starting time for this signal is controlled by the CLK signal. As long as the other timings' relative relationships remain remain the same (i.e. CNTRLA is before CNTRLB but after CNTRLC), the timing should be simple. For the relative relationships, please see Figure 15 on page 42.

6.5 Restrictions

There are some restrictions to be placed on the use of this circuit because of the impedance matching scheme used in this design. The transmission line length is critical to the operation of the impedance matching scheme because this length allows the plateau in the driver output voltage to be seen. When the transmission line is too short, the net looks like a lumped load and the voltage transitions smoothly from one level to the other without any plateau. If there is no plateau, the comparison between the output voltage and the reference voltage is useless. Also, if the plateau is too short then the comparator will not be able to respond properly thereby causing the scheme to break down.
The series termination used in this driver may not be ideal for clock signal transmission. For the smoothest clock signals, a parallel termination should be used. The one problem with the series termination is the step in voltage at the near end. Depending on how close the receiver is to the near end of the line, this step may be visible at the receiver. Clock signals need to be monotonic in the transition band. However, from the simulation of the network, monotonicity is not a problem. The load is far enough away to allow a monotonic transition of any signal at the receiver.

There are some signals that should not be activated at all before the power up cycle is complete. These signals are those that activate the memory modules. The matching of the driver should take place after on chip power sources stabilize and just before the initialization procedure occurs. In particular, the RAS signal is one that activates the memory modules. Certain sequences of transitions could put the module into an unwanted test mode, a refresh cycle or a read/write cycle. The RAS lines may be activated as long as the data is assumed invalid, the write enable and output enable are disabled, and no other lines are being matched simultaneously.

The restrictions on the use of this driver as a RAS line driver are that certain other signals must be held inactive while the RAS lines are active. By first matching the RAS line’s impedance, then the rest of the impedances, this restriction is not difficult to deal with. The controller is responsible for the sequencing of the fingers, the sequencing of the matching of different lines, and the power down of the feedback circuitry.
7. Results

7.1 Characterizing Drivers

There are several characteristics that can be emphasized in driver design. In order to compare drivers, the design emphasis of a particular driver must be analyzed. Otherwise, the comparison is meaningless. Care must be taken when comparing driver performance since underlying design criteria (di/dt, dv/dt) often set the performance. Thus, caution must be used when comparing drivers and especially when stating generalizations about the drivers.

Inherently, this driver design is quite different from other designs. This design will adjust its output impedance through the feedback circuitry to try to match the load. The emphasis in this design is the output impedance and the delay. Di/dt, dv/dt, noise and simultaneous switching are secondary.

When using the typical method of measuring di/dt and dv/dt, this design should have a much larger spread because, effectively, it is more than just one driver. It is a 32 ohm driver and a 100 ohm driver all in one so, the only fair way to compare di/dt and dv/dt is to set the impedance of this driver and compare to another driver of this same impedance.

The voltage swing on the drivers must be the same too. Many drivers are designed in "CMOS technology with TTL interface specifications". The output voltage on such drivers does not reach 5 volts. These drivers are not a fair comparison since the output voltage swings are not equal.
7.2 Driving High Capacitance Nets

Purely capacitive nets do not present a problem. The driver will select the lowest impedance, resulting in an RC time delay and an exponential waveform. However, adding transmission lines to the net makes the waveforms more complex due to the reflections that occur. The impedance matching driver will adjust to the load by changing the output impedance to match this transmission line load. If the load from line to line varies (even from lumped load to transmission line load), the impedance matching scheme is very important to the driver. Although the design does not eliminate the problems caused by multiple reflections, it does improve overall performance.

Given the freedom to change the impedance of the transmission lines by making them wider the response improves too. Reducing the mismatch between the heavily loaded transmission line and the lightly loaded transmission line allows reflective peaks to be minimized. However, the driver design can only dampen out the multiple reflections and determine which nets look like transmission lines (or lumped loads). The driver dampens out the multiple reflections by allowing its output impedance to be set by the feedback circuitry. The driver determines which loads are transmission lines by the speed with which it drives the load. The speed is controlled by the sizing of the predriver stage.

Transmission lines- when short- allow the reflections to return to the input before the input transition is complete. Such transmission lines normally look like lumped capacitive loads, and are normally driven using a low impedance driver. When the rise time is less than twice the one way delay time, the nets behave as transmission lines. Setting the rise time such that the stubs look capacitive is important. Otherwise, the timing and measurement necessary in the feedback scheme would not work properly. Therefore, the speed of the driver is decreased to allow the stubs to look capacitive and to simplify the model.
7.3 Actual Net and Simplification

Simplification of the net is not necessary to simulate with the Advanced Statistical Analysis Program (ASTAP), but it is useful in understanding what is happening. As seen in Figure 6 on page 21, there are many small stubs of transmission lines in the net. These stubs are too short to be considered transmission lines. The reflections from the far end arrive before the input transition is complete. Therefore, the driver is driving a large lumped load and a transmission line as shown in Figure 16 on page 48.

In this case, the driver chooses (through the feedback scheme) the lowest impedance configuration. The small impedance lets the lumped load be driven without too much delay. With the processor to memory, a 57 ohm driver is chosen because the transmission line impedance is originally about 75 ohms but loaded with significant capacitance. This load reduces the impedance seen by the driver. These simplifications of lumped loads and different characteristic impedances make the network easier to understand.

7.4 Results

The results of the simulations of the impedance matching driver show that the driver improves the performance of the overall system. Comparing the impedance matching driver at 80 ohms impedance to a typical 5 volt, 80 ohm CMOS impedance driver shows that the matching driver has very similar characteristics. The delay time and the rise and fall times are very comparable as seen in Figure 18 on page 50. However, for the particular load being tested, the matching driver would settle to an impedance of 57 ohms rather than 80 ohms. The 57 ohm impedance seems to match the transmission line better and improve the delay time needed to drive this load network.

This impedance matching driver measures the impedance of the line and matches to that impedance so that the voltage transition at the far end of the line is quicker, smoother, and better matched. As shown in Figure 19 on page 51, the overshoot and ringing are slightly larger but the delay time is smaller. This figure shows the drivers connected to the processor end of the network. Here, the
Figure 16. Simplified model of the net (Memory to processor). Modeling the short stubs as one large lumped load.

distributed capacitance reduces a 75 ohm line to a 57 ohm line. However, when the drivers are connected to the other end of the line, the memory end of the network, the impedance matching driver chooses the lowest impedance driver. The heavily loaded output node of the driver causes the entire load to look like a large lumped capacitive load. Therefore, the lowest impedance driver is ideal to keep the delay small and to try to match the impedance. This impedance matching driver's lowest output impedance is not quite low enough to match this line exactly but the response of this driver compared to a traditional 80 ohm driver is significantly better, as seen in Figure 20 on page 52.
Figure 17. Simplified model of the net (Processor to memory). Modeling the short stubs as one large lumped load.

The impedance matching driver is better than a driver used in memory card subsystem configurations. The matching driver allows the signal transmission from the driver to the load to be much smoother and faster. The driver's variable output impedance lets the matching be better in system configurations such as those with plug in board. Previously, drivers used in the systems with pluggable boards needed to drive a light load in best case conditions and a hefty load in worst case conditions. Satisfying these two conditions means choosing a driver which is mediocre at both of these extremes.

With this new driver performance is improved, as shown in Figure 21 on page 53. The network used in this simulation consists of transmission line stubs and capacitors as loads on the main transmission line connecting the loads to each other. The network with eight loads should use a lower impedance
Figure 18. Driver output comparison at 80 ohm load. Two drivers with impedances set to 80 ohms. Looking at the far end waveform.

driver than the network with four loads due to the additional capacitance contributed by the four extra loads.

The impedance matching driver must be characterized by the traditional means also. In the traditional sense, drivers are characterized by the di/dt, dv/dt, delay and amount of current output. A test circuit with 3 inductors and 3 capacitors is used to compare this driver with other already established drivers. Comparing di/dt, dv/dt and current in the matching driver and the established driver is only fair if the impedances are the same so the impedance of the matching driver is set to about 80 ohms. The current outputs of the drivers are comparable and very close given the same impedance. Di/dt
Compare drivers both at HD input
Matching driver (1) vs. 80 Ohm driver (3) vs. 40 Ohm driver (4)

Figure 19. Driver output comparison (driving at processor input end). Two drivers driving processor end of network. Looking at far end waveforms.

and dv/dt of the entire driver, however, will be much more variable since there is an impedance range on the matching driver. Comparing di/dt and dv/dt over the whole driver, the matching driver should have a larger variation. However, di/dt and dv/dt are only 2 characteristics of a driver. The impedance matching benefits seen in performance are much more important than the noise seen on the lines. If the delay decreases, the system can be run faster and the overall performance will improve. The drivers may need to be staggered to prevent the simultaneous switching restriction from becoming a problem. However, for a particular impedance, the di/dt and dv/dt should be very comparable to another driver of the same impedance. (See page 54 for table.)
Figure 20. Driver output comparison (driving at memory input end). Two drivers driving memory end of network. Looking at both far and near end waveforms.

The matching driver can provide significant performance improvement over a typical driver in certain configurations. Given that the impedance of the load changes such as in pluggable memory systems the driver will improve the performance. The overshoots and undershoots in lightly loaded nets should be reduced; the time delay in lightly loaded nets should be more comparable to the time delay in heavily loaded nets and the overall performance will be significantly better.
Figure 21. Driver output comparison (four vs. eight loads). Drivers with four module loads or eight module loads.

7.5 Restrictions

This driver is set up so that the impedance of the line is measured and the output impedance is set as close to this value as possible. In certain cases, however, this driver will not be optimal. When process conditions vary, the impedances will shift significantly high or low (BC or WC). A large range of impedances is needed to allow the driver to match typical transmission lines as the process conditions vary. Also, increasing the number of bits would decrease the spread between resistances and allow better matches. Since there are only 3 bits, the sizes are chosen so that the impedances
Table 2. Driver characterization

<table>
<thead>
<tr>
<th>Driver</th>
<th>( \frac{\text{di}}{\text{dt}} ) (GND) (mA/ns)</th>
<th>( \frac{\text{di}}{\text{dt}} ) (VDD) (mA/ns)</th>
<th>( \frac{\text{dv}}{\text{dt}} ) (V/ns)</th>
<th>current (mA)</th>
<th>rising delay (ns)</th>
<th>falling delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 Ohm Matching</td>
<td>9</td>
<td>21.5</td>
<td>0.7</td>
<td>29.2</td>
<td>2.19</td>
<td>3.84</td>
</tr>
<tr>
<td>80 Ohm Matching</td>
<td>10</td>
<td>22.5</td>
<td>0.8</td>
<td>33.6</td>
<td>2.2</td>
<td>3.71</td>
</tr>
<tr>
<td>32 Ohm Matching</td>
<td>27</td>
<td>34.5</td>
<td>1.35</td>
<td>49</td>
<td>2.20</td>
<td>2.98</td>
</tr>
<tr>
<td>80 Ohm Fixed</td>
<td>23</td>
<td>17.2</td>
<td>0.6</td>
<td>30.6</td>
<td>1.8</td>
<td>1.31</td>
</tr>
</tbody>
</table>

range from 25 to 100 ohms (nominal process) with a fairly linear breakdown. However, lower impedance mismatches will show up more because the impedance mismatch is more significant. Therefore, with the device size ratios as they are, the mismatch on the lower impedance loads may be larger than the mismatch on the higher impedance loads.

A major restriction on this driver is the length of the transmission lines. Short stubs are allowed only to the point where they look like lumped loads. If they begin to look like transmission lines, it will cause the timing of the feedback to be off. Long transmission lines (with one way delays of 1 ns or more) are perfect for this driver (the longer, the better) because the plateau that the comparator is trying to measure needs to be present for at least 2 ns to allow the latches and comparator to react to the voltage level.
Using this driver as a RAS line driver (or any signal driver where the activation of the line during power up is restricted) is restricted. The restriction stems from the fact that during power up and after Vcc stabilizes RAS must be greater than the least positive up level (LPUL). Initialization cycles are required but they must be RAS only or column address select (CAS) before RAS refresh. However, transitioning the RAS lines low (i.e. active) with CAS inactive and output enable inactive should not cause damage to the array nor enter the module into some obscure test mode.

Minimizing the RAS active time may allow this driver to drive the RAS lines. Minimum RAS time is a restriction to obtain valid data only. Since valid data is of no concern during this time, allowing RAS line test pulses to occur may have no harmful effect on the memory modules.

7.6 Building Restrictions

Besides the restrictions above, there are some minor changes or improvements necessary before this circuit can be built reliably. First of all, the area constraint must be considered. Since all of this circuitry may not fit into one I/O cell area, some things will have to change. Slowing down the circuit will allow smaller device sizes (and decrease noise). Secondly, a second gain stage after the inverter of the comparator may be necessary to assure valid voltage levels. Thirdly, when the line lengths are longer, the plateau remains longer and allows more time for the latches to set. When another gain stage is added, the plateau must remain longer; thus, the minimum transmission line length must be increased. The process must also be controlled. Since MOS transistors are used as resistors, any process variation will shift the resistance values and make the output impedance less predictable. Since a feedback circuit controls the matching, the designer does not need to know the exact output impedance. Also, the range of resistance values may need to be decreased; this will allow a finer spread in resistances, more accurate matching and in some cases, a reduction in area. These restrictions are minor and the usefulness of this circuit design has been shown. The concept of the impedance matching circuit has been shown to improve performance by matching to the transmission line load. It is important to consider this driver in designing memory subsystems for optimal performance.
8. Conclusions

8.1 Summary

The goal of this project is to design a driver with better characteristics, specific to the network of receivers as the load. The driver may be used in a system which can be configured with, for example, between two and ten memory cards with significantly less performance loss than would be seen when a driver with fixed output impedance is used. In addition, the average overshoots/undershoots seen with this driver will be less. This driver design matches the output impedance of the driver to the transmission line impedance of the line.

The impedance matching driver is advantageous in configurable systems because the impedance of the load varies greatly from configuration to configuration. This design improves the noise, overshoot and undershoot problems by matching the load.

Driving transmission line loads and large capacitive loads require special characteristics. High speeds result in every load looking like a transmission line stub causing many unnecessary reflections. Slowing the driver down allows the shorter stubs to look like lumped capacitors, and therefore reduce the reflections. The largest reflections are caused by mismatches in the transmission line impedances. Mismatches within the transmission lines can not be reduced by a driver design. Such mismatches must be reduced by changing the impedance of the wiring by widening the line. The width of the wiring in the capacitively loaded transmission line should be minimum width; the width of the wiring in the unloaded line should be larger than minimum width to decrease the impedance. Thus, the gap between the two impedances will decrease.
Mismatches between the driver and the transmission line load occur because of the capacitive loading and the wiring changes made to decrease other mismatches in the line. An impedance matching driver adjusts the output impedance to match the load impedance. Thus, as the load changes the driver will change too and the performance of the overall system will improve. Other drivers do not have the option of changing the output impedance so the lowest impedance driver is chosen for the design (to fit the worst case conditions). This driver must also drive the best case conditions which can be drastically different. Allowing the driver to match the output impedances is equivalent to selecting a different driver for each configuration without physically having to replace the driver in the system.

The impedance matching driver is a self adjusting driver with good characteristics when compared to an equivalent impedance driver. The major advantage is that this driver design selects the appropriate output impedance for the load. Although some restrictions apply, this driver allows the performance of the system to be optimal to the particular configuration.

8.2 Future Designs and Suggestions

Improvements on this driver design should begin with the speed of the feedback network. Allowing the driver to match dynamically could be advantageous for loads that change during the "ON" cycle of the system. Also, the design needs several improvements. The gain of the feedback system should be larger, the sizes of the devices should be reduced and the overall reliability of the design as process parameters change should be investigated. The design proves a concept: impedance matching drivers are advantageous to configurable systems by improving the overall performance. Any performance improvement in signal transmission is helpful in speeding up cycle times of computer systems thereby increasing the overall speed of computer systems.
8.3 Concluding Remarks

The impedance matching driver is designed to drive moderate capacitance and transmission line loads comprised of a network of receivers typical in memory subsystems. The impedance matching driver consists of the driver and a feedback scheme. The main advantage is that the output impedance is set to match the load impedance through a feedback scheme. This feedback scheme uses a successive approximation technique to match the impedance during the power up phase of the system. The feedback includes a voltage comparator, comparing the output voltage to half the voltage swing, several latches to remember the output impedance necessary, a pulse generation circuit to generate the critical timings and some bias circuitry to assure operation of the circuitry. The driver stage consists of an output stage used to set the output impedance and a predriver stage used to produce the three state capabilities of the driver and to control the switching speed of the output stage. The impedance matching circuitry and the driver circuitry interact to improve the performance of the overall system.
References


