NOISE MEASUREMENT TO 40PPM
USING DIGITAL SIGNAL PROCESSING
BY
LENNY SHEET

SUBMITTED TO THE DEPARTMENT OF
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JANUARY, 1990

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Submitted to the Department of Electrical Engineering
in partial fulfillment of the
requirements for the Degrees of Master and Bachelor
of Science in Electrical Engineering
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ABSTRACT

A system for measuring the difference of the power spectrum between two high level white noise signals is designed and partially implemented. Measurement of the difference is done to a precision of 40PPM using digital signal processing techniques. A stable system (small drift in time) using spectrum estimation is designed. The system contains an analog filter, an attenuator, an A/D converter, and a digital filter. The drift in time of the above components of the system is measured. Using these data, the stability of the system and the precision of the measurements are determined using error analysis. The stability of the system is also determined by measurements of a stable signal source.

Thesis Supervisor: Prof. J. Roberge

Title: Professor of Electrical Engineering
I dedicate this thesis to Maria Shum.
ACKNOWLEDGEMENT

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I. INTRODUCTION

Noise measurement to a precision of 40 parts per million to determine the total power within a certain frequency range serves as a non-destructive method for testing the radiation hardness of voltage reference diodes. Determining the radiation hardness characteristics of these diodes without the need for radiation exposure is an attractive way for pre-screening such devices.

The processing of amplified noise and the detection of the resulting signal have been done using analog techniques [1]. In this project, measurement of noise signals and other signals is performed using digital design techniques. The advantages of digital circuitry (it has greater stability and higher resolution) are attractive in this application.

![Power Spectrum of Noise Signal](Figure 1.1)

The noise power spectrum of the diodes is shown in Figure 1.1. In the low frequency region 1/f noise dominates; in the high frequency region capacitive shunting effect dominates. The mid-frequency region...
has a flat spectrum. A noise signal with a flat spectrum over the entire frequency range is called a white noise. The purpose of this project is to measure the difference of this flat spectrum level between two noise signals.

A spectrum analysis method is employed for the measurement of the total power within a certain region of frequencies of the noise signal (which is white over the frequency region of concern). Given a signal $X(t)$, it can be sampled at a rate $1/T$ to form $x(n)$ as follows:

$$X(t) = X(nT) = x(n) \quad (1.1)$$

The spectrum $S_X(f)$ of a given signal $x(t)$ is defined as follows:

$$S_X(f) = \sum_{n=0}^{N} C_X(n) \exp(-j2\pi fn) \quad (1.2)$$

where $C_X(n) = E[x(n)x(N+n)]$.

In reality $C_X(n)$, the auto-correlation function, must be estimated in order to obtain the spectrum. In this project, spectrum estimation will be done by mean-squaring of the filtered signal. In other words, the signal is first passed through a band-pass filter to select the range of frequencies of concern, which will be from 1 kHz to 30 kHz. The mean square of the resulting signal will be taken. Let $h(n)$ denote the system function of the filter. Then the resulting signal after processing will be
\[ G(f) = \frac{1}{N} \sum_{i=0}^{N} \left[ \sum_{k=0}^{M} h(k)x(i-k) \right]^2 \]  

(1.3)

where \( M \) is the length of the filter (i.e. \( h(n) = 0 \), for \( n>M \)) and \( N \) is the number of samples to be averaged.

The mean and variance of \( G(f) \) can be calculated for a signal \( x(n) \) with \( E[x(n)] = 0 \) and \( \text{Var}[x(n)] = \sigma^2 \). The mean of \( G(f) \) is

\[ E[G(f)] = \sigma^2 \left[ \sum_{n=0}^{M} h^2(n) \right] \]  

(1.4)

and the variance of \( G(f) \) is

\[ \text{Var}[G(f)] = \frac{2\sigma^4}{N} \left[ \sum_{n=0}^{M} h^4(n) \right] \]  

(1.5)

From these relationships, we see that the ratio of the variance of \( G(f) \) to the square of the mean of \( G(f) \) is

\[ \frac{\text{Var}[G(f)]}{E^2[G(f)]} = \frac{2}{N} \left[ \sum_{n=0}^{M} h^4(n) \right] \left[ \sum_{n=0}^{M} h^2(n) \right] \]  

(1.6)

If \( h(n) \) is a rectangular window (i.e. \( h(n)=1 \) for \( 0<n<M \), 0 elsewhere), then we have
We see that the ratio is proportional to $1/N$, which means increasing $N$ decreases this ratio. For our objective of 40PPM accuracy, we want $2/N \leq (40 \times 10^{-6})^2$. The required value is $N \geq 1.29 \times 10^9$.

The problem of measuring a signal to 40PPM precision is reduced to one of measuring the difference of the power spectrum level between two signals to 40PPM precision. In the revised problem, noise errors in the system do not cause problems as long as the errors do not drift more than the specified precision over the time of measurements. Thus, when the statistics of the noise do not vary, the measurement of this difference between signals can be made to a high precision provided this difference is small. Once this difference can be measured to a high precision, a calibrated noise signal can be used to get a high precision measurement of an unknown signal. The spectrum level of the unknown signal is the spectrum level of the calibrated signal plus or minus the difference that has been measured. In this paper, a system for measuring the difference between signals to high precision is described.
II. MEASUREMENT SYSTEM

The measurement system is shown in Figure 2.0.1.

(Figure 2.0.1) Measurement System

The amplified high level signals first pass through the analog band-pass filter which serves to reduce aliasing when the analog signal is converted to a digital signal. The attenuator attenuates the input signals by different amounts so that the outputs of the system can be made equal for varying inputs to the system. The analog-to-digital converter converts analog signals to digital signals for processing. Squaring and averaging of the signal are performed to get the desired results (the spectrum estimations of the signals).

In this way the difference of the spectrum level between two signals can be measured. Even though the precision of measurement of the individual spectrum levels is not 40PPM, the measurement of the difference of the spectrum level between the two signals can achieve this precision. First, the calibrated signal is measured with the attenuator in the mid-range. Then the second signal is measured several times. The goal is to
determine the attenuator setting for the second signal that gives the same output as the calibrated signal. This concept will be further elaborated when discussing the attenuator.
The detailed descriptions of the various elements are included in the following sections.

1. Analog Bandpass Filter

The analog bandpass filter acts as an anti-aliasing filter for the analog-to-digital converter. In order to avoid aliasing, the bandwidth $B$ of the filter must be less than $1/2T$, where $T$ is the sampling period of the analog to digital converter. In addition, this filter serves to reduce $1/f$ noise at low frequencies.

The specifications for the filter are given in figure 2.1.1. The lower passband frequency of 1 kHz is chosen to reduce $1/f$ noise in the low frequency region since the "knee" frequency of the $1/f$ noise is approximately 1 KHz. The upper passband frequency of 30 KHz is chosen so that tolerable amount of aliasing will result given the sampling rate of 67KHz of the analog-to-digital converter. The ripple in the passband will not be a significant source of error in the measurement since we are making a comparison between two signals that have identical (flat) spectrums. Both signals will be affected in the same way by the ripple. Figure 2.1.2 gives a plot of the desired filter on the HP 3562A Spectrum Analyzer.
A Chebyshev filter is used for the implementation. The magnitude of the frequency response of Chebyshev filters has an equiripple behavior, in either the passband or the stopband, and the ripple is such that the maximum error in the band where the ripple occurs is minimized. The response in the band free of ripples is monotonic. Here, the design of a Chebyshev filter where the passband contains ripples is used.

A lowpass filter is designed first. The system function for the Chebyshev low pass filter is

\[ |H_a(\omega)|^2 = 1 / [1 + \epsilon^2 v_n^2(\omega/\omega_p)] \]  

(2.1.3)

where \( \omega = 2\pi f \), \( \omega_p \) is the pass band frequency of the low pass filter, \( \epsilon \) is the ripple factor, and \( v_n(x) = \cos(n \cos^{-1}x) \). When \( x > 1 \), we have \( v_n(x) = \cosh(n \cosh^{-1}x) \). Substituting \( S = j\omega \) in equation 2.1.3, we have...
Figure 2.1.2

Plot of Anti-Alias Filter

Chebyshev Filter, 1 kHz to 30 kHz passband
\[
H_a(s)H_a(-s) = 1 / \left[ 1 + \epsilon^2 v_n^2(s/j\Omega_p) \right]
\]  

(2.1.4)

\(V_n(x)\) can be expressed as a polynomial of order \(n\) in \(x\). Therefore,

\[
V_n(x) = \sum_{i=0}^{n} a_i x^i.
\]

(2.1.5)

The values of \(a_i\) for \(n = 1, 2, \ldots, 10\) are given in Table 2.1.1.

**Table 2.1.1 Coefficients for Chebyshev Polynomials \(V_n(0)\) of order \(n\), in ascending powers of variable \(x\)**

<table>
<thead>
<tr>
<th>(n)</th>
<th>Coefficients of (V_n(x)) in ascending powers of (x): (t_{ij}) is the element in the (i^{th}) row, (i = 1, 2, 3, \ldots) and ((j+1)^{th}) column, (j = 0, 1, 2, \ldots)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0, 1</td>
</tr>
<tr>
<td>2</td>
<td>-1, 0, 2</td>
</tr>
<tr>
<td>3</td>
<td>0, -3, 0, 4</td>
</tr>
<tr>
<td>4</td>
<td>1, 0, -8, 0, 8</td>
</tr>
<tr>
<td>5</td>
<td>0, 5, 0, -20, 0, 16</td>
</tr>
<tr>
<td>6</td>
<td>-1, 0, 18, 0, -48, 0, 32</td>
</tr>
<tr>
<td>7</td>
<td>0, -7, 0, 56, 0, -112, 0, 64</td>
</tr>
<tr>
<td>8</td>
<td>1, 0, -32, 0, 160, 0, -256, 0, 128</td>
</tr>
<tr>
<td>9</td>
<td>0, 9, 0, -120, 0, 432, 0, -576, 0, 256</td>
</tr>
<tr>
<td>10</td>
<td>-1, 0, 50, 0, -400, 0, 1120, 0, -1280, 0, 512</td>
</tr>
</tbody>
</table>

The sequence of polynomials \((V_n(x))\) satisfies the following properties:
a) \((V_n(x))\) forms an orthogonal set over \(-1 \leq x \leq 1\); it is verifiable that

\[
\int_{-1}^{1} \frac{1}{\sqrt{1-x^2}} V_n(x)V_m(x)dx = \begin{cases} 
0, & m \neq n, \\
\pi/2, & m-n=0, \\
\pi, & m-n \neq 0.
\end{cases}
\]

b) \(V_n(x) = -V_n(-x)\), for odd \(n\),
\(V_n(x) = V_n(-x)\), for even \(n\).

c) \(V_n(1) = 1\), for all \(n\).

d) \(V_n(-1) = 1\) and \(V_n(0) = (-1)^{n/2}\), for even \(n\),
\(V_n(-1) = -1\) and \(V_n(0) = 0\), for odd \(n\).

e) The range of \(V_n(x)\) is between \(-1\) and \(1\), for \(-1 \leq x \leq 1\), and within this range \(V_n(x)\) varies with an equal ripple as \(x\) varies.

f) The zeros of \(V_n(x)\) lie in \(-1 \leq x \leq 1\).

Figure 2.1.3 defines the lowpass Chebychev filter.
Frequencies \( \Omega_p \) and \( \Omega_s \) are to be determined by the transformation from a bandpass filter to a lowpass filter. The following transformation for the conversion is used.

\[
\frac{\Omega}{\sqrt[4]{\frac{\Omega_L \Omega_H}{\Omega}}} = \frac{\sqrt{\Omega_H}}{\sqrt{\Omega_L}} - \frac{\sqrt{\Omega_L}}{\sqrt{\Omega_H}} \quad (2.1.6)
\]

Using \( \Omega_L = 2\pi \times 10^3 \text{ rad/s} \) and \( \Omega_H = 6\pi \times 10^4 \text{ rad/s} \), we have the new transformed frequencies \( \Omega_0' = -10.34 \text{ rad/s} \), \( \Omega_1' = -1 \text{ rad/s} \), \( \Omega_2' = 1 \text{ rad/s} \), \( \Omega_3' = 2.052 \text{ rad/s} \). Therefore, we have \( \Omega_p = 1 \text{ rad/s} \) and \( \Omega_s = 2.052 \text{ rad/s} \). When the specification at \( \Omega_3' \) is satisfied, the one at \( \Omega_0' \) is also satisfied.

To determine \( \epsilon \), consider \( |H_a(\Omega)|^2 \) at \( \Omega = \Omega_p \). Since \( V_n(1) = 1 \), then at \( \Omega = \Omega_p \), we have \( 10 \log(1+\epsilon^2) = 1 \). This implies that \( \epsilon = 0.5088 \). At \( \Omega = \Omega_s \), the specification is \( |H_a(\Omega_s)|^2 \leq (.01)^2 \). This gives \( 1/[1 + \epsilon^2 V_n^2(2.052)] \leq (.01)^2 \), or \( V_n(2.052) \geq 197 \). The minimum value of \( n \) which satisfies this is \( n = 5 \). Therefore, a fifth order Chebyshev filter is required.

The lowpass filter is designed using five second order sections in cascade. The poles of the Chebyshev lowpass filter transfer function is obtained by setting the denominator of the transfer function equal to 0.

\[
1 + \epsilon^2 V_n^2(s/j\Omega_p) = 0. \quad (2.1.7)
\]
Let $s/j\Omega_p = \cos(w) - \cos(u+jv)$, where $w = u+jv$ is another complex variable ($u$ and $v$ are real). Then from the definition of $V_n(x)$,

$$V_n(s/j\Omega_p) = \cos[n \cos^{-1}(s/j\Omega_p)] = \cos(nw) - \cos[n(u+jv)]$$

$$= \cos(nu)\cosh(nv) - j\sin(nu)\sinh(nv). \quad (2.1.8)$$

From equation 2.1.7, $V_n(s/j\Omega_p) = \pm j/\epsilon$. Therefore,

$$\cos(nu)\cosh(nv) - j\sin(nu)\sinh(nv) = \pm j/\epsilon$$

or $\cos(nu)\cosh(nv) - 0$, and $\sin(nu)\sinh(nv) = \pm 1/\epsilon. \quad (2.1.9)$

Since $\cosh(nv) > 0$ for all values of $nv$, it follows that $\cos(nu) = 0$.

This gives $nu = (2r+1)\pi/2$ or $u_r = (2r+1)\pi/2n$. Substituting this into equation 2.1.9 we have $\sinh(nv) = 1/\epsilon$. Solving for $e^V$, this gives

$$e^V = \left[ \frac{1}{\epsilon} + \left(\frac{1}{\epsilon^2} + 1\right)^{1/n} \right]^{1/n} \quad (2.1.10)$$

Since $s_r = j\Omega_p \cos(u_r+jv) = j\Omega_p[\cos(u_r)\cosh(v) - j \sin(u_r)\sinh(v)]$

$$= \Omega_p[\sin(u_r)\sinh(v) + j \cos(u_r)\cosh(v)] \quad (2.1.11)$$

These poles are transformed to form the poles of the band pass filter with the desired passbands using the following frequency transformation.
The bandpass filter is designed using five second-ordered sections (10 poles). Once the lowpass filter poles have been transformed into bandpass filter poles (using equation 2.1.6), each second-ordered section is a bandpass filter with the following system function:

$$H(s) = \frac{T_0 + 2\zeta \omega_0 s}{s^2 + 2\zeta \omega_0 s + \omega_0^2}$$

(2.1.13)

Table 2.1.2 gives the values of $\zeta$, $T_0$, $\omega_0$ and the two poles for each section.

<table>
<thead>
<tr>
<th>section</th>
<th>$\zeta$</th>
<th>$T_0$</th>
<th>$\omega_0$</th>
<th>poles (rad/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>.08416</td>
<td>-22.93</td>
<td>187,371</td>
<td>-1.577E4 ± j 1.867E5</td>
</tr>
<tr>
<td>2</td>
<td>.08416</td>
<td>-22.93</td>
<td>6,321</td>
<td>-5.320E2 ± j 6.299E3</td>
</tr>
<tr>
<td>3</td>
<td>.31355</td>
<td>-3.634</td>
<td>126,763</td>
<td>-3.925E4 ± j 1.204E5</td>
</tr>
<tr>
<td>4</td>
<td>.31355</td>
<td>-3.634</td>
<td>9,343</td>
<td>-2.930E3 ± j 8.872E3</td>
</tr>
<tr>
<td>5</td>
<td>.76637</td>
<td>-.8876</td>
<td>34,413</td>
<td>-2.637E4 ± j 2.211E4</td>
</tr>
</tbody>
</table>

(Table 2.1.2) Parameters for the Analog Filter

Each section is an active filter implemented by using resistors, capacitors, and an operational amplifier. The circuit diagram for a single second order section is given in Figure 2.1.4. The measured values of $R_1$, $R_2$, $R_3$, $R_4$, $C_1$, $C_2$, $C_3$ are given in Table 2.1.3.
(Figure 2.1.4) Circuit Diagram for a Second Order Section

Table 2.1.3 Parameters for the Five Second Order Sections

<table>
<thead>
<tr>
<th>section</th>
<th>$R_1$ (kΩ)</th>
<th>$R_2$ (kΩ)</th>
<th>$R_3$ (kΩ)</th>
<th>$R_4$ (kΩ)</th>
<th>$C_1$</th>
<th>$C_2$</th>
<th>$C_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>5.11</td>
<td>60.4</td>
<td>10</td>
<td>1.18</td>
<td>301pF</td>
<td>301pF</td>
<td>47pF</td>
</tr>
<tr>
<td>2</td>
<td>4.688</td>
<td>52.3</td>
<td>10</td>
<td>1.4</td>
<td>10.1nF</td>
<td>10.1nF</td>
<td>47pF</td>
</tr>
<tr>
<td>3</td>
<td>4.5456</td>
<td>14.0</td>
<td>10</td>
<td>2.89</td>
<td>.983nF</td>
<td>.983nF</td>
<td>47pF</td>
</tr>
<tr>
<td>4</td>
<td>6.0491</td>
<td>19.109</td>
<td>10</td>
<td>2.808</td>
<td>9.91nF</td>
<td>9.91nF</td>
<td>47pF</td>
</tr>
<tr>
<td>5</td>
<td>2.543</td>
<td>3.320</td>
<td>10</td>
<td>1.922</td>
<td>10.0nF</td>
<td>10.0nF</td>
<td>47pF</td>
</tr>
</tbody>
</table>

Figure 2.1.5 gives a plot of the system function of the filter measured on the HP 3562A Spectrum Analyzer.
(Figure 2.1.3) Plot of Actualized Analog Bandpass Filter

\[
\begin{align*}
X &= 60.083 kHz \\
Y_a &= -60.708 \text{ dB}
\end{align*}
\]

\[
Y = -14.17 \quad \Delta Y = 46.5 \text{ dB}
\]

FREQ RESP

-10

10.0

/Div

dB

-90.0

Fxd Y 100

Log Hz

100K

BREADBOARD IMPLEMENTATION OF ANTI-ALIAS FILTER

MEASUREMENT SET-UP (HP 2562A): MEASUREMENT MODE: SWEEP SINE, LOG SWEEP

AVG = 1, FIXED INTEGRATE, SOURCE 100 mV PEAK, CHANNEL 1 x 2 AUTO RANGE UP + DOWN
2. Attenuator

An attenuator is placed in front of the analog to digital converter to measure the difference between noise levels with greater resolution than that of the analog to digital converter (Figure 2.2.1). The method of adding a variable attenuator for higher resolution allows for the comparison of the measurement of a calibrated noise signal with that of the desired signal. Since the difference between these signals will be small, \( \alpha \) can have a small range. Consider, for example, a range for \( \alpha \) of \( 0 < \alpha < 0.025 \). In this case, \( 0.975 < V_o/V_i < 1 \). A multiplying digital-to-analog converter is used in the implementation of the attenuator. If the multiplying digital to analog converter has 12 bits of resolution with 12 bits of accuracy, then the error of \( \pm 1 \) LSB will become an error in \( \alpha \) of \( \pm 0.025/2E+12 = \pm 2E-17.3 \). This value gives 17 bits of resolution in the adjustment of \( V_o/V_i \).

With the attenuator set to its mid-value, a measurement is first made with a necessary \( N \) to achieve the desired accuracy (40ppm), using a calibrated noise source as input signal. Then the desired signal is measured with this measurement being compared to the first measurement to determine whether it is larger or smaller. The attenuator is adjusted so that successive measurements will yield results closer to that of the calibrated signal. Another measurement is made using a larger value of \( N \). A comparison is again made. The process continues until the measurement has the same value as that of the calibrated noise signal. The setting of the attenuator is used to determine the value of the input signal relative to the calibration signal.
(Figure 2.2.1) Implementation of Adjustable Attenuator

The circuit design of the attenuator is shown in Figure 2.2.2. The voltage reference terminal of the digital-to-analog convertor is used as the input. The digital inputs of the digital-to-analog convertor are used as the adjustments for the attenuator. The input attenuated by the multiplying digital-to-analog convertor is subtracted from the original signal. Thus, we have

\[ V_0 = (1 - \alpha) V_i \]  

(2.2.1)

where \( \alpha \) is the multiplying factor of the digital-to-analog convertor.

The value of \( \alpha \) is determined by the digital adjustments. If \( x_0, x_1, \ldots, x_{11} \) are the digital adjustments of the attenuator, then

\[ \alpha = \alpha_0 \sum_{i=0}^{11} x_i 2^i. \]

where \( \alpha_0 \) is the maximum multiplying factor.
The PMI DAC 8221, a 12 bit multiplying digital-to-analog converter is used. The specifications are shown in Appendix I. The analog switches in the D/A converter are controlled by the digital inputs. If the digital input is 0 there is no contribution to the output current; but if the digital input is 1 then there is a contribution to the output. The amount of contribution is based on the position of the analog switch on the resistor ladder network.

Using the Fluke 5200A Programmable AC Calibrator as the input source and the Fluke 8506A Thermal RMS Digital Multimeter as the measurement device, the attenuation of the attenuator is measured for different digital adjustments. A list of the attenuation values vs adjustment settings for inputs of 1V and 2V is given in Appendix II.

Using the measured values given in Appendix II, the values of $a_0$, the maximum value of $a$, is estimated using least square to be $a_0 = 0.02209$. 11 of the 12 bits of the digital-to-analog convertor are used for the adjustment. The precision is $0.02209 / 2^{11} = 1.06 \times 10^{-5}$. 
Figure 2.2.2  System Diagram for Attenuator Using D/A
3. Analog to Digital Converter (A/D)

An analog-to-digital converter is characterized by its resolution ($N$ bits) and its sampling period ($T$). The A/D converter converts an analog signal $X(t)$ to a digital signal $x(n)$. This is done by sampling $X(t)$ at periodic intervals of $T$. Thus,

$$x(n) = X'(nT)$$ (2.3.1)

where $X'(t) = \sum_{n=-\infty}^{\infty} X(t) \delta(t-nT)$

Therefore, in an analog-to-digital conversion, a series of numbers ($x(n)$) is obtained which corresponds to the input signal $X(t)$; each number represents the amplitude of one of the samples forming the signal $X'(t)$. In order to carry out the conversion process satisfactorily, it is necessary to store the analog sample $X'(t)$. The amplitudes of the stored samples are then converted into digital numbers. The amplitude of a stored sample can have an infinite number of values, whereas the digital number can only have discrete values. It is therefore necessary to replace the exact amplitude of the sample by a whole number of quanta, or steps such that the resultant value of the amplitude is as close as possible to that of the actual amplitude. This process is called quantization. Thus, an A/D converter with a resolution of $N$ bits has a potential $\pm 1/2$ LSB error due to finite number of bits.
The conversion process of the analog-to-digital converter that is used is called successive approximation. The basic operation of a successive approximation A/D converter is shown in Figure 2.3.1. The values of the various bits of the binary word representing $V_x$ are determined starting with MSB. Here, $V_x$ is the voltage of $X(t)$ at a certain sampling time. The following expression of $V_x$ is used:

$$V_x = V_{ref} \left[ \frac{b_1}{2} + \frac{b_2}{2^2} + \cdots + \frac{b_n}{2^n} \right]$$  \hspace{1cm} (2.3.2)

where $V_{ref}$ is the voltage set by the reference.

(Figure 2.3.1) Operation of a Successive Approximation A/D

Figure 2.3.2 shows the various possible changes of the voltage $V$ of the D/A converter during a conversion operation for a 3 bit A/D converter.
(Figure 2.3.2) Possible D/A voltages during a conversion of 3 bits A/D

The range of inputs for the analog-to-digital converter is set to be $-5 \text{ volts} \leq V \leq 5 \text{ volts}$. The shifted or offset binary code is used. This code is illustrated in equation 2.3.3.

$$V = \left(\frac{2V_{\text{ref}}}{2^n}\right) \left(a_12^{n-1} + a_22^{n-2} + \ldots + a_{12}\right) - V_{\text{ref}} \quad (2.3.3)$$

The Burr-Brown ADC 80 AG-12 analog-to-digital converter is used in this project. It has a resolution of 12 bits and a sampling period of $T = 15 \mu S$. The circuit diagram for the analog-to-digital converter part of the system is shown in Figure 2.3.3. The specifications for the ADC 80 AG-12 converter is in Appendix III.
**Figure 2.3.3 A** Connections For A/D

- Analog common
- Digital common
- +15V
- -15V

**Figure 2.3.3 B** Connections For inverters

- Analog common
- Digital common
- +15V
### A. Banana

+5V Digital Common Analog Common +15V -15V Ref Out

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>LED's</td>
<td>LED's</td>
<td>gain adjust</td>
<td>gain adjust</td>
<td>gain adjust</td>
<td>gain adjust</td>
</tr>
<tr>
<td>inv1 pin14</td>
<td>inv1 pin7</td>
<td>stage(16)</td>
<td>stage(16)</td>
<td>stage(16)</td>
<td></td>
</tr>
<tr>
<td>inv2 pin14</td>
<td>inv2 pin7</td>
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<td></td>
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<td></td>
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</table>

### B. BNC

<table>
<thead>
<tr>
<th>INPUT</th>
<th>CONVERT</th>
<th>STATUS</th>
<th>SERIAL OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D PIN13</td>
<td>A/D PIN18</td>
<td>A/D PIN22</td>
<td>A/D PIN26</td>
</tr>
</tbody>
</table>

### C. LED's (+5V TO D. COMMON)

<table>
<thead>
<tr>
<th>BIT 1</th>
<th>BIT 2</th>
<th>BIT 3</th>
<th>BIT 4</th>
<th>BIT 5</th>
<th>BIT 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>inv1 pin2</td>
<td>inv1 pin4</td>
<td>inv1 pin6</td>
<td>inv1 pin12</td>
<td>inv1 pin10</td>
<td>inv1 pin8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BIT 7</th>
<th>BIT 8</th>
<th>BIT 9</th>
<th>BIT 10</th>
<th>BIT 11</th>
<th>BIT 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>inv2 pin2</td>
<td>inv2 pin4</td>
<td>inv2 pin6</td>
<td>inv2 pin12</td>
<td>inv2 pin10</td>
<td>inv2 pin8</td>
</tr>
</tbody>
</table>

### D. 37 PIN CANNON CONNECT

- Bits 1-12 to Cannon 8-19
- Status to Cannon 2
- Digital Common to Cannon 31

---

**FIGURE 2.3.3C** List of PANEL FEATURES
4. Digital Bandpass Filter

The digital filter is used to select the range of frequencies over which the measurement is made. The bandwidth, $B$, from 2 kHz to 15 kHz, is stable enough, so that during the period of measurement there is no significant drift. In addition, the gain in the passband does not drift during this measurement time period. The low drift for these parameters of the filter is necessary for consistent measurements at different time periods.

The specifications for the pass band tolerance, stop band tolerance, and transition region tolerance are given in Figure 2.4.1. The stop band tolerance $\delta_1$ is small enough to eliminate the unwanted frequency components of the stopband. The transition bandwidth of 1 KHz for the upper pass band is chosen to give a sharp roll off.

![Diagram of frequency response](image)

<table>
<thead>
<tr>
<th>$f_0$</th>
<th>$f_1$</th>
<th>$f_2$</th>
<th>$f_3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 KHz</td>
<td>2 KHz</td>
<td>15 KHz</td>
<td>16 KHz</td>
</tr>
</tbody>
</table>

$\delta_1 = 0.01$ (40 dB)

(Figure 2.4.1) Specifications for the Digital Filter
An analog low pass filter is designed first. Figure 2.4.2 defines the low pass filter. Again, Equation 2.1.6 is used to determine $\Omega_p$ and $\Omega_s$. Using $f_L = 2$ KHz and $f_H = 15$ KHz, the following values are calculated:

$$\Omega_0' = -2.231 \text{ rad/s} \quad \Omega_1' = -1 \text{ rad/s}$$

$$\Omega_2' = 1 \text{ rad/s} \quad \Omega_3' = 1.087 \text{ rad/s}$$

Therefore, $\Omega_p = 1 \text{ rad/s}$ and $\Omega_s = 1.087 \text{ rad/s}$.

(Figure 2.4.2) Low Pass Filter

First, an analog Chebychev filter is designed. The bilinear transformation is used to transform the analog filter to a digital filter. The bilinear transformation is given in Equation 2.4.2.
Using equation 2.1.3 for the Chebychev filter, the desired filter is designed by calculating the appropriate parameters. At $\Omega = 0$, Equation 2.1.3 becomes

\[
(1 - \delta_2)^2 = 1 / (1+\epsilon^2).
\]

Then $\epsilon = 0.1425$.

At $s = \Omega_s$, the condition is $|H(\Omega)|^2 \leq \delta_1^2$, or $V_n(x_0) \geq (1/\epsilon)^*/(\delta_1^{-2} - 1) = 702$, where $x_0 = \Omega_s/\Omega_p = 1.087$. Therefore, it is required to find the minimum value of $n$ such that $V_n(1.087) \geq 702$. The required value is $n = 20$. Thus the Chebychev filter is of order 20.

The poles of the low pass filter are derived by the use of Equation 2.1.11. Replacing $S_r$ by the expression for $s$ in equation 2.4.2 and solving for $Z$ yields the poles. After some algebraic manipulations, the poles are of the form $Z_r = X_r + jY_r$ with $X_r$ and $Y_r$ given as follows:

\[
X_r = \frac{1 - (\Omega_p T/2)[\sinh^2(\nu) \sin^2(\beta) + \cosh^2(\nu) \cos^2(\beta)]}{[1 - (\Omega_p T/2) \sinh(\nu) \sin(\beta)]^2 + [(\Omega_p T/2) \cosh(\nu) \cos(\beta)]^2}
\]

\[
Y_r = \frac{2(\Omega_p T/2) \cosh(\nu) \cos(\beta)}{[1 - (\Omega_p T/2) \sinh(\nu) \sin(\beta)]^2 + [(\Omega_p T/2) \cosh(\nu) \cos(\beta)]^2}
\]

where $\Omega_p$ is the analog lowpass filter passband frequency ($\Omega_p = 1$), $\beta = (2r+1)\pi/2n$, $T = 0.1$ and $r = 0, 1, \ldots, 2n-1$. In addition,
\[
e^\nu = \left[ \frac{1}{\varepsilon} + \frac{1}{\varepsilon^2 + 1} \right]^{1/n}
\]  

(2.4.5)

Notice that \(X_{2n-1-r} = X_r\) and \(Y_{2n-1-r} = -Y_r\). The zeros of the filter are all located at \(z = -1\). Thus,

\[
H(z) = (z+1)^n \prod_{r=0}^{n-1} \frac{z - z_r}{(1 + z^{-1})^n} \prod_{r=0}^{n-1} \frac{1 - z_r z^{-1}}{z - z_r} 
\]

(2.4.6)

The above expression gives the system function for the low pass digital filter. To transform the lowpass filter to a band pass filter, the following transformation is used \[7\]:

\[
z' = \frac{z^2 - (2ak/k+1) z^{-1} + (k-1/k+1)}{(k-1/k+1) z^2 - (2ak/k+1) z^{-1} + 1} \quad \text{P}(z^{-1})
\]

(2.4.7)

where \(\alpha = \frac{\cos[(\omega_a + \omega_b)/2]}{\cos[(\omega_a - \omega_b)/2]}\), \(k = \cot \left( \frac{\omega_a - \omega_b}{2} \right) \tan \left( \frac{\theta_p}{2} \right)\)

\[
\theta_p = 2 \tan^{-1}(\Omega_p T/2);
\omega_a = \Omega_2 T_1; \quad \Omega_2 = 2 \pi f_2;
\omega_b = \Omega_1 T_1; \quad \Omega_1 = 2 \pi f_1;
T_1 = 1.5 \times 10^{-5}.
\]

Since \(f_1 = 2\) KHz and \(f_2 = 15\) KHz then \(\omega_a = .188\) and \(\omega_b = 1.41\)

Substituting equation 2.4.7 into \(H(Z)\) we have

\[
H(z) = [Q(z^{-1}) - \text{P}(z^{-1})]^n \prod_{r=0}^{n-1} \frac{Q(z^{-1}) + z_r \text{P}(z^{-1})}{Q(z^{-1})} 
\]

(2.4.8)
Solving for the poles and zeros, we have

\[ H(z) = \frac{(1 - z^{-2})^n}{\prod (1 - z_r' z^{-1})} = \frac{\sum a_i z^{-i}}{\sum b_i z^{-i}} \quad (2.4.9) \]

where \( z_r' \)s are solutions to \( Q(z^{-1}) + z_r P(z^{-1}) = 0 \) and \( |z_r'| \leq 1 \). The program `pole.pas` (Appendix IV) calculates the poles \( z_r' = x_r' + j y_r' \). The locations of the poles are shown on Table 2.4.1.

To normalize \( H(z) \) so that in the pass band there is unity gain, the system function is multiplied by a factor \( k \).

\[ H(z) = k \frac{A(z)}{B(z)} \quad (2.4.10) \]

To determine the value of \( k \), \( \omega = 0 \) is substituted in the lowpass filter system function since \( |H(e^{j\omega})|_{\omega=0} = 1 \). The program `amp.pas` (Appendix V) takes the lowpass filter poles to calculate the magnitude of the filter (i.e. the value of \( 1/k \)) at the desired frequency. The result is \( k = 5.784 \times 10^{-10} \).

From the above system function, we have \( H(z) = Y(z)/X(z) \). The system is implemented using second order sections. There are twenty such sections in this digital filter. Therefore, we have

\[ H(z) = k \prod_{r=1}^{20} H_r(z) \quad (2.4.12) \]

with \( H_r(z) = \frac{1 + z^{-2}}{(1 - z_r' z^{-1})(1 - z_r'^* z^{-1})} \)
<table>
<thead>
<tr>
<th>Q</th>
<th>x</th>
<th>y</th>
<th>Im</th>
<th>Re</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.36484200E+01</td>
<td>1.8697000E-01</td>
<td>1.9876400E+00</td>
<td>1.4384700E+00</td>
</tr>
<tr>
<td>3</td>
<td>2.7382000E+00</td>
<td>1.2383200E+00</td>
<td>1.5552300E+00</td>
<td>1.5673200E+00</td>
</tr>
<tr>
<td>4</td>
<td>1.8752000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
<tr>
<td>5</td>
<td>1.6432000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
<tr>
<td>6</td>
<td>1.4122000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
<tr>
<td>7</td>
<td>1.1812000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
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<td>8</td>
<td>9.4982000E+00</td>
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<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
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<td>7.1718000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
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<tr>
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<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
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<tr>
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<td>2.5109000E+00</td>
<td>1.2393200E+00</td>
<td>1.9913200E+00</td>
<td>1.5425000E+00</td>
</tr>
</tbody>
</table>

Tbk

Table 2.4.1

Folds of the Warma-Bend Pass Filter

<table>
<thead>
<tr>
<th>t</th>
<th>5.3434800E+00</th>
<th>5.3434800E+00</th>
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<tbody>
<tr>
<td>1</td>
<td>1.0324800E+00</td>
<td>4.2134800E+00</td>
</tr>
<tr>
<td>2</td>
<td>1.0324800E+00</td>
<td>4.2134800E+00</td>
</tr>
<tr>
<td>3</td>
<td>1.0324800E+00</td>
<td>4.2134800E+00</td>
</tr>
<tr>
<td>4</td>
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<td>4.2134800E+00</td>
</tr>
<tr>
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<td>1.0324800E+00</td>
<td>4.2134800E+00</td>
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<td>6</td>
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<tr>
<td>7</td>
<td>1.0324800E+00</td>
<td>4.2134800E+00</td>
</tr>
</tbody>
</table>

(Continued)
where \( z_r' \) and \( z_r'^* \) are a conjugate pole pair.

The output of the system is then

\[
20 \sum_{r=1}^{20} Y(z) = k \Pi H_r(z) X(z) \tag{2.4.13}
\]

Consider the input passing through one of these second order sections. Then

\[
Y_r(z) = H_r(z)X_r(z) = \frac{1 + z^{-2}}{1 + a_rz^{-1} + b_rz^{-2}} \tag{2.4.14}
\]

with \( a_r = -2\text{Re}(z_r) \) and \( b_r = |z_r|^2 \). Then

\[
y(n) = x(n) + x(n-2) - a_1y(n-1) - a_2y(n-2). \tag{2.4.15}
\]

There are 2 multiplications and 3 additions for each value of \( y(n) \). Considering the entire system, then there are \( 20(2) + 1 = 41 \) multiplications (One for multiplication by \( k \)) and \( 20(3) = 60 \) additions for each value of \( y(n) \). The program coef.pas (Appendix VI) is used to calculate the values of \( a_r \)'s and \( b_r \)'s for \( 1 \leq r \leq 20 \). The values of the coefficients are shown on Table 2.4.2.

The program Filter.pas (Appendix VII) implements the digital filter by taking the outputs of coef.pas to form the 20 second order sections. The data from the A/D converter are convolved with the impulse response of each second order section. Thus we have
<table>
<thead>
<tr>
<th>Term</th>
<th>Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\text{AR} = -2.289 \times 10^{-0}$</td>
</tr>
<tr>
<td>2</td>
<td>$\text{AR} = -1.626 \times 10^{-0}$</td>
</tr>
<tr>
<td>3</td>
<td>$\text{AR} = -1.240 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>4</td>
<td>$\text{AR} = -1.558 \times 2 \times 10^{-0}$</td>
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<td>5</td>
<td>$\text{AR} = -1.584 \times 2 \times 10^{-0}$</td>
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<td>6</td>
<td>$\text{AR} = -1.942 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>7</td>
<td>$\text{AR} = -1.673 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>8</td>
<td>$\text{AR} = -1.928 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>9</td>
<td>$\text{AR} = -1.833 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>10</td>
<td>$\text{AR} = -1.319 \times 2 \times 10^{-0}$</td>
</tr>
<tr>
<td>11</td>
<td>$\text{AR} = -1.935 \times 2 \times 10^{-0}$</td>
</tr>
</tbody>
</table>

Note: The table is a representation of the AR coefficients from a model.
\[ y_1(n) = x(n) \ast h_1(n) \]
\[ y_2(n) = y_1(n) \ast h_2(n) \]
\[ \ldots \]
\[ y_{20}(n) = y_{19}(n) \ast h_{20}(n) \]
\[ y(n) = y_{20}(n) \]

The filtered signal can then be squared and averaged, as described in the next section.
5. Squaring and Averaging

Squaring and averaging are done by the computer. The program Filter.pas also performs the squaring and averaging computations. The output is

\[ S_x = \frac{1}{N} \sum_{i=0}^{N-1} x_i^2 \]  

(2.5.1)

The program Filter.pas uses a recursive averaging method. Thus, if \( S_x(i) \) is the spectrum estimation using \( i \) data points, then the next spectrum estimation, \( S_x(i+1) \), given \( x_{i+1} \) is

\[ S_x(i+1) = \frac{i \times S_x(i) + x_{i+1}^2}{i+1} \]  

(2.5.2)

For every sample point there are 3 multiplications and 1 additions involved in squaring and averaging. Thus for every sample point the total number of multiplications is 44 and the total number of additions is 61.
III SYSTEM ANALYSIS

The operation of the system and the drift error of the system are considered to determine the effectiveness of the system. The block diagram with the system functions of the various components of the system is given in Figure 3.0.1.

(Figure 3.0.1) Block Diagram of System with System Functions
1. Operation of System

Figure 3.0.1 is used to analyze the operation of the system. First, the measurement method is described. The procedures for measurement is as follows:

a. One of the two signals (the calibrated signal) is first measured with the attenuator at the middle adjustment setting (i.e. 100000000000). This setting corresponds to $\alpha = .0110$. The necessary number of sample points is taken to achieve the desired precision ($N = 1.29 \times 10^9$ for 40PPM precision).

b. The second signal is then measured with the first bit of the attenuator set to one (i.e. 100000000000) using $N = 1.29 \times 10^9$. The measurement for this output is compared with the measurement of the output for the calibrated signal. If the second measurement is greater than the first measurement, the first bit is changed back to zero; otherwise the first bit remains one.

c. The second bit is set to one with another measurement taken. The same procedure as in step b is repeated.

d. This procedure is repeated until the first 11 bits of the attenuator setting has been adjusted.
At the end of the measurements, there are two attenuator settings, one for each signal. These two settings can be used to determine the spectrum of the signal relative to the first.

From Figure 3.0.1, the spectral estimation is

\[
S_x(f) = \beta^2 \frac{N}{\sum_{n=0}^{N} \sum_{i} x(i)h(n-i)}^2
\]  

(3.1.1)

with \( x(n) = \int X(\tau)h_a(t-\tau) \, d\tau \bigg|_{t=nT} \)

where \( h_a(t) \) is the analog filter impulse response, \( h(n) \) is the digital filter impulse response, and \( \beta=1-\alpha \) for the attenuator.

For the two signals, we have

\[
S_1'(f) = \beta_1^2 \frac{N}{\sum_{n=0}^{N} \sum_{i} x_1(i)h(n-i)}^2 - \beta_1^2 S_1(f)
\]  

(3.1.2)

\[
S_2'(f) = \beta_2^2 \frac{N}{\sum_{n=0}^{N} \sum_{i} x_2(i)h(n-i)}^2 - \beta_2^2 S_2(f)
\]

where \( S_1(f) \) and \( S_2(f) \) are the actual spectrum levels, and \( S_1'(f) \) and \( S_2'(f) \) are the measured spectrum level. But the attenuator is adjusted so that \( S_1'(f) = S_2'(f) \); call this \( S_x(f) \). After some manipulation, we have

\[
S_2(f) - S_1(f) = S_x(f) \left[ \frac{1}{\beta_2^2} - \frac{1}{\beta_1^2} \right]
\]  

(3.1.3)

or

\[
S_2(f) = \frac{\beta_1^2}{\beta_2^2} S_1(f)
\]
Thus, the difference of the spectrum level between the two signal can be computed. Since $S_1(f)$ is a calibrated signal, with precision of about 40PPM, $S_2(f)$ can be calculated to 40PPM if the necessary number of sample points are taken so that $S_x(f)$ is measured to 40PPM precision. Since for the attenuator, the maximum value of $\alpha, \alpha_0$, is .02209, the difference of the spectral level between the two signals must not exceed -1.1% of either signal.

In the above analysis the error of the system has not been taken into account. A detailed analysis of the error in the system is given as follows.
2. System Drift Error Analysis

In order to analyze the drift error in the system, the drift error of the individual components of the system is analyzed at the various stages of the system. There are several possible sources of drift error including outside noise, error from the analog filter, error from the attenuator, error from the A/D converter, and error from the digital filter. This error analysis will be used to analyze the performance of the system. For each component, the drift error is modelled as an error signal with mean of zero and a variance which characterizes how much drift is associated with that component. At the output of the digital filter the variance of the drift error is compared with the variance of the desired output to evaluate the performance of the system.

a. Outside Noise

All outside noise are taken into account at the input of the analog filter (at the input to the system). Although there are outside noise contributions at different stages of the system, they are dealt with as if coming from the input to the system. However, since the statistics of the outside noise does not change, there is no contribution to the drift error.

b. Analog Band Pass Filter
The analog filter error is modeled as a perturbation in the gain of the actual filter. Thus, the system function of the analog filter is

\[ H_{a_{\text{TOT}}}(s) = k_a[H_a(s)] + k_a'[H_a(s)] \]  

(3.2.1)

where \( k_a = 0.19566 \) from measurements of the analog filter in Appendix X, and \( |[H_a(s)]| = 1. \)

Figure 3.2.1 shows the block diagram.

\[ \text{Figure 3.2.1) Analog Filter with Drift Error Consideration} \]

In the figure, the input signal is a preamplified white noise with a spectrum level of \( W_0. \)

c. Attenuator

The attenuator drift error is modeled as follows:

\[ \beta_{\text{TOT}} = \beta + n_1(t) \]  

(3.2.2)

where \( \beta = 1 - \alpha. \)
Figure 3.2.2 shows the attenuator using this model.

(Figure 3.2.2) Attenuator with Drift Error

\[ Y'(t) \xrightarrow{\beta} Z'(t) \]

\[ n1(t) \]

The A/D converter drift error is modeled in a similar way to the modeling of the attenuator.

\[ z'(t) \rightarrow z'(n) + n2(n) \] \hspace{1cm} (3.2.3)

Figure 3.2.3 shows the A/D converter with the error.

(Figure 3.2.3) A/D Converter with Error
e. Digital Band Pass Filter

Since the digital filter is implemented as an algorithm on the computer, there is no drift error associated with this part of the system.

Figure 3.2.3 shows the block diagram.

(Figure 3.2.3) Digital Filter Block Diagram

Let $b'(n)$ be the output of the digital filter containing the drift error with $b(n)$ as the output without the error and $e(n)$ the error signal. In other words $b'(n) = b(n) + e(n)$.

The ratio \[
\frac{\text{Var}[e(n)]}{\text{Var}[b(n)]}
\] is used to determine the drift of the system.

After manipulation, we have

\[
\epsilon'^2 = \frac{\text{Var}[e(n)]}{\text{Var}[b(n)]} \int h_a'(t)dt \cdot \int h_a(t)dt + \sigma_1^2 + \sigma_2^2 \cdot \int h_a(t)dt \cdot \int h_a^2(t)dt
\]  

\[ (3.2.6) \]
where \( \int h_a(t)^2 \, dt / \int h_a(t)^2 \, dt = k_a^2 / k_a^2 \)

\[ \int h_a(t)^2 \, dt = 1.53 \times 10^3 \]

\( \beta^2 \approx 1 \)

and \( W_0 \) is the spectrum level of the input preamplified white noise signal with a value of \( \approx 1 \) V^2/Hz.

The values of \( k_a^2 / k_a^2 \), \( \sigma_1^2 \), and \( \sigma_2^2 \), the mean square drift errors for the analog filter, the attenuator and the A/D converter, have to be determined.
a. Drift Error (Individual Sections)

To evaluate the drift error, the variance of $e_4$ (equation 3.2.13) is used. However, to evaluate $\epsilon'^2$ the mean square drift for the individual components of the system has to be estimated. The drift error associated with the different parts of the system is evaluated.

1. Analog Filter

The drift of the amplitude of the analog filter in time is tested by providing an input with an rms value of 1 volt. The amplitude of the filter can then be calculated using the measured output. The Fluke 5200A Programmable AC Calibrator provides the 1 volt input to the filter. The output of the filter at several pass band frequencies are measured through a period of time (in this case approximately 2 months). The chosen frequencies are 1 KHz, 2 KHz, 6 KHz, 20 KHz, and 30 KHz. The measured data are shown in Appendix X.

From the data the average drift error can be extracted. For four days the average measured drift are .000248, .000030, .000020, .000050, and .000132 for the respective frequencies mentioned above. These values are used to estimate the average drift for a day in the pass band frequencies. The pass band frequency range is partitioned into five regions. A drift error is allocated to each region. Table 3.2.1 shows the partitioning and the allocation.
Table 3.2.1 Partitioning of Pass Band Frequencies with Appropriate Error Allocation

<table>
<thead>
<tr>
<th>Frequency Range</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>1KHz - 1.5KHz</td>
<td>0.000248</td>
</tr>
<tr>
<td>1.5KHz - 4KHz</td>
<td>0.000030</td>
</tr>
<tr>
<td>4KHz - 13KHz</td>
<td>0.000020</td>
</tr>
<tr>
<td>13KHz - 25KHz</td>
<td>0.000050</td>
</tr>
<tr>
<td>25KHz - 30KHz</td>
<td>0.000132</td>
</tr>
</tbody>
</table>

However, since the digital filter has a passband from 2KHz to 15KHz, only the drift in this passband has to be considered. Thus, the partition becomes

Table 3.2.2 Partitioning of Pass Band Frequencies with Modification by Digital Filter

<table>
<thead>
<tr>
<th>Frequency Range</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>2KHz to 4KHz</td>
<td>0.000030</td>
</tr>
<tr>
<td>4KHz to 13KHz</td>
<td>0.000020</td>
</tr>
<tr>
<td>13KHz to 15KHz</td>
<td>0.000050</td>
</tr>
</tbody>
</table>

The average drift for a day is then calculated.
average drift = $\frac{2(0.000030)+9(0.000020)+2(0.000050)}{13}$

= $2.615 \times 10^{-5}$.

Thus, in the model $(k_a + k_a') [H_a(s)]$, we have $k_a' = 2.615 \times 10^{-5}$. Since $k_a = 0.19566$, then $k_a'/k_a = 1.34 \times 10^{-4}$.

2. Attenuator

The drift in time of the attenuator is measured also using the Fluke 5200A Programmable AC Calibrator as the input and the Fluke 8506A Thermal RMS Digital Multimeter as the measurement device. Measurements are taken over a two week period to determine the amount of drift of the attenuator. The results are shown in Appendix XI. From the data it is seen that the drift over four days is less than $10^{-5} \text{ V}^2$ (worst case error). Thus, $\text{Var}[n_1(t)] = \sigma_1^2 = (10^{-5})^2 \text{ V}^2$.

3. Analog-to-Digital Converter

The drift of the A/D converter is measured by sending an 1V DC input to the A/D converter to measure the corresponding output over a period of several weeks. The Lambda power supply provides the 1V input. The output is read off the LED's. Appendix XII gives the input and output
values over the several weeks of measurements. From the data the drift error is estimated to be approximately $1.59 \times 10^{-3}$ $\nu^2$ in four days.

Therefore, $\text{Var}[n_2(n)]$

$\approx (1.59 \times 10^{-3})^2$. 
b. Drift Error (Entire System)

Using

\[ \frac{k_a'}{k_a^2} = (1.34 \times 10^{-4})^2 \]
\[ \sigma_1^2 = (10^{-5})^2 \]
and \[ \sigma_2^2 = (1.59 \times 10^{-3})^2 \]

for the parameters in equation 3.2.6, the value of \( \epsilon^2 \) is evaluated.

Thus, \( \epsilon^2 = 1.80 \times 10^{-8} + 6.54 \times 10^{-14} + 1.65 \times 10^{-9} \approx 1.97 \times 10^{-8} \),
and \( \epsilon' \approx 1.40 \times 10^{-4} \).

The amount of drift for this system in four days is thus approximately 140PPM. The number of sample points that can be used during this limited time is determined.

To determine the precision achieved through squaring and averaging, equation 2.5.2 is used. This is shown below.

\[
\frac{\text{Var}[S_x]}{E^2[S_x]} = \frac{2}{N} \quad (3.2.7)
\]

The constraint is that the measurements should be taken in four days so the system drift does not exceed 140PPM. Since 12 measurements are needed, one for the calibrated signal and 11 for the unknown signal, 8 hours are used for each measurement. In section 2.4 the number of multiplications and additions that is needed by the digital filter, and squar-
squaring and averaging was determined. For each sample point 101 mathematical operations (multiplications and additions) are required. Using the IBM p.c. that runs at about $10^5$ operations per second, the time needed for 101 operations is $1.01 \times 10^{-3}$ seconds. In addition, the A/D converter samples at $T = 15 \mu S$. The total amount of time needed for each point is thus $1.025 \times 10^{-3}$ seconds. In 8 hours the number of points that can be sampled and computed is $2.81 \times 10^7$. Using equation 3.2.7, then

\[
\frac{\text{Var}[S_x]}{E^2[S_x]} = \frac{2}{N} = 7.12 \times 10^{-8}
\]

This gives an accuracy of $2.67 \times 10^{-4}$. Since this value is greater than the drift error for one day, this error dominates. Thus the accuracy achieved is approximately 267PPM.
IV MEASUREMENT OF AC SIGNAL

The measurements of an AC signal through a period of several weeks are used to determine the drift in time of the measurement system as given in Figure 2.0.1. The Fluke 5200A Programmable AC Calibrator provides the 10V rms signal at 6KHz. The attenuator is set at \(1 - \alpha/2 = 0.98847\). The output of the A/D converter is fed into the P.C. The Metrobyte PDMA-16 card is used to collect the data for the system. The resulting measurement is the rms voltage of the input signal with the appropriate attenuations by the attenuator and the filters. Measurements are taken every seven days to measure the drift of the system.

Table 4.0.1 shows the measurement results. Each trial measurement takes \(N = 10^7\) samples and requires about 3 hours of computation.

<table>
<thead>
<tr>
<th>Date</th>
<th>Measurement (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9/8/89</td>
<td>1.91488</td>
</tr>
<tr>
<td>9/15/89</td>
<td>1.91581</td>
</tr>
<tr>
<td>9/22/89</td>
<td>1.91644</td>
</tr>
<tr>
<td>9/29/89</td>
<td>1.91743</td>
</tr>
<tr>
<td>10/6/89</td>
<td>1.91852</td>
</tr>
</tbody>
</table>
From the above information, the drift of the system in 7 days is \( \approx 10^{-3} \) V. Normalizing the result, we have a drift of \( \approx 5 \times 10^{-4} \) or 500PPM in 7 days.
V RESULTS AND DISCUSSION

The system uses digital signal processing to estimate the spectrum of a preamplified white noise signal. The spectrum of the signal under consideration is compared with that of the calibrated signal. Thus, only the drift of the system in time has to be considered. Since the digital filter and the squaring and averaging is implemented in a computer program, there is no drift error associated with them. The greatest amount of drift error comes from the analog filter. This drift error, from the drift of the passband gain of the analog filter, is reduced by the digital filter since the digital filter has a narrower passband than the analog filter. The total drift error per day of the system is about 40PPM. Furthermore, the processor for the computation limits the precision because the more accurate the result, the more sample point, and thus the more time, is required. A measurement of the difference between the spectrum level of the two signals using this system achieves a precision of 220PPM when a preamplified white noise signal of approximately $1V^2/Hz$ is used.

With a drift of 40PPM in one day, the system can thus achieve a precision of 200PPM using a processor that computes at about $10^5$ operations per second. However, the precision can be improved with processors that compute at faster rates. To achieve the 40PPM precision, a processor that computes at a rate of $5.5 \times 10^6$ operations per second is required since the amount of time used for each sample point is $101 \times (5.5 \times$
$10^6 \gamma^{-1} + 1.5 \times 10^{-5} = 3.35 \times 10^{-5}$ seconds, and the number of sample points in a 12 hour interval is $1.29 \times 10^9$. This gives the 40PPM precision.

A second way to improve the system is to decrease the order of the digital filter. By decreasing the order of the digital filter, less computations are required for each sample point. Thus, if the digital filter were to be decreased to a fifth order filter, the number of computation for each sample point would be decreased by a factor of 4, to about 25 operations. The same processor can accept 4 times as many point for computation in the same duration of time. Then the precision will improve by a factor of two. However, by doing this, the transition region will be wider resulting in more drift in the transition region.

Since most of the drift comes from the analog filter, this part of the system can be improved so the drift error decreases. One way of decreasing the drift is to reduce the order of the filter. By reducing the order of the filter, fewer circuit components are needed. With less components the analog filter drifts less. However, the tradeoff is that the transition region is wider resulting in more aliasing when sampling.

In order to measure the noise signal to 40PPM the signal must not drift more than 40PPM. If the signal drifts more than 40PPM, then the measurement to 40PPM is not a significant value. In that case, the measurement is limited by the drift of the signal.
Even more important, the calibrated noise signal must not drift more than 40PPM since this signal is used as the standard for comparison. In addition, the spectrum level of this calibrated noise signal must be known to 40PPM. Thus, the precision of the measurement depends heavily on the precision of this calibrated signal.

In the progress of doing the thesis project, a certain amount of time was devoted to the debugging of the Pascal programs used to implement the digital filter. Several obstacles were encountered. There were, at first, several logical errors in the programs producing erroneous output calculations. Because the compilation of these programs took much time, a significant amount of time was required to correct these errors. Another task was to create data files for which the programs can insert and retrieve data. The "reset" and "rewrite" commands were used to open the files for the input and output of data respectively. The corresponding commands used to input and output data were "read" and "write" respectively.

In working with the A/D converter there was, at first, problem with grounding. I was not certain how to connect the analog ground and digital ground to assure that the A/D converter operate correctly. Eventually, I found out that the analog ground and the digital ground should be connected to a single point on the board.
Data acquisition of the A/D converter output using the PDMA-16 acquisition board was a task that took a significant amount of time. First, there was the need to write some software so that the acquisition board can collect data at 67 KHz. In addition, since the IBM P.C. does not have enough memory to collect the required amount of data in a single batch, the collection of data was divided into several batches. The computations (filtering, squaring and averaging) took place after each batch.

White noise measurements were not made; only measurements of AC signals were made to test the measurement system for drift error. The components of system are ready to measure white noise. However, the system as a whole requires some interfacing for noise measurement. There may be significant amount of aliasing since the sampling rate of the A/D converter at 67 KHz is very close to the Nyquist rate of 60 KHz. However, since one signal is compared against another, this is not a problem. In addition, there may be some problem with data acquisition. Furthermore, since the acquisition board uses Basic for data acquisition and the digital filter is written in Pascal, there is a need to create compatible data files.
DAC-8221
DUAL 12-BIT BUFFERED MULTIPlying CMOS D/A CONVERTER

PRELIMINARY

A common 12-bit (TTU/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. With WR and CS lines at logic low, the input data latches are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by DAC A/DAC B control input.

PIN CONNECTIONS

FUNCTIONAL DIAGRAM
ABSOLUTE MAXIMUM RATINGS
(TA = +25°C, unless otherwise noted.)

VDD to AGND ............................................. 0V, +17V
VDD to DGND ............................................. 0V, -17V
AGND to DGND ............................................ 0.3V, VOD -0.3V
Digital Input Voltage to DGND ............................ -0.3V, VDD -0.3V
IOUTA, IOUTB to AGND ..................................... -0.3V, VDD -0.3V
VREFA, VREFB to AGND ................................... ±25V
Power Dissipation (Any Package) to +75°C ........... 650mW
Derate Above +75°C by ................................ 6mW/°C

Operating Temperature Range
AW Version ........................................ -55°C to +125°C
EW, FW Versions ........................................ -40°C to +85°C
GP, HP, HPC Versions .................................. 0°C to +70°C

DICE JUNCTION TEMPERATURE
Storage Temperature .................................... -65°C to +125°C
Lead Temperature (Soldering, 60 sec.) ............... +250°C

CAUTION:
1. Do not apply voltages higher than VDD or less than AGND potential except VREF and VOD.
2. Do not exceed TA = -25°C to +125°C for DAC-8221AW; TA = -40°C to +85°C for DAC-8221EW/FW; TA = 0°C to +70°C for DAC-8221AG/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B.
3. Do not insert this device into powered sockets. Remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS at VDD = +5V or +15V, VREFA = VREFB = -10V, VOUTA = VOUTB = 0V; AGND = DGND = 0V; TA = -55°C to +125°C apply for DAC-8221AW; TA = -40°C to +85°C apply for DAC-8221EW/FW; TA = 0°C to +70°C apply for DAC-8221AG/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>DAC-8221</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>N</td>
<td>Specifications apply to both DAC A and DAC B.</td>
<td>12</td>
</tr>
<tr>
<td>Total Integral Nonlinearity</td>
<td>INL</td>
<td>Endpoint Linearity Error</td>
<td>DAC-8221A/E/G</td>
</tr>
<tr>
<td>Differential Nonlinearity</td>
<td>DNL</td>
<td>All Grades are Monotonic</td>
<td>DAC-8221A/E/G</td>
</tr>
<tr>
<td>Full Scale Gain Error (Note 1)</td>
<td>GFSE</td>
<td>T_A = -25°C</td>
<td>DAC-8221A/E/G</td>
</tr>
<tr>
<td>Gain Temperature Coefficient</td>
<td>TCGFS</td>
<td>(Notes 2, 7)</td>
<td>DAC-8221A/E/G</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>ILEAK</td>
<td>All Digital Inputs: 0000 0000 0000</td>
<td>T_A = -25°C</td>
</tr>
<tr>
<td>Input Resistance (VREFA, VREFB)</td>
<td>RIN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(Input Resistance Match)</td>
<td>∆VREFA - B</td>
<td>VREFA = VREFB</td>
<td>VREFA = VREFB</td>
</tr>
</tbody>
</table>

DIGITAL INPUTS

<table>
<thead>
<tr>
<th>DIGITAL INPUTS</th>
<th>SYMBOL</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Input High</td>
<td>VINH</td>
<td>VDD = ±5V</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD = ±15V</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Digital Input Low</td>
<td>VIL</td>
<td>VDD = ±5V</td>
<td>-</td>
<td>1.3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDD = ±15V</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
</tr>
<tr>
<td>Input Current</td>
<td>IIN</td>
<td>VIN = 0V or VDD</td>
<td>T_A = -25°C</td>
<td>T_A = Full Temp Range</td>
<td>±0.001</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIN = VINH</td>
<td>±10</td>
<td>±10</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>CIN</td>
<td>DBO—DO11</td>
<td>WR, CS, DAC A/DAC B</td>
<td>-</td>
<td>- 10</td>
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<tr>
<td>(Note 2)</td>
<td></td>
<td>WR, CS, DAC A/DAC B</td>
<td>-</td>
<td>15</td>
<td>-</td>
</tr>
</tbody>
</table>

PRELIMINARY
CRTICAL CHARACTERISTICS at \( V_{DD} = +5V \) or +15V. \( V_{REF} = V_{REF} = +10V, V_{OUT} = V_{OUT} = 0V. \) AGND = DGND = 0V; -5°C to +125°C apply for DAC-8221AW; \( T_A = -40^\circ C \) to +85°C apply for DAC-8221EW/FW; \( T_A = 0^\circ C \) to +70°C apply for DAC-821GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DD} )</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>mA</td>
</tr>
</tbody>
</table>

PERFORMANCE CHARACTERISTICS

- **Power Supply Currents**
  - \( I_{DD} \): All Digital Inputs \( V_{IN} \) or \( V_{IN} \)
  - \( I_{PSR} \): All Digital Inputs \( 0V \) or \( V_{DD} \)

- **PSRR**: \( jV_{PSR} = -5\% \)

- **Setting Time**
  - For DACs \( T_A = +25^\circ C \)

- **Capacitance**
  - \( C_{OUTA} \): DAC Latches Loaded
  - \( C_{OUTB} \): DAC Latches Loaded
  - \( C_{OUTA} \): with \( 00000000000 \)
  - \( C_{OUTB} \): with \( 11111111111 \)
  - \( C_{OUTA} \): \( 90 \) pF
  - \( C_{OUTB} \): \( 90 \) pF

- **Gain (A)\( \times 12 \)**

- **Analog Characteristics**
  - \( V_{DD} = +5V \)
  - \( V_{DD} = +15V \)
  - \( -40^\circ C \) to \( +85^\circ C \)
  - \( -55^\circ C \) to \( +125^\circ C \)

<table>
<thead>
<tr>
<th>( V_{DD} = +5V )</th>
<th>( V_{DD} = +15V )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( -25^\circ C )</td>
<td>( -25^\circ C )</td>
</tr>
<tr>
<td>( -55^\circ C )</td>
<td>( +125^\circ C )</td>
</tr>
</tbody>
</table>

- **Gain (A)\( \times 12 \)**
  - \( I_{CS} \): DAC Digital Inputs \( 0V \)
  - \( I_{CH} \): DAC Digital Inputs \( +5V \)
  - \( I_{AS} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
  - \( T_A = +25^\circ C \)
  - \( T_A = +70^\circ C \)

<table>
<thead>
<tr>
<th>( T_A = +25^\circ C )</th>
<th>( T_A = +70^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
</tbody>
</table>

- **Analog Characteristics**
  - \( I_{DB} \): DAC Digital Inputs \( 0V \)
  - \( I_{DS} \): DAC Digital Inputs \( +5V \)
  - \( I_{DN} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
  - \( T_A = +25^\circ C \)
  - \( T_A = +70^\circ C \)

<table>
<thead>
<tr>
<th>( T_A = +25^\circ C )</th>
<th>( T_A = +70^\circ C )</th>
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<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
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</tbody>
</table>

- **Analog Characteristics**
  - \( I_{DB} \): DAC Digital Inputs \( 0V \)
  - \( I_{DS} \): DAC Digital Inputs \( +5V \)
  - \( I_{DN} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
  - \( T_A = +25^\circ C \)
  - \( T_A = +70^\circ C \)

<table>
<thead>
<tr>
<th>( T_A = +25^\circ C )</th>
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<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
</tbody>
</table>

- **Gain (A)\( \times 12 \)**
  - \( I_{DB} \): DAC Digital Inputs \( 0V \)
  - \( I_{DS} \): DAC Digital Inputs \( +5V \)
  - \( I_{DN} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
  - \( T_A = +25^\circ C \)
  - \( T_A = +70^\circ C \)

<table>
<thead>
<tr>
<th>( T_A = +25^\circ C )</th>
<th>( T_A = +70^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
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<td>( 0.1 )</td>
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</table>

- **Analog Characteristics**
  - \( I_{DB} \): DAC Digital Inputs \( 0V \)
  - \( I_{DS} \): DAC Digital Inputs \( +5V \)
  - \( I_{DN} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
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</thead>
<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
</tbody>
</table>

- **Gain (A)\( \times 12 \)**
  - \( I_{DB} \): DAC Digital Inputs \( 0V \)
  - \( I_{DS} \): DAC Digital Inputs \( +5V \)
  - \( I_{DN} \): DAC Digital Inputs \( +15V \)

- **Analog Characteristics**
  - \( T_A = +25^\circ C \)
  - \( T_A = +70^\circ C \)

<table>
<thead>
<tr>
<th>( T_A = +25^\circ C )</th>
<th>( T_A = +70^\circ C )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
<tr>
<td>( 0.1 )</td>
<td>( 0.1 )</td>
</tr>
</tbody>
</table>
### APPENDIX II

Output for various attenuator settings with inputs of 1V and 2V

<table>
<thead>
<tr>
<th>attenuator setting</th>
<th>1V</th>
<th>2V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000000000001</td>
<td>.99959</td>
<td>1.99916</td>
</tr>
<tr>
<td>0000000000010</td>
<td>.99958</td>
<td>1.99914</td>
</tr>
<tr>
<td>0000000000100</td>
<td>.99957</td>
<td>1.99914</td>
</tr>
<tr>
<td>0000000010000</td>
<td>.99955</td>
<td>1.99910</td>
</tr>
<tr>
<td>0000000100000</td>
<td>.99951</td>
<td>1.99901</td>
</tr>
<tr>
<td>0000001000000</td>
<td>.99942</td>
<td>1.99884</td>
</tr>
<tr>
<td>0000010000000</td>
<td>.99925</td>
<td>1.99850</td>
</tr>
<tr>
<td>0000100000000</td>
<td>.99891</td>
<td>1.99780</td>
</tr>
<tr>
<td>0001000000000</td>
<td>.99821</td>
<td>1.99642</td>
</tr>
<tr>
<td>0010000000000</td>
<td>.99683</td>
<td>1.99366</td>
</tr>
<tr>
<td>0100000000000</td>
<td>.99407</td>
<td>1.98813</td>
</tr>
<tr>
<td>1000000000000</td>
<td>.98855</td>
<td>1.97709</td>
</tr>
</tbody>
</table>
ADC80

General Purpose ANALOG-TO-DIGITAL CONVERTER

FEATURES
- INDUSTRY-STANDARD 12-BIT ADC
- LOW COST
- ±0.012% LINEARITY
- 25μs MAX CONVERSION TIME
- ±12V or ±15V OPERATION
- NO MISSING CODES -25°C to +85°C
- HERMETIC 32-PIN PACKAGE
- PARALLEL AND SERIAL OUTPUTS
- 595mW MAX DISSIPATION

DESCRIPTION

The ADC80 is a 12-bit successive-approximation analog-to-digital converter, utilizing state-of-the-art CMOS and laser-trimmed bipolar die custom designed for freedom from latch-up and optimum AC performance. It is complete with a comparator, a monolithic 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, and a CMOS logic chip containing the successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Gain and offset errors may be externally trimmed to zero, enabling initial endpoint accuracies of better than ±0.12% (±1/2LSB).

The maximum conversion time of 25μs makes the ADC80 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to 40kHz. In addition, the ADC80 may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80 operates equally well with either ±15V or ±12V analog power supplies, and also requires use of a +5V logic power supply. However, unlike many ADC80-type products, a +5V analog power supply is not required. It is packaged in a hermetic 32-pin side-brazed ceramic dual-in-line package.
### SPECIFICATIONS

#### ELECTRICAL

- **Temperature**: TA = -25°C to +25°C, ±5V = 12V or 15V, Vcc = -5V unless otherwise specified

#### THRESHOLD VOLTAGES

<table>
<thead>
<tr>
<th>ADC80AG-12, ADC80-AQZ-12*</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A/D Voltage Ranges: Unipolar</td>
<td>0 to +5.0 to +10V</td>
<td>±2.5, ±2.5, ±10V</td>
<td>±2.5, ±2.5, ±10V</td>
<td>V</td>
</tr>
<tr>
<td>BIPOLAR</td>
<td>4.9</td>
<td>5</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>Impedance: 0 to -5V, ±2.5V</td>
<td>2.45</td>
<td>2.5</td>
<td>2.55</td>
<td>kΩ</td>
</tr>
<tr>
<td>0 to -10V, -5V</td>
<td>4.9</td>
<td>5</td>
<td>5.1</td>
<td>kΩ</td>
</tr>
<tr>
<td>±10V</td>
<td>9.8</td>
<td>10</td>
<td>10.2</td>
<td>kΩ</td>
</tr>
</tbody>
</table>

#### DIGITAL

Logic Characteristics (Over specified temperature range)

- **Vin**: Logic '1'
  - 2V
- **Vss**: Logic '0'
  - -0.3V
- **IV**: (Vref = +2.7V)
  - +0.8V
- **IV**: (Vref = +0.4V)
  - -150μA
- Convert Command Pulse Width
  - 100ns

#### CHARACTERISTICS

- **Accuracy**
  - Gain Error
    - ±0.1% of FSR
  - Offset Error, Unipolar
    - ±0.05% of FSR
  - Bipolar
    - ±0.1% of FSR
  - Linearity Error: ADC80AG-12, ADC80-AQZ-12
    - ±0.048% of FSR
  - ADC80AG-10
    - ±0.03% of FSR
  - Differential Linearity Error
    - ±1/2 LSB
  - Inherent Quantization Error
    - ±1/2 LSB

#### Conversion Time

<table>
<thead>
<tr>
<th>ADC80AG-12, ADC80-AQZ-12</th>
<th>16</th>
<th>22</th>
<th>25</th>
<th>μs</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC80AG-10</td>
<td>13</td>
<td>26</td>
<td>34</td>
<td>μs</td>
</tr>
</tbody>
</table>

#### POWER SUPPLY SENSITIVITY

<table>
<thead>
<tr>
<th>VIN</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>±1.4V ≤ VIN ≤ ±15V</td>
<td>±1.2V ≤ VSS ≤ ±5V</td>
</tr>
<tr>
<td>±0.003V</td>
<td>±0.008V</td>
</tr>
<tr>
<td>±0.002V</td>
<td>±0.005V</td>
</tr>
</tbody>
</table>

#### SHIFT

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>±10%</td>
</tr>
<tr>
<td>Offset, Unipolar</td>
<td>±15μV</td>
</tr>
<tr>
<td>Bipolar</td>
<td>±15μV</td>
</tr>
<tr>
<td>Linearity Error Drift</td>
<td>±7μV</td>
</tr>
<tr>
<td>Differential Linearity over Temperature Range</td>
<td>±1μV</td>
</tr>
<tr>
<td>No Missing Code Temperature Range</td>
<td>±2μV</td>
</tr>
<tr>
<td>Monotonicity Over Temperature Range</td>
<td>±0μV</td>
</tr>
</tbody>
</table>

#### TEMPERATURE RANGE (Ambient)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Operating (derated specs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Range</td>
<td>±25°C</td>
</tr>
<tr>
<td></td>
<td>±65°C</td>
</tr>
</tbody>
</table>

### NOTES:

1. ADC80AG-12 is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range of the ADC80AG-12.
2. Accurate conversion will be obtained by obtain a convert command pulse with at least 10μs; however, it must be limited to 2μs to ensure the specified conversion time.
3. Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section.
4. FSR means Full-Scale Range and is ±20V for ±5V range, ±10V for ±10V and 0 to ±10V ranges, etc. (5) Includes drift due to linearity, gain, and offset drift.
5. Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Preasure" section.
6. CSB means Complementary Straight Binary, and CTC means Complementary Two's Complement coding. See Table 1 for additional information. (7) NRZ means Non-Return-to-Zero coding. (8) External timing must be constant during conversion, and must not exceed 200μs for guaranteed specifications.
CONNECTION DIAGRAM

<table>
<thead>
<tr>
<th>Pin 1</th>
<th>Bit 6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 2</td>
<td>Bit 5</td>
</tr>
<tr>
<td>Pin 3</td>
<td>Bit 4</td>
</tr>
<tr>
<td>Pin 4</td>
<td>Bit 3</td>
</tr>
<tr>
<td>Pin 5</td>
<td>Bit 2</td>
</tr>
<tr>
<td>Pin 6</td>
<td>Bit 1 (MSB)</td>
</tr>
<tr>
<td>Pin 7</td>
<td>Bit 0 (LSB)</td>
</tr>
<tr>
<td>Pin 8</td>
<td>+5V Digital Supply</td>
</tr>
<tr>
<td>Pin 9</td>
<td>-5V Digital Supply</td>
</tr>
<tr>
<td>Pin 10</td>
<td>Digital Common</td>
</tr>
<tr>
<td>Pin 11</td>
<td>Comparator In</td>
</tr>
<tr>
<td>Pin 12</td>
<td>R1 10V Range</td>
</tr>
<tr>
<td>Pin 13</td>
<td>Analog Offset</td>
</tr>
<tr>
<td>Pin 14</td>
<td>Comparator In</td>
</tr>
<tr>
<td>Pin 15</td>
<td>Analog Common</td>
</tr>
<tr>
<td>Pin 16</td>
<td>Vcc</td>
</tr>
</tbody>
</table>

* +5V applied to pin 7 has no effect on circuit.

MECHANICAL

* Leads in true position within 0.1" (2.54mm) at MMC at sealing plane.
* Seal ring is connected to Pin 10.

** Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic, hermetic
MATING CONNECTOR: 2022MC
WEIGHT: 7.3g (0.26oz)

ABSOLUTE MAXIMUM RATINGS

+Vcc to Analog Common: 0 to +16.5V
-Vcc to Analog Common: 0 to -16.5V
Vcc to Digital Common: 0 to +7V
Analog Common to Digital Common: ±0.5V
Logic Inputs (Convert Command, Clock In) to Digital Common: -0.3V to +0.5V
Analog Inputs (Alternating, Bipolar Offset) to Analog Common: ±16.5V
Reference Output: Indefinite Short to Common, Momentary Short to Vcc
Lead Temperature, Soldering: ±300°C, 10s

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate ESD handling procedures should be followed.
Stresses above those tested under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

TOP VIEW

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Model</th>
<th>Resolution (Bts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC80AG-10</td>
<td>10</td>
</tr>
<tr>
<td>ADC80AG-12</td>
<td>12</td>
</tr>
<tr>
<td>ADC80AG-12Q</td>
<td>12</td>
</tr>
<tr>
<td>ADC80AGZ-12</td>
<td>12</td>
</tr>
</tbody>
</table>

NOTES: (1) A suffix indicates Environmental Screening; see Table IV for details.
(2) ADC80AG-12Q is not recommended for new designs. Standard ADC80AG-12 now meets the extended power supply range.

TYPICAL PERFORMANCE CURVES

POWER SUPPLY REJECTION

VS POWER SUPPLY RIPPLE FREQUENCY

% of FS Error vs Frequency (Hz)

CAUTION: These devices are sensitive to electrostatic discharge. Appropriate ESD handling procedures should be followed.
Stresses above those tested under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.


## DISCUSSION OF SPECIFICATIONS

### LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Under this definition of linearity (sometimes referred to as integral linearity), ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale, providing a significantly better definition of converter accuracy than the beststraight-line-fit definition of linearity employed by some manufacturers.

The zero or minus full-scale value is located at an analog input value 1/2LSB before the first code transition (FFE:end to FFE:end). The plus full-scale value is located at an analog value 3/2LSB beyond the last code transition (000 to 000). See Figure 1 which illustrates these relationships. A linearity specification which guarantees ±1/2LSB maximum linearity error assures the user that no code transition will differ from the ideal transition value by more than ±1/2LSB.

Thus, for a converter connected for bipolar operation and defined with a full-scale range (or span) of 20V (±10V operation), the minus full-scale value of −10V is 2.44mV below the first code transition (FFE:end to FFE:end at −9.99768V) and the plus full-scale value of +10V is 7.32mV above the last code transition (001 to 000 at +9.99268V). Ideal transitions occur 1LSB (4.88mV) apart, and the ±1/2LSB linearity specification guarantees that no actual transition will vary from the ideal by more than 2.44mV. The LSB weights, transition values, and code definitions for each possible ADC80 analog input signal range are described in Table 1.

### TABLE 1. Input Voltages, Transition Values, LSB Values, and Code Definitions.

<table>
<thead>
<tr>
<th>Binary Output</th>
<th>Analog Input Voltage Range</th>
<th>Defined As:</th>
<th>±10V</th>
<th>±5V</th>
<th>±2.5V</th>
<th>0 to +10V</th>
<th>0 to +5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code Designation</td>
<td></td>
<td>COB or CTC</td>
<td>COB or CTC</td>
<td>COB or CTC</td>
<td>COB or CTC</td>
<td>COB or CTC</td>
<td>COB or CTC</td>
</tr>
<tr>
<td>One Least Significant Bit (LSB)</td>
<td>F5/4/2</td>
<td>20V/2</td>
<td>10V/2</td>
<td>5V/2</td>
<td>10V/2</td>
<td>5V/2</td>
<td>10V/2</td>
</tr>
<tr>
<td>n = 8</td>
<td>78.13mV</td>
<td>39.06mV</td>
<td>18.53mV</td>
<td>39.06mV</td>
<td>18.53mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n = 10</td>
<td>18.53mV</td>
<td>9.77mV</td>
<td>4.88mV</td>
<td>9.77mV</td>
<td>4.88mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n = 18</td>
<td>4.88mV</td>
<td>2.44mV</td>
<td>1.22mV</td>
<td>2.44mV</td>
<td>1.22mV</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transition Values</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>MSB LSB</td>
<td>001 to 000n</td>
<td>+Full Scale</td>
<td>+10V - 3/2LSB</td>
<td>+5V - 3/2LSB</td>
<td>+2.5V - 3/2LSB</td>
<td>+10V - 3/2LSB</td>
<td>+5V - 3/2LSB</td>
</tr>
<tr>
<td>000 to FFb</td>
<td>+Full Scale</td>
<td>+10V - 3/2LSB</td>
<td>+5V - 3/2LSB</td>
<td>+2.5V - 3/2LSB</td>
<td>+10V - 3/2LSB</td>
<td>+5V - 3/2LSB</td>
<td>+2.5V - 3/2LSB</td>
</tr>
<tr>
<td>FFb to FFb</td>
<td>+1/2LSB</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

COS = Complementary Offset Binary

COS = Complementary Straight Binary

CTC = Complementary Truncation Complement

F5/4/2 = Complementary Offset Binary

**Note:** The LSB is available on page 6.
CODE WIDTH (QUANTUM)

Code width (or quantum) is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1 LSB, which for 12-bit operation with a 20V span is equal to 4.88mV. Refer to Table I for LSB values for other ADC80 input ranges.

DIFFERENTIAL LSB ERROR AND NO MISSING CODES

Differential linearity error is the difference between an ideal 1 LSB code width (quantum) and the actual code width. A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input is increased throughout the range, requiring that every input quantum must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1 LSB), a missing-code will occur but the converter may still be monotonic. Thus, no missing codes represent a more stringent definition of performance than does monotonicity. ADC80 is guaranteed to have no missing codes to 12-bit resolution over its full specification temperature range.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2 LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

UNIPOLAR OFFSET ERROR

An ADC80 connected for unipolar operation has an analog input range of 0V to plus full-scale. The first output code transition should occur at an analog input value 1/2 LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value, and is applicable only to converters operating in the unipolar mode.

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset at the first transition value above the minus full-scale value. The ADC80 follows this convention. Thus, bipolar offset error for the ADC80 is defined as the deviation of the actual transition value from the ideal transition value located 1/2 LSB above minus full scale.

GAIN ERROR

The last output code transition (00000 to 00000) occurs for an analog input value 3/2 LSB below the nominal plus full-scale value. Gain error is the deviation of the actual analog value at the last transition point from the ideal value.

ACCURACY DRIFT VS TEMPERATURE

The temperature coefficients for gain, unipolar offset, and bipolar offset specify the maximum change from the actual 25°C value to the value at the extremes of the specified temperature range. The temperature coefficient applies independently to the two halves of the full-scale range above and below +25°C.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC80 assume application of the rated power supply voltages of ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a change in the plus full-scale value. This, of course, results in a proportional change in all transition values (i.e., a gain error). The specification describes the maximum change in the plus full-scale value from the initial value for independent changes in each power supply voltage.

TIMING CONSIDERATIONS

Timing relationships of the ADC80 are shown in Figure 2. It should be noted that although the convert command pulse width must be between 100ns and 2µs to obtain the specified conversion time with internal clock, the ADC will accept longer convert commands with no loss of accuracy, assuming that the analog input signal is stable.
low state. In addition, although the initial state of the converter will be indeterminate when power is first applied, it is designed to time-out and be ready to accept a convert command within approximately 25μs after power-up, provided that either an external clock source is present or the internal clock is not inhibited.

During conversion, the decision as to the proper state of any bit (bit "n") is made on the rising edge of clock pulse \( t_n + 1 \). Thus, a complete conversion requires 13 clock pulses with the status output dropping from logic "1" to logic "0" shortly after the rising edge of the 13th clock pulse, and with valid output data ready to be read at that time. A new conversion may not be initiated until 50ns after the fall of the last clock pulse (pulse 13 for 12-bit operation).

Additional convert commands applied during conversion will be ignored.

**DEFINITION OF DIGITAL CODES**

**Parallel Data**

Three binary codes are available on the ADC80 parallel output; all three are complementary codes, meaning that logic "0" is true. The available codes are complementary straight binary (CSB) for unipolar input signal ranges, and complementary offset binary (COB) and complementary two's complement (CTC) for bipolar input signal ranges. CTC coding is obtained by complementing bit 1 (the MSB) of the COB code; the complement of bit 1 is available on pin 8.

**Serial Data**

Two (complementary) straight binary codes are available on the serial output of the ADC80: as in the parallel case, they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values of Table I also apply to the serial data output, except that the CTC code is not available. All clock pulses available from the ADC80 have equal pulse widths to facilitate transfer of the serial data into external logic devices without external shaping.

**LAYOUT AND OPERATING INSTRUCTIONS**

**LAYOUT PRECAUTIONS**

Analog and digital commons are not connected together internally in the ADC80, but should be connected together as close to the unit as possible, preferably to an analog common ground plane beneath the converter. If these common lines must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input lines and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common. If external gain and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC80 as possible.

**POWER SUPPLY DECOUPLING**

The power supplies should be bypassed with 1μF to 10μF tantalum bypass capacitors located close to the converter to obtain noise-free operation. Noise on the power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

**ANALOG SIGNAL SOURCE IMPEDANCE**

The signal source supplying the analog input signal to the ADC80 will be driving into a nominal DC input impedance of 2.5kΩ to 10kΩ depending upon the range selected. However, the output impedance of the driving source should be very low, such as the output impedance provided by a wideband, fast-settling operational amplifier. Transients in A/D input current are caused by the changes in output current of the internal D/A converter as it tests the various bits. The output voltage of the driving source must remain constant while furnishing these fast transient changes. If the application requires a sample/hold, select a sample/hold with sufficient bandwidth to preserve the accuracy or use a separate wideband buffer amplifier to lower the output impedance.

**INPUT SCALING**

The ADC80 offers five standard input ranges: 0V to +5V, 0V to +10V, ±2.5V, ±5V, and ±10V. The input range should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the converter. Select the appropriate input range as indicated by Table II. The input circuit architecture is illustrated in Figure 3. External peaking resistors can be added to modify the factory-set input ranges (such as addition of a small external input resistor to change the 10V range to a 10.24V range). Alternatively, the gain range of the converter may easily be increased a small amount by use of a low temperature coefficient potentiometer in series with the analog input signal or by decreasing the value of the gain adjust series resistor in Figure 5.

**TABLE II. ADC80 Input Scaling Connections.**

<table>
<thead>
<tr>
<th>Input Signal Range</th>
<th>Output Code</th>
<th>Connect Pin 12 To Pin</th>
<th>Connect Pin 14 To</th>
<th>Connect Input Signal To</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10V</td>
<td>COB or CTC</td>
<td>11</td>
<td>Input Signal</td>
<td>14</td>
</tr>
<tr>
<td>±5V</td>
<td>COB or CTC</td>
<td>11</td>
<td>Open</td>
<td>13</td>
</tr>
<tr>
<td>±2.5V</td>
<td>COB or CTC</td>
<td>11</td>
<td>Pin 11</td>
<td>13</td>
</tr>
<tr>
<td>0 to +5V</td>
<td>CSB</td>
<td>15</td>
<td>Pin 11</td>
<td>13</td>
</tr>
<tr>
<td>0 to +10V</td>
<td>CSB</td>
<td>15</td>
<td>Open</td>
<td>13</td>
</tr>
</tbody>
</table>

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CALIBRATION

Optional External Gain And Offset Adjustments

Gain and offset errors may be trimmed to zero using external offset and gain trim potentiometers connected to the ADC80 as shown in Figures 4 and 5 for both unipolar and bipolar operation. Multiturn potentiometers with 100ppm/°C or better TCR are recommended for minimum drift over temperature and time. These pots may be of any value between 10kΩ and 100kΩ. All fixed resistors should be 20% carbon or better. Although not necessary in some applications, pin 16 (Gain Adjust) should be preferably bypassed with a 0.01µF nonpolarized capacitor to analog common to minimize noise pickup at this high impedance point, even if no external adjustment is required.

GAIN—Connect the gain adjust potentiometer as shown in Figure 5. Set the input voltage to the nominal full-scale value minus 3/2LSB. Once again refer to Table I, this value is +10V -7.32mV or +9.99265V the -10V to +10V range. Adjust the gain potentiometer until the output code is alternating between 000 and 001n with an approximate 50% duty cycle. As in the case of offset adjustment, this procedure sets the end-point transitions to a precisely known value.

CLOCK OPTIONS

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with inexpensive TTL logic as shown in Figures 6 through 9. When operating with an external clock, conversion time may be as short as 15µs (800kHz external clock frequency) with assured performance within specified limits. When operating with the internal clock, pin 19 (external clock input) and pin 20 (clock inhibit) may be left unconnected. No external pull-up resistors are required due to the inclusion of pull-up resistors on the ADC80. Pin 20 (clock inhibit) must be grounded to use with an external clock, which is applied to pin 19.

SHORT-CYCLE FEATURE

A short-cycle input (pin 21) permits the conversion to be terminated after any number of desired bits has been converted, allowing shorter conversion times in applications not requiring full 12-bit resolution. In these situations, the short-cycle pin should be connected to the output pin of the next bit after the desired resolution. For example, when 10-bit resolution is desired, pin 21 is connected to pin 28 (bit 11). In this example, the conversion cycle terminates and status is reset after the bit 10 decision. Short-cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times (with internal clock) are shown in Table III. Also shown are recommended minimum conversion times (external clock) for these conversion lengths to obtain the stated accuracies. The ADC80 is not factory-tested for these external clock conversion speeds and the product is not guaranteed to achieve the stated accuracies under these operating conditions; the recommended values are offered as a guide to the user.

TABLE III. Short-Cycle Connections and Conversion Times for 8-, 10-, and 12-Bit Resolutions—ADC80.

<table>
<thead>
<tr>
<th>Resolution (Bits)</th>
<th>12</th>
<th>10</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connect pin 21 to</td>
<td>Pin 9 or NC</td>
<td>Pin 29</td>
<td>Pin 30</td>
</tr>
<tr>
<td>Maximum Conversion Time** (µs) Internal Clock</td>
<td>25</td>
<td>22</td>
<td>18</td>
</tr>
<tr>
<td>Minimum Conversion Time** (µs) External Clock</td>
<td>18</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>Maximum Linearity Error at -75°C (% of FSR)</td>
<td>0.012</td>
<td>0.048</td>
<td>0.29</td>
</tr>
</tbody>
</table>

*NOTE (1) Conversion time to maintain ±1/2LSB linearity error.
FIGURE 6. Internal Clock—Normat Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

FIGURE 7. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

FIGURE 9. Continuous Conversion with 600ns between Conversions. (Circuit insures that conversion will start when power is applied.)

TABLE IV. Screening Flow for ADC80AG-12Q

<table>
<thead>
<tr>
<th>Screening Level</th>
<th>Screening Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Visual</td>
<td>Burr-Brown QC411B</td>
</tr>
<tr>
<td>High Temperature Storage (Stabilization Bake)</td>
<td>1008, C, 24 hour, +150°C</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>1010, C, 10 cycles, -65°C to +150°C</td>
</tr>
<tr>
<td>Constant Acceleration</td>
<td>2001, A, 5000 G</td>
</tr>
<tr>
<td>Electrical Test</td>
<td>Burr-Brown test procedure</td>
</tr>
<tr>
<td>Burn-In</td>
<td>1015, B, 160 hour, +125°C, steady-state</td>
</tr>
<tr>
<td>Humidity: Fine Lines Gross</td>
<td>1014, A1 or A2, or</td>
</tr>
<tr>
<td>Moisture-</td>
<td>Burr-Brown test procedure</td>
</tr>
<tr>
<td>Final Electrical</td>
<td>Burr-Brown test procedure</td>
</tr>
<tr>
<td>Final Drift</td>
<td>Burr-Brown test procedure</td>
</tr>
<tr>
<td>External Visual</td>
<td>Burr-Brown QC3168</td>
</tr>
</tbody>
</table>

ENVIRONMENTAL SCREENING

The inherent reliability of a semiconductor device is controlled by the design, materials, and fabrication of the device—it cannot be improved by testing. However, the use of environmental screening can eliminate the majority of those units which would fail early in their lifetimes (infant mortality) through the application of carefully selected accelerated stress levels. Burr-Brown Q models are environmentally screened versions of our standard industrial products, designed to provide enhanced reliability. The screening illustrated in Table IV is performed to selected methods of MIL-STD-883. Reference to these methods provides a convenient way of communicating the screening levels and basic procedures employed; it does not imply conformance to any other military standards or to any methods of MIL-STD-883 other than those specified. Burr-Brown's detailed procedures may vary slightly, model-to-model, from those in MIL-STD-883.
APPENDIX IV

(Program to calculate the poles of the digital filter)

Program Poles(input, output, file1, file2);

Type
    NUM = 0 .. 50;
    Vector = array [NUM] of real;
    Matrix = array [NUM] of Vector;

Const
    N1=20.0;
    N2=20;
    U=1.010425884;
    V=0.144777302;
    T1=1.5E-5;
    T2=1E-1;
    fp=1.0;
    fl=2E3;
    f2=1.5E4;
    PI=3.141592654;

Var
    A, B, C, D, E, F, G : real;
    I, J : integer;
    M, N : Matrix;
    file1, file2 : file of real;

Begin
    (Calculate poles of low-pass filter)
    Begin
        Rewrite (file1);
        Rewrite (file2);
        C := fp*T2/2.0;
        J := 0;
        For I := 0 to 2*N2-1 do
            Begin
                A := (2*I + 1)/(2*N1);
                B := A*PI;
                D := cos(B);
                E := sin(B);
                X[I] := 1-sqr(C)*(sqr(V)*sqr(E)+sqr(U)*sqr(D));
                A := (sqr(1-V*C*E)+sqr(U*C*D));
                X[I] := X[I]/A;
                Y[I] := 2.0*U*C*D;
                Y[I] := Y[I]/A;
            End;
        Begin
            For I := 0 to 2*N2-1 do
                If (sqr(X[I])+sqr(Y[I]))<1 then
                    Begin
                        X[J] := X[I];
                        Y[J] := Y[I];
                        J := J+1;
                    End;
    End;
End;
Begin
A := 2*PI*f2*T1;
B := 2*PI*f1*T1;
C := f2*T2/2;
E := (A-B)/2;
F := (A+B)/2;
D := cos(F)/cos(E);
F := C*cos(E)/sin(E);
A := 2*D*F/(F+1);
B := (F-1)/(F+1);
J := 0;
For I := 0 to N2-1 do
Begin
W[I] := X[I] + 1;
Z[I] := 2*W[I]*Y[I]*sqr(A);
W[I] := (sqr(W[I]) - sqr(Y[I]))*sqr(A);
W[I] := W[I] - 4*((1+B*X[I])*(X[I]+B) - B*sqr(Y[I]));
Z[I] := Z[I] - 4*Y[I]*(I+sqr(B)+2*B*X[I]);
R[I] := sqrt(sqr(W[I])+sqr(Z[I]));
S[I] := arctan(Z[I]/W[I]);
If (W[I]<0) then
Begin
S[t] := S[I] + PI;
End;
R[I] := sqrt(R[I]);
S[I] := S[I]/2;
W[I] := R[I]*cos(S[I]);
Z[I] := R[I]*sin(S[I]);
M[1,I] := A*(X[I]+1) + W[I];
M[2,I] := A*(X[I]+1) - W[I];
N[1,I] := A*Y[I] + Z[I];
F := 2*(sqr(X[I]*B+1)+sqr(B)*sqr(Y[I]));
G := M[1,I];
M[1,I] := (M[1,I]*(X[I]*B+1)+N[1,I]*B*Y[I])/F;
N[1,I] := (N[1,I]*(X[I]*B+1)-G*B*Y[I])/F;
G := M[2,I];
Begin
H[J] := M[1,I];
K[J] := N[1,I];
J := J+1;
End;
Begin
H[J] := M[2,I];
K[J] := N[2,I];
J := J+1;
End;
End;
End;
Begin
For I := 0 to 19 do
Begin
   Write(file1, H[I]);
   Write(file2, K[I]);
End;
End;
End.
APPENDIX V

(Program to calculate amplitude of low pass filter for input frequency)

Program amp(input, output, file1, file2);

Type

NUM = 0 .. 100;

Vector = array [NUM] of real;

Var

I, J : integer;
alpha, A, B, C, D, E, X, Y, angle : real;
file1, file2 : file of real;

Begin

Readln (alpha);
A := sqr(1 + cos(alpha));
B := sqr(sin(alpha));
E := sqrt(B + A);
A := 1;
Reset(file1);
Reset(file2);
For I := 0 to 9 do
Begin
read(file1, X);
read(file2, Y);
B := sqr(sin(alpha) + Y);
C := sqr(cos(alpha) - X);
D := sqr(sin(alpha) - Y);
A := (A * E) / (sqrt(C + D) * sqrt(C + B));
End;
Begin
writeln(A);
end;
end.
APPENDIX VI

(Program to calculate the coefficients of the denominator of the system function of the digital filter)
Program coef(input, output, file1, file2);
  Const
    N=20;
  Type
    NUM = 0 .. 50;
    Vector = array [NUM] of real;
  Var
    I, J, N1, N2 : integer;
    U, V, W, X, Y, Z : vector;
    file1, file2 : file of real;
Begin
  Writeln('denominator coefficients');
  Reset(file1);
  Reset(file2);
  For I := 1 to 20 do
    Begin
      read(file1, X[I]);
      read(file2, W[I]);
      Y[I] := -2.0*X[I];
      V[I] := sqr(X[I])+sqr(W[I]);
    End;
  Rewrite(file1);
  Rewrite(file2);
  For J := 1 to 20 do
    Begin
      Write(file1, Y[J]);
      Write(file2, V[J]);
    End;
End.
APPENDIX VII

Program Filter (input, output, file1, file2, file3);
const
  N = 1000000;
  K = 3.3454656E-19;
Type
  NUM = 0..100;
  Vector = array[NUM] of real;
Var
  I, J, M1 : integer;
  A, B, C : real;
  X, Y, W, Z : Vector;
  file1, file2, file3 : file of real;
Begin
  Readln(M1);
  Reset(file1);
  Reset(file2);
  Reset(file3);
  B := 0;
  For I := 1 to 20 do
    Begin
      Read(file1, W[I]);
      Read(file2, Z[I]);
      Begin
        For J := 0 to M1 do
          Begin
          End;
        For J := 0 to M do
          Begin
            X[J] := Y[J];
          End;
        End;
    End;
  For J := 0 to M do
    Begin
      B := (B*(J-1) + sqr(X[I]))/J;
    End;
  B := K*B;
  writeln(B);
End.
APPENDIX VIII

Program ampl(input, output, file1, file2);
Type
    NUM = 0 .. 100;
    Vector = array [NUM] of real;
Var
    I, J, M : integer;
    alpha, A, B, C, D, E, F, X, Y, angle : real;
    file1, file2 : file of real;
Begin
    alpha := 0;
    F := 0;
    Readln(M);
    For J := 1 to 100 do
    Begin
        alpha := alpha + 0.036;
        A := sqr(1-cos(2*alpha));
        B := sqr(sin(2*alpha));
        E := sqrt(B+A);
        A := file1;
        Reset(file1);
        Reset(file2);
        For I := 1 to M do
        Begin
            read(file1, X);
            read(file2, Y);
            B := sqr(sin(alpha)+Y);
            C := sqr(cos(alpha)-X);
            D := sqr(sin(alpha)-Y);
            A := (A*E)/(sqrt(C+D)*sqrt(C+B));
        End;
        F := F + 3.6E-2*sqr(A);
    End;
    A := F/E;
    writeln(A);
End.
End.
APPENDIX IX

(This program evaluates the value of either side of Parseval's Equation)

Program error(input, output);

label 10;

Type
  NUM= 0 .. 100;
  Vector = array [NUM] of real;
  Matrix = array [NUM] of Vector;

Var
  nu, de, I, J, K, L, M : integer;
  sol, R, S : real;
  X, Y, H, D : Vector;
  AA : Matrix;

Procedure T(M, N : integer; A, B : Vector);

label 10;

Var
  I, K, INDEX : integer;
  BH : real;

Begin
  For K := 0 to M do
    Begin
      BH := 0;
      For I := 1 to N do
        Begin
          INDEX := K-I;
          If INDEX < 0 then goto 10
          Else BH := BH + B[I]*H[INDEX];
        10 : End;
    End;
  End;

Procedure F(M, N : integer; A, B : Vector);

label 20, 30;

Var
  MIN, K, I : integer;
  HA : real;

Begin
  Begin
    If N < M then MIN := N else MIN := M;
  End;
  Begin
    For K := 0 to N do
      Begin
        If K > MIN then goto 20;
        HA := 0;
        For I := 0 to M-K do
          Begin
            HA := HA + B[I]*A[I+K];
          End;
      End;
  End;
End;
D[K] := HA;
goto 30;
20 : D[K] := 0;
30 : End;
End;
End;

Procedure BB(N : integer; B : Vector);
Var
I, J, INDEX1, INDEX2 : integer;
Begin
For I := 0 to N do
Begin
AA[I,0] := B[1];
End;
For J := 1 to N do
Begin
For I := 0 to N do
Begin
INDEX1 := I+J;
INDEX2 := I-J;
If INDEX2 < 0 then AA[I,J] := B[INDEX1]
Else
Begin
If I+J > N then AA[I,J] := B[INDEX2]
End;
End;
End;
End;
End;

(Tody of main program)
Begin
Readln(NU);
Readln(DE);
For I := 0 to NU do
Begin
Readln (X[I]);
End;
For I := 0 to DE do
Begin
Readln (Y[I]);
End;
T(NU, DE, X, Y);
F(NU, DE, X, H);
BB(DE, Y);
Begin
For I := 0 to DE-1 do
Begin
  If AA[I,DE-I] = 0 then
  Begin
    For L := I+1 to DE do
    Begin
      If not (AA[L,DE-I]=0) then
      Begin
        For M := 0 to DE-I do
        Begin
          S := A[I,M];
          AA[I,M] := AA[L,M];
          AA[L,M] := S;
          S := D[I];
          D[L] := D[I];
          D[I] := S;
        End;
        goto 10;
      End;
    End;
  End;
Else
  10:
  Begin
    For J := I+1 to DE do
    Begin
      R := AA[J,DE-I]/AA[I,DE-I];
      D[J] := D[J] - R*D[I];
      For K := 0 to DE-I do
      Begin
      End;
    End;
  End;
End;
sol := D[DE]/AA[DE,0];
writeln(sol);
End.
# APPENDIX X

Data from measurement of Analog Filter at Different Frequencies with an 1V input.

<table>
<thead>
<tr>
<th>Date</th>
<th>time</th>
<th>1 KHz</th>
<th>2 KHz</th>
<th>6 KHz</th>
<th>20 KHz</th>
<th>30 KHz</th>
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</thead>
<tbody>
<tr>
<td>11/30/88</td>
<td>10:15</td>
<td>.17775</td>
<td>.18508</td>
<td>.19671</td>
<td>.19416</td>
<td>.16782</td>
</tr>
<tr>
<td></td>
<td>4:10</td>
<td>.17792</td>
<td>.18508</td>
<td>.19671</td>
<td>.19418</td>
<td>.16789</td>
</tr>
<tr>
<td>12/1/88</td>
<td>10:05</td>
<td>.17791</td>
<td>.18508</td>
<td>.19671</td>
<td>.19417</td>
<td>.16783</td>
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<td>3:30</td>
<td>.17795</td>
<td>.18508</td>
<td>.19672</td>
<td>.19419</td>
<td>.16790</td>
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<td>12/2/88</td>
<td>9:30</td>
<td>.17784</td>
<td>.18509</td>
<td>.19672</td>
<td>.19418</td>
<td>.16779</td>
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<td>8:15</td>
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<td>.18514</td>
<td>.19676</td>
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<td>4:50</td>
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<td>.19676</td>
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<td>12/5/88</td>
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<td>1:32</td>
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<td>.18512</td>
<td>.19675</td>
<td>.19424</td>
<td>.16798</td>
</tr>
<tr>
<td></td>
<td>9:26</td>
<td>.17825</td>
<td>.18512</td>
<td>.19674</td>
<td>.19424</td>
<td>.16796</td>
</tr>
<tr>
<td>12/8/88</td>
<td>9:56</td>
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<td>4:53</td>
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<td>.18513</td>
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## APPENDIX XI

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VII. REFERENCES


