Vibration-to-Electric Energy Conversion Using a Mechanically-Varied Capacitor

by

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Bachelor of Science in Electrical Engineering and Computer Science
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Abstract

Past research in vibration energy harvesting has focused on the use of variable capacitors, magnets, or piezoelectric materials as the basis of energy transduction. However, few of these studies have explored the detailed circuits required to make the energy harvesting work. In contrast, this thesis develops and demonstrates a circuit to support variable-capacitor-based energy harvesting. The circuit combines a diode-based charge pump with an asynchronous inductive flyback mechanism to return the pumped energy to a central reservoir. A cantilever beam variable capacitor with 650 pF DC capacitance and 347.77 pF zero-to-peak AC capacitance, formed by a 43.56 cm² spring steel top plate attached to an aluminum base, drives the experimental charge pump near 1.56 kHz.

HSPICE simulation confirms that given a maximum to minimum capacitance ratio larger than 1.65 and realistic models for the transistor and diodes, the circuit can harvest approximately 1 μW of power. This power level is achieved after optimizing the flyback path to run at approximately 1/4 of the mechanical vibration frequency with a duty ratio of 0.0019. Simulation also shows that unless a source-referenced clock drives the MOSFET, spurious energy injection can occur, which would inflate the circuit's conversion efficiency if the harvester is driven by an external clock.

A working vibration energy harvester comprising a time varying capacitor with a capacitance ratio of 3.27 converted sufficient energy to sustain 6 V across a 20 MΩ load. This translates to an average power of 1.8 μW. Based on a theoretical harvesting limit of 40.67 μW, the prototype achieved a conversion efficiency of 4.43 %. Additional experiments confirm that the harvester was not sustained by clock energy injection. Finally, the harvester could start up from a reservoir voltage of 89 mV, suggesting that the circuit can be initiated by an attached piezoelectric film.

Thesis Supervisor: Jeffrey H. Lang
Title: Associate Director, Laboratory for Electronic and Electromagnetic Systems
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Chapter 1

Introduction

More than two thousand years ago, Greeks and Romans used waterwheels, placed strategically along streams, to mechanically rotate gears that helped grind corn. This simple idea spread around the world, and over the centuries, people built upon the original design in hopes of improving the conversion efficiency between flowing water and useful energy. In 1862, turbines situated in Wisconsin managed to produce 12.5 kW of power based solely on water gushing through the equipment when the dam doors opened. The above development serves to illustrate that the concept of energy harvesting is nothing new. Rather, the methodology and principles of creating an efficient system evolves.

Scavenging the energy of ambient vibrations constitutes one such methodology, and this will be the focus of the present thesis. Broadly speaking, vibration energy harvesting involves the creation of some physical structure that can couple in kinetic energy from small vibrations and convert it into storable electric energy. Due to the growing demand of autonomous sensors that must function without the need for human intervention, interest in this topic has burgeoned in recent years. Although other methods of energy scavenging, such as those involving thermal and chemical gradients, tidal waves, and photons, are also being actively researched, the wide availability of vibration energy makes it a very good candidate, and this thesis will
show that the parts necessary to carry out such energy harvesting are relatively simple.

This chapter presents a broad overview of the current affairs in vibration energy harvesting, including the different methods presently employed as well as the reasons behind the continual interest in this topic. Furthermore, important achievements documented in the literature will be summarized and categorized.

1.1 Concept of Energy Harvesting

Fundamentally, energy harvesting involves the conversion of ambient energy such as light, heat, or mechanical motion into electrical energy that can directly power an external system or be stored in battery cells for future use. If the energy source is further limited to mechanical kinetic energy, or vibrations, three main strategies of conversion dominate: piezoelectric, magnetic, and electric. Magnetic conversion can be further subcategorized into systems with varying inductance and systems that employ moving permanent magnets. Likewise, electric conversion uses either a time varying capacitor or a permanent electret, where a fixed charge distribution is introduced in the dielectric layer between the capacitor plates. Although the scope of this thesis covers variable capacitor electric energy harvesting only, all three strategies have their own merits.

Piezoelectric materials, such as quartz and barium titanate, contain permanently-polarized structures that produce an electric field when the materials deform as a result of an imposed mechanical force [1]. Such a mechanically excited element can be modeled as a sinusoidal current source with a capacitive source impedance [2] where the amplitude of the current depends on the amount of force applied. Therefore, if this structure is placed near a constantly vibrating source, such as office walls near a construction site, it can harvest the vibration energy and generate electric power.

Magnetic energy harvesting, on the other hand, seeks to convert vibrational kinetic energy into an induced voltage across coils of wire, which then can deliver power to an
appropriate load. This is typically done by attaching either a permanent magnet, such as that made from Neodymium Iron Boron, or a coil of wire onto a cantilever beam that is vibrationally actuated [3]; the other one remains fixed. In either scenario, the coil will cut through magnetic flux as the cantilever beam vibrates, creating an induced voltage in accordance to Faraday's law. Vibration energy can also be coupled into the system through the use of a variable inductor, although no studies have been done on this to date due to inherent advantages of using permanent magnets. While this method of energy harvesting possess very high conversion efficiency, magnets, bulky in nature, make these type of systems difficult to integrate with the load it is driving.

Finally, electric energy harvesting couples vibration energy into the system by having it perform work on charges via the electric field between parallel plate capacitors. In a typical scenario, charges are injected onto capacitor plates when they are closest together, meaning that the capacitance is at its maximum. Because charges of opposite polarity reside on the separate plates, the plates tend to collapse when no external force is applied. Therefore, as vibration energy separates the two plates, it performs positive work on the charges, which are then drained from the plates when the capacitor voltage is highest and harvested using power electronics. Besides the variable capacitor, one can also employ a layer of embedded charge, or electret, in the dielectric to carry out electric energy harvesting [4]. Such a distribution of permanent charges induces a voltage on the capacitor plates, polarizing them. As external vibration moves the capacitor plates and alters the capacitance, charge transport along the plates delivers power to the load. Most state of the art electret systems currently have power densities inferior to those found in variable capacitor systems, so the variable capacitor is preferred until further advances are made in the use of embedded charges.
1.2 Reasons to Research

Although the method of harvesting energy varies vastly, the ultimate goal of all vibration energy harvesters is to deliver the converted electrical energy to an attached load that requires power. One might question the necessity of expunging proven techniques of expending electrochemical energy stored on batteries in favor of energy harvesting circuits, some of which cannot perform nearly as efficiently compared to batteries. In reality, while batteries can painlessly power common household items including alarm clocks, radios, and wireless keyboards, many scenarios require extended lifetime a typical battery cannot provide. Batteries are also limited to certain temperature ranges; beyond those ranges, they begin to malfunction.

Consider the difficulty of powering an RF sensor network that must operate in harsh environments for prolonged periods of time, perhaps a couple years. In military applications, motion sensors used for tracking enemy movement might be dropped into enemy territories from low-flying planes. Or, seismological sensors could be deployed in uninhabited areas accessible only by helicopters. As a final example, wildlife researchers tracking the behavior of rare bird species might need RFID chips placed on birds; trying to replace the batteries on these radio frequency tags after releasing the birds back into nature is difficult and time consuming. Even when the research can be completed within the battery lifetime, poisonous mercury pollution from battery corrosion can occur if they are not ultimately recovered.

In all these cases, the sensors must be autonomous as far as energy supply goes, since physical access to the units is costly, if not impossible. Even if battery replacement were possible, trying to switch out batteries from thousands of sensor units simultaneously require a tremendous amount of manpower, which can be just as, if not more, infeasible. With an energy harvesting circuit powering these sensor units, the above problems can be solved.

Applications of energy harvesting are not limited to sensor networks. In the
army, for example, standard issue equipment such as night vision goggles and radio transmitters require power supplies. However, carrying excess batteries increases the load on the soldiers, so it is preferable that the electronics be powered off available ambient energy sources. This might include recoil energy from a rifle or parasitic compression energy from the sole of a soldier’s boot striking the ground [5].

Of course, in order to successfully maintain power delivery to its load, an energy harvesting circuit needs to fulfill two requirements: efficiency and the ability to store converted energy. Vibrations in nature, although common, usually do not occur at very high frequencies. Typical frequencies might range from a few hertz to a couple kilohertz. High conversion efficiency insures that as much energy as possible can be extracted from these slow vibrations. Furthermore, because there are often dead times between the occurrence of vibrations, the system must be capable of storing unused energy efficiently in anticipation of later times when power demand exceeds the amount harvested.

These two requirements are difficult to meet using traditional energy harvesting techniques. As a baseline of comparison, solar panels are often only 10–20 % efficient, whereas the goal of energy harvesting circuits lie around 70–80 % efficiency. Sending the harvested energy into a capacitive or electrochemical source usually requires the use of DC/DC converters, a circuit topology falling in the regime of power electronis. Being able to maintain high efficiency in this energy flyback portion of the system as the amplitude and frequency of harvested energy change requires careful design.

1.3 Previous Works

A careful literature survey of recent developments in the field of energy harvesting is appropriate for placing the current thesis in context. However, due to the wide range of techniques used for energy harvesting, some as unusual as exploiting chemical and thermal gradients, this thesis will limit the survey to vibrational kinetic energy
Numerous research groups have focused on piezoelectric energy harvesting due to its potential of achieving the highest converted power per unit volume [6]. Kymissis et al employed unimorph strip made from piezoceramic composite material and a stave made from a multilayer laminate of PVDF foil inside sport sneakers to harvest the parasitic kinetic energy generated during walking [5]. An input signal of 1 Hz, similar in frequency to a person walking briskly, produced 20 mW peak power for the PVDF and 80 mW for the unimorph; this translates to roughly 1–2 mJ per step.

In order to maximize the amount of energy harvested from piezoelectric materials, Ottman et al developed a DSP-controlled, adaptive DC-DC converter that accurately determined the duty ratio of the active devices as a function the instantaneous mechanical excitation amplitude [7]. They showed that as the mechanical excitation increases past a certain point, the optimal duty ratio becomes essentially a constant. A prototype circuit demonstrates a 325 % increase in harvested power using this technique.

As part of Berkeley Wireless Research Center's (BWRC) goal of making an autonomous 1.9 GHz chip-on-board RF transmit beacon, Roundy et al explored the use of a two layer piezoelectric bender mounted as a cantilever beam that harvested vibration energy [8]. They showed that with a driving vibration of 2.25 m/s² at 60 Hz, a maximum of 375μW can be transferred into a purely resistive load. On the other hand, if a capacitive load is attached to store the harvested energy for later use, the maximum delivered power drops to 180μW. In this paper, the authors also implement a shutdown control as part of the power circuitry that prevents the load from consuming energy stored on the capacitor when the capacitor voltage falls below a certain threshold.

In the area of magnetic energy harvesting, Williams and Yates derived an equation relating the amount of generated power as a function of the damping factor for a generator that consists of a permanent magnet attached to a micromachined
spring-mass system [9]. Barring physical limitations of the system, the magnet travels a longer distance near resonance due to peaking in the system's transfer function; this directly translates to increased harvested energy. They note, however, that low damping factor made the system more frequency selective, so if the ambient vibration covers a larger frequency spectrum, the resistive load attached to the inductor coil can be changed to make the harvesting broadband.

Glynne-Jones et al made two actual prototypes of electromagnetic generators used for powering intelligent sensor systems [3]. In these prototypes, coils were hand wound onto a cantilever beam attached to a shaker table and immersed in magnetic fields generated from permanent magnets. When mounted on the engine block of a car, the second prototype device produced an average power of 157 $\mu$W and a peak power of 3.9 mW.

Research in capacitive electric energy harvesting focuses on two general areas: the variable capacitor itself and the power electronic circuitry that processes the converted energy. Miao et al fabricated and conducted tests on a micro electro-mechanical system (MEMS) capacitor that can vary its capacitance from 1 pF to 100 pF [10]. In a single charge-constrained cycle (refer to Chapter 2), this variable capacitor is capable of producing 24 $\mu$W of power using a 10 Hz vibration. However, they do not show results from actual supporting power electronics circuitry, so the overall energy harvesting ability of the system is unknown.

Mur-Miranda conducted extensive research, using both a variable capacitor macro model machined from blocks of aluminum and a MEMS capacitive comb drive transducer, on an electric energy harvesting circuit topology that exploited the charge-constrained cycle [11]. Using a bread-board prototype that implemented both the power electronics and the gate driver control circuitry for the active devices, he demonstrated energy conversion from the vibrational source and showed that output waveforms matched theoretical calculations. Due to the inefficiencies of the power electronics circuit used, however, the converted energy could not be translated back
as a gain in voltage at a storage capacitor.

Recently, Miyazaki et al reported a prototype vibration-to-electric variable capacitor energy converter that exhibited a measured power generation of 120 nW [12]. The power electronics used in this experiment resembled that used by Mur-Miranda; two complementary MOSFET switches regulate the flow of current through an inductor to charge and discharge the variable capacitor during specific portions of a mechanical cycle. The measured conversion efficiency of this prototype comes out to 21%. As Section 3.8 will show, however, the clock signal driving the MOSFET switches can inadvertently inject energy into the system, and because measurements relating to such injection are not available within this paper, it is unknown what fraction of the “harvested” energy actually came from the vibration source.

From the above literature search, one sees that most fully functional state of the art energy harvesting systems fall into the piezoelectric and magnetic regimes. The only working prototype for a capacitive electric energy scavenging system comes from Miyazaki et al as described in the preceding paragraph, but because possible clock injection issues did not receive attention there, a more thorough investigation is warranted. This reason, added to the fact that piezoelectric film can harm the environment and magnetic systems are relatively bulky, paves way for further research into the capacitive electric energy harvesting scheme.

1.4 Chapter Summary

This chapter served both as an introduction to the world of energy harvesting as well as motivation for the rest of this thesis. As noted, numerous techniques exist for harvesting energy from the environment that otherwise would have been lost. Potential energy sources include solar power, thermal and chemical gradients, acoustic noise, and vibration. Vibrational energy harvesting can be furthered divided into piezoelectric, magnetic, and electric, depending on how vibration energy is coupled into the
system. All are active areas of research, but this thesis will focus on the variable capacitor electric conversion process. Emphasis will be placed on the electronics and circuit topologies as opposed to the implementation of the variable capacitor using MEMS.

Chapter 2 provides the reader with a review of capacitive electric energy harvesting, sufficient to understand the theoretical, simulation, and experimental results that follow. Related laboratory measurement techniques will also be discussed. Chapter 3 outlines critical HSPICE simulation results that lead directly to a final design of the energy harvesting circuit topology, one of the main goals of this thesis. Then, in Chapter 4, experimental data based on a fabricated circuit board is presented and compared with computer simulations. Chapter 5 summarizes the thesis and its conclusions, and presents possible directions for future work in this area of research.

If the reader has access to HSPICE and wishes to modify certain design parameters and observe the effect they have on conversion efficiency, refer to Appendix (A) for the complete set of HSPICE decks. The model files of all the active components, which were downloaded off the Internet, are also included.
Chapter 2

Foundations of Energy Harvesting

As explained in Chapter 1, there exists a broad array of techniques for energy harvesting, of which piezoelectric, electric, and magnetic are perhaps the most prominent. Based on the specific harvesting strategy used, electric and magnetic energy scavenging can be further divided into two subcategories each. Capacitive electric energy harvesting, the main focus of this thesis, usually relies on either charge-constrained or voltage-constrained cycles, both of which will be fully explained below. Although methodologies that fall between these two are also theoretically possible, power electronics, switch-like in nature, rarely permit them.

In this chapter, the fundamentals behind electric energy harvesting will be explored. Mathematics relating contours in the Q-V plane to the amount of harvested energy per cycle are covered first, followed by a direct application of the formulated concepts to a charge-constrained circuit topology presented in [11]. An alternative topology based on self-synchronous diodes, which forms the centerpiece of this thesis, is shown next, along with detailed equations that model the charge flow on the variable capacitor and explain the impact of parasitic diode capacitances. Once the charge pump portion of the capacitive energy harvester has been developed, an energy flyback mechanism will be added and analyzed, and the pros and cons for various flyback techniques will be discussed. The chapter concludes with important labora-
tory concepts relevant to the characterization of energy harvesting circuits, including methods of measuring the AC capacitance of a variable capacitor.

By the end of the chapter, an idealized capacitive energy harvesting circuit with inductive flyback will have been developed, although decisions on the specific component values will be left for Chapter 3. The chosen topology forms the basis upon which the simulations carried out in the next chapter will be based; further improvements to the circuit will curb the problem of clock energy injection, but the main topology will not change.

2.1 The Q-V plane

Consider a single capacitor with capacitance $C$ and voltage $v_C$. At any given time, the energy stored on the capacitor can be expressed as

$$W_C = \frac{1}{2} C v_C^2 = \frac{1}{2} Q v_C,$$

where $Q = C v_C$ from fundamental physics. In a physical system, $Q$, $v_C$, and $C$ can vary as a function of time. For argument purpose, assume that the distance between the capacitor plates is variable, implying that $C$ can change. If we plot $Q$ and $v_C$ values parametrically over time in a Q-V plane as $C$ goes from a maximum value to a minimum value and back up, a graph similar to Fig. 2-1 will result. Note that the two contours shown in this figure represent typical cases; numerous circuit topologies produce contours dissimilar to both.

Notice that the slope of lines $A$ and $C$ in both diagram represents the capacitance value in that duration of the cycle. In drawing these figures, an implicit assumption is made that the capacitor charging (path $A$) and discharging (path $C$) occur much faster than the rate at which the capacitance changes. Were this not true, path $A$ and $C$ would not be straight lines. Finally, note that a “short” path does not imply
Enclosed area representing net converted energy in one cycle.

(a) Charge-constrained

(b) Voltage-constrained

Figure 2-1: Two typical electric energy conversion cycles.

that the time duration associated with that path is short; in fact, path B in both cases takes the longest time to traverse.

The distinction between the two cycle, one charge-constrained and one voltage-constrained, depends on which variable, \( Q \) or \( V \), is held fixed during the time when the capacitance value drops from maximum to minimum. For circuits where the variable capacitor is disconnected when the circuit traverses path B, Fig. 2-1(a) shows that the charge on the capacitor plates remains fixed as the capacitance decreases. On the other hand, for circuits that connect the capacitor to a voltage source during path B, Fig. 2-1(b) illustrates the capacitor voltage remains fixed as the capacitance drops.

Now, consider the area enclosed by path A-B-C in each case. For the charge-constrained cycle,

\[
W_{\text{CHARGE}} = \frac{1}{2} Q_O \Delta v_C \tag{2.2}
\]

where \( Q_O \) represents the amount of constrained charge on the capacitor plates when the plates move apart. For the voltage constrained cycle,

\[
W_{\text{VOLTAGE}} = \frac{1}{2} \Delta Q v_{C,O} \tag{2.3}
\]
where \( v_{C,O} \) represents the constrained voltage when the plates move apart. Comparing Eq. (2.2) and Eq. (2.3) with Eq. (2.1), it is seen that the enclosed area exactly represents the net energy gained by the capacitor in one cycle [13]. Therefore, the primary goal of a well designed energy harvesting circuit is to increase the amount of area surrounded by path A-B-C while retaining high conversion efficiency and the ability to operate asynchronously.

### 2.2 A Synchronous Charge-Constrained Circuit

Fig. 2-2 shows an example of a circuit topology that employs the charge-constrained energy harvesting technique described earlier [11]. Assume that the current through the inductor starts at 0 A and that \( C_{\text{VAR}} \), initially at its maximum value \( C_{\text{MAX}} \), is uncharged. At the beginning of a cycle, \( M_1 \) turns on, resulting in \( i_L \), the current in the inductor, ramping up according to \( v_L = L \frac{di_L}{dt} \). When \( i_L \) reaches a desired value, \( M_1 \) is turned off by the control circuitry and \( M_2 \) is simultaneously turned on. Because of the continuity of \( i_L \), \( C_{\text{VAR}} \) begins to charge up all the while staying at a capacitance value of \( C_{\text{MAX}} \); the mechanical cycle is assumed to be much longer than the electrical charging and discharging.

Once \( i_L \) reaches 0 A, the control circuitry turns \( M_2 \) off, resulting in \( C_{\text{VAR}} \) being isolated from the rest of the circuit. Therefore, as vibrational force causes \( C_{\text{VAR}} \) to
move apart and reach $C_{\text{VAR}} = C_{\text{MIN}}$, an energy harvesting cycle is carried out. The harvested energy can be transferred back to $C_{\text{RES}}$ through a reverse cycle of inductor charging and discharging.

There are several disadvantages to this topology, however. Perhaps the most important are the need for accurate transistor turn-on and turn-off, power consumption in the control electronics, and excessive conduction loss. Preliminary simulations in HSPICE not presented in this work indicate a necessity to hit the turn-on and turn-off points precisely in order to convert energy efficiently. For example, during the charging phase of $C_{\text{VAR}}$, $M_2$ must turn off as soon as $i_L$ reaches 0 A, or else it is possible for resonance between the capacitors and inductor to ring $v_{\text{VAR}}$ down again. However, if $M_2$ turns off too early, parts of the charge extracted from $C_{\text{RES}}$ to ramp up $i_L$ will be wasted. There are similar considerations for the second half of the cycle in which the harvested energy is transferred back to $C_{\text{RES}}$. Such precisions in the gate drive signals are difficult to achieve due to the delay between the detection of zero crossing points in $i_L$ and the toggling of the MOSFET switches, which can result in limited conversion efficiency.

Power consumed in driving the MOSFET switches of this topology can be quite large, due to the complexity of accurately controlling two active devices. In an autonomous sensor IC, this power consumption would directly lower the amount of stored energy available to drive the energy harvester load. A circuit topology that requires only one active device is preferred since its gate drive electronics can be implemented with much less complexity, resulting in decreased power usage.

Finally, there is a severe disadvantage when conduction loss is considered. In the two transistor topology, current flows through $M_1$, $M_2$, $M_2$, and $M_1$ respectively, amounting to 4 transistor conduction losses every scavenging cycle. Given that such conduction losses are comparable in magnitude to the amount of energy harvested, this charge-constrained circuit topology is not desirable.

To overcome these flaws, an asynchronous capacitive electric energy harvesting
2.3 The Asynchronous Topology: An Overview

Fig. 2-3 illustrates the building blocks of an asynchronous energy harvesting circuit. The heart of this circuit lies in the charge pump, formed from two diodes and a variable capacitor, that converts vibration energy into electric energy by moving charges from reservoir onto the variable capacitor and pushing energized charges into a temporary energy storage. Both the reservoir and temporary storage consists of a single capacitor. The flyback mechanism insures that the voltage at the reservoir is maintained while the load draws power from the reservoir.

First, the charge pump block, connected to the reservoir and temporary storage capacitors, is examined alone. Consider the circuit shown in Fig. 2-4, which includes 3 capacitors and 2 diodes. In Chapter 3, the precise operation of this circuit will be explored. For now, an intuitive understanding is developed. Assume that the capacitor starts at its maximum possible value and that all three capacitors are charged to
Because all the node voltages are equal, diodes $D_1$ and $D_2$ are both off. Now, through an external means such as vibrational motion, the capacitor plates are moved apart, causing $C_{VAR}$ to drop. Because the charge on the middle capacitor is constrained by two diodes that are off, a drop in capacitance implies that $v_{VAR}$ must rise to keep $Q = CV$ satisfied; this corresponds to path B in Fig. 2-1. This rise in voltage turns on $D_2$, resulting in $C_{VAR}$ partially discharging. Unlike path C, $C_{VAR}$ does not completely discharge into $C_S$ but stops when $v_{VAR} = v_S$. At this point, $D_2$ turns off.

Now, as the capacitor plates move back towards each other, again due to an external force, the cycle is also charge-constrained because both $D_1$ and $D_2$ are off. As $C_{VAR}$ increases, $v_{VAR}$ drops, forcing $D_1$ to turn on and resulting in a partial charging of the variable capacitor. This corresponds roughly to path A. The charging of the capacitor causes $v_{VAR}$ to rise, eventually turning off $D_1$ and returning the circuit to its starting point. Thus, this circuit acts as a charge pump from $C_{RES}$ to $C_S$, adding net stored energy to the capacitor over time.

2.4 Limitations Without Flyback

As more and more energy conversion cycles are carried out, $C_S$ in Fig. 2-4 begins to accumulate large amounts of charge. Eventually, $v_S$ rises so high that the variation in $C_{VAR}$ is unable to pump more charge to $C_S$; equivalently, charge can no longer flow from $C_{RES}$ onto $C_{VAR}$. The maximum $v_S$ given a certain variation in $C_{VAR}$ will
now be explored using a cycle-to-cycle iteration process. For the first pass of the derivation, ideal diodes are used, meaning that the forward voltage drop is $V_D = 0 \text{ V}$, the parasitic diode capacitance is $C_D = 0 \text{ F}$, and the reverse bias leakage current coefficient is $I_S = 0 \text{ A}$.

Assume that the variation limits of $C_{VAR}$ are such that $C_{MIN} \leq C_{VAR} \leq C_{MAX}$ and that $v_{VAR} = v_{RES}$ (i.e. diode $D_1$ has just equalized the voltage between the reservoir and the variable capacitor). Define a complete energy harvesting cycle as the time in which $C_{VAR}$ undergoes one capacitance variation from maximum to minimum back to maximum; take $v_{S,i}$, where $i$ is an integer index starting at 0, to represent the voltage on $C_S$ when $C_{VAR} = C_{MAX}$. Finally, since the variation on $C_{RES}$ is so small, represent the reservoir capacitor as a constant voltage source.

Fig. 2-5(a) shows the equivalent circuit diagram at the start of cycle $n-1$. At this point, the total capacitor charge on $C_{VAR}$ and $C_S$ is

$$Q_{total} = C_{MAX}v_{RES} + C_{S}v_{S,n-1}.$$  \hfill (2.4)

Now consider the variable of interest in the next cycle, namely $v_{S,n}$. It is easy to see that $v_S$ does not change once $D_2$ stops conducting, so analyzing this portion of the circuit operation when $C_{VAR}$ drops in value and $v_{VAR}$ increases in value is sufficient. The point where $C_{VAR} = C_{MIN}$ is shown in Fig. 2-5(b).

Because $D_1$ does not conduct when $v_{VAR} > v_{RES}$, charge-constrained operation
dictates that $Q_T = Q_{VAR} + Q_3$ is constant, giving

$$v_{S,n} = \frac{C_S}{C_{MIN} + C_S} v_{S,n-1} + \frac{C_{MAX}}{C_{MIN} + C_S} v_{RES}$$

(2.5)

when $C_{VAR} = C_{MIN}$. Furthermore, initial condition gives $v_{S,0} = v_{RES}$.

Define $\alpha = \frac{C_S}{C_{MIN} + C_S}$ and $\beta = \frac{C_{MAX}}{C_{MIN} + C_S} v_{RES}$. Eq. (2.5) can then be written as

$$v_{S,n} = \alpha v_{S,n-1} + \beta,$$

(2.6)

which is a recurrence relation in variable $v_{S,n}$. Such a recurrence relation can be solved by determining the homogeneous and particular solution for the associated recurrence equation

$$r^n = \alpha r^{n-1} + \beta,$$

(2.7)

which is obtained by substituting $r^i = v_{S,n}$ into Eq. (2.6). The homogeneous solution must satisfy

$$r^n = \alpha r^{n-1},$$

(2.8)

and therefore by inspection,

$$v_{S,n}^{(h)} = K \alpha^n.$$

(2.9)

From Eq. (2.7), one particular solution that works is

$$v_{S,n}^{(p)} = \frac{\beta}{1 - \alpha},$$

(2.10)

which, when combined when the homogeneous solution and simplified, results in

$$v_{S,n} = v_{S,n}^{(h)} + v_{S,n}^{(p)} = K \left( \frac{C_S}{C_{MIN} + C_S} \right)^n + C_{MAX} \frac{C_{MIN}}{C_{MIN}} v_{RES}.$$

(2.11)

Now, using the initial condition $v_{S,0} = v_{RES}$,

$$K = v_{RES} \left( 1 - \frac{C_{MAX}}{C_{MIN}} \right)$$

(2.12)
and so the cycle-to-cycle variation of the storage node voltage is

\[ v_{S,n} = v_{RES} \left[ \left(1 - \frac{C_{\text{MAX}}}{C_{\text{MIN}}} \right) \left( \frac{C_{S}}{C_{\text{MIN}} + C_{S}} \right)^n + \frac{C_{\text{MAX}}}{C_{\text{MIN}}} \right]. \]  \hspace{1cm} (2.13)

To check that Eq. (2.13) makes sense, substitute the extreme case of \( n = 0 \) to obtain

\[ v_{S,0} = v_{RES} \]  \hspace{1cm} (2.14)

as expected from the initial condition. To determine the voltage limit on the storage capacitor without the flyback block illustrated in Fig. 2-3, plug in \( n = \infty \) to obtain

\[ v_{S,\infty} = \frac{C_{\text{MAX}}}{C_{\text{MIN}}} v_{RES}. \]  \hspace{1cm} (2.15)

Eq. (2.15) interestingly indicates that the maximum storage on \( C_S \) depends on the ratio of \( C_{\text{MAX}} \) to \( C_{\text{MIN}} \). Because the efficiency of the energy harvester will inevitably hinge upon the maximum temporary energy storage capacity, it is reasonable to explore Eq. (2.15) in more detail. Writing out the terms, the equation becomes

\[ v_{S,\infty} = \frac{C_{\text{DC}} + C_{\text{AC}}}{C_{\text{DC}} - C_{\text{AC}}} v_{RES} \]  \hspace{1cm} (2.16)

where \( C_{\text{AC}} \) indicates the positive zero-to-peak magnitude of the capacitance variation. From Eq. (2.16), it is apparent that given a fixed \( C_{\text{AC}} \), a smaller \( C_{\text{DC}} \) will allow \( v_S \) to reach a higher ultimate value. Hence, minimizing parallel parasitic capacitances becomes a design goal for this particular circuit topology.

Having worked out the circuit behavior using ideal diodes, now consider the situation when the diode’s junction capacitance \( C_1 \) is included. The modified circuit diagram is shown in Fig. 2-6. In order to understand the behavior of this non-ideal circuit, one cycle needs to be divided up into five stages: \( D_2 \) closed, \( D_1 \) and \( D_2 \) opened, \( D_1 \) closed, \( D_1 \) and \( D_2 \) opened, and \( D_2 \) closed again. For the equivalent circuit diagram of each stage, refer to Fig. 2-7. Note that the ordering of the stages is
slightly different compared to the ideal case analysis. Here, the cycle begins with $D_2$ on instead of $D_1$ on. In Stage 1, the amount of charge stored on $C_S$ is

$$Q_{S,n-1} = C_S v_{S,n-1}.$$

(2.17)

Now, as the capacitance begins to increase from $C_{\text{MIN}}$, assume, without loss of generality, that $D_2$ turns off first before $D_1$ turns on; this brings the circuit into Stage 2. From Stage 1 to Stage 2, the amount of charge at node X is conserved. Paying attention to the polarity of charge on $C_{32}$ and $C_S$ carefully, one can write that

$$Q_S - Q_{J2} = C_S v_{S,n-1}.$$

(2.18)

As the capacitor plate moves apart and $C_{\text{VAR}} = C_{\text{MAX}}$, $D_1$ turns on and the circuit enters Stage 3. At this moment, $v_{\text{VAR}} = v_{\text{RES}}$, so by Kirchhoff’s Voltage Law,

$$v_S + v_{J2} = v_{\text{RES}}$$

(2.19)

$$\frac{Q_S}{C_S} + \frac{Q_{J2}}{C_{J2}} = v_{\text{RES}}.$$

(2.20)

Multiplying Eq. (2.18) through by $C_S$,

$$Q_S C_S - Q_{J2} C_S = C_S^2 v_{S,n-1}.$$

(2.21)
which, when substituted into Eq. (2.20), gives

\[ Q_S C_{J2} + Q_S C_s - C_s v_{S,n-1} = v_{RES} C_S C_{J2} . \]  

(2.22)

Hence, \( Q_S \), the amount of charge on the storage capacitor during Stage 3, is

\[ Q_S = \frac{v_{RES} C_S C_{J2} + C_s^2 v_{S,n-1}}{C_s + C_{J2}} . \]  

(2.23)

At the same time, the amount of charge on \( C_{VAR} \) is

\[ Q_{VAR} = C_{MAX} v_{RES} . \]  

(2.24)

Now, again without loss of generality, assume that \( D_1 \) opens before \( D_2 \) turns on, resulting in charge conservation for both node X and Y in Fig. 2-7(d). This is Stage 4
of the circuit operation. Defining $Q_{J2}$ as the amount of charge on $C_{J2}$, the total charge on all capacitors sums to

$$Q_{\text{TOT}} = (Q_S - Q_2) + (Q_{\text{VAR}} + Q_2) = Q_S + Q_{\text{VAR}} ,$$

where $Q_S$ and $Q_{\text{VAR}}$ are defined in Eq. (2.23) and Eq. (2.24).

Finally, $D_2$ turns on as $C_{\text{VAR}}$ drops to its minimum value once more. The charge at node $Z$ is equivalent to the sum of the charges at node $X$ and $Y$ in Stage 4. Therefore, by distributing $Q_{\text{TOT}}$ across the 3 capacitors and solving for $v_{S,n}$, one obtains that

$$v_{S,n} = \frac{C_S^2}{(C_S + C_{J2})(C_{J1} + C_{\text{MIN}} + C_S)}v_{S,n-1} + \frac{C_{J1} + C_{\text{MAX}} + \frac{C_{J2}C_S}{C_{J2} + C_S}}{C_{J1} + C_{\text{MIN}} + C_S}v_{\text{RES}} .$$

Defining

$$\alpha = \frac{C_S^2}{(C_S + C_{J2})(C_{J1} + C_{\text{MIN}} + C_S)}$$

and

$$\beta = \frac{C_{J1} + C_{\text{MAX}} + \frac{C_{J2}C_S}{C_{J2} + C_S}}{C_{J1} + C_{\text{MIN}} + C_S}v_{\text{RES}} ,$$

Eq. (2.26) can be rewritten as

$$v_{S,n} = \alpha v_{S,n-1} + \beta ,$$

which is similar to Eq. (2.6) except for the definition of $\alpha$ and $\beta$. The technique for solving recurrence relation used earlier in the ideal energy harvesting cycle can be directly applied here. In the end,

$$v_{S,n}^{(h)} = K \left( \frac{C_S^2}{(C_S + C_{J2})(C_{J1} + C_{\text{MIN}} + C_S)} \right)^n$$

$$v_{S,n}^{(p)} = \left( \frac{(C_S + C_{J2})(C_{J1} + C_{\text{MAX}} + \frac{C_{J2}C_S}{C_{J2} + C_S})}{(C_{J1} + C_{J2})C_S + (C_{J2} + C_S)C_{\text{MIN}} + C_{J1}C_{J2}} \right)v_{\text{RES}} .$$
Using the initial condition and defining

\[ \gamma = \frac{(C_S + C_{12})(C_{31} + C_{\text{MAX}} + \frac{C_{12}C_S}{C_{12} + C_S})}{(C_{31} + C_{12})C_S + (C_{12} + C_S)C_{\text{MIN}} + C_{31}C_{12}}, \]  

(2.32)

the full cycle-to-cycle variation in the storage capacitor voltage is

\[ v_{S,n} = [(1 - \gamma)\alpha^n + \gamma]v_{\text{RES}}. \]

(2.33)

Again, check the derived equation with an extreme case of \( n = 0 \). Here, \( v_{S,0} = v_{\text{RES}} \), which is consistent with the initial condition. Since \( \alpha < 1 \), substitute \( n = \infty \) to yield

\[ v_{S,\infty} = \gamma v_{\text{RES}}. \]

(2.34)

Grouping terms on the numerator and denominator of Eq. (2.34) makes it apparent that the voltage limit on the storage capacitor is significantly smaller compared to the ideal case. Hence, energy harvesting efficiency goes down with increasing \( C_{31} \) and \( C_{12} \), which indicates that diodes with small parasitics are preferred. As \( C_{31} \) and \( C_{12} \) approaches 0, \( v_{S,\infty} \) approaches \( \frac{C_{\text{MAX}}}{C_{\text{MIN}}}v_{\text{RES}} \); this makes sense because diodes without parasitic junction capacitance are ideal diodes.

### 2.5 Energy Flyback Technique

So far, the charge pump has been analyzed as a standalone block. However, as seen from the previous section, the energy harvesting cycle becomes less efficient as charge builds up on the storage capacitor \( C_S \). Furthermore, referring back to Fig. 2-3, the load is attached to \( C_{\text{RES}} \) instead of \( C_S \). In this thesis, the load comprises of a 10 MΩ scope probe measuring \( v_{\text{RES}} \) in series with another 10 MΩ resistor. Therefore, flying the converted energy back into a reservoir capacitor that satisfies \( C_{\text{RES}} \gg C_S \) must occur as part of the circuit operation.
Broadly speaking, there are two main methods of energy flyback: inductive and capacitive. Inductive flyback, shown in Fig. 2-8 without parasitic components, operates by first ramping up the current in $L_{FB}$ using a voltage difference across the inductor. Then, at a later time, the inductive path is disconnected by means of a transistor switch, forcing current to “freewheel” through $D_{FB}$ in the second half of the flyback cycle. Topologically, the inductive flyback portion of Fig. 2-8 looks remarkably similar to a DC/DC buck converter. The main difference stems from the fact that in a buck converter, the main objective is to maintain a constant output voltage $v_{OUT}$ while the circuit here deliberately tries to pull $v_{RES}$ up as efficiently as possible.

Theoretically, the efficiency of such a flyback system can reach 100%, but due to parasitic core and wire loss in the inductor as well as conduction and switching loss in the MOSFET and diodes, part of the energy is lost. For now, ignore the non-idealities of the inductor and focus on the conduction loss. Chapter 3 will provide justification as to why inductor parasitics prove to be non-critical. Assume that the CLK signal is high enough to force the MOSFET into the triode region. In this case, the conduction loss is resistive:

$$\langle P_{FET,COND} \rangle = \langle i_{FET}v_{FET} \rangle \approx i_{RMS}^2 R_{DS,ON}$$  \hspace{1cm} (2.35)$$

where $R_{DS,ON}$ is the equivalent on-resistance of the MOSFET in triode region. On the other hand, because a diode exhibits constant forward bias voltage drop across
In summary, the root-mean-square current is important for a transistor while the average current is important for a diode. The total energy lost per cycle of an inductive flyback circuit is therefore

\[
W_{\text{loss}} = i_{\text{FB}}^2 R_{\text{DS,ON}} \frac{D}{f_{\text{FB}}} + (i_D) v_D \frac{1 - D}{f_{\text{FB}}} \tag{2.37}
\]

with \(f_{\text{FB}}\) representing the frequency at which the flyback portion of the energy harvesting circuit operates and \(D\) representing the duty ratio of the MOSFET.

For a capacitive flyback strategy, such as that shown in Fig. 2-9, the storage and reservoir capacitor are simply shorted together through a transistor at regular times during the circuit operation. Energy flyback occurs by way of voltage equalization between \(C_S\) and \(C_{\text{RES}}\); given that both \(D_1\) and \(D_2\) are off during the time of flyback, charge conservation along with the fact that \(v_S > v_{\text{RES}}\) results in \(v_{\text{RES}}\) increasing after the equalization. Mathematically, the total charge initially is

\[
Q_{\text{TOT,0}} = C_S v_S + C_{\text{RES}} v_{\text{RES}} \tag{2.38}
\]
and the total initial energy is

\[ W_{\text{TOT},0} = \frac{1}{2} C_s v_s^2 + \frac{1}{2} C_{\text{RES}} v_{\text{RES}}^2. \]  

(2.39)

When the circuit reaches steady state operation after the MOSFET has been turned on, the voltage on the capacitors equalizes to a final value \( v_F \). However, charge is conserved, leading to

\[ Q_{\text{TOT},F} = (C_s + C_{\text{RES}}) v_F = Q_{\text{TOT},0} \]  

(2.40)

\[ W_{\text{TOT},F} = \frac{1}{2} (C_s + C_{\text{RES}}) v_F^2 \]  

(2.41)

with \( v_F \) determined from Eq. (2.38) and Eq. (2.40) to be

\[ v_F = \frac{C_s v_s + C_{\text{RES}} v_{\text{RES}}}{C_s + C_{\text{RES}}}. \]  

(2.42)

Therefore, the amount of energy lost per capacitive flyback cycle is

\[ W_{\text{LOSS}} = W_{\text{TOT},0} - W_{\text{TOT},F} = \frac{1}{2} \left( \frac{C_s C_{\text{RES}}}{C_s + C_{\text{RES}}} \right) (v_s - v_{\text{RES}})^2, \]  

(2.43)

which increases in magnitude as the voltage difference between the reservoir and storage node increases. Note that in contrast with the inductive flyback loss, the capacitive strategy energy loss is independent of the \( f_{\text{FB}} \). Despite this independence, inductive flyback is still superior to capacitive flyback given typical component values.

## 2.6 Bucket Brigade Capacitive Flyback

The reader might wonder whether using multiple capacitors in the flyback path will increase the efficiency of energy flyback. An example of such a flyback circuit is shown in Fig. 2-10. In this diagram, \( W_{\text{IN}} \), the energy being fed into the system, comes from the vibrational source and \( W_{\text{OUT}} \), the energy being taken out, goes into the reservoir.
Imagine \( C_1 \) as the storage capacitor \( C_s \) and the voltage source \( v_{\text{RES}} \) as the reservoir capacitor \( C_{\text{RES}} \).

In order to calculate the energy flyback efficiency of this setup, the periodic steady state (PSS) condition must first be determined. PSS denotes the situation in which all the circuit state variables (i.e., voltages and currents) return to the same value after every cycle of circuit operation. In this case, a complete cycle involves the variable capacitor's capacitance going from maximum to minimum back to maximum, or equivalently, a single \( W_{\text{IN}} \) injection.

The exact calculations involved in deriving the PSS condition of an \( n \)-capacitor bucket brigade is extremely involved and offers no additional insight into the circuit operation. Therefore, a more intuitive approach is offered. First assume all capacitors are equivalent, meaning that \( C_1 = C_2 = \ldots = C_{n-2} = C_{n-1} = C \). Consider any capacitor \( C_i, 1 < i < n - 1 \), that is sandwiched between two other neighboring capacitors. When the switch on its left, \( S_{i-1,i} \), closes, \( v_i \) equalizes with \( v_{i-1} \) and reaches some intermediate voltage between the two original values. Then, when the switch on the right, \( S_{i,i+1} \), closes, \( v_i \) equalizes with \( v_{i+1} \) and reaches a different intermediate voltage. But these two operations are exactly equivalent to averaging the center voltage with its two neighboring voltage, so one would expect that after many cycles, the progression of \( v_1, v_2, \ldots, v_{n-2}, v_{n-1} \) becomes linear and evenly spaced.

In fact, that is exactly what happens for a bucket brigade of capacitors in PSS.
The PSS voltage on each capacitor can be expressed as

\[ v_i = v_1 - (i - 1) \frac{v_{1} - v_{\text{RES}}}{n - 2}. \]  \hfill (2.44)

Having determined the PSS condition, the energy flyback efficiency analysis can proceed. The steps in determining \( \eta \) where \( \eta = \frac{W_{\text{OUT}}}{W_{\text{IN}}} \) is as follows:

1. Begin with PSS capacitor voltages on the \( k \)-th energy flyback cycle of \( v_{1(k)}, v_{2(k)}, \ldots, v_{n-2(k)}, \) and \( v_{n-1(k)} \).

2. Inject \( W_{\text{IN}} \) into the system at \( C_1 \).

3. One at a time, turn switches \( S_{1,2}, S_{2,3}, \ldots, S_{n-2,n-1}, \) and \( S_{n-1,n} \) on then off. Denote this as the switch rippling stage.

4. Determine \( v_{1(k+1)}, v_{2(k+1)}, \ldots, v_{n-2(k+1)}, \) and \( v_{n-1(k+1)} \) and require that \( v_{i(k+1)} = v_{i(k)} \) for all \( i \) such that \( 1 \leq i \leq n - 1 \).

During Step 1, the amount of energy stored on \( C_1 \) is

\[ W_{1,0} = \frac{1}{2} C v_{1,0}^2 = \frac{Q_{1,0}^2}{2C} ; \]  \hfill (2.45)

all the capacitance values are simply \( C \) since they are assumed to be equal, as mentioned earlier. After Step 2, the total energy stored on \( C_1 \) becomes

\[ W_{1,0} = \frac{Q_{1,0}^2}{2C} + W_{\text{IN}} = \frac{Q_{1,F}^2}{2C} , \]  \hfill (2.46)

which, when multiplied through with \( 2C \) and simplified, gives

\[ Q_{1,F} = \sqrt{Q_{1,0}^2 + 2CW_{\text{IN}}} . \]  \hfill (2.47)

Finally, this allows the change in \( Q_1 \) to be calculated:

\[ \Delta Q_1 = Q_{1,F} - Q_{1,0} = \sqrt{Q_{1,0}^2 + 2CW_{\text{IN}}} - Q_{1,0} . \]  \hfill (2.48)
Because all capacitor voltages must return to their original values \( v_{i(k)} \) after Step 3 and 4, the entire \( \Delta Q_1 \) must ripple all the way through and exit into the voltage source \( v_{\text{RES}} \). Therefore, \( W_{\text{OUT}} \) can be determined as

\[
W_{\text{OUT}} = \Delta Q_1 v_{\text{RES}} = \left( \sqrt{Q_{1,0}^2 + 2C W_{\text{IN}} - Q_{1,0}} \right) v_{\text{RES}}.
\] (2.49)

The only thing necessary before characterizing \( \eta \), the efficiency of a bucket brigade energy flyback circuit, is the value for \( Q_{1,0} \). This charge can be obtained by examining the voltage equalization between \( C_1 \) and \( C_2 \) more closely. From Eq. (2.44),

\[
v_{2,\text{PSS}} = v_{1,0} - \frac{v_{1,0} - v_{\text{RES}}}{n - 2}
\] (2.50)

where \( v_{2,\text{PSS}} \) means the PSS voltage on \( C_i \). Denote the voltage on \( C_1 \) before Step 2 as \( v_{1,0} \) and the voltage after Step 2 as \( v_{1,F} \). This gives

\[
\frac{1}{2} C v_{1,F}^2 = \frac{1}{2} C v_{1,0} + W_{\text{IN}}
\] (2.51)

\[
v_{1,F} = \sqrt{v_{1,0}^2 + \frac{2W_{\text{IN}}}{C}}.
\] (2.52)

After Step 3 when the switch is closed, the final voltage is the average of \( v_{1,F} \) and \( v_{2,\text{PSS}} \) since the capacitors are equal in value. But this final voltage will be the ultimate voltage on \( C_1 \) during this cycle since the switch opens after equalization occurs. In order to satisfy PSS,

\[
\frac{1}{2} v_{1,F} + \frac{1}{2} \left( v_{1,0} - \frac{v_{1,0} - v_{\text{RES}}}{n - 2} \right) = v_{1,0}.
\] (2.53)

Substituting Eq. (2.52) into Eq. (2.53) and simplifying,

\[
v_{1,0} = \frac{-2(n-1)v_{\text{RES}} - \sqrt{4(n-1)^2 v_{\text{RES}}^2 - 4\alpha (-2n+3)}}{-4n+6}
\] (2.54)

where \( \alpha = \frac{2}{C} (n-2)^2 W_{\text{IN}} - v_{\text{RES}}^2 \). Note that the negative solution for the quadratic equation was selected since \( v_{1,0} > 0 \). The required expression for \( Q_{1,0} \) is simply
Figure 2-11: Flyback efficiency versus number of bucket brigade capacitors.

\[ Q_{1,o} = C v_{1,o}. \] Finally, referring back to Eq. (2.49), \( \eta \) is

\[
\eta \equiv \frac{W_{\text{OUT}}}{W_{\text{IN}}} = \frac{\sqrt{Q_{1,o}^2 + 2C W_{\text{IN}} - Q_{1,o}}}{} \cdot v_{\text{RES}}.
\] (2.55)

Substituting in the expression for \( Q_{1,o} \) into Eq. (2.55) and plotting the result in MathCAD, one obtains an efficiency versus \( n \) plot, which is shown in Fig. 2-11. The efficiency decreases as the number of capacitors increases. Note that because the derivation is invalid for \( n < 3 \), the section of the curve with \( \eta > 1 \) can be safely ignored.

From the above derivation, it is apparent that the use of a bucket brigade capacitive energy flyback is inferior to the solution of a direct flyback in which \( C_s \) is shorted to \( C_{\text{RES}} \) through the MOSFET. Another disadvantage of using such a flyback scheme is the large number of switches involved. Because these switches will be implemented using discrete transistors, each of them will exhibit conduction loss due to a finite \( R_{\text{ON}} \) value. Therefore, the actual efficiency will be much smaller than that predicted by the previous calculation.
In summary, the best flyback topology out of the three possible candidates — inductor, direct shorting switch, and capacitive bucket brigade — is the inductor. Not only does it possess the highest theoretical flyback efficiency relative to the other two mechanisms, the inductive flyback is also very simple to implement. The only major drawback comes from the inherent bulkiness associated with inductors, but because the design goals do not include minimizing the overall system size, the remainder of this thesis will use the inductive flyback topology.

2.7 Relevant Measuring Techniques

The AC variation of $C_{VAR}$ constitutes an important parameter to characterize accurately in the energy harvesting circuit. Such a circuit was proposed in [11] and will be repeated here for convenience. Consider the op-amp network shown in Fig. 2-12. There are two additional power line bypass capacitors not shown in the schematic; one is a 0.22 µF film capacitor connected between $v_+$ and ground while the other is a 1 nF capacitor connected between $v_+$ and $v_-$. If $\omega \ll \frac{1}{RC} = 100$ krad/s, the impedance in the flyback path can be approximated by $Z_{FB} \approx R = 100$ kΩ. Therefore, if the output voltage is approximately sinusoidal,
Figure 2-13: Circuit to accurately determine the DC value of a capacitor.

which is valid under the assumption that $C_{AC} \ll C_{DC}$, it can be expressed as

$$v_{OUT} = -i_{VAR} R$$  \hspace{1cm} (2.56)

Taking $C_{VAR} = C_{DC} + C_{AC} \sin(\omega t)$,

$$v_{OUT} = (10 \ V) \omega R C_{AC} \cos(\omega t)$$  \hspace{1cm} (2.57)

which implies that

$$C_{AC} = \frac{|v_{OUT}|}{(10 \ V) \omega R}$$  \hspace{1cm} (2.58)

Hence, by measuring the output voltage at specific frequencies, $C_{AC}$ can be determined as long as $\omega \ll \frac{1}{R C}$. Note that purpose of $C$ is to attenuate high frequency noise that can severely mask the output signal.

The DC capacitance of $C_{VAR}$ also is a parameter of interest. Usually, this value can be directly determined using a bridge circuit or a multimeter with capacitance measuring capability. If an alternative method is desired, the circuit topology shown in Fig. 2-13 can also be considered. This is nothing more than an impedance voltage divider where

$$\hat{V}_C = \frac{1}{1 + j \omega R C_{DC}} \hat{V}_S$$  \hspace{1cm} (2.59)

with the hatted variables representing complex amplitudes. Taking the magnitudes
of both side,

\[ |V_C| = \frac{V_S}{\sqrt{1 + (ωR C_{DC})^2}}. \]  \hspace{1cm} (2.60)

Finally, solving for \( C_{DC} \), one gets

\[ C_{DC} = \sqrt{\frac{(\frac{V_S}{V_C})^2 - 1}{ωR}}. \]  \hspace{1cm} (2.61)

As will be documented in Chapter 4, the circuits shown in Fig. 2-12 and Fig. 2-13 give \( C_{DC} = 650 \) pF and \( C_{AC,MAX} = 317.36 \) pF for the variable capacitor used in this thesis.

\[ \text{Chapter 2.8 Chapter Summary} \]

This chapter mapped out the theoretical foundations behind energy harvesting circuits, the most important one being the Q-V plane contours and their relationship to scavenged energy. Two typical capacitive conversion cycles were given — charge-constrained and voltage-constrained — and the circuit topology explored in [11] was given as an example employing charge-constrained cycles. However, due to the topology’s synchronous nature, excessive power consumption for the gate drive, and high conduction loss, it is undesirable as an energy harvester. An alternative topology based on an asynchronous diode charge pump connected to an energy flyback mechanism was proposed instead.

In order to sustain the efficiency of energy harvesting and to power the load connected at the reservoir, three possible flyback circuits were analyzed, including the inductor, direct shorting switch, and the capacitive bucket brigade. Although bulky, the inductive flyback allowed for maximum theoretical flyback efficiency, 100 %, and required few components to implement. Hence, the topology chosen for this thesis uses inductive flyback.
Comparing Eq. (2.15) and Eq. (2.34), it is apparent that parasitic diode capacitances hurt the overall conversion efficiency by decreasing the maximum voltage level $C_S$ can reach. This implies that diodes with low junction capacitance should be used for the charge pump. Furthermore, if the circuit is implemented on an IC, one must observe careful circuit layout techniques to avoid creating excessive parasitic capacitances.

The remaining chapters of this thesis builds upon the established foundations and examine second-order effects that are difficult to characterize analytically. Chapter 3 examines in greater details the effect of device parasitics through the use of HSPICE, a specialized circuit simulation program, and addresses energy flyback timing optimization. Chapter 4 presents experimental results from a PCB that was designed and optimized based on simulation results; the variable capacitor used will also be characterized.
Chapter 3

Circuit Simulation and Design

Although the theoretical foundations of electric energy harvesting laid out in the preceding chapter are important, a computer-based simulation nonetheless is necessary to pinpoint the most efficient circuit implementation. The discussion in Chapter 2 lacked specific component values, maximum tolerable parasitic sizes, and other important details necessary for the development of a successful prototype circuit board (PCB). In this chapter, results from various HSPICE simulations that comprehensively survey the effect of different design choices will be first presented; they will then lead to the formation of the actual circuit schematic upon which the final set of experimental data presented in Chapter 4 is based.

3.1 Creating the Variable Capacitor

Because HSPICE inherently does not provide an easy way of simulating mechanical variable capacitors with moving plates, the first task involves creating a circuit equivalent that can represent the vibrating plates accurately enough. Based upon the discussion in [14], a variable capacitor can be represented by a subcircuit consisting of a fixed value capacitor in series with a dependent source whose voltage depends on the...
voltage difference across the terminals of the subcircuit. Such a circuit configuration is shown in Fig. 3-1. The two-port impedance of this subcircuit is

\[
Z_{IN} \equiv \frac{V_{IN}}{I_{IN}} = \frac{1}{sC_{DC} (1 + A)} .
\]

Eq. (3.1) suggests that the subcircuit behaves equivalently to a capacitor that has capacitance \( C_{DC} (1 + A) \), which means that if \( A = \frac{C_{AC}}{C_{DC}} \sin (\omega t + \phi) \), the two-port model is precisely a variable capacitor with frequency \( \omega \), DC value \( C_{DC} \), AC amplitude \( C_{AC} \), and angle \( \phi \). Given the desired value for \( A \), the dependent voltage source \( Av_{IN} \) must have the value

\[
Av_{IN} = v_{IN} \frac{C_{AC}}{C_{DC}} \sin (\omega t + \phi) ,
\]

which is simply a multiplication of the two-port voltage, a sinusoidal excitation of amplitude 1, and a constant \( C_{AC}/C_{DC} \).

Such a dependent voltage source can be specified in HSPICE through the use of a polynomial function [15]; refer to Appendix (A) for the actual code implementing the variable capacitor subcircuit. Verification of the variable capacitor implementation involves attaching the subcircuit to a fixed voltage source \( V_S \) and gauging the amount of current flowing into the subcircuit. Defining \( C_{VAR}(t) = C_{DC} + C_{AC}(t) \), correct operation requires

\[
i_{IN} = \frac{d}{dt} (C_{VAR}(t)V_S) = V_S \frac{d}{dt} (C_{AC}(t)) .
\]
As an example, if $C_{DC} = 1.22 \, \text{nF}$, $C_{AC} = 300 \, \text{pF}$, and $V_s = 1 \, \text{V}$, the input current should be $i_{IN} = 3.58 \, \cos (2\pi \times 1900t) \, \mu\text{A}$. Computer simulation of the two-port input current, shown in Fig. 3-2, confirms that the subcircuit behaves correctly. Although shown with a sinusoidal variation, the capacitor model, through additional parameter fitting, can also accommodate non-linear mechanical effects.

### 3.2 Inductor Modeling

A real wire-wound inductor will inevitably have parasitic losses associated with it. Because the success of electric energy harvesting hinges upon high power conversion efficiency, parasitic resistances associated with wire loss and core loss must be accurately modeled. Capacitive effects, significant for radio frequency applications, will not be considered here since environmental vibration doing work on the electrical charges occur at much lower frequencies.
Characterization of the energy flyback inductor has been performed in [11] using a multimeter and a bridge instrument set at 300 kHz. The final model, with $R_C$ representing the core loss and $R_W$ representing the winding loss, is shown in Fig. 3-3. Extracted parameter values are $L = 2.5 \text{ mH}$, chosen to limit the rate of current ramping and prevent inductor saturation, $R_C = 360 \text{ k}$, and $R_W = 8 \Omega$ for the experimental circuit. Note that by modeling the core loss as a linear resistor, one implicitly disregards nonlinear loss mechanisms found in the inductor. Although not critical in the simulation phase, these second-order effects turn out to be important when a close fit between experimental data and simulation is desired. Refer to Chapter 4 for more details.

### 3.3 Power Devices

Because the amount of energy harvested from the vibrational source is on the order of several $\mu$W, power electronic components in the circuit, including diodes and MOSFETs, also require accurate modeling to insure that the associated losses do not exceed the converted energy. To model the components with precision, they must first be selected. As with most circuits processing power, diodes exhibiting nearly ideal behaviors are desirable; this translates to a low forward bias voltage drop, small parasitic resistance and capacitance, as well as low reverse bias leakage. Based on these limitations, the 1N6263 Schottky barrier diode was selected. As will become evident later from simulation results, the best MOSFET for energy harvesting should have low on-resistance, small parasitic gate capacitance, and a weak body diode. These
requirements lead to the selection of a 2N7002 n-channel MOSFET for use in this circuit.

Buermen extracted the appropriate HSPICE parameters for the 1N6263 Schottky barrier diode in [16]; Vishay, a company specializing in semiconductor devices, generated the HSPICE model for the 2N7002 n-channel MOSFET. Briefly, the Schottky barrier diode model contains two diodes, each with its own set of parameters, in parallel; one of them serves as a parasitic component. The n-channel MOSFET model accounts for parasitic p-channel MOSFET, gate capacitance, and the body diode. For the complete model files, refer to Appendix (A).

3.4 Oscilloscope Probes

As will be shown in simulations later during this chapter, the parasitic resistance presented to the circuit due to the presence of oscilloscope probes can significantly affect the energy conversion efficiency. In an extreme case, a simulation that results in positive converted energy can see its reservoir voltage collapse when a 10 MΩ equivalent probe resistance is included as a load.

The significant problems posed by the scope probes arise because they form unexpected current paths through which charge that had work done on it can leak to ground, greatly decreasing conversion efficiency. As an example, if the scope probe is attached to a point in the circuit with DC voltage $V_{\text{NODE}} = 2$ V, the parasitic resistance will on average dissipate

$$\langle P_{\text{Diss}} \rangle = \frac{V^2}{R} = \frac{2^2}{10^6} = 0.4 \ \mu W,$$

which could realistically exceed the amount of harvested energy.

In order to minimize probe loss, all probe points on the final PCB design require a series 10 MΩ resistor in front of the scope probe entry point; this halves the consumed
power at the expense of voltage resolution on the oscilloscope. With this in mind, all simulations will have a 20 MΩ parasitic resistance attached to probing nodes, the most prominent ones being $v_{\text{RES}}$ and $v_{\text{S}}$, in order to assure that measurements can be taken on the actual board.

### 3.5 Gate Drive Modeling

In order to feed the converted energy from the temporary storage capacitor $C_S$ back into the reservoir capacitor $C_{\text{RES}}$, the n-channel MOSFET serving as a pass transistor must be driven on and off in a timely fashion. The actual choice of drive strength and frequency will be discussed later in the chapter after simulation results are presented, but it is nonetheless important to discuss ways in which the clock signal can be modeled with sufficient precision in HSPICE.

Based on the selection of an LMC555 CMOS timer configured in astable operation as the gate drive, two important limitations must be modeled: finite rise time and saturation voltage limits from $V_{\text{SS}}$, the bottom power rail, and $V_{\text{DD}}$, the top power rail. These nonidealities are important because both contribute to additional power loss during the conversion — finite rise time incur switching losses while saturation voltage limits give rise to leakage current at the low end and higher than expected channel on-resistance at the high end. From the LMC555 datasheet, the rise and fall time are both 15 ns and the saturation voltage limit is 0.3 V from either supply rail.

### 3.6 Simulating the Two Diode Circuit

To better understand the energy harvesting process, the first part of the circuit, namely the components of the charge pump, is simulated on its own. As a starting point, a reservoir capacitor of value $C_{\text{RES}} = 1 \, \mu F$ and a storage capacitor of value $C_S = 3.3 \, nF$ are chosen; the value of $C_S$ insures that parasitic capacitance from the
oscilloscope probe and other sources do not dominate.

Fig. 3-4 shows the schematic for this section of the energy harvesting circuit, repeated from Chapter 2 for convenience. The schematic lacks any source of voltage excitation; instead, before the simulation in HSPICE begins, all the individual node voltages, $v_{\text{RES}}$, $v_{\text{VAR}}$, and $v_S$ are initialized to 6 V. This allows the system to begin with some initial energy that is necessary to start the energy conversion process. In a real circuit, a battery that can be disconnected would serve as this initial energy injection source.
During each cycle of operation, within which $C_{\text{RES}}$ decreases from its maximum value and goes back up, energy flows from both the reservoir capacitor and the vibrational source into $C_S$, as shown earlier in Chapter 2. The voltage waveforms for $v_{\text{RES}}$, $v_{\text{VAR}}$, and $v_S$ plotted in Fig. 3-5 indicate the effects of these energy transfers. As expected, the energy transferred to $C_S$ causes $v_S$ to rise in accordance to $W_S = \frac{1}{2} C_S v_S^2$. At the same time, $v_{\text{RES}}$ drops as charge is pulled out of $C_{\text{RES}}$ and placed onto $C_{\text{VAR}}$ for the vibrational source to do work on. However, because $C_{\text{RES}} \gg C_{\text{VAR}}$, the decrease in $v_{\text{RES}}$ is insignificant, allowing $v_{\text{RES}}$ to be treated as a constant during this part of the simulation. Furthermore, $v_{\text{VAR}}$ oscillates up and down as $C_{\text{VAR}}$ varies, also in agreement with the predicted behavior.

In each energy conversion cycle,

$$W_{\text{CONV}} = \frac{1}{2} Q_o \Delta v_{\text{VAR}} = \frac{1}{2} Q_o^2 \left( \frac{1}{C_{\text{MIN}}} - \frac{1}{C_{\text{MAX}}} \right)$$  \hspace{1cm} (3.5)$$

where $Q_o$ is the amount of constrained charge and $C_{\text{MIN}}$ and $C_{\text{MAX}}$ are the minimum and maximum capacitance value for the vibrating capacitor. As more and more conversion cycles occur, $Q_o$ decreases due to increasing difficulty of placing additional charge on $C_{\text{VAR}}$ (refer to Eq. (2.15)). This results in the decreasing step height for $v_S$.

The theoretical maximum voltage that $v_S$ can obtain has been calculated in Chapter 2. Using the derived formula,

$$v_{\text{S,MAX}} = \frac{C_{\text{MAX}}}{C_{\text{MIN}}} v_{\text{S,O}} = 1.65 \times 6 \text{ V} = 9.9 \text{ V}$$  \hspace{1cm} (3.6)$$

if we take $C_{\text{DC}} = 1.22 \text{ nF}$ and $C_{\text{AC}} = 300 \sin(2\pi \times 1900t) \text{ pF}$ like in the earlier example. Looking at Fig. 3-5, it is apparent that $v_S$ does not approach 9.9 V but instead flattens out at around 9.5 V. This discrepancy stems from the fact that the theoretical calculations presented in Chapter 2 ignored the forward bias voltage drop of the Schottky barrier diodes.

55
Figure 3-6: Current waveforms for charge pump circuit with $C_{DC} = 1.22$ nF, $C_{AC} = 300$ pF, $C_{RES} = 1$ $\mu$F, $C_s = 3.3$ nF, and $v_{INIT} = 6$ V. The vertical axis represents current plotted in amps and the horizontal axis represents time plotted in seconds.

Fig. 3-6 shows the current passing through the two diodes. The simulated waveforms shows that the diodes conduct in alternating fashion, in agreement with theory. However, theoretical calculation ignored the effect of leakage current during the time when diodes are reverse biased. Simulations later in this chapter confirms that diode leakage has a detrimental effect on the efficiency of energy harvesting (due to the careful selection of Schottky diodes with maximum $I_S = 0.15$ $\mu$A, the reverse bias leakage current is not readily visible in the simulated waveforms).

Comparing the current and voltage waveforms, one finds that $v_S$ ramps up when $D_2$ is conducting and stays flat when $D_1$ is conducting. This makes sense intuitively because the only time when harvested energy can flow into $C_s$ occurs while $D_2$ conducts. Finally, notice the decreasing amplitude of conducted current; this shows that as $v_S$ rises, $C_{VAR}$ discharges less into $C_s$ per cycle and therefore extracts fewer charges from the reservoir.

For this part of the energy harvesting circuit to be considered successful, positive
net energy should result after a few cycles of vibrational motion. For any capacitor, the change in stored energy given an original voltage $v_O$ and a final voltage $v_F$ is

$$\Delta W_C = \frac{1}{2} C \left( v_F^2 - v_O^2 \right).$$ \hspace{1cm} (3.7)

Using the same simulation parameters as above, the reservoir voltage droops from $v_{RES} = 6 \text{ V}$ to $v_{RES} = 5.9923 \text{ V}$ after 4 cycles. During the same period of time, the temporary storage node rises from $v_S = 6 \text{ V}$ to $v_S = 8.2268 \text{ V}$. Therefore,

$$\Delta W_{TOT} = \frac{1}{2} C_{RES} \left( v_{RES,F}^2 - v_{RES,O}^2 \right) + \frac{1}{2} C_S \left( v_{S,F}^2 - v_{S,O}^2 \right)$$

$$= -\frac{1}{2} \left( 10^{-6} \text{ F} \right) \left( 0.092 \text{ V}^2 \right) + \frac{1}{2} \left( 3.3 \times 10^{-9} \text{ F} \right) \left( 31.680 \text{ V}^2 \right)$$ \hspace{1cm} (3.8)

$$= 6 \text{ nJ}.$$ \hspace{1cm} (3.9)

The net energy of the system is rising, indicating a success in injecting mechanical vibration energy into the circuit.

### 3.7 Two Diode Circuit with Energy Flyback

Now that the charge pump portion of the circuit has been shown to convert positive energy, the inductive energy flyback consisting of a pass transistor, freewheeling diode, and an inductor will be added. Their addition, along with a parasitic probe resistance $R_p$ mentioned earlier, completes the entire circuit except for the transistor gate drive; the schematic is shown in Fig. 3-7.

As a first pass simulation, the gate of the MOSFET is driven in such a way that it is impossible for energy to be accidentally injected into the system. In HSPICE, this amounts to modeling the transistor as a variable resistor, with resistance value varying discontinuously from the MOSFET $R_{ON}$ value to $10^{10} \Omega$ as a controlling node voltage sweeps through $v_T$, the threshold voltage of the MOSFET. Other relevant parameters are $C_{RES} = 1 \mu\text{F}$, $C_S = 3.3 \text{ nF}$, $R_p = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $57$
Figure 3-7: The complete energy harvesting circuit without gate drive.

\( R_W = 8 \, \Omega, \ C_{DC} = 1.22 \, \text{nF}, \ C_{AC} = 300 \, \text{pF}, \) and \( v_{\text{INIT}} = 6 \, \text{V}, \) where \( v_{\text{INIT}} \) represents the voltage initialized on all the nodes before energy harvesting begins. The CLK signal is temporarily modeled with 1 ns rise and fall time, \( v_L = 0 \, \text{V}, \ v_H = 10 \, \text{V}, \)
\( f_{\text{CLK}} = \frac{f_{\text{MECH}}}{4} = 475 \, \text{Hz} \) where \( f_{\text{MECH}} = 1.9 \, \text{kHz} \) denotes the mechanical resonant frequency of the variable capacitor, and duty cycle \( D = 0.0019. \)

The key parameter, \( v_{\text{RES}} \), is graphed in Fig. 3-8. Initially, a lot of charge is drawn from \( C_{\text{RES}} \) because the circuit needs to reach its PSS state from the initialized voltage. After the initial drop, it is apparent from the simulation results that \( v_{\text{RES}} \) begins to rise at an approximately linear rate following each 4-step drop, which corresponds to the fact that \( f_{\text{CLK}} = \frac{f_{\text{MECH}}}{4} \). A simple calculation confirms that, ignoring the initial voltage drop, the circuit converts

\[
\Delta W_{\text{RES}} = \frac{1}{2} C_{\text{RES}} (6.0013 \, \text{V}^2 - 5.9989 \, \text{V}^2) = 14 \, \text{nJ} .
\]  

(3.11)

Since the voltage rise happens in \( t = 99.32 \, \text{ms} \),

\[
P_{\text{CONV}} = \frac{\Delta W_{\text{RES}}}{t} = 0.145 \, \mu\text{W} .
\]  

(3.12)

It is also instructive to observe \( v_{\text{VAR}} \) and \( v_S \) along with the current flowing through \( D_1 \) and \( D_2 \). These waveforms appear in Fig. 3-9 and Fig. 3-10. As Fig. 3-9 shows,
Figure 3-8: $v_{RES}$ as a function of time for an ideally driven circuit. Here, $C_{RES} = 1 \mu F$, $C_S = 3.3 \, nF$, $R_F = 20 \, M\Omega$, $L_{FB} = 2.5 \, mH$, $R_C = 360 \, k\Omega$, $R_W = 8 \, \Omega$, $C_{DC} = 1.22 \, nF$, $C_{AC} = 300 \, pF$, and $v_{INIT} = 6 \, V$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

$C_S$ builds up charge in agreement with theory derived in Chapter 2 and discharges when the inductive flyback turns on. Also, $v_S$ follows $v_{VAR}$ with approximately a $v_D$ diode forward bias voltage drop subtracted when $D_2$ conducts; this also agrees well with theory.

Comparing Fig. 3-10 to Fig. 3-6, one sees that instead of the current peaks tapering off due to the buildup of charge on $C_S$, the circuit with energy flyback allows sustained amounts of current to flow from $C_{RES}$ into $C_S$. The only limit preventing the linear rise in $v_{RES}$ from continuing forever is that the energy flyback becomes incrementally more difficult as the peak value of $v_{RES}$ approaches the theoretical maximum of $v_S$ as derived in Eq. (2.15). Of course, an external circuit powered off the energy stored on $C_{RES}$ will prevent this saturation from happening.

The above waveforms provide a general feel as to how a successful energy harvesting circuit might operate, but they do not represent the circuit accurately and
Figure 3-9: $v_{\text{VAR}}$ and $v_S$ as a function of time for an ideally driven circuit. Here, $C_{\text{RES}} = 1 \ \mu\text{F}$, $C_S = 3.3 \ \text{nF}$, $R_P = 20 \ \text{M}\Omega$, $L_{\text{FB}} = 2.5 \ \text{mH}$, $R_C = 360 \ \text{k}\Omega$, $R_W = 8 \ \Omega$, $C_{\text{DC}} = 1.22 \ \text{nF}$, $C_{\text{AC}} = 300 \ \text{pF}$, and $v_{\text{INIT}} = 6 \ \text{V}$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

are intended for reference only. The main deficiency of modeling the MOSFET as an abrupt variable resistor is that when the transistor enters saturation, the behavior is no longer resistive. Furthermore, in cutoff, the exact $R_{\text{OFF}}$ value may well be different than the one arbitrarily chosen in the current simulation.

Before leaving the idealized circuit model, it is helpful to determine the amount of energy converted as a function of the flyback switch turn-on frequency $f_{\text{CLK}}$. The result of this set of simulations is shown in Table 3.1. As the frequency increases, the amount of power converted initially increases, then drops off as the frequency moves above a certain point, suggesting that an optimal point of operation exists. When the actual MOSFET model is substituted for the idealized variable resistor, this observation will be revisited.
Figure 3-10: $i_D1$ and $i_D2$ as a function of time for an ideally driven circuit. Here, $C_{RES} = 1 \, \mu F$, $C_S = 3.3 \, nF$, $R_P = 20 \, M\Omega$, $L_{FB} = 2.5 \, mH$, $R_C = 360 \, k\Omega$, $R_W = 8 \, \Omega$, $C_{DC} = 1.22 \, nF$, $C_{AC} = 300 \, pF$, and $v_{INIT} = 6 \, V$. The vertical axis represents current plotted in amps and the horizontal axis represents time plotted in seconds.

3.8 Gate Drive, A First Attempt

Having crudely simulated the complete energy harvesting circuit, the gate drive can now be considered. As a first attempt, the MOSFET will be driven by a CLK signal referenced to ground and modeled after the limitations of an LMC555CM National Semiconductor CMOS timer, resulting in $t_{\text{RISE}} = t_{\text{FALL}} = 15 \, \text{ns}$, $v_L = 0.3 \, V$, $v_H = 19.7 \, V$, $f_{CLK} = \frac{19 \, \text{kHz}}{4} = 475 \, \text{Hz}$, and duty cycle $D = 0.0019$. The HSPICE transistor model for a 2N7002 n-channel MOSFET is substituted in place of the variable resistor model used in the previous section. Also, note that the high $v_H$ selected for driving the gate relates to the non-zero MOSFET source potential; to turn on the transistor hard requires $v_{GS} > v_T$.

Fig. 3-11 shows the rising $v_{RES}$ as a function of time simulated using the above parameters. Based on the increasing reservoir voltage, it is tempting to argue that this particular setup converts net energy. Using the previously derived formula, the
Table 3.1: Ideal converted power as a function of $f_{\text{CLK}}$. Here, $C_{\text{RES}} = 1 \ \mu\text{F}$, $C_S = 3.3 \ \text{nF}$, $R_P = 20 \ \text{M}\Omega$, $L_{\text{FB}} = 2.5 \ \text{mH}$, $R_C = 360 \ \text{k}\Omega$, $R_W = 8 \ \Omega$, $C_{\text{DC}} = 1.22 \ \text{nF}$, $C_{\text{AC}} = 300 \ \text{pF}$, and $v_{\text{INIT}} = 6 \ \text{V}$. $v_O$ represents the starting voltage of $C_{\text{RES}}$ and $v_F$ represents the final voltage of $C_{\text{RES}}$.

The amount of energy increase on $C_{\text{RES}}$ is

$$\Delta W_{\text{RES}} = \frac{1}{2} C_{\text{RES}} (6.0034 \ V^2 - 5.9991 \ V^2) = 26 \ \text{nJ}$$

(3.13)

given that one ignores the initial voltage drop like what was done earlier. The equivalent power is

$$P_{\text{CONV}} = \frac{\Delta W_{\text{RES}}}{t} = 0.875 \ \mu\text{W}.$$  

(3.14)

However, with an actual MOSFET in place of the idealized variable resistor model, one can reasonably question whether the parasitic capacitances of the transistor, combined with the numerous discrete and parasitic diodes present in the circuit, can cause spurious energy injection in addition to the desired vibration energy conversion. If such energy injection from the clock signal exists, the amount of energy converted must be adjusted to reflect this undesired energy source.

This question can be examined using two different methods. The first uses the fact that as the $v_{\text{GS}}$ of a MOSFET exceeds its $v_T$ by a large margin, further increases in $v_{\text{GS}}$ do not significantly decrease $R_{\text{ON}}$. Therefore, the amount of energy converted, which relates inversely to conduction loss, should not change drastically as the gate voltage ramps up. Secondly, if the clock signal is indeed injecting energy, an increase in clock frequency will cause the amount of injected energy to increase proportionally.
Figure 3-11: $v_{RES}$ as a function of time for a ground-referenced CLK drive. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_P = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ } \Omega$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{INIT} = 6 \text{ V}$, $t_{\text{rise}} = t_{\text{fall}} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 19.7 \text{ V}$, $f_{CLK} = 475 \text{ Hz}$, and $D = 0.0019$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

To test the dependency of $P_{\text{CONV}}$ on $v_G$, a series of simulations were performed at linear increments of the gate voltage. All other circuit parameters remain the same. As Table 3.2 shows, $P_{\text{CONV}}$ increases significantly as $v_G$ increases, much more than that predicted by the drop in $R_{\text{ON}}$. This suggests that there is a high probability that at least part of the converted energy comes from unwanted injection through the transistor.

To verify the source of additional energy injection, another set of simulations were run, each with a different energy flyback clocking frequency. Under normal circumstances where no net energy is injected through the transistor, the net energy converted should remain relatively constant as long as the mechanical vibration frequency is fixed. Fundamentally, as long as the energy flyback does not occur after so many mechanical cycles that $v_S$ builds up to a point near saturation as explained in

63
Table 3.2: Converted power as a function of $v_G$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \, nF$, $R_P = 20 \, M\Omega$, $L_{FB} = 2.5 \, mH$, $R_C = 360 \, k\Omega$, $R_W = 8 \, \Omega$, $C_{DC} = 1.22 \, nF$, $C_{AC} = 300 \, pF$, $v_{INIT} = 6 \, V$, $t_{RISE} = t_{FALL} = 15 \, ns$, $v_L = 0.3 \, V$, $f_{CLK} = 475 \, Hz$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_f$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$v_G$ (V)</th>
<th>$v_O$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{CONV}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>5.9995</td>
<td>5.9724</td>
<td>$-5.50 \times 10^{-6}$</td>
</tr>
<tr>
<td>10.7</td>
<td>5.9989</td>
<td>5.9921</td>
<td>$-1.40 \times 10^{-6}$</td>
</tr>
<tr>
<td>16.7</td>
<td>5.9990</td>
<td>6.0029</td>
<td>$0.79 \times 10^{-6}$</td>
</tr>
<tr>
<td>22.7</td>
<td>5.9991</td>
<td>6.0041</td>
<td>$1.02 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Table 3.3: Converted power as a function of $f_{CLK}$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \, nF$, $R_P = 20 \, M\Omega$, $L_{FB} = 2.5 \, mH$, $R_C = 360 \, k\Omega$, $R_W = 8 \, \Omega$, $C_{DC} = 1.22 \, nF$, $C_{AC} = 300 \, pF$, $v_{INIT} = 6 \, V$, $t_{RISE} = t_{FALL} = 15 \, ns$, $v_L = 0.3 \, V$, $v_H = 10.7 \, V$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_f$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$f_{CLK}$ (kHz)</th>
<th>$v_O$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{CONV}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.095</td>
<td>5.9989</td>
<td>5.9742</td>
<td>$-5.01 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.190</td>
<td>5.9989</td>
<td>5.9784</td>
<td>$-4.16 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.475</td>
<td>5.9989</td>
<td>5.9921</td>
<td>$-1.40 \times 10^{-6}$</td>
</tr>
<tr>
<td>1.900</td>
<td>5.9989</td>
<td>6.0043</td>
<td>$1.10 \times 10^{-6}$</td>
</tr>
<tr>
<td>3.800</td>
<td>5.9989</td>
<td>6.0126</td>
<td>$2.79 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Chapter 2, a slower flyback usually is more efficient because each flyback cycle incurs conduction losses; sending more energy back over fewer cycles lessens these losses.

Table 3.3 shows the results of the simulations; all test cases were run with $v_G = 10.7 \, V$. Just like $v_G$, increasing the clock frequency also dramatically increases the net converted energy. These data further support the hypothesis that a ground-referenced clock signal injects additional energy into the circuit, making this gate drive topology undesirable as far as energy harvesting circuit goes. This is also the reason why the reported energy conversion efficiency in [12] might be inaccurate; part of the harvested energy could have been injected by the gate drives used in that experiment.

The injection of energy from a clock signal deserves further analysis. In a typical
MOSFET circuit, the gate drive mechanism works to turn on the transistor by supplying an influx of charge onto the transistor’s gate capacitor. The amount of charge placed on the gate, $Q_{G}$, gives rise to some injected energy, originating from the power supply of the clock signal generator, in the electric field between the plates of the capacitor. Upon transistor turn-off, the same amount of charge should be extracted from the capacitor plates, resulting in no net change in the system’s energy. However, imagine a situation under which the MOSFET gate capacitor couples through one capacitor terminal into additional capacitors and diodes. If a diode turns on and leaks a certain amount of charge, $Q_{\text{LEAK}}$, away from the gate capacitor into another capacitor node with non-zero voltage, the gate drive can no longer extract all the injected energy (by conservation of energy, the extracted energy is the injected energy subtracted by the energy remaining in the system), implying that $W_{\text{IN,CLK}} > W_{\text{OUT,CLK}}$. Fig. 3-12(a) and Fig. 3-12(b) illustrates this process. Hence, unless this problem is corrected, all experimental data collected will be misleading.
### 3.9 Corrected Gate Drive

Given that a ground-referenced clock signal cannot be used, the natural alternative, a source-referenced signal, is explored. One major disadvantage of a source-referenced clock stems from the fact that the voltage supply driving the clocking circuitry must be floating since the MOSFET's source remains above 0 V throughout the circuit operation. Given that the goal of this thesis focuses on the macro model of the energy harvester and the operation of the power electronics, batteries are used to create the required floating voltage source. Such a gate-drive strategy is shown in Fig. 3-13.

In order to gauge the validity of this alternative, similar test runs regarding $v_{GS}$ and $f_{CLK}$ were done. Note that unlike the ground-referenced case, the floating clock signal is exactly $v_{GS}$; this voltage equality allows the transistor to be turned on at the same strength regardless of what the source voltage becomes. In the ground-referenced case, the MOSFET can fail to turn on if the source voltage is allowed to climb too high.

Table 3.4 shows $P_{\text{CONV}}$ as a function of $v_{GS}$ using the same parameters chosen earlier for the ground-referenced clock. Observe that the amount of converted power is now independent of the gate-source voltage, indicating that there no longer exists a path inside the MOSFET through which spurious energy can slip into the system.
Table 3.4: Converted power as a function of $v_{GS}$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_P = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ } \Omega$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{\text{INIT}} = 6 \text{ V}$, $t_{\text{RISE}} = t_{\text{FALL}} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $f_{\text{CLK}} = 475 \text{ Hz}$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$v_{GS}$ (V)</th>
<th>$v_o$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{\text{CONV}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>6.0000</td>
<td>5.9752</td>
<td>$-5.034 \times 10^{-6}$</td>
</tr>
<tr>
<td>5</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.773 \times 10^{-6}$</td>
</tr>
<tr>
<td>11</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.773 \times 10^{-6}$</td>
</tr>
<tr>
<td>17</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.773 \times 10^{-6}$</td>
</tr>
<tr>
<td>23</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.773 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Table 3.5: Converted power as a function of $f_{\text{CLK}}$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_P = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ } \Omega$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{\text{INIT}} = 6 \text{ V}$, $t_{\text{RISE}} = t_{\text{FALL}} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$f_{\text{CLK}}$ (kHz)</th>
<th>$v_o$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{\text{CONV}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.095</td>
<td>6.0000</td>
<td>5.9943</td>
<td>$-1.620 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.190</td>
<td>6.0000</td>
<td>5.9989</td>
<td>$-0.251 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.475</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.773 \times 10^{-6}$</td>
</tr>
<tr>
<td>1.900</td>
<td>6.0000</td>
<td>5.9964</td>
<td>$-0.732 \times 10^{-6}$</td>
</tr>
<tr>
<td>3.800</td>
<td>6.0000</td>
<td>5.9957</td>
<td>$-0.880 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

An extra test case of $v_{GS} = 2 \text{ V}$ confirms that when the MOSFET is not turned on hard, $R_{ON}$ is high enough that conduction loss overwhelms the converted electrical energy.

The effect of source-referenced energy flyback clocking frequency on the converted power with $v_{GS} = 5 \text{ V}$ can be seen in Table 3.5. The converted power still is not constant as a function of $f_{\text{CLK}}$, but now instead of monotonically increasing, it behaves similarly to the idealized, variable resistor case explored earlier. Recalling the limitation on $v_S$ given the absence of energy flyback, the lower $P_{\text{CONV}}$ for small $f_{\text{CLK}}$ can easily be explained. Fig. 3-14 shows waveform of $v_S$ under slow energy flyback condition. Here, $v_S$ rises so high that it begins to saturate, which is the primary
Figure 3-14: $v_S$ as a function of time for slow energy flyback clocking. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \ nF$, $R_P = 20 \ M\Omega$, $L_{FB} = 2.5 \ mH$, $R_C = 360 \ k\Omega$, $R_W = 8 \ \Omega$, $C_{DC} = 1.22 \ nF$, $C_{AC} = 300 \ pF$, $v_{INIT} = 6 \ V$, $t_{RISE} = t_{FALL} = 15 \ ns$, $v_L = 0.3 \ V$, $v_H = 5 \ V$, $f_{CLK} = 190 \ Hz$, and $D = 0.0019$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

reason why $P_{CONV}$ decreases for slow $f_{CLK}$. On the other hand, the drop in $P_{CONV}$ for large $f_{CLK}$ is mainly due to conduction losses dominating the converted energy since large $f_{CLK}$ implies feeding back energy faster than the mechanical conversion.

Given the drop off in $P_{CONV}$ both for low and high $f_{CLK}$, an optimal value can be found. Simulations in HSPICE result in the highest $P_{CONV}$ when the flyback frequency is set between 400-500 Hz. This is approximately one-quarter of $f_{MECH}$.

### 3.10 Parameter Optimization

Having decided on the gate drive topology, one can now modify certain parameters within the completed energy harvesting circuit to see the effect they have on conversion efficiency. For clarity, the next few sections will use a fixed set of circuit parameters.
Table 3.6: Converted power as a function of $R_C$ and $R_W$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_P = 20 \text{ M\Omega}$, $L_{FB} = 2.5 \text{ mH}$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{INIT} = 6 \text{ V}$, $t_{RISE} = t_{FALL} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, $f_{CLK} = 475 \text{ Hz}$, and $D = 0.0019$. $v_O$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$R_C$ (kΩ)</th>
<th>$R_W$ (Ω)</th>
<th>$v_O$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{CONV}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>8</td>
<td>6.0000</td>
<td>6.0017</td>
<td>$0.346 \times 10^{-6}$</td>
</tr>
<tr>
<td>100</td>
<td>8</td>
<td>6.0000</td>
<td>6.0029</td>
<td>$0.590 \times 10^{-6}$</td>
</tr>
<tr>
<td>360</td>
<td>8</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>360</td>
<td>30</td>
<td>6.0000</td>
<td>6.0030</td>
<td>$0.610 \times 10^{-6}$</td>
</tr>
<tr>
<td>360</td>
<td>60</td>
<td>6.0000</td>
<td>6.0021</td>
<td>$0.427 \times 10^{-6}$</td>
</tr>
<tr>
<td>360</td>
<td>200</td>
<td>6.0000</td>
<td>5.9983</td>
<td>$-0.346 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

3.10.1 Effect of Inductor Parasitics

In this section, the resistor values modeling the core loss and winding loss of the flyback inductor will be considered. Table 3.6 shows the converted power for various combinations of $R_C$ and $R_W$. When the core loss is increased more than 3 times by scaling down $R_C$, $P_{CONV}$ drops only by 25%. Therefore, although higher core loss negatively affects the converted power as expected, slight modeling error in the inductor parasitic will not lead to disastrous results. Similar conclusions can be made regarding $R_W$; however, as the simulation data shows, excessive wiring loss will lead to negative net energy conversion.
<table>
<thead>
<tr>
<th>$f_{CLK}$ (kHz)</th>
<th>$D$</th>
<th>$v_o$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{CONV}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.475</td>
<td>0.0010</td>
<td>6.0000</td>
<td>5.9921</td>
<td>$-1.606 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.475</td>
<td>0.0019</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.475</td>
<td>0.0028</td>
<td>6.0000</td>
<td>5.9991</td>
<td>$-0.183 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Table 3.7: Converted power as a function of $D$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_P = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ \Omega}$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{INIT} = 6 \text{ V}$, $t_{RISE} = t_{FALL} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, and $f_{CLK} = 475 \text{ Hz}$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

3.10.2 Effect of Clock’s Duty Ratio

As described earlier, the clock signal of the flyback pass transistor exerts a significant influence on the circuit’s energy conversion efficiency. Earlier, the effect of flyback frequency on conversion efficiency was outlined. Here, the duty ratio of the clock is varied in order to gauge the effect it has on circuit performance. The results of these simulations are shown in Table 3.7.

Interestingly, the duty ratio, defined as the percentage of the clock period during which the clock output is high, must remain within a very tight margin in order to achieve net positive energy conversion. At very low duty ratio, current in the flyback inductor $L_{FB}$ does not ramp up high enough to prevent saturation of $v_S$. If the duty ratio becomes too large, the inductor draws out so much charge from $C_S$ that $v_S$ actually dips below $v_{INIT}$ by almost 0.75 V; this causes $D_2$ to start conducting, breaking down the charge-constrained cycle before it reaches completion. Further simulations indicate that positive conversion will occur only if the pulse width of the on-cycle is between 3-5 ns.

To summarize, $f_{CLK}$ dictates the height to which $v_S$ rises to while $D$ determines how much $v_S$ falls by after one conduction cycle of the MOSFET and freewheeling diode. The desired behavior of the gate drive signal is to prevent $v_S$ from entering the saturation, or non-linear, region of operation and keep $v_S$ in PSS with a minimum
The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_p = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ \Omega}$, $C_{DC} = 1.22 \text{ nF}$, $v_{INIT} = 6 \text{ V}$, $t_{RISE} = t_{FALL} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, $f_{CLK} = 475 \text{ Hz}$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

<table>
<thead>
<tr>
<th>$C_{AC}$ (pF)</th>
<th>$v_o$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{CONV}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>6.0000</td>
<td>5.9869</td>
<td>$-2.661 \times 10^{-6}$</td>
</tr>
<tr>
<td>200</td>
<td>6.0000</td>
<td>5.9923</td>
<td>$-1.565 \times 10^{-6}$</td>
</tr>
<tr>
<td>300</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>400</td>
<td>6.0000</td>
<td>6.0234</td>
<td>$4.769 \times 10^{-6}$</td>
</tr>
<tr>
<td>500</td>
<td>6.0000</td>
<td>6.0542</td>
<td>$11.074 \times 10^{-6}$</td>
</tr>
<tr>
<td>600</td>
<td>6.0000</td>
<td>6.1001</td>
<td>$20.529 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Table 3.8: Converted power as a function of $C_{AC}$. The circuit parameters used in simulation are $C_{RES} = 1 \mu F$, $C_S = 3.3 \text{ nF}$, $R_p = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ \Omega}$, $C_{DC} = 1.22 \text{ nF}$, $v_{INIT} = 6 \text{ V}$, $t_{RISE} = t_{FALL} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, $f_{CLK} = 475 \text{ Hz}$, and $D = 0.0019$. $v_o$ represents the starting voltage of $C_{RES}$ and $v_F$ represents the final voltage of $C_{RES}$.

value no lower than $v_{INIT}$. Satisfying these two conditions, perhaps through the use of a PWM flyback control system that senses $v_S$, allow the energy flyback process to occur at maximum efficiency.

### 3.10.3 Effect of Capacitance Variation

In Chapter 2, the equation that determined the saturation point of $v_S$ was derived. Based on previous discussions, energy harvesting should, in theory, occur at higher efficiency given a greater variation in $C_{AC}$. To verify this, a set of simulations with different variable capacitor amplitudes were run, and the results are summarized in Table 3.8. The benefits of using a variable capacitor with large $C_{AC}$ is apparent. However, in actuality, fabricating a device that can, for example, exhibit a capacitance variation ratio of more than 2:1 is quite challenging. Notice that given $C_{DC} = 1.22 \text{ nF}$, a $C_{AC} < 300 \text{ pF}$ results in negative net energy conversion. This sets an absolute minimum capacitance variation ratio that must be achieved in order for energy harvesting under this circuit topology to work. It is

$$
\Gamma_{MIN} = \frac{C_{DC} + C_{AC}}{C_{DC} - C_{AC}} \approx 1.65 .
$$

(3.15)
Table 3.9: Converted power as a function of \( C_{RES} \) and \( C_S \). The circuit parameters used in simulation are \( R_P = 20 \, \text{M}\Omega \), \( L_{FB} = 2.5 \, \text{mH} \), \( R_C = 360 \, \text{k}\Omega \), \( R_W = 8 \, \Omega \), \( C_{DC} = 1.22 \, \text{nF} \), \( C_{AC} = 300 \, \text{pF} \), \( v_{INIT} = 6 \, \text{V} \), \( t_{RISE} = t_{FALL} = 15 \, \text{ns} \), \( v_L = 0.3 \, \text{V} \), \( v_H = 5 \, \text{V} \), \( f_{CLK} = 475 \, \text{Hz} \), and \( D = 0.0019 \). \( v_O \) represents the starting voltage of \( C_{RES} \) and \( v_F \) represents the final voltage of \( C_{RES} \).

3.10.4 Effect of Capacitor Values

The values of \( C_{RES} \) and \( C_S \) were both arbitrarily chosen with the goal of having \( C_{RES} \gg C_S \). In this section, the effect of changing these two capacitances, or the lack thereof, will be explored. Table 3.9 shows these results.

Although the data set seems to suggest that increasing \( C_S \) helps raise conversion efficiency, care must be taken since this capacitance increase also results in a larger initial voltage dip, as shown in Fig. 3-15. This can be explained by the fact that raising the voltage of a large \( C_S \) requires more charge, so \( v_S \) does not rise as high. This prevents the current ramping of the flyback inductor from obtaining a high enough amplitude to allow for net increase in \( v_{RES} \), at least initially. Using too big a \( C_S \) can cause so much dip in voltage that the energy harvesting circuit fails to recover.

On the other hand, increasing \( C_{RES} \) does not significantly affect the energy conversion efficiency. \( v_{RES} \) rises less because of the increased capacitance, but the overall converted power remains relatively constant. However, using a very large \( C_{RES} \) precludes easy visual measurement on the oscilloscope since the voltage rise, one of the main metrics to gauge successful energy harvesting, will become so small that the scope can no longer resolve it.
Figure 3-15: $v_S$ as a function of time for $C_S = 10 \text{nF}$. Here, $C_{RES} = 1 \mu\text{F}$, $R_P = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_C = 360 \text{ k}\Omega$, $R_W = 8 \text{ } \Omega$, $C_{DC} = 1.22 \text{ nF}$, $C_{AC} = 300 \text{ pF}$, $v_{INIT} = 6 \text{ V}$, $t_{\text{rise}} = t_{\text{fall}} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 5 \text{ V}$, $f_{CLK} = 475 \text{ Hz}$, and $D = 0.0019$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

3.10.5 Effect of Initial Voltage Level

To “jump-start” the energy harvesting circuit, a voltage source, such as a battery, is necessary to charge all the circuit nodes to a certain voltage. However, up to this point, the magnitude of this voltage has not been well determined. This section attempts to resolve this uncertainty. For the set of data points resulting from different values of $v_{INIT}$, refer to Table 3.10.

As one can see, the amount of power converted rises proportionally to $v_{INIT}$. Certainly, this parameter can be increased as large as possible limited only by conduction losses (such as that resulting from $v_{INIT} = 50 \text{ V}$) and device stresses on the MOSFET and diode. In most cases, however, a voltage source with higher voltage directly leads to a physically larger design, which might result from a bulkier battery.
Table 3.10: Converted power as a function of $v_{\text{INIT}}$. The circuit parameters used in simulation are $C_{\text{RES}} = 1$ µF, $C_S = 3.3$ nF, $R_P = 20$ MΩ, $L_{\text{FB}} = 2.5$ mH, $R_C = 360$ kΩ, $R_W = 8$ Ω, $C_{\text{DC}} = 1.22$ nF, $C_{\text{AC}} = 300$ pF, $t_{\text{Rise}} = t_{\text{Fall}} = 15$ ns, $v_L = 0.3$ V, $v_H = 5$ V, $f_{\text{CLK}} = 475$ Hz, and $D = 0.0019$. $v_O$ represents the starting voltage of $C_{\text{RES}}$ and $v_F$ represents the final voltage of $C_{\text{RES}}$.

<table>
<thead>
<tr>
<th>$v_{\text{INIT}}$ (V)</th>
<th>$v_O$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{\text{CONV}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>1.5000</td>
<td>1.4956</td>
<td>$-0.223 \times 10^{-6}$</td>
</tr>
<tr>
<td>6.0</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>10.0</td>
<td>10.0000</td>
<td>10.0120</td>
<td>$4.070 \times 10^{-6}$</td>
</tr>
<tr>
<td>50.0</td>
<td>50.0000</td>
<td>49.9120</td>
<td>$-149.021 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

Table 3.11: Converted power as a function of $I_S$. The circuit parameters used in simulation are $C_{\text{RES}} = 1$ µF, $C_S = 3.3$ nF, $R_P = 20$ MΩ, $L_{\text{FB}} = 2.5$ mH, $R_C = 360$ kΩ, $R_W = 8$ Ω, $C_{\text{DC}} = 1.22$ nF, $C_{\text{AC}} = 300$ pF, $v_{\text{INIT}} = 6$ V, $t_{\text{Rise}} = t_{\text{Fall}} = 15$ ns, $v_L = 0.3$ V, $v_H = 5$ V, $f_{\text{CLK}} = 475$ Hz, and $D = 0.0019$. $v_O$ represents the starting voltage of $C_{\text{RES}}$ and $v_F$ represents the final voltage of $C_{\text{RES}}$.

<table>
<thead>
<tr>
<th>$I_S$ (µA)</th>
<th>$v_O$ (V)</th>
<th>$v_F$ (V)</th>
<th>$P_{\text{CONV}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.150</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>0.600</td>
<td>6.0000</td>
<td>5.9893</td>
<td>$-2.174 \times 10^{-6}$</td>
</tr>
<tr>
<td>1.000</td>
<td>6.0000</td>
<td>5.9756</td>
<td>$-4.953 \times 10^{-6}$</td>
</tr>
<tr>
<td>2.000</td>
<td>6.0000</td>
<td>5.9415</td>
<td>$-11.840 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

3.10.6 Effect of Diode Leakage

Selection of low leakage diode allows the energy harvesting cycle to operate as ideally as possible. As the $I_S$ of a diode increases, more and more charge leaks out during the vibration-to-electric energy conversion cycle, which leads directly to decreased amount of harvested energy. To study this effect, the $I_S$ parameter in the HSPICE model of the 1N6263 Schottky barrier diodes was modified. This set of test runs is summarized in Table 3.11. As the simulation shows, Schottky diodes with very low leakage, with $I_S < 0.2$ µA, are necessary to achieve positive net energy conversion. Practically speaking, however, Schottky diodes with extremely low leakage are hard to find.
Table 3.12: Converted power as a function of $t_{\text{RISE}}$ and $t_{\text{FALL}}$. The circuit parameters used in simulation are $C_{\text{RES}} = 1 \, \mu\text{F}$, $C_{\text{S}} = 3.3 \, \text{nF}$, $R_{\text{p}} = 20 \, \text{M}\Omega$, $L_{\text{FB}} = 2.5 \, \text{mH}$, $R_{\text{C}} = 360 \, \text{k}\Omega$, $R_{\text{W}} = 8 \, \Omega$, $C_{\text{DC}} = 1.22 \, \text{nF}$, $C_{\text{AC}} = 300 \, \text{pF}$, $v_{\text{INIT}} = 6 \, \text{V}$, $v_{\text{L}} = 0.3 \, \text{V}$, $v_{\text{H}} = 5 \, \text{V}$, $f_{\text{CLK}} = 475 \, \text{Hz}$, and $D = 0.0019$. $v_{\text{O}}$ represents the starting voltage of $C_{\text{RES}}$ and $v_{\text{F}}$ represents the final voltage of $C_{\text{RES}}$.

<table>
<thead>
<tr>
<th>$t_{\text{RISE}}$ (ns)</th>
<th>$t_{\text{FALL}}$ (ns)</th>
<th>$v_{\text{O}}$ (V)</th>
<th>$v_{\text{F}}$ (V)</th>
<th>$P_{\text{CONV}}$ (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>15</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
<tr>
<td>15</td>
<td>30</td>
<td>6.0000</td>
<td>6.0037</td>
<td>$0.753 \times 10^{-6}$</td>
</tr>
<tr>
<td>15</td>
<td>100</td>
<td>6.0000</td>
<td>6.0036</td>
<td>$0.732 \times 10^{-6}$</td>
</tr>
<tr>
<td>30</td>
<td>15</td>
<td>6.0000</td>
<td>6.0037</td>
<td>$0.753 \times 10^{-6}$</td>
</tr>
<tr>
<td>100</td>
<td>15</td>
<td>6.0000</td>
<td>6.0038</td>
<td>$0.786 \times 10^{-6}$</td>
</tr>
</tbody>
</table>

3.10.7 Effect of Rise and Fall Time

Finally, it is instructive to see how the sharpness of the gate driving clock edges affects the energy harvesting efficiency. In the realm of power electronics, transistors and diodes perform like switches, either turning fully on or fully off. Therefore, a soft edge with long rise and fall times should cause the converted power to drop.

From the simulation results, larger $t_{\text{RISE}}$ and $t_{\text{FALL}}$ do indeed decrease the converted power but only very slightly. Therefore, as long as the edges are not overly soft, their effect on the conversion efficiency can be safely disregarded.

3.11 Chapter Summary

This chapter built upon the theoretical foundations established earlier through the use of HSPICE, a circuit simulation program. Various parameters, including the capacitor values, initial starting voltage, and inductor parasitics, were altered to gauge their effects on the overall energy conversion efficiency. Among all the parameters, $I_{\text{S}}$, $v_{\text{INIT}}$, $C_{\text{AC}}$, $D$, and $f_{\text{CLK}}$ seem to have the most influence. However, perhaps the single most important thing that allows the circuit to function properly is the source-
referenced gate drive, which removed the spurious source of energy injection through the MOSFET.

Through iterations of optimization, it is decided that the following set of parameters would be used in the experimental circuit presented in the next chapter. They are as follows: $C_{RES} = 1 \mu F$, $C_S = 3.3 \, nF$, $R_p = 20 \, M\Omega$, $L_{FB} = 2.5 \, mH$, $R_C = 360 \, k\Omega$, $R_W = 8 \, \Omega$, $v_{INIT} = 6 \, V$, $t_{RISE} = t_{FALL} = 15 \, ns$, $v_L = 0.3 \, V$, $v_H = 5 \, V$, $f_{CLK} = \frac{1.9 \, kHz}{4} = 475 \, Hz$, and $D = 0.0019$. In fact, these are precisely the parameter values used as the base case for most simulations performed in this chapter. Chapter 4 explores how closely the fabricated printed circuit board and variable capacitor follows the simulation results.
A successful circuit not only needs to be simulated in HSPICE but also built and demonstrated. This chapter will attempt to bridge the gap between simulation results and an actual energy harvesting circuit that was constructed on a printed circuit board, as shown in Fig. 4-1. By looking at oscilloscope waveforms of $v_{\text{RES}}$, $v_{\text{VAR}}$, and $v_{\text{S}}$, and comparing them to simulated waveforms, one can determine the accuracy of the modeling, which ultimately allows for missing second-order parasitic components to be extracted and included. Further topological and device optimization can then follow in order to try to raise the energy conversion efficiency even more.

Two different variable capacitor designs are examined in this chapter. The first one consists of two machined aluminum blocks tightened with screws to form the two plates of a parallel capacitor [11]. Although functional, this design cannot generate enough capacitance variation to successfully convert positive net energy; a second design corrects for this deficiency.
4.1 Aluminum Block Capacitor Characterization

Documented in [11], the dimensions of the aluminum block capacitor are repeated here for convenience of the reader. The machined top section, with two rectangular grooves milled out, forms a $3 \text{ cm} \times 3 \text{ cm}$ overlap region with the bottom section. In order to allow for the gap height to easily vary with vibration, the grooves leave only a 0.2 cm thick cantilever beam with $W_B = 3 \text{ cm}$ and $L_B = 1 \text{ cm}$ on either side of the central column as support. Finally, to offset the two sections apart and set $C_{\text{DC}}$, the nominal capacitance, one strip of 25 $\mu$m thick, nonconducting Mylar tape was placed at the edges of the structure before the two pieces were screwed together using nylon screws. A picture of the aluminum variable capacitor appears in Fig. 4-2, with the dark gray areas representing Mylar tapes, the shaded areas representing aluminum blocks, and the hatched area indicating drilled regions.

To maximize the $Q$, or quality factor, of the capacitor at resonance, which directly leads to a larger capacitance variation, the entire aluminum structure is enclosed in a vacuum chamber created using thick cylindrical plexiglass. The vacuum also serves to decrease the water vapor content within the compressible air film region between the two parallel plates in order to prevent condensation, observed in previous experiments, that could short out the variable capacitor.
The vacuum chamber is attached directly to a Ling Dynamic System V456 shaker table, shown in Fig. 4-3, set in the vertical position and controlled by a PA 1000L amplifier system. Together, this combination can provide a maximum sinusoidal acceleration peak of 1147 m/s² on the variable capacitor proof mass within the frequency range of 5–7500 Hz.

Given the assumed gap height of 25 μm and a parallel plate area of 9 cm², one can calculate a theoretical value of $C_{DC} = 318.6 \, \text{pF}$. In reality, measurements performed on a standard bridge machine show that the tightness of the nylon screws strongly influences the nominal capacitance. Typical measured values range from 752.4 pF to 1.323 nF. The fact that all the measurements exceed the theoretical value by more than two fold suggests that the two end columns contribute additional parasitic capacitances. These parasitics directly decrease the conversion efficiency, as evident from Eq. (2.16), because they only contribute to $C_{DC}$ and not $C_{AC}$.

After numerous attempts to decrease $C_{DC}$, the screw tightness was fixed to give $C_{DC} = 752.4 \, \text{pF}$. Under this condition, various shaking strengths were dialed into the PA 1000L at $f = 1900$ Hz and the output voltages from the $C_{AC}$ measurement amplifier setup described at the end of Chapter 2 for an evacuated variable capacitor.
were recorded. Note that for these measurements, a 5 V capacitor bias was used instead of the 10 V employed earlier. These data, along with the corresponding $C_{AC}$, are shown in Table 4.1.

The amplifier output appears approximately sinusoidal up to 30 mV peak-to-peak input into the PA 1000L shaker table driver. At an input of 40 mV, the bottom peaks of the sinusoidal waveform begin to saturate, indicating non-linear capacitor movement. With further increases in the driver amplitude, the amplifier output exhibits severe harmonic distortion, possibly indicating the excitation of additional vibrational modes not anticipated in the original design. Fig. 4-4 shows $v_{OUT}$ at three different shaking strengths.

To gauge the linearity of the capacitor response, $C_{AC}$ was plotted against the PA 1000L input voltage; the result appears in Fig. 4-5. For light shaking, $dC_{VAR}/dt$, and hence $v_{OUT}$ as well as $C_{AC}$, should be approximately linear with respect to shaking strength. This is because given

$$C_{VAR} = \frac{\epsilon_0 A}{x_{DC} + x_{AC} \sin(\omega t)},$$  \hspace{1cm} (4.1)$$

with $x_{DC}$ and $x_{AC}$ representing the nominal and variation in gap height respectively,
The time derivative is

\[
\frac{dC_{\text{VAR}}}{dt} = -\frac{\epsilon_0 A_0 x_{\text{AC}}}{[x_{\text{DC}} + x_{\text{AC}} \sin(\omega t)]^2} \cos(\omega t) .
\]  

(4.2)

Taking \( x_{\text{AC}} \ll x_{\text{DC}} \), the denominator of Eq. (4.2) is almost constant, resulting in the desired linearity.

From Fig. 4-5, it appears that the linear relationship holds fairly well; increases in the shaking strength lead to proportional increases in the capacitance variation. However, the trend line that best fit the data set is actually a third order polynomial, suggesting that the supporting cantilever beams exhibits spring-stiffening nonlinearities.

As a last step in characterizing the aluminum block capacitor, the quality factor both in air and vacuum will be roughly extracted. For the capacitive response as a function of input drive frequency given \( v_{\text{AMP, p-p}} = 20 \text{ mV} \), refer to Fig. 4-6. Changes in the resonance frequency and the maximum capacitance variation at resonance between the nominal and evacuated setup indicates functionality of the vacuum pump. By estimating \( Q \) using the “peakiness” of these two curves in a log-log plot, one

<table>
<thead>
<tr>
<th>( v_{\text{AMP, p-p}} ) (mV)</th>
<th>( v_{\text{OUT, p-p}} ) (mV)</th>
<th>( C_{\text{AC}} ) (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.0</td>
<td>0.25</td>
</tr>
<tr>
<td>5</td>
<td>11.2</td>
<td>0.94</td>
</tr>
<tr>
<td>10</td>
<td>25.6</td>
<td>2.14</td>
</tr>
<tr>
<td>15</td>
<td>41.6</td>
<td>3.47</td>
</tr>
<tr>
<td>20</td>
<td>54.0</td>
<td>4.50</td>
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<tr>
<td>30</td>
<td>82.0</td>
<td>6.83</td>
</tr>
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<td>35</td>
<td>92.0</td>
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<td>40</td>
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<td>8.83</td>
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<td>112.0</td>
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<td>50</td>
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<td>10.17</td>
</tr>
<tr>
<td>60</td>
<td>124.0</td>
<td>10.33</td>
</tr>
</tbody>
</table>

Table 4.1: \( C_{\text{AC}} \) of aluminum block capacitor as a function of shaking strength.
obtains that $Q_{\text{AIR}} \approx 2.6$ and $Q_{\text{VAC}} \approx 4.5$. The marginal change in quality factor, which is directly related to squeeze-film damping between the parallel plates, indicate that the partial vacuum, although sufficiently lower than atmospheric pressure, is not great.

4.2 Energy Harvesting with Aluminum Capacitor

Even assuming that the harmonic distorted waveform will not degrade the conversion efficiency of the energy flyback circuit, the measured $C_{\text{AC}}$ for the aluminum block capacitor, according to simulation, does not come close to the variation necessary for obtaining positive energy harvesting. Nevertheless, the variable capacitor was attached to the fabricated PCB and tested.

Although most of the energy harvesting circuit design has already been described in Chapter 3, a few components deserve additional attention. To decrease the amount
of reverse diode leakage, 1N6263W surface mount Schottky barrier diodes were chosen to serve as the two “automated switches.” The use of 2N7002E surface mount NMOS as the switch controlling the energy flyback path helped minimize the amount of gate capacitance seen by the clock signal. Finally, in order to generate a narrow 4 μs pulse for driving the NMOS gate, the CD4047BCN low power monostable multivibrator chip by Fairchild was employed.

To startup the energy harvester, some initial charges must be placed on $C_{RES}$. This is accomplished by connecting batteries through a shorted jumper to the reservoir capacitor at the beginning of the experiment. Then, the jumper connection is removed to allow the reservoir voltage to evolve over time, with positive change indicating success of the energy harvester.

As stated in Chapter 3, the use of oscilloscope probes will inevitably drain energy out of the system due to resistive losses. This effect is reduced in half by placing 10 MΩ resistors in series with the probes; however, this also means that the measured PCB test point voltages will be half the actual values. This important point must be kept in mind while looking through the remaining oscilloscope waveforms in this chapter.
With the energy flyback MOSFET driven by a 492.56 Hz clock signal, which is approximately \( f/4 \) where \( f \) represents the shaker frequency, the AC voltage waveform on the temporary storage node, \( v_S \), looks like Fig. 4-7 when \( v_{AMP,p-p} = 100 \) mV. First, notice that the triangularly shaped waveform exhibits a frequency that matches \( f_{CLK} \). This makes sense since the two diodes continue to pump charge onto \( C_S \) until the inductive flyback path is enabled, at which point energy flows from the temporary storage node back into \( C_{RES} \). The individual charge pumping process, which occurs at \( 4 \times f_{CLK} \), accounts for the humps between the energy flyback points.

The HSPICE simulation deck parameters were modified to match this particular setup, with \( C_{DC} = 752.4 \) pF and \( C_{AC} = 10.33 \) pF. Refer to Fig. 4-8 for the simulation results. Certainly, the general shape of \( v_S \) matches quite well. Furthermore, a comparison of the peak-to-peak voltage amplitudes show that simulation quantitatively describe the actual waveform with reasonable accuracy. Accounting for peaking, \( v_{S,p-p} = 40 \) mV for the simulated waveform and \( v_{S,p-p} = 30 \) mV for the actual waveform.

With \( v_S \) verified, the next step is to examine an important indicator that shows
whether positive net energy results. If the diode energy harvesting circuit is to succeed, \( v_{\text{RES}} \) must rise without the presence of any external power supplies except the vibrational source. By precharging \( v_{\text{RES}} \) to \( v_{\text{INIT}} \) and "loading" the reservoir node with an oscilloscope probe, the first order decay at that node can be monitored under different shaking strengths to determine the efficiency of the inductive energy flyback.

Waveforms of \( v_{\text{RES}} \) for both \( v_{\text{AMP},p-p} = 0 \) mV and \( v_{\text{AMP},p-p} = 100 \) mV are shown in Fig. 4-9. Unfortunately, due to the limitation in capacitance variation for the aluminum block capacitor, no significant differences can be observed between the two cases. This failure necessitates the need to find a better variable capacitor design.

### 4.3 Design of a Cantilever Beam Capacitor

The previous variable capacitor did not result in positive net energy conversion because the amount of capacitance variation required for success was not known when it was designed for [11]. The present goal of the redesign includes a target \( C_{\text{DC}} = 500 \) pF, a \( C_{\text{MAX}}/C_{\text{MIN}} \) ratio greater than 2, an out-of-plane resonant frequency
3.6.035
6.03
6.025
6.02
6.015
6.01
6.005
6
5.995
5.99
0
2m
4m
Time (tin) (TIME)

Figure 4-8: HSPICE waveform of $v_S$ for $C_{DC} = 752.4$ pF and $C_{AC} = 10.33$ pF. Here, $C_{RES} = 1 \mu F$, $C_S = 3.3$ nF, $R_P = 20$ M$\Omega$, $L_{FB} = 2.5$ mH, $R_C = 360$ k$\Omega$, $R_W = 8$ $\Omega$, $v_{INIT} = 6$ V, $t_{RISE} = t_{FALL} = 15$ ns, $v_L = 0.3$ V, $v_H = 4.2$ V, $f_{CLK} = 475$ Hz, and $D = 0.0019$. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

$f_{MECH} = 1900$ Hz. To prevent unwanted in-plane rotational or twisting motion, other resonant modes should be kept well above 1900 Hz.

4.3.1 Qualitative Description

Cantilever beam design used in the first variable capacitor will again be employed in the modified version. However, to decrease the amount of distortion and increase $C_{AC}$, the new design tethers the top plate via 8 beams to an outer frame, which in turn is firmly attached to a thick bottom metal plate. When the bottom plate is screwed onto the shaker table and shaken, the cantilevers will bend and provide the out-of-plane motion necessary for creating the capacitance variation. The amount of vertical travel for the top plate will depend directly on the stiffness of the cantilever beams.
4.3.2 Setting the Effective Spring Constant

From fundamental physics, the natural frequency of a spring-mass system is simply

$$\omega_n = 2\pi f = \sqrt{\frac{k}{m}}$$  \hspace{1cm} (4.3)

where $k$ represents the effective spring constant and $m$ represents the oscillating mass. If damping due to drag force is introduced, the equation becomes

$$\omega' = 2\pi f' = \sqrt{\frac{k}{m} - \left(\frac{b}{2m}\right)^2}$$  \hspace{1cm} (4.4)

with the additional $b$ term representing the coefficient of damping.

A member of the spring steel family, 1095 blue-tempered and polished spring steel, was used for the top plate of the capacitor due to its ability to restore quickly from deformations; undesired changes in the plate’s flatness could result in shorts. This sets the density of the material at $\rho_{\text{steel}} \approx 7850 \text{ kg/m}^3$ and the Young's Modulus at $E_{\text{steel}} = 205 \text{ GPa}$. 

Figure 4-9: Waveform of $v_{\text{RES}}$ for aluminum capacitor with different shaking.
To arrive at a preliminary design, some estimations will be made. First, even though the final variable capacitor will have its top plate attached to an outer frame through a number of cantilever beams, the total mass of the cantilever beams is assumed to be small compared to the center proof mass. Furthermore, squeeze-film damping, a result of air being pushed out horizontally as the top plate approaches the bottom plate rapidly, will also be ignored initially.

As a first guess, the center proof mass area, $A_C$, is set at $16 \text{ cm}^2$, with each side being 4 cm. Also, the thickness of the spring steel, $H$, is chosen to be 0.3 mm. These parameters completely determine $m$ as

$$m = \rho_{\text{STEEL}} A_C H = 3.84 \text{ g}.$$  \hspace{1cm} (4.5)

Therefore, to achieve $f_{\text{MECH}} = 1900 \text{ Hz}$,

$$k = [2\pi (1900 \text{ Hz})]^2 (3.84 \text{ g}) = 547.265 \text{ kN/m}$$  \hspace{1cm} (4.6)

### 4.3.3 Dimensioning the Cantilever Beams

Because the top plate is tethered to the frame using 8 rectangular cantilever beams, each beam need only exhibit an effective spring constant of 68.41 kN/m. To derive the spring constant equation for a single beam, the boundary conditions on both side must be specified. Given that the frame cannot vibrate, the beam edge next to the frame will have both zero displacement and zero slope. The other edge, attached to the center proof mass, will have non-zero displacement but remain relatively horizontal; to simply calculations, the slope of the beam at this edge is taken to be zero.

From [17], the effective spring constant of such a beam is

$$k = W \left( \frac{H}{L} \right)^3 E$$  \hspace{1cm} (4.7)
where $W$ is the width, $L$ is the length, and $H$ is the thickness. To make the final capacitor fit reasonably into a vacuum chamber, the length is chosen to be $L = 0.8$ cm. Since the thickness is 0.3 mm as selected earlier, $W = 0.633$ cm.

### 4.3.4 Gap Engineering

The goal of the design included achieving $C_{DC} = 500$ pF, which was chosen based on HSPICE simulations performed in Chapter 3. To obtain this capacitance based on the $A_C$ of the top plate, the gap between the top plate and bottom plate needs to be

$$d = \frac{\varepsilon_0 A_C}{C_{DC}} = 28.3 \mu m .$$  \hspace{1cm} (4.8)

This distance is very close to the thickness of the Mylar tape spacers used in the original variable capacitor; therefore, strips of Mylar tape also serve to separate the top and bottom capacitor plate in the new design. The theoretical $C_{DC}$ is therefore

$$C_{DC} = \frac{\varepsilon_0 A_C}{25 \mu m} = 566.4 \text{ pF} .$$  \hspace{1cm} (4.9)

Hence, to achieve $C_{MAX}/C_{MIN} \gg 2$, the capacitor must produce $C_{AC} > 190$ pF.

### 4.3.5 Calculating the Capacitance Variation

In order to gauge the ability of the new variable capacitor to produce top plate out-of-plane movement, a mechanical model of the shaker system was developed, as shown in Fig. 4-10. There are essentially 3 forces that act upon the top plate proof mass: acceleration force due to the shaker, viscous force due to squeeze-film damping, and the restoring spring force. In the calculation below, gravitational force is ignored for simplicity. By dividing the absolute position between a stationary ground reference plane and the bottom surface of the proof mass up into two sections, one being the positional variation of the shaker and the other being the distance between the bottom
and top capacitor plates, and applying Newton's Third Law,

\[ m \frac{d^2}{dt^2} [x(t) + y(t)] + b \frac{dy(t)}{dt} + ky(t) = 0. \]  

(4.10)

Manipulating Eq. (4.10) a bit, one sees that

\[ m \frac{d^2 x(t)}{dt^2} = - \left( \frac{d^2 y(t)}{dt^2} + b \frac{dy(t)}{dt} + ky(t) \right), \]  

(4.11)

with the left hand side of the equation representing the apparent force supplied by the shaker table. At the out-of-plane resonance frequency, the first and last terms on the right hand side cancel, leaving

\[ m \frac{d^2 x(t)}{dt^2} = -b \frac{dy(t)}{dt}. \]  

(4.12)

As mentioned earlier, the shaker table exhibits at most \( \frac{dx(t)}{dt^2} = 1147 \) m/s². Furthermore, the proof mass is \( m = 3.84 \) g. Therefore, the only variable necessary for figuring out \( \frac{dy(t)}{dt} \) is the coefficient of damping for an evacuated system. For a set of
rectangular parallel plate, the coefficient of damping is derived in [18]:

$$b = 0.427 \mu_{\text{AIR}} \frac{A_C^2}{d^5}.$$  \hspace{1cm} (4.13)

Here, $\mu_{\text{AIR}}$ represents the coefficient of viscosity for air under the environment of interest (at atmospheric pressure, $\mu_{\text{AIR},0} = 1.74 \times 10^{-5}$ kg/m-s). $A_C$ is the plate area and $d$ is the plate separation. Hence, at atmospheric pressure, $b_0 = 1217.3$ N-s/m given a plate area of 16 cm$^2$ and a separation of 25 $\mu$m.

In an evacuated system where the air pressure is high enough that the gas can still be considered a continuum, [19] shows that through an empirical fit,

$$\mu_{\text{AIR}} = \frac{\mu_{\text{AIR},0}}{1 + 9.658 k_n^{1.159}}$$  \hspace{1cm} (4.14)

with $k_n$ being the Knudsen number of the system. In general,

$$k_n = \frac{\lambda}{l}$$  \hspace{1cm} (4.15)

where $\lambda$ is the molecular free path and $l$ is the dimension of the body, which in this case is simply the distance between the moving plate and the stationary "wall" beneath it. Finally,

$$\lambda \approx 5 \text{ cm}/P$$  \hspace{1cm} (4.16)

with $P$, measured in mTorr, being the pressure of the evacuated system.

Because the vacuum chamber does not house a pressure gauge, the pressure of the achieved vacuum inside cannot easily be measured. Assuming a final pressure of 760 mTorr, which is 0.1 % of atmospheric pressure,

$$\lambda = \frac{5 \text{ cm}}{0.001 \times 760,000 \text{ mTorr}} = 65.79 \text{ $\mu$m}.$$  \hspace{1cm} (4.17)

This means that

$$k_n = \frac{65.79 \text{ $\mu$m}}{25 \text{ $\mu$m}} = 2.6316$$  \hspace{1cm} (4.18)
and therefore $\mu_{\text{AIR}} = 0.568 \times 10^{-6}$ kg/m-s. Finally,

$$b = \frac{\mu_{\text{AIR}}}{\mu_{\text{AIR},0}} \times b_0 = 39.81 \text{ N-s/m}.$$  \hspace{1cm} (4.19)

Referring back to Eq. (4.12) and assuming a purely sinusoidal acceleration from the shaker table,

$$\frac{dy(t)}{dt} = -\frac{m \frac{d^2x(t)}{dt^2}}{b} = -0.111 \sin(\omega t) \text{ m/s},$$  \hspace{1cm} (4.20)

which means that the vertical travel will be

$$y(t) = -0.111 \int \sin(\omega t) \ dt = y_o + \frac{0.111}{\omega} \cos(\omega t),$$  \hspace{1cm} (4.21)

where $y_o$ stands for the nominal gap size of 25 $\mu$m. Given that $f_{\text{MECH}} = 1900$ Hz, the amount of vertical travel in one direction is 9.3 $\mu$m, which results in a capacitance variation of

$$\frac{C_{\text{MAX}}}{C_{\text{MIN}}} = \frac{y_o + 9.3 \ \mu m}{y_o - 9.3 \ \mu m} = 2.1.$$  \hspace{1cm} (4.22)

This ratio assumes equal travel on both sides of the nominal plate position, which is a good first order approximation but might not be true for the fabricated capacitor.

### 4.3.6 Second-Order Spring Constant Consideration

It is known [17] that the effective spring constant of a cantilever beam can change when significant stretching occurs in the lengthwise direction. To see if this effect must be taken into consideration, the ratio of $\Delta L/L$ for the tethering cantilever beams will now be calculated. Fig. 4-11 shows a cantilever beam bent upwards when the center proof mass has reached its maximum vertical travel. In this figure, $L$ is the nominal length of the beam and $L'$ is the stretched length. The amount that the proof mass moves, 9.3 $\mu$m, corresponds to the value calculated in the previous section.
Figure 4-11: Cantilever beam when the proof mass is at maximum vertical travel.

Modeling the stretched beam as a “raised cosine,” one can write that

\[ y(x) = -4.65 \cos \left( \frac{2\pi x}{1.6 \text{ cm}} \right) \mu m + 4.65 \mu m \] (4.23)

by taking the horizontal direction as the x-axis and noting that the original length is \( L = 0.8 \text{ cm} \) as designed earlier. Integrating small segments of the line across the desired region,

\[ L' = \int_{0 \text{ cm}}^{0.8 \text{ cm}} ds \] (4.24)

\[ = \int_{0 \text{ cm}}^{0.8 \text{ cm}} \sqrt{1 + \left( \frac{dy}{dx} \right)^2} \, dx \] (4.25)

\[ = \int_{0 \text{ cm}}^{0.8 \text{ cm}} \sqrt{1 + \left[ \frac{4.65 \times 2\pi}{1.6 \times 10^4 \sin \left( \frac{2\pi x}{1.6 \text{ cm}} \right)} \right]^2} \, dx . \] (4.26)

Using the Taylor series expansion of

\[ (1 + x)^p = 1 + px + \frac{p(p - 1)}{2!} x^2 + \cdots , \] (4.27)

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which holds when $|x| < 1$, Eq. (4.26) can be approximated as

$$L' \approx \int_{0.8 \text{ cm}}^{0.8 \text{ cm}} \left[ 1 + \frac{1}{2} \left( \frac{4.65 \times 2\pi}{1.6 \times 10^4 \text{ cm}} \sin \left( \frac{2\pi x}{1.6 \text{ cm}} \right) \right)^2 \right] dx .$$ (4.28)

To simply calculation, define

$$\alpha = \frac{1}{2} \left( \frac{4.65 \times 2\pi}{1.6 \times 10^4 \text{ cm}} \right)^2, \quad \beta = \frac{2\pi}{1.6 \text{ cm}}$$ (4.29)

so Eq. (4.28) becomes

$$L' \approx \int_{0 \text{ cm}}^{0.8 \text{ cm}} \left[ 1 + \alpha \sin^2 (\beta x) \right] dx$$ (4.30)

$$= \int_{0 \text{ cm}}^{0.8 \text{ cm}} \left[ 1 + \alpha \left[ \frac{1}{2} - \frac{1}{2} \cos (2\beta x) \right] \right] dx$$ (4.31)

$$= \left[ (1 + \frac{\alpha}{2}) x - \frac{\alpha}{4\beta} \sin (2\beta x) \right]^{0.8 \text{ cm}}_{0 \text{ cm}}$$ (4.32)

$$= 0.80000067 \text{ cm} .$$ (4.33)

Therefore, the strain on the cantilever beam is

$$\epsilon \equiv \frac{\Delta L}{L} = \frac{L' - L}{L} = 83.36 \mu\% .$$ (4.34)

By multiplying the result of Eq. (4.34) with $E_{\text{STEEL}}$ and the cross-sectional area of the spring, one can determine the additional force caused by spring stiffening. For the dimensions used in the variable capacitor,

$$F_{\text{STIFF}} = \epsilon EW \text{H} = 0.325 \text{ N} .$$ (4.35)

This force is negligible when compared to the shaker table output of 178 N under naturally cooled conditions, meaning that second-order variations on the effective spring constant can be safely ignored.
4.3.7 Design Verification Using FEM

The previous sections presented a rather idealized design methodology for the variable capacitor. In order to more accurately determine the behavior of this design when it is subject to additional second-order effects that are not easily calculated, the paper design was placed into Pro/Engineer Wildfire for a finite element analysis. Results from the preliminary design are shown in Fig. 4-12. FEM indicates that the critical resonant mode, namely the out-of-plane mode, actually occurs at 470 Hz instead of the desired 1.9 kHz. Plate torsion and rotation occurs at 987 Hz and 995 Hz respectively, which is close enough to the desired resonant frequency that they can potentially be problematic.

There are several reasons why the FEM results differ so drastically from the hand calculations:

1. The “beams” are actually short and wide, which means that they behave more like plates than cantilever beams. Hence, the effective spring constant equation
used in earlier analysis is not precise.

2. No guiding mass exists on the top plate to prevent plate deformation, a phenomenon that invalidates the assumed zero slope boundary condition applied to the inner edge of the cantilever beam.

3. Hand calculation ignored the mass of the 8 cantilever beams; they can slightly decrease the resonant frequency.

The first two reasons likely accounts for most of the discrepancies. Instead of recomputing the theoretical resonance frequency using plate theory, the preliminary design was modified directly in Pro/Engineer Wildfire and simulated until the desired frequency occurred.

After several design iterations, the following 3 changes were made to the original design:

1. Spring steel thickness was increased from 0.3 mm to 1.27 mm. This provides a tremendous boost in the spring constant since \( k \propto \left( \frac{H}{L} \right)^3 \).

2. All the cantilever beam widths were increased from 0.633 cm to 0.7 cm. This change increased the spring constant enough to achieve the desired resonant frequency.

3. Curvatures of 2 mm in radius were inserted in all perpendicular intersections. The main advantage of this modification relates to the decreased stress level observed in the top capacitor plate, which can extend the time before the plate fatigued and failed.

The final simulated design exhibits an out-of-plane resonance mode at 1.917 kHz and unwanted secondary resonances beyond 6.448 kHz. A factor of 3 separating the desired and undesired resonance helps reduce the chance that the unwanted modes will be accidentally excited. Fig. 4-13(a) shows the AutoCAD design file used to cut
Figure 4-13: Final design for the new variable capacitor, completely assembled.

4.3.8 Additional Design Considerations

There are a few caveats to consider before leaving the topic of the variable capacitor behind. First, because the bottom capacitor plate is machined from a solid piece of aluminum, the screws holding the structure together must be made out of nylon to
prevent the top and bottom plates from shorting. The nylon screws require calibration before the beginning of each experiment since vibration and thermal gradients can easily cause the tightness to change, altering the amount of capacitance variation observed. Furthermore, because outer casing of the shaker table is grounded, care must be taken to either insulate the bottom plate from the shaker using a layer of Mylar tape or have the bottom plate serve as the ground node when the capacitor is connected to the energy harvesting circuit.

4.4 Characterizing the Cantilever Beam Capacitor

Before placing the redesigned capacitor into the energy harvesting circuit, the variable capacitor will be characterized, similar to the aluminum block capacitor. Using a standard bridge, the nominal capacitance is determined to be $C_{DC} = 650 \text{ pF}$, which is close to the predicted value of 566.4 pF. The additional undesired capacitance stems from the outer frame of the top capacitor plate.

Although the original design envisioned the variable capacitor encased in the vacuum chamber, experiments indicate that the chamber exhibits inferior mechanical behavior, in part due to the slightly tilted supporting screw that holds the chamber and capacitor together. Rather than making a new vacuum chamber, the new capacitor was connected by a nylon screw directly to the shaker table and tested. Perhaps due to the altered geometries, water does not condense between the plate even during heavy shaking. Therefore, all of the following data corresponds to the new variable capacitor operating in atmospheric pressure, with the bottom capacitor plate grounded. The reason for grounding the bottom plate instead of the top will be explored in a later section.

Because the designed $f_{MECH}$ did not incorporate the effect of squeeze-film damping, which can lower the resonance frequency significantly, a frequency sweep was first performed on the structure to determine the atmospheric out-of-plane reso-
nance point. For the capacitive response as a function of input drive frequency given $v_{\text{AMP,p-p}} = 100 \text{ mV}$, refer to Fig. 4-14. The resonance frequency is $f_{\text{MECH}} = 1560 \text{ Hz}$ with $Q \approx 3.5$, but because the resonance waveform is less distorted at heavy shaking for $f = 1500 \text{ Hz}$, data shown below are all run at this lower frequency unless otherwise noted.

Just like the aluminum block capacitor, the cantilever beam design should have relatively linear response at low shaking levels (refer to Eq. (4.2)). Refer to Fig. 4-15 for the experimental data. As expected, the response is almost linear until the shaker table amplifier reaches $v_{\text{AMP,p-p}} = 300 \text{ mV}$, at which point the response begins to saturate. Compared the the aluminum block capacitor, whose response appears in Fig. 4-5, the new design can reach much greater $C_{AC}$ and the saturation occurs at a much gentler pace.

For the new capacitor design, one might be interested in looking at the actual $dC/dt$ waveforms at the output of the $C_{AC}$ measurement amplifier circuit. Fig. 4-16 shows the responses for 3 different shaking strengths — light, medium, and heavy. Doubling the shaking strength doubles the $v_{\text{OUT}}$ response to first order, but notice
that for heavy shaking, the waveform exhibits visible distortion near the top and bottom of the sinusoidal cycle, similar to the aluminum block capacitor. Nonetheless, the amount of harmonic distortion is visibly less compared to the previous capacitor design.

4.5 Energy Harvesting with Steel Capacitor

With the cantilever beam capacitor fully characterized, it is now placed into the energy harvesting circuit with the goal of allowing $v_{RES}$ to be sustained at a constant voltage level after the batteries used to precharge the reservoir to $v_{INIT}$ are removed. The ability to sustain the reservoir voltage directly implies that the generated power exceeds the dissipated power, which includes losses in the diode, MOSFET, inductor, and reservoir node scope probe. In order to facilitate visualization, $C_{RES}$ is charged up and allowed to freely evolve for 50 seconds as shaking occurs. As a baseline, the experiment is carried out with no shaking but the flyback MOSFET gate drive running; Fig. 4-17 shows the obtained data. Because the waveform decays toward
0 V, one can conclude sensibly that the energy harvesting circuit cannot sustain itself when no vibration energy enters the system. This waveform further suggests that the gate drive, carefully considered in Chapter 3 due to its ability to inject power into the system if not designed correctly, does not inject sufficient energy to keep the system going. As noted earlier, verifications similar to this one were not carried out in [12].

Next, a family of curves for increasingly heavy shaking are plotted together in Fig. 4-18. Below a certain threshold for $v_{\text{AMP},p-p}, 80 \text{ mV}$ in this case, no significant change in the decay rate is observed. This can be seen by comparing, for example, the $v_{\text{AMP},p-p} = 20 \text{ mV}$ curve to the baseline plot in Fig. 4-17.

Several points of interest exist when one carefully observes the family of curves. First, as expected, the first order decay time constant increases with increasing shaking. This makes sense because the decay constant $\tau_{\text{RES}}$ depends on the net power flow into and out of the reservoir node. The diode pumping charge into the variable capacitor and the scope probe attached to the reservoir both contribute to negative energy flow while the harvested energy sent back back from $C_S$ contributes positively.
Energy flow at $C_{RES}$ changes $v_{RES}$ according to

$$\Delta W = \frac{1}{2} C (v_{RES,F}^2 - v_{RES,O}^2) \tag{4.36}$$

where $\Delta W$ is the net energy flowing, $v_{RES,O}$ is the original node voltage, and $v_{RES,F}$ is the final node voltage. Since the original $dv_{RES}/dt$ is negative, experimental data indicate that at $v_{RES} = 6$ V, losses exceed generation. However, after approximately 25 seconds, a shaking strength $v_{AMP,p-p} \geq 160$ mV results in $v_{RES}$ flattening out, which shows that the net energy flow at the $C_{RES}$ node becomes zero.

It is also instructive to see that the energy harvesting circuit can generate a reservoir voltage that exceeds the original level of $v_{INIT}$. To observe this waveform, the shaker table is first configured to run off $v_{AMP,p-p} = 250$ mV for a few minutes to allow $v_{RES}$ to settle at the equilibrium point that the shaking level can sustain. Then, the oscilloscope is changed into single trigger mode and forced to trigger just when the shaking ramps up to $v_{AMP,p-p} = 380$ mV. Fig. 4-19 results after the trigger completes. One sees that as soon as the shaking level increases, $v_{RES}$ begins to rise in an exponential manner and manages to exceed $v_{INIT}$ after approximately 11 seconds.
Figure 4-18: First order decay at $v_{\text{RES}}$ for increasingly heavy shaking. The number immediately below the curve indicates the $v_{\text{AMP},p-p}$ used to generate that curve.

One can repeat the previous procedure to generate another family of curves, this time all rising, similar to the set found in Fig. 4-18. Due to limitations in shaking magnitude, the start voltage is now lowered to $v_{\text{INIT}} = 1.44$ V. Consult Fig. 4-20 for the results.

The difference between Fig. 4-18 and Fig. 4-9 can be attributed to the capacitor redesign, which significantly increased the upper limit of $C_{AC}$. Whereas the aluminum block capacitor failed to sustain the reservoir voltage above the baseline response, the spring steel capacitor easily achieves this. Before proceeding with a few verifications to prove that the success of the energy harvesting circuit does not come from energy sources other than the vibrating capacitor, a few additional caveats are explored and the achieved experimental data is compared against simulation.
4.6 Starting Up the System

Through this thesis, the energy harvesting circuit has always been assumed to evolve from a precharged state where $C_{RES}$ is charged to some predetermined voltage level $v_{INIT}$. When building up an actual system, the mechanism to deliver this initial charge becomes important. More critical, however, is the question concerning how much charge is enough to jump start the energy harvesting circuit. To answer this question, $v_{INIT}$ is lowered continually until the system no longer responds to the shaker table suddenly starting. Through numerous experimental trials, it was discovered that the lowest voltage level that can be seen on the oscilloscope (i.e. above the noise floor) is still sufficient to allow system startup. This voltage level corresponds to $v_{INIT} = 89$ mV. A sample startup sequence showing the energy harvesting circuit turning on from an initial voltage of $v_{INIT} \approx 200$ mV is shown in Fig. 4-21.
Figure 4-20: Rising curves at $v_{\text{RES}}$ for increasingly heavy shaking. The number immediately below the curves indicates the $v_{\text{AMP,pp}}$ used to generate that curve.

4.7 Sensitivity to Frequency Variation

Experiments conducted so far assumed that the shaking frequency perfectly matches the out-of-plane resonance frequency that the variable capacitor was designed for, enabling maximum capacitance variation in system. However, in any real-life application, an exact match cannot be expected at all time. To be useful, the operation of the energy harvesting circuit should not depend too strongly on such frequency matching. Fig. 4-22 shows the equilibrium voltage where $v_{\text{RES}}$ flattens out as a function of the shaker table drive frequency, which effectively simulates environmental vibration. Vibrations more than 150 Hz away from the designed center frequency causes the equilibrium voltage to drop more than 37%, meaning that the power available to an attached load drops down to 39% of the original quantity. Having said that, the system can be made to tolerate frequency variations by shaping the mechanical response of the variable capacitor into something less “peaky,” or equivalently, with a smaller quality factor $Q$. Of course, decreasing $Q$ means that the capacitance variation at the designed frequency suffers, so a trade-off exists. If one does not know
the spectrum of the environmental vibration \textit{a priori}, the variable capacitor might be designed to allow its $Q$ to be tuned actively.

4.8 Simulation Revisited

The HSPICE simulation deck used for simulating the aluminum block capacitor is modified to accommodate the new $C_{DC} = 650$ pF and a $C_{AC}$ range of 2.54 pF to 347.77 pF, representing almost no shaking to very heavy shaking. To test the accuracy of the simulation with respect to experimental data, simulation and experimental data points corresponding to $v_{AMP, p-p} = 320$ mV, which translates to $C_{AC} = 234.84$ pF, are compared. Referring back to Fig. 4-18, an accurate simulation model will result in net dissipation at the reservoir node when $v_{RES} > 4.6$ V and net generation when $v_{RES} < 4.6$ V. These two conditions are necessary for an equilibrium voltage level to occur at $v_{RES} = 4.6$ V when $v_{AMP, p-p} = 320$ mV.

However, running the simulation model at the said conditions actually results in net generation when $4$ V $\leq v_{RES} \leq 22$ V, indicating that the model is too optimistic.
Figure 4-22: Plot of $v_{RES}$ as a function of frequency with $v_{AMP,p-p} = 320$ mV.

The change from net generation to net dissipation at 22 V results from nonlinear device losses, as explained in Chapter 3. Therefore, to obtain an equilibrium point lower than 22 V, the prototype circuit must contain another source of nonlinear loss not modeled in the current simulation. One likely source of this nonlinearity is the inductor core loss, which is currently modeled as a linear resistive loss $R_C$.

To achieve a more accurate model of the inductor at $f_{MECH} = 1500$ Hz, the inductor is put in series with a low-loss 14.14 μF capacitor, as shown in Fig. 4-23, and driven with a function generator $v_{DR}$. The value of the capacitor was chosen such that the resonant frequency of the LC network came out at $f = 865$ Hz, which is close to the frequency of the variable capacitor vibration.

Normally, if the inductor core loss is linear, the ratio of $v_C/v_{DR}$ should remain constant for all values of $v_{DR}$. Experimentally, this ratio, as well as the phase lag $\phi_C$ between $v_{DR}$ and $v_C$, are plotted in Fig. 4-24 for $f = 865$ Hz. The voltage ratio and phase lag are not constant as the drive voltage from the function generator increases beyond 1.2 V peak-to-peak; this suggests that modeling the inductor core loss with a linear $R_C$ is very inaccurate.
Figure 4-23: LC network used to characterize the nonlinear inductor core loss.

Figure 4-24: Plot of $\frac{v_C}{V_{DR}}$ and $\phi_C$ as a function of $V_{DR,p-p}$ at $f = 865$ Hz.

In order to model the nonlinearity in HSPICE, the LC network is replicated in the simulation, but the inductor is now modeled using an ideal inductor, a wire loss resistor, and a core loss resistor that is “tuned” to give the correct $v_C/v_{DR}$ ratio for different $v_{DR}$. A schematic of this setup is shown in Fig. 4-25. When enough $R_C$ values are obtained, they can be combined to form a piecewise linear resistor whose resistance varies as its terminal voltage swings across different voltage zones.

Below $v_{DR,p-p} = 1.2$ V, the linear behavior of the inductor is modeled by $R_C = 400$ kΩ. Beyond that, as the voltage ratio of $v_C$ to $v_{DR}$ begins to drop, HSPICE indicates that the best $R_C$ to model the core loss drops abruptly from around 8 kΩ to
700 Ω as the driving voltage increases from 1.5 V peak-to-peak to 2.2 V peak-to-peak. This large change in $R_C$ shows that the low experimental equilibrium voltage levels are reasonable since higher $v_{RES}$ directly results in a larger voltage across the inductor terminals, which greatly increases core loss.

However, the modeled core loss of the inductor must still be put in context of the entire energy harvesting circuit. One cannot reasonably expect that an inductor characterization done in isolation can be placed back into the full circuit model and make the simulated equilibrium voltage level match experimental data without further tuning. Hence, using the characterized nonlinear core loss as a starting point, the piecewise linear function is tweaked until the simulation closely matches experimental data. A plot showing both the modified nonlinear resistor and the original experimental characterization appears in Fig. 4-26. The two piecewise linear functions, although not matching perfectly, shows very similar trends and magnitudes, indicating that a nonlinear inductor core loss does in fact explain the discrepancies between the original simulations and the experimental waveforms.

It is interesting to see the simulated waveforms after the nonlinear resistor has been incorporated into the inductor model. Fig. 4-27 shows the first order waveform $v_{RES}$ when $v_{INIT} = 6$ V, $C_{DC} = 650$ pF, and $C_{AC} = 234.84$ pF. The decaying $v_{RES}$ matches the experimental data in Fig. 4-18, which shows that the reservoir node cannot be maintained at 6 V with the given capacitance variation. From Fig. 4-18, the first order decay should reach equilibrium when $v_{RES} = 4.6$ V. This can be checked

![Figure 4-25: LC network used to model the nonlinear core loss in HSPICE.](image-url)
Figure 4-26: Comparison of the piecewise linear functions modeling $R_C$, one obtained directly from inductor characterization and the other obtained by fitting simulation results to experimental data.

by setting $V_{INIT} = 4.6$ V and seeing whether the waveform of $V_{RES}$ remains flat. The simulated result for this case, shown in Fig. 4-28, does indeed show an equilibrium voltage level at $V_{RES} = 4.6$ V.

4.9 Energy Conversion Verification

Earlier, it was shown that with the redesigned capacitor attached to the energy harvesting circuit, loaded at the reservoir node with a 10 MΩ resistor in series with a 10 MΩ scope probe, the system manages to sustain itself, indicating successful energy harvesting. However, some experimental verifications must occur in order to show that the ability for the system to sustain itself does not result from unaccounted energy sources.

As a first step, the loading at the reservoir node is stepped up by bypassing the 10 MΩ resistor, resulting in an effective 10 MΩ load due to the scope probe alone.
Figure 4-27: $v_{\text{RES}}$ as a function of time with nonlinear core loss. The circuit parameters used in simulation are $C_{\text{RES}} = 1 \mu F$, $C_s = 3.3 \text{ nF}$, $R_p = 20 \text{ M}\Omega$, $L_{FB} = 2.5 \text{ mH}$, $R_w = 8 \Omega$, $C_{DC} = 650 \text{ pF}$, $C_{AC} = 234.84 \text{ pF}$, $v_{\text{INIT}} = 6 \text{ V}$, $t_{\text{RISE}} = t_{\text{FALL}} = 15 \text{ ns}$, $v_L = 0.3 \text{ V}$, $v_H = 4.2 \text{ V}$, $f_{\text{CLK}} = 375 \text{ Hz}$, and $D = 0.0015$. $R_C$ is modeled as a piecewise linear resistor shown in Fig. 4-26. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

Since the power dissipated by a load of value $R$ is

$$P_{\text{DISS}} = \frac{v_{\text{RES}}^2}{R}$$

(4.37)

assuming that $v_{\text{RES}}$ does not change too much, dissipation due to the reservoir node scope probe should increase by a factor of 2. To establish a baseline behavior, the first order decay for $v_{\text{RES}}$ is observed experimentally when the shaker table is turned off; the result appears in Fig. 4-29. As expected, a smaller resistance causes the reservoir capacitor to discharge with a faster $\tau_{\text{RES}}$ and also reach a lower equilibrium voltage level.

Now, the same experiment is performed while the shaker table is shaking with $v_{\text{AMP},p-p} = 100 \text{ mV}$. If the same behavior occurs, one can infer that the scope probe is indeed dissipating power as it should. Results shown in Fig. 4-30 confirms that this
Figure 4-28: $v_{\text{RES}}$ as a function of time with nonlinear core loss. The circuit parameters used in simulation are $C_{\text{RES}} = 1 \mu F$, $C_S = 3.3 \, \text{nF}$, $R_P = 20 \, \text{M}\Omega$, $L_{\text{FB}} = 2.5 \, \text{mH}$, $R_w = 8 \, \Omega$, $C_{\text{DC}} = 650 \, \text{pF}$, $C_{\text{AC}} = 234.84 \, \text{pF}$, $v_{\text{INIT}} = 4.6 \, \text{V}$, $t_{\text{RISE}} = t_{\text{FALL}} = 15 \, \text{ns}$, $v_L = 0.3 \, \text{V}$, $v_H = 4.2 \, \text{V}$, $f_{\text{CLK}} = 375 \, \text{Hz}$, and $D = 0.0015$. $R_C$ is modeled as a piece-wise linear resistor shown in Fig. 4-26. The vertical axis represents voltage plotted in volts and the horizontal axis represents time plotted in seconds.

Various potential sources of energy injection are next considered, one at a time. When the capacitor was characterized in Section 4.4, the bottom capacitor plate was connected to ground. The main reason for choosing this over grounding the top plate becomes apparent when the output waveforms from the amplifier setup measuring $dC/dt$, shown in Fig. 4-31, are compared for the two cases. When the top plate is grounded, a lot of high frequency noise couples into the variable capacitor output. These noise most likely include power electronic switching noise present in the lab as well as radio waves traveling through the air. Although appearing with magnitudes in the mV regime, these noise could in theory couple energy through the capacitor between the bottom plate and the shaker table into the energy harvesting circuit, similar to the problem seen in Chapter 3 when energy coupled through the
MOSFET gate capacitor. Grounding the bottom plate reduces the noise feedthrough significantly, removing this potentially disastrous energy source.

Even though there exist little possibility of energy injection through the scope probes, this potential injection source is also tested. With the circuit sustaining itself, the probes at $C_{RES}$ and $C_S$ are removed, one at a time, to see whether $v_{RES}$ begins to decay. If $v_{RES}$ cannot be maintained when the probes are removed, then it is highly likely that energy injection from the oscilloscope exists. However, no such change are observed experimentally; the system continues to sustain $v_{RES}$ and the first order decay characteristic look exactly the same.

Finally, the elusive capacitive injection path that exists between the MOSFET gate driver and the energy harvesting circuit must be examined carefully. As mentioned earlier, the circuit can maintain $v_{RES}$ at a fixed voltage when the reservoir node scope probe is connected, meaning that at the minimum, the overall system is

---

1The probe measuring the waveform at $C_S$ does not contribute to power consumption since its coupling mode is set to “AC.” In this mode, any DC signal will see an infinite oscilloscope input resistance. Hence, in all the earlier simulations, the only parasitic resistance included is the one at the reservoir node.
Figure 4-30: $v_{\text{RES}}$ as a function of reservoir loading with $v_{\text{AMP, p-p}} = 100$ mV.

\[
P_{\text{GEN}} > \frac{v_{\text{RES}}^2}{R} = 1.8 \, \mu\text{W} ;
\]

the reader is reminded that $R$ is the equivalent resistance of two 10 M\(\Omega\) resistors in series. Now, consider the theoretical maximum that the gate driver could ever inject into the system, keeping in mind that in reality, such levels of injection is impossible since the MOSFET capacitor must discharge when the device turns off — only the amount of charge that leaks across the diode $D_2$ will contribute to the energy injection. This maximum is

\[
P_{\text{INJ, MAX}} = \frac{1}{2} C_{\text{GS}} v_{\text{GS}}^2 f
\]

where $C_{\text{GS}}$ is the MOSFET gate-source capacitance, $v_{\text{GS}}$ is the clock voltage, and $f$ is the clock frequency. Using $C_{\text{GS}} = 28$ pF, which was obtained in the datasheet for the 2N7002 MOSFET, $v_{\text{GS}} = 4.2$ V, and $f = \frac{1500}{4} = 375$ Hz, the maximum injected power from the clock is 0.1 \(\mu\text{W}\), which is less than 1.8 \(\mu\text{W}\) by a very safe margin.

To further prove that success of the energy harvesting circuit does not hinge on clock power injection, an experiment using two different levels of $v_{\text{GS}}$ is conducted. If
the sustained voltage level at $C_{RES}$ is not a function of $v_{GS}$, one can safely conclude that clock power injection is not an issue. This is because as stated in Eq. (4.39), the amount of injected power is proportional to $v_{GS}$, so if the system relied on such power injection, its behavior will change when $v_{GS}$ changes. The experimental result appears in Fig. 4-32; they show that since the clock voltage does not have a significant effect on the energy conversion, successful energy harvesting does not hinge on clock power injection.

### 4.10 Energy Conversion Efficiency

Having verified the behavior of the energy harvesting circuit, the only thing that remains to be calculated is the system’s efficiency. As a figure of merit, efficiency will be defined as

$$
\eta \equiv \frac{\text{Power delivered to load}}{\text{Theoretical power harvested from Q-V cycle}} \quad (4.40)
$$
Here, the numerator represents the amount of useful energy the energy harvesting circuit can provide and the denominator represents the theoretical maximum that the circuit would be able to deliver to the load if the process was 100% efficient. To make a fair comparison, the denominator will be calculated using circuit parameters of the actual prototype; if \( V_{\text{INIT}} \) could be made arbitrarily large, for example, the theoretical maximum would increase, but the comparison would not be fair.

As mentioned earlier, the prototype system is loaded at the reservoir node with a 20 M\( \Omega \) load. Hence, the amount of useful power delivered to the load is 1.8 \( \mu \text{W} \). To determine the denominator, it is instructive to explore the \( Q-V \) plane once more, this time tracing out the path that corresponds to the diode-based energy harvesting circuit. Refer to Fig. 4-33 for the trace; note that \( Q_{\text{VAR}} \) and \( C_{\text{VAR}} \) stands for the charge and capacitance of the variable capacitor respectively.

Begin the cycle by considering Point 1 in the figure, which corresponds to the moment when both diodes are off and the plates of the variable capacitor are beginning to pull apart. At this point,

\[
v_1 = v_{\text{INIT}} = 6 \text{ V}
\]  

(4.41)
Figure 4-33: \( Q \)-\( V \) plane trace representing theoretical harvesting maximum.

and therefore

\[
Q_{1,2} = C_{\text{MAX}} v_{\text{INIT}} = 5.8 \times 10^{-9} \text{ Cb} .
\]  

(4.42)

When Point 2 in the cycle is reached, the capacitor plates have moved apart to their maximum separation under charge-constrained conditions, and hence

\[
v_2 = \frac{Q_{1,2}}{C_{\text{MIN}}} = \frac{C_{\text{MAX}}}{C_{\text{MIN}}} v_{\text{INIT}} = 17.44 \text{ V} .
\]  

(4.43)

The trace between Point 2 and Point 3 represents the voltage equalization between \( C_{\text{VAR}} \) and \( C_S \) when \( D_2 \) turns on. By charge conservation, one can write

\[
v_3 = \frac{Q_{1,2} + Q_S}{C_{\text{MIN}} + C_S} = 7.05 \text{ V} .
\]  

(4.44)

\( Q_S \) in Eq. (4.44) represents the amount of charge on \( C_S \) before the equalization occurs. From this, one can also deduce that

\[
Q_{3,4} = C_{\text{MIN}} v_3 = 2.3 \times 10^{-9} \text{ Cb} .
\]  

(4.45)
Finally, the capacitor plates move toward each other until the maximum capacitance occurs at Point 4. Here,

\[ v_4 = \frac{Q_{3,4}}{C_{\text{MAX}}} = 2.38 \text{ V}. \quad (4.46) \]

Having determined all the critical values, one can calculate the area enclosed by the trace, which represents the amount of harvested energy per cycle. To do this, areas \( A_1 \), \( A_2 \), and \( A_3 \) are computed:

\[
A_1 = \frac{1}{2} (v_1 - v_4) (Q_{1,2} - Q_{3,4}) = 5.25 \times 10^{-9} \text{ J} \quad (4.47)
\]

\[
A_2 = \frac{1}{2} (v_2 - v_3) (Q_{1,2} - Q_{3,4}) = 18.18 \times 10^{-9} \text{ J} \quad (4.48)
\]

\[
A_3 = (v_3 - v_1) (Q_{1,2} - Q_{3,4}) = 3.68 \times 10^{-9} \text{ J}. \quad (4.49)
\]

Therefore, the theoretical maximum harvested energy per cycle is

\[
W_{\text{IN}} = A_1 + A_2 + A_3 = 27.11 \text{ nJ}, \quad (4.50)
\]

which means that

\[
P_{\text{IN,MAX}} = W_{\text{IN}} f_{\text{MECH}} = 40.67 \mu\text{W}. \quad (4.51)
\]

Finally, referring back to Eq. (4.40),

\[
\eta = \frac{1.8 \mu\text{W}}{40.67 \mu\text{W}} = 4.43\%. \quad (4.52)
\]

If desired, one can also compute an efficiency value that takes into account the losses in the MOSFET and diodes. The difference between this computation and the previous stems from the fact that including the active device losses means that the actual amount of energy harvested can be compared to the theoretical maximum found in Eq. (4.51). Referring back to Eq. (2.35) and Eq. (2.36) and looking up the datasheets for the active devices,

\[
(P_{\text{FET,COND}}) \approx (14.14 \mu\text{A})^2 (1.8 \Omega) = 0.36 \text{ nW} \quad (4.53)
\]

118
and

\[ \langle P_{D,COND} \rangle \approx (10 \ \mu A) (0.2 \ V) = 2 \ \mu W . \]  \hspace{1cm} (4.54)

Adding these losses to the power delivered to the load, one obtains that

\[ \eta' = \frac{3.8 \ \mu W}{40.67 \ \mu W} = 9.34 \% . \]  \hspace{1cm} (4.55)

### 4.11 Chapter Summary

A prototype energy harvesting circuit which can sustain itself while loaded by one 20 MΩ load has been built and fully characterized in this chapter. The first variable capacitor built out of two aluminum blocks could not travel enough vertically, resulting in insufficient \( C_{AC} \) to allow the power electronics to successfully convert positive net energy. A redesigned version using cantilever beam theory resulted in much larger capacitance variation and significantly less harmonic distortion for heavy shaking. After verifying that the new variable capacitor could sustain \( v_{RES} \) indefinitely, various experiments were performed to verify that the success of the circuit did not depend on any unaccounted power source other than the vibrating capacitor. Finally, an estimated efficiency was computed for the prototyped circuit.
Chapter 5

Summary, Conclusions, and Possible Future Work

Having gone through the entire process of exploring a novel diode-based energy harvesting topology, from fundamental circuit theory to HSPICE simulations and system prototyping, one might wonder what further improvements can be made to the harvesting system. Before answering that question, each chapter will first be summarized briefly and the important conclusions will be highlighted. Numerous suggestions on future improvements to the system follow, under the assumption that the energy harvesting circuit will eventually be integrated with the variable capacitor onto a MEMS IC. Finally, several points will be made with regards to the interface between electronic loads and the energy harvesting circuit.

5.1 Chapter Summaries

Chapter 1 introduced the concept of energy harvesting and suggested the most common strategies — piezoelectric, magnetic, and electric. Magnetic energy harvesting was further divided into systems that used a variable inductor and systems that em-
ployed moving magnets. Likewise, electric energy harvesting could be done using either a variable capacitor or permanent electrets. After numerous motivational applications, including autonomous sensors and alternative green energy sources, were given, a comprehensive literature review of all the common strategies followed in Section 1.3. Macro scale piezoelectric energy harvester, reported in [5], managed to produce 80 mW of power using unimorphs, while those on the micro scale, shown in [8], delivered 375 µW to a resistive load. Glynne-Jones et al achieved an average power of 157 µW using a permanent magnet harvester [3]. Finally, Miyazaki et al described a capacitive electric energy harvesting circuit in [12] that generated 120 nW of power using the circuit topology proposed by Mur-Miranda in [11].

Chapter 2 provided the theoretical foundations useful for understanding the capacitive energy harvesting circuits presented in this thesis. Section 2.1 introduced the concept of a $Q-V$ plane and related contours in this plane to the electrical and mechanical behavior of the energy harvester. Two typical cases, the charge-constrained and voltage-constrained cycle, were shown, and a synchronous harvester topology using two MOSFET switches [11] was given in Section 2.2 as a circuit example that employed charge-constrained cycles. Weakness in this topology lead to the proposal of an asynchronous diode-based topology, the topic of this thesis, that did not require complicated clocking schemes. The charge pump portion of this topology was analyzed separately, both with and without the parasitic diode capacitances; this lead to Eq. (2.15) and Eq. (2.34). Then, three different types of energy flyback mechanisms — inductor, direct shorting switch, and capacitive bucket brigade — were discussed in Section 2.5 and Section 2.6, and the maximum theoretical efficiency for each was derived. Finally, circuits that can measure $C_{DC}$ and $C_{AC}$ of a variable capacitor were described.

In Chapter 3, the theoretical derivations presented in Chapter 2 were compared against simulated results with the help of HSPICE. To allow for maximum precision, the simulation used accurate model files for active components and included the effects of various parasitics such as scope probe resistance and inductor core loss.
HSPICE indicated that when the charge pump portion was acting alone, the energy harvester successfully harvested 6 nJ after four mechanical cycles. Section 3.7, Section 3.8, and Section 3.9 investigated the flyback portion of the energy harvester by first using an abrupt variable resistor and then the actual model file to represent the MOSFET switch in the flyback path. In the latter two of these three sections, both a ground-referenced and a source-referenced gate drive were explored. The result of these simulations appeared in Table 3.2 and Table 3.4. Finally, circuit parameters, including the clock frequency, duty ratio, capacitor sizes, and MOSFET gating strength, were optimized through a series of HSPICE iterations. This optimization procedure produced the following parameter values: $C_{\text{RES}} = 1 \ \mu\text{F}$, $C_S = 3.3 \ \text{nF}$, $R_P = 20 \ \text{M\Omega}$, $L_{FB} = 2.5 \ \text{mH}$, $R_C = 360 \ \text{k\Omega}$, $R_W = 8 \ \Omega$, $v_{\text{INIT}} = 6 \ \text{V}$, $t_{\text{RISE}} = t_{\text{FALL}} = 15 \ \text{ns}$, $v_L = 0.3 \ \text{V}$, $v_H = 5 \ \text{V}$, $f_{\text{CLK}} = 475 \ \text{Hz}$, and $D = 0.0019$. Using these values, the capacitive energy harvester converted approximately 0.8 $\mu\text{W}$ of power.

Chapter 4 presented the experimental results of a prototype circuit built using the optimized parameters. Two different capacitor designs were explored, one being the aluminum block capacitor used in [11] and the other being a cantilever beam variable capacitor made from spring steel. The aluminum block capacitor was characterized in Section 4.1 to have $C_{\text{DC}} = 752.4 \ \text{pF}$ and $C_{\text{AC}} = 10.33 \ \text{pF}$ (refer to Fig. 4-5). This variable capacitor was placed into the capacitive energy harvester and tested; resulting waveforms appear in Section 4.2. Similar to the aluminum block capacitor, the spring steel variable capacitor was designed in a finite element modeling package, characterized, and placed into the harvester. In the end, the spring steel capacitor exhibited $C_{\text{DC}} = 650$ and $C_{\text{AC}} = 347.77 \ \text{pF}$. Using this capacitor, experiments were carried out using the oscilloscope probe as a load to determine the amount of energy harvested. Fig. 4-19 and Fig. 4-20 both show successful energy harvesting using the spring steel variable capacitor. After the possibility of spurious clock energy injection was ruled out in Section 4.9, the HSPICE simulations were revisited in an attempt to close the differences between simulated and experimental data. Finally, in Section 4.10, the overall energy conversion efficiency of the asynchronous capacitive
energy harvesting circuit was calculated to be 4.43 % based on the 1.8 $\mu$W of power it harvested.

5.2 Important Conclusions

Several important insights come directly from the analysis of the charge pump and flyback mechanism in Chapter 2. Eq. (2.15) and Eq. (2.34) show that parasitic diode capacitances hurt the energy conversion efficiency by limiting the highest value that $v_S$ can reach. These two equations also suggest that in order to make the energy harvester work, the ratio $C_{\text{MAX}}/C_{\text{MIN}}$ must be maximized; hence, parasitic capacitances parallel to the variable capacitor must also be carefully controlled. Analysis done in Section 2.5 and Section 2.6 lead to the conclusion that an inductive flyback works best compared to the direct shorting switch and capacitive bucket brigade because of its high theoretical flyback efficiency and simple implementation. Bucket brigade flyback actually performs worse as more and more capacitive stages are added, a phenomenon that is not at all obvious.

Circuit simulation in Chapter 3 not only confirmed the theory derived in Chapter 2 but also lead to additional conclusions. First, simulation results shown in Fig. 3-5 and Fig. 3-6 confirm that an energy flyback mechanism is critical to the success of this harvester topology since $v_S$ would quickly saturate otherwise. More importantly, however, the data shown in Table 3.2 and Table 3.4 suggest that it is possible for the clocking signal of the MOSFET to inadvertently inject energy into the harvesting circuit. As either the clock voltage or frequency increases for the ground-referenced case, the converted energy also increases. This is not observed when a source-referenced gate drive is used, however. Therefore, in order to obtain accurate results for a capacitive energy harvesting circuit that requires gate drives, any spurious energy injection must be either prevented a priori or subtracted from the overall converted energy.

The experimental implementation of the capacitive energy harvesting circuit in
Chapter 4 leads to many interesting findings as well. As accentuated by Section 4.2 and Section 4.5, the experimental setup confirms that a large $C_{\text{MAX}}/C_{\text{MIN}}$ ratio is critical in achieving net positive energy conversion. Furthermore, Eq. (4.34) and Eq. (4.35) show that second-order spring stiffening effects are not critical to macro scale variable capacitor designs as long as the vibration source exhibits a large enough force. Based on Section 4.6, it appears that the energy harvesting circuit can be started up using just a piezoelectric film since the system functions with $V_{\text{INIT}}$ as low as 89 mV. Finally, an important conclusion can be made about the flyback inductor modeling. Due to nonlinear inductor core loss that occurs around the circuit operation frequency of 1500 kHz, $R_L$ in the HSPICE simulation must be represented as a piecewise linear resistor in order to achieve a good match between simulated and experimental data. The inductor characterization process can be found in Section 4.8.

5.3 Future Improvements

Although the prototype circuit successfully sustained its reservoir voltage when driving a resistive load, there are numerous improvements that can be made to the energy harvesting circuit both to make it more feasible in real-life applications and to improve its efficiency. Perhaps the most glaring omission from this thesis is any indication of a flyback control loop that automatically adjusts the MOSFET gate drive. In the simulation and experiments, the clock frequency on the gate was manually set to the optimized $f_{\text{MECH}}/4$ extracted from HSPICE results. However, commercial applications deployed as autonomous sensors preclude human interaction, so the circuit must be able to perform its own clock optimization. In theory, it should be possible to have the system run through a set of clock frequencies and duty ratios every so often to recalibrate for optimized energy flyback.

On a similar note, the fabricated variable capacitor in this thesis has a known out-of-plane resonance value which the clock can be tuned to. In a complete system-on-chip (SOC) solution where there might be adaptation circuitry that guides the
system to harvest energy in the frequency spectrum containing the most vibration energy, the clock frequency can continuously vary. Therefore, a sensor that detects the current frequency of capacitor plate vibration should be built to dynamically adjust the clocking. This sensor might consist of a simple voltage or current waveform frequency detector attached to the output ports of the variable capacitor. It goes without say that the ideal sensor must consume very little additional power.

In order to improve the efficiency of energy harvesting, further optimization of the circuit parameters can be performed. For this thesis, HSPICE optimization involved sweeping one or two parameters through a certain range while keeping all other parameters fixed. No attempts have been made to extensively search the entire design space for ideal values since there is a severe limit on simulation speed due to the “stiffness” of the circuit. It is envisioned that in order for further optimization to occur, equations relating the parameters to the conversion efficiency must be derived explicitly; simulation can then fine tune the obtained solution.

The efficiency of this macro system cannot be improved greatly due to parasitic resistance, capacitance, and inductance present in the breadboard and PCB wires. To improve power density and decrease parasitic losses, the energy harvesting circuit needs to be built directly into an IC. This involves designing a MEMS variable capacitor, possibly using a comb drive, that can match the spring steel capacitor in terms of its capacitance variation. Certainly, this task is nontrivial. The remaining parts of the circuit must be designed such that the process flow allows for both MEMS and traditional semiconductor devices to reside on the same chip in order to leave out long bond wires, which present significant inductances. The components will also need to withstand the high voltage that appears due to the $C_{\text{MAX}}/C_{\text{MIN}}$ ratio boost as the circuit goes through the Q-V plane trace. Finally, since the microfabrication of a high Q inductor with large inductance is extremely challenging, innovative flyback topologies must be researched.
5.4 Interfacing with the Load

To successfully interface the energy harvesting circuit with a real-life load such as a low power sensor, many considerations must be taken into account. Most importantly, it is not unreasonable to expect that the magnitude of vibration will vary as a function of time, meaning that the amount of available power from the variable capacitor can change significantly. If the load continues to draw power for extended amounts of time and completely depletes $C_{\text{RES}}$, the energy harvesting circuit will fail. Therefore, a successful interface will provide a shutdown signal from the energy harvesting circuit to the load that will command a temporary stoppage in power consumption. The shutdown signal can be derived from $v_{\text{RES}}$; when it falls below a certain safety limit $v_{\text{TH}}$, the digital signal changes from 0 to 1.

The load should understand that power delivery cannot be guaranteed at all times and be able to perform sensibly when the power rail level changes. A sensor detecting radiation level in air, for example, should degrade gracefully in terms of its signal-to-noise ratio as $v_{\text{RES}}$ droops; sensor precision is directly proportional to expended power. As another example, a RF transmitter can decrease its output signal power when the reservoir reaches some critical level.

The type of load present to the energy harvesting circuit also matters. In this thesis, a purely resistive load with no reverse signal injection was considered. However, in the world of power electronics, many loads appear capacitive or inductive. These loads could in theory negatively affect the performance of the energy harvesting circuit, since it is optimized without these additional parasitics at the reservoir node. Furthermore, reverse injection can cause the two diodes $D_1$ and $D_2$ to accidentally turn on at inappropriate times, resulting in a $Q$-$V$ cycle that does not follow the charge-constrained trace accurately. For example, if the load is highly capacitive with a large capacitance value, a sudden voltage spike on the load will momentarily forward bias $D_1$. 
5.5 Final Words

The subject of energy harvesting presents itself as an uniquely challenging field of research. While recent trends in digital computational systems have been to steadily increase power consumption in order to achieve speed and accuracy, energy harvesting provides a mean of steadily providing $\mu$W's of power to autonomous systems where speed might not be of utmost importance; rather, the main goal is to keep the system sustained indefinitely without human interaction. Perhaps in the near future, a car passing by residential apartments will generate enough vibrational power to have sensors execute a complete cycle of air contaminant analysis and make sure no harmful biological agents are present.
Appendix A

HSPICE Simulation Code

A.1 Complete Simulation Deck

The complete set of HSPICE code used to generate simulation data for the energy harvesting circuit is shown below. The first few \textit{vmeas} statements create ammeters in appropriate branches for current monitoring. A few lines lower, \textit{varcap} defines a subcircuit that models the behavior of a variable capacitor, as explained in Chapter 3.

Most of the parameter definitions toward the end of the file are self-explanatory, but a few deserves mention. The initial starting voltage of the circuit, as defined by the battery used to precharge the capacitors, is set by \textit{vinit}. If the starting peak of variable capacitor, currently a sine wave, needs to be shifted, one can adjust the \textit{delay} parameter. Also, the total parasitic resistance due to the scope probe and any series resistor (in this thesis, a series resistor of 10 M\textOmega was used) should be entered in \textit{rp}. Finally, \textit{n} denotes the number of cycles to wait before the flyback transistor activates.

The HSPICE deck also refers to two device model files; those can be found in Appendix (A.2). Both of them were downloaded from the Internet.
Energy Harvesting Circuit (diode based)

*** Netlist ***

vmeas1 res resp 0
vmeas2 mid midp 0
vmeas3 res1 res 0
vmeas4 fbd fb 0
vcntrl gate fb pulse(0.3 4.2 0m 15n 15n 4u 'n/freq')

x1 resp mid dn6263
x2 midp out dn6263
xvar mid 0 varcap
cres res 0 1uF
cs out 0 3.3mF
rload res 0 'rload'

xpass out gate fb n7002
x3 0 fbd dn6263
rldc fb pl 8
rlp pl resl 360k
lfb pl resl 2.5mH

.subckt varcap v+ v-
cvar v+ vx 'cdc'
evar v- vx poly(2) var 0 v+ v- 0 0 0 0 'ca/cdc'
vvar var 0 sin(0 1 'freq' 'delay')
rvar var 0 1g
.ends varcap

.ic v(res)='vinit' v(mid)='vinit' v(out)='vinit'
.param cdc=650pF
.param ca=317.36pF
.param freq=1.5kHz
.param delay=-135u
.param vinit=6
.param rload=20meg
.param n=4
.include 'lib/diode.lib'
.include 'lib/n7002.lib'

*** Analysis ***
.tran 0.1m 30m
.options post=2 brief accurate

.end
A.2 Device Models

The two device models, one for the Schottky barrier diode and one for the MOSFET, are reproduced below. To successfully use these model files in conjunction with the main HSPICE code, save them into individual files, one called *diode.lib* and the other called *n7002.lib*. Be sure they reside in the correct directory structure referenced to the main code; if they need to be saved alongside the main code, remember to make the appropriate modifications to the *include* statements.

```
.subckt dn6263 1 2
  d1 1 2 sd
  d2 1 2 pnd

.model sd d ( N = 1.68359 Is = 1.50122E-007
  + Rs = 31.3769 Eg = 0.69 Xti = 2
  + Cjo = 2E-012 Vj = 0.393705 M = 0.196045
  + Fc = 0.5 Tt = 1.443E-009 Bv = 70
  + Ibv = 0.001 Kf = 0 Af = 1 )

.model pnd d ( Is = 1.165E-014 Rs = 1.06783
  + Eg = 1.11 Xti = 3 )

.ends

.subckt n7002 4 1 2
  m1 3 1 2 2 nmos w=18981u l=0.50u
  m2 2 1 2 4 pmos w=18981u l=0.70u
  r1 4 3 rtemp 1000E-3
  cgs 1 2 23E-12
dbd 2 4 dbd

.model nmos nmos ( Level = 3 Tox = 5E-8
  + Rs = 220E-3 Rd = 0 Nsub = 3.3E17
  + Kp = 6.5E-5 Uo = 650
  + Vmax = 0 Xj = 5E-7 Kappa = 2E-1
  + Eta = 1E-4 Tpg = 1
  + Is = 0 Ld = 0
  + Cgso = 0 Cgdo = 0 Cgbo = 0
  + Tlev = 1 Eex = -1.5 Tcv = 2.3E-3
```

130
Nfs = 0.8E12
Delta = 0.1

.model pmos pmos (Level = 3 Tox = 5E-8
+ Nsub = 1.5E16 Tpg = -1)

.model dbd d (Cjo = 26E-12 Vj = 0.38
+ M = 0.38 Rs = 0.1 Fc = 0.5
+ Is = 1E-12 Tt = 5E-8 N = 1
+ Bv = 26)

.model rtemp r (Tc1 = 5E-3 Tc2 = 5.5E-6)

.ends
Bibliography


