Fusing Strategies for the Dual-Voltage Fault
by
Rupam Shrivastava

Submitted to the Department of Electrical Engineering and Computer Science
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Master of Science
at the

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Abstract

This thesis focuses on the 42V - 14V fault in a dual voltage system and discusses the possibility of effective fusing. A simple model for the system had been created from technical documentation. Based on the model and the goal of achieving a stable state through fusing, constraints are set on the load fuse currents and circuit parameters. Further, modifications to the circuit have been theorized and evaluated for their ability to bring the circuit to the stable state. The thesis concludes with an effective fusing strategy based on actively detecting the fault and taking corrective actions.

Thesis Supervisor: Dr. Thomas Keim
Title: Principal Research Engineer
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I would also like to thank Prof. David J. Perreault for his short but very insightful guidance to my project. His way of attacking assumptions has taught me to not just look for general trends but to bear in mind the importance of exceptions. I would also like to thank all the people associated with the Consortium including Gary Desgrosseliers, Karin Strasswimmer, Kiyomi Boyd and Vivian Mizuno for all the help they did to make my stay at LEES comfortable and enjoyable.

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List Of Symbols

$I_{Fk}$ : Fuse current rating for the fuse in the k'th circuit

$I_{Lk}$ : Load current for the k'th circuit

$G_k$ : Load Conductance for the k'th circuit

$F_1$ : Generic symbol for 42V fuse

$F_2$ : Generic symbol for 14V fuse

$R_1$ : Resistance of the 42V load

$R_2$ : Resistance of the 14V load

$G_1$ : Conductance of the 42V load

$G_2$ : Conductance of the 14V load

$G_L$ : Combined parallel conductance of the shorted 42V and 14V load

$G_{1\text{max}}$ : Maximum possible conductance of the 42V load

$G_{2\text{max}}$ : Maximum possible conductance of the 14V load

$G_{L\text{max}}$ : Maximum value of $G_L$

$V_1$ : Thevenin equivalent source of value 42V for the 42V bus

$V_2$ : Thevenin equivalent source of value 14V for the 14V bus

$r_1$ : Thevenin equivalent resistance for the 42V bus

$r_2$ : Thevenin equivalent resistance for the 14V bus

$I_{F1}$ : Fusing current of Fuse $F_1$

$I_{F2}$ : Fusing current of Fuse $F_2$

$g_1$ : $1/r_1$

$g_2$ : $1/r_2$

$G_1$ : $1/R_1$
List Of Symbols

\( G_2 : 1/R_2 \)

\( i_1 \) : Current in fuse \( F_1 \) at the time of fault

\( i_2 \) : Current in fuse \( F_2 \) at the time of fault

\( i_{12} \) : Current in fuse \( F_1 \) after fuse \( F_2 \) blows (if fuse \( F_2 \) blows)

\( i_{21} \) : Current in fuse \( F_2 \) after fuse \( F_1 \) blows (if fuse \( F_1 \) blows)

\( I_{P1}^F \) : Maximum load current in the 42V load \((R_1)\)

\( I_{P2}^F \) : Maximum load current in the 14V load \((R_2)\)

\( G_{La}, G_{Lb}, G_{Lc}, G_{Ld}, G_{Le} \) : Symbols to locate specific points on the \( G_L \) space

\( i_{2}^' \) : Current in fuse \( F_2 \) at the time of fault with the Zener modification

\( V_Z \) : Zener breakdown voltage

\( \Delta V_Z \) : Range of the Zener breakdown voltages for the Zener modification to work

\( g_z \) : Zener conductance in the breakdown region

\( a \) : Symbol to define relationship between \( V_Z \) and \( V_1 \)

\( V_a, V_b, V_p, V_q \) : Symbols to define certain voltages in the operation of the Zener modification and diode modification circuits

\( G_{Pcond} \) : PTC device (and any resistance in series with it) conductance

\( L_1 \) : Generic 42V load

\( L_2 \) : Generic 14V load

\( G_{42}, G_1 \) : Another symbol for the conductance of the 42V load

\( G_{14}, G_2 \) : Another symbol for the conductance of the 14V load

\( I_{42}, I_1 \) : Current rating of the 42V constant current load

\( I_{14}, I_2 \) : Current rating of the 14V constant current load

\( P_{42}, P_1 \) : Power rating of the 42V constant power load

\( P_{14}, P_2 \) : Power rating of the 14V constant power load

\( I_{MAX} \) : Maximum current in the 14V circuit

\( G_{1max} \) : Maximum value of \( G_1 \)

\( G_{2max} \) : Maximum value of \( G_2 \)
List Of Symbols

$I_{1\text{max}}$: Maximum value of $I_1$
$I_{2\text{max}}$: Maximum value of $I_2$
$P_{1\text{max}}$: Maximum value of $P_1$
$P_{2\text{max}}$: Maximum value of $P_2$

$V_x$: Generic voltage bus (can be 42V or 14V)

$g_x$: Equivalent conductance of the generic voltage bus (can be $g_{42}$ or $g_{14}$)

$G_x$: Conductance of the load attached to the generic voltage bus (can be $G_{42}$ or $G_{14}$)

$I_x$: Current rating of the load attached to the generic voltage bus (can be $I_{42}$ or $I_{14}$)

$P_x$: Power rating of the load attached to the generic voltage bus (can be $P_{42}$ or $P_{14}$)

$v_{g_x}$: Voltage drop across $g_x$

$V_{1\text{max}}$: Maximum value of the 42V voltage bus

$V_{2\text{max}}$: Maximum value of the 14V voltage bus

$V_{1\text{nom}}$: Nominal value of the 42V voltage bus

$V_{2\text{nom}}$: Nominal value of the 14V voltage bus

$V_{1\text{min}}$: Minimum value of the 42V voltage bus

$V_{2\text{min}}$: Minimum value of the 14V voltage bus

$j_{\text{res}}$: Constant resistance load ratio parameter for bus voltage at its minimum value

$j_{\text{cur}}$: Constant current load ratio parameter for bus voltage at its minimum value

$j_{\text{pow}}$: Constant power load ratio parameter for bus voltage at its minimum value

$k_{\text{res}}$: Constant resistance load ratio parameter for bus voltage at its nominal value

$k_{\text{cur}}$: Constant current load ratio parameter for bus voltage at its nominal value

$k_{\text{pow}}$: Constant power load ratio parameter for bus voltage at its nominal value

$l_{\text{res}}$: Constant resistance load ratio parameter for bus voltage at its maximum value

$l_{\text{cur}}$: Constant current load ratio parameter for bus voltage at its maximum value

$l_{\text{pow}}$: Constant power load ratio parameter for bus voltage at its maximum value

$I_{L1}$: Current in load $L_1$
\[ I_{L2} : \text{Current in load} \ L_2 \]
\[ I_L : I_{L1} + I_{L2} \]
\[ V : \text{Common voltage at the shorted loads} \]
\[ f(V) : \text{Function to relate} \ I_L \ \text{to} \ V \]
\[ F1 : \text{Ratio between maximum load current and fuse rating for the 42V fuse} \]
\[ F2 : \text{Ratio between maximum load current and fuse rating for the 14V fuse} \]
Chapter 1

Introduction To The Circuit And The Associated Problem

1.1 Introduction

Dual-voltage (e.g. 42V/14V) automobiles present the electrical system designer with challenges not found in today’s cars. One such challenge is the design of a fault protection system to restore the electrical system to a safe state in the event of short circuits and/or faulted components. In conventional cars, simple fuses are the principal elements of the fault protection system. But in dual-voltage automobiles, a new class of fault (the bus-to-bus or 42V – 14V fault) can occur. It can be shown (and is shown here), that fuses alone cannot be used to protect against such an event. This thesis will show some methods which can be considered to achieve a dual voltage system which always returns to a safe condition after a bus-to-bus fault.

1.1.1 Current Fusing Circuits

Figure 1.1 presents a schematic representation of a typical 14V electrical system, showing fuses and loads represented by resistors. From [1], the largest fuse rating in the 1997 Ford Taurus was 40A. We will presume that this is typical for automobiles in general. Thus,

\[ \text{max} I_{F_k} = 40A \quad k = 1,2,...n \]  

(1.1)

Here \( I_{F_k} \) designated the fuse current rating for the fuse in the \( k \)’th circuit. The fusing current for a circuit is by design more than the normal loading current in the circuit. Thus, if the load is modelled as a resistor then the fusing current sets a limit on how small the resistance of the load can be, or in other words, how large the conductance of the load can be. Putting the same in equation form, we get,

\[ V_{G_k} = I_{L_k} < I_{F_k} \]  

(1.2)
Introduction To The Circuit And The Associated Problem

where,
\[ V = \text{bus voltage}, \]
\[ G_k = \frac{1}{R_k} = \text{Load Conductance for circuit } k, \]
\[ I_{Lk} = \text{Load current for circuit } k \]

If we substitute the maximum value of \( I_{Fk} \) then,
\[ G_k < \max(I_{Fk})/V = G_{2\text{max}} \quad (1.3) \]

where, \( G_{2\text{max}} = \text{maximum value for any 14V load conductance (the subscript 2 has been used to differentiate from } G_{1\text{max}} = \text{maximum value for any 42V load conductance). We will shortly introduce a second bus and will commonly use the subscript 2 to indicate the 14V system and the subscript 1 to represent the 42V system.} \]
\[ G_{2\text{max}} = 40A/14V \approx 3\text{mhos} \quad (1.4) \]

Thus, we have an upper bound on the value of the conductance that any load in any 14V circuit can have. Since, similar data for the 42V circuit does not exist at present, we assume that
\[ G_{1\text{max}} = K\text{mhos}. \quad (1.5) \]

Figure 1.1: Current Fusing Circuits
If the 42V circuit is designed to cater to loads whose power demand is about 3 times that of 14V loads, then we can estimate K:

\[
P_{42V} = 3P_{14V}
\]

(1.6)

\[
42^2 K = 3 \times 14^2 \times 3
\]

(1.7)

Hence,

\[
K = 1
\]

(1.8)

We can also choose other values for K depending on the conditions.

1.1.2 Fault Considered

In a dual-voltage car, the second distribution system can be expected to look schematically just like Figure 1.1. Our concern in this paper is for faults between any branch of the 14V system and any branch of the 42V system. Figure 1.2 shows the fault considered for analysis. The explanations for the various current values and resistances are as follows:

- \( R_1 \) = Resistance of the 42V load
- \( R_2 \) = Resistance of the 14V load
- \( I_{F1} \) = Fusing current of Fuse \( F_1 \)
- \( I_{F2} \) = Fusing current of Fuse \( F_2 \)

Although Figure 1.2 is very simple, it can be used to represent any possible 42V – 14V

![Diagram](image)

Figure 1.2: Fault Circuit Considered
fault. Faults between different circuits will result in different values of the parameters $I_{F1}$, $I_{F2}$, $R_1$ and $R_2$. Note that even for a fixed pair of circuits, it is possible for $R_1$ and $R_2$ to assume different values at different times. In particular, it is quite common for electrical loads to be turned off in which case the corresponding load resistance is essentially infinite.

1.1.3 Safe Clearance Of The Fault

In the event of the fault, we define the safe clearance of the fault as any sequence of fuse blowing which will eventually result in a safe operating condition. With 2 fuses in place, we can have a total of 5 choices for fuse blowing events, i.e.

1. Neither of the fuses blowing
2. Fuse $F_1$ blowing only
3. Fuse $F_2$ blowing only
4. Fuse $F_1$ blowing, then Fuse $F_2$ blowing
5. Fuse $F_2$ blowing, then Fuse $F_1$ blowing

The start and the end results of all these combinations of fuse blowing are shown in Figure 1.3. Condition (1) is clearly an unacceptable outcome. The voltage applied to loads $R_1$ and $R_2$ will be between the voltage of the buses; the exact value will be strongly influenced by the resistance values.
by the magnitude of the effective series resistances of the two sources. (The simple diagram of Figure 1.3 does not explicitly indicate the source resistances.) In general, in state 1, there is a large current flowing in the fault and a high (possibly harmful) voltage on load $R_2$.

Condition (3) has the same detrimental features (current in the fault and high voltage on $R_2$) as Condition (1).

Some have argued that condition (2) is a safe outcome. The voltage across $R_1$ is lower than its intended value. Load $R_1$ may not function properly or at all with such a small voltage, but the low voltage is not likely to damage load $R_1$. But current still flows in the fault. If we could be confident that the real world fault would behave as its model (a zero impedance short circuit), this line of reasoning might be worth considering. But the real world fault may have a small non-zero resistance. If the fault were to have a resistance which would support just a couple of volts at a few amps, the resulting heating, occurring in a very small volume, could cause excessive temperature. So, for the purposes of this study, we will consider only conditions (4) and (5) to be safe processes. Our methodology will enable us to design the fuse currents $I_{F1}$ and $I_{F2}$ and other circuit parameters such that the fault is safely cleared by one of these fusing events.

1.2 Equivalent Circuit At Fault

In this section, we describe an equivalent circuit for the system considered. Figure 1.4 shows the circuit. The equivalent circuit has the following features:

- **Voltage bus**: We have introduced an equivalent Thevenin circuit for the buses. Thus, we have replaced the 42V and the 14V bus by a voltage source of voltage 42V and 14V and a series resistance $r_1$ and $r_2$ respectively.
- **Loads**: The loads have been modelled as resistors of value $R_1$ and $R_2$.
- **Fault**: The fault has been shown as a short circuit of zero resistance between the positive ends of the 42V and 14V loads.

Check Table 1.1 for clearer definitions. Since, the circuit topology makes it simpler to work with conductances rather than resistances, we will replace resistances with conductances defined accordingly. See Table 1.2. The value $G_L$ is of importance. It represents the conductance of the parallel combination of $R_1$ and $R_2$. And with the help of Eq. (1.5) and Eq. (1.4), we get a maximum $G_L$ of

$$G_{L_{\text{max}}} = 3 + K$$

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**Introduction To The Circuit And The Associated Problem**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_1$</td>
<td>Thevenin equivalent source of value 42V for the 42V bus</td>
</tr>
<tr>
<td>$V_2$</td>
<td>Thevenin equivalent source of value 14V for the 14V bus</td>
</tr>
<tr>
<td>$r_1$</td>
<td>Thevenin equivalent resistance for the 42V bus</td>
</tr>
<tr>
<td>$r_2$</td>
<td>Thevenin equivalent resistance for the 14V bus</td>
</tr>
<tr>
<td>$R_1$</td>
<td>42V Load Resistance</td>
</tr>
<tr>
<td>$R_2$</td>
<td>14V Load Resistance</td>
</tr>
<tr>
<td>$I_{F1}$</td>
<td>Fuse current rating for the 42V load</td>
</tr>
<tr>
<td>$I_{F2}$</td>
<td>Fuse current rating for the 14V load</td>
</tr>
</tbody>
</table>

Table 1.1: Parameter Definition For The Equivalent Circuit

<table>
<thead>
<tr>
<th>Conductance</th>
<th>Relation to resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_1$</td>
<td>$1/r_1$</td>
</tr>
<tr>
<td>$g_2$</td>
<td>$1/r_2$</td>
</tr>
<tr>
<td>$G_1$</td>
<td>$1/R_1$</td>
</tr>
<tr>
<td>$G_2$</td>
<td>$1/R_2$</td>
</tr>
<tr>
<td>$G_L$</td>
<td>$1/R_1 + 1/R_2$</td>
</tr>
</tbody>
</table>

Table 1.2: Conductance Definitions For The Equivalent Circuit

---
Table 1.3: Current Definitions For The Faulted Circuit

<table>
<thead>
<tr>
<th>Current</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i_1)</td>
<td>Current in fuse (F_1) at the time of fault</td>
</tr>
<tr>
<td>(i_2)</td>
<td>Current in fuse (F_2) at the time of fault</td>
</tr>
<tr>
<td>(i_{12})</td>
<td>Current in fuse (F_1) after fuse (F_2) blows (if fuse (F_2) blows)</td>
</tr>
<tr>
<td>(i_{21})</td>
<td>Current in fuse (F_2) after fuse (F_1) blows (if fuse (F_1) blows)</td>
</tr>
<tr>
<td>(I_{F_1}^p)</td>
<td>Maximum load current in the 42V load ((R_1))</td>
</tr>
<tr>
<td>(I_{F_2}^p)</td>
<td>Maximum load current in the 14V load ((R_2))</td>
</tr>
</tbody>
</table>

Table 1.3 provides word definitions for the various currents in the circuit. Please refer to Figure 1.5 for the schematic definitions and sign conventions.

1.2.1 Current Expressions

Solving for the currents gives the following expressions:

\[
I_{F_1}^p = \frac{V_1}{(1/g_1 + 1/G_{1\text{max}})} \quad (1.10)
\]

\[
I_{F_2}^p = \frac{V_2}{(1/g_2 + 1/G_{2\text{max}})} \quad (1.11)
\]

\[
i_1 = \frac{g_1 [V_1 (G_L + g_2) - V_2 g_2]}{g_1 + g_2 + G_L} \quad (1.12)
\]

\[
i_2 = -\frac{g_2 [V_2 (G_L + g_1) - V_1 g_1]}{g_1 + g_2 + G_L} \quad (1.13)
\]
Introduction To The Circuit And The Associated Problem

(a) Normal Operating Conditions

(b) At The Time Of The Fault

(c) After Fuse 2 Blows

(d) After Fuse 1 Blows

Figure 1.5: Current Definitions
Introduction To The Circuit And The Associated Problem

\[ i_{21} = \frac{V_2 G_L g_2}{g_2 + G_L} \]  
\[ i_{12} = \frac{V_1 G_L g_1}{g_1 + G_L} \]  

1.3 Fusing Strategies And Conditions

In this section, we will summarize the fusing strategies and the conditions needed for them to be realized.

1.3.1 Fusing Strategy 1: Fuse $F_1$ Blowing Followed By Fuse $F_2$

The conditions for fuse $F_1$ and Fuse $F_2$ blowing in succession are as follows:

1. $i_1 > I_{F1}$: This condition says that the fault current in fuse $F_1$ is more than its fusing current so that Fuse $F_1$ blows.

2. $i_2 < I_{F2}$: This condition says that the fault current in fuse $F_2$ is less than its fusing current so that $F_2$ does not blow.

3. $i_{21} > I_{F2}$: This condition says that the fault current in fuse $F_2$ after Fuse $F_1$ has blown is more than its fusing current so that $F_2$ does blow.

4. $I_{F1} > I^*_{F1}$: This condition says that the fusing current of Fuse $F_1$ is more than its maximum loading current, so that Fuse $F_1$ does not blow in the normal operating conditions.

5. $I_{F2} > I^*_{F2}$: This condition says that the fusing current of Fuse $F_2$ is more than its maximum loading current, so that Fuse $F_2$ does not blow in the normal operating conditions.

Note that condition (2) is not formally necessary for the $F_1$ then $F_2$ scenario to unfold. But if $i_2 > I_{F2}$, the amount of inequality will need to be small. If $i_2 > I_{F2}$, the only way to blow $F_1$ followed by $F_2$ is if Fuse $F_1$ is more overloaded with respect to its rating, so that it blows first.
1.3.1.1 Choice Of $I_{F1}$ And $I_{F2}$

The first and fourth of conditions in section 1.3.1 can be satisfied by choosing $I_{F1}$ such that

$$i_1 > I_{F1} > I_{F1}^p$$  

(1.16)

For the conditions (2), (3) and (5) stated above to be satisfied, we can choose the fusing current $I_{F2}$ such that

$$i_{21} > I_{F2} > i_2, I_{F2}^p$$  

(1.17)

Here we have used the convention that $x > y, z$ is equivalent to $x > y, x > z$. Thus, the three conditions

$$i_1 > I_{F1}^p$$  

(1.18)

$$i_{21} > i_2, I_{F2}^p$$  

(1.19)

can ensure us the possibility to select $I_{F1}$ and $I_{F2}$ to implement Fusing strategy 1, with respect to the two circuits under consideration.

1.3.2 Fusing Strategy 2: Fuse $F_2$ Blowing Followed By Fuse $F_1$

The conditions for fuse $F_2$ and Fuse $F_1$ blowing in succession are as follows

1. $i_1 < I_{F1}$: This condition says that the fault current in fuse $F_1$ is less than its fusing current so that Fuse $F_1$ does not blow.

2. $i_2 > I_{F2}$: This condition says that the fault current in fuse $F_2$ is more than its fusing current so that $F_2$ blows.

3. $i_{12} > I_{F1}$: This condition says that the fault current in fuse $F_1$ after Fuse $F_2$ has blown off is more than its fusing current so that $F_1$ does blow.

4. $I_{F1} > I_{F1}^p$ : This condition says that the fusing current of Fuse $F_1$ is more than its maximum loading current, so that Fuse $F_1$ does not blow in the normal operating conditions.

5. $I_{F2} > I_{F2}^p$ : This condition says that the fusing current of Fuse $F_2$ is more than its maximum loading current, so that Fuse $F_2$ does not blow in the normal operating conditions.

Here it is Condition (1) which is sufficient but not necessary for the $F_2$ then $F_1$ scenario.
1.3.2.1 Choice Of $I_{F1}$ And $I_{F2}$

The first and the fourth conditions stated in section 1.3.2 can be satisfied by choosing $I_{F2}$ such that

$$i_2 > I_{F2} > I_{F2}'$$

(1.20)

For the conditions (2), (3) and (5) stated above to be satisfied, we can choose the fusing current $I_{F1}$ such that

$$i_{12} > I_{F1} > i_1, I_{F1}'$$

(1.21)

Thus, the three conditions

$$i_2 > I_{F2}$$

(1.22)

$$i_{12} > i_1, I_{F1}$$

(1.23)

can ensure us the possibility to select $I_{F1}$ and $I_{F2}$ to implement Fusing strategy 2, with respect to the two circuits under consideration.

1.3.3 Basic Plot Used

As was shown in the section 1.2.1, the currents $i_1, i_2, i_{12}, i_{21}$ are functions of $G_L$ rather than $G_1$ or $G_2$, we will plot these currents versus $G_L$ to get a clearer perspective of the safe operating conditions. To be noted is the fact that we need not consider the plots beyond $G_{Lmax}$ (as defined in Eq (1.9)) because any conductance cannot go beyond this value. Figure 1.6 shows the basic working area that we will be using to define the safe clearance conditions. This plot shows $G_L$ plotted on the $x -$ axis from 0 to $G_{Lmax}$. The $y -$ axis will have the plots of the fault currents and the maximum load currents separately for Fuse F1 and Fuse F2.

![Figure 1.6: Basic Plot Used](image)
1.4 Fusing Strategy 1: Fuse $F_1$ Blowing Followed By Fuse $F_2$

1.4.1 Ensuring Fuse $F_1$ Blows For All $G_L$

Plotted below in Figure 1.7 are the currents $i_1$ and $I_{F_1}$ for different values of $g_1$ and $g_2$. Observe first Figure 1.7 (a). In the portion $G_L > G_{La}$, we find that $i_1 > I_{F_1}$ and thus condition in Eq. (1.18) is satisfied. Thus in circuits where the smallest possible $G_L$ is large enough (which can occur if some loads are permanently energized) we can pick a value of $I_{F_1}$ so that Eq. (1.18) is satisfied. In Figure 1.7 (b) and (c), which represent progressively larger values of $g_1$ and $g_2$ relative to Figure 1.7 (a), the range of allowable $G_L$ grows. For large enough $g_1$ and $g_2$, it is possible that

$$i_1|_{G_L=0} > I_{F_1}$$

(1.24)

In that case, it is possible to pick a fuse rating $I_{F_1}$ which satisfies Eq. (1.18) for all possible $G_L$. The condition necessary for this to be true is

$$\frac{g_2g_1(V_1 - V_2)}{g_1 + g_2} > \frac{G_{1max}g_1V_1}{G_{1max} + g_1}$$

(1.25)

which, for $V_1/V_2 = 3$, translates into

$$g_2 > \frac{3g_1G_{1max}}{2g_1 - G_{1max}}$$

(1.26)

which turns out to be a relatively unrestrictive condition since $g_2$ is an order of magnitude higher than $G_{1max}$.

1.4.2 Ensuring Fuse $F_2$ Blows After Fuse $F_1$ For All $G_L$

Plotted below in Figure 1.8 are the currents $i_2$, $i_{21}$ and $I_{F_2}$ for some values of $g_1$ and $g_2$. Since $i_2$ is a monotonically decreasing function of $G_L$ and $i_{21}$ is a monotonically increasing function of $G_L$, for the first of inequalities (Eq. (1.18)) to be true for even a range of $G_L$, we need

$$i_{21}(G_L = G_{Lmax}) > i_2(G_L = G_{Lmax})$$

(1.27)

thus,

$$\frac{V_2G_{Lmax}g_2}{g_2 + G_{Lmax}} > \frac{-g_2[V_2(G_{Lmax} + g_1) - V_1g_1]}{g_1 + g_2 + G_{Lmax}}$$

(1.28)
Figure 1.7: Plots Of Currents Through Fuse $F_1$ For Different Values Of $g_1$ And $g_2$

This, translates into (using $V_1/V_2 = 3$)

$$g_2 < \frac{G_{L_{\text{max}}}(2G_{L_{\text{max}}}-g_1)}{2(g_1-G_{L_{\text{max}}})}$$

(1.29)

$g_1$ is expected to be an order of magnitude higher than $G_1$ (since it is the series equivalent resistance and we do not want a high voltage drop across it). Thus $(2G_{L_{\text{max}}}-g_1)$ in the numerator of the R.H.S. of Eq. (1.29) is a very small number, probably negative. Thus, this condition states that $g_2$ must be less than a small number which may be negative. Thus, for all practical cases, this condition is not obeyed. We may conclude that we cannot ensure blowing of Fuse $F_2$ after Fuse $F_1$ for many loading conditions.

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1.4.3 Summary Of Fusing Strategy 1

As has been proved, we can ensure blowing of Fuse $F_1$ for many conditions but we cannot ensure blowing of Fuse $F_2$ after Fuse $F_1$ has blown. Thus, we cannot strictly implement this fusing strategy.

1.5 Fusing Strategy 2: Fuse $F_2$ Blowing Followed By Fuse $F_1$

1.5.1 Ensuring Fuse $F_2$ Blows For All $G_L$

Plotted below in Figure 1.9 are the currents $i_2$ and $I_{F_2}$ for different values of $g_1$ and $g_2$. $i_2$, being a function of $g_1$ and $g_2$ shifts as shown. Observe Figure 1.9 (a). In the portion $G_L < G_{ld}$, we find that $i_2 > I_{F_2}$ and thus the condition in Eq. (1.22) is satisfied. Thus, in this shaded region we can choose $I_{F2}$ such that $I_{F2} < I_{F2} < i_2$. In (b) and (c), this condition is fulfilled for all values of $G_L$. The ability to draw a horizontal line in the shaded region from $G_L = 0$ to $G_{L_{max}}$ implies exactly this. And it is also clear that Figure (b) represents the boundary between (a) and (c). Thus, (b) can be used to define conditions on $g_1$ and $g_2$ so that the condition in Eq. (1.22) is satisfied for all $G_L$ values. The condition shown in Figure (b) translates into current $i_2$ passing through point $A$ (see Figure 1.9 (b)) or $(G_{L_{max}}, \frac{V_2}{g_2 + G_{2max}})$. Thus, substituting the values for the currents,

$$\frac{V_2}{g_2 + G_{2max}} < \frac{-g_2[V_2(G_{L_{max}} + g_1) - V_1 g_1]}{g_2 + g_1 + G_{L_{max}}} \quad (1.30)$$

This translates into (using $V_1/V_2 = 3$)

$$g_2 > \frac{-g_1 G_{2max} + 2 G_{2max} G_{L_{max}}}{2 g_1 - G_{L_{max}} - G_{2max}} \quad (1.31)$$

$$g_2 > \frac{-3g_1 + 6(3 + K)}{2g_1 - 6 - K} \quad (1.32)$$

The condition in Eq. (1.32) is very easily met. The right hand side is always less than zero for reasonable values of $g_1$, so the condition is met for any positive $g_2$. This unusual result is a consequence of $V_1/V_2$ being exactly 3. But in a range of practical cases, including cases where $V_1/V_2$ deviates from 3, the condition is still easily met for most plausible values of $g_1$, $G_{1_{max}}$ and $G_{2max}$.
1.5.2 Ensuring Fuse $F_1$ Blows After Fuse $F_2$ For All $G_L$

Plotted below in Figure 1.10 are the currents $i_1, i_{12}$ and $I_{F_1}$ for some values of $g_1$ and $g_2$. In the portion $G_L > G_{Le}$, we find that $i_{12} > I_{F_1}, i_1$ and thus condition in Eq. (1.23) is satisfied. The solution for $G_{Le}$ is given by

$$G_{Le} = 2g_1$$  \hspace{1cm} (1.33)

We want the point $G_{Le}$ to be less than $G_{L_{max}}$ so that we can have some loads for which the Fuse $F_1$ blows after Fuse $F_2$ blows. However, $g_1$ is expected to be an order of magnitude higher than $G_1$ and $G_{L_{max}}$. So $G_{Le} < G_{L_{max}}$ is not possible. Thus, for all practical cases, Fuse $F_1$ cannot be made to blow after Fuse $F_2$ has blown.
1.5.3 Summary Of Fusing Strategy 2

As has been proved, we can ensure blowing of Fuse $F_2$ but not blowing of Fuse $F_1$ after Fuse $F_2$ has blown. Thus, we cannot strictly implement this fusing strategy.

1.6 Conclusions

We have shown that the fusing strategies as envisaged theoretically cannot be implemented in practice. This result has been known for a long time by the automotive industry. With this chapter we have provided a mathematical footing and have shown that, without special measures, we cannot guarantee that both the fuses will blow in practical circumstances. In the next chapters, we will develop a strategy to get over this restriction and ensure both fuses blowing under all circuit operating conditions.
Chapter 2

Passive Circuit Modifications To The Dual Voltage System

2.1 Introduction

As we saw before, the circuit in its working state cannot guarantee us the blowing of both the fuses. Hence, we look for modifications to the circuit, which do not affect the normal functionality of the circuit, but will become active in the event of a 42V – 14V fault.

2.2 Bottleneck Conditions

As we saw before, the conditions \( i_{21} > i_2 \) and \( i_{12} > i_1 \) are not satisfied for any circuit topology. In this section, we will introduce another condition that is not satisfied in many cases. Consider Eq.(1.19) as rewritten here

\[
i_{21} > I_{p2} \tag{2.1}
\]

or,

\[
\frac{V_2 G_L g_2}{g_2 + G_L} > \frac{V_2 g_2 G_{2max}}{g_2 + G_{2max}} \tag{2.2}
\]

Consider a 14V load which can in its operation range from 0 to \( G_{2max} \). Now consider a 42V – 14V fault occurring when this load is switched off i.e. \( G_2 = 0 \). Thus, \( G_L = G_1 \) for the definition of \( i_{21} \) and \( G_2 = G_{2max} \) for the definition of \( I_{p2} \). Hence, this condition actually puts the condition (1.19) to the toughest test by minimizing \( i_{21} \). Substituting as discussed,

\[
\frac{V_2 G_1 g_2}{g_2 + G_1} > \frac{V_2 g_2 G_{2max}}{g_2 + G_{2max}} \tag{2.3}
\]

This leads to,

\[
G_1 > G_{2max} \tag{2.4}
\]
2.3 Modification 1: Addition Of Zener

We will introduce a Zener diode to the circuit in the position shown in Figure 2.1. In the next section, we describe how we want the circuit to work.

2.3.1 Desired Sequence Of Events With The Zener Modification

We want the following operation sequence to be followed with the Zener in place:

- In the normal operation of the 14V circuit, the Zener is back biased but not to the Zener breakdown voltage. Thus, the Zener acts as an open circuit and therefore doesn’t affect the circuit operation.
- In the event of a 42V – 14V fault, the Zener goes into reverse breakdown and provides a shorting path to the ground.
- Fuse F1 blows disconnecting the 42V circuit from the loads
- Zener goes into off state once again after Fuse F1 blows
2.3.2 Effectiveness Of The Zener Modification

We will prove the efficacy of the Zener circuit with respect to the condition \( i_{21} > i_2 \). Consider Figure 2.2. This figure compares the circuit with and without the Zener after the fault occurs. Observe voltage \( V_a \) and \( V_b \). With the Zener in place, voltage \( V_b \) tends to stay around the Zener breakdown voltage. (Let's call the Zener breakdown voltage \( V_{Z} \)). Now concentrate on currents \( i_2 \) and \( i'_2 \).

\[
i_2 = (V_a - V_2)g_2
\]
\[
i'_2 = (V_b - V_2)g_2 \approx (V_Z - V_2)g_2
\]

Figure 2.3 shows the comparison of the circuits with and without the Zener for the case when Fuse F1 has blown and compares them for the current \( i_{21} \). We find that since the Zener is off, the two circuits are the same and thus \( i'_{21} = i_{21} \).

It is noteworthy that the we have to this point only postulated that the circuit will work this way. We have yet to establish the conditions in which the circuit actually works in this manner. Note that, \( i'_2 \) (or \( i_2 \) in the Zener circuit) is a function of the Zener breakdown voltage \( (V_Z) \) and is thus manipulatable by choice of \( V_Z \). \( i_{21} \) on the other hand stays unaffected by the inclusion of the Zener. Thus, with a proper choice of the reverse breakdown voltage \( (V_Z) \), we can bring \( i_2 \) down so that it may be able to satisfy \( i_{21} > i_2 \).

2.3.3 Analyzing The Zener Circuit

Figure 2.4 shows the actual Zener model that we will use. We take the Zener as an open circuit when it is not conducting and as a voltage source with a series resistance when it is conducting. The voltage source being equal to the Zener breakdown voltage. We will also relate the Zener breakdown voltage to \( V_1 \) as

\[
V_Z = \alpha V_1
\]

Envisaging a strategy involving Fuse F1 blowing and then Fuse F2 blowing, we need the following conditions to be true for the operating sequence that we have in mind to occur.

1. \( V_Z > V_p \): With reference to Figure 2.5, this condition states that the Zener will not turn on (or break down) under normal operating conditions of the 14V circuit.
Passive Circuit Modifications To The Dual Voltage System

Figure 2.2: Comparison Of The Circuits With The Without The Zener At The Time Of The Fault

(a) 

(b)
Passive Circuit Modifications To The Dual Voltage System

Figure 2.3: Comparison Of The Circuits With The Without The Zener After Fuse F1 Blows
Passive Circuit Modifications To The Dual Voltage System

Figure 2.4: Zener Model

2. $V_Z < V_q$: With reference to Figure 2.6, this condition states that the Zener will turn on in the event of a fault. For the Zener to go into conduction, it is sufficient for the condition $V_Z < V_q$ to be met when the circuit is analyzed in the absence of the Zener. To indicate that, the Zener is shown in dotted lines.

3. $i_1 > I_{F1}$: With reference to Figure 2.7, this condition ensures that Fuse F1 will blow in the case of a fault.

4. $i_2 < I_{F2}$: With reference to Figure 2.7, this condition ensures that Fuse F2 will not blow in the case of a fault.

5. $i_{21} > I_{F2}$: With reference to Figure 2.8, this condition ensures that Fuse F2 will blow after Fuse F1 has blown.

6. $I_{F1} > I_{F1}^p$: This condition ensures that Fuse F1 will not blow under normal operating conditions of the 42V circuit.

7. $I_{F2} > I_{F2}^p$: This condition ensures that Fuse F2 will not blow under normal operating conditions of the 14V circuit.
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Figure 2.5: Figure For Condition 1

Zener off

Figure 2.6: Figure For Condition 2

Zener conducting

Figure 2.7: Figure For Condition 3 And 4
2.3.3.1 Condition 1

\[ V_Z > V_p \]  \hspace{1cm} (2.8)
\[ \alpha V_1 > \frac{V_2 g_2}{G_2 + g_2} \]  \hspace{1cm} (2.9)

or, if \( V_1 = 3V_2 \),
\[ \alpha > \frac{g_2}{3(G_2 + g_2)} \]  \hspace{1cm} (2.10)

In the bottleneck case, when the fault occurs when there is no load on the 14V circuit, \( G_2 = 0 \). Thus,
\[ \alpha > \frac{1}{3} \]  \hspace{1cm} (2.11)

2.3.3.2 Condition 2

\[ V_Z < V_q \]  \hspace{1cm} (2.12)
\[ \alpha V_1 > \frac{V_1 g_1 + V_2 g_2}{g_1 + g_2 + G_L} \]  \hspace{1cm} (2.13)

or, if \( V_1 = 3V_2 \),
\[ \alpha > \frac{3g_1 + g_2}{3(g_1 + g_2 + G_L)} \]  \hspace{1cm} (2.14)
2.3.3.3 Condition 3 And 6

Observe that if we can ensure $i_1 > I_{F1}$, then we can choose $I_{F1}$ such that $i_1 > I_{F1} > I_{F1}^p$ and satisfy both of the conditions 3 and 6. Thus,

$$\frac{g_1 [(V_1 (g_2 + g_Z + G_L) - V_2 g_Z - V_2 g_Z)]}{g_1 + g_2 + g_Z + G_L} < \frac{V_1 g_1 g_Z}{g_1 + G_1} \quad (2.15)$$

Using, $V_1 = 3V_2$,

$$g_Z [3(g_1 - \alpha (g_1 + G_1))] > G_1 g_2 - 2g_1 g_2 - 3G_2 g_1 \quad (2.16)$$

Let us postulate that the coefficient of $g_Z$ in Eq. (2.16) is a positive number. Then,

$$g_Z > \frac{G_1 g_2 - 2g_1 g_2 - 3G_2 g_1}{3(g_1 - \alpha (g_1 + G_1))} \quad (2.17)$$

This represents a condition on the on-state incremental conductance of the Zener, a condition which presumably can always be satisfied with a big enough device. The condition for the right hand side of Eq. (2.16) to be positive is

$$\alpha < \frac{g_1}{g_1 + G_1} \quad (2.18)$$

2.3.3.4 Condition 4, 5 And 7

Observe that if we can ensure $i_2 > i_2, I_{F2}$, then we can choose $I_{F2}$ such that $i_2 > I_{F2} > i_2, I_{F2}^p$ and satisfy all of the conditions 4, 5 and 7. Firstly, if we need $i_2$ to flow in the direction shown, then we need $V_b > V_2$ (Figure 2.2)

$$\frac{V_1 g_1 + V_2 g_Z + V_2 g_Z}{g_1 + g_2 + g_Z + G_L} > V_2 \quad (2.19)$$

Using $V_1 = 3V_2$,

$$g_Z [3\alpha - 1] > G_L - 2g_1 \quad (2.20)$$

Using Eq. (2.11)

$$\alpha > \frac{1}{3} \quad (2.21)$$

so we can divide both sides of Eq. 2.20 by $(3\alpha - 1)$ without changing the direction of the inequality and,

$$g_Z > \frac{G_L - 2g_1}{3\alpha - 1} \quad (2.22)$$
Passive Circuit Modifications To The Dual Voltage System

This is a trivial condition which says that $g_Z > a$ negative number (check the numerator and remember $g_1 > G_L$). Now, we consider the regular conditions,

$$i_{21} > i_2$$  \hspace{1cm} (2.23)

$$\frac{V_2 g_2 G_L}{g_2 + G_L} > \frac{-g_2[V_2(g_1 + g_Z + G_L) - V_1 g_1 - V_2 g_Z]}{g_1 + g_2 + g_Z + G_L}$$  \hspace{1cm} (2.24)

Using $V_1 = 3V_2$,

$$g_Z[G_L + (g_2 + G_L)(1 - 3\alpha)] > 2g_1 g_2 - 2G_L^2 + G_L g_1 - 2g_2 G_L$$  \hspace{1cm} (2.25)

Now, the right hand side of Eq. 2.25 is a positive number for $g_1 > 2G_L$ (take 2$g_2$ common from the first and fourth terms and $G_L$ common from the second and third terms), and so should be the L.H.S. Thus,

$$G_L + (g_2 + G_L)(1 - 3\alpha) > 0$$  \hspace{1cm} (2.26)

or,

$$\alpha < \frac{g_2 + 2G_L}{3(g_2 + G_L)}$$  \hspace{1cm} (2.27)

and,

$$g_Z > \frac{2g_1 g_2 - 2G_L^2 + G_L g_1 - 2g_2 G_L}{G_L + (g_2 + G_L)(1 - 3\alpha)}$$  \hspace{1cm} (2.28)

Now, we remain with the condition,

$$i_{21} > I_{P2}$$  \hspace{1cm} (2.29)

This results in the earlier bottleneck condition that we found out, namely Eq. (2.4) rewritten here

$$G_1 > G_{2\text{max}}$$  \hspace{1cm} (2.30)

### 2.3.3.5 Collecting The Results And Analysis

Collecting all the constraints on $\alpha$ together, we have,

$$\frac{g_2}{3(G_2 + g_2)}, \frac{1}{3} < \alpha < \frac{g_1}{g_1 + G_1}, \frac{3g_1 + g_2}{3(g_1 + g_2 + G_L)}, \frac{2G_L + g_2}{3(g_2 + G_L)}$$  \hspace{1cm} (2.31)

Collecting all the $g_Z$ conditions we have,

$$g_Z > \frac{G_1 g_2 - 2g_1 g_2 - 3G_2 g_1}{3(g_1 - \alpha(g_1 + G_1))}, \frac{2g_1 g_2 - 2G_L^2 + G_L g_1 - 2g_2 G_L}{G_L + (g_2 + G_L)(1 - 3\alpha)}$$  \hspace{1cm} (2.32)
We also have the bottleneck condition

$$G_1 > G_{2\text{max}}$$  \hfill (2.33)

Eq. (2.31, 2.32) and (2.33) summarize all the conditions needed for the strategy to work. Let us reduce the complexity. Consider first two expressions in the $\alpha < 1$ conditions. Let us postulate

$$\frac{3g_1 + g_2}{3(g_1 + g_2 + G_L)} < \frac{g_1}{g_1 + G_1}$$  \hfill (2.34)

This can be shown to be true if

$$g_2G_1 < 2g_1g_2 + g_1G_2$$  \hfill (2.35)

which is satisfied always if $2g_1 > G_1$. Consider now two of the other expressions. Let us postulate

$$\frac{3g_1 + g_2}{3(g_1 + g_2 + G_L)} > \frac{2G_L + g_2}{3(g_2 + G_L)}$$  \hfill (2.36)

This holds if

$$g_1(2g_2 + G_L) > 2G_L(g_2 + G_L)$$  \hfill (2.37)

which again is true, as can be seen by comparison of each of the product constituents. Amongst the $1 < \alpha$ conditions, it is also easy to see that

$$\frac{1}{3} > \frac{g_2}{3(G_2 + g_2)}$$  \hfill (2.38)

Thus, we are left with the final conditions on $\alpha$ as

$$\frac{1}{3} < \alpha < \frac{2G_L + g_2}{3(g_2 + G_L)}$$  \hfill (2.39)

Now let us consider the possible range within which $\alpha$ (and thus $V_Z$) can be chosen.

$$\Delta V_Z = \Delta \alpha V_1$$  \hfill (2.40)

Equivalently,

$$\Delta V_Z = V_1(\frac{2G_L + g_2}{3(g_2 + G_L)} - \frac{1}{3})$$  \hfill (2.41)

Thus,

$$\Delta V_Z = \frac{14G_L}{g_2 + G_L}$$  \hfill (2.42)

or

$$14 < V_Z < 14(1 + \frac{G_L}{g_2 + G_L})$$  \hfill (2.43)
This is the allowable range of variability for $V_Z$, assuming the values of $V_1$ and $V_2$ remain fixed at exactly 42 and 14 volts. Since $g_2 >> G_L$, this seems to be a very restrictive range.

2.3.3.6 Conclusions Concerning The Zener Circuit

After defining $\Delta V_Z$ as in Eq. (2.42), we will need to make sure that the Zener voltage can be maintained in that range, considering different operating temperature and device to device variability. Further, the circuit needs to work even if the bus voltages (in our model the bus voltages represent the 42V and 14V batteries) vary. Therefore the condition in Eq. (2.8) translates to

$$V_{Z\text{min}} > V_{2\text{max}}$$  \hspace{1cm} (2.44)

We have from [2] that the automobile will be expected to function with $V_2$ anywhere in the range of 9 to 16 volts, the protection circuit should also work in the face of variations of $V_1$ and $V_2$. To rigorously assess these possibilities, it would be necessary to redo much of the foregoing, using different values of $V_1/V_2$ and different values for $V_2$. But such extensive effort is probably unproductive.

The requirement in Eq. (2.44) and the required range of operation for $V_2$ tells us immediately that the lowest $V_Z$ will be above 16 volts. Yet that same Zener diode is required to reliably turn on following a fault even when $V_2$ is as low as 9 volts and $V_1$ is at the same time way below nominal, perhaps as low as 30 volts. The requirement in Eq. (2.42) shows that for nominal $V_1$ and $V_2$, for the circuit to operate as intended, the allowable range of $V_Z$ is quite limited, perhaps only 10% of the nominal $V_2$. If this analysis were repeated with $V_1 = 30V$ and $V_2 = 9V$, we would expect that the condition corresponding to Eq. (2.42) would restrict $V_Z$ to within a small range (say 10%) above 9 volts.

Since it is impossible for $V_Z$ to be both greater than 16 volts and also within 10% of 9 volts, the Zener circuit considered here works only if $V_1$ and $V_2$ are tightly constrained to their nominal values. When real world variability of operating conditions is considered, this circuit cannot always operate as intended.

2.4 Modification 2: Addition Of A Diode

We seek a further circuit modification which gives more flexibility in the selection of the Zener voltage $V_Z$ to make the circuit work in all conditions. The condition $i_{21} > i_2$ is the hardest condition to fulfill. Observe that the most restrictive condition on $\alpha$ was given by Eq. (2.27) which was a result of the $i_{21} > i_2$ condition. Here we introduce a modification to the circuit that will get us rid of this condition totally.
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Figure 2.9: Circuit Modification With The Diode

The modification is in the form of a diode placed at the 14V circuit as shown in Figure 2.9.

2.4.1 Desired Sequence Of Events With The Diode Modification

We want the following operation sequence to be followed with the Zener and the diode in place:

1. In the normal operation of the 14V circuit, the Zener is back biased but not to the Zener breakdown voltage. The diode is forward biased. Thus, the Zener acts as an open circuit and the diode acts as a short and therefore neither component affects normal circuit operation.

2. In the event of a 42V - 14V fault, the Zener goes into reverse breakdown and provides a shorting path to the ground. The diode however, become back biased and opens the circuit therefore isolating the 14V supply from the circuit.

3. Fuse F1 blows disconnecting the 42V circuit from the loads

4. The Zener goes into off state once again after Fuse F1 blows. The diode becomes conducting again.

5. Fuse F2 blows
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Figure 2.10: Comparison Of The Circuits With And Without The Zener Plus Diode Modification At The Time Of The Fault

2.4.2 Effectiveness Of The Diode Modification

We will prove the efficacy of this modified circuit with respect to the condition \( i_{21} > i_2 \). Consider Figure 2.10. This figure compares the circuit with and without the modification before Fuse F1 blows. Observe that, since now the diode opens the circuit, there is no current \( i_2 \) flowing. Thus the condition \( i_{21} > i_2 \) is always satisfied. At this time, we will refrain from actually analyzing the circuit to quantify its superiority with respect to the Zener-only modified circuit. Instead, we will introduce another modification to the circuit which will get us through the condition in Eq. (2.4) as stated here again.

\[
G_1 > G_{2_{max}}
\]  

(2.45)
2.5 Modification 3: Addition Of A PTC (Positive Temperature Coefficient) Device

With this modification, we hope to get rid of the condition in Eq. (2.45). We add the PTC device to the circuit as shown in Figure 2.11. Please note that what we are calling a PTC device is an abstract device having the same circuit element properties as a real PTC device, for example the Polyswitch® family of devices manufactured by Tyco Electronics. When a small current is passed through these devices, they present a small resistance. When the current is raised above a threshold, the resistance quickly rises. As the resistance rises, it approaches the voltage of the source and the current in the device falls. The device remains in its new, high resistance state for as long as the potential is maintained across it. When the potential is removed (or reduced to a low enough value), the transition reverses and the device becomes a low resistance.

We postulate an abstract device because we have learned that Tyco’s products, while exhibiting all the properties described above, will not provide adequate service life in the present application. We present this work because it illustrates the potential of a device with a strong positive temperature coefficient of resistivity. While we have not found a source for suitable devices, the existence of the Polyswitch® products offer hope that similar devices can be found. This same analysis also explains the performance of a circuit containing a synthesized circuit element (made e.g. with transistors) having the prescribed element properties.
2.5.1 Desired Sequence Of Events With The PTC Modification

We want the circuit to operate in the following sequence of events:

1. In the normal operating conditions, the Zener stays off and does not affect the functioning of the 14V circuit. The diode is forward biased and therefore does not affect the 14V circuit. The PTC device, due to the high voltage applied to it (42V), trips and becomes an open circuit. Thus, it does not affect the 42V circuit.

2. In the event of a fault, the Zener breaks down and conducts a large current so that Fuse F1 blows. The diode gets reverse biased and cuts off the 14V circuit. The PTC device stays tripped and thus is an open circuit still.

3. Fuse F1 blows.

4. The Zener goes back into off state due to the lessening of the voltage on it. The diode becomes forward biased and conducts again. The PTC device now working on a lower voltage goes into the conduction stage and thus provides a shorting path to the current from the 14V bus.

5. Fuse F2 blows.

2.5.2 Effectiveness Of The The PTC Modification

Keep in mind that all the conditions have been satisfied by the circuit without the PTC device except the one stated in Eq. (2.45). Observe that the PTC device has been added in parallel to the load $G_1$. It becomes active only when Fuse F1 has blown and at that time it is in the conduction state. Let us call the conductance of the PTC device (and any resistance added in series to it) as $G_{cond}$. Thus, it adds to $G_1$ (since they are in parallel). Thus, the condition in Eq. (2.45) changes to

$$G_1 + G_{cond} > G_{2max}$$  \hspace{1cm} (2.46)

Eq. 2.46 states that we should choose $G_1$ and $G_{cond}$ such that their sum is more than $G_2$. However, in practice, we cannot choose $G_1$. Thus, we say that if we can satisfy

$$G_{cond} > G_{2max}$$  \hspace{1cm} (2.47)

then we can be sure that the condition in Eq. (2.46) will always be satisfied. It is notable to see that the condition in Eq. (2.45) has been reduced to Eq. (2.47), effectively making it in our control. That is, we can design a PTC device such that it satisfies Eq. (2.47).
2.6 Conclusions

As discussed earlier, the PTC device that we have theorized is closest to a practical element known as the Polymeric Positive Temperature Coefficient or a PPTC device. We have analyzed the feasibility of the PPTC device in this circuit in Appendix A. Thus, in this chapter, we have tried to incorporate simple passive circuit elements to the original circuit and tried to implement the aforesaid fusing strategies. However, we have found that such implementations are either not robust enough to work on all operating conditions (Zener modification) or cannot be implemented with practical circuit elements (PTC device modification). Hence, we conclude that simple passive element modification will not be able to bring the circuit to a safe operating condition. In the next chapter, we will work on a strategy which works with active circuit elements and latching circuits to achieve the same end result.
Chapter 3

Active Circuit Modifications For The Dual Voltage System

3.1 Introduction

We have seen in chapter 1 that the dual voltage fault by itself cannot clear the fuses. Circuit modifications by passive components gives us an effective scheme of fault clearance. However, its implementation with practical circuit elements is not feasible. Apart from this, we have only considered constant resistance loads which are switchable. In general, we can have any type of loads in an automobile. Thus, the discussions in the previous chapters was incomplete in that sense. In this chapter, we will incorporate different types of loads and introduce a new protection circuit based on fault sensing and active correction. The solution proposed here is simple and robust.

3.1.1 Fault Considered

As said earlier, we will be considering generic loads on the automobile. Thus, for sake of completeness, we will introduce the fault considered with general loads designated by $L_1$ and $L_2$. The explanations for the various circuit parameters are as follows.

$L_1 = $ Generic 42V load
$L_2 = $ Generic 14V load
$I_{F1} = $ Fusing current of fuse $F_1$
$I_{F2} = $ Fusing current of fuse $F_2$

Figure 3.1 can be used to represent any possible 42V–14V fault. Faults between different circuits will result in different values of the parameters $I_{F1}$ and $I_{F2}$. Also $L_1$ and $L_2$ can take different configurations as purely resistive, constant current, or even constant power loads. Note that even for a fixed pair of circuits, it is possible for $L_1$ and $L_2$ to assume different values at different times. In particular, it is quite common for electrical loads to be turned off in which case the corresponding load is essentially absent.
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3.2 Equivalent Circuit At Fault

We will introduce the equivalent circuit at fault with the generic loads in place instead of the constant resistance loads. Figure 3.2 shows the circuit. Table 3.1 defines the parameters of the circuit of Figure 3.2. We will also use the definitions of Table 3.2 for the various currents in the circuit. Please refer to Figure 3.3 for a diagrammatic definition of the currents.

3.3 Fault Clearance

In this section, we introduce the concept of an ideal fault detector system and try to develop its properties with respect to the actions it takes after the fault occurs. Assume that we
have a detector system which tells us exactly when the 42V - 14V fault occurs and assume also that it sits on the 14V circuit load. We want the following sequence of events to occur:

- The system detects the 42V - 14V fault.
- Once, it has detected the fault, the system shorts the 14V load directly to ground. Lets call this for the time being the "crowbar" action. Both the 42V and the 14V loads are now shorted directly to ground.
- Since the 42V and the 14V fuses are designed to blow in the event of such a fault (i.e the loads shorting directly to ground), they blow out.
- Both the 42V and the 14V sources are therefore cleared from the fault.

Fig. 3.4 shows the above. It is also obvious that the detection system will be an active circuit which uses some voltages and currents in the circuit and makes a decision based on
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Figure 3.3: Current Definitions

(a) Normal operating conditions

(b) At the time of fault
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1) System detects fault
2) Shorts the load
3) Fuses blow
4) Loads isolated

Figure 3.4: Operation Of The Fault Detector System

that. It is also clear that this detection system can be put on either of the 42V or the 14V circuits with essentially the same outcome.

3.4 Issues With The Fault Detection System

The ideal detection system that we just introduced needs to follow certain properties. Firstly, it preferably should not take inputs from both the 42V and the 14V circuits. That is because it does not know beforehand the other circuit to which the one associated with the protection device has faulted. If all the inputs to detection system come from the circuit to which it is linked, a simple system results. If information from the circuit to which it has faulted is required, it will be necessary to receive information from all the candidate circuits. Further, in the event of a fault, there will need to be means to determine which of the inputs from the candidate circuits contains actionable information. We would also want to inputs to this circuit to be simple and discrete. That will help to simplify the design of the system and reduce its cost.
3.5 Fault Indicators

For a 42V-14V fault, we find the following indicators that can help us detect the fault. Let’s start with the fault indicator sitting on the 42V bus.

- Fuse F1 blowing: If the fuse blows in response to a 42V-14V fault, we can use this event to trigger our crowbar, which will also blow the 14V circuit fuse $F_2$, since its load is also effectively shorted.

- Fuse F2 blowing: If the fuse blows in response to a 42V-14V fault, we can use this event to trigger our crowbar, which will also blow the 42V circuit fuse $F_1$, since its load is also effectively shorted.

- Load voltage falling and Fuse Current rising in the 42V circuit: We can use this condition to trigger our crowbar. (Note that this indicator will not work if there is a constant power load attached to the bus under consideration.)

- Load voltage rising and Fuse current rising in the 14V circuit. (This indicator will also not work in the case of a constant power load attached to the circuit.)

Note that we did not separate voltage falling and current rising as independent indicators of the 42V-14V fault. This is so because in the accepted normal operation of the 42V circuit, the bus voltage (and thus the load voltage) may fall [3] and thus can trigger a false alarm. In a similar vein, we did not separate the voltage rise and current rise as two different indicators for the 14V circuit [2]. Also note that even if any one of the actions from above takes place in the event of a fault, we can use it effectively to activate our crowbar. That means that in one fault event Fuse $F_1$ might blow and trigger the crowbar sitting on the 42V load, while in another event Fuse $F_2$ might blow and trigger a crowbar sitting on the 14V load resulting in essentially the same action. The simplest and the most discrete signal might be blowing of the fuses $F_1$ or $F_2$. In the next section, we will discuss its reliability as a fault indicator.

3.6 Fuse Blowing As A Fault Indicator

In the last section we talked about the crowbar action. It would be a simple act to provide a crowbar at each fuse. If we are able additionally to provide a reliable indication that a given circuit is involved is a bus-to-bus short circuit, we could trigger the corresponding crowbar and return the system to a safe state. In this section, we will show that the blowing
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of a fuse can serve as the reliable indication we need.

To provide a reliable basis for action, it would be sufficient to know that in the event of any 42V-14V fault, either fuse \( F_1 \) or fuse \( F_2 \) will blow. To this point, we have not demonstrated that this is the case. In this section, we will develop the conditions under which we can rely on a bus-to-bus fault blowing either fuse \( F_1 \) of fuse \( F_2 \). We will achieve this by placing restrictions on the range of values allowable for the equivalent source conductances \( g_1 \) and \( g_2 \). In particular, we can achieve our guaranteed fuse-blowing objectives by making these conductances large enough so that the post-fault current will blow a fuse.

In practice, the conditions we will derive do not require the system designer to do things much differently than he would in the absence of the possibility of bus-to-bus fault. We will derive our conditions by requiring that under reasonable circumstances, only a small fraction of the source voltage appears across the source conductance, the larger fraction being applied to the load. In most cases, the system will achieve this objective at least approximately, even if it were designed without consideration of 42V-14V faults. All we will do is apply a quantitative restriction.

In a few cases, the system designer may need to change his design to meet our restriction. But if that happens, the change will probably be restricted to using a slightly larger wire cross section than would otherwise have been chosen. The cost and mass impact on the wire harness and the vehicle should be very modest.

For generality’s sake, we will consider not only switchable resistance loads, but also switchable constant current and constant power loads. The reader will see that inclusion of these multiple load types substantially complicates the development which we will present. But even with this additional effort, we do not claim full generality. A circuit could, for example, serve a combination of these load types. It seems plausible that a system that is safe for both a purely resistive load and a purely constant-power load would be safe for a load which was a combination of these two types. But we do not provide a proof of this statement.

Even though this analysis lacks full generality, it nevertheless provides a substantial insight into a powerful method to make a system safe against 42V-14V faults. We show by example the methods necessary to expand this work to include other load types. If a system were to be designed using another load type, the designer could easily perform the indicated analysis, following by analogy the steps described here. Or he could restrict himself to load cases analyzed here.

Note that the proposed system of detection and protection will be designed for only the case of hard (i.e. low impedance) 42V-14V shorts. These will comprise the vast majority of
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all 42V-14V faults. It is formally possible to have a high impedance short, which does not blow a fuse but still poses a hazard. The system being investigated cannot detect such a short. But this is probably an acceptable risk. The mechanisms which would produce such a high impedance short exist on today's auto fleet (where the risk is a high impedance short to ground). Today's fusing does not respond to high impedance shorts to ground, and the risk is evidently acceptable.

3.6.1 Circuit Model Considered

Fig. 3.3 (b) shows the general circuit that we will analyze. The character of the load present on any circuit at the time of a fault can vary widely. Quite commonly, the load will appear to the source to be a fixed resistance. In other cases, internal controls can cause a load to assume a constant power characteristics, in which the current drawn by the load rises as voltage falls. Constant current loads are a third possibility. Or the load on a given circuit could be some combination of these types. We will consider all the cases where the load on any circuit has one of these characteristics (constant resistance, constant current and constant power). Note that there would be 9 different possible load combinations which will give rise to different circuits for analysis. These are shown in the following list. The symbol $G_{42}$ stands for a 42V constant resistance load. Similarly $I_{14}$ stands for a 14V constant current load. A load designated by the symbol $P$ is a constant power load.

1. $G_{42}$ shorting with $G_{14}$
2. $G_{42}$ shorting with $I_{14}$
3. $G_{42}$ shorting with $P_{14}$
4. $I_{42}$ shorting with $G_{14}$
5. $I_{42}$ shorting with $I_{14}$
6. $I_{42}$ shorting with $P_{14}$
7. $P_{42}$ shorting with $G_{14}$
8. $P_{42}$ shorting with $I_{14}$
9. $P_{42}$ shorting with $P_{14}$
3.6.2 Circuit Analysis

By considering the three kinds of loads, we have added complexity to the problem. Further, in the case of a constant power load, the current is a solution to a quadratic equation (see Appendix B). Although the circuits are simple enough that an analytical solution may have been possible, we chose a general numerical approach to the problem, using simulations in MATLAB to verify the circuit properties for all the operating conditions.

3.6.3 Electrical System Design Assumption

We will require that the electrical system feeding a given load be designed to assure that no more than a certain fraction of the open-circuit voltage will appear across the equivalent series resistance of the source, when the source is at its nominal value (42V or 14V). We will quantize this fraction with the symbol $k$. Thus, $k = 6$ means that $\frac{1}{6} \times$ or less of the voltage is dropped across the equivalent series resistance. If $k = 6$, than at least 83% ($5/6$) of the power delivered by the source is being consumed by the load. We will apply the same value of $k$ to both the 42V and the 14V circuits. Thus the voltage drop across $g_1$ is no more than $V_1/k$, and the voltage drop across $g_2$ is no more than $V_2/k$.

Although we choose to use one value of $k$ for both voltages, we will choose to use different values of $k$, depending on the type of load serves. Superficially, it would seem simpler to choose a single value of $k$, independent of the load type. But, when considered in more detail this choice leads to substantial complications. For example, a choice of $k = 6$ seems eminently reasonable for a resistive load. But for a constant power load, this same choice results in nearly half the source voltage being lost to a drop across the equivalent series resistance when the 14V source voltage is at the lower limit of its allowable range. This condition is at the minimum unattractive, and for many cases, may result in an unallowable temperature rise in the conductor serving the load.

So we choose to assign a different $k$ to each load type, giving rise to the self explanatory symbols $k_{res}$, $k_{cur}$ and $k_{pow}$. For a simpler discussion in the next sections, we will further define the ratio variables given in Table 3.3. To choose the various ratio variables, we will start with a choice of $k_{res}$, and then compute the remaining variables with the constraint that for a given equivalent series resistance, the maximum current, $I_{MAX}$, considering the full range of allowable source voltage, will be the same, independent of the type of load.
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<table>
<thead>
<tr>
<th>Ratio Variable</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>( j_{res} )</td>
<td>Constant resistance load ratio parameter for bus voltage at its minimum value</td>
</tr>
<tr>
<td>( j_{cur} )</td>
<td>Constant current load ratio parameter for bus voltage at its minimum value</td>
</tr>
<tr>
<td>( j_{pow} )</td>
<td>Constant power load ratio parameter for bus voltage at its minimum value</td>
</tr>
<tr>
<td>( k_{res} )</td>
<td>Constant resistance load ratio parameter for bus voltage at its nominal value</td>
</tr>
<tr>
<td>( k_{cur} )</td>
<td>Constant current load ratio parameter for bus voltage at its nominal value</td>
</tr>
<tr>
<td>( k_{pow} )</td>
<td>Constant power load ratio parameter for bus voltage at its nominal value</td>
</tr>
<tr>
<td>( l_{res} )</td>
<td>Constant resistance load ratio parameter for bus voltage at its maximum value</td>
</tr>
<tr>
<td>( l_{cur} )</td>
<td>Constant current load ratio parameter for bus voltage at its maximum value</td>
</tr>
<tr>
<td>( l_{pow} )</td>
<td>Constant power load ratio parameter for bus voltage at its maximum value</td>
</tr>
</tbody>
</table>

Table 3.3: Currents in the Different Loads

3.7 Generalized Approach To Circuit Analysis

The above assumptions are very useful in the sense that they help us to find the upper limit of the conductance of a constant resistance load, current in a constant current load and power in a constant power load. We show below how this is done. We will use the following nomenclature for the voltage source values (with "x" denoting that the voltage source can either be 14V or 42V):

1. \( V_{x_{\text{min}}} \): Voltage \( V_x \) operating at minimum value.
2. \( V_{x_{\text{nom}}} \): Voltage \( V_x \) operating at nominal value.
3. \( V_{x_{\text{max}}} \): Voltage \( V_x \) operating at maximum value.

3.7.1 Constant Resistance Load

Relation Between Ratio Variables: For a constant resistance load served by a resistively modelled series impedance, the ratio of the voltage dropped on the series resistance will be a constant irrespective of the voltage impressed. Thus,

\[
 j_{res} = k_{res} = l_{res} \tag{3.1}
\]
Limit On Load Values: Fig. 3.5(a) shows a voltage source driving a constant resistance load. The drop across \( g_x \) (let denote it by \( v_{g_x} \)) in this case turns out to be

\[
v_{g_x} = \frac{V_x G_x}{g_x + G_x}
\]

(3.2)

Now since,

\[
v_{g_x} < \frac{V_x}{k_{res}}
\]

(3.3)

We get,

\[
\frac{V_x G_x}{g_x + G_x} < \frac{V_x}{k_{res}}
\]

(3.4)

which simplifies to

\[
G_x < \frac{g_x}{k_{res} - 1}
\]

(3.5)

or

\[
G_{x_{max}} = \frac{g_x}{k_{res} - 1}
\]

(3.6)

Thus, our assumption of proper wire harness design allows us to write an expression for the upper limit of how large the load can be, given the magnitude of the equivalent series source resistance. As source voltage varies, the current drawn by a constant resistance load is maximum when the voltage is maximum. Its value is

\[
I_{MAX} = \frac{V_{x_{max}} G_x}{I_{res}} = \frac{V_{x_{max}} g_x}{k_{res}}
\]

(3.7)

We will limit the current in the constant current and the constant power loads by this value and calculate the \( j, k \) and \( l \) values for them.

Let us calculate the ratio variables for the 14V circuit. If we choose a value of \( k_{res} = 6 \), then we have

\[
j_{res} = k_{res} = l_{res} = 6
\]

(3.8)

With \( I_{MAX} = 40A \), we get (from Eq. 3.7),

\[
g_x = g_1 = 15 \text{ mhos}
\]

(3.9)
3.7.2 Constant Current Load

Relation Between Ratio Variables: For a constant current load, the current remains constant as the input voltage varies from $V_{\text{min}}$ through $V_{\text{nom}}$ to $V_{\text{max}}$. Thus, we have

$$I_x = \frac{V_{\text{min}} g_x}{j_{\text{cur}}} = \frac{V_{\text{nom}} g_x}{k_{\text{cur}}} = \frac{V_{\text{max}} g_x}{l_{\text{cur}}} \quad (3.10)$$

Therefore,

$$j_{\text{cur}} = k_{\text{cur}} \frac{V_{\text{min}}}{V_{\text{nom}}} , \quad l_{\text{cur}} = k_{\text{cur}} \frac{V_{\text{max}}}{V_{\text{nom}}} \quad (3.11)$$

Limit On Load Values: This case is straightforward since the maximum current that can flow in a constant resistance load is also the limit on a constant current load. Thus,

$$I_x < I_{\text{MAX}} = \frac{V_{\text{max}} g_x}{k_{\text{res}}} \quad (3.12)$$

This condition can be used to define $k_{\text{cur}}$ which is the drop at nominal voltage conditions. For a constant current load, the current remains the same irrespective of the voltage. Thus, if the load is drawing $I_{\text{max}}$ at $V_{\text{max}}$, it will draw it at $V_{\text{nom}}$ too. Thus,

$$I_{\text{MAX}} = \frac{V_{\text{max}} g_x}{k_{\text{res}}} = \frac{V_{\text{nom}} g_x}{k_{\text{cur}}} \quad (3.13)$$

Thus, $j_{\text{cur}}$ and $l_{\text{cur}}$ can also be found.

With our earlier choice of $k_{\text{res}} = 6$, we get from Eq. 3.13 for $V_{\text{min}} = 9V$, $V_{\text{nom}} = 14V$ and $V_{\text{max}} = 16V$

$$k_{\text{cur}} = k_{\text{res}} \frac{V_{\text{nom}}}{V_{\text{max}}} = 5.25 \quad (3.14)$$

and from Eq. 3.11

$$j_{\text{cur}} = 3.375 , \quad l_{\text{cur}} = 6 \quad (3.15)$$

3.7.3 Constant Power Load

Relation Between Ratio Variables: In this case, it's the power that remains constant as the voltage varies from $V_{\text{min}}$ through $V_{\text{nom}}$ to $V_{\text{max}}$. For details of the analysis of constant power loads attached to a constant voltage bus, refer to Appendix B. We have repeated Eq B.3 here for convenience

$$v_{gs} = V_{\text{nom}} - \frac{V_x + \sqrt{V_x^2 - 4P_x}}{2} g_x \quad (3.16)$$
Let's write this equation for the voltage at its nominal value.

\[ v_{gs} = V_{x_{nom}} - \frac{V_{x_{nom}}^2 + \sqrt{V_{x_{nom}}^4 - 4 \frac{P_x}{g_x}}}{2} < \frac{V_{x_{nom}}}{k_{pow}} \]  

(3.17)

where we have included the criteria of dropping less than \( \frac{1}{k_{pow}} \) of the total voltage across the series resistance. This translates into

\[ P_x < g_x V_{x_{nom}}^2 \left( \frac{k_{pow} - 1}{k_{pow}^2} \right) \]  

(3.18)

For the voltage at its minimum value, we will have a similar expression

\[ P_x < g_x V_{x_{min}}^2 \left( \frac{j_{pow} - 1}{j_{pow}^2} \right) \]  

(3.19)

Since the power in both expressions is the same, we can equate them and also include the expression for the variables at \( V_x = V_{x_{max}} \)

\[ g_x V_{x_{min}}^2 \left( \frac{j_{pow} - 1}{j_{pow}^2} \right) = g_x V_{x_{nom}}^2 \left( \frac{k_{pow} - 1}{k_{pow}^2} \right) = g_x V_{x_{max}}^2 \left( \frac{l_{pow} - 1}{l_{pow}^2} \right) \]  

(3.20)

These equations define the relationship between \( j_{pow}, k_{pow} \) and \( l_{pow} \).

**Limit On Load Values:** In the case of a constant power load, the maximum current is drawn when the voltage applied to the load is at its minimum value. Thus, \( I_{max} \) is achieved at \( V_{x_{min}} \). Thus,

\[ I_{MAX} = \frac{V_{x_{max}} g_x}{l_{res}} = \frac{V_{x_{min}} g_x}{j_{pow}} \]  

(3.21)

Thus,

\[ j_{pow} = l_{res} \frac{V_{x_{min}}}{V_{x_{max}}} \]  

(3.22)

Thus, we can compute \( j_{pow} \) and \( l_{pow} \) too. The maximum power is given by Eq. 3.18 and is thus,

\[ P_{x_{max}} = g_x V_{x_{nom}}^2 \left( \frac{k_{pow} - 1}{k_{pow}^2} \right) \]  

(3.23)

The values for the ratio variables for the constant power loads will therefore be (from Eq. 3.22),

\[ j_{pow} = 3.37 \]  

(3.24)

And from Eq. 3.20 we have,

\[ k_{pow} = 10.5 \]  

(3.25)
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3.7.4 Load Value Limits And Design Criteria And The Value Of $k_{res}$

The aim of the previous discussion was to develop a strategy for choosing loads value limits (given by $G_{z_{max}}$, $I_{z_{max}}$ and $P_{z_{max}}$ in Eq. 3.6, Eq. 3.13 and Eq. 3.23) and design criteria to ensure these maximum values. The design criteria are in the form of the $k$ values since an electrical system designer would want to work with nominal values. To summarize the discussions in the previous sections, we will state the final results as thus, starting with a chosen value of $k_{res}$. By, Eq. 3.13

$$k_{cur} = k_{res} \frac{V_{z_{nom}}}{V_{z_{max}}} \quad (3.27)$$

By eliminating $j_{pow}$ between Eq. 3.21 and Eq. 3.20, we get,

$$k_{pow} = \frac{2}{1 - \sqrt{1 - \left(\frac{V_{z_{min}}}{V_{z_{nom}}}\right)^2} [1 - \left(\frac{k_{res}(\frac{V_{z_{min}}}{V_{z_{max}}})-2}{k_{res}(\frac{V_{z_{min}}}{V_{z_{max}}})^2}\right]} \quad (3.28)$$
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<table>
<thead>
<tr>
<th>Constant Resistance Load</th>
<th>Constant Current Load</th>
<th>Constant Power Load</th>
</tr>
</thead>
<tbody>
<tr>
<td>( j )</td>
<td>( j_{res} = 6 )</td>
<td>( j_{pow} = 3.38 )</td>
</tr>
<tr>
<td>( k )</td>
<td>( k_{res} = 6 )</td>
<td>( k_{pow} = 10.5 )</td>
</tr>
<tr>
<td>( l )</td>
<td>( l_{res} = 6 )</td>
<td>( l_{pow} = 14.08 )</td>
</tr>
<tr>
<td>( G_{2max} = 3 \text{ mhos} )</td>
<td>( I_{2max} = 40 \text{ A} )</td>
<td>( P_{2max} = 253 \text{ W} )</td>
</tr>
</tbody>
</table>

Table 3.4: Values For Ratio Variables And Maximum Loads For The 14V Circuit For \( g_2 = 15 \text{ mhos} \)

Thus, we have expressed all the \( k \)'s in terms of \( k_{res} \). Now, we need to take care of the maximum load values. We have,

\[
G_{x_{max}} = \frac{g_x}{k_{res} - 1} \quad (3.29)
\]

\[
I_{x_{max}} = \frac{V_{x_{nom}} g_x}{k_{cur}} \quad (3.30)
\]

\[
P_{x_{max}} = g_x V_{x_{nom}}^2 \left( \frac{k_{pow} - 1}{k_{pow}} \right) \quad (3.31)
\]

Thus, started with choosing a value for \( k_{res} \), we can decide the values of \( k_{cur} \) and \( k_{pow} \) and also come up with the maximum values for the load ratings of constant current and constant power loads.

So there are 3 \( k \)'s that we need to consider, namely \( k_{res} \), \( k_{cur} \) and \( k_{pow} \). A similar set of \( k \)'s exist for 42V and the 14V systems. So, our 14V electrical system designer would keep track of 3 values so that the maximum current in any 14V circuit is limited to a certain value. Similarly, the 42V electrical system designer will also keep track of the rest of the 3 \( k \)'s. For illustration, we have summarized the \( k \) values for the 14V circuit in Table 3.4. We have also included the maximum load ratings based on Eq. 3.29, Eq. 3.30 and Eq. 3.31. Thus, a 14V wire harness designer will keep the numbers \( k_{res} = 6 \), \( k_{cur} = 5.25 \) and \( k_{pow} = 10.5 \) in mind. For a choice of \( k = 6 \) for the 42V circuit we get the following table shown in Table 3.5. For reference, the voltages \( V_{1_{min}}, V_{1_{nom}} \) and \( V_{1_{max}} \) are 30V, 42V and 48V. The assumption taken in calculating the values of the maximum loads is that the value of \( g_1 \) which gives the maximum current in the 42V circuit is the same as the value of \( g_2 \) which gives the maximum current in the 14V circuit. Thus, for the maximum current condition \( g_1 = g_2 = 15 \text{ mhos} \). This choice is completely arbitrary and is at the sole discretion of the designer. If he wants to serve loads with current rating higher than 120A (or for that matter power rating higher than 2683W), he will need to use harnesses with higher conductance than 15 mhos.
Table 3.5: Values For Ratio Variables And Maximum Loads For The 42V Circuit For $g_1 = 15$ mhos

![Figure 3.6: Circuit For The Discussion Of The Fuse Current Ratings](image)

### 3.7.5 Fuse Ratings

The fuses are designed such that they should not blow in the event of supply voltage swings. This means that they allow a suitable range of supply voltage variation for which they would not blow. The fuse ratings are therefore closely linked to the maximum current that can flow in the circuit. Therefore, if we designate the upper limits of the range as $V_{1\text{max}}$ and $V_{2\text{max}}$ respectively for the 42V and the 14V circuits, we can determine the lower bound on the fuse rating current (defined in Table 3.2) as

$$I_{F1}^* = \frac{V_{1\text{max}} g_1}{k_{res}}$$  \hspace{1cm} (3.32)$$

$$I_{F2}^* = \frac{V_{2\text{max}} g_2}{k_{res}}$$  \hspace{1cm} (3.33)$$
3.7.6 General Circuit Equation

Consider the generalized circuit model shown in Fig. 3.7. We want to analyze this circuit for the case when the loads 1 and 2 can be any of constant resistance, constant current and constant power. Consider Table 3.6. It shows the currents flowing in the loads given the voltage $V$ applied on them. Thus, for example, if we want to analyze a 42V constant resistance load shorting with a 14V constant current load then we can find the total load current as

$$I_L = I_{L1} + I_{L2} = VG_1 + I_2$$  \hspace{1cm} (3.34)

Thus, for any load combination we will get the total load current $I_L$ as a function of $V$. Let's call this function $f(V)$ for the time being.

$$I_L = f(V)$$  \hspace{1cm} (3.35)

This $I_L$ is also equal to $i_1 - i_2$. Thus

$$i_1 - i_2 = I_L = f(V)$$  \hspace{1cm} (3.36)
or,

\[(V_1 - V)g_1 + (V_2 - V)g_2 = I_L = f(V)\]  

(3.37)

### 3.7.7 Choice Of Bus Voltages \(V_1\) And \(V_2\)

Another thing to be noted is that, in the event of a fault, the voltages may not be at their designed values of 42V and 14V. They may be undergoing a dc swing as explained earlier. We need to find the values of \(V_1\) and \(V_2\) which minimizes the fault currents \(i_1\) and \(i_2\). Let us call this as the worst case bus voltage condition. This can be done by analyzing the derivatives \(\frac{\delta V}{\delta V_1}\), \(\frac{\delta V}{\delta V_2}\), \(\frac{\delta f}{\delta V_1}\) and \(\frac{\delta f}{\delta V_2}\). For example, to evaluate \(\frac{\delta f}{\delta V_1}\), we will begin with Eq. (3.37) and take its derivative with respect to \(V_1\).

\[(1 - \frac{\delta V}{\delta V_1})g_1 + (0 - \frac{\delta V}{\delta V_1})g_2 = \frac{\delta f(V)}{\delta V} \frac{\delta V}{\delta V_1}\]  

(3.38)

Thus,

\[\frac{\delta V}{\delta V_1} = \frac{g_1}{g_1 + g_2 + f'(V)}\]  

(3.39)

where we have replaced \(\frac{\delta f(V)}{\delta V}\) with \(f'(V)\). Now, since

\[i_1 = (V_1 - V)g_1\]  

(3.40)

we get,

\[\frac{\delta i_1}{\delta V_1} = (1 - \frac{\delta V}{\delta V_1})g_1\]  

(3.41)

Substituting \(\frac{\delta V}{\delta V_1}\) from Eq. (3.39), we get,

\[\frac{\delta i_1}{\delta V_1} = \frac{g_1(g_2 + f'(V))}{g_1 + g_2 + f'(V)}\]  

(3.42)

In a similar fashion, we can find out all the derivatives \(\frac{\delta V}{\delta V_1}\), \(\frac{\delta f}{\delta V_1}\), \(\frac{\delta f}{\delta V_2}\) and \(\frac{\delta f}{\delta V_2}\). Thus, all the derivatives are given by

\[\frac{\delta l_1}{\delta V_1} = \frac{g_1(g_2 + f'(V))}{g_1 + g_2 + f'(V)}\]  

(3.43)

\[\frac{\delta l_1}{\delta V_2} = \frac{-g_1 g_2}{g_1 + g_2 + f'(V)}\]  

(3.44)

\[\frac{\delta l_2}{\delta V_1} = \frac{-g_2(g_1 + f'(V))}{g_1 + g_2 + f'(V)}\]  

(3.45)

\[\frac{\delta l_2}{\delta V_2} = \frac{g_1 g_2}{g_1 + g_2 + f'(V)}\]  

(3.46)
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<table>
<thead>
<tr>
<th>Case</th>
<th>Load Combination</th>
<th>$f(V)$</th>
<th>$f'(V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$G_{42} - G_{14}$</td>
<td>$V_{G1} + V_{G2}$</td>
<td>$G_1 + G_2$</td>
</tr>
<tr>
<td>2</td>
<td>$G_{42} - I_{14}$</td>
<td>$V_{G1} + I_2$</td>
<td>$G_1$</td>
</tr>
<tr>
<td>3</td>
<td>$I_{42} - G_{14}$</td>
<td>$I_1 + V_{G2}$</td>
<td>$G_2$</td>
</tr>
<tr>
<td>4</td>
<td>$I_{42} - I_{14}$</td>
<td>$I_1 + I_2$</td>
<td>$0$</td>
</tr>
<tr>
<td>5</td>
<td>$G_{42} - P_{14}$</td>
<td>$V_{G1} + P_2/V$</td>
<td>$G_1 - P/V^2$</td>
</tr>
<tr>
<td>6</td>
<td>$I_{42} - P_{14}$</td>
<td>$I_1 + P_2/V$</td>
<td>$-P_2/V^2$</td>
</tr>
<tr>
<td>7</td>
<td>$P_{42} - G_{14}$</td>
<td>$P_1/V + V_{G2}$</td>
<td>$-P_1/V^2 + G_2$</td>
</tr>
<tr>
<td>8</td>
<td>$P_{42} - I_{14}$</td>
<td>$P_1/V + I_2$</td>
<td>$-P_1/V^2$</td>
</tr>
<tr>
<td>9</td>
<td>$P_{42} - P_{14}$</td>
<td>$P_1/V + P_2/V$</td>
<td>$-P_1/V^2 - P_2/V^2$</td>
</tr>
</tbody>
</table>

Table 3.7: $f'(V)$ Values For The Different Load Combinations Under Consideration

Given,

\[ g_2 + f'(V) > 0 \quad \text{and} \quad g_1 + f'(V) > 0 \]  
(3.47)

or,

\[ f'(V) > -g_1 \quad \text{and} \quad f'(V) > -g_2 \]  
(3.48)

we can say that all the derivatives will either be positive (\(\frac{\partial f}{\partial V_1}\) and \(\frac{\partial f}{\partial V_2}\)) or negative (\(\frac{\partial f}{\partial V_1}\) and \(\frac{\partial f}{\partial V_2}\)). Thus, given condition in Eq. (3.48), we can say that \(i_1\) and \(i_2\) minimize when \(V_1\) minimizes and \(V_2\) maximizes. This is therefore the worst case bus voltage condition that we were looking for. In other words, if \(V_1\) is at its minimum and \(V_2\) is at its maximum (given Eq. (3.48)), we will have both the fault currents at their minimum values. Let us see the load combinations for which this condition is obeyed. See Table 3.7. The cases for \(G_{42} - G_{14}\), \(G_{42} - I_{14}\), \(I_{42} - G_{14}\) and \(I_{42} - I_{14}\) are pretty straight forward. For them, \(f'(V) \geq 0\) and thus the condition in Eq. (3.48) is satisfied. Let us analyze the case for \(I_{42} - P_{14}\). Condition in Eq. (3.48) would mean

\[ f'(V) = -P_2/V^2 > -g_1 \]  
(3.49)

Thus,

\[ P_2/V^2 < g_1 \]  
(3.50)

Let us try to maximize the left hand side of this equation. The maximum power that bus voltage \(V_2\) can provide is given by (See Appendix B)

\[ P_{2\text{max}} = \frac{V_2^2 g_2}{4} \]  
(3.51)

Substituting,

\[ \frac{V_2^2 g_2}{4V^2} < g_1 \]  
(3.52)

\[ -52 - \]
Let us replace $V_2^2$ with $V^2$ since $V > V_2$,

$$\frac{V^2 g_2}{4V_2^2} < g_1$$  \hspace{1cm} (3.53)

Thus, we get

$$\frac{g_2}{4} < g_1$$  \hspace{1cm} (3.54)

which is plausible but not always true. The other condition

$$f'(V) = -P_1/V^2 > -g_2$$  \hspace{1cm} (3.55)

will lead to

$$\frac{g_2}{4} < g_2$$  \hspace{1cm} (3.56)

which is always satisfied. Thus, for the case $I_{42} - P_{14}$, we can be sure that the derivatives $\frac{g_1}{V_1}$ and $\frac{g_2}{V_1}$ will be positive and negative respectively. Hence, for this case, we can put $V_1$ at its extremum value (i.e. minimum), but we cannot do the same with $V_2$. The case for $G_{42} - P_{14}$ also behaves in the same way since $f'(V)$ for that can be equal to $f'(V)$ for $I_{42} - P_{14}$ since,

$$G_1 - P/V^2 = -P/V^2 \quad \text{for} \quad G_1 = 0$$  \hspace{1cm} (3.57)

We will do a similar analysis for the case $P_{42} - I_{14}$.

$$P_1/V^2 < g_1$$  \hspace{1cm} (3.58)

Let us try to maximize the left hand side of this equation. The maximum power that bus voltage $V_1$ can provide is given by (See Appendix B)

$$P_{1\text{max}} = \frac{V_1^2 g_1}{4}$$  \hspace{1cm} (3.59)

Substituting,

$$\frac{V_1^2 g_1}{4V_2^2} < g_1$$  \hspace{1cm} (3.60)

Let us replace $V$ with $V_2$ to maximize the left hand side.

$$\frac{V_2^2 g_1}{4V_2^2} < g_1$$  \hspace{1cm} (3.61)

which leads to

$$V_2 > V_1/2$$  \hspace{1cm} (3.62)

Obviously, barring the case when $V_2 = 16V$ and $V_1 = 30V$, we are always sure that $V_2 < V_1/2$. Thus, we see that the condition in Eq. (3.48) is never satisfied for the case of the load being $P_{42} - I_{14}$. Similar statements can be made for the load cases being
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Thus, for those load combinations the worst case bus voltages are not the extremum values (i.e. minimum for $V_1$ and maximum for $V_2$).

Thus, for the first four load cases, we have the worst case bus voltage condition for both $V_1$ and $V_2$, for the next two cases, we have the worst case bus voltage in an explicit form only for $V_1$, while for the last three cases, we do not have the condition in any explicit form. We could, if we wanted, have three different types of simulation for these three types. However, for the sake of simplicity, we will treat the last five cases with one method of solution and simulate them for varying values of both $V_1$ and $V_2$. This means that for the first four cases, the bus voltages can be fixed to their worst case values and the rest of the circuit can be simulated for the remaining independent parameters. For the last five load cases, the bus voltages will also be independent parameters which can vary over their entire range (i.e. $30V < V_1 < 48V$ and $9V < V_2 < 16V$).

3.8 Simulation Settings

Now that we have relations for the fault currents and the fuse ratings, we can simulate the circuit for a range of the independent circuit parameters and check whether one of the two fuses blow or not. We choose the following values for the parameters.

- $V_{1\text{max}} = 48V$
- $V_{2\text{max}} = 16V$
- $V_{1\text{nom}} = 42V$
- $V_{2\text{nom}} = 14V$
- $V_{1\text{min}} = 30V$
- $V_{2\text{min}} = 9V$
- $F_1 = 1.5$
- $F_2 = 1.5$
- $k_{res} = 6$ for both the 14V and the 42V circuits

The values $F_1$ and $F_2$ refer to the safety factor attached to the fuses. In circuit terms, it means that the fuse would not blow until its rated current is exceed by $F_1$ times its value.
Mathematically, for fuse $F_1$ to blow,

$$i_1 > F_1 \cdot I^2_{F_1} \quad (3.63)$$

### 3.8.1 Independent Circuit Parameters

In this section, we will try to ascertain the independent circuit parameters for the simulation settings. Let’s take the example of a 42V constant resistance load shorting with a 14V constant power load. The following can be separated as independent variables.

- The two conductances $g_1$ and $g_2$ can be varied independently of each other. Eq. 3.9 gives the value of $g_x = 15$ mhos for the 14V circuit. Thus, $g_2$ can vary from 0-15 mhos. Since, we do not know the value of the maximum current in the 42V circuit to carry out a similar calculation for $g_1$, we will choose its range from 0-15 mhos too. Thus, $g_1$ and $g_2$ vary from 0-15 mhos.

- The conductance value of the 42V load ($G_1$) can be treated as independent provided it obeys the relation given in Eq. (3.5). Thus, it can be varied from 0 to $\frac{V_1}{g_1}$.

- The power value of the 14V constant power load ($P_2$) can be treated as independent provided it obeys the relation given in Eq. (3.31). The computed value for $k_{pow}$ is 10.5. And therefore, $P_2$ can be varied from 0 to $0.0861 V^2_2 g_2$.

- As discussed earlier, this load case will treat $V_1$ and $V_2$ as independent parameters varying over their full ranges.

### 3.8.2 Goal Searching

In the output of this simulation, we will be searching for any combination of the independent parameters which can result in a condition in which neither of the fuses $F_1$ or $F_2$ blow. Thus, all the other combinations will lead to one of the fuses blowing (if both of the fuses can blow, then the one with the smaller time to blow will blow first). Thus, in the simulation we will search for points (in the independent parameter space) at which both of the following conditions are obeyed.

$$i_1 < I^2_{F_1} \quad \text{and} \quad i_2 < I^2_{F_2} \quad (3.64)$$
3.8.3 Output Of The Simulation

To illustrate the output of the simulation, we will plot the values of $g_1$ and $g_2$ for which none of the fuses blow. Observe that there will be two or more additional independent parameters (in the case considered above there are four $V_1$, $V_2$, $G_1$, and $P_2$) but we do not care about their actual values, only whether they lead to a case in which neither of the fuses blow. Any useful result cannot include a situation where these other independent parameters lie within their allowable range, our solution must apply for any allowable value. On the other hand, we can design or at least choose $g_1$ and $g_2$ such that they may obey the relation we want (in this case, at least one of the fuses blowing, or the complement of the condition that we are looking at). Since our point search in the $g_1$ and $g_2$ plane is for discrete points, we will get an output of the kind shown in Fig. 3.8. The "*" signs on the graph indicate the values of $g_1$ and $g_2$ at which there exist some $G_1$ and $P_2$ for which neither of the fuses will blow for at least one combination of $V_1$ and $V_2$. Thus, they represent values which we need to avoid. Fig. 3.9 and Fig. 3.10 shows the result plotted for $g_1$ on the x-axis and $g_2$ on the y-axis with values ranging from 0-15 for each conductance.

3.8.4 Simulation Code Example

The simulation code is present in Appendix C.
3.8.5 Simulation Results

We performed calculations as described above for all possible combinations of load types. For all values of $V_{\text{imin}} > 30V$, we do not get any values for $g_1$ and $g_2$ for which neither of the fuse blows. The graphs in Fig. 3.9 and Fig. 3.10 show the results of the simulation for $V_{\text{imin}} = 30V$.

3.9 Further Simulations

In this simulation, we used the values of the constant variables as given in Section 3.8. The choice of $V_1 = 30V$ has the relevance that this represents the lowermost value of the 42V bus voltage. With the values chosen for simulation right now, we could not achieve fuse blowing at $V_1 = 30V$. We can rerun the simulations for different values of the other parameters. In particular, we can start with a high value of $k_{\text{res}}$ and with $F_1 = F_2 = 1$ and keep on increasing $F_1$, $F_2$ until we first fail to achieve fusing. Then we can choose a different value of $k_{\text{res}}$ and repeat the same.

3.10 Conclusions

After the simulations run on these combinations of the fuse safety factors and $k_{\text{res}}$, we get the graph in Fig. 3.11, which shows choices of fuse safety factors and $k_{\text{res}}$ which meet our goal. Each square corresponds to a case for which fusing takes place at a minimum of $V_1 = 30V$ (and consequently not at $V_1 = 29V$). Similarly, the triangles correspond to 29V. This result clearly shows that we can arrive at a strategy for choosing the appropriate fuse safety factors and the ratio $k_{\text{res}}$ to ensure that for all possible combinations of the voltages and currents in the circuit, we will achieve fusing of at least one of the fuses. We can therefore activate a crowbar and achieve active response to a 42V-14V fault.

The beauty of this strategy is that it can do no harm. If following a fuse clearing, we actuate the corresponding crowbar, one of two results are obtained:

- If there is no 42V-14V fault, nothing happens.
- If there is a 42V-14V short, the action of the crowbar brings the circuit to a safe state.
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Note that we do not claim to have done an exhaustive search over all possible load states for all circuits. Combination loads (e.g. constant resistance and constant power elements on the same circuit) can certainly exist. It is possible that combination loads will present protection challenges less demanding than the "pure" or "extreme" loads considered here, but we offer no proof. And other load characteristics can exist. One example is a dc motor with a high inertia.

It is possible that in evaluating the design for any given automobile, other calculation methods may prove more efficient. If the vast majority of possible faults are constant-resistance-to-constant-resistance, they can be quickly dispatched, and the remaining possibilities may be explicitly evaluated pairwise in an exhaustive search. Some possible circuit pairs may be removed from consideration (if, for example, they share no common loads or cable sections).

We do expect that the basic elements of the analysis presented here will continue to be useful. And we believe that the general design method we illustrated will be nearly universally effective at reaching satisfactory final designs. In particular, we refer to selecting higher values for $k_{res}$. In practice, this is equivalent to selecting heavier wires in the wire harness. Heavier wires deliver more fault current, clearing fuses in more cases. In practice, the need for heavier wires may well be limited to one or a few problem circuits. The selection of one number ($k_{res}$) to apply to every circuit in the car is a computational convenience which probably should not be used in the practical case.
Active Circuit Modifications For The Dual Voltage System

Figure 3.9: Simulation Results For $V_{1\text{max}} = 48V$, $V_{2\text{max}} = 16V$, $V_1 = 30V$, $V_2 = 16V$, $F_1 = 1.5$, $F_2 = 1.5$
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Figure 3.10: Simulation Results For $V_{1\text{max}} = 48V$, $V_{2\text{max}} = 16V$, $V_1 = 30V$, $V_2 = 16V$, $F_1 = 1.5$, $F_2 = 1.5$ (cont.)

Figure 3.11: Lower Limits On The Choice For Fuse Safety Factors And $k_{res}$
4.1 Introduction

Dual-Voltage (e.g. 42V/14V) automobiles present the electrical system designer with challenges not found in today's cars. One such challenge is the design of a fault protection system to restore the electrical system to a safe state in the event of short circuits and/or faulted components. In conventional cars, simple fuses are the principal elements of the fault protection system. But in dual voltage automobiles, a new class of fault (the bus-to-bus or 42V – 14V fault) can occur. It has been shown that fuses alone cannot be used to protect against such an event. This thesis has shown some methods which can be implemented relatively simply to achieve a dual voltage system which always returns to a safe condition after a bus-to-bus fault.

4.2 Evaluation Of Thesis Objectives And Contributions

In chapter 1, we have shown that the fusing topologies currently in place cannot be relied upon to clear the bus-to-bus fault. Thus, left by itself, the bus-to-bus fault will not be able to clear both the fuses and bring the system to a stable state. This result has been known to the automobile industry for quite a while now. But, with the discussion in chapter 1, we have provided a mathematical footing to it. Chapter 1 also set the stage for further work in the form of modifications to the circuit.

In chapter 2, we worked upon passive circuit modifications to the dual voltage system. We came up with modifications in the form of Zener diodes, simple diode and a Positive Temperature Coefficient device. We have however, found that such modifications are either not robust enough to work on all operating conditions (Zener modification) or cannot be implemented with practical circuit elements (PTC modification). Hence, we concluded that simple passive element modification will not be able to bring the circuit to a safe operating condition. Thus, we were all set to work upon the next logical step which was incorporation
of active circuit elements and latching circuits to achieve the same result.

Chapter 3 worked on active circuit modifications to the dual voltage circuit. We simulated the circuit for all possible operating conditions in the form of the three main types of load that the electrical system of a car may have, and tested the latching circuit for its successful operation. Note that we do not claim to have done an exhaustive search over all possible load states for all circuits. Combination loads (e.g. constant resistance and constant power elements on the same circuit) can certainly exist. It is possible that combination loads will present protection challenges less demanding that the pure or extreme loads considered here, but we offer no proof. And other load characteristics can exist. However, we do expect that the basic elements of the analysis presented here will continue to be useful. And we believe that the general design method we illustrated will be nearly universally effective at reaching satisfactory final designs. These operating conditions included the types of load that an automobile can have, the possible switched state of these loads, the dc swing on the voltages of the voltage bus and certain transient voltage disturbances in the system. As a result of these simulations, we found out that within certain constraints, which are relatively practical, we can achieve fusing for both the fuses and bring the circuit to a safe state. We concluded the chapter by stating these constraints on the circuit which translate into design rules for the electrical system designer.

4.3 Future Work

The circuit modifications introduced in this thesis has been proven to work in all the operating conditions that the electrical system in a car maybe subject to. Comprehensive simulations support the above claim. However, the final test of the proposed modification would be in a real life environment where we build the system and test it on an actual dual-voltage automobile. We can also test it on a current 14V automobile augmented with a 42V wire harness. Recommended future work would include tests like this and verification of the suitability of the proposed modifications.
Appendix A

Appendix—Analyzing The Circuit With The PPTC Device

We had stated in Chapter 2 that a PTC device can be theorized to have certain properties and implemented into the circuit so that the fusing strategy works. Here, we will try to evaluate a practical part similar to the idealized device, namely a PPTC (Polymeric Positive temperature Coefficient) device, for its suitability in this application. Before we go into analyzing the circuit with the PPTC, we will state the design conditions for a PPTC.

A.1 Design Criteria For A PPTC

A PPTC has to follow all of these conditions to work properly

- The maximum voltage across a PPTC should not exceed $V_{max}$.
- The maximum current should not exceed $I_{max}$.
- The minimum current needed to trip a PPTC is called $I_{trip}$.
- In order to reset a PPTC from its tripped state, the voltage in the circuit should decrease such that the power dissipation in the PPTC goes below a design parameter $P_{trip}$.
- The ON state resistance of the PPTC may vary between $R_{min}$ and $R_{max}$. We will relax this condition and assume that the ON state resistance is a constant value $R$.

A.2 PPTC Model

From the above given conditions, we will be concentrating on the trip current $I_{trip}$, the trip power $P_{trip}$ and the ON state resistance $R$. To understand these conditions, we will model the PPTC as follows. Figure A.1 shows the resistance to temperature behavior of the PPTC. Thus, the resistance stays at a constant value so long as the temperature is below a specific value $T_{trip}$. This resistance is $R$. As the voltage applied on the PPTC rises,
the power dissipation rises till the temperature of the PPTC tends to go above $T_{trip}$. At this point the PPTC trips and the resistance rises to a value such that the temperature is maintained constant at $T_{trip}$. Thus, the PPTC now becomes a constant power device. Note that there is a voltage $V_{trip}$, which defines the trip point if the PPTC is connected to a voltage source. With this information, we can describe the voltage current characteristics of the PPTC as shown in Figure A.2. To bring the PPTC to its conducting state from the tripped state as given in its specification sheet, we need to reduce the power dissipated in it below a certain threshold. Lets call this power threshold as $P_{trip}$. This threshold is again defined by $I_{trip}$ and $V_{trip}$.
Appendix - Analyzing The Circuit With The PPTC Device

Figure A.3: Tripping Circuit For PPTC

A.3 Evaluating Conditions For The PPTC Design

In normal operation, our proposed circuit wants the PPTC device to stay in the high resistance state. The relevant circuit is shown in Figure A.3. Thus, we need the PPTC to "trip" to the high resistance state as soon as the circuit it turned on. The power dissipated in the PPTC is given by

\[ P = \frac{V^2}{R} \quad \text{for} \quad V \leq V_{\text{trip}} \quad (A.1) \]

where,
- \( V \)=applied voltage on the PPTC,
- \( R \)=conducting state resistance of the PPTC

The PPTC temperature of the PPTC is given by

\[ T = T_0 + \frac{P}{U} = T_0 + \frac{V^2}{UR} \quad (A.2) \]

where,
- \( U \)=temperature coefficient to power dissipation of the PPTC

At \( P = P_{\text{trip}} \), \( T = T_{\text{trip}} \). Thus,

\[ T_{\text{trip}} = T_0 + \frac{P_{\text{trip}}}{U} \quad (A.3) \]

Also, since power is defined in terms of the voltage, this point also specifies the trip voltage \( V_{\text{trip}} \). Therefore,

\[ T_{\text{trip}} = T_0 + \frac{V_{\text{trip}}^2}{UR} \quad (A.4) \]

We need to find the expression for \( V_{\text{trip}} \). The specification sheets define the tripping in terms of the current going above a given value \( I_{\text{trip}} \). Thus, \( I_{\text{trip}}V_{\text{trip}} = P_{\text{trip}} \). Therefore, from the specification sheets, we can find out \( V_{\text{trip}} \).

We need the PPTC in the high resistance state in the normal functioning of the circuit. This, means that the effective voltage applied to it should exceed \( V_{\text{trip}} \). To evaluate this
condition, we will derive a Thevenin equivalent for the circuit in the normal operation of
the PPTC. Figure A.4 shows the circuit and its Thevenin equivalent. The expressions for
the circuit parameters are:

\[ V_{TH} = \frac{V_1 g_1}{g_1 + G_1} \]  
(A.5)

\[ R_{TH} = \frac{R_e (g_1 + G_1) + 1}{g_1 + G_1} \]  
(A.6)

Thus, to trip the device, we need

\[ \frac{V_{TH} R}{R + R_{TH}} > V_{trip} \]  
(A.7)

Thus,

\[ \frac{V_1 g_1 R}{(g_1 + G_1)(R + R_e) + 1} > V_{trip} \]  
(A.8)

Which translates to

\[ R_e < \frac{V_1 R g_1 - V_{trip}}{V_{trip}(g_1 + G_1)} - R \]  
(A.9)

The other condition is the one pertaining to keeping the Zener turned off in the normal
operation of the 14V circuit. The relevant circuit is shown in Figure A.5. Observe that for
ascertaining the condition for the Zener to turn on, we need to check out the circuit without
the Zener and make sure that the voltage goes above the Zener breakdown voltage. The
Zener thus has been shown in dotted lines (to indicate its absence in the calculation) We
will again relax this condition by simply specifying \( V_Z > V_2 \). This translates into,

\[ \alpha > \frac{1}{3} \]  
(A.10)

where \( \alpha \) is the same as defined in Section 2.3.3. The second condition in Section 2.5.1 says
that the Zener should conduct in the event of a fault. The relevant circuit is shown in
Figure A.6. Thus, we need \( V_b > V_Z \) or,
Figure A.5: Normal Operation Of The 14V Circuit

Figure A.6: Circuit Without The Zener To Ascertain The Condition For Its Blowing
Appendix-Analyzing The Circuit With The PPTC Device

Figure A.7: Circuit In The Event Of The Fault

\[ \frac{V_1 g_1}{g_1 + G_L} > \alpha V_1 \]  \hspace{1cm} (A.11)

Simplifying,

\[ \alpha < \frac{g_1}{g_1 + G_L} \]  \hspace{1cm} (A.12)

Fuse F1 should blow according to the third condition. The relevant circuit is shown in Figure A.7. We therefore need,

\[ i_1 > I_{F1} \]  \hspace{1cm} (A.13)

\[ \frac{g_1 [V_1 (g_2 + G_L) - V_2 g_2]}{g_1 + g_2 + G_L} > \frac{V_1 g_1 G_1}{g_1 + G_1} \]  \hspace{1cm} (A.14)

Simplifying,

\[ g_2 [(1 - \alpha) (g_1 + G_1) - G_1] > g_1 (G_1 - G_L) \]  \hspace{1cm} (A.15)

With the same reasoning that was used in Section 2.3.3.3, we can say the the multiplicand to gZ will be a positive number. Or,

\[ \alpha < \frac{g_1}{g_1 + G_1} \]  \hspace{1cm} (A.16)

Working on the fourth condition, we need to keep the Zener off after Fuse F1 blows. We find that the condition developed in Eq. (A.10) will ensure us that the Zener will never conduct when connected to the 14V circuit. However, the other condition is that of the PPTC reverting to the conducting state. Before we do that, let us try to elaborate on the PPTC design rules we gave in Section A.1. For a circuit given in Figure A.8, the PPTC will go back to conducting state when the following condition is met.

\[ \frac{V^2}{4R_a} < P_{trip} \]  \hspace{1cm} (A.17)
To implement the same condition in our circuit, we need to do the following transformation to the Thevenin equivalent circuit as shown in Figure A.9. Now, we implement the turn off condition as follows,

\[ \frac{V_{TH}^2}{4R_{TH}} < P_{trip} \]  \hspace{1cm} (A.18)

This simplifies into,

\[ R_c > \frac{V_z^2 g_2^2 - 4P_{trip}(g_2 + G_L)}{4P_{trip}(g_2 + G_L)^2} \]  \hspace{1cm} (A.19)

Finally, after this we need Fuse F2 to blow. If we notice carefully, this condition of \( i_{z1} > I_{F2}^0 \) was the first bottleneck condition we found in Section 2.2 and resolved in Section 2.5.2 giving rise to the condition

\[ G_{cond} > G_{2\text{max}} \]  \hspace{1cm} (A.20)
A.4 Concluding The PPTC Modification Circuit

Collecting all the $R_e$ conditions (Eq. (A.9) and (A.19))

$$\frac{V_2^2 g_2^2 - 4P_{\text{trip}}(g_2 + G_L)}{4P_{\text{trip}}(g_2 + G_L)^2} < R_e < \frac{V_T R g_1 - V_{\text{trip}}}{V_T(g_1 + G_1) - R}$$  \hspace{1cm} (A.21)

Collecting all the $\alpha$ conditions i.e. Eq. (A.10),(A.12) and (A.16)

$$\frac{1}{3} < \alpha < \frac{g_1}{g_1 + G_1}, \frac{g_1}{g_1 + G_L}$$  \hspace{1cm} (A.22)

The $g_2$ condition Eq. (A.15)

$$g_2 > \frac{g_1(G_1 - G_L)}{[(1 - \alpha)(g_1 + G_1) - G_1]}$$  \hspace{1cm} (A.23)

And the condition

$$G_{P_{\text{cond}}} > G_{2_{\text{max}}}$$  \hspace{1cm} (A.24)

which is closely related to the $R_e$ conditions. These summarize the conditions needed for the proper operation of the fusing strategy. We use this condition (Eq. (A.24)) to pick up a value of $G_{P_{\text{cond}}}$. Since, $G_{2_{\text{max}}} = 3$ (as found in Eq.(1.4)), we choose a value for $G_{P_{\text{cond}}} = 4$ and use the conditions in Eq. (A.21) to find out the bounds on the design parameters of the PPTC. Since,

$$G_{P_{\text{cond}}} = \frac{1}{R_e + R} = 4$$  \hspace{1cm} (A.25)

For $R > 0$, we have,

$$R_e \leq \frac{1}{4}$$  \hspace{1cm} (A.26)

Thus,

$$\frac{V_2^2 g_2^2 - 4P_{\text{trip}}(g_2 + G_L)}{4P_{\text{trip}}(g_2 + G_L)^2} \leq \frac{1}{4}$$  \hspace{1cm} (A.27)

Leading to,

$$P_{\text{trip}} > \frac{V_2^2 g_2^2}{4(g_2 + G_L) + (g_2 + G_L)^2} \approx V_2^2 \approx 200W$$  \hspace{1cm} (A.28)

Which is a very high value for a typical PPTC. Higher side values go to about 35W. Thus, we presume that $P_{\text{trip}}$ would be close to about 200W and not more. Thus, $R_e \approx \frac{1}{4}$. Therefore, Eq. A.9 leads to the condition

$$\frac{V_T R g_1 - V_T}{V_T(g_1 + G_1)} > R + R_e$$  \hspace{1cm} (A.29)

or,

$$\frac{V_T R g_1 - V_T}{V_T(g_1 + G_1)} > \frac{1}{4}$$  \hspace{1cm} (A.30)
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Simplifying, we get,

\[ R > \frac{V_{\text{trip}}(1 + \frac{1}{4}(g_1 + G_1))}{V_1 g_1} \]  

(A.31)

Therefore, we can get an accurate idea of what values to choose for \( P_{\text{trip}} \) and \( R \) for the PPTC. Thus, we can design a PPTC keeping all these design criteria in mind and design a Zener keeping Eq. (A.22) in mind.

A.5 Problem With The PPTC

We have put forward a scheme of designing the PPTC which would work in the way we want it to. However, we need the PPTC to operate in the tripped state in the unaffected condition and to return to conducting state only in the event of the fault. But the present PPTC commercially available does not allow it to stay in a tripped state for such a long time. The present architecture only allows a tripped state time of 4 hours. Thus, the present strategy cannot be implemented with commercially available PPTC’s. However, were a PPTC with suitable specifications to be designed, we could apply it to the circuit and bring it to safety in the event of the 42V – 14V fault.

A.6 Conclusion

We see that the with the above modifications, we can make the circuit to work in the way we want it to. However, the only road block is the inability of the commercial PPTC to work in the tripped state for a adequately long time.
Appendix B

Appendix-Analyzing A Constant Power Load Driven By A Constant Voltage Source

We discuss the issues related to a constant power load and its behavior when driven by a constant voltage source such as the voltage bus in our model. The assumption made is that the constant power load has been designed for the given voltage source and the voltage source will be able to supply the required amount of power to the load. For a detailed discussion of a load design for a voltage source see Appendix C. For our discussion, the circuit considered is shown in Fig. B.1.

B.1 Circuit Analysis

We will start with the basic constant power relation

\[ IV = P \]  \hspace{1cm} (B.1)

where,
\[ I = \text{current flowing in the constant power load} \]

Figure B.1: Circuit Considered In The Analysis Of A Constant Power Load
Appendix-Analyzing A Constant Power Load Driven By A Constant Voltage Source

\begin{align*}
\text{V} &= \text{voltage across the constant power load} \\
\text{P} &= \text{power rating of the load} \\
\text{This translates into,} \\
(V_x - V)g_x V &= P \\
\text{(B.2)}
\end{align*}

This is a quadratic equation with two solutions as shown in Fig. B.2 which represents the load line analysis of the constant power load. We can see that there can be two solutions for the voltage across the load. However, a properly designed load will operate at the high voltage solution since the other solution drives a lot of current through the wire harness resulting in very high losses. Thus, the solution to the quadratic in Eq. (B.2) is

\begin{align*}
V &= \frac{V_x + \sqrt{V_x^2 - 4 \frac{P_x}{g_x}}}{2} \\
\text{(B.3)}
\end{align*}

And the current is

\begin{align*}
I &= \frac{g_x(V_x - \sqrt{V_x^2 - 4 \frac{P_x}{g_x}})}{2} \\
\text{(B.4)}
\end{align*}

Also note that the voltage source modelled this way cannot serve a power load with rating above $V_x^2 g_x/4$, because this leads to a complex solution to both the current and the voltage and implies that the load line and the source lines never intersect.
Appendix C

Appendix-Simulation Code

C.1 Code 1

This code is for the load cases $G_{42} - G_{14}$, $G_{42} - I_{14}$, $I_{42} - G_{14}$ and $I_{42} - I_{14}$

```matlab
function LoadCase=LoadCase(L1,L2);

Vlmax=48; V2max=16; V1=32; V2=16; F1=1.5; F2=1.5;

Ng1=20; Ng2=20; g1=linspace(0.001,30,Ng1);
g2=linspace(0.001,30,Ng2); NG1=20; NG2=20; NI1=20; NI2=20; NP1=20;
NP2=20; hold on; vgx_ratio=6;

for ig1=1:Ng1
    for ig2=1:Ng2
        Glmax=g1(ig1)/(vgx_ratio-1);
        I2max=V2max*g2(ig2)/(vgx_ratio);
        Gl=linspace(0.001,Glmax,NG1);
        I2=linspace(0.001,I2max,NI2);
        IFlo=Vlmax*gl(ig1)/(vgx_ratio);
        IF2o=V2max*g2(ig2)/(vgx_ratio);
        for iGl=1:NG1
            for iI2=1:NI2
                V=(V1-V)*gl(iGl)+V2-I2(iI2)/gl(iGl)+g2(iI2)+Gl(iGl));
                i1=(V1-V)*g1(ig1);
                i2=(V-V2)*g2(ig2);
                if abs(i1)<F1*IFlo & abs(i2)<F2*IF2o
                    plot(gl(iGl),g2(ig2),'
```
for ig1=1:Ng1
  for ig2=1:Ng2
    G2max=g2(ig2)/(vgx_ratio-1);
    I1max=V1max*g1(ig1)/(vgx_ratio);
    G2=linspace(0.001,G2max,NG2);
    I1=linspace(0.001,I1max,NI1);
    IF1o=V1max*g1(ig1)/(vgx_ratio);
    IF2o=V2max*g2(ig2)/(vgx_ratio);
    for iG2=1:NG2
      for iIl=1:NI1
        %V=solve('(V1-V)*g1(ig1)+(V2-V)*g2(ig2)=V*G2(iG2)+I1(iI1)', 'V')
        V=(g1(ig1)*V1+g2(ig2)*V2-I1(iI))/1(g1(ig1)+g2(ig2)+G2(iG2));
        i1=(V1-V)*g1(ig1);
        i2=(V2-V)*g2(ig2);
        if abs(i1)<F1*IF1o & abs(i2)<F2*IF2o
          plot(g1(ig1),g2(ig2),'g*');
        end
      end
    end
  end
end

for ig1=1:Ng1
  for ig2=1:Ng2
    I1max=V1max*g1(ig1)/(vgx_ratio);
    I2max=V2max*g2(ig2)/(vgx_ratio);
    I1=linspace(0.001,I1max,NI1);
    I2=linspace(0.001,I2max,NI2);
    IF1o=V1max*g1(ig1)/(vgx_ratio);
    IF2o=V2max*g2(ig2)/(vgx_ratio);
    for iI1=1:NI1
      for iI2=1:NI2
        %V=solve('(V1-V)*g1(ig1)+(V2-V)*g2(ig2)=V*I1(iI1)+I2(iI2)', 'V')
        V=(g1(ig1)*V1+g2(ig2)*V2-I1(iI1))/1(g1(ig1)+g2(ig2)+I1(iI1));
        i1=(V1-V)*g1(ig1);
        i2=(V2-V)*g2(ig2);
        if abs(i1)<F1*IF1o & abs(i2)<F2*IF2o
          plot(g1(ig1),g2(ig2),'g*');
        end
      end
    end
  end
end
%V=solve('\((V1-V)g1(ig1)+(V2-V)g2(ig2)=I1(iI1)+I2(iI2)\)', 'V')
V= (g1(ig1)V1+g2(ig2)V2-I1(iI1)-I2(iI2))/(g2(ig2)+g1(ig1));
i1=(V1-V)*g1(ig1);
i2=(V-V2)*g2(ig2);
if abs(i1)<F1*IFlo & abs(i2)<F2*IF2o
  plot(gl(ig1),g2(ig2),'g*');
end
end
end
end

%%%%%
42 G 14 G

for ig1=1:Ngl
  for ig2=1:Ng2
    G1max=g1(ig1)/(vgx_ratio-1);
    G2max=g2(ig2)/(vgx_ratio-1);
    G1=linspace(0.001,G1max,NG1);
    G2=linspace(0.001,G2max,NG2);
    IFlo=V1max*gl(ig1)/(vgx_ratio);
    IF2o=V2max*g2(ig2)/(vgx_ratio);
    for iG1=1:NG1
      for iG2=1:NG2
        %V=solve('\((V1-V)g1(ig1)+(V2-V)g2(ig2)=V*G1(iG1)+V*G2(iG2)\)', 'V')
        V= (g1(ig1)V1+g2(ig2)V2)/(g1(ig1)+g2(ig2)+G1(iG1)+G2(iG2));
        i1=(V1-V)*g1(ig1);
        i2=(V-V2)*g2(ig2);
        if abs(i1)<F1*IFlo & abs(i2)<F2*IF2o
          plot(gl(ig1),g2(ig2),'g*');
        end
      end
    end
  end
end
C.2 Code 2

The next code is for the other load cases viz. $I_{42} - P_{14}, G_{42} - P_{14}, P_{42} - G_{14}, P_{42} - I_{14}$ and $P_{42} - P_{14}$

function LoadCase_2=LoadCase_2(L1,L2);

V1max=48; V2max=16; V1min=32; V2min=9; F1=1.5; F2=1.5;

Ng1=15; Ng2=15; NV1=10; NV2=10; V1=linspace(V1min,V1max,NV1);
V2=linspace(V2min,V2max,NV2); g1=linspace(0.001,15,Ng1);
g2=linspace(0.001,15,Ng2); NG1=10; NG2=10; NI1=10; NI2=10; NP1=10;
NP2=10; hold on; sym V; vg_ratio=8;

for iV1=1:NV1
  for iV2=1:NV2
    for ig1=1:Ng1
      for ig2=1:Ng2
        G2max=g2(ig2)/(vg_ratio-1);
P1max=V1max^2*g1(ig1)*(1-(vg_ratio-2)^2/(vg_ratio)^2)/4;
        G2=linspace(0.001,G2max,NG2);
P1=linspace(0.001,P1max,NI1);
        IF1o=V1max*g1(ig1)/(vg_ratio);
        IF2o=V2max*g2(ig2)/(vg_ratio);
        for iG2=1:NG2
          for iP1=1:NI1
            V=solve('(V1(iV1)-V)*g1(ig1)+(V2(iV2)-V)*g2(ig2)=V*G2(iG2)
              +P1(iP1)*V','V')
            V=1/2/(g1(ig1)+g2(ig2)+G2(iG2))*g1(ig1)*V1(iV1)+g2(ig2)*V2(iV2)
              +V1(iV2)^2*V1(iV1)^2+2*V1(iV1)*V2(iV2)^2+2*V2(iV2)
              +4*P1(iP1)*g1(ig1)-4*P1(iP1)*G2(iG2)^2/(1/2));
i1=(V1(iV1)-V)*g1(ig1);
i2=(V-V2(iV2))*g2(ig2);
            if abs(i1)<F1*IF1o & abs(i2)<F2*IF2o
              plot(g1(ig1),g2(ig2),'g*'); xlabel('g1');
              ylabell('g2');
            end
          end
        end
      end
    end
  end
end

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for iV1=1:NV1
    for iV2=1:NV2
        for ig1=1:Ngl
            for ig2=1:Ng2
                I2max=V2max*g2(ig2)/(vgx_ratio);
                Plmax=V1max^2*g1(ig1)*(1-(vgx_ratio-2)^2/(vgx_ratio)^2)/4;
                I2=linspace(0.001,I2max,NI2);
                Pl=linspace(0.001,Plmax,NP1);
                IF1o=V1max*gl(igl)/(vgx_ratio);
                IF2o=V2max*g2(ig2)/(vgx_ratio);
                for iI2=1:NI2
                    for iPl=1:NP1
                        V=solve(' (V1(iV1)-V)*gl(igl)+(V2(iV2)-V)*g2(ig2)=I2(iI2)
                \%+P1(iP1)\%/V','V')
                        V=1/2/(g2(ig2)+gl(igl))*(g1(ig1)*V1(iV1)+g2(ig2)*V2(iV2)
                        -I2(iI2)+g1(ig1)^2+V1(iV1)^2+2*g1(ig1)*V1(iV1)*g2(ig2)
                        *V2(iV2)^2-2*g1(ig1)*V1(iV1)*I2(iI2)+g2(ig2)^2*V2(iV2)^2
                        -I2(iI2)+g2(ig2)*V2(iV2)+I2(iI2)^2-4*I2(iI2)-4*P1(iP1)*g2(ig2)
                        -4*P1(iP1)*g2(ig2)^(1/2));
                        il=(V1(iV1)-V)*gl(igl);
                        i2=(V-V2(iV2))*g2(ig2);
                        if abs(il)<F1*IF1o & abs(i2)<F2*IF2o
                            plot(g1(ig1),g2(ig2),'g*'); xlabel('g1');
                            ylabel('g2');
                        end
                    end
                end
            end
        end
    end
end
Appendix-Simulation Code

P2max=V2max^2*g2(ig2)*(1-(vgx_ratio-2)^2/(vgx_ratio)^2)/4;
P1=linspace(0.001,P1max,NP1);
P2=linspace(0.001,P2max,NP2);
IF1o=V1max*g1(ig1)/(vgx_ratio);
IF2o=V2max*g2(ig2)/(vgx_ratio);
for iP1=1:NP1
  for iP2=1:NP2
    %V=solve('(Vl(iVl)-V)*g1(ig1)+(V2(iV2)-V)*g2(ig2)=P1(iP1)/V'
    %'+P2(iP2)/V', 'V')
    V=1/2/(g2(ig2)+g1(ig1))*(g1(ig1)*Vl(iVl)+g2(ig2)*V2(iV2)+
    +(g1(ig1)^2*Vl(iVl)^2+2*g1(ig1)*Vl(iVl)*g2(ig2)*V2(iV2)+
    +g2(ig2)^2*V2(iV2)^2-2*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1))^(-1/2));
    il=(Vl(iVl)-V)*g1(ig1);
    i2=(V-V2(iV2))*g2(ig2);
    if abs(il)<Fl*IFlo & abs(i2)<F2*IF2o
      plot(g1(ig1),g2(ig2),'g*'); xlabel('g1');
      ylabel('g2');
    end
  end
end
end

for iVl=i:NV1
  for iV2=l:NV2
    for igl=l:Ngl
      for ig2=l:Ng2
        Glmax=g1(ig1)/(vgx_ratio-1);
P2max=V2max^2*g2(ig2)*(1-(vgx_ratio-2)^2/(vgx_ratio)^2)/4;
P1=linspace(0.001,G1max,NG1);
P2=linspace(0.001,P2max,NG2);
IF1o=V1max*g1(ig1)/(vgx_ratio);
IF2o=V2max*g2(ig2)/(vgx_ratio);
for iG1=1:NG1
  for iP2=1:NP2
    %V=solve('(V1(iV1)-V)*g1(ig1)+(V2(iV2)-V)*g2(ig2)=P1(iP1)/V'
    %'+P2(iP2)/V', 'V')
    V=1/2/(g2(ig2)+g1(ig1))/G1max*(g1(ig1)*Vl(iVl)+g2(ig2)*V2(iV2)+
    +(g1(ig1)^2*Vl(iVl)^2+2*g1(ig1)*Vl(iVl)*g2(ig2)*V2(iV2)+
    +g2(ig2)^2*V2(iV2)^2-2*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1))^(-1/2));
    il=(Vl(iVl)-V)*g1(ig1);
    i2=(V-V2(iV2))*g2(ig2);
    if abs(il)<Fl*IFlo & abs(i2)<F2*IF2o
      plot(g1(ig1),g2(ig2),'g*'); xlabel('g1');
      ylabel('g2');
    end
  end
end
end
end
end

%%%%%%%%%%%%%%%%% 42 G 14 P
for iV1=1:NV1
  for iV2=1:NV2
    for ig1=1:Ng1
      for ig2=1:Ng2
        Glmax=g1(ig1)/(vgx_ratio-1);
P2max=V2max^2*g2(ig2)*(1-(vgx_ratio-2)^2/(vgx_ratio)^2)/4;
P1=linspace(0.001,G1max,NG1);
P2=linspace(0.001,P2max,NG2);
IF1o=V1max*g1(ig1)/(vgx_ratio);
IF2o=V2max*g2(ig2)/(vgx_ratio);
for iG1=1:NG1
  for iP2=1:NP2
    %V=solve('(V1(iV1)-V)*g1(ig1)+(V2(iV2)-V)*g2(ig2)=P1(iP1)/V'
    %'+P2(iP2)/V', 'V')
    V=1/2/(g2(ig2)+g1(ig1))/G1max*(g1(ig1)*Vl(iVl)+g2(ig2)*V2(iV2)+
    +(g1(ig1)^2*Vl(iVl)^2+2*g1(ig1)*Vl(iVl)*g2(ig2)*V2(iV2)+
    +g2(ig2)^2*V2(iV2)^2-2*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1)-4*P1(iP1)*g1(ig1))^(-1/2));
    il=(Vl(iVl)-V)*g1(ig1);
    i2=(V-V2(iV2))*g2(ig2);
    if abs(il)<Fl*IFlo & abs(i2)<F2*IF2o
      plot(g1(ig1),g2(ig2),'g*'); xlabel('g1');
      ylabel('g2');
    end
  end
end
end
end
end
end
end
end
end
end
end
end

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Appendix - Simulation Code

V2(iV2) + g2(ig2) - 2*V2(iV2) - 2 - 4*P2(iP2) - g1(ig1) - 4*P2(iP2)...
* g2(ig2) - 4*P2(iP2) - g1(ig1))^(1/2));

i1 = (V1(iV1) - V) * g1(ig1);

i2 = (V - V2(iV2)) * g2(ig2);

if abs(i1) < F1*IF1o & abs(i2) < F2*IF2o
    plot(g1(ig1), g2(ig2), 'g*');
end

end

end

end

%%%

for iV1 = 1:NV1
    for iV2 = 1:NV2
        for ig1 = 1:Ngl
            for ig2 = 1:Ng2
                Ilmax = Vlmax * g1(igl) / (vgx_ratio);
                P2max = V2max^2 * g2(ig2) * (1 - (vgx_ratio - 2)^2 / (vgx_ratio)^2)) / 4;
                I1 = linspace(0.001, Ilmax, NI1);
                P2 = linspace(0.001, P2max, NP2);
                IF1o = Vlmax * g1(igl) / (vgx_ratio);
                IF2o = V2max * g2(ig2) / (vgx_ratio);
                for iIl = 1:NI1
                    for iP2 = 1:NP2
                        % V = solve('(V1(iV1) - V) * g1(ig1) + (V2(iV2) - V) * g2(ig2) = I1(iI1)
                        % + P2(iP2) / V', 'V')
                        V = 1/2 / (g2(ig2) + g1(igl)) * (g1(ig1) * V1(iV1) + g2(ig2)...
                            + V2(iV2) - I1(iI1) + g1(ig1) * 2*V1(iV1) + 2 + g1(ig1) * V1(iV1)...
                            + g2(ig2) * V2(iV2) - 2 * g1(igl) * V1(iV1) * I1(iI1) + g2(ig2) * 2...
                            + V2(iV2) - 2 * g2(ig2) * V2(iV2) * I1(iI1) + I1(iI1) * 2 - 4 * P2(iP2) * g2(ig2)...
                            + 4 * P2(iP2) * g1(igl))^(1/2);
                        i1 = (V1(iV1) - V) * g1(ig1);
                        i2 = (V - V2(iV2)) * g2(ig2);
                        if abs(i1) < F1*IF1o & abs(i2) < F2*IF2o
                            plot(g1(ig1), g2(ig2), 'g*');
                        end
                    end
                end
            end
        end
    end
end

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end
end
