Abstract
Clock buffers constitute a major source of power dissipation in VLSI circuits. In CMOS the load is primarily capacitive and hence an inductive shunt can reduce real power needs. This almost-adiabatic topology is referred to as a resonant buffer. Two resonant buffers can be actively controlled by additional variable capacitance, to deliver quadrature signals from a single incoming clock. The cost of this quadrature generation is added complexity of control algorithm and the advantage is 85% less power than alternate methods. This topology is used to create quadrature signals and drive the clock inputs of a bang-bang half-rate phase detector in a 10GBit/sec Clock and Data Recovery Circuit. The 0.13um CMOS implementation shows significant power savings. A useful closed form expression for jitter transfer characteristic of generic linear-time-invariant filters is derived and applied to the proposed buffer to show it can be transparently integrated in existing CDR architectures. The work for this thesis was conducted in part at Analog Devices Inc.
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Chapter 1

Introduction

1.1 Summary

Clock network buffers constitute one of the major sources of power dissipation in VLSI circuits. There are many techniques commonly used to mitigate this problem. In resonant buffers, an inductive load is added in parallel with the original capacitive load to increase the output voltage swing without the need for additional current driving ability on the part of the buffer. Unfortunately the intrinsic narrow-band nature of these circuits, limits their applicability when phase accuracy is of extreme importance. Such attention to phase considerations is typical of phase/frequency locked loops used in fiber optic Clock and Data Recovery (CDR) systems.

In this document, I look at a subset of resonant buffers used to control quadrature clock networks. In particular, I present a closed loop technique that allows a pair of resonant buffers to generate quadrature signals from a common input, eliminating the need to generate these signals with an additional circuit and, therefore, further reducing overall power consumption. This technique could also be used to minimize the quadrature error between two existing quadrature clocks.
1.2 Background

In this section I give some background information about the problem analyzed in my research. In particular I look at the relevance of this research in the context of CMOS Clock and Data Recovery (CDR) systems for Fiber Optic applications.

Analog Devices Inc. (ADI) is currently working on the development of a new transceiver system for 10 Gb/s fiber optic transceiver applications. The circuits are being designed for fabrication on the 0.13μm CMOS process\textsuperscript{1} owned by Taiwan Semiconductor Manufacturing Company (TSMC). The CDR at the core of the transceiver is based on a phase/frequency locked loop topology originally proposed by [4] and [10], and further evolved by Dr. Jack Kenney and Lawrence De Vito (both of Analog Devices).

Power consumption is a very important design consideration in VLSI circuits such as CDRs, mainly due to the need for increased component density on telecommunication equipment racks. Clock network buffers are one source of large power dissipation because of the large capacitive loads that they are usually required to drive and their unity activity factor.

In this particular application most of the critical path circuitry is designed in current mode logic (CML) [16]. An example of a common CML cell is shown in figure 1-1. This topology takes advantage of a differential structure, able to steer the tail current between the complementary outputs. In a typical CML buffer, clock rate requirements limit the size of the resistive load. A large enough tail current must be then set to meet output voltage swing specifications. This means that power dissipation in the buffer increases approximately linearly with the size of the capacitive load.

The need for power can be somewhat reduced with the use of inductive loads in

\textsuperscript{1} Other process options include: Low-voltage thin Fluorinated Silica Glass (silicon dioxide), 1.0V (RF) and 3.3V transistors, 1 polysilicon layer, 8 copper interconnect layers, standard top metal layer.
the buffer that can resonate with the capacitive load at a frequency close to that of the clock. In the resulting configuration, usually referred to as a resonant buffer, the tradeoff between load impedance and clock rate is broken and one can significantly reduce the total power dissipation of the CML buffer.

In this work I look a particular set of such resonant buffers used to control the CDR’s 10 Gb/s half-rate bang-bang (HRBB) phase-detector quadrature clock network. The resonant quadrature buffer topology is shown in in figure 1-2. Closed loop controls (not shown in the picture) alter the center frequencies of the resonating structures (tanks) such that the output clock signals have a relative phase of 90 degrees.

The need for a quadrature clock can be explained as follows: in a HRBB phase detector, all edges of one of the clock phases are used to align the absolute clock phase to that of the incoming data (see figure 1-3). At the same time, the edges of the other clock phase can be used to trigger data sampling. In order to reduce the error rate of the CDR to a minimum, it is best for the two clocks to be exactly in
quadrature (i.e. 90 degrees out of phase), so that data sampling occurs in the middle of the data eye.

Interestingly, this structure can also be driven with two clock phases already in quadrature without requiring any design changes. In that case, the closed-loop control acts to reduce any quadrature error\(^2\) present in the incoming signals. This is possible because the dynamic range of the control has to be much larger in the case of the buffer generating quadrature clocks versus the buffer correcting quadrature of existing clocks.

It should be noted that the resonant buffer cannot be operated without the presence of closed loop control because any mismatch present between the tanks of the two buffers can lead to significant quadrature error static phase error of the main CDR control loop. To this effect, later in this document, it is shown that the resonant buffer can be a significant source of quadrature error when operated in an open-loop configuration and driven by two clocks in quadrature.

The goal of the author’s research has been to establish the feasibility of the reso-

\(^2\)Quadrature error is defined as the difference between the relative phase of the two clock signals and 90 degrees. That is, if the clocks are in exact quadrature the error should be zero.
Figure 1-3: Typical input signals of a half-rate bang-bang phase detector. Both rising and falling edges are used, so the clock frequency is half of the data rate.

nant buffer topology and to propose a control system that can successfully accomplish the goal of generating two clocks output in quadrature. The design is based on some original and some modified pre-existing circuits. Furthermore, data is presented showing how the use of this buffer topology can reduce power consumption in the case of the CDR topology currently in design at Analog Devices.

1.3 Previous work

The idea of resonating parasitic capacitive loads with the deliberate introduction of shunt inductances to extend clock rate and reduce power consumption, is a very old concept present in a remarkable number of circuit designs.

A recent example of low-power rail drivers uses harmonic decomposition and multiple resonant structures to build arbitrary waveforms on a network (signal frequencies of 10 MHz) [13]. [2] analyzes in detail the topic of resonant structures driving clock networks in low-power applications. Of particular relevance is the almost non-overlapping resonant clock driver, as a first step in multi phase resonant drivers [3].

Related to this topic, is the use of standing wave structures to distribute signals over very wide clock arrays in the context of large digital chips [14]. Also useful is
another analysis of resonant structures’ importance in very high frequency CMOS RF integrated circuits [12].

Unfortunately, the author was not able to find any evidence of use of closed-loop control techniques to enable generation of quadrature clock signals at frequencies in the order of tens of GHz.
Chapter 2

The Resonant Buffer

In this chapter we look at the general structure of the resonant buffer. While hinting at the design of its control, we focus on the signal-path circuitry. We provide some background on the function and behavior of resonant buffers with an eye to the practical implications of their use in a CDR system.

2.1 Buffer Signal Path

Figure 1-2 shows a schematic view of a single CML quadrature clock network. The source-coupled pair which constitutes the core of the CML buffer can be simply viewed as a current steering element, able to redirect the tail current in different proportions to the two complementary outputs. Two identical buffers are connected to the same input clock signal. Because of the high clock frequency (5GHz), the input clock signals are most likely approximated by a sinusoidal signal with a differential amplitude (peak to peak) of 0.8V. The output clock signal is expected to have similar voltage characteristics.

The current steering element of the CML buffer is loaded with a similar resonant structure (tank) on each of the outputs. Four tanks are needed in a quadrature CML
buffer\textsuperscript{1}. In particular, the total impedance of the tank will determine the output voltage waveform. Here follows a list of the major components of the tank impedance (drawn in figure 2-1).

![Figure 2-1: Complete and simplified model for the resonant load (tank).](image)

- **Parasitic Capacitive Load.** This load is constituted mainly by interconnect capacitance and gate capacitance of the driven phase detector. Although this is a complex distributed structure, we will approximate it with a lumped capacitor $C$ to ground and an unknown series resistor $R_C$ (to provide a finite impedance at high frequencies – i.e. to limit the quality). A recent estimate \cite{8} claims the total parasitic load is approximately $0.5pF$. Process variations and different biasing conditions can substantially alter this value. All circuit simulations take care of this fact by looking at different process and temperature corners.

- **Output Impedance of the Current Steering Element.** This depends greatly on the current steering circuit topology. One can assume that the resistive component of the output impedance ($R_O$) will be made high enough not to have a significant effect on the total impedance of the tank (e.g. with the use of a cascode configuration). Similarly, the capacitive component ($C_O$) can be

\textsuperscript{1}One could also imagine a buffer which uses only two tanks, placed between the complementary outputs of each buffer. Since this is a fundamentally equivalent representation of the buffer, only the case of four tanks is analyzed.
considered insignificant compared to the parasitic capacitive load. The NMOS transistors used in the CML current steering circuit have very low drain capacitance and the limited voltage gain of the buffer makes the Miller effect almost irrelevant.

- **Additional Capacitance.** In order to have a control handle on the tuning of the tank, additional capacitance \(C_{\text{extra}}\) in parallel with the parasitic load is introduced. The extra capacitance comes in the form of Metal-Insulator-Metal capacitors (MIMCAPs) and MOS varactors, which are common structures in the TSMC 0.13\(\mu\)m process used by ADI. Since this capacitive load is at the core of the control strategy of the resonant buffer, a complete discussion of the specific implementation of this extra capacitance is provided, along with the description of the control architecture.

- **Lumped Inductor to the Power Supply.** The inductor is built in the metal 8 layer. This is the main design handle of the resonant structure. The value of the inductor is chosen such that the resonant frequency is that of the clock when the extra capacitive elements are controlled to provide an effective load half-way between their minimum and maximum. If \(\frac{w_c}{2\pi}\) is the clock frequency then

\[
L \approx \frac{1}{(C + C_{\text{extra}}) w_c^2}.
\]

The equivalent series resistance of the inductor \(R_L\) is subject to some constraints and tradeoffs. In order to significantly improve the power efficiency of the buffer, the tank quality factor should be higher than unity. At the same time, to reduce possible tank impedance phase sensitivity on mismatches between buffers, one would like the overall quality factor of the tank to be low. Finally, to avoid duty cycle distortion problems, the low frequency tank impedance should be kept at a minimum.
All these concerns can be addressed by designing a relatively high Q (≈ 10) inductor.

As figure 2-1 suggests, the resonant load is quite complicated to handle in hand calculations. An equivalent parallel tank model can be used, since this analysis is concerned only with operation in a small frequency band around the clock frequency. In the case of the parallel tank, the total load impedance seen by the current steering circuit is:

\[ Z_{\text{load}} = \frac{sLR_p}{s^2LC_{\text{TOT}}R_p + sL + R_p}. \]  

This is a canonical second order system with a natural frequency of \( w_n = \sqrt{\frac{1}{LC_{\text{TOT}}}} \) and a damping factor \( \xi = \sqrt{\frac{L}{C_{\text{TOT}}}} \frac{1}{2R_p} \). Figure 2-2 shows a plot of the impedance of the actual resonating structure and that of the equivalent parallel tank for a typical set of design values: \( C_{\text{TOT}} \approx 0.72 \text{pF}, L \approx 1.3 \text{nH} \) and a total tank Q of 4.5. One can see that near the resonance frequency of the tank (≈ 5 GHz) the approximation holds very well.

### 2.1.1 Effects of the Buffer Capacitance Control

Since we plan to control the tank behavior through changes in tank capacitance, it is important to model the static and the dynamic effects of this process.

In a static sense, we can perform a linear expansion of the tank impedance phase variation around the resonance frequency as a function of the capacitance \( C_{\text{TOT}} \).

Although the operation is quite complex (see appendix A.1), the result is simple:

\[ \angle Z_{\text{tank}}|_{w=w_n} \approx -\frac{Q}{C_{\text{TOT}}} \Delta C, \]  

where the angle is expressed in radians. This means that the phase of the tank impedance is proportional to the Q of the tank and to the additional capacitance (\( \Delta C \)) and is inversely proportional to the total nominal capacitance (\( C_{\text{TOT}} \)).
result changes slightly, in a small signal sense, if we operate the buffer off the resonant frequency, providing the outgoing clock signal with a significant carrier phase contribution. Nevertheless, the general relationship between phase of tank impedance and Q remains unchanged.

It is also very interesting to discuss the dynamic behavior of the phase of tank impedance as a function of changes in capacitance. When capacitance is added or subtracted from the tank, a particular solution will appear in the system (see appendix

\[ To provide output in quadrature, one buffer should contribute +45 degrees of phase to its output, while the other contributes −45 degree of phase.\]
A.2). This solution will decay as a first order system with time constant

\[ \tau_{\omega} = \frac{2Q}{w_n}. \] (2.4)

2.1.2 Transmission of Phase Modulation Information

The clock signal delivered to the resonant buffer contains phase information (in the form of phase modulation of the clock carrier) fundamental to the operation of the phase/frequency locked loop of the CDR. The effects of the resonant buffer on the phase modulation of the clock are analyzed in detail in chapter 3. We show how the resonant buffer can be safely used in the current design of the CDR architecture. As a by-product of this analysis, we present a complete mathematical framework that allows to look at the effects of any generic LTI filters to narrow-band phase-modulated signals.

2.2 Background: Open-Loop Resonant Buffer

Historically, the signal path for the resonant driver was first designed by Bharath Reddy of Analog Devices. The original application differed significantly from the work presented here in a number of ways.

- A couple of buffers are driven by two clock signals in quadrature created from a single phase with the use of a polyphase filter.

- The only closed-loop control at run-time is an Automatic Gain Control (AGC) unit that changes the tail current of each buffer to maintain a constant output voltage swing of 0.8V (differential).

- The two resonant buffers rely simply on process symmetry to ensure that equal phase contribution are given to the two input clock carrier signals.
• At startup, a helper circuit tests the sum of the tail currents of the two CML buffers and selects additional capacitance to be added to the four tanks. The additional capacitance comes in the form of identical MIMCAPs (one for each of the four tanks) added to the tanks from a library of many possible values. The helper circuit chooses the MIMCAP value (the same for all four tanks) that minimizes power consumption.

• The goal for the circuit was to replace a pair of traditional CML drivers, therefore reducing overall power consumption.

Under these considerations the author was asked to calculate how much such a circuit would contribute to the overall static quadrature error of the signal delivered to the HRBB phase-detector. This would determine whether a closed-loop phase control system for the two resonant buffers was needed. The results of this work are presented in Appendix B. As the analysis shows, the buffer, in its original application, could have contributed a significant amount of static quadrature error and therefore, closed-loop control was needed. Furthermore, the idea of using the resonant buffer to create quadrature signals proved to be capable of further reducing system power consumption\(^3\). It is in light of these considerations that a closed-loop control was proposed.

### 2.2.1 Relative Power Efficiency between Operation Modes

As we just mentioned, the two CML buffers in the system can be operated to contribute only a small phase shift to the incoming clock carrier, or instead, to contribute a larger phase shift (around ± 45 degrees) when generating quadrature from a single phase of the incoming clock.

These two operation modes correspond respectively to tuning the buffers’ center frequency to the clock frequency and to tuning the buffers so that the clock frequency

\(^3\)Evidence for overall power reduction of the system is presented later in this document.
coincides with the $-3 \, dB$ point of the resonant loads magnitude response (see figure 2-2).

If the CML buffers are to provide a constant output clock magnitude, the tail currents of the buffers will be approximately $\sqrt{2}$ larger when operating to generate quadrature than when simply offering small phase corrections to two existing phases of the incoming clock.

Furthermore, it should be mentioned that if the relative phase contributions of the buffers has to be 90 degrees (when generating quadrature), then the most efficient way to operate the overall system is for each of the two buffers to provide an equal but opposite phase contribution (one buffer $+45$ and the other $-45$ degrees). If this configuration is not possible (see section 4.3), then power performance is degraded. Nevertheless, simulations show that for small offsets, the penalty is minor. For instance operating the two buffers so that one contributes $+30$ and the other $-60$ degrees increases power consumption by only 3.5%, compared to the optimum.

### 2.3 Circuits

In this section, we look at the circuits that constitute the signal path of the resonant buffer. Discussion of the closed-loop control to ensure quadrature generation is left for chapter 4. In this section, we also mention the Automatic Gain Control (AGC) system wrapped around each CML resonant buffer.

#### 2.3.1 Current steering

Figure 2-4 shows the general topology of a single CML buffer. Two of these buffers are used in the overall system, one for each of the output clock phases to be generated. The design is based on an original project by Bharath Reddy of Analog Devices.

The input signal is delivered differentially to the buffer by $\text{inp}$ and $\text{inn}$. The
buffer provides two signal outputs: `outp` and `outn` to be delivered to the HRBB phase detector; `peakp` and `peakn` to be used by the peak detector of the AGC loop. Reference current busses (`ib1` and `ib2`) are provided by the biasing tree of the CDR chip. The circuit is powered from the 1.8 V chip supply network (`vddbb`). Node `tune` is the control handle of the AGC loop.

Node `ito` is used by the closed-loop control circuitry to obtain a relative measure of the buffer tail current\footnote{As described later in chapter 4, we are only interested in detecting the condition for minimum power consumption.}

### 2.3.2 Additional capacitive loads

As shown in figure 2-1, the capacitive component of the tank comes, in large part, from the combination of parasitic loads and additional capacitive loads which are used to modify the buffer phase contribution to the carrier. The structure of the additional capacitive loads is shown in figures 2-5, 2-6 and 2-7.

**MIMCAP cells**

16 switchable MIMCAP\footnote{MIMCAP stands for Metal-Insulator-Metal capacitor.} cells are controlled by a 4-bit logic bus (`capsel<>`). On the CDR chip, the logic supply voltage is of 1.0 V. The equivalent nominal capacitance for one cell between nodes `t` and `b` is shown in the table 2.1.

<table>
<thead>
<tr>
<th><code>sel</code></th>
<th>Equiv. C</th>
<th>ESR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 V</td>
<td>38 fF</td>
<td>37 Ω</td>
</tr>
<tr>
<td>0.0 V</td>
<td>8.6 fF</td>
<td>116 Ω</td>
</tr>
</tbody>
</table>

Table 2.1: Nominal characteristics of a single MIMCAP cell (test performed with a 5 GHz, 0.8 V<sub>pk-pk</sub> differential signal).
MOS varactor cells

Three varactor cells are controlled with a bus of three analog voltages ($v_{cntr1}$). The control voltages are used to bias a couple of back-to-back P-well MOS varactors, built using the deep N-well mask available in this process. Figure 2-3 shows the nominal capacitance for one cell between nodes A and B versus the control voltage.

Figure 2-3: Nominal characteristics of a single varactor cell (test performed with a 5GHz, 0.8 $V_{pk-pk}$ differential signal).

The dynamic range of the varactor is 38.0 ± 13.5 fF and is centered for a control voltage of 0.9 V. The transfer function between control voltage and equivalent capacitance has a maximum of 42 fF/V around the center of the dynamic range and a minimum of 11 fF/V. The varactor cell takes advantage of the 3.3 V supply
provided on the CDR chip in order to obtain a higher tuning range. A set of voltage clamps is needed to ensure that the control voltage is kept between 0.4 V and 1.5 V. This avoids saturating transistors or exceeding breakdown voltages for the process.

### 2.3.3 Shunt Inductor

The position of the shunt inductor in the CML driver is shown in figure 2-4. The implementation uses a spiral of Metal 8. Layout and equivalent circuit model are shown in figure 2-8. The design was obtained, upon request, from Dr. Check Lee of Analog Devices, who used a method of moments analysis tools to derive an accurate circuit model.

The overall inductance of the element is approximately 700 nH. At ambient temperature, the equivalent series resistance at 5 GHz is 1.9 Ω for an overall inductor quality factor (Q) of 11.5. At 130 °C, the equivalent series resistance increases by approx. 30%.

### 2.3.4 Automatic Gain Control Loop

As already discussed, the buffer is loaded with a resonant structure whose impedance magnitude is extremely sensitive to a number of factors. In particular, the resonant buffer phase transfer is meant to be controlled by adjustments of its capacitive load. This, in turn, can result in wide variations in the peak-to-peak magnitude of the buffer output signal.

In order to assure an approximatively constant output signal magnitude, each CML current steering element is wrapped in an Automatic Gain Control loop as shown in figure 2-9. A copy of the CML buffer output signal is fed to a differential peak detector. The peak detector output is compared by means of a differential amplifier with a reference voltage (800mV_{pk,pk}) and the resulting error signal is used to control the tail current of the CML buffer (see figure 2-4, transistor mn11).
The peak detector was designed initially by Bharath Reddy of Analog Devices and it is not shown here. The control loop, from buffer output amplitude to buffer tail current, is stabilized with the use of a miller-multiplied capacitor within the peak-detector. This dominant pole sets the unity gain frequency of the loop in the vicinity of 20 MHz with a phase margin of more than 60 degrees. It should be mentioned that the exact behavior of the loop is hard to model without taking into consideration the varying nature of the tank characteristics. Several simulations, under all process and temperature corners and under all configuration of the buffer additional capacitive load, are necessary to ensure a robust design.
Figure 2-4: Current steering circuitry of the CML buffer along with the shunt inductor and the extra capacitive loads.
Figure 2-5: Extra capacitive loads.
Figure 2-6: Switchable MIMCAP cell.

Figure 2-7: Varactor cell.
Figure 2-8: Inductor model and layout.

A

B

Metal 7

Metal 8

Legend:

C1 = 47.1f
R1 = 17.5
C2 = 41.7f
R2 = 6.8
Cpi = 20.5f
R3 = 1.9
L3 = 0.706m

Legend:

Metal 8

Metal 7

Figure 2-8: Inductor model and layout.
Figure 2-9: Automatic Gain Control loop.
Chapter 3

Jitter transfer of generic LTI filters

In this chapter we look at the behavior of Linear Time Invariant (LTI) filters when stimulated by a phase modulated signal. This discussion is fundamental in understanding if the proposed architecture for a resonant buffer can be safely inserted in the CDR phase/frequency control loop. Here, we propose a closed form solution to the problem and we provide a real example that demonstrates its validity. A discussion of a non-linear model to characterize phase noise in ring oscillators is presented in [7] and more recently discussed in [15].

The CDR architecture, for which the discussed resonant buffer is intended, requires that the signal path delivering the clock to the phase detector have a sufficiently large jitter bandwidth to avoid affecting the closed loop behavior of the system. The clock signal at this stage (see fig. 3-1) carries phase information, coming from the system Voltage Controlled Oscillator (VCO) and the subsequent Phase Shifter.

The behavior of the clock signal path between the Phase Shifter and the Phase Detector depends on two elements: the transmission line characteristics of the physical electrical link between the two blocks and the response of the buffer used to deliver the signal to the phase detector. In general, the two elements can be modeled together as an LTI filter with a known frequency response. The question then arises as to
what effect does this filter have on the information contained in the incoming phase modulated signal.

3.1 Jittered signals as Phase Modulated signals

In order to proceed with the analysis, we need to develop a mathematical description of a jittered clock signal. Jitter is the time displacement of certain features of a signal (typically, zero crossings) in a clocked system from where they are expected to appear. In the case of the clock signal driving the CDR phase detector, jitter is used to transfer information about the phase of the clock signal. The phase detector compares the zero crossings of incoming data and clock and determines the leading signal. This information is then used by the system to generate an error signal which drives the closed loop control of the CDR.

In the case of a purely sinusoidal clock signal (typical of this very high frequency application), jitter can be described as a time-dependent change in the instantaneous phase of the signal. This can be written as

\[ x(t) = \cos[w_c t + f_j(t)], \]  

(3.1)
where $x(t)$ is the jittered signal, $w_c/2\pi$ is the clock frequency and $f_j(t)$ is the time dependent jitter generating function. This is by all means equivalent to the description of a Phase Modulated (PM) signal.

In practical engineering applications, it is very common to measure the Jitter Transfer characteristic of a system. In principle, this is a very simple question (albeit one of no easy answer). Take a signal such as $x(t)$ and put it through an unknown system. If the output can be approximated also by a function

$$y(t) \approx \alpha \cos [w_c t + g_j(t)], \quad (3.2)$$

then we conclude that there is a representation of this same system in which for an jitter input of $f_j(t)$ we obtain an output $g_j(t)$. It should be noted that there is not reason to believe that if the unknown system is LTI, the transfer characteristics of jitter (that is from $f_j(t)$ to $g_j(t)$) should be also linear and time invariant.

In spite of this fact, practical measurement have long been performed, using sinusoidal jitter generating functions and assuming linearity and time-invariance of jitter transfer. Much like in the characterization of a LTI system, the magnitude (and potentially the phase) of the input and output sinusoidal jitter generating functions are recorded for a wide range of frequencies. Lee and Hajimiri show how such a measurement can be very useful in understanding, at least to a certain degree of approximation, the behavior of the system with respect to jitter [11].

Figure 3-2 shows a typical setup for a jitter transfer measurement [5]. An unjittered carrier signal (a simple sinusoid) is passed through a phase shifter which changes the signal instantaneous phase according to the test signal coming from a Vector Network Analyzer (VNA). This induces sinusoidal jitter on the carrier. This signal is then passed though the system under test (D.U.T.). The output from the D.U.T. is then mixed back with the original unjittered signal, filtered and passed to the input of the VNA. In this fashion, the VNA is able to record the jitter transfer characteristics.
of the D.U.T. at all the frequencies of interest. It should be noted that the input of the VNA cannot distinguish between Phase Modulation and Amplitude Modulation at the output of the D.U.T.. This is due to the the fact that energy giving rise to these distinct phenomena is combined in the mixing process. In order to circumvent this problem, the test setup has to be able to cancel any AM component of the signal coming from the D.U.T. before mixing with the unjittered carrier is performed. This can be accomplished with a limiting amplifier.

### 3.2 LTI filters

Now that we have established a mathematical description of jitter, describing the phenomena as Phase Modulation of a carrier, we are ready to examine the jitter transfer characteristic of a generic LTI filter.

#### 3.2.1 The small deviation ratio approximation

Let’s take a sinusoidal carrier at a frequency $w_c$ and modulate its instantaneous phase proportionally to a sinusoidal function of frequency $w_j$. The resulting jittered signal

---

Figure 3-2: Typical jitter measurement setup.
\[ p(t) = \cos [w_c t + X \cos(w_j t)] . \] (3.3)

The constant \( X \) represents the amplitude of the jitter component. It is called \textit{deviation ratio} because it can also be expressed as \( \Delta w/w_j \) or the ratio of the peak frequency deviation of the carrier to the jitter frequency at which it occurs [1].

Since we are looking at LTI systems, it is useful to express the signal \( p(t) \) as a summation of sinusoidal signals which are eigenfunctions of the LTI system. This can be accomplished through a well known manipulation. The result is:

\[
p(t) = J_0(X) \cos(w_c t) \\
+ J_1(X) \cos \left[ (w_c + w_j) t + \frac{\pi}{2} \right] + J_1(X) \cos \left[ (w_c - w_j) t + \frac{\pi}{2} \right] \\
- J_2(X) \cos \left[ (w_c + 2w_j) t \right] - J_2(X) \cos \left[ (w_c - 2w_j) t \right] \\
+ \cdots .
\] (3.4)

Therefore, a PM signal is composed of a carrier frequency and a number of sidebands. The sidebands amplitude is controlled by the Bessel functions \( J_n(X) \), where \( n \) is an integer number associated with each sideband.

In general, it can be proven that for small deviation ratios (below 1.0), equation (3.4) can be approximated as follows:

\[
p(t) \approx J_0(X) \cos(w_c t) \\
+ J_1(X) \cos \left[ (w_c + w_j) t + \frac{\pi}{2} \right] + J_1(X) \cos \left[ (w_c - w_j) t + \frac{\pi}{2} \right],
\] (3.5)

therefore considering only the first two sidebands around the carrier frequency.

Furthermore, in the case of deviation ratios even smaller than in the above approximation, the Bessel functions can be approximated by their first order Taylor
expansions, resulting in an even simpler expression:

\[ p(t) \approx \cos(w_c \, t) + \frac{X}{2} \cos \left( (w_c + w_j) \, t + \frac{\pi}{2} \right) + \frac{X}{2} \cos \left( (w_c - w_j) \, t + \frac{\pi}{2} \right), \] (3.6)

This mathematical approximation of a PM signal is better explained with the help of a vector representation. As it is customary, the real part of the vectors in the complex plane represent the signal. Figure 3-3 shows how the sidebands, when small compared to the carrier magnitude, contribute only to an instantaneous change of the carrier phase.

![Figure 3-3: Approximate vector representation of a PM signal. The signal is composed by the sum of its three vector components.](image)

The relative phase of the sidebands can determine whether the modulation effects the phase of the carrier, the amplitude or both.\(^1\) To gain a better understanding, let’s look at an Amplitude Modulated sinusoidal signal.

\[ s(t) = [1 + Y \cos(w_a \, t)] \cos(w_c \, t). \] (3.7)

In this expression, the constant \(Y\) represents the magnitude of the amplitude modu-

\(^1\)In the general case the sidebands can effect both phase and amplitude of the carrier.
lation component. Using simple trigonometric identities, we can rewrite (3.7) as:

\[ s(t) = \cos(w_c \ t) \]
\[ + \frac{Y}{2} \cos[(w_c + w_a) \ t] + \frac{Y}{2} \cos[(w_c - w_a) \ t]. \]  

(3.8)

Figure 3-4: Vector representation of an AM signal. The signal is composed by the sum of its three vector components.

We can then compare the vector representation of this signal in figure 3-4 with that in figure 3-3. It should be evident how the phase of the sidebands plays a fundamental role in determining the type of modulation that the carrier experiences.

### 3.2.2 LTI filtering of PM signals

We are ready to apply the PM signal \( p(t) \) to a generic LTI filter \( H(j \ w) \). If we use the approximation in equation (3.5) we can express the output signal as:

\[ x(t) = |H_1| \ J_0 X \ \cos[w_c \ t + \angle H_1] \]
\[ + |H_2| \ J_1(X) \ \cos[(w_c + w_j) \ t + \angle H_2 + \frac{\pi}{2}] \]
\[ + |H_3| \ J_1(X) \ \cos[(w_c - w_j) \ t + \angle H_3 + \frac{\pi}{2}], \]  

(3.9)
where:

\[ H_1 \equiv H(jw_c) \]
\[ H_2 \equiv H(j(w_c + w_j)) \] (3.10)
\[ H_3 \equiv H(j(w_c - w_j)). \]

A vector representation of signal \( x(t) \) is shown in picture 3-5. Note that the magnitude and the phase time-independent component of the sidebands is arbitrarily effected by the filtering process.

![vector representation](image)

**Figure 3-5**: Approximate vector representation of the signal \( x(t) \).

Since we know nothing about the relative phases of the sidebands, we cannot assume that the output signal \( x(t) \) is a purely PM signal. Instead, we should concentrate our effort in rewriting equation (3.9) in a form in which the individual phase and amplitude modulation components become explicit.

To accomplish this goal we follow the following steps:

1. A simple test signal, \( test(t) \) (to be developed later as eq. (3.11)), composed of a carrier plus a single *small* sideband is analyzed in vector space to explicitly reveal its PM and AM components. The vector representing the sideband is decomposed into four components (to be developed later as eq. (3.12)). Two components explain *phase* modulation of the carrier. One of these components moves clockwise around the carrier and one moves counter-clockwise (like in figure 3-3). The remaining two components explain *amplitude* modulation.
Again, one of these components moves clockwise around the carrier and one moves counter-clockwise (like in figure 3-4).

2. The technique developed in the previous step, is then applied to each of the two sidebands of the signal $x(t)$, which have arbitrary phase and magnitude after passing through the LTI filter $H(jw)$.

(a) The upper sideband is first decomposed in two components rotating together with the carrier (i.e. at the same rate as the carrier), as shown in figure 3-6. $A$ is perpendicular and $B$ is parallel to the carrier. The magnitude of the components changes as the upper sideband rotates around the carrier.

(b) As shown in figure 3-7, $A$ (representing FM) is further decomposed in two constant amplitude components: $V_1$, moving counter-clockwise with phase $(w_c + w_j) t$ and $V_2$, moving clockwise with phase $(w_c - w_j) t$. $B$ (representing AM) is further decomposed in two constant amplitude components: $V_3$, moving counter-clockwise with phase $(w_c + w_j) t$ and $V_4$, moving clockwise with phase $(w_c - w_j) t$.

(c) The lower sideband is then decomposed into two components rotating together with the carrier (i.e. at the same rate as the carrier), as shown in figure 3-8. $C$ is parallel and $D$ is perpendicular to the carrier. The magnitude of the components changes as the lower sideband rotates around the carrier.

(d) As shown in figure 3-9, $C$ (representing AM) is further decomposed in two constant amplitude components: $V_5$, moving clockwise with phase $(w_c - w_j) t$ and $V_6$, moving counter-clockwise with phase $(w_c + w_j) t$. $D$ (representing FM) is further decomposed in two constant amplitude components: $V_7$, moving clockwise with phase $(w_c - w_j) t$ and $V_8$, moving
Figure 3-6: The upper sideband is decomposed into two components rotating together with the carrier: $A$ is perpendicular and $B$ is parallel to the carrier. The magnitude of the components changes as the upper sideband rotates around the carrier.

Figure 3-7: $A$ (representing FM) is decomposed in two constant amplitude components: $V_1$, moving counter-clockwise with phase $(w_c + w_j) t$ and $V_2$, moving clockwise with phase $(w_c - w_j) t$. $B$ (representing AM) is decomposed in two constant amplitude components: $V_3$, moving counter-clockwise with phase $(w_c + w_j) t$ and $V_4$, moving clockwise with phase $(w_c - w_j) t$. 
Figure 3-8: The lower sideband is decomposed into two components rotating together with the carrier: $C$ is parallel and $D$ is perpendicular to the carrier. The magnitude of the components changes as the lower sideband rotates around the carrier.

Figure 3-9: $C$ (representing AM) is decomposed in two constant amplitude components: $V_5$, moving clockwise with phase $(w_c - w_j) t$ and $V_6$, moving counter-clockwise with phase $(w_c + w_j) t$. $D$ (representing FM) is decomposed in two constant amplitude components: $V_7$, moving clockwise with phase $(w_c - w_j) t$ and $V_8$, moving counter-clockwise with phase $(w_c + w_j) t$. 

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counter-clockwise with phase \((w_c + w_j) t\)

The result of this successive series of decompositions is a new expression for \(x(t)\) composed of a carrier and eight sidebands (four describing AM and four describing PM).

3. By means of vector addition, the signal \(x(t)\) is simplified and rewritten as the sum of a carrier and four sidebands (eq. (3.13)), much like the form of signal \(test(t)\) after the decomposition of step 1. In particular:

- Components \(V_1\) and \(V_8\) are added to describe the upper sideband of the PM component.
- Components \(V_2\) and \(V_7\) are added to describe the lower sideband of the PM component.
- Components \(V_3\) and \(V_6\) are added to describe the upper sideband of the AM component.
- Components \(V_4\) and \(V_5\) are added to describe the lower sideband of the AM component.

4. By referring back to equations (3.5) and (3.8), we can then write down the magnitude (and phase) of the PM and AM components of the signal \(x(t)\).

5. Finally, the magnitude and phase of the modulations of signal \(x(t)\) are compared with those of signal \(p(t)\) (the PM signal applied to the filter \(H(jw)\) to generate \(x(t)\)) to derive the jitter transfer and the jitter to AM transfer functions for the filter \(H(jw)\).

With this graphical framework in mind, we can now delve into the mathematical representation of the decomposition process.
Take the generic signal, \( \text{test}(t) \), which contains a carrier and only one sideband at a frequency \( w_c + w_1 \):

\[
\text{test}(t) = \cos[w_c \ t + \gamma_c] + \alpha \cos[(w_c + w_1) \ t + \gamma_1]. \quad (3.11)
\]

For completeness, both carrier and sideband have their own arbitrary phase constant \( \gamma_c \) and \( \gamma_1 \). Also note that the direction of rotation of the sideband depends on the sign of the frequency \( w_1 \).

With the help of the vector representations developed above for AM and PM signals, we can rewrite the expression for \( \text{test}(t) \) so that each modulation component is explicit.

\[
\text{test}(t) = \cos[w_c \ t + \gamma_c] + \frac{\alpha}{2} \left\{ \right.
\begin{align*}
+ \cos[(w_c + w_1) \ t + \gamma_1] & + \cos[(w_c - w_1) \ t - \gamma_1 + 2\gamma_c] \quad \leftarrow \text{carrier} \\
+ \cos[(w_c + w_1) \ t + \gamma_1] & - \cos[(w_c - w_1) \ t - \gamma_1 + 2\gamma_c] \quad \leftarrow \text{AM mod.} \\
\end{align*}
\left. \right\} \quad \leftarrow \text{PM mod.} \quad (3.12)
\]

In equation (3.12), the PM component (expressed by the sum of two vectors) is always orthogonal to the carrier, while the AM component is always parallel to the carrier. Note that (3.11) and (3.12) are perfectly identical since the extra terms in (3.12) cancel each other out.

Using similar approximations to those of section 3.2.1, we can rewrite the signal \( \text{test}(t) \) in a form that explicitly shows the Amplitude and Phase modulations of the carrier.

\[
\text{test}(t) \approx \\
[1 + \alpha \cos(w_1 \ t + (\gamma_1 - \gamma_c))] \cos[w_c \ t + \gamma_c + \alpha \cos(\pm w_1 \ t + (\gamma_1 - \gamma_c) - \frac{\pi}{2})] \\
\]

(3.13)

The same technique can be applied to the signal \( x(t) \) of equation (3.9). Decom-
posing each of the two sidebands in their AM and PM components:

\[
x(t) = |H_1| J_0(X) \cos [w_c t + \angle H_1] \quad \leftarrow \text{carrier} \\
+ |H_2| J_1(X) \cos \left[ (w_c + w_j) t + \angle H_2 + \frac{\pi}{2} \right] \quad \leftarrow \text{AM mod.}
\]
\[
+ \frac{|H_2|}{2} J_1(X) \cos \left[ (w_c - w_j) t + \angle H_2 + 2\angle H_1 - \frac{\pi}{2} \right]
\]
\[
+ \frac{|H_3|}{2} J_1(X) \cos \left[ (w_c - w_j) t + \angle H_2 + \frac{\pi}{2} \right]
\]
\[
+ \frac{|H_3|}{2} J_1(X) \cos \left[ (w_c + w_j) t - \angle H_2 + \angle H_1 - \frac{\pi}{2} \right] \quad \leftarrow \text{PM mod.}
\]
\[
- \frac{|H_2|}{2} J_1(X) \cos \left[ (w_c - w_j) t - \angle H_2 + 2\angle H_1 - \frac{\pi}{2} \right]
\]
\[
+ \frac{|H_3|}{2} J_1(X) \cos \left[ (w_c - w_j) t + \angle H_2 + \frac{\pi}{2} \right]
\]
\[
- \frac{|H_3|}{2} J_1(X) \cos \left[ (w_c + w_j) t - \angle H_2 + 2\angle H_1 - \frac{\pi}{2} \right] .
\]

(3.14)

**Jitter transfer**

In order to calculate jitter transfer magnitude and phase of the generic LTI filter, we have to perform a vector sum of the PM modulation component of equation (3.14) to obtain a signal of the form shown in equation (3.5).

Ignoring the AM modulation component, we can write \(x(t)\) as follows:

\[
x_{PM}(t) = A \left\{ J_0(\alpha X) \cos (w_c t + \gamma_c) \\
+ J_1(\alpha X) \cos \left[ (w_c + w_j) t + \gamma_j + \gamma_c + \frac{\pi}{2} \right] \\
+ J_1(\alpha X) \cos \left[ (w_c - w_j) t - \gamma_j + \gamma_c + \frac{\pi}{2} \right] \right\},
\]

(3.15)
where $\alpha$ is the jitter transfer magnitude, $\gamma_j$ is the jitter transfer phase and $A$ is a constant. Performing the necessary vector sums:

$$
A J_0(\alpha X) = |H_1| J_0(X)
$$

$$
\gamma_c = \angle H_1
$$

$$
A J_1(\alpha X) = \frac{J_1(X)}{2} \left| H_2 \right| e^{j(\angle H_2 - \angle H_1)} + \left| H_3 \right| e^{j(\angle H_3 - \angle H_1)}
$$

$$
\gamma_j = \angle \left( |H_2| e^{j(\angle H_2 - \angle H_1)} + |H_3| e^{j(\angle H_3 - \angle H_1)} \right)
$$

Therefore, under the less-restrictive small deviation-ratio approximation, we can combine the equations in (3.16) and produce an open form that allows numerical estimation of $\alpha$, the jitter transfer magnitude:

$$
\frac{J_1(\alpha X)}{J_0(\alpha X)} = \frac{J_1(X)}{J_0(X)} \left( \frac{|H_2| e^{j(\angle H_2 - \angle H_1)} + |H_3| e^{j(\angle H_3 - \angle H_1)}}{2|H_1|} \right)
$$

$$
\gamma_j = \angle \left( |H_2| e^{j(\angle H_2 - \angle H_1)} + |H_3| e^{j(\angle H_3 - \angle H_1)} \right)
$$

(3.17)

Note that the expression under the square root is under all circumstances real and positive.

Similarly, we can simplify the expression for $\gamma_j$, the jitter transfer phase:

$$
\gamma_j = \angle (H_2 H_1^* + H_1 H_3^*)
$$

(3.18)

Finally, in the case of very small ratios $X$ and $\alpha X$, we can replace the Bessel functions in equation (3.17) with their first order Taylor expansion. This allows the derivation of a closed form solution for $\alpha$.

$$
\alpha \approx \sqrt{|H_3 H_1^* + H_1 H_3^*| (H_2 H_1^* + H_1 H_3^*)} \frac{2 H_1 H_3^*}{2 H_1 H_3^*}
$$

(3.19)
Jitter to Amplitude Modulation transfer

As we have discussed previously, the output of the generic LTI filter can contain a certain amount of Amplitude Modulation. While this is not necessarily interesting from the point of view of a digital system (like the one proposed in this thesis), for completeness, we will present the equations that describe Jitter to Amplitude Modulation transfer magnitude and phase.

If we look only at the AM component of the output signal, we can write x(t) as follows:

\[ x_{AM}(t) = A \left\{ \cos(w_c t + \gamma_c) \\
+ \frac{\beta X}{2} \cos \left[ (w_c + w_j) t + \gamma_a + \gamma_c + \frac{\pi}{2} \right] \\
+ \frac{\beta X}{2} \cos \left[ (w_c - w_j) t - \gamma_a + \gamma_c - \frac{\pi}{2} \right] \right\}, \quad (3.20) \]

In this model, the frequency of the AM component is identical to that of the incoming jitter \( w_j \), and \( \beta \) represents the ratio between the AM modulation index of the LTI filter output signal and the deviation ratio of the incoming jittered signal.

Performing vector operations similar to those used to calculate jitter transfer, we can derive explicit expressions for \( \beta \) and \( \gamma_a \).

\[
\beta = \frac{J_1(X)}{X J_0(X)} \left| \frac{H_2 e^{j(\omega H_2 - \omega H_1)} - |H_3| e^{j(\omega H_1 - \omega H_3)}}{|H_1|} \right|
= \frac{J_1(X)}{X J_0(X)} \sqrt{(H_1 H_2^* - H_3 H_3^*)} \frac{H_2 H_1^* - H_3 H_3^*}{H_1 H_1^*} \approx \frac{\sqrt{(H_1 H_2^* - H_3 H_3^*)} (H_2 H_1^* - H_3 H_3^*)}{2 H_1 H_1^*} (3.21) \]

\[
\gamma_j = \angle \left( |H_2| e^{j(\omega H_2 - \omega H_1)} - |H_3| e^{j(\omega H_1 - \omega H_3)} \right) = \angle (H_2 H_1^* - H_1 H_3^*) \quad (3.22) \]
3.3 Jitter behavior of resonant tank

Now that we have developed a theoretical framework to predict jitter transfer of any LTI filter, we can devote our attention to the more specific case of the clock network of figure 3-1. In particular, we want to answer the question of whether a resonant buffer could effect the closed loop behavior of the frequency/phase lock loop.

3.3.1 Tank configuration

In this analysis, we assume that the clock frequency is $5.0 \, GHz$. Furthermore, because of the nature of Current Mode Logic, we consider only differential signals in our analysis.

Figure 3-10 shows two possible configuration for the CML buffer load. In the case of load A, the tank quality factor is determined by the equivalent series resistance of the inductor. Under certain circumstances, one might want to reduce the quality factor arbitrarily. This goal is obtained (as shown by load B) by placing a resistor in parallel with the tank.\(^2\)

![Diagram of two possible configurations for the resonant buffer loads.]

Because of constraints in the design, we are aiming at a unity gain for the entire buffer at the clock frequency. In the actual design, this is obtained with the use of

\(^2\)In this case, we simply ignore the equivalent series resistance of the inductor for frequencies close to resonance.
a closed loop Automatic Gain Control unit, in the “$G_m$ stage” of the buffer. At the same time, the nature of equations (3.19) and (3.18) is such that a constant gain factor in the transfer function of the LTI filter under consideration, is irrelevant. Therefore, we simply ignore constant gain factors for the remainder of the chapter.

In the case of load A, the LTI transfer function of the resonant buffer is proportional to:

$$H_A(jw) \propto \frac{1 + jw \frac{L}{R}}{(1 - LCw^2) + jwRC}.$$  (3.23)

In the case of load B:

$$H_B(jw) \propto \frac{jwL}{(1 - LCw^2) + jw\frac{L}{R}}.$$  (3.24)

The buffer, as we discuss in this thesis, can be operated in one of three different configurations that result in a phase contribution to the carrier clock signal of 0, +45, or −45 degrees. This constitutes the first constraint on the parameters $L$, $C$ and $R$. Additionally, the maximum overall quality factor of the tank is constrained by the equivalent series resistance of the inductor which, in turn, is determined by the physical design. Practically, the effective Q of tank will be in the range of $5 − 10$.

With these considerations in place and assuming a value of $L = 1\, \text{nH}$, table 3.1 shows the different component values for all the possible configurations of the resonant buffer\(^3\).

### 3.3.2 Jitter transfer

We now have a series of LTI models for the loads facing the CML buffer that cover most of the likely configuration of the design. Equations (3.17) and (3.18) let us plot for each of these configurations the predicted magnitude and phase of the jitter.

\(^3\)In the case of load A, the Q was calculated using the formula for a tank in which all elements are connected in series. This greatly simplified the calculations while maintaining an acceptable level of accuracy.
Transfer function. Figures 3-11 and 3-12 show the results for a small variation ratio of $X = 0.1$.

These calculations have been further corroborated using a numerical simulation developed originally by Larry De Vito of Analog Devices, with contributions from the author. The simulation code appears in Appendix C.

A number of conclusions can be drawn from this analysis.

- Under all circumstances the jitter transfer bandwidth $^4$ of the LTI buffer is in excess of 200 MHz.

- All jitter magnitude peaking$^5$ is maintained below $+2dB$ and in all but one of the test cases it is only a fraction of $+1dB$.

Qualitatively, we can also observe that, in the case of 0 degree phase contribution to the carrier, the jitter bandwidth of the tank is very close to the amplitude transfer bandwidth of the tank. In the case of $\pm 45$ degrees phase contribution to the carrier, the jitter bandwidth is increased approximately by a factor of two.

Therefore, given these characteristics and a closed-loop bandwidth of the CDR control-loop below 10MHz, it is reasonable to conclude that the resonant buffer will

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Tank & Clock phase (deg.) & Tank $Q = 5$ & & Tank $Q = 10$ & \\
& & $C$ (pF) & $R$ (Ω) & $C$ (pF) & $R$ (Ω) \\
\hline
A & 0 & 0.973 & 6.41 & 1.00 & 3.16 \\
& +45 & 0.735 & 7.35 & 0.895 & 3.34 \\
& −45 & 1.16 & 5.87 & 1.10 & 3.01 \\
\hline
B & 0 & 1.01 & 157 & 1.01 & 315 \\
& +45 & 0.830 & 174 & 0.917 & 330 \\
& −45 & 1.24 & 142 & 1.12 & 299 \\
\hline
\end{tabular}
\end{table}

Table 3.1: Component values for the test configurations of the resonant buffer.

\footnotesize{$^4$Jitter transfer bandwidth is defined here to be the frequency at which the jitter transfer magnitude falls to $−3dB$ of its low-frequency value.}

\footnotesize{$^5$Jitter magnitude peaking is defined as the maximum magnitude reached by jitter magnitude relative to low-frequency values.}
have virtually no impact on the behavior of the clock network.

A final note should be made on the potential for the resonant buffer to generate large amounts of Amplitude modulation on the clock signal that could interfere with the operation of the bang-bang half rate phase detector. Figures 3-13 and 3-14 show the amplitude modulation magnitude (as a fraction of carrier magnitude) for the two configurations of the buffer LTI load. In all cases, the AM magnitude is always less than 20 $dB$ lower than the carrier magnitude and, therefore, we can safely conclude that it will not have an effect of the rest of the CDR system.
Figure 3-11: Configuration A: Jitter transfer magnitude and phase for buffer LTI load. $Q$ refers to the quality factor of the tank and $angle$ to the phase contribution given to the clock carrier.
Figure 3-12: Configuration B: Jitter transfer magnitude and phase for buffer LTI load.
Figure 3-13: Configuration A: Amplitude modulation magnitude (as fraction of carrier magnitude) for buffer LTI load.

Figure 3-14: Configuration B: Amplitude modulation magnitude (as fraction of carrier magnitude) for buffer LTI load.
Chapter 4

Buffer Control Architecture

This chapter describes the control architecture for the resonant buffer. A combination of digital and analog circuits ensures that under a wide range of process variations and run-time temperature variations, the resonant buffer is able to deliver the two phases of the output clock in relative quadrature.

The original idea for the control loop was first given to the author by Lawrence De Vito of Analog Devices. The phases of the two output clock signals are measured with the help of a phase detector\(^1\). If the phases are not in exact quadrature, a differential current error signal is produced and integrated by a charge pump. The differential output voltage of the charge pump is then used to control the additional capacitive loads in the resonant buffer. In particular, when capacitance is increased to the buffer generating one output clock phase, it is decreased in the other buffer. This system was first thought of in the context of the two resonant buffer being driven with two clock phases in quadrature. The resonant buffer would then be responsible for correcting only small quadrature errors present in the incoming signal.

Under the suggestion of Dr. John (Jack) Kenney of Analog Devices, the objective

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\(^1\)This is a different circuit than the HRBB phase detector to which the resonant buffer delivers the quadrature clock. In order to avoid confusion, in this chapter we always refer to the CDR phase detector as the “HRBB phase detector”.  

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of the resonant buffer control expanded to include the generation of quadrature signals from a single input clock phase. While the general approach described above does not change, this application requires a much wider control dynamic range. In particular, the center frequency of the buffer load tanks must be moved farther away from the clock frequency than in the original application.

An initial study of the problem showed that, within the boundaries of the available processing technology, the objective of creating quadrature generation could not be accomplished with a simple analog control loop. The fairly poor tuning range of MOS varactors does not allow to obtain a wide enough change in the capacitive load of the resonant buffer. As shown in section 2.3.2, the MOS varactor cells show a total tuning range of about 50% of their maximum capacitance (compared to more than 75% in the case of MIMCAP cells). As a consequence, a buffer that employs only MOS varactors and still satisfies the required capacitive tuning range, requires a total capacitive load hard to manage. In particular, to obtain tank resonant frequencies centered around the clock frequency, lower value inductors are needed which are typically lossier structures. This, in turn, reduces the tank overall quality factor, further widening the needed capacitive tuning range, and reducing the power efficiency of the buffer.

Because of the above considerations, the final resonant buffer control architecture features a combination of an inner analog control loop, which acts directly on the MOS varactors in the buffer, and an outer digital system, which is capable of switching MIMCAP cells in and out as needed. The rest of the chapter describes this system in detail.

4.1 Inner Analog Control Loop

A schematic representation of the inner analog control loop is presented in figure 4-1. The rest of the system is not shown and we assume, for the time being, that the
overall buffer architecture ensures that the dynamic range of the sole analog loop can guarantee zero quadrature error at the output of the buffer.

Figure 4-1: Inner analog control loop.

A fully-differential phase detector produces a set of differential currents proportional to the quadrature error between the two clock phases delivered to the HRBB phase detector. These sets of differential currents are then passed onto a differential charge pump (with a common mode output voltage of $0.9\,\text{V}$ or the voltage at which the MOS varactor cells are approximately at the center of their dynamic range). Each of the two outputs of the charge pump is then used to drive the control voltage of the varactor cells in one of the two CML buffers$^2$. The charge pump therefore controls differentially the MOS varactor cells in the two buffers, by adding (or subtracting) capacitance to one buffer, while performing the opposite operation on the other. Overall, the inner analog loop is a pure differential control that provides negative feedback, so that a positive quadrature error at the input of the loop phase detector will generate a charge pump capacitive voltage, which, in turn, will shift the capacitive loads to reduce the initial error.

$^2$Note that while figure 2-5 shows three control voltages for each of the varactor cells, all three are connected together to one side of the charge pump output.
Two additional features are present in the inner control loop and enable exchange of information with the outer digital system.

- The charge pump can be reset by enabling a logic control signal reset. In the reset state, the charge pump outputs are both equal to 0.9 V. This allows an external system to disable the inner control loop and to set all varactor cells to the center of their capacitive range.

- A detector (named “detect clamps” in figure 4-1) compares the difference of the output voltages from the charge pump, with fixed references of 0.8 V and −0.8 V. If the former exceeds either reference, the appropriate logic flag, range_detect_high or range_detect_low, is enabled. This allows the inner analog control loop to inform the outer digital system that it is close to the boundaries of its dynamic range and that MIMCAP cells might need to be switched. Figure 2-3 shows that the useful range of each varactor cell is approximately 0.3 V wider of the boundaries built into the detect clamps.

4.1.1 Phase detector

Only marginal effort was made in developing the phase detector, charge pump and detect clamps circuits, since these are readily available modules. Nevertheless, in order to provide reasonable data for stability and power consumptions calculations, a brief discussion follows for each of the three components.

Given the differential nature of the circuit and the need for accurate detection of quadrature error, particular care is needed in designing a balanced and matched phase detector. Figure 4-2 shows a phase detector topology that can accomplish this goal. The detector is of the Gilbert type. Two identical copies of the same multiplier (XOR) cell are used to preserve symmetry in the resonant buffer tanks. They are wired as to constructively add their outputs. $V_{ref}$ is a voltage reference coming from the CDR main biasing tree. The reference is used to provide two equal tail currents.
The phase detector can be loaded with two current mirrors that connect directly to the charge pump.

A simulation was run to test this topology. The tail currents were set both to 60µA and all input devices (marked in figure 4-2 by the letters A and B) were minimum length, 3µm wide. Each of the inputs were a properly biased, 0.8V peak-to-peak differential sine waves.

Figure 4-3 shows the differential output current of the phase detector, as the inputs relative phases go from 105 to 75 degrees in decrements of 5 degrees. The transfer function of the phase detector is approximately (ignoring any dynamic response and the large 5GHz ripple):

\[ I_{\text{diff}}^{\text{OUT}} \approx 19.3 \mu A \cos(\Delta \phi), \]  

where \( \Delta \phi \) is the phase difference between the input clock signals.

In the final design, the detector devices must be chosen to be of larger width to increase matching. Bharath Reddy created a phase detector/charge pump (see next section) design with similar topology that offers an input referred error of 3.3 degrees.
Figure 4-3: Phase detector differential current output. Input phase difference goes from 105 to 75 degrees in decrements of 5 degrees.

(95% confidence interval). The input gates of the detector result in an additional load of approximately 60 $fF$ on each single-ended output of the CML buffer.\(^3\) This level of accuracy is well within the quadrature error allowed at the input of the HRBB phase detector. If, in a different context, higher accuracy were required, larger devices could be used. It should be noted that, in general, power consumption of this block is independent of the size of the input devices.

\(^3\)This fact was taken in consideration in the circuit simulations. An allowance of 100 $fF$ on each single-ended output of the CML buffer was provisioned. In case the detector did not provide a sufficiently large capacitive load, additional MIMCAP should be added to reach the 100 $fF$ target.
4.1.2 Charge Pump

Figure 4-4 shows the preliminary design for a charge pump in the inner analog control loop. The output currents from the phase detector are redirected through current mirrors to the input of the charge pump. The capacitive load $C$ is divided into two equally sized MIMCAPs to maintain total symmetry. The goal of the charge pump is to integrate the difference between the input currents.

![Schematic view of the loop charge pump and its biasing circuits.](image)

The remaining part of the circuit is concerned with maintaining proper voltage bias at the charge pump capacitive loads\(^4\). To this effect, the common voltage at points A and B is sensed through two source followers, whose outputs are connected through a voltage divider resistive network. The resistances $R$ are chosen so they are much larger of the output impedance of the source followers. The voltage at node C is then compared to the reference voltage $V_{\text{common}}$ (lowered by one $V_T$) at the sense amplifier. If C is lower than the reference, the amplifier reduces the current going through the NMOS sources at the bottom of the charge pump and vice-versa.

\(^4\)This design takes inspiration from the biasing circuitry of the CDR charge pump, developed by Bharath Reddy and Jack Kenney of ADI.
The current mirrors between the phase detector and the charge pump have a ratio of 1. So do the mirrors in the DC biasing circuitry. Therefore the current $I_{\text{sense amp}}$ is set close to the sum of the two $I_{\text{tail}}$ currents in the phase detector (i.e. $120 \mu A$). The source followers do not need particularly fast responses, so their load currents are also very small.

The maximum differential voltage swing at the output of the charge pump, is dictated by the choice of common mode voltage, the voltage supply and the output impedance of the top and bottom current mirrors. If the latter is too low, then the voltage swing might be severely limited. Powering this circuit with the $1.8 \, V$ chip supply and setting $V_{\text{common}}$ to $0.9 \, V$ allows enough dynamic range to directly drive the control voltages of the varactor cells.

Finally, the reset feature can be implemented with the use of a switch across the charge pump capacitors.

### 4.1.3 Detect Clamps

The detect clamps are a simple circuit which compares the differential output of the charge pump with two references $0.8 \, V$ and $-0.8 \, V$. This operation can be accomplished with the use of a differential amplifier at each of the charge pumps outputs. Since the common mode voltage of the charge pump is kept at $V_{\text{common}}$, the reference for both differential amplifiers can be taken to be $0.4 \, V$ above $V_{\text{common}}$. This arrangement provides a symmetrical load for the charge pump outputs and maintains circuit balance. The output of each of the differential amplifiers is then latched for use by the outer digital system. The latching signal is provided by the digital circuitry.

Overall static power consumption of this module should not exceed $100 \, uA$. This goal can be easily accomplished because of the very low frequency nature of the application.
4.1.4 Loop Stability

The control loop described so far is an example of dominant pole compensated control. The integration performed in the charge pump, ensures the stability of the loop and sets, at the same time, the closed-loop time constant of the response.

As previously mentioned in section 4.1, the analog control loop can only differentially effect the two phases of the clock signal, and therefore cannot influence the performance of the CDR major control loop. In fact, while the clock is maintained in quadrature by the inner analog control loop, the CDR loop acts only on the common mode of the two phases of the clock signal.

The design is therefore not particularly concerned with the bandwidth of the inner analog control loop. A value for the capacitor $C$ in the charge pump can be chosen, so that crossover occurs at a maximum arbitrary frequency of about $1MHz$.

The loop gain can be approximated as follows, paying attention to choose the maximum possible value for each gain component. Linearizing the transfer function of the phase detector around zero quadrature error ($\phi_{error}$) from eq. (4.1):

$$I_{OUT}^{diff} \approx 19.4 \mu A \phi_{error},$$  \hspace{1cm} (4.2)

where angles are expressed in radians. There are two buffers, so a factor of 2 should be added in the overall gain between error signal and quadrature error. The varactor cells are assumed to be biased in their region of maximum incremental capacitance. The Q of the tanks is taken to be 11.0 and the tanks are considered tuned close to the clock frequency (where capacitive change to phase gain is highest) so that eq. (2.3)
applies. This leads to the following approximate loop transfer function:

\[
L(s) = 2 \text{(phase detector gain)} \frac{1}{sC} \left( \text{max varactor } C/V \right) \left( -\frac{Q}{C_{TOT}} \right)
\]

\[
= 2 \times 19.4 \mu A \times \frac{1}{sC} \times 42 fF/V \times (-) \frac{11}{700 fF}
\]

\[
= \frac{1}{sC} 2.57 \times 10^{-5} \frac{1}{\Omega}
\]

(4.3)

For unity gain to occur at a maximum of 1MHz, the charge pump capacitive load should be at least:

\[
C \approx 4.1 pF.
\]

(4.4)

Implementing this capacitance with MIMCAPs, the area required is about 4100\(\mu m^2\). This area could be additionally reduced by choosing a faster response time or by introducing a gain reduction in the current mirrors between the phase detector and the charge pump.

### 4.2 Start-up Tuning Sweep

In terms of power consumption and control dynamic range utilization, it is ideal that when the inner analog control loop has settled, one of the CML resonant buffer provides a phase contribution of +45 degrees while the other provides an opposite contribution of −45 degrees to the clock carrier.

Since the analog control loop can only act differentially on the phase contribution of the two CML buffers, it is the responsibility of the outer digital system to “center” the operation of the inner loop. This is accomplished by choosing the MIMCAP combination (equal for both CML buffers) that provides close to zero phase contribution to the carrier, while the varactors are set to the center of their dynamic range.

As it was mentioned, because of the sensitivity of the tank impedance to elements such as the amount of resistive parasitics in the load and the relative position of clock
and tank center frequency, each tuned buffer tail current is set by the AGC circuit which tries to maintain a constant 400mV\textsubscript{pk−pk} single ended output signal.

This arrangement allows for a simple but rather ingenious way to “tune” both tanks during start-up, first suggested by Bharath Reddy of Analog Devices. While the inner analog control loop is interrupted by enabling the \textbf{reset} signal to the charge pump, the tail currents for both I and Q phase clocks are mirrored and added together. A digital circuit then sweeps through all the possible values of additional capacitance by switching in the MIMCAP cells one at a time. This sweeping is done with identical additional capacitance for both the I and Q buffer tanks. The digital circuit then detects the number of MIMCAP cells that need to be switched in to give the lower tail currents in the buffers and selects that configuration.

Detection of the current range is done with the help of a rudimentary A/D converter, while the flag for initiating start-up procedures is provided by the central CDR digital control logic. After the switching of each MIMCAP cell takes place, the logic waits an arbitrary 50 ns for the AGC loop to settle and then looks at the sum of the two buffers tail currents (which should be approximatively equal, within the bounds of circuit matching).

Figure 4-8 shows the the result of simulating such a sweep on the tail current of one of the two CML buffers for an incoming clock frequency of 5.3 GHz, nominal process and ambient temperature. The MIMCAP cells are all off at time zero and are progressively turned on, one at a time. In this particular case the digital logic would choose to leave on 6 of the total 15 MIMCAP cells at the end of start-up procedures.

Simulations over all process corners, temperatures and incoming clock speeds, show that this procedure centers the resonant frequency of the tanks on the incoming clock frequency so that each of the two CML buffers phase contribution to the incoming signal is within a range of ± 10 degrees\textsuperscript{5}. In addition, as shown in appendix B,

\textsuperscript{5}If the resonant frequency and the clock frequency were perfectly aligned the phase contribution should be zero. This is not possible because of the discrete nature of the capacitance added by MIMCAP cells.
we can expect the relative phase contribution of each of the two buffers to be within 3 degrees of each other.

### 4.3 Run-time MIMCAP Switching

Once the start-up tuning sweep has taken place, the outer digital system sets the MIMCAP count for both CML buffers to the value that ensures minimum tail currents for a given output signal amplitude (enforced by the AGC circuits). By happy coincidence, this results in tuning of the tanks close to the clock frequency so that their phase contribution to the clock carrier is minimized (within the resolution of the MIMCAP cells). When this happens, the inner analog control loop is enabled by lowering the reset signal to the charge pump.

Immediately, the phase detector of the inner control loop produces a large differential current error signal, indicating that the two CML buffers are not generating quadrature. This signal is integrated by the, now enabled, charge pump, which controls differentially the varactor cells in each of the two CML buffers.

Because of the reasons discussed at the beginning of this chapter, most of the capacitive tuning range resides in the MIMCAP cells. In particular, in each buffer the varactors account for only $3 \times 38 \, fF = 114\, fF$ of nominal capacitive tuning, while the MIMCAP cells account for $15 \times 29.4 \, fF = 441 \, fF$ - a ratio of about $1/4$. While this allows enough dynamic range of the buffer, it also means that under certain situations there might be the need for switching MIMCAP cells during active CDR operations. Much time and effort was dedicated to avoid such run-time switching, by providing more evolved start-up procedures. Unfortunately, it simply proved an unattainable goal\(^6\).

\(^6\)In particular, it was the ability of sustaining large run-time temperature variations, that proved the hardest requirement to meet. Temperature variation effects the quality factor of the planar metal inductors used in the buffer. When buffers are operating close to ±45 degrees of phase contribution to the clock carrier, this in turn results in the need for very large correction in buffer capacitive loads, which can’t be guaranteed with the use of varactor cells only
The detect clamps are used to detect when a run-time switch of MIMCAP cells is necessary. Here is a description of the process:

1. During run-time, a timing signal is provided every 50 \( \mu s \) to the outer digital system from the CDR main control logic. The timing of this signal is meant to allow the charge pump of the inner analog control loop to settle completely (or to exhaust its dynamic range). When the signal is received, the outer digital system latches the `range_detect_high` or `range_detect_low` from the detect clamps.

2. If either `range_detect_high` or `range_detect_low` is high\(^7\), then the outer digital system initiates the procedure to differentially turn on or off one MIMCAP cell in one of the two CML buffers and to do the opposite in for the other buffer.

3. If no more MIMCAP cells can be turned on or off in one of the CML buffers, then no action is taken for that specific buffer while the other is switched as usual. While this provision can disrupt the symmetry between the two CML buffers, and therefore, effect negatively the power efficiency of the circuit (see section 2.2.1), it is necessary to give the buffer enough dynamic range to ensure quadrature generation at all times.

4. The outer digital loop then waits for the next timing signal to repeat this procedure.

It should be noted that the outer digital system is stable because of two provisions:

- The time distance between timing signals allow full settling of the inner analog control loop.

- In the absence of any external disturbances to the loop, the contribution of switching one MIMCAP cell is not enough to drive the detect clamps from a

\(^7\)Unless a circuit failure occurs, only one of the signals can be high during run-time.
state of range_detect_low to a state of range_detect_high and vice-versa. This is because the dynamic range of single MIMCAP cell is 29.4 \( fF \), while the range of the all the varactor cells from an input control voltage of 0.9 + 0.4 V to 0.9 − 0.4 V is 70.2 \( fF \). Even allowing for wide process variations, in conjunction with the strictly first order response of the inner control loop, this ratio (in excess of 2 to 1) ensures that no periodic instability occurs where MIMCAP cells are being turn on and off in a periodic steady state.

4.3.1 Slow switching of MIMCAP cells

The system described above allows for seamless interaction between the inner control loop and the outer digital system. In particular, the dynamic range of the analog loop is extended with the use of run-time switching of MIMCAP cells.

A slight complication arises from the fact that while MIMCAP cells are being switched, the inner analog control loop must be able to adjust fast enough, in order to keep the buffer output clock phases in quadrature. A solution to this problem was first suggested by Jack Kenney of Analog Devices. A special slow inverter is used to drive the sel logic control of the MIMCAP cell to be switched. Figure 4-5 shows the test setup for such a slow inverter. The slow inverter (mn3 and mp0) is built using maximum length and devices and is loaded with a MIMCAP of nominal size 1 \( pF \). The inverter provides a way to slowly vary the effective capacitance of the MIMCAP cell. Given the large die area needed to lay out such a structure, only one copy per CML buffer is used. A series of pass gates allows each MIMCAP cell to be driven by a regular (“fast”) inverter or the slow inverter.

Switching a MIMCAP cell from the on to the off state does not turn the cell into a high-impedance connection. Table 2.1 shows how the cell retains its capacitive behavior in both states (for a frequency of 5 \( GHz \)). This is also true during slow
switching (see figure 4-6). In other words, the cell always looks capacitive, while the value of the effective capacitance changes during switching. This phenomena is due to the high level of capacitive coupling through the substrate within the cell. An unfortunate consequence of this coupling is the effective limitation of the MIMCAP cells dynamic range.

The fast inverters are used during the start-up tuning sweep as well as during run-time to maintain a MIMCAP cell in its state of on or off. When the outer digital system determines that a MIMCAP needs to be switched, the following actions take place:
1. Node vcap is pre-charged to the right state of logic high or logic low, with the help of pre-charge gates (not shown in the test circuit).

2. After 1 $\mu s$, the pass gate between the SLOW inverter and the MIMCAP cell to be switched is enabled.

3. After 1 $\mu s$, the pass gate between the FAST inverter and the MIMCAP cell to be switched is disabled.

4. After 1 $\mu s$, the SLOW and FAST inverters are switched.

5. The system waits for 15 $\mu s$ for the MIMCAP cell to fully switch.

6. The pass gate between the FAST inverter and the switched MIMCAP cell is enabled.
Figure 4-7: Schematic representation of the inner analog control loop for study of capacitive disturbances, $c(s)$, to output phase response, $e(s)$.

7. After 1 $\mu s$, the pass gate between the SLOW inverter and the switched MIM-CAP cell is disabled.

This operation can take place well within the 50 $\mu s$ between timing signals to the outer digital system from the CDR control logic.

The circuit in figure 4-5 was used to simulate the performance of slow MIMCAP cell switching. As for most simulations performed in this thesis, the presence of a high frequency clock and the need to observe phenomena in the $\mu s$ scale resulted in stiff simulations, which are notoriously long and difficult to handle.

Figure 4-9 shows the input current to a MIMCAP cell and the voltage at node $v_{sel}$, during switching with the SLOW inverter setup described above. The cell is driven with a differential voltage signal of $0.8V_{pk-pk}$ at the clock frequency of 5 $GHz$, much like in the environment of the resonant buffer. The input current to the MIMCAP cell can be then used to calculate the equivalent time it takes for the MIMCAP cell to fully switch. The behavior of the switching can be approximated by a linear transition from fully on to fully off that lasts around 2 $\mu s$.

This ramp of linearly changing capacitance can be then viewed as a disturbance of the inner analog control loop (see figure 4-7). Using the same assumptions of section
4.1.4, we can calculate the transfer function between disturbances in capacitance, \( C(s) \), and output phase of the resonant buffer, \( e(s) \), as:

\[
\frac{e}{C}(s) = \frac{H(s)}{1 + H(s) \ G(s)} = \frac{2 \ \frac{Q}{C_{ror}}}{1 + L(s)} = 5.0 \times 10^6 \ \frac{s}{1 + \frac{s}{2 \pi \times 10^6 \ Hz} \ sec} \ F,
\]

where \( L(s) \) is defined in eq. (4.3) and the value of \( C \) is taken from eq. (4.4).

The disturbance can be then modeled as a ramp:

\[
C(s) = \frac{1}{s^2} \ \frac{29.4 \ fF \ sec}{2 \ \mu s} = \frac{1}{s^2} \ 1.5 \times 10^{-8} \ F.
\]  

With the help of the final value theorem, we can calculate the value of the error at the output due to the disturbance (which occurs in steady state):

\[
e_{ss} = \lim_{s \to 0} s \ \frac{e}{C}(s) \ C(s) = 0.075 \ rad = 4.3 \ degrees.
\]  

This error appears at the output of the resonant buffer when a MIMCAP is switched for a short period of time (about \( 2 \mu s \)). When steady state operation of the of the inner analog control loop is reached, switches of MIMCAP cells should be a very rare occurrence, determined by large changes of environment temperature (which happen on the \( 1 \ ms \) time scale or slower). The design therefore allows for infrequent appearance of this error at the output of the resonant buffer.

It should be noted that the calculated error in eq. (4.7) is just an approximation. On one side, the assumptions in section 4.1.4 were meant to ensure a maximum unity gain cross-over frequency of the inner analog control loop of \( 1 \ MHz \), and therefore, the calculated error underestimates the actual observation when cross-over occurs at a lower frequency. At the same time, the similar duration of the inner analog control
loop time response and of the capacitive disturbance ramp suggests that the error in eq. (4.7) might be an overestimation of actual behavior. Overall, it is plausible to assume that the calculated value is within a factor of 2 of the expected observation.

4.4 Other Circuits

A/D Converter

The A/D converter needed to measure the sum of the tail currents of the CML buffers during the start-up tuning sweep was designed by Bharath Reddy of Analog Devices and it is not shown here. It should be mentioned that after start-up, the circuit is disabled and powered down. Therefore, we do not need to consider it for the purpose of power consumption calculations.

Control Logic

The control logic for the outer digital system is fully described in this chapter. It can be easily implemented with static CMOS logic blocks available for the process. With the exception of the clock counters, latches associated with the detect clamp output signals, it is an entirely clocked sequential circuit. Flip-flops are used to regulate the timing of each step during the slow switching MIMCAP cells.

4.5 Test Environment

The buffer was simulated in an open loop configuration. Figure 4-10 shows the test setup. Most accessory circuits are modeled with the least number of components possible as to speed the overall simulation while maintaining a reasonable level of approximation.

Figure 4-11 shows the circuit model for the buffer delivering the input clock signal to the resonant buffer in the actual CDR design. The output from the clock buffer
is delivered to a model of the HRBB phase detector (figures 4-12-4-15), which is in turn supplied with a pseudo-random sequence for its data inputs.

Even in the absence of any control structures within the resonant buffer (with the exception of the AGC circuits), the simulation is extremely stiff, with coexisting time constants that vary from the clock period to the tens of microseconds. It was only thanks to Analog Devices computing network (which takes advantage of unused computation power of all personal workstations) that a complete set of simulations could be run.

Particular attention was given to ensure that, under the series of algorithms described in this chapter, the resonant buffer has enough dynamic range to deliver output clocks in relative quadrature to the HRBB phase detector. Simulations were run for a permutation of all process, input clock frequencies and temperature corners, as well as for all possible switching combinations of MIMCAP cells and for all capacitance dynamic range corners of the varactor cells. The results were then used to verify the behavior of the outer digital system.
Figure 4-8: Tail current of one CML buffer during a start-up sweep: $F_{\text{clock}} = 5.3 \, GHz$, NOMINAL process and ambient temperature.
Figure 4-9: Input current to a MIMCAP cell (node t) and voltage at node vsel during slow switching (nominal process and ambient temperature). Cell is turned off during the first 10 µs and is then turned back on.
Figure 4-10: Test environment for the resonant buffer.
Figure 4-11: Model for circuits delivering the input clock to the buffer.
Figure 4-12: HRBB phase detector simplified model.
Figure 4-13: latchcml2x simplified model.
Figure 4-14: latchcml1p5x simplified model.
Figure 4-15: HRBB phase detector bias tree model.
Chapter 5

Conclusions

5.1 Power Estimates

The overall run-time power consumption estimate for the resonant buffer is shown in table 5.1. The data is presented in the case of nominal and maximum power consumption. For the CML buffers and the varactor cells biasing, the data is derived from open loop simulations. For the other elements of the inner analog control loop (phase detector, charge pump and detect clamps), the values quoted are the result of estimation from similar existing circuits.

The outer digital system built with static logic has a negligible contribution to the overall power consumption at run-time.

In the power budgeting for the overall CDR system, the potential contribution of the resonant buffer is significant. The polyphase filter which is responsible, in the current design, for the generation of the two clock phases in quadrature, has a nominal power consumption of 80 $mW$. Two resistively loaded CML buffers to drive the clock inputs of the HRBB phase detector require a nominal power of 45 $mW$ (see section 1.2). The resonant buffer can replace the need for both of these circuits resulting in a net nominal power savings in excess of 100 $mW$. 
### Table 5.1: Run-time power consumption

<table>
<thead>
<tr>
<th></th>
<th>Nom.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CML buffers (x2):</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tail Current</td>
<td>5.0 mA (1.8 V)</td>
<td>14.2 mA (1.8 V)</td>
</tr>
<tr>
<td>Source followers</td>
<td>2.0 mA (1.8 V)</td>
<td>2.4 mA (1.8 V)</td>
</tr>
<tr>
<td>Others</td>
<td>0.2 mA (1.8 V)</td>
<td>0.2 mA (1.8 V)</td>
</tr>
<tr>
<td>Peak detector - AGC (x2):</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>200 µA (3.3 V)</td>
<td>280 µA (3.3 V)</td>
</tr>
<tr>
<td></td>
<td>600 µA (1.8 V)</td>
<td>840 µA (1.8 V)</td>
</tr>
<tr>
<td>Varactor cells biasing:</td>
<td>300 µA (3.3 V)</td>
<td>600 µA (3.3 V)</td>
</tr>
<tr>
<td>Inner analog control loop:</td>
<td>800 µA (3.3 V)</td>
<td>1.6 mA (3.3 V)</td>
</tr>
<tr>
<td>Outer digital system:</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TOTAL</td>
<td>18.3 mW</td>
<td>39.9 mW</td>
</tr>
</tbody>
</table>

In the case where the resonant buffer were used in open loop in conjunction with the polyphase filter (therefore, functioning as a power-efficient replacement of the resistively loaded CML buffers), the overall power savings are limited to a range of 15 – 20 mW. It should be noted that, in this case, the tail currents of the buffers are reduced by a factor of $\sqrt{2}$ because of the different tuning of the resonant structures when quadrature generation is not required.

#### 5.2 Delivered Quadrature Accuracy

The accuracy of quadrature delivery at the output of the resonant buffer depends on the mode of operation.

If the resonant buffer is used to generate quadrature and the full control architecture described in this thesis is implemented, quadrature accuracy depends entirely on the performance of the inner analog control loop phase detector. Using the assumptions of section 4.1.1, the expected contribution to quadrature error from the resonant buffer is 3.3 degrees (95% confidence interval). Occasionally, this error can increase by about 4.3 degrees for 2 µs when MIMCAP switching is required at run-time.
If quadrature generation is not required and the resonant buffer is operated in open loop, then the accuracy of quadrature delivery depends on the physical matching of the two channels. As discussed in appendix B, the expected contribution to quadrature error from the resonant buffer is 2.5 degrees (95% confidence interval)\textsuperscript{1}.

5.3 Future Work

In order to reach full implementation of the resonant buffers, the following steps are required. The circuit design of all element of the control architecture must be completed. Layout and consequent re-verification of the design with parasitic data must take place.

5.4 Final Conclusions

This thesis shows how a resonant buffer can successfully be used to increase power performance in CDR applications for which concurrent drive of large capacitive loads and generation of two clock phases in quadrature is needed. This architecture can be transparently integrated in an existing design, thanks to the high jitter bandwidth of the resonant structures being used.

\textsuperscript{1}Note that this value is calculated assuming a resonant structure quality factor of 10.
Appendix A

Analysis of Tank Behavior under Capacitive Variations

A.1 Dependence of Tank Impedance Phase on Capacitive Variations

The goal of this short derivation is to obtain an estimate of the dependence of tank
impedance phase on the capacitive load $C_{TOT}$ variations. The exact expression for
the tank impedance phase can be obtained from (2.2) and the equality $s = w_i$:

$$\angle Z_{load} = \frac{\pi}{2} - \tan^{-1}\left(\frac{Lw}{R_P - LC_{TOT} R_P w^2}\right) = \tan^{-1}\left(\frac{R_P - LC_{TOT} R_P w^2}{Lw}\right)$$  \hspace{1cm} (A.1)

Performing a linear expansion of $\angle Z_{load}$ for $C_{TOT}$ around some value $C_o$, and then
setting the frequency $w = w_n = 1/\sqrt{L C_o}$:

$$\angle Z_{tank}|_{w = w_n} \approx -\frac{R_P}{\sqrt{L C_o}} (C_{TOT} - C_o).$$ \hspace{1cm} (A.2)
Finally, considering a parallel tank for which $R_P = QLw_n$, where $Q$ is the quality factor of the tank,

$$\mathcal{L}Z_{\text{tank}}|_{w=w_n} \approx -QLw_n^2(C_{\text{TOT}} - C_o) = \frac{Q}{C_{\text{TOT}}} \Delta C.$$  \tag{A.3}

$\Delta C$ is defined as the variation in total load capacitance of the tank from the value that makes the input signal frequency $w$ and the resonance frequency $w_n$ coincide.
A.2 Dynamic Effects of Tank Capacitance Changes

This section describes the approximate dynamic response of a parallel tank when its internal capacitive load is changed.

If the tank has been connected to a sinusoidal current source of fixed frequency for a long time, the voltage response of the system should also be a sine function because the system is linear and the stimulus is an eigenfunction of the system. In other words, all particular solutions that might have been present in the system have decayed away.

In the specific case of a parallel tank, which is a second order system, any particular solution decays with a damping factor of \( \xi = \sqrt{\frac{L}{C} \frac{1}{2R}} \). This decay can be described using a similar approach to that of Appendix A.1 as a time constant:

\[
\tau_L = \frac{2Q}{w_n}. \tag{A.4}
\]

Suppose now that after a long time, the capacitive load of the tank is changed. The voltage response of the tank will now be approximately the linear combination of two elements: a decaying sine function corresponding to the input up to that point in time and a new sine function which should become the only solution once the decaying component has become negligible.

Therefore, one can conclude that the dynamic response of tank output voltage phase to changes in tank capacitance is approximately that of single left half plane pole with time constant \( \tau_L \).
Appendix B

Open-Loop Phase Mismatch

Characteristics of Resonant Buffer

This appendix looks at the potential for a set of resonant buffers operated in an open-open loop fashion (see section 2.2) to significantly contribute to the overall static quadrature error of the signal delivered to the HRBB phase-detector.

B.1 Quadrature Error Estimation

In order to estimate the potential quadrature error between the outputs of the resonant clock buffer, one has to analyze all significant sources of mismatch between the tanks. The total phase difference between the output clocks is caused by the phase contributions of all the four tanks present in the buffer, in addition to any phase contribution from the inputs. Therefore, we talk about the phase error contribution of only one tank until the end of this subsection, when we make the final considerations about the performance of the entire buffer.

Referring back to figure 2-1, the tank is composed by the following main elements: parasitic capacitance of about $0.5pF$ (divided between gate capacitance and interconnect parasitic), additional capacitance of about $0.2pF$, metal 8 inductor (ap-
prox. 1.3nH$^1$. In the resonant buffer described so far, the additional capacitance is composed only of MIMCAPs selected at start-up. It is nevertheless important to anticipate that with the use of a closed-loop control, some of the additional capacitance assigned to the MIMCAPs should be converted into MOS varactors. For this reason, I describe the expected mismatch of both MIMCAPs and MOS varactors, although in the final considerations about the need for closed-loop phase error control, I will assume an additional capacitance realized entirely with MIMCAPs.

The CDR phase detector loads each output of the current steering elements with 12 gates of 16/0.13µm NMOS transistors (with source and bulk shorted together). For these fairly wide NMOS transistors, I assume that the main contributors of $\Delta I_d$ are the mismatch of the gate lengths, of the oxide thicknesses and of the thresholds. The first of these two components are present also in the total gate capacitance mismatch. If we further assume the threshold mismatch to be small, then the gate capacitance mismatch should be, to the first order, slightly smaller than $\Delta I_d$, expressed as a fraction of the total drain current through the test transistors. Using a simple Root of Squared Sums (RSS) approximation$^2$ we can estimate the total mismatch due to the phase detector gates capacitance to be around $5fF$ out of a total of $0.25pF$.

Gate capacitance accounts for about half of the total parasitic capacitance. The remaining part is due to interconnect parasitic. Since the interconnects are not perse structures monitored at production time, I will estimate that the mismatch of their parasitic capacitance will be at least equal to that of the gates capacitance (i.e. 2.0%). It should be noted that the interconnects are much larger structures than the transistors and therefore, should be much easier to match. Nevertheless, they are not structures, specifically monitored at production time. Therefore, this guess is

---

$^1$I do not consider any other elements in this analysis since they are too small to make any relevant contribution to overall quadrature error.

$^2$The RSS approximation assumes independent Gaussian distributions for all the elements of a mismatch. Therefore, it calculates the total expected mismatch as the square root of the sum of the squares of the independent element mismatches.

$^3$All mismatches are expressed as 95% confidence intervals.
hopefully not too far from reality. In any case, the total sensitivity of the final answer on this parameter is pretty low as not to be able to change my conclusions in any major way.

In the case of MIMCAP structures and 0.1pF capacitors, the predicted mismatch is about 0.21%. This is in agreement with other data posted in the literature [6]. Nevertheless, as a cautionary note, I will report that Prof. Duane Boning of M.I.T. thinks that the MIMCAP mismatch can be much larger than reported by TSMC. Prof. Boning studies in detail semiconductor processing variations. He suggests that insulator thickness can vary from point to point on the same wafer up to 5%.

As mentioned before, MOS capacitors might also be present in the tank as part of the additional capacitance component. Assuming the use of P-type well varactors, we can extrapolate the approximate mismatch by looking at comparable size transistors. In the case of 0.2pF varactors, the predicted mismatch is 6.4fF.

This leaves the inductor for which very little data is available. Reference [9] provides some empirical formulae for the design of integrated spiral inductors. They all seem to point to the fact that the overall inductance value of the structure is rather insensitive to changes in width and thickness of individual metal stripes, insofar as the total size of the inductor remains constant (the large size of the structure suggests this is a very good assumption to make). Therefore, I assume no significant mismatch between the inductors.

The cross-sectional area of the inductor stripes does indeed effect the Q of the inductors. This has, nevertheless, little effect in terms of the overall Q of the tank, since this feature is set almost exclusively by the additional resistor $R_{L2}$ of figure 2-1, which we can assume to be closely matched within a few percentage points. Mismatches in Q have only a second order effect on the buffer quadrature error, since they only change the relationship between excess capacitance in the tank and tank phase response.
Table B.1: Summary of the predicted capacitive mismatches in the resonant buffer tanks.

### B.2 Results

The mismatches estimates of the tank capacitive components are summarized in table B.1. Once again, using the RSS approximation, the total capacitive mismatch due to a single tank is approximately $8.25fF$. If we take into account the effect of all four tanks, the approximate capacitive mismatch for the quadrature clock resonant buffer is $0.81\%$ of the total capacitive load present in the buffer.

Equation (2.3) provides a mean to estimate the total predicted quadrature error for the buffer. Table B.2 shows the results for different quality factor for the tanks. The results are shown both in degrees (on a 5GHz signal) and in percentage of the 10Ghz unit interval. The table shows also the maximum theoretical error by simply adding the relevant components of table B.1 (ignoring the assumptions about component independence of the RSS approximation).

<table>
<thead>
<tr>
<th>Tank quality factor (Q)</th>
<th>Est. tot. quad. error degrees</th>
<th>Max. tot. quad. error degrees</th>
<th>U.I.</th>
<th>U.I.</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.0</td>
<td>1.85</td>
<td>3.38</td>
<td>1.02%</td>
<td>1.86%</td>
</tr>
<tr>
<td>4.5</td>
<td>2.08</td>
<td>3.80</td>
<td>1.16%</td>
<td>2.12%</td>
</tr>
<tr>
<td>5.0</td>
<td>2.31</td>
<td>4.22</td>
<td>1.27%</td>
<td>2.32%</td>
</tr>
</tbody>
</table>

Table B.2: Quadrature error estimates for the resonant buffer, given different tank quality factor.
B.3 Conclusion

In the overall CDR design, the total allocated quadrature error at the output of the resonant clock buffer is 1.0%. This assumes the inputs of the resonant buffer do not contain any quadrature error. Nevertheless, the polyphase filter responsible for the generation of the quadrature signals is also a source of quadrature error. Therefore, considering that the estimate made in this appendix is rather conservative, it is evident that the measured quadrature error at the output of the buffer is most likely not going to meet specifications.
Appendix C

Numerical Simulation of Resonant Tank Jitter Transfer

The following code is a simulation for Mathematica 5.0 (Wolfram Research, Inc.) written originally by Larry De Vito of Analog Devices. The author contributed with a number of modification and by optimizing the code for faster running time.

The goal of the numerical simulation is to calculate the magnitude of the jitter transfer function for a given LTI filter model. While the code can be adapted to fit a wide variety of situations, the specific instance presented below tries to reproduce the predictions of Chapter 3, and, in particular, the case of tank configuration A (see figure 3-10).

The simulation follows the following general procedure for all sample jitter frequencies in the range of interest:

1. Construct the approximated frequency-domain representation of a phase-modulated signal by summation of the carrier and the first four pairs of sidebands.

2. Multiply the resulting input signal by the frequency response of the designated LTI filter, therefore approximating the frequency-domain description of the output signal.
3. Using the inverse FFT, calculate the periodic-steady-state time-domain form of the output signal.

4. Taking in consideration the rising-edge zero crossings of the output signal and the deviation ratio used in the first step, calculate jitter transfer magnitude. Jitter magnitude of the output signal is extrapolated looking at the maximum time deviation of the output zero crossings from their expected times in an unjittered signal.

Output plots for the above code are shown in figure C-1. These plots confirm the calculations used to produce the plots of figure 3-11. Furthermore, figure C-2 and C-3 show a comparison between the results of the numerical simulation presented above and the results obtained in Chapter 3 using explicit solutions to the jitter problem. The two sets of results match precisely, further corroborating the analysis of Chapter 3.
(* Initialization of graphics elements and macro definition *)

SetOptions[EngineeringForm, NumberFunction -> (If[#3 == "", ",", "e"]*#3 & )];
SetOptions[EngineeringForm, ExponentStep -> 1];

<< "Graphics'Legend";
<< "Graphics'Graphics";
<< "Graphics'MultipleListPlot"

num[x_] := PaddedForm[N[x], 3, ExponentFunction -> (If[3*Quotient[#1, 3] == 0 || #1 == -1, Null, 3*Quotient[#1, 3]] & ), NumberFormat -> (If[#3 == "", ",", "e"]*#3 & )];
p[a___, b___] := 1/(1/a + 1/b);

primefreq = {1, 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, 37, 43, 53, 61, 73, 89, 113, 149, 199, 251, 307, 401, 541, 761, 97, 1409, 1999};
dB[m_] := Transpose[{Log10., 2.*2.4441*6*primefreq, 20*Log10[10., m]}];

logticks = {{{{-20, "20", 0.03}, {0.301, "2"}, {0.4771, "3"}, {0.6021, ""}, {0.699, "5"}, {0.7781, ""}, {0.8451, ""}, {0.9031, ""}, {0.9542, ""}, {1, "ten", 0.03}, {1.301, ""}, {1.4771, ""}, {1.6021, ""}, {1.699, "5"}, {1.7781, ""}, {1.8451, ""}, {1.9031, ""}, {1.9542, ""}, {2, "hun", 0.03}, {2.301, ""}, {2.4771, ""}, {2.6021, ""}, {2.699, "5"}, {2.7781, ""}, {2.8451, ""}, {2.9031, ""}, {2.9542, ""}, {3, "1k", 0.03}}, {{-20, "20", 0.03}, {-15, "-15", 0.03}, {-10, "-10", 0.03}, {-5, "-5", 0.03}, {-3, "-3", 0.03}, {0, "zero", 0.03}, {3, "3", 0.03}, {5, "5", 0.03}, {10, "10", 0.03}, {15, "15", 0.03}, {20, "20", 0.03}, {-19, ""}, {-18, ""}, {-17, ""}, {-16, ""}, {-14, ""}, {-13, ""}, {-12, ""}, {-11, ""}, {-9, ""}, {-8, ""}, {-7, ""}, {-6, ""}, {-4, ""}, {0.5, ""}, {0, 0.005}], {1, "", 0.03}, {1.5, ""}, {0, 0.005}}, {{2, "", 0.03}, {2.5, ""}, {0, 0.005}, {-0.5, ""}, {0, 0.005}, {1, "", 0.03}, {1.5, ""}, {0, 0.005}], {-2, ""}, {0.03}, {-2.5, ""}, {0, 0.005}, {4, ""}, {6, ""}, {7, ""}, {8, ""}, {9, ""}, {11, ""}, {12, ""}, {13, ""}, {14, ""}, {16, ""}, {17, ""}, {18, ""}, {19, ""}}];
timeticks = {{{1.*-9, ""}, {2.*-9, ""}, {3.*-9, ""}, {4.*-9, ""}, {5.*-9, ""}, {6.*-9, ""}, {7.*-9, ""}, {8.*-9, ""}, {9.*-9, ""}, {1.*-8, ""}, {1.1*-8, ""}, {1.2*-8, ""}, {1.3*-8, ""}, {1.4*-8, ""}, {1.5*-8, ""}, {16ns}, {20ns}}];

interp = Compile[{prev, _Real, {nx, _Real}}, N[Abs[ArcSin[nx]]/Abs[ArcSin[prev]] + Abs[ArcSin[nx]]]];

(* Define a function to extract the jitter transfer magnitude from a given *)
(* time domain signal. The function looks only at rising edge zero crossings. *)
calcjit[signalraw_] := (signal = signalraw/((Max[signalraw] − Min[signalraw])/2);
    signdata = (NonNegative[#1] & ) /@ signal;
    statusup = MapThread[If[#1 == True && #2 == False, "up", 0] &, {signdata, RotateRight[signdata]}];
    whereup = Flatten[Position[statusup, "up"]];
    uponly = signal[whereup];
    uponlyrot = RotateRight[signal][whereup];
    intall = MapThread[interp[#1, #2] &, {uponlyrot, uponly}];
    actual = whereup − intall;
    ideal = Table[i16, {i, 0, 2047}] + 13;
    jitter = actual − ideal;
Return[((Max[jitter] - Min[jitter])/16)*Pi])

(* Set up time and frequency arrays for plotting *)

(* Carrier is 5 GHz; 16 samples per cycle; 2048 cycles in record *)
(* Time point is 12.5 ps; each freq bin is 2.44141 MHz *)
(* Modulation freq is simply multiples of bin freq *)
(* The FFT needs 2^14 freq bins in multiples of 2.44141 MHz/bin *)
(* 1/(2^15 12.5^-12) plus one point at dc *)

time = Table[t*1.25^-11, {t, 0, 32767}];
freqw = Table[I*2*Pi*(bin/(2^15*1.25^-11)), {bin, 0, 2^14}];
zip = Table[0., {bin, 1, 2^14 + 1}];

(* Construct FM signal from Bessel components and weight these *)
(* components with the tank response. *)
(* Note that the function xfr[-,-,-] requires {zip, freqw, tank[-,-]} *)

(* This is the tank of configuration (A) *)
tank[values_, freqw_] := ((r + l*#1)/(1 + c*r*#1 + c*l*#1^2) /. values &)@Flatten[freqw];

(* For a give frequency: *)
(* calculate the time domain signal using FFT, then extract the jitter *)
(* information. Then calculate the jitter transfer magnitude. *)

xfr[values_, freqmod_, dr_] := (whereSB = (If[NonNegative[2049 - #1], {2049 - #1}, {Abs[2047 - #1]}] & )/@
{0, -freqmod, freqmod, -2*freqmod, 2*freqmod, -3*freqmod, 3*freqmod, -4*freqmod, 4*freqmod};
weightedbess = {BesselJ[0, dr], BesselJ[1, dr], -BesselJ[1, dr], BesselJ[2, dr], BesselJ[2, dr], BesselJ[3, dr], -BesselJ[3, dr], BesselJ[4, dr],
BesselJ[4, dr]}*tank[values, freqw[[Flatten[whereSB]]]]; firsthalf = ReplacePart[zip, weightedbess, whereSB, Table[{i}, {i, 9}]]; secondhalf = Conjugate[Reverse[Take[firsthalf, {2, 2^14}]]];
whole = Flatten[Append[firsthalf, secondhalf]]; fmfilt = Re[Chop[InverseFourier[whole, FourierParameters -> {1, -1}], 10^-20]]; Return[calcjit[fmfilt]/dr];

(* Repeat for all frequency of interest to create plot *)
(* The deviation ratio is implicitly introduced here as 0.1. *)

transfer[values_] := (Return[Table[xfr[values, primefreq[[freq]], 0.1], {freq, 1, Length[primefreq]}];])

(* Sample values and plots *)
a0q5 = transfer[{1 -> 1.*^-9, c -> 9.73^-13, r -> 6.41}];
a0q10 = transfer[{1 -> 1.*^-9, c -> 1.*^-12, r -> 3.16}];
ap45q5 = transfer[{1 -> 1.*^-9, c -> 7.35^-13, r -> 7.35}];
ap45q10 = transfer[{1 -> 1.*^-9, c -> 8.95^-13, r -> 3.34}];
an45q5 = transfer[{1 -> 1.*^-9, c -> 1.16^-12, r -> 5.87}];
an45q10 = transfer[{1 -> 1.*^-9, c -> 1.1^-12, r -> 3.01}];

MultipleListPlot[db[a0q5], db[a0q10], db[ap45q5], db[ap45q10],
db[an45q5], db[an45q10],
PlotLegend -> {"q=5, angle=0", "q=10, angle=0", "q=5, angle=+45",
"q=10, angle=+45", "q=5, angle=-45", "q=10, angle=-45"},
}
PlotRange -> All, GridLines -> Automatic, PlotJoined -> True,
LegendSize -> {0.5, 0.5}, LegendPosition -> {1, -0.5},
AxesLabel -> {"\![10\"x\"] Hz", "\[Alpha\] (dB)"},
LegendBorder -> None, AxesOrigin -> {Log[10., 2.44141*^6], 0};
MultipleListPlot[dB[a0q5], dB[a0q10], dB[ap45q5], dB[ap45q10],
dB[an45q5], dB[an45q10],
PlotLegend -> {"q=5, angle=0", "q=10, angle=0", "q=5, angle=+45",
"q=10, angle=+45", "q=5, angle=-45", "q=10, angle=-45"},
PlotRange -> {All, {-3, 3}}, GridLines -> Automatic, PlotJoined -> True,
LegendSize -> {0.5, 0.5}, LegendPosition -> {1, -0.5},
AxesLabel -> {"\![10\"x\"] Hz", "\[Alpha\] (dB)"},
LegendBorder -> None, AxesOrigin -> {Log[10., 2.44141*^6], 0};
Figure C-1: Simulation output: jitter transfer magnitude. Case of tank configuration A. $Q$ refers to the quality factor of the tank and $\text{angle}$ to the phase contribution given to the clock carrier.
Figure C-2: Comparison of simulation output (SIM) and results obtained in Chapter 3 (CF) for tank configuration A, Q = 5.

Figure C-3: Comparison of simulation output (SIM) and results obtained in Chapter 3 (CF) for tank configuration A, Q = 10.
Bibliography


