An Automated Bench Testing System

for Direct Current Parameters of Instrumentation Amplifiers

by

Arthur Musah

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Electrical [Computer] Science and Engineering

and Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

May 18, 2005

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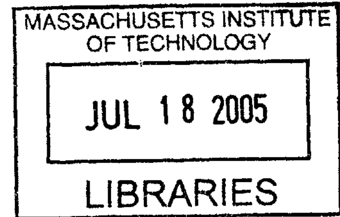

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ABSTRACT

Electrical testing is performed at multiple stages in the production of analog integrated circuits (ICs). An efficient system for low-volume IC testing is one that automates bench tests and provides good measurement precision and accuracy, while costing far less than the standard automated test equipment (ATE) used for high-volume manufacturing purposes. This thesis describes the design and implementation of an automated bench system for measuring the important direct current parameters associated with analog instrumentation amplifiers: voltage offset, input bias currents, input offset current, output swing, common mode rejection, power supply rejection, quiescent current and gain error. The system is developed on the PXI platform and consists of measurement and signal generating hardware modules, a Windows-based computer, a resource printed circuit board (PCB), a test-configuration PCB and LabVIEW-based software. The system is versatile and supports the testing of different instrumentation amplifier types and pin-outs. The performance of the system is characterized with respect to ATE results for the Texas Instruments instrumentation amplifier INA126.

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Chapter 1 Introduction

1.1 Motivation for an Automated Bench Testing System

Electrical testing is a routine and essential task performed at multiple stages in the production of integrated circuits (ICs). Manufacturing involves the probing of individual dies for critical electrical parameters at the wafer stage. This probing permits the manufacturer to monitor yields and to avoid wasting assembly time on bad die. In later stages of manufacturing, when the ICs have been assembled into packages, a final test of select electrical parameters is usually performed again in order to ensure that only devices that meet product data sheet specifications are shipped out. Outside manufacturing, engineers need to be able to electrically test ICs for the purposes of investigating device failures or for the qualification of new integrated circuit products. It is in this other kind of testing, which usually involves a few rounds of testing some tens or hundreds of units, that a need arises for a custom testing solution.

Automatic test equipment (ATE) used by semiconductor manufacturers to test packaged ICs before delivering them to customers costs hundreds of thousands of dollars to acquire and is expensive to operate. Therefore, the available automatic test resources within a company are typically limited and are utilized for a broad range of testing tasks, from manufacturing to product development and product support. Manufacturing purposes generally make fuller use of the features and high-speed functionality of ATE, and have the highest priority for test time on the ATE. Product development, characterization, qualification and support take lower priority. Often, the lower priority non-manufacturing tasks need only to be able to test low volumes of ICs and therefore do not need the high throughput demanded by manufacturing. The expensive high-speed capability of the test equipment is therefore superfluous in non-manufacturing testing.

Bench tests are often employed by engineers when only a few devices need to be tested as part of non-manufacturing tasks. Bench testing is generally a makeshift, highly adaptable setup at an electrical bench equipped with a standard set of tools: an oscilloscope, a multimeter, voltage sources, perhaps a bread board or some simple frequently used circuitry implemented on a printed circuit board, passive and active

devices, etc. Bench testing involves manually setting up the test conditions for the device to be tested, applying the inputs, measuring some outputs, perhaps doing a few quick calculations and recording the data obtained. It is a quick avenue available for an electrical engineering probing a problem and is an extremely versatile and therefore useful method of performing electrical tests.

However, as the number of devices increases from two to a few tens to some hundreds, the need for automation of the testing arises. At this point an automated test system that provides acceptable trade-offs in speed and versatility for a gain in affordability and suitability becomes very attractive. Marrying the most suitable ideas from the two extremes of ATE and bench testing, one comes up with the concept of the automated bench testing system.

This thesis is concerned with the design, building and characterization of an automated bench testing system for measuring the properties of instrumentation amplifiers from Texas Instruments Incorporated. The overarching objective for the successful implementation of the system was to have the capability of measuring the DC parameters of a broad range of instrumentation amplifier types at speeds lower than those obtained from ATE but with comparable accuracy.

1.2 Previous Work

A precise and accurate automated bench system for measuring the direct current parameters of operational amplifiers has previously been implemented. [1] Although the operational amplifier (op-amp) system measures parameters similar to those of instrumentation amplifiers, the circuitry and resources necessary for performing the instrumentation amplifier tests are different and demand the implementation of a unique solution. The PXI hardware platform and the LabVIEW software development environment used in the op-amp solution are also employed in the new test system implemented herein for instrumentation amplifiers.

1.3 Instrumentation Amplifiers

Instrumentation amplifiers are electrical devices that perform amplification of differential input signals to a high degree of accuracy. Instrumentation amplifiers are also characterized by their ability to reject common mode input signals very effectively. As a consequence of these two key properties instrumentation amplifiers can be used to measure very small differential voltages to a high degree of accuracy and are especially suitable for instrumentation applications, hence their name.

An instrumentation amplifier device generally has an inverting and a non-inverting input pin, two power supply pins, two pins across which a gain-setting resistor can be connected, an output pin and an output reference pin. This functional model of an instrumentation amplifier is represented in Figure 1.

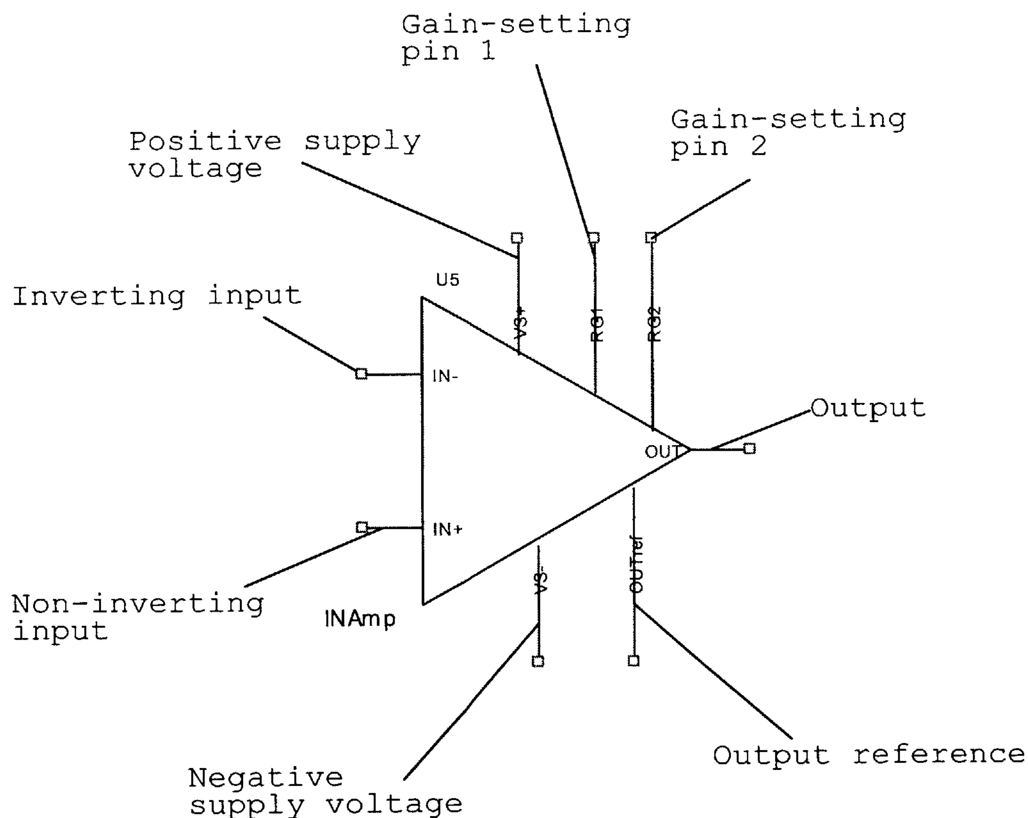

Figure 1. The functional model of an instrumentation amplifier.

Different internal architectures or topologies exist for integrated circuit instrumentation amplifiers, but all consist of networks of op-amp building blocks and high-precision resistors. Instrumentation amplifiers are distinctly different from op-amps because feedback is often implemented internally in the former. The most common types are the difference amplifier, the two op-amp instrumentation amplifier and the three op-amp instrumentation amplifier [2].

The difference amplifier type instrumentation amplifier is shown in Figure 2. This consists of one op-amp with high-precision resistors. The feedback and input resistor combination R2 and R1 determine the amplifier gain. Occasionally, the end of R2 connected to the output is left unwired and brought out as a separate pin for the user to connect directly to the output for the default gain or via an extra resistor to change the gain. An example of a TI instrumentation amplifier with this topology is the INA132.

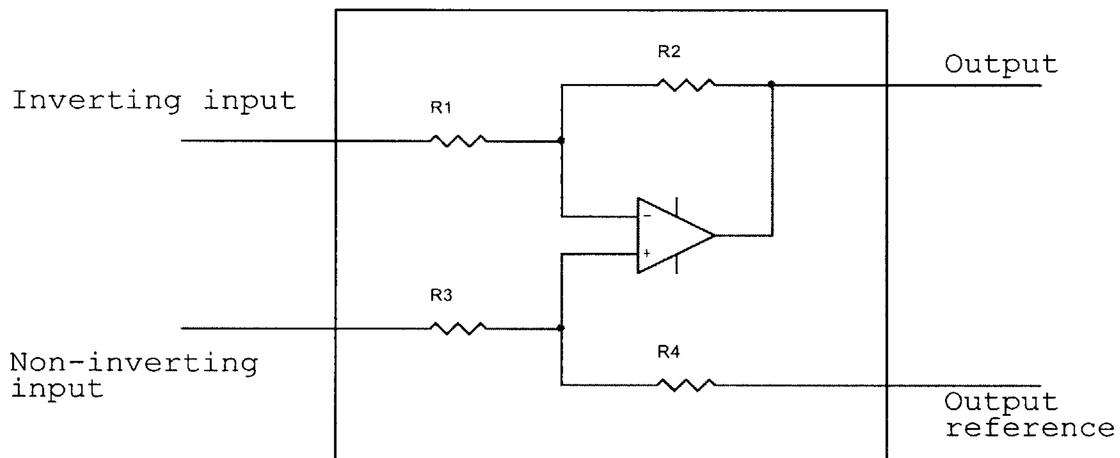

Figure 2. The internal topology of a "difference amp" type instrumentation amplifier.

The three op-amp instrumentation amplifier has three op-amps and precision resistors connected as shown in Figure 3. An example of at TI device with this topology is the INA128 instrumentation amplifier.

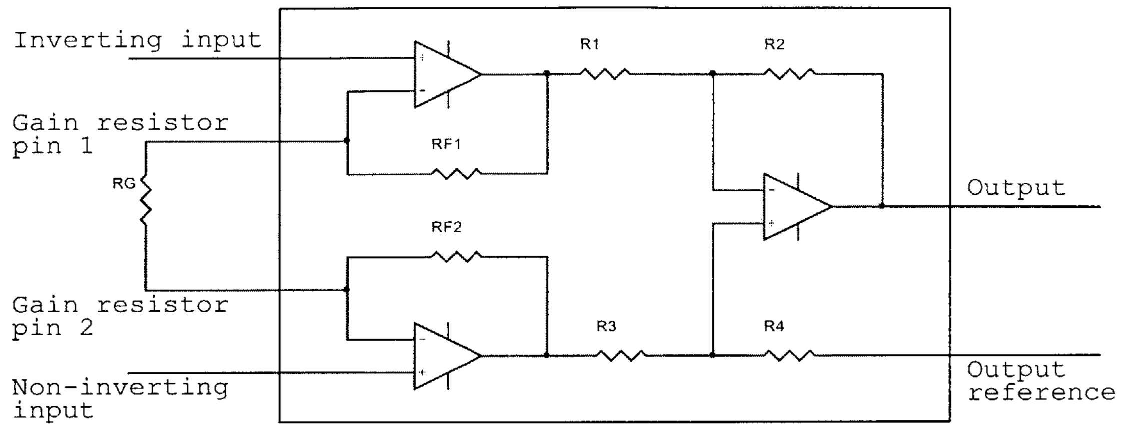

Figure 3. The internal topology of the "3 op-amp" type instrumentation amplifier.

Figure 4 shows the two-op-amp instrumentation amplifier topology, which is used in the TI device INA126.

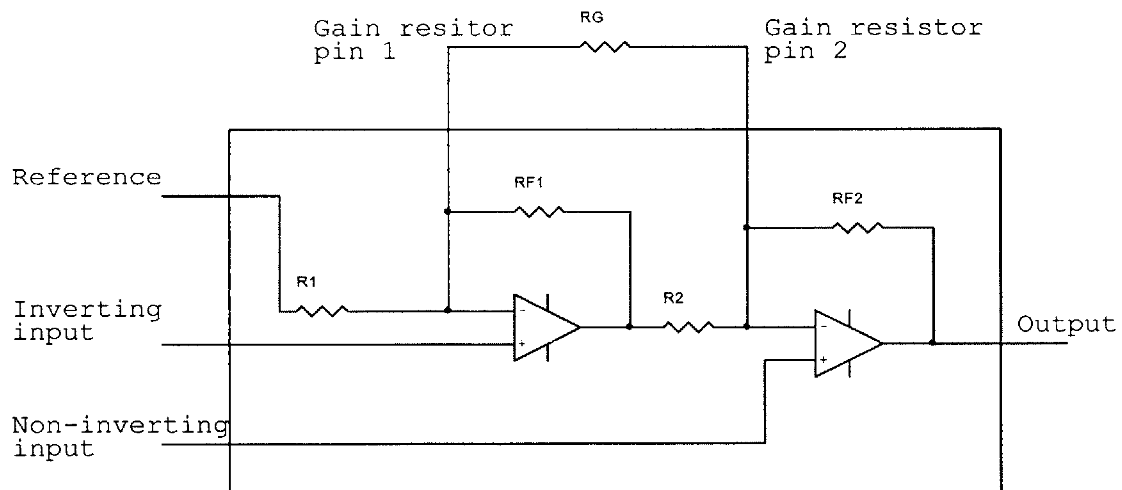

Figure 4. The internal topology of the "2 op-amp" type instrumentation amplifier.

1.3.1 The Ideal Instrumentation Amplifier

A perfect instrumentation amplifier has no offset voltage at its inputs. Consequently, it has a zero voltage output when the same voltage is applied to both of its

inputs. This characteristic is constant over its entire specified power supply voltage and common mode input voltage ranges. It draws no current from its supplies when it is not loaded, and no current flows into or out of its inputs. Its gain is perfectly linear and accurately defined by a characteristic gain equation. Its output voltage is capable of rising as high as the positive power supply voltage and dropping as low as the negative supply voltage.

In reality, however, the above properties do not hold. Quantification of the limitations of the above mentioned properties in a real amplifier give rise to the parameters defined in the next section.

1.3.2 The Real Instrumentation Amplifier

The parameters measured by the AutoBench system are frequently referred to as the direct current (DC) parameters of an instrumentation amplifier. They are so called because their measurement involves direct current inputs and outputs. Typically, most of the parameters specified in the manufacturer's data sheet for an instrumentation amplifier are DC parameters. [3]

The bench system's functionality was restricted to the DC parameters because these are the most frequently measured parameters in development, qualification and support related testing of instrumentation amplifiers. Supporting less frequently used AC parameters such as amplifier bandwidth and slew rate would have increased the complexity of the bench testing system without commensurately improving the system's utility.

The AutoBench system was designed to be capable of measuring the following DC parameters: input offset voltage, input bias and offset currents, power supply rejection, quiescent current, common mode rejection, output swing and gain error.

1.3.2.1 Input Offset Voltage (VOS)

Input offset voltage (VOS) is the voltage that shows up at the output of the amplifier when the amplifier's inputs are grounded, i.e. both inputs are zero and common mode is zero. In a real instrumentation amplifier the VOS is non-ideal and is therefore not

zero as would be expected in the perfect situation. The VOS parameter gives a measure of the goodness of the amplifier, with smaller VOS being better.

1.3.2.2 Power Supply Rejection Ratio (PSRR)

The power supply rejection (PSR) is an indication of how the VOS of an instrumentation amplifier changes with respect to variations in the power supply voltages. PSRR is defined as the ratio of the change in VOS to the causative change in power supply voltages. The parameter is determined by measuring VOS, with inputs grounded, at each of the extremes of the power supply range and calculating the desired ratio. PSRR is reported in units of V/V or as PSR in units of dB.

1.3.2.3 Common Mode Rejection Ratio (CMRR)

Common mode rejection (CMR) is an indication of how the VOS of an instrumentation amplifier changes with respect to variations in the common mode voltage at the inputs of the amplifier. CMRR is defined as the ratio of the change in VOS to the causative change in common mode voltage. The parameter is determined by simultaneously connecting both inputs of the amplifier to different voltages within the acceptable range of common mode inputs defined for the device, and measuring the output voltage. Essentially this is a measure of VOS, with both inputs connected to non-zero voltages. The power supplies and all other factors are kept constant for all measurements. CMRR is reported in units of V/V or as CMR in dB.

1.3.2.4 Quiescent Current (IQ)

Quiescent current is the current drawn by the instrumentation amplifier when its output is not loaded and the inputs are both grounded. This parameter is an indication of the power consumption of the amplifier when it is not being used but its supplies are connected. It is a useful parameter to know in the design of an application that uses an instrumentation amplifier as it allows one to determine if power to the device needs to be cut off or can be left on. IQ is also a useful parameter to test if one wants to make a quick test to determine if an amplifier is functional or damaged.

1.3.2.5 Input Bias Currents (IB+ and IB-) and Input Offset Current (IOS)

The input bias current (IB) of an instrumentation amplifier is the current flowing into or out of its input. IB+ is used to denote the bias current associated with the non-inverting input of the amplifier while IB- is used to denote the bias current associated with the inverting input. The sum of IB+ and IB- is the input offset current (IOS).

1.3.2.6 Output Swing (SW+ and SW-)

The output swing of an instrumentation amplifier is the specification of how close the voltage at the amplifier output can get to the amplifier's rail, i.e. the power supply voltage. Two values are specified: one for the swing to the positive rail, the positive swing (SW+), and the other for the swing to the negative rail, the negative swing (SW-).

1.3.2.7 Gain Error (GERR)

The gain error parameter is a measure of how the actual gain of the instrumentation amplifier deviates from the ideal gain. The gain error is reported as a percentage of the expected gain derived from the amplifier's gain equation for the particular configuration of gain-setting resistors.

1.3.3 INA126P Parameter Specifications

The range of values for the supported instrumentation amplifier test parameters are shown in Table 1. [3]

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input offset voltage	VOS		+/-100	+/-250	uV
Power supply rejection	PSRR		5	15	uV/V
Common mode rejection	CMRR	83	94		dB
Quiescent current	IQ		+/-175	+/-200	uA
Input bias current	IB		-10	-25	nA
Input offset current	IOS		+/-0.5	+/-2	nA
Positive output swing	SW+	(V+)-0.9	(V+)-0.75		V
Negative output swing	SW-	(V-)+0.95	(V-)+0.8		V
Gain error	GERR		+/-0.02	+/-0.1	%

Table 1. Specifications for the direct current parameters of the INA126P amplifier.

The gain of the INA126 instrumentation amplifier is defined by Equation 1.

$$Gain = 5 + 80{,}000 / R_G$$

(Eq. 1)

R_G in Equation 1 is the value of the gain-setting resistor connected across the two gain-setting pins of the instrumentation amplifier. Therefore, the gain of the INA126 amplifier is 5 when there is no connection between the gain-setting pins since the resistance across them is infinite.

1.4 Overview of the Automated Bench System

The automated bench (AutoBench) system consists of hardware and software. The hardware is developed on the PXI platform, which allows for integration of multiple instrumentation devices into a system controlled by a desktop computer. Two printed circuit boards (PCBs) are designed for the system. A Resource PCB is used to provide a compact and organized interface to the bulky resources and the many cables of the PXI devices. A Test Configuration PCB mounts on top of the Resource PCB and implements the circuits needed for testing instrumentation amplifiers. The hardware is designed for versatility and the Resource Board interface allows for test solutions for other device families to be developed on the system.

Software is developed in the LabVIEW graphical programming environment, which is especially conducive for PXI platform development due to the availability of device support. An overview of the system is shown in Figure 5.

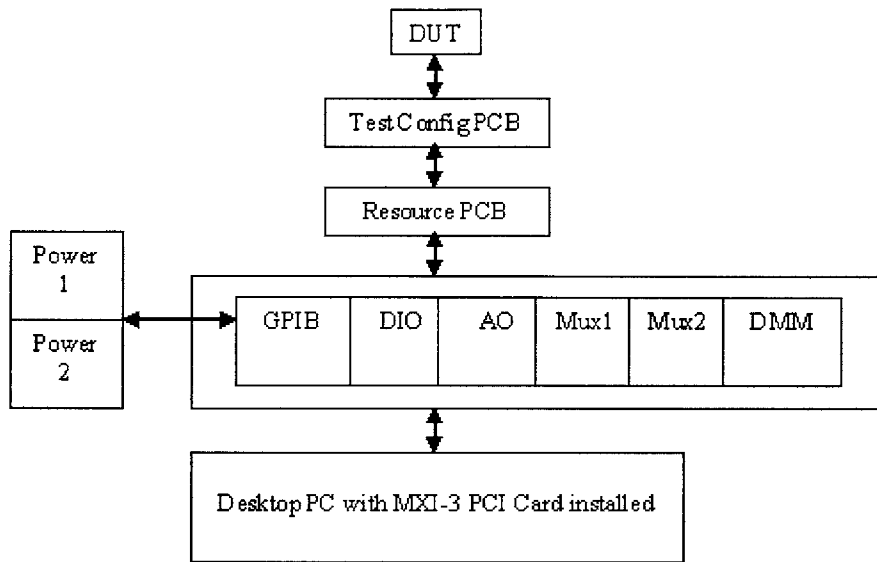

Figure 5. Connections between components of the AutoBench system indicate signal or information flows.

Chapter 2 Test Methods for DC Parameters

The procedure for measuring a parameter generally involves the configuration of appropriate gain and load, the selection of inputs to the DUT, the selection of the DUT channel being tested, the conditioning and reading of outputs, and the calculation of the parameter value. The methods used to measure each of the parameters above are described in the following subsections.

2.1 Measuring VOS

The VOS is measured on the AutoBench system by grounding both inputs of the DUT, powering the DUT, and taking a reading of the voltage at the output. The DUT gain and load resistances are configured as necessary for the device being tested. The output reference pin of the DUT is at ground. Due to the small (usually microvolt) value of the VOS, the output voltage at the DUT is gained up with the programmable gain amplifier- (PGA-) based amplification circuitry before being read with the digital multimeter. The setup for the measurement is shown in Figure 6. The voltage reading obtained in this first step of the VOS measurement is named VoutA and its value is given by Equation 2.

Errors are introduced in the VOS value of the DUT by the offset voltages of the devices in the gaining up stage. Therefore an extra reading is obtained with the PGA-based amplifier inputs connected to ground as shown in Figure 7. This second reading, named VoutB, has a value defined by Equation 3. The two readings are used to derive an accurate value for the DUT VOS in software by using Equation 4.

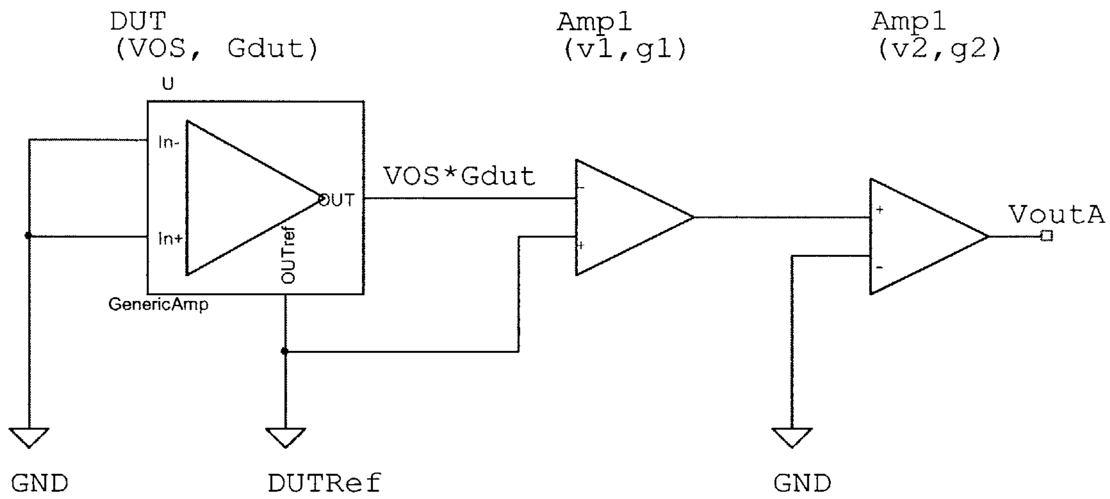

Figure 6. The first step of the test configuration used to measure VOS.

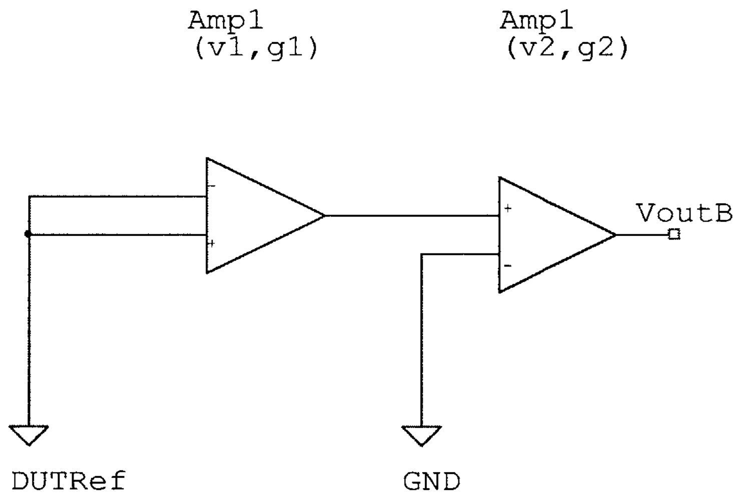

Figure 7. The second step of the VOS measurement is a reading of the error contributed by the output amplification circuitry.

$$VoutA = -VOS \cdot G_{DUT} \cdot g1 \cdot g2 + v1 \cdot g1 \cdot g2 + v2 \cdot g2$$

(Eq. 2)

$$VoutB = v1 \cdot g1 \cdot g2 + v2 \cdot g2 = Verr$$

(Eq. 3)

$$VOS = \frac{VoutA - VoutB}{-1 \cdot G_{DUT} \cdot g1 \cdot g2}$$

(Eq. 4)

2.2 Measuring PSRR

Power supply rejection ratio (PSRR) is an indication of how the VOS of an instrumentation amplifier changes with respect to changes in the power supply voltages. Therefore, it is determined by varying the power supply voltages across the extremes of the specified supply range and determining the resulting variation in the VOS.

The DUT gain and load resistances are configured as necessary for the device being tested. The inputs are grounded as in the VOS test. The smallest supply range, VSrange1, is applied to the DUT supply pins and the voltage at the output of the amplifier is measured as V1. Then the largest supply range is applied to the DUT supply pins and the voltage at the output of the amplifier is measured as V2. PSRR is then calculated as the ratio of the difference in the output voltages measured to the difference in the supply voltage ranges applied, as in Equation 5.

There is no need for a separate error voltage reading in the PSRR determination. The error voltages introduced by the amplification circuitry stay the same for the two output voltage readings and get eliminated in the subtraction.

$$PSRR = \left(\frac{V2 - V1}{VSrange2 - VSrange1} \right) \times \left(-\frac{1}{G_{DUT} \cdot G_{PGA}} \right)$$

(Eq. 5)

2.3 Measuring CMRR

The common mode rejection parameter indicates how the amplifier's VOS changes with respect to variations in the common mode voltage. In measuring this

parameter, the CMR of the amplifier is assumed to be approximately linear and a reading of the VOS is taken at two common mode voltages at the DUT inputs.

The common mode rejection test can be done either with the DUT inputs connected together and therefore at the exact same common mode voltage, or with the DUT inputs connected across a source imbalance resistance or capacitor and resistor pair. The latter option allows for the CMRR test to be done in a manner that simulates a real-world situation where the impedances of the sources connected to the DUT inputs are often not equal. The data sheets for instrumentation amplifiers usually specify a source imbalance value; therefore inclusion of support for a CMRR test with source imbalance was seen to be useful.

In the first type of CMRR test, the common mode voltage is applied to the two DUT inputs directly since they are connected together. In the second type of CMRR test, the common mode voltage is applied to one DUT input directly and to the other DUT input across the source imbalance. The results are generally similar.

To perform the test, the DUT is placed in the desired gain-setting and load configurations. The DUT is powered. A common mode voltage (VINlo) in the negative common mode voltage range is applied to the inputs and the corresponding output voltage, VOUTlo, is measured. A second common mode voltage (VINhi), this time in the positive common mode voltage range, is applied to the DUT inputs and the corresponding output voltage, VOUThi, is measured. The output voltage measurements are taken by the digital multimeter after amplification of the voltages by the PGA-based amplifier. The CMRR is determined by calculating the ratio of the difference in output voltages to the difference in common mode input voltages and compensating for the gains of the DUT and the amplification circuitry. This ratio is shown in Equation 6. As with the PSRR test, there is no need to perform a separate error measurement for the amplification circuitry as these errors get eliminated in the subtractions.

$$CMRR = \left(\frac{VOUThi - VOUTlo}{VINhi - VINlo} \right) \times \left(\frac{1}{G_{DUT} \cdot G_{PGA}} \right)$$

(Eq. 6)

2.4 Measuring IQ

IQ is the current an amplifier draws when its output is not loaded. For this test the DUT supply voltage (VS) is supplied from the power supply unit through a high-current high-voltage operational amplifier buffer with a small known resistance, R, at its output. The voltage after the resistor, labeled DUT VS in the Figure 8, is what is applied to the supply pin on the DUT.

The current is determined by measuring the voltage across the known resistance R, and applying a simple Ohm's law calculation. In addition, an empty socket current value is subtracted from the current value obtained to compensate for the leakage current of this setup. The empty socket current value is determined prior to the parameter test by performing an IQ test with the DUT socket empty.

The potential difference across the known resistance R is determined by applying the voltage at the two ends of the resistor to the inputs of a difference amplifier. The difference amplifier (INA145) has a much higher common mode voltage range (+/-28V) than the other amplification devices and accurately measures the differential voltage at its inputs, i.e. the potential drop across R. The PXI signal multiplexer module is then used to channel the output voltage of the difference-amplifier to the digital multimeter which reads the voltage. The software adjusts for the gain of the difference amplifier (statically configured to 101) and calculates the current according to Equation 7.

This IQ derivation procedure is performed in turn for the negative and positive DUT supplies in order to obtain readings for IQ- and IQ+ respectively. The other DUT supply pin is driven through the buffer normally while the complementary supply pin's IQ value is being determined.

$$IQ = \left(\frac{V1 - V2}{R} \times \frac{1}{G_{AMP}} \right) - IQ_{emptysocket}$$

(Eq. 7)

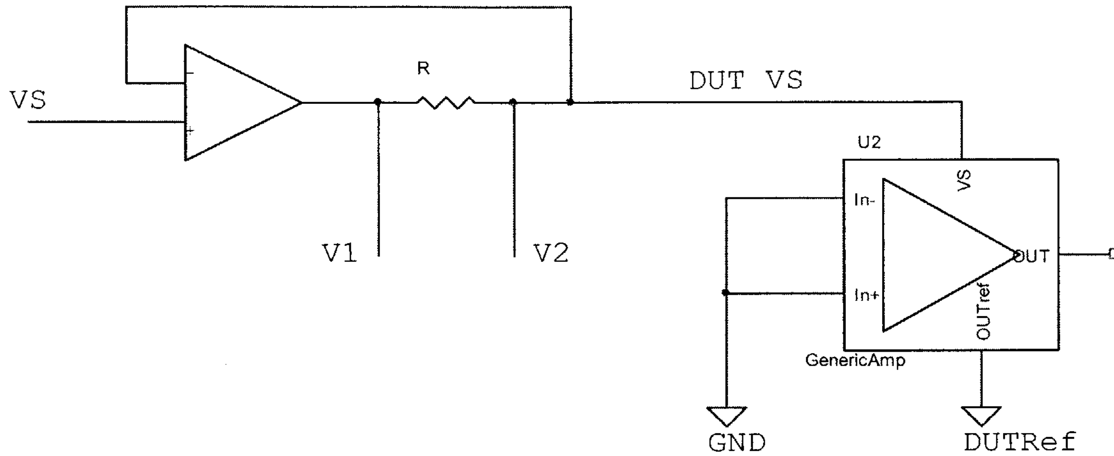

Figure 8. The test configuration for measuring IQ of an instrumentation amplifier.

2.5 Measuring IB+, IB- and IOS

The bias current for each DUT input is derived from two measurements. First, a measurement equivalent to that performed in the first VOS step is taken. The inputs to the DUT are both grounded, the DUT output voltage is gained up by the PGA-based amplifier and the voltage is read with the digital multimeter as VOUTgnd. Second, the DUT input for which the bias current is being determined is connected to ground via a 10MΩ resistor, while the other input is connected directly to ground. The DUT output voltage is again gained up and read as VOUTbias. The contribution to the DUT input offset due to the bias current on the one input is then calculated as the difference in the two output voltages measured divided by the 10MΩ resistance through which the bias current was flowing. The IB corresponding to the input under consideration is then obtained by compensating for the DUT and amplification stage gains. Again, the errors from the amplification stage are eliminated in the subtraction and do not need to explicitly accounted for in the procedure. The derivation is given by the formula in Equation 8. The setup for the IB measurements is shown in Figure 8.

$$IB = \left(\frac{VOUTgnd - VOUTbias}{10M\Omega}\right) \times \left(\frac{1}{G_{DUT} \cdot G_{AMP}}\right)$$

(Eq. 8)

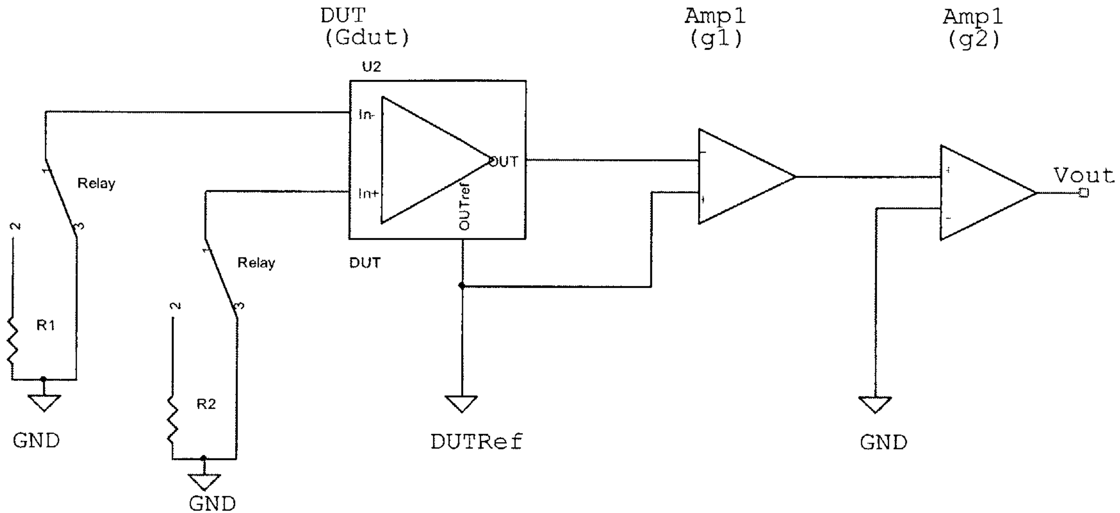

Figure 9. The configuration for measuring the bias and offset currents of an amplifier's inputs.

2.6 Measuring SW+ and SW-

The output voltage swing test involves applying a differential signal to the DUT by applying a voltage from the SEV generator to the non-inverting DUT input and grounding the inverting DUT input. The value of the differential input voltage used is the value of the power supply voltage to which the output is to be railed, attenuated by the gain of the DUT.

The output of the DUT is then compared with the appropriate supply voltage using the difference amplifier output path, which has a high common mode voltage range. The difference amplifier performs a subtraction of the supply voltage and the DUT output voltage, multiplies the result by its gain of 101 and the result is measured using the digital multimeter.

The high gain of 101 proves problematic in the testing stage of the system. Therefore the PGAmp in gain configuration 1 was used to perform a swing test at lower DUT supply voltages than the ones specified in the product data sheet.

2.7 Measuring GERR

The gain error parameter test involves the application of a zero common mode differential signal of high precision to the DUT inputs and determining how close the output voltage of the amplifier is to the voltage promised by the gain equation.

A 10V reference voltage used by the Precision Differential Voltage generator is used as the gold standard voltage to which the DUT output voltage is compared. Thus the DUT output voltage is always expected to be 10V in the GERR tests. The DUT is put into the desired gain configuration. The PDV generator is then used to provide input voltages whose difference equals the gold standard divided by twice the DUT gain. The 10V reference and the DUT output are then fed to the output amplification circuitry, where a PGA-based amplifier is used to perform a subtraction of the two signal values. To improve the accuracy of the measurement, the inputs to the amplification stage are flipped and another reading is taken. The two readings are added and divided by 2 to remove offset voltage contributions from the output amplifiers and the GERR is calculated as shown by Equation 9.

$$GERR = \left(\frac{V1 + V2}{2}\right) \times \left(-\frac{1}{G_{PGA} \cdot 100}\right)$$

(Eq. 9)

The hardware is set up as shown in Figure 6 for the first part of the VOS test, except the inputs are not grounded.

Chapter 3 System Hardware

Figure 10. The assembled instrumentation amplifier AutoBench system.

The AutoBench system hardware consists of the following components:

1. Resource Hardware
2. Test Configuration Board
3. DUT Socket Adapters
4. Desktop Computer with MXI-3 Link

A picture of the assembled test system is shown in Figure 10.

3.1 Resource Hardware

The National Instruments PXI (PCI Extensions for Instrumentation) platform provides a wide range of hardware modules that can be interfaced to a personal computer for control and automation of custom test solutions. [4] The AutoBench system was designed on this platform and consists of the following PXI modules: PXI Chassis, Digital I/O, Analog Output, Signal Multiplexers and a Digital Multimeter. In addition, two external power supplies were used to provide power to the Test Configuration Board.

3.1.1 PXI Chassis

The PXI Chassis PXI-1006 consists of a case with 18 slots for plugging in PXI hardware module cards such as the Digital I/O card and Digital Multimeter card. It provides a rugged and organized mechanical frame that protects the modules used in the test application. The chassis also supplies the various installed modules with power. [5]

3.1.2 Digital I/O Module

The PXI-6509 digital I/O (DIO) module has 96 bidirectional digital input/output lines that can be controlled individually or as byte-wide channels. No external supply is required for outputs and 5VDC reference pins are provided. [6]

The digital I/O module is used to provide digital signals to devices like the analog signal muxes, the digitally-configurable variable gain instrumentation amplifiers and the serially-configurable multiplying DAC that are used on the Test Configuration Board.

The relays on the Test Configuration Board are also controlled via output lines from the digital I/O module.

3.1.3 Analog Output Module

The PXI-6704 is a hardware module that can be used to output analog signals. The module has 16 channels for voltage capable of outputting voltages from -10V to +10V to 16-bit resolution. The module also has 16 current channels capable of sourcing up to 20mA of current, with values configurable to 16-bit resolution. [7]

The analog output module is used to supply the test voltage inputs to the DUT for the CMRR and output swing test procedures. The voltage provided by the PXI-6704 can be further amplified by a gain of 1 or 2, using a high-current, high-voltage op-amp with a relay-configurable resistive feedback path. This additional amplification option is used to provide a larger range of voltages (-20V to +20V) that can be applied as DUT inputs in performing CMRR and output swing test. The resulting resolution of the voltages available from this input path is reduced from 1mA to 2mA, but this is still adequate for CMRR and output swing tests. The larger range is useful for supporting devices whose common mode voltage and output voltage magnitudes are specified to be higher than 10V. (For example, the INA126 instrumentation amplifier used in later chapters to study the capability of the assembled AutoBench system has a minimum common mode voltage range of +/-11.25V.)

3.1.4 Signal Muxes

The PXI-2503 is an analog signal multiplexer that can be configured to operate in a 1-wire mode with 48 input channels, a 2-wire mode with 24 input channels or a 4-wire mode with 12 input channels. [8]

The AutoBench system uses two of these mux modules. One signal mux is dedicated to operating in 2-wire mode and is used for multiplexing the voltage-measuring functionality of the single digital multimeter available in the system across potential differences to be measured at multiple locations. The second signal mux is dedicated to operating in 4-wire mode and is used for to multiplex the 4-wire resistance-measuring

capability of the digital multimeter across multiple resistors that need to be precisely calibrated on the Test Configuration Board.

3.1.5 Digital Multimeter Module

The PXI-4070 is a 6 ½ digit digital multimeter capable of measuring voltages of magnitudes up to 300V and currents as large as 1A to varying resolutions. The resolution is software-configurable from 10 bits to 23-bits, depending on the range of the input signal. The multimeter is also capable of performing 2-wire and 4-wire resistance measurements. [9]

The AutoBench system makes use of the resistance and voltage measuring capabilities of the PXI-4070 to calibrate resistor values and for measuring voltages in the test procedures. The digital multimeter inputs are multiplexed to multiple signals that need to be measured by means of the PXI-2503 signal muxes. The function of the digital multimeter is determined by the control software, depending on the test being performed.

3.1.6 Power Supplies

Two Agilent E3631A power supplies are used in the AutoBench system. Each E3631A power supply has three outputs: a 6V output capable of sourcing up to 5A of current, -25V and +25V outputs with a common ground capable of sourcing up to 1A each. The 6V ground is isolated from the 25V ground. All three output channels can be configured individually. [10]

The AutoBench system makes use of the 25V power supply channels. One power supply unit is used to provide the configurable dual supplies to the device under test (DUT). The other is used to provide a +25V signal and a -25V signal to voltage regulators available on the Test Configuration Board. The voltage regulators adapt the 25V signals to +15V, -15V, +20V and -20V, which are the voltages needed to power various active devices other than the DUT on the Test Configuration Board.

3.1.7 Resource Interface Board

A printed circuit board was designed to provide an organized and compact interface to the hardware resources described above. [11] The various resource modules

are connected via cables to individual connectors on the Resource Interface Board. The footprints for the connectors and the signal traces on the Resource Interface Board are shown in Figure 11. The Resource Interface Board is mounted on standoffs, which allow the board to rest above the bench surface. The resource signals are made available on a neat interface on the top side of the board by means of two high density connectors (each with 240-pins). The Test Configuration Board was designed with complimentary connectors on its bottom side and can therefore be mounted firmly onto the neat interface on the Resource Board to have access to all the resource hardware. The printed circuit boards were designed using the Protel software.

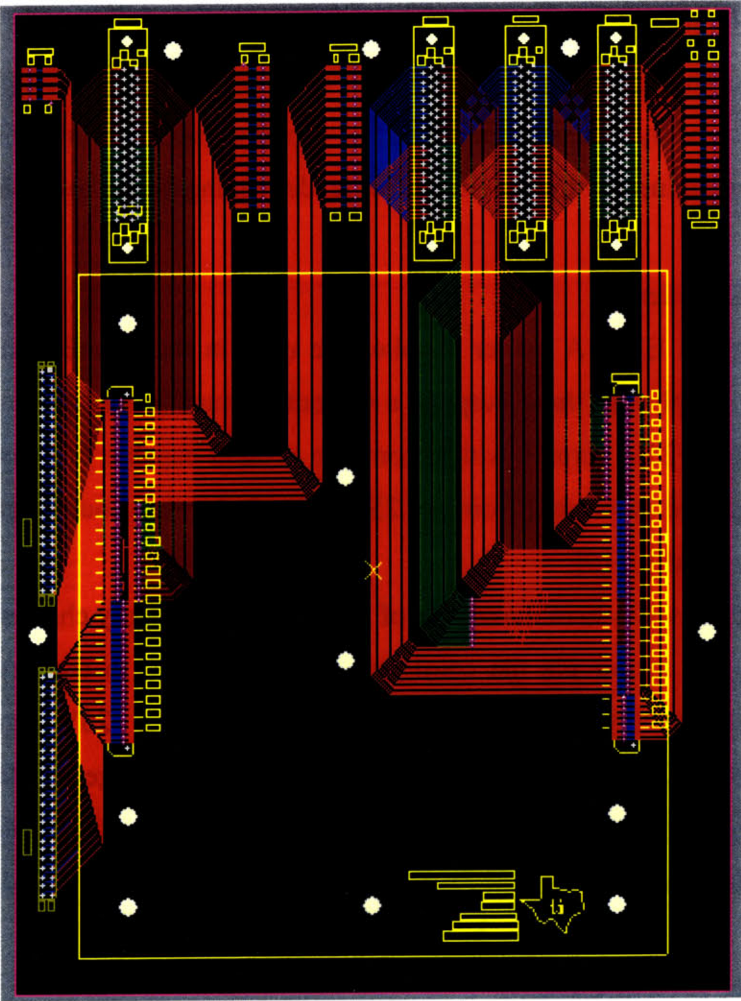

Figure 11. A PCB drawing of the Resource Interface board showing the connectors and signal traces.

3.2 Test Configuration Board

The Instrumentation Amplifier Test Configuration Board (INA-TCB) is a printed circuit board that implements the circuits needed for testing instrumentation amplifiers. The circuits implemented on this board adapt the more general resources available in the AutoBench system to the particular interface of inputs, loads, outputs and conditions necessary for performing the various parameter tests on the instrumentation amplifier. The INA-TCB consists of the following parts:

1. Resource Interface Connectors
2. Voltage Regulators
3. Input Circuitry
4. DUT Interface
5. Output Amplification Circuitry

This circuitry is implemented on a 4-layer PCB with top and bottom signal planes, an internal subdivided ground plane and an internal subdivided power plane. The two signal layers and the device footprints are shown in Figure 12. A bill of materials used on the INA-TCB is given in Table 2.

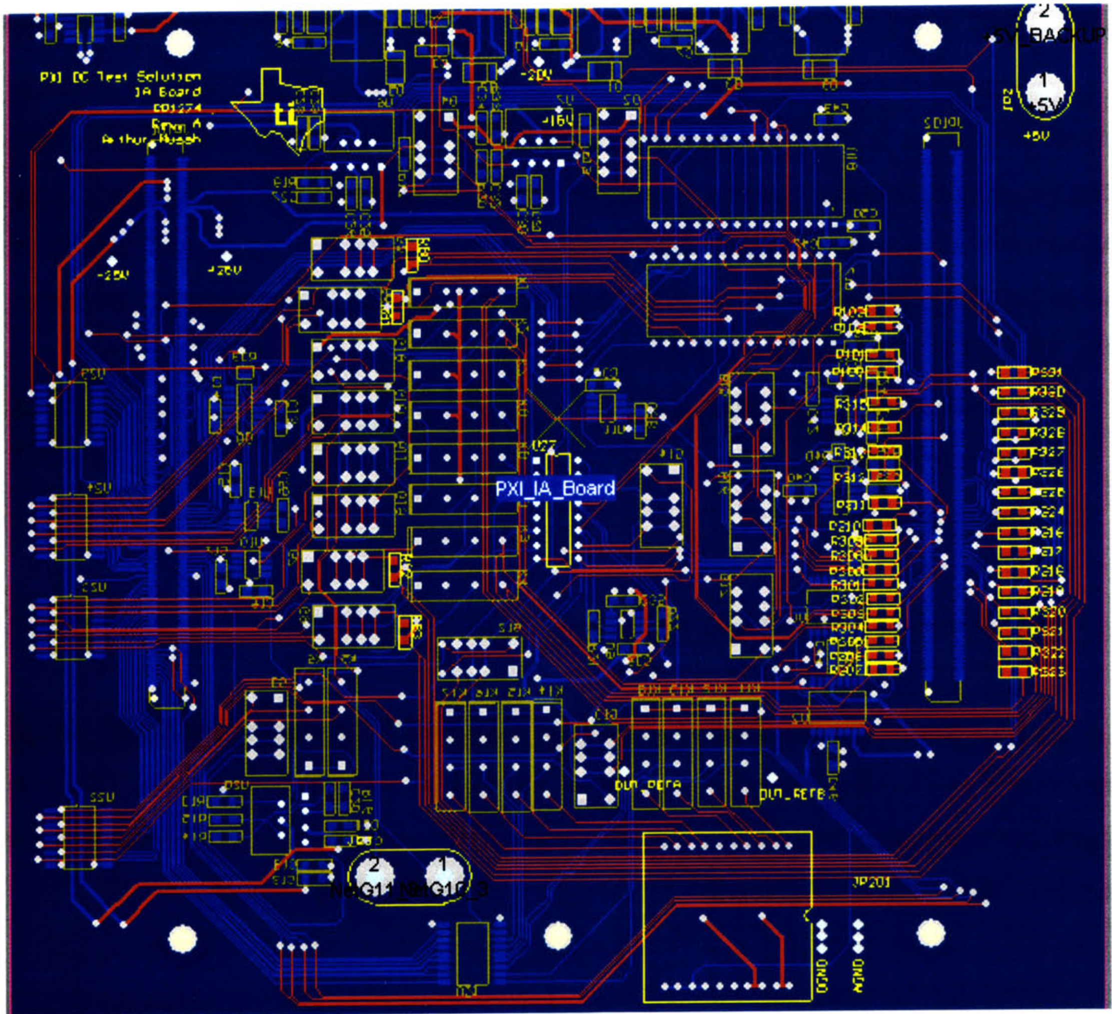

Figure 12. The PCB diagram for the INA Test Configuration Board, showing the signal layers and device footprints.

Designator	Device	Description	Company
D1 thru D9	DL4002	Diode	
G2 thru G19	TXS2-4.5	2 Form C relay	
K1 thru K18	9001-05-00	SPST relays	Coto
JP2, JP3	Mini banana plug	Header, 2-Pin	
JP101, JP102	BSE-120-01-F-D-A	Connector	Samtec
U1	PGA204	Programmable gain amplifier	TI
U2	PGA205	Programmable gain amplifier	TI
U3	INA145	Difference amplifier	TI
U4, U8	OPA4277	Quad op-amps	TI
U6, U7, U20	OPA547T	Op-amps	TI
U9	OPA2277	Dual op-amp	TI
U10	REF102	Voltage reference	TI
U11, U28	OPA277	Single op-amp	TI
U12, U14	LM317KTER	Positive voltage regulators	TI
U13, U15	LM337KTER	Negative voltage regulators	TI
U17, U18	ADG406BN	16-channel analog mux	ADI
U19	LTC1595BCS8	Multiplying DAC	LTC
U21, U22, U23, U24, U25	ULN2803A-DW	8-relay driver packs	TI
U27	16-pin socket	16-pin DUT socket	
C1, C2, C13, C14, C15, C19, C22	0.1uF	Ceramic chip capacitors	
C25, C28, C30, C33, C35, C36	0.1uF	Ceramic chip capacitors	
C37, C38, C39, C40, C41, C42	0.1uF	Ceramic chip capacitors	
C20, C27, C32	0.01uF	Ceramic chip capacitors	
C43, C44, C45, C46	1uF	Ceramic chip capacitors	
C55	100pF	Ceramic chip capacitor	
C4, C6, C8, C10, C16, C17	1uF tantalum, 25V	Polarized capacitors	
C3, C5, C7, C9	1uF tantalum, 35V	Polarized capacitors	
C18, C21, C26, C29, C31, C34	10uF tantalum	Polarized capacitors	
R1	1.82K	Resistor	
R2, R6	121R	Resistors	
R3	3.65K	Resistor	
R4, R8	243R	Resistors	
R5	1.3K	Resistor	
R7	2.67K	Resistor	
R13, R14, R23	1K, 0.1%	Resistors	
R15	2K, 0.1%	Resistor	
R16, R18, R20	200K	Resistors	
R17, R19	100R	Resistors	
R21, R22	100K, 1%	Resistors	
R24	100K, 0.1%	Resistor	
R25	10K	Resistor	
R80, R81, R82, R83	10M, 1% or better	Resistors	
R100 to R103, R300 to R331	0R	Resistor	
R39, R40	PR100-B-2	10K pair, matched to 0.1%	

Table 2. Bill of materials for the INA Test Configuration Board.

3.2.1 Resource Interface Connectors

The BTE/BSE complementary pair of high density surface mount connectors from SAMTEC is used to channel the signals available on the Resource Board to the INA-TCB. The BSE connectors are located on the INA-TCB.

3.2.2 Voltage Regulators

The parts labeled U12 through U15 in Figure 13 are voltage regulators used to adapt the +25V and -25V external power supply signals to the operating voltages required by the active devices on the INA-TCB. The LM317KTER is a positive voltage regulator; two of these are used to provide the +15V (U14) and the +20V (U12) voltages. The LM337KTER is a negative voltage regulator and is used to provide the -15V (U15) and -20V (U13) voltages.

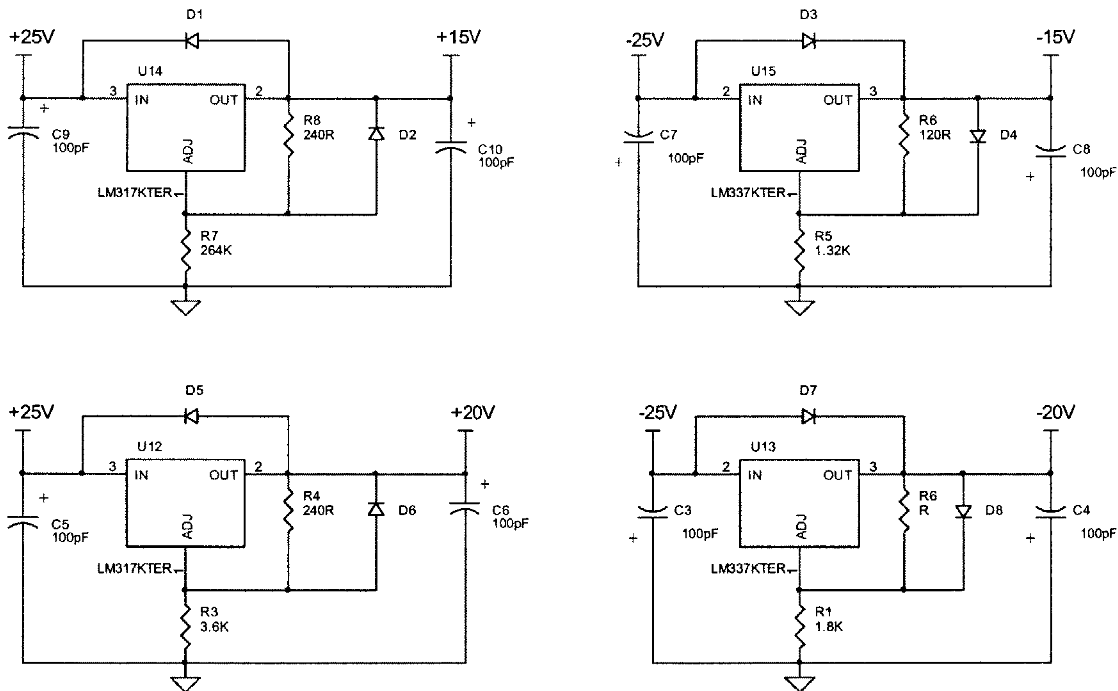

Figure 13. Voltage regulators on the INA Test Configuration Board adapt the 25V external supplies to the voltages required by the active devices on the board.

3.2.3 Input Circuitry

Different parameter tests require different resolution and range of inputs. To support the different requirement on inputs to the DUT, the following input circuitry is implemented:

1. Single-Ended Voltage Inputs
2. Precision Differential Voltage Inputs
3. Grounding Inputs
4. DUT Supply Inputs

3.2.3.1 Single-Ended Voltage Inputs

The single-ended voltage inputs path consists of a voltage channel on the Analog Output Module, the high-current high-voltage op-amp U20 with relay-selectable feedback that configures gain, and relays that allow for application of the voltage directly to the DUT inputs or across a source imbalance resistor. This system is called the SEV or Single-Ended Voltage generator and is shown in Figure 14.

This input path is used in the CMRR and SWING tests.

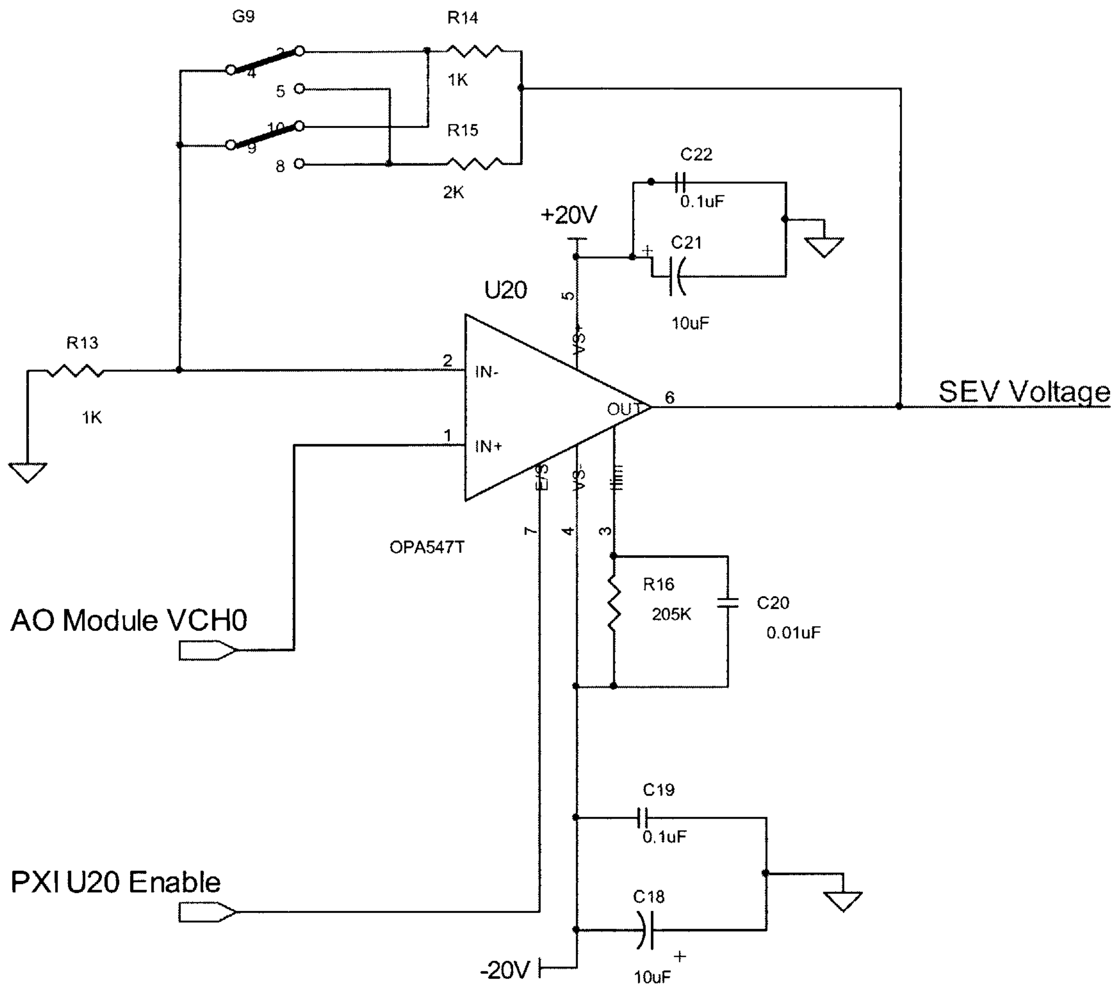

Figure 14. Voltages are generated with an Analog Output channel and amplified by a high voltage op-amp to produce the Single Ended Voltage (SEV) resource.

3.2.3.2 Precision Differential Voltage Inputs

This input path includes a 16-bit multiplying DAC (U19) with an output range of 0 to -10V, which is configurable via a serial interface through the digital I/O. This path made available for two reasons. First, to provide higher precision voltage signals. Second, to provide a differential input signal centered at 0V to the inputs of the DUT. The single-ended output of the DAC is passed through a buffer op-amp and a copy of the resulting voltage is channeled through an inverting amplifier configured to provide gain of -1. The resulting positive and negative voltages have the same magnitude and provide the differential input signals with 0 common mode that is required for tests like GERR. This

method allows for decoupling of common mode rejection limitations of the DUT from the errors due to gain nonlinearity. This input source is called the Precision Differential Voltage (PDV) generator, and is shown in Figure 15.

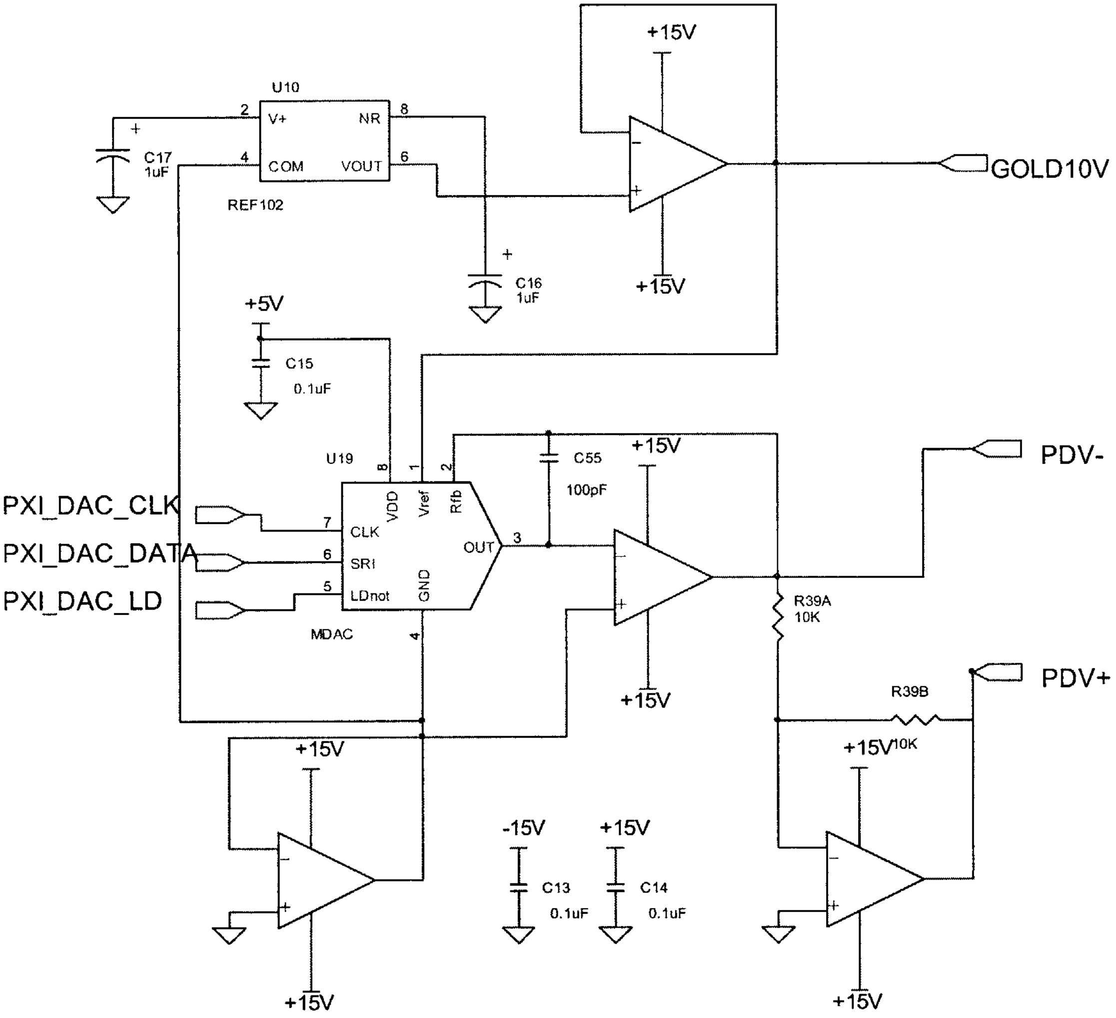

Figure 15. A 16-bit DAC is used to generate the Precision Differential Voltage, PDV, resource.

3.2.3.3 Grounding Inputs

Relays provide the ability to connect each DUT input to the ground signal either directly or through a 10MΩ resistor (resistors R80, R81, R82 and R83 in Figure16). This capability is necessary for performing the VOS, PSRR, IB and IQ tests.

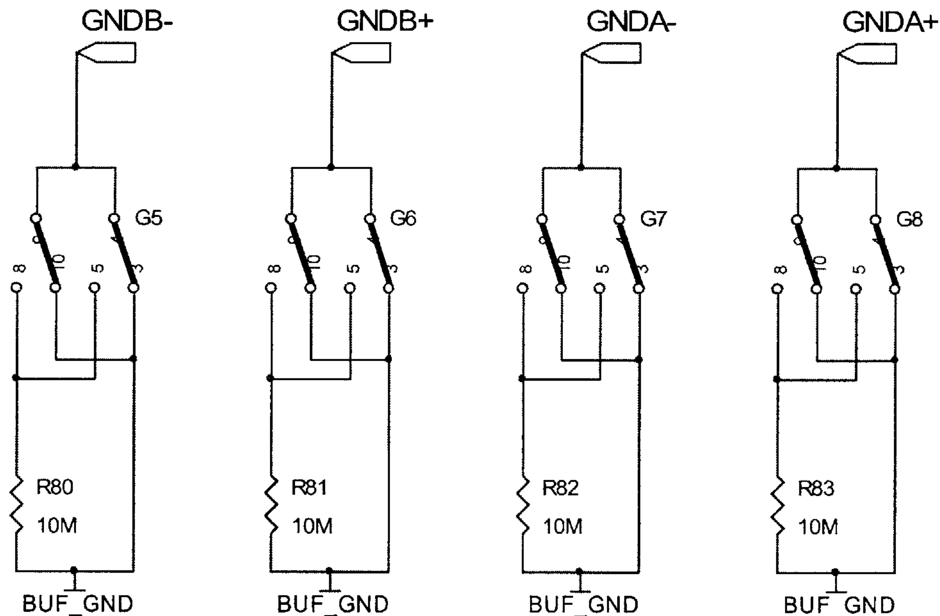

Figure 16. Direct ground paths and resistive paths to the ground signal are available for the inputs of the DUT.

3.2.3.4 DUT Supply Inputs

The DUT is powered through high-voltage high-current op-amp buffers that can be bypassed. A 100Ω resistor (R17 and R19) in series with each of the DUT power supply pins permits supply current measurement by measuring the voltage drop across the known resistances and applying Ohm's law. The circuit is shown in Figure 17.

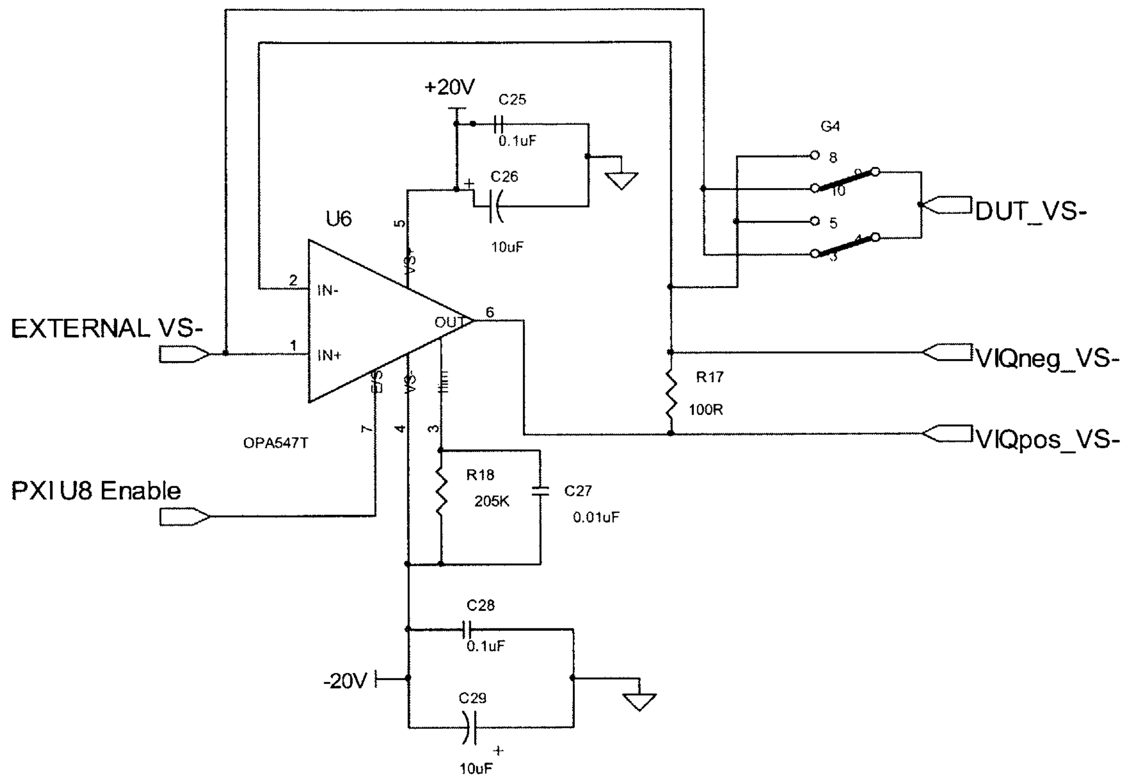

Figure 17. The DUT power is supplied through a resistor to enable measurement of the current flowing into the DUT supply pins.

3.2.4 DUT Interface

The DUT Interface consists of 16-pin connector in the middle of the INA-TCB, and provides support for the testing of both 8-pin single amplifier ICs and 16-pin dual amplifier ICs. A signal hardwired interface is presented on the INA-TCB, but this can be adapted to suit the pin-out of different instrumentation amplifiers using Socket Adapter Boards.

The DUT Interface consists of ground drivers for the DUT reference pins, gain-resistor connections, load connections, relays for selecting which amplifier channel to apply inputs and measure outputs from and the DUT socket itself. Two loads per amplifier channel are supported. Four gain resistors can be connected to both amplifier channels. The DUT Interface circuitry is shown in Figure 18.

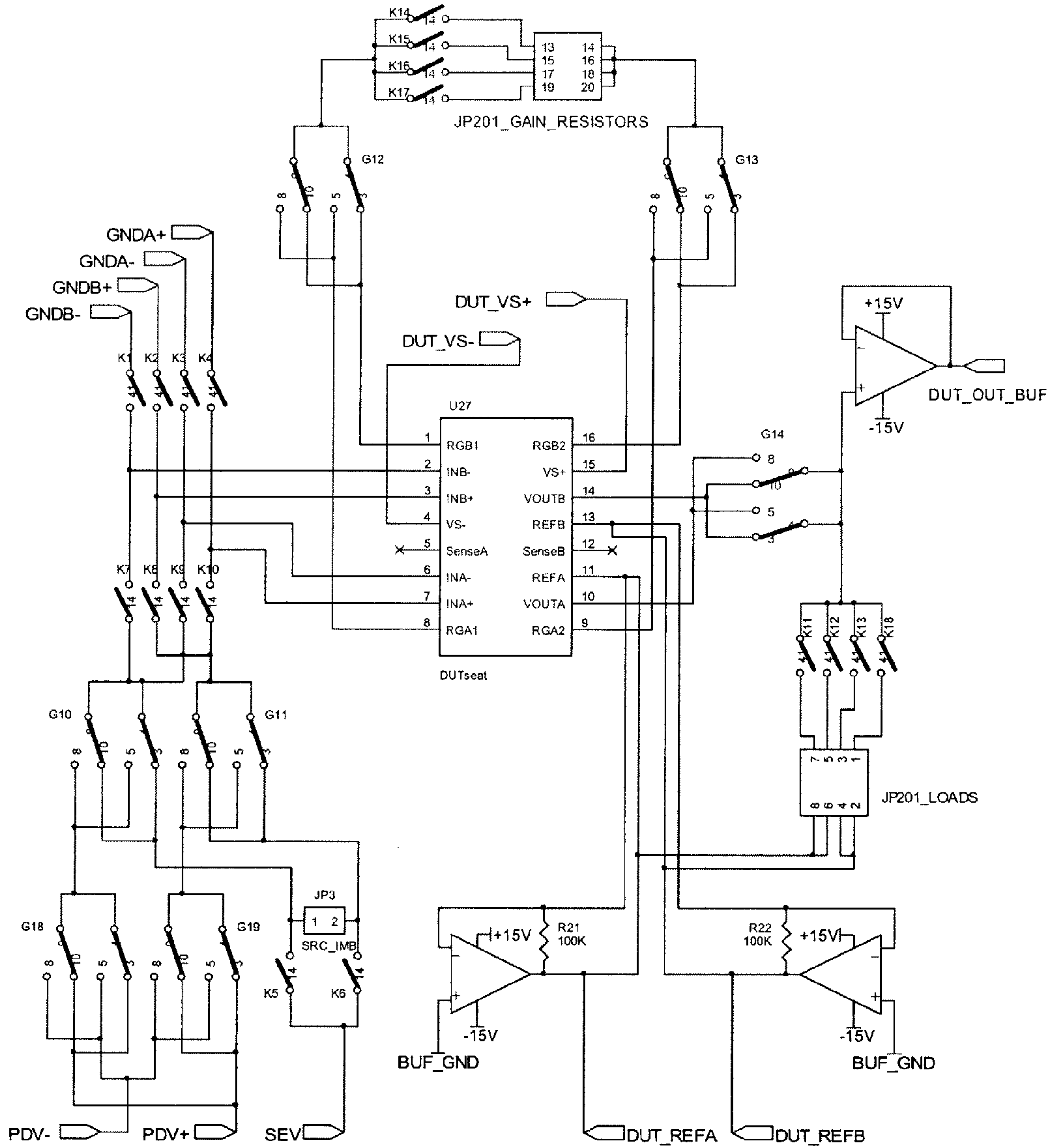

Figure 18. The DUT interface connections to multiple inputs, multiple gain-setting resistors, and multiple loads. Support for dual channel amplifier packages is included. Relays are used to swap between the possible configurations.

3.2.5 Output Measurement Circuitry

Relays are used to select the amplifier channel output that the measurements are to be taken from. A pair of 16-input analog multiplexers (muxes), U17 and U18, are used to select the signals to be passed to the measurement amplification stage. The signal selection is done via digital enable and select signals.

The amplification stage consists of three amplifier options, each with different advantages and limitations. A summing junction amplifier is implemented using the three op-amps U4A, U4B and U4C, and the resistor network consisting of R40A, R40B and R25. This option is used to perform a comparison of two voltages that are supposed to be the same, such as in the gain error test. The comparison is done by applying the two signals with opposite signs, thereby performing an amplification of their difference. The summing junction amplifier is useful for this kind of subtraction because unlike the PGA-based amplifier, it introduces little additional error from its own common mode rejection limitations. The output of the summing junction is then magnified by a known gain factor through the PGA-based amplifier and fed to the digital multimeter.

The PGA-based amplifier is a two-stage amplifier consisting of instrumentation amplifiers with digitally configurable gain that provide good gain accuracy. The first stage is a PGA204 device with gain options of 1, 10, 100 and 1000. The second stage is a PGA205 device with gain options of 1, 2, 4 and 8. In cascade, they provide gain options of 1, 2, 4, 8, 10, 20, 40, 80, 100, 200, 400, 800, 1000, 2000, 4000, and 8000. Of course, depending on the initial input signal the output of the amplifier might rail and not provide the expected gain. The PGA-cascade amplifier is used for gaining up small voltages by known factors before measuring with the digital multimeter.

Additionally, a difference amplifier statically configured in a gain of 101 is made available on the INA-TCB measurement path. Due to the high common mode voltage range of the INA145 (U3), it is used for measurements involving signals with high common modes. For example, in the output SWING tests, the DUT output is railed and the voltage obtained is compared with the relevant DUT supply voltage. It is also used in the quiescent current, IQ, tests to measure the potential difference across a known resistance through which the IQ is flowing. In these cases, the summing junction and

PGA-cascade amplifiers do not have large enough common mode voltage ranges to be useful and the difference amplifier is thus used. The circuitry is shown in Figure 19.

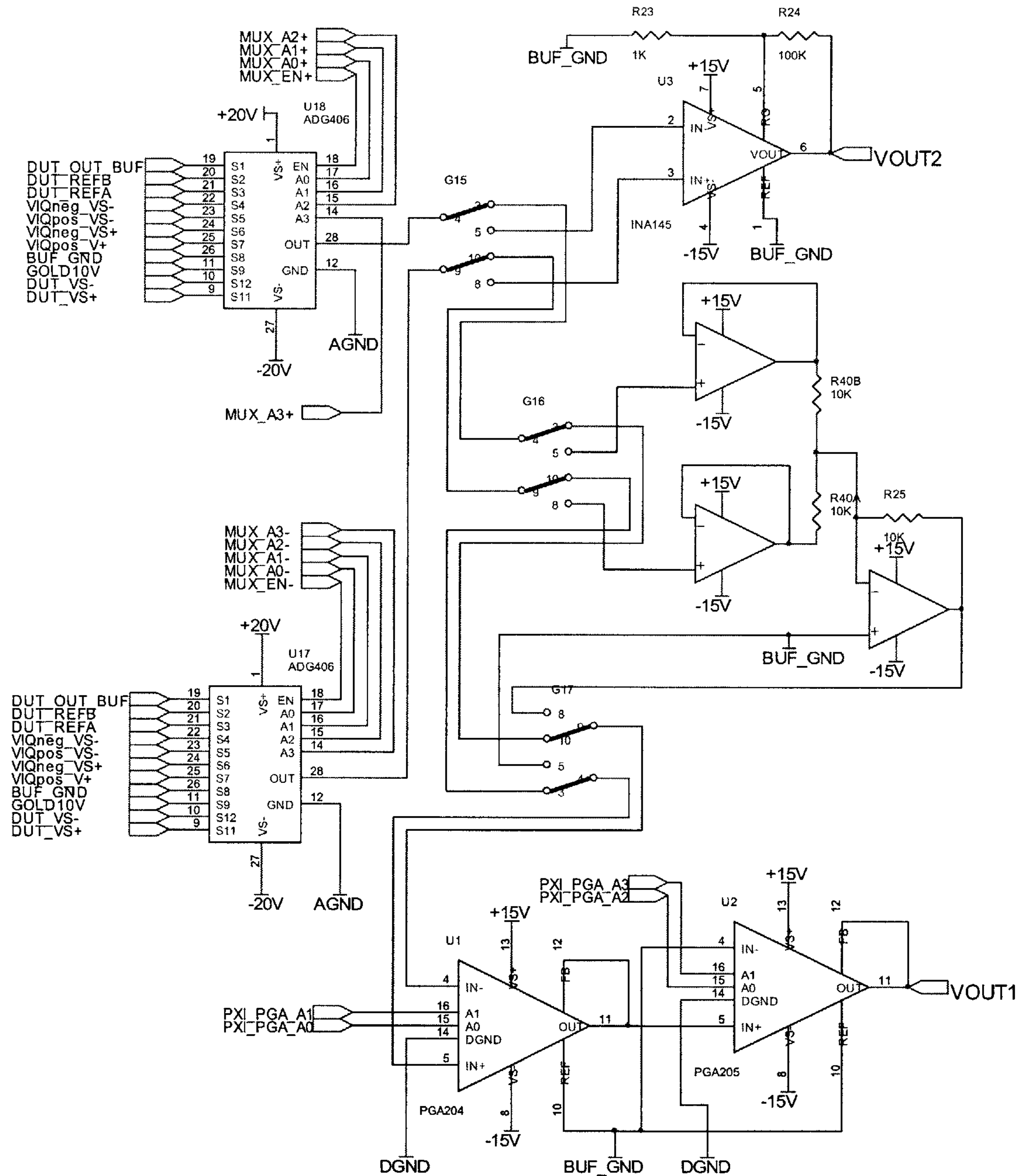

Figure 19. The output measurement circuitry includes multiple amplification paths to support signals of different characteristics. The output signals are measured differentially. Analog multiplexers are used to select the signals for the amplification stage.

3.3 DUT Socket Adapters

In order to use the fixed DUT interface available on the INA-TCB, DUT Socket Adapter boards were designed for a number of single and dual channel instrumentation amplifiers. The DUT Socket Adapter implements the rewiring necessary to make the pin-out of a particular instrumentation amplifier conform to the pin-out of the DUT interface on the INA-TCB. Figure 20 shows the Socket Adapter routing for a number of devices that could potentially be tested on the AutoBench system.

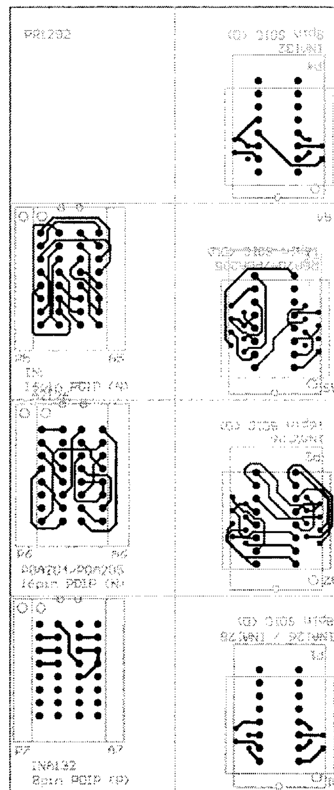

Figure 20. A PCB diagram for the DUT socket adapters.

3.4 The Desktop Computer

The desktop computer is the controller for the AutoBench system. The computer provides the processor for executing code. The computer also integrates all the resources,

stores the data and presents the system's user interface on its monitor. A Pentium 4 based desktop computer running Windows is used for the controller.

The controller computer communicates with the PXI platform resources via a high speed data bus called the MXI-3 link. The MXI-3 link consists of a card that plugs into a hardware slot in the computer frame, a card that plugs into the PXI chassis, and a cable that connects the two systems.

Chapter 4 System Software

The software for the AutoBench system was developed in the National Instruments program development environment called LabVIEW. [12] The software is written in the LabVIEW graphical programming language, by means of encapsulating functional blocks in diagrams. Each individual program is called a virtual instrument, or VI, and the programs used inside a VI are called subVIs or sub virtual instruments. A VI generally consists of a front panel view and a block diagram view. The front panel presents a graphical user interface through which a user can interact with the VI during program execution. The control diagram view provides a graphical chart of functional components and data flow in the VI. Data flows from component to component within a VI by means of diagrammatic wires between the components. The order of program execution is determined by the flow of data. An example of LabVIEW VI front panel is shown in Figure 21 and an example of a LabVIEW VI control diagram is shown in Figure 22.

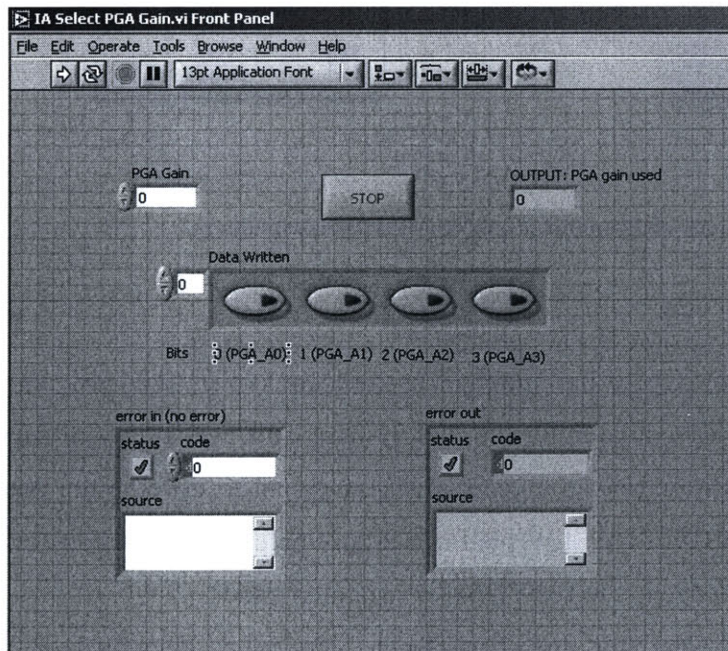

Figure 21. The front panel for a LabVIEW virtual instrument.

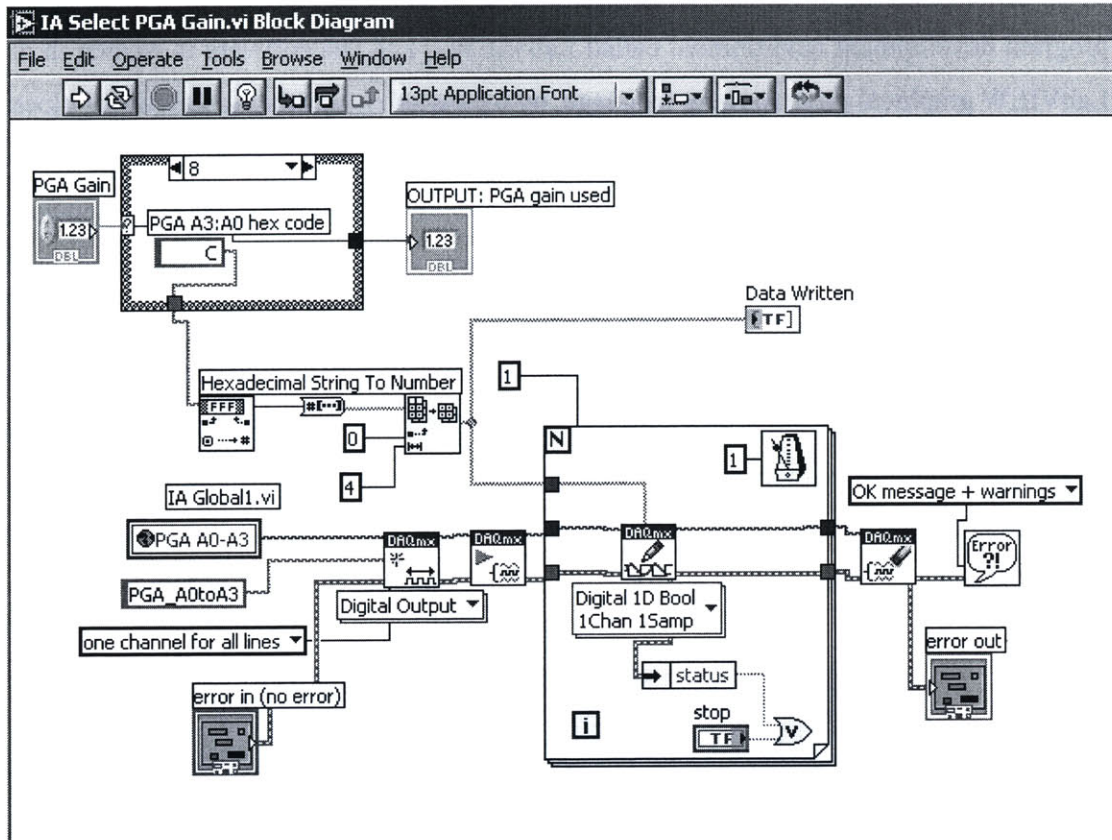

Figure 22. The block diagram for a LabVIEW virtual instrument.

The LabVIEW programming environment comes with drivers for the various hardware modules available for the PXI system. This availability of support for the test automation hardware makes it especially convenient to develop the AutoBench system software on the PXI/LabVIEW platform. Many predefined functions or VI's also make development of code in the LabVIEW environment quick.

The software for the AutoBench system is described in the subsequent subsections by means of representative block diagrams rather than images of the LabVIEW virtual instruments themselves. Representative diagrams are chosen over the VI images as the VI images are often quite large and have complicated wiring that is not

visually easy to follow, whereas the diagrams provide a clearer and more concise view of the software ideas.

The software is organized into three hierarchical levels. At the topmost level is the Single INA Channel Test Program, which provides the graphical user interface (GUI) through which a user interacts with the test system. This top level program contains the subVIs that implement the individual instrumentation amplifier tests. The top level program also performs the writing of data into an appropriately formatted spreadsheet for storage.

At the middle level of the program hierarchy lie the subVIs that implement the individual tests. Seven of these exist for executing each of the seven instrumentation amplifier DC parameter tests described in the Test Methodology section.

At the lowest level of the program hierarchy lie the auxiliary functions, the subVIs that implement different aspects of the control of the hardware, e.g. programming the MDAC voltage on the INA-TCB and controlling the closing and opening of the different relays on the INA-TCB.

4.1 The Auxiliary SubVIs

The auxiliary subVIs are functions written to capture the operation of distinct hardware resources in the AutoBench system that are used across multiple parameter tests. The subVIs are instantiated locally when they are needed in a particular test.

4.1.1 IA Power to Board Regulators ON

The IA Power to Board Regulators ON subVI is used to select the voltage and current settings required of the External Power Supply 2, which is used to power the voltage regulators on the INA-TCB.

The name of the resource used as the External Power Supply 2 is supplied from the global variable file. The name and desired voltage and current values are fed as inputs to a predefined VISA Write subVI available in LabVIEW for writing a command buffer to a GPIB device. Figure 23 shows the block diagram for the IA Power to Board Regulators ON subVI. A voltage of +25V capable of sourcing up to 1A is requested of

the positive 25V channel on the E3631A, while a voltage of -25V at 1A is requested of the negative 25V channel on the same device.

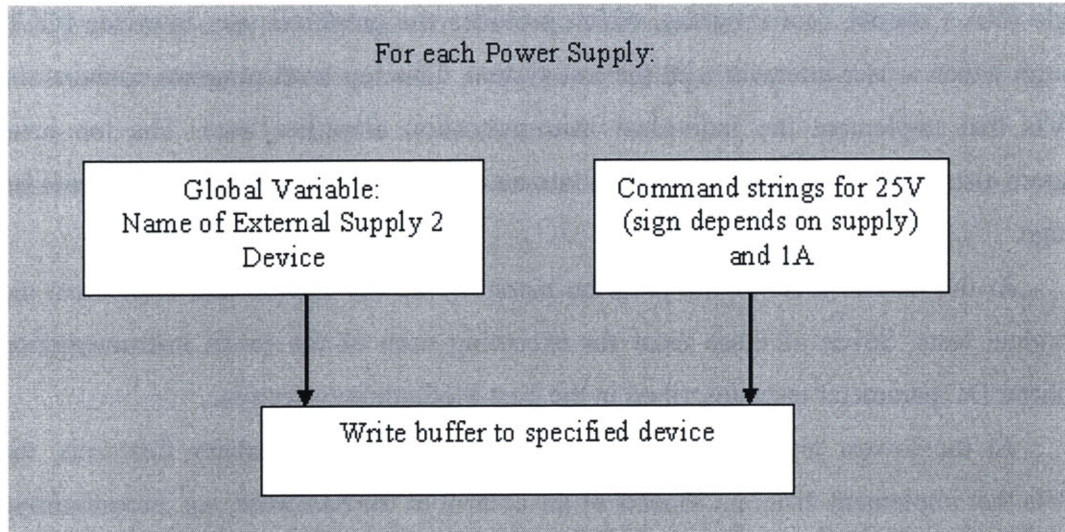

Figure 23. Program flow for the IA Power to Board Regulators ON subVI.

4.1.2 IA Power to Board Regulators OFF

The IA Power to Board Regulators OFF subVI is used to turn off the External Power Supply 2, by requesting 0V and 0A from both the positive and negative 25V channel on the E3631A device.

The name of the resource used as the External Power Supply 2 is supplied from a global variable file. The name and desired voltage and current values are fed as inputs to a predefined VISA Write subVI, as with the function that turns the power supply on. Figure 24 shows the block diagram for the IA Power to Board Regulators OFF subVI.

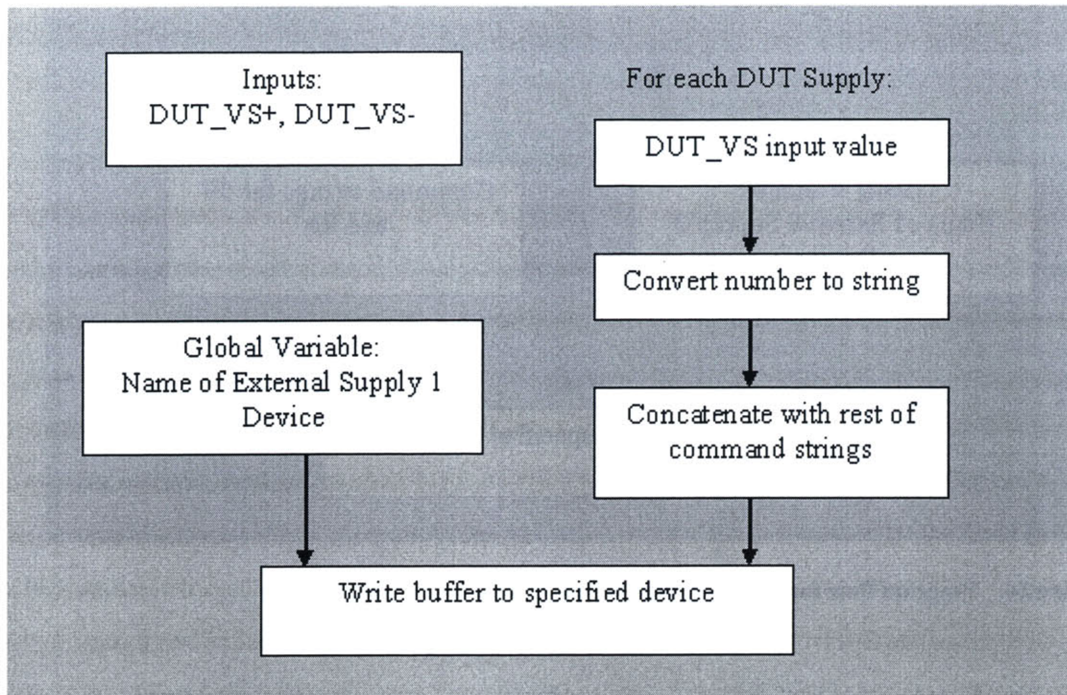

Figure 25. Program flow for the IA Set DUT Supplies subVI.

4.1.4 IA DUT Supplies OFF

The IA DUT Supplies OFF subVI is used to turn off the External Power Supply 1, by requesting 0V and 0A from both the positive and negative 25V channels on the appropriate E3631A device.

The name of the resource used as the External Power Supply 1 is supplied from the global variable file. The name and desired voltage and current values are fed as inputs to a predefined VISA Write subVI. The command is then written to the device. Figure 26 shows the block diagram for the IA DUT Supplies OFF subVI.

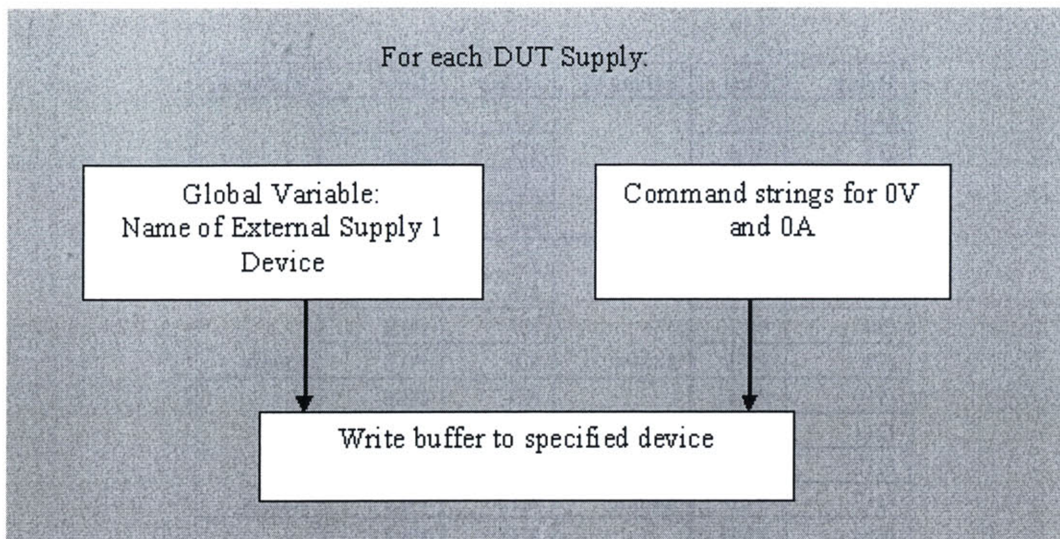

Figure 26. Program flow for the IA DUT Supplies OFF subVI.

4.1.5 IA SET Selected Relays

The relays labeled Gx and Kx are controlled by the Digital I/O Module lines indicated in Table 3. The IA SET Selected Relays subVI is used to set a group of desired relays while leaving the state of the other relays unchanged. The subVI accepts two hexadecimal string inputs: a StringG and a StringK. The two strings indicate the relays that are to be set and the ones that are to be kept in their old state. Each relay on the INA-TCB has a dedicated bit in the input string. If the bit is 1, the corresponding relay is set. If the bit is 0, the corresponding relay is left in its old state. The information in StringG pertains to the relays labeled Gx, while the information in StringK pertains to the relays labeled Kx. The mapping of relays to bits is shown in Table 3. The relays are set by outputting a high signal on the appropriate Digital I/O Module line. The RelayStates global variable is also updated. The block diagram of the flow of the IA Set Selected Relays subVI is shown in Figure 27.

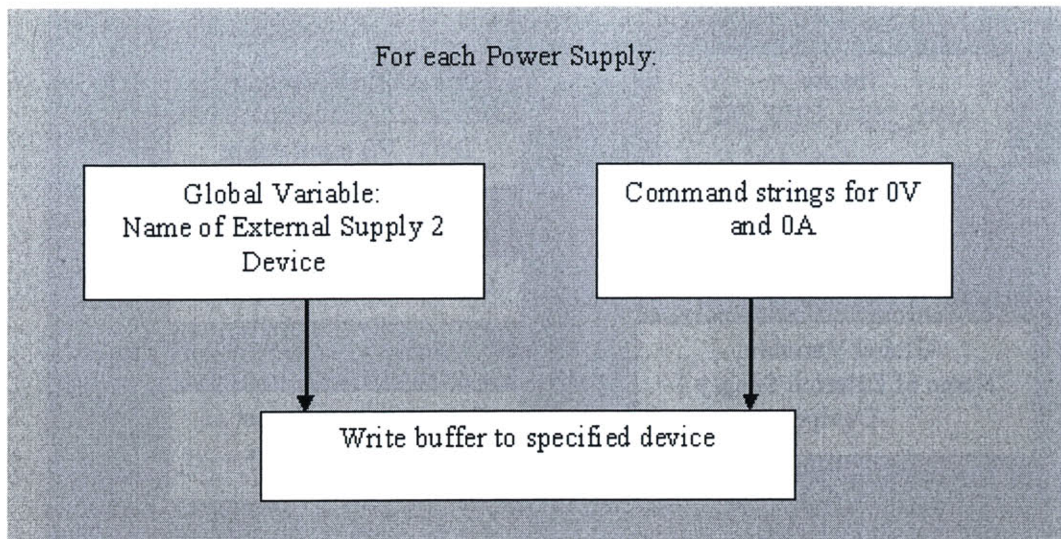

Figure 24. Program flow for the IA Power to Board Regulators OFF subVI.

4.1.3 IA Set DUT Supplies

The IA Set DUT Supplies is used to request the desired DUT supply voltages from the External Power Supply 1 resource in the AutoBench system. The function accepts two number inputs: a positive supply voltage and a negative supply voltage. Each number input is converted to an engineering string and concatenated with the rest of voltage request string required by the E3631A device. The command string and the name of the power supply device serving as External Power Supply 1 are passed as inputs to the VISA Write subVI in LabVIEW, which writes an appropriate buffer to the device specified by the name input. The hardware receives the command via the GPIB communication interface and executes it to output the voltage requested. Separate write commands are issued for the positive voltage and the negative voltage. Figure 25 shows a block diagram of the IA Set DUT Supplies.

Relay	Line	String G	Relay	Line	String K
G15	P1.5		K1	P0.6	
G2	P1.6		K2	P0.4	
G4	P1.7		K3	P8.2	
G5	P0.7	xxxx0	K4	P8.0	xxxx0
G6	P0.5		K5	P7.1	
G7	P8.3		K6	P7.2	
G8	P8.1		K7	P0.2	
G9	P7.3	xxx0x	K8	P0.0	xxx0x
G10	P0.1		K9	P8.6	
G11	P8.7		K10	P8.4	
G12	P7.6		K11	P6.0	
G13	P7.0	xx0xx	K12	P6.1	xx0xx
G14	P7.7		K13	P6.2	
G16	P7.5		K14	P6.4	
G17	P7.4		K15	P6.5	
G18	P0.3	x0xxx	K16	P6.6	x0xxx
G19	P8.5		K17	P6.7	
x	x		K18	P6.3	
x	x		x	x	
x	x	0xxxx	x	x	0xxxx

Table 3. The mapping of the Digital I/O lines to relay controls.

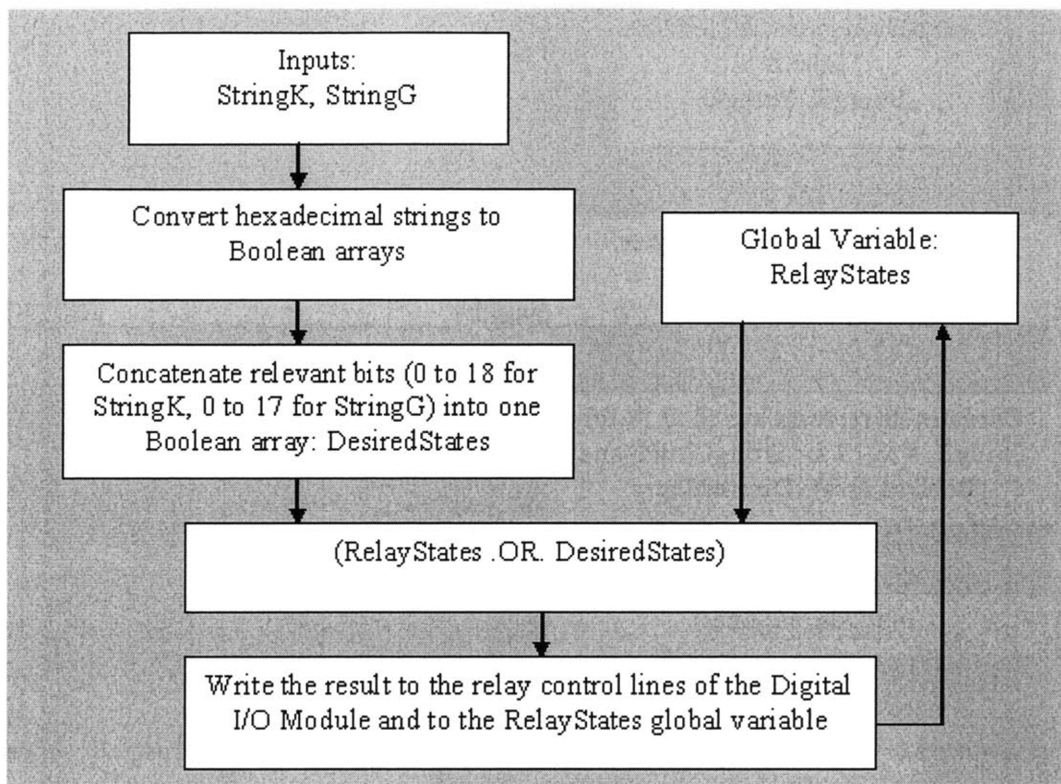

Figure 27. Program flow for the IA SET Selected Relays subVI.

4.1.6 IA RESET Selected Relays

The IA RESET Selected Relays subVI is used to reset a group of desired relays while leaving the state of the other relays unchanged. As with the SET subVI, this subVI accepts two hexadecimal input strings whose bits map to control signals for the Gx and Kx relays on the INA-TCB. A control bit with value 1 results in the corresponding relay to be reset, whereas a control bit with value 0 causes the corresponding relay to maintain its old state. The block diagram depicting the program flow in the IA RESET Selected Relays subVI is shown in Figure 28.

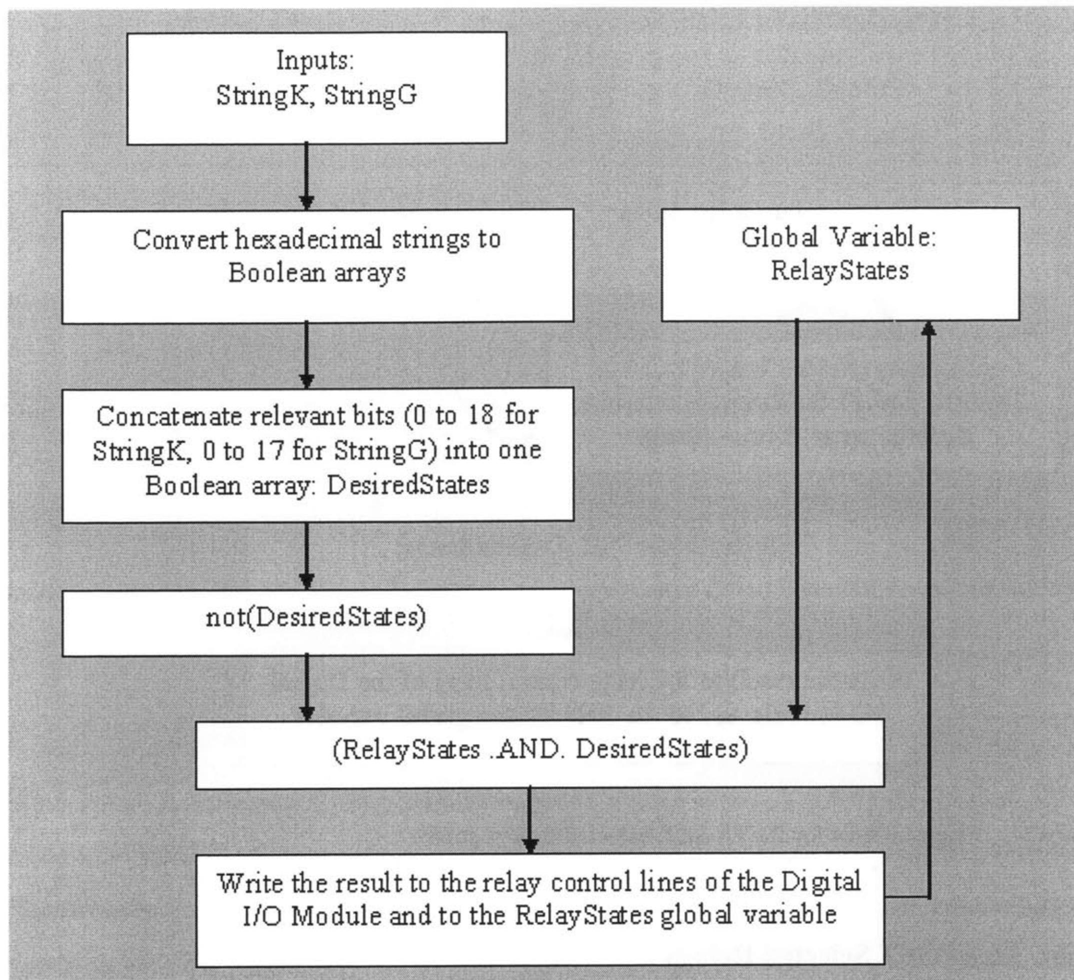

Figure 28. Program flow for the IA RESET Selected Relays subVI.

4.1.7 IA RESET ALL Relays

The IA RESET ALL Relays subVI is used to put all the relays on the INA-TCB in their default state. The subVI is generally used at the end of a parameter test program to ensure that the relays are reverted to their default states in order to avoid unexpected effects in subsequent programs. The IA RESET ALL Relays subVI has no inputs, and simply writes 0 bits to all Digital I/O Module lines that control relays. The new states of the relays are also written to the RelayStates global variable. The program flow is shown in the block diagram of Figure 29.

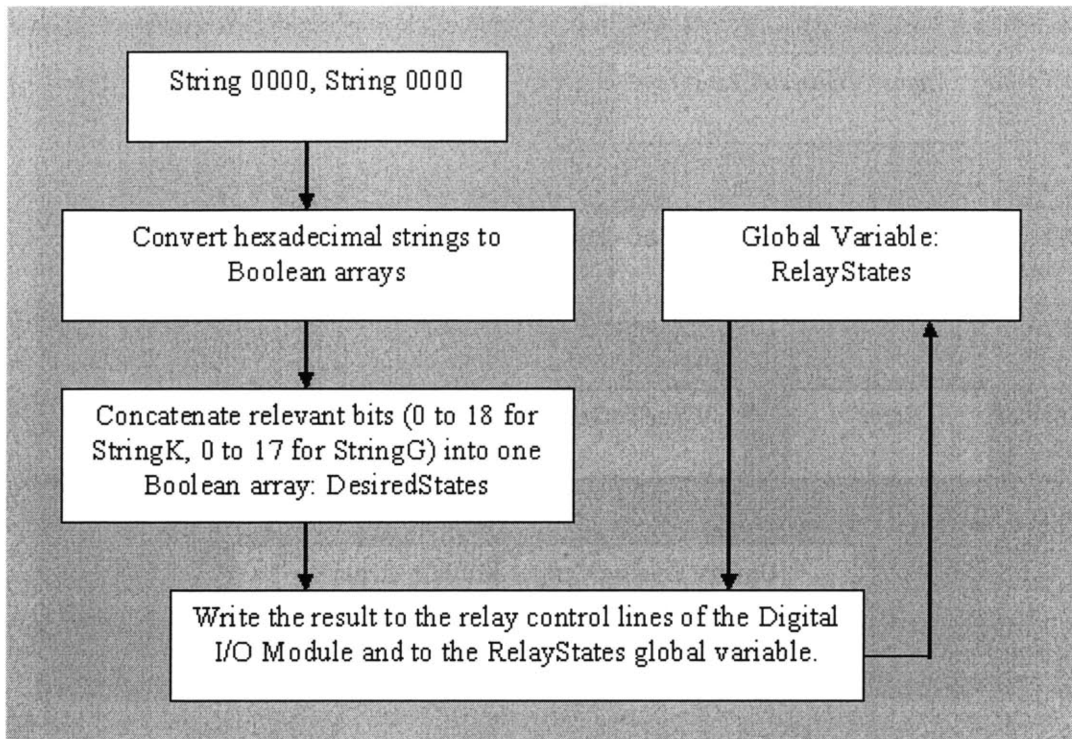

Figure 29. Program flow for the IA RESET ALL Relays subVI.

4.1.8 IA Output CM Voltage Gain3

The IA Output CM Voltage Gain3 subVI is used to output a third of the voltage required from the SEV generating path on the INA-TCB. The subVI accepts an input number equal to the voltage desired. A check is performed to ensure that the requested SEV output is within the -18V to +18V range. If the input is in the appropriate range, the input is divided by 3 to compensate for the amplification by 3 obtained from the high voltage amplifier in the SEV generator and the voltage obtained is output on the appropriate channel of the Analog Output Module. A block diagram for the IA Output CM Voltage Gain3 subVI is shown in Figure 30.

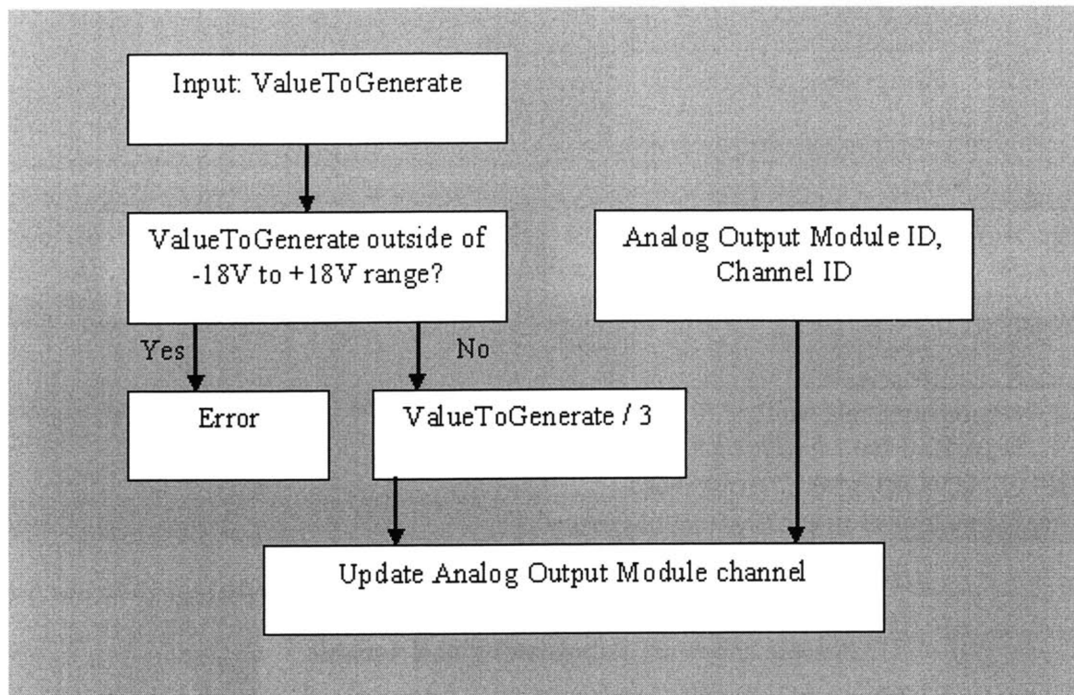

Figure 30. Program flow for the IA Output CM Voltage Gain3 subVI.

4.1.9 IA Output MDAC Voltage

The IA Output MDAC Voltage subVI is used to configure the DAC that is used to generate the Precision Differential Voltage on the INA-TCB. The subVI accepts an input number corresponding to the voltage desired, converts it to the appropriate Boolean array, and programs the MDAC via its serial interface using the appropriate lines of the Digital I/O Module of the AutoBench system.

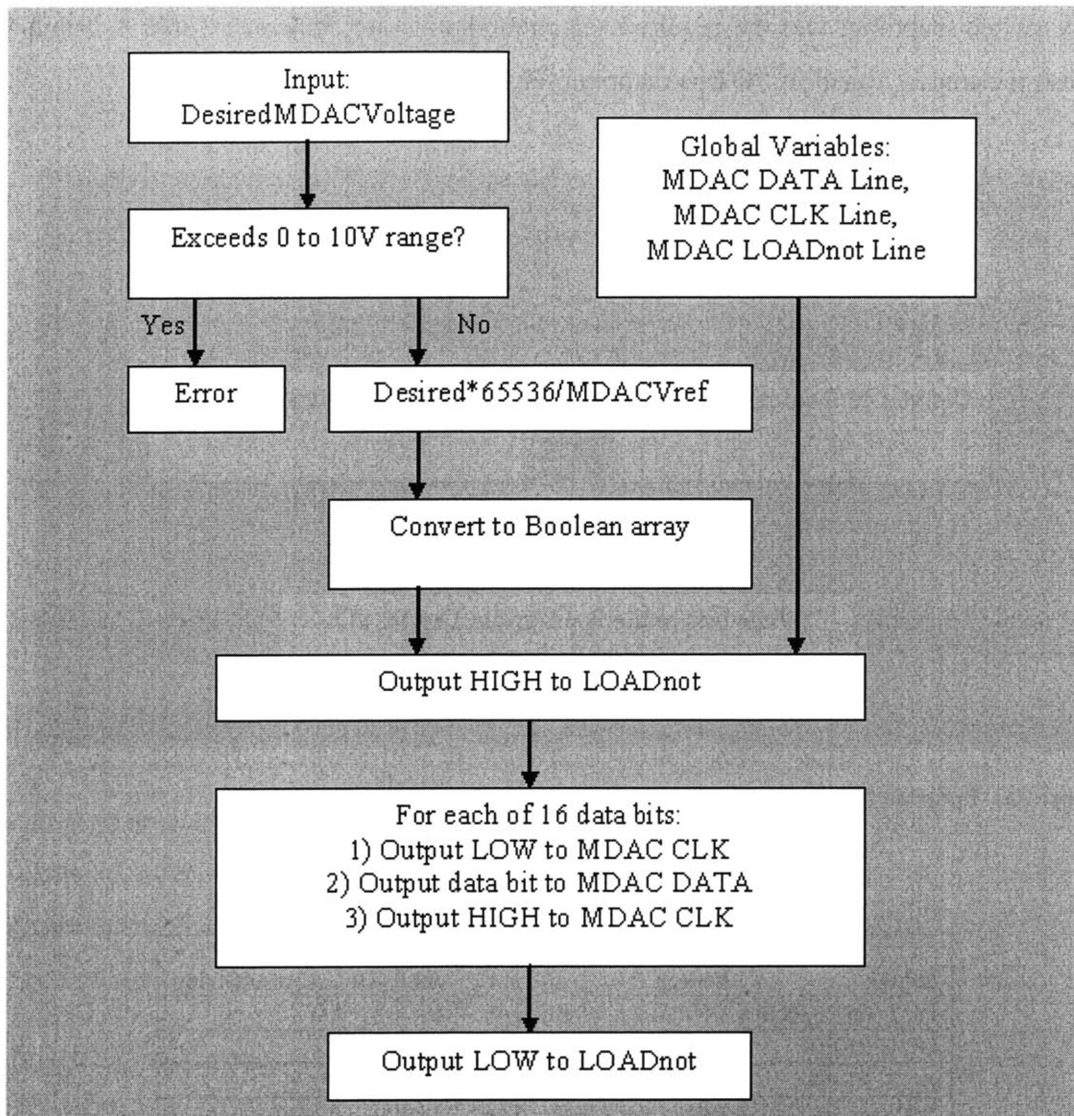

Figure 31. Program flow for the IA Output MDAC Voltage subVI.

4.1.10 IA Select MUXN Output

The IA Select MUXN Output subVI is used to select which of the input signals to the analog mux U18 to pass through to the output. The subVI expects a hexadecimal string input. The input string is converted to a number and then to a Boolean array, after which the 4 least significant bits are extracted as the switch select signals A3, A2, A1 and A0 for the mux. The bits are written to the appropriate Digital I/O Module lines to implement the selection. Figure 32 shows a block diagram for the subVI. The signal to

mux switch mapping, and the required selection signals are shown in Table 4. Table 5 shows the control signal to I/O line mapping for MUXN.

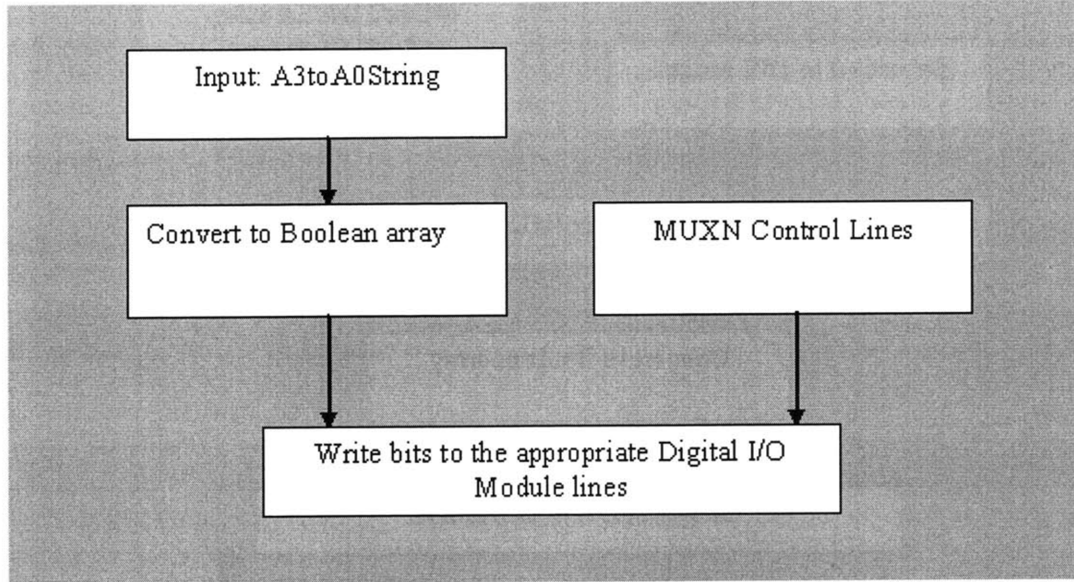

Figure 32. Program flow for the IA Select MUXN Output subVI.

Signal	MUX Switch	A3	A2	A1	A0	A3toA0String
DUT_OUT_BUF	S1	0	0	0	0	0
DUT_REFB	S2	0	0	0	1	1
DUT_REFA	S3	0	0	1	0	2
VIQneg_VS-	S4	0	0	1	1	3
VIQpos_VS-	S5	0	1	0	0	4
VIQneg_VS+	S6	0	1	0	1	5
VIQpos_VS+	S7	0	1	1	0	6
BUF_GND	S8	0	1	1	1	7
MDAC_Vref	S9	1	0	0	0	8
DUT_VS-	S10	1	0	0	1	9
DUT_VS+	S11	1	0	1	0	A
Unused	S12	1	0	1	1	B
Unused	S13	1	1	0	0	C
Unused	S14	1	1	0	1	D
Unused	S15	1	1	1	0	E
Unused	S16	1	1	1	1	F

Table 4. The mapping of amplification stage input signals to the analog multiplexer switches.

Signal	Digital I/O Module Line
MUXN_EN	P4.7
MUXN_A0	P4.6
MUXN_A1	P4.5
MUXN_A2	P4.4
MUXN_A3	P4.3

Table 5. The mapping of DIO lines to control signals for MUXN.

4.1.11 IA Select MUXP Output

The IA Select MUXP Output subVI is used to select which of the input signals to the analog mux U17 to pass through to the output. This subVI is equivalent to the IA Select MUXN Output subVI, with the data being written to the appropriate Digital I/O Module lines. Table 6 shows the control signal to I/O line mapping for MUXP.

Signal	Digital I/O Module Line
MUXP_EN	P2.6
MUXP_A0	P2.5
MUXP_A1	P2.4
MUXP_A2	P2.3
MUXP_A3	P2.2

Table 6. The mapping of DIO lines to control signals for MUXP.

4.1.12 IA Enable MUXN

The IA Enable MUXN subVI is used to provide the enable signal for the selection of input to output signal for mux U18 on the INA-TCB. The high signal is written to the appropriate Digital I/O Module line to achieve the desired effect. The block diagram for the subVI is shown in Figure 33.

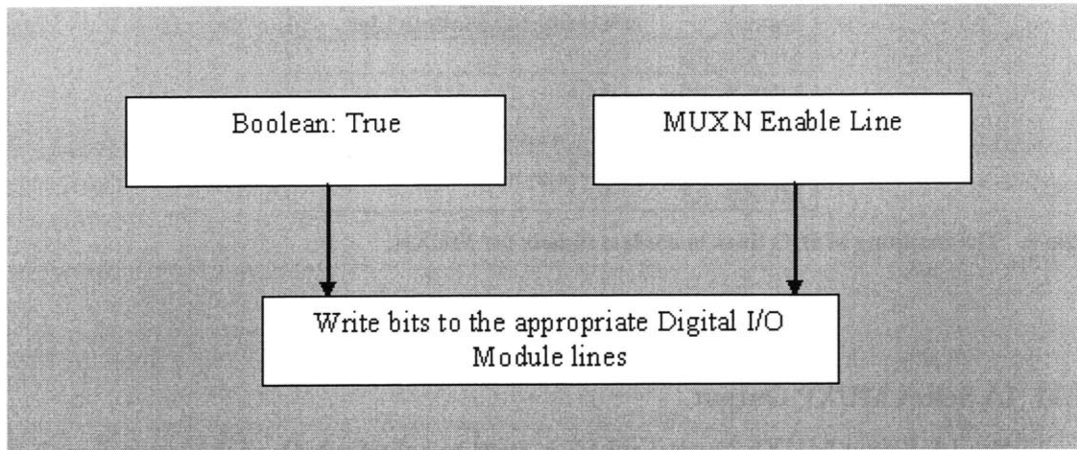

Figure 33. Program flow for the IA Enable MUXN subVI.

4.1.13 IA Enable MUXP

The IA Enable MUXP subVI is used to provide the enable signal for the selection of input to output signal for mux U17 on the INA-TCB. The high signal is written to the appropriate Digital I/O Module line to achieve the desired effect. The block diagram for the subVI is similar to the one shown in Figure 33 but with the appropriate Digital I/O Module line selected for MUXP Enable.

4.1.14 IA Disable MUXN

The IA Disable MUXN subVI disables the output of mux U18 on the INA-TCB. This subVI is equivalent to the IA Enable MUXN subVI, only the Boolean value written to the Digital I/O Module line is False, causing a low value to be written to the line.

4.1.15 IA Disable MUXP

The IA Disable MUXP subVI disables the output of mux U17 on the INA-TCB. This subVI is equivalent to the IA Enable MUXP subVI, only the Boolean value written to the Digital I/O Module line is False, causing a low value to be written to the line.

4.1.16 IA Select Voltage Amplifier

The IA Select Voltage Amplifier subVI is used to connect the outputs of the MUXN and MUXP analog muxes to the appropriate amplification circuitry path. Three relays are used to do this channeling of output signals. A block diagram for the subVI is shown in Figure 34. The possible inputs to the subVI, the corresponding amplifiers selected as well as the states of the 3 relays are shown in Table 7.

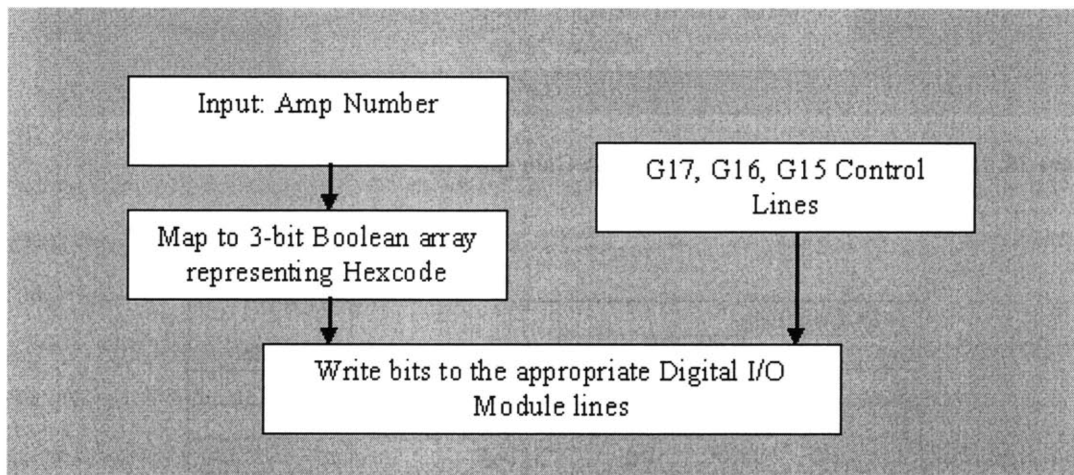

Figure 34. Program flow for the IA Select Voltage Amplifier subVI.

Input	Amp Selected	G15	G16	G17	Hexcode
0	Programmable Gain Amplifier	0	0	0	0
1	Summing Amplifier	0	1	1	3
2	Difference Amplifier	1	X	X	4
3	None	0	0	1	1

Table 7. The mapping of the amp selection relay states to output amplifier selected.

4.1.17 IA Select PGA Gain

The IA Select PGA Gain subVI is used to provide the selection signal for the U1 and U2 amplifiers on the INA-TCB. The subVI accepts a numerical input, the Gain. This input is mapped to a 4-bit Boolean array that is written to the appropriate Digital I/O Module lines to set the control signal for the two programmable gain amplifiers. The

block diagram is shown in Figure 35. The possible gains, the corresponding signal and hexadecimal code are shown in Table 8.

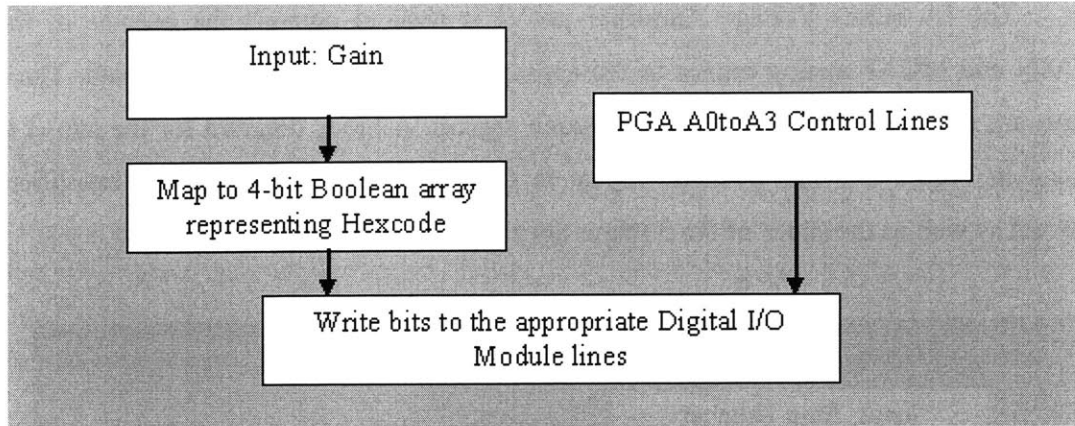

Figure 35. Program flow for the IA Select PGA Gain subVI.

PGA Gain Bits					
A3	**A2**	**A1**	**A0**	**Gain**	**Hexcode**
0	0	0	0	1*1=1	0
0	1	0	0	2*1=2	4
1	0	0	0	4*1=4	8
1	1	0	0	8*1=8	C
0	0	0	1	1*10=10	1
0	1	0	1	2*10=20	5
1	0	0	1	4*10=40	9
1	1	0	1	8*10=80	D
0	0	1	0	1*100=100	2
0	1	1	0	2*100=100	6
1	0	1	0	4*100=400	A
1	1	1	0	8*100=800	E
0	0	1	1	1*1000=1000	3
0	1	1	1	2*1000=2000	7
1	0	1	1	4*1000=4000	B
1	1	1	1	8*1000=8000	F

Table 8. The mapping of control signals to PGAmp gain.

4.1.18 Measure EA1_VOUT

The Measure EA1_VOUT subVI is used to connect the output of the PGA-based amplifier to the Digital Multimeter Module (DMM), and measure the voltage. PXI

MUX2 is configured to operate in 2-wire mode. PXI MUX2 ch0 is connected to com0 and com0 is connected to ab0. This causes the PGA-based amplifier output to be connected to the DMM. The DMM is initialized and configured to take voltage readings and adapting the resolution and range of the measured to the signal automatically. The voltage is read and its value checked to be within range. The PXI MUX 2 switches are disconnected and the device is placed in its default state. The steps are carried out by predefined subVIs available in the National Instruments Data Acquisition Package (NI-DAQ). The subVI outputs the voltage reading. A block diagram for the program flow in the Measure EA1_VOUT subVI is shown in Figure 36.

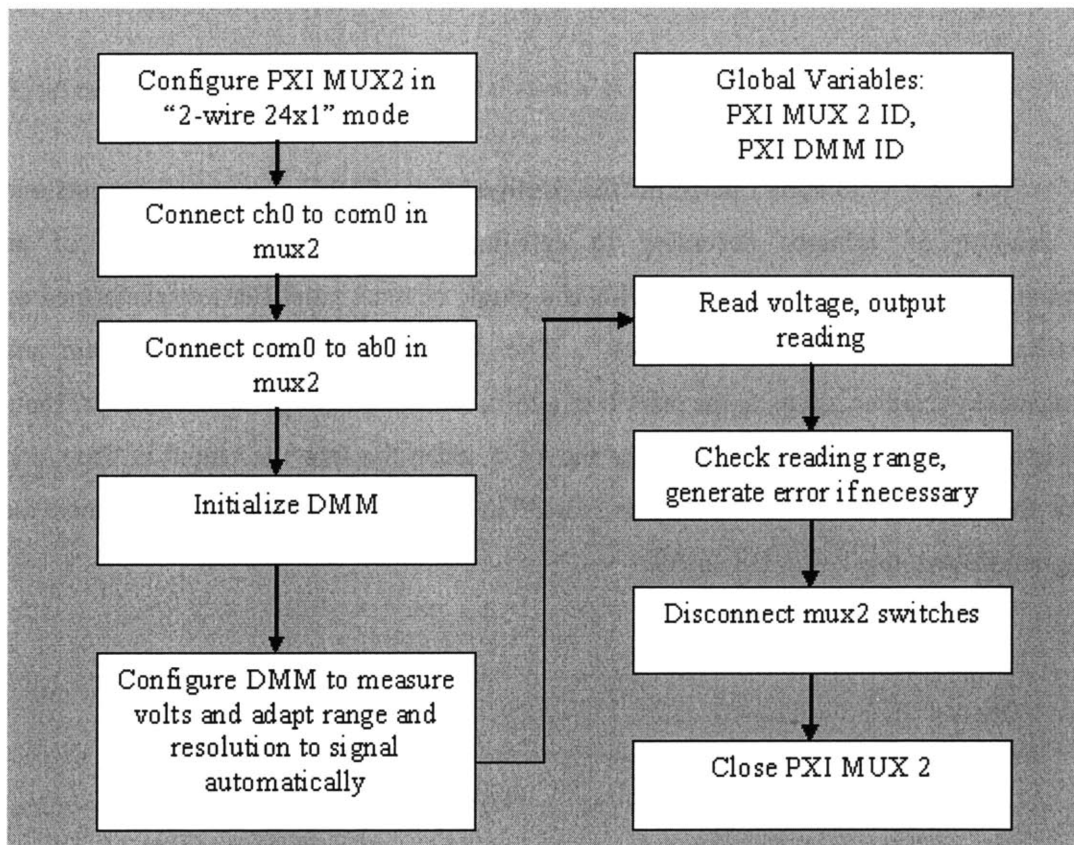

Figure 36. Program flow for the Measure EA1_VOUT subVI.

4.1.19 Measure EA2_VOUT

The Measure EA2_VOUT subVI is used to connect the output of the difference amplifier to the Digital Multimeter Module, and measure the voltage. The subVI is equivalent to the Measure EA1_VOUT subVI, except that the PXI MUX 2 switch connections are ch1 to com0 and com0 to ab0.

4.2 The Parameter Test SubVIs

The test procedure for each instrumentation amplifier parameter is captured in a separate subVI. The subVIs for the various tests are described below.

4.2.1 The Test VOS SubVI

The Test VOS subVI performs the configuration of DUT inputs and outputs and the reading of voltages necessary to calculate the input offset voltage of an instrumentation amplifier under test. This is a single channel amplifier test performed on the Channel B pins of the DUT interface. The DUT Gain and PGAmp Gain are numbers expected as inputs to the subVI. In addition the subVI expects an Execute? input that is a Boolean. The subVI calculates the VOS when the Execute? input is True, and skips the VOS routine when the input is False. The block diagram in Figure 37 shows the program flow in the Test VOS subVI.

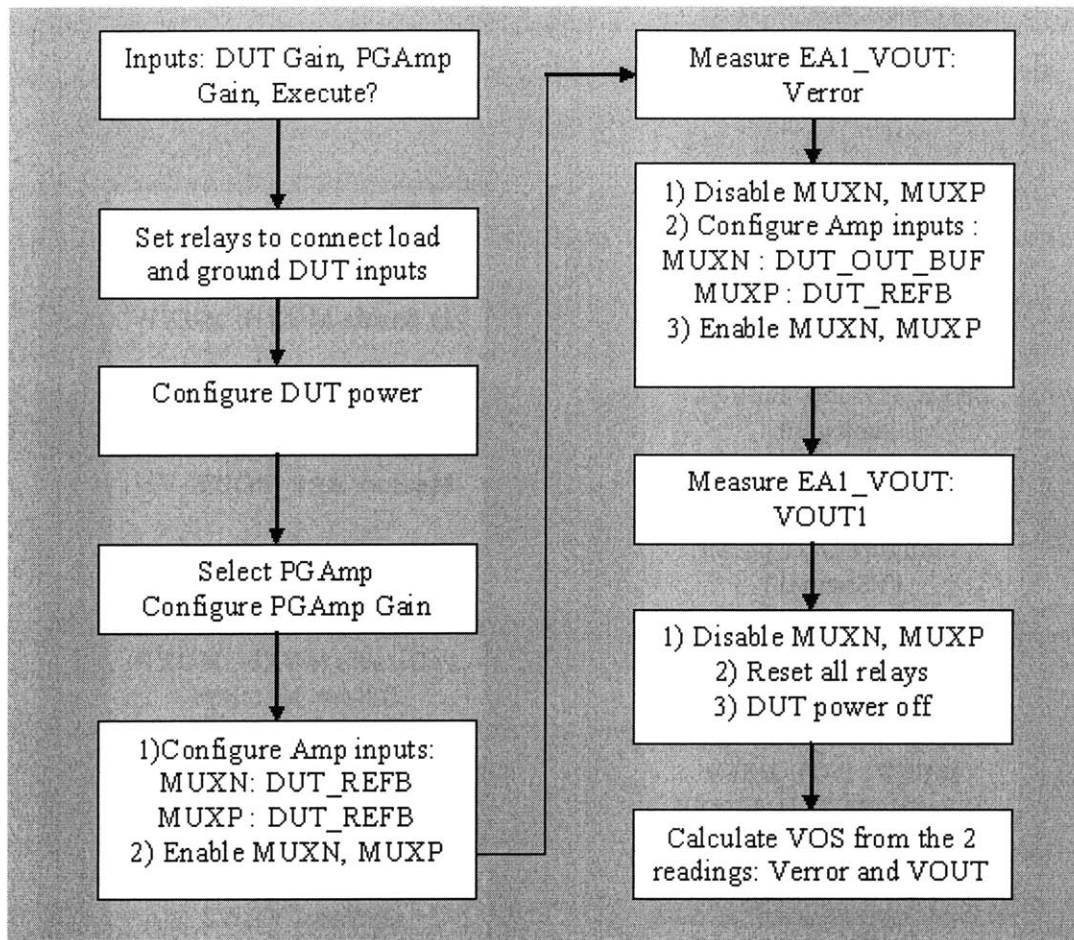

Figure 37. Program flow for the Test VOS subVI.

4.2.2 The Test PSRR SubVI

The Test PSRR subVI is used to perform the system configurations and measurements needed to calculate the power supply rejection ratio of an instrumentation amplifier under test. This is a single channel amplifier test performed on the Channel B pins of the DUT interface. Figure 38 shows the program flow for the Test PSRR subVI.

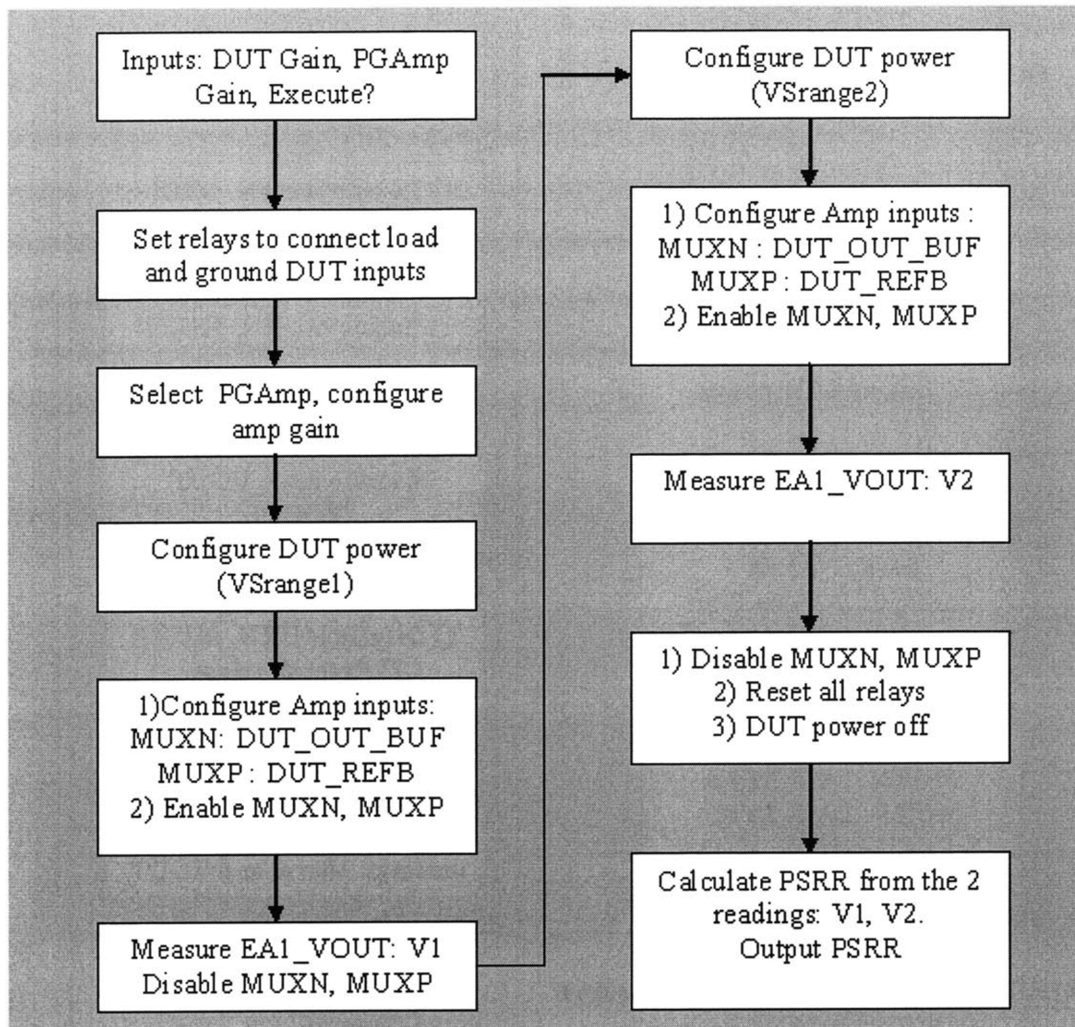

Figure 38. Program flow for the Test PSRR subVI.

4.2.3 The Test CMRR SubVI

The Test CMRR subVI is used to perform the system configurations and measurements needed to calculate the common mode rejection ratio of an instrumentation amplifier under test. This is a single channel amplifier test performed on the Channel B pins of the DUT interface. Figure 39 shows the program flow for the Test CMRR subVI.

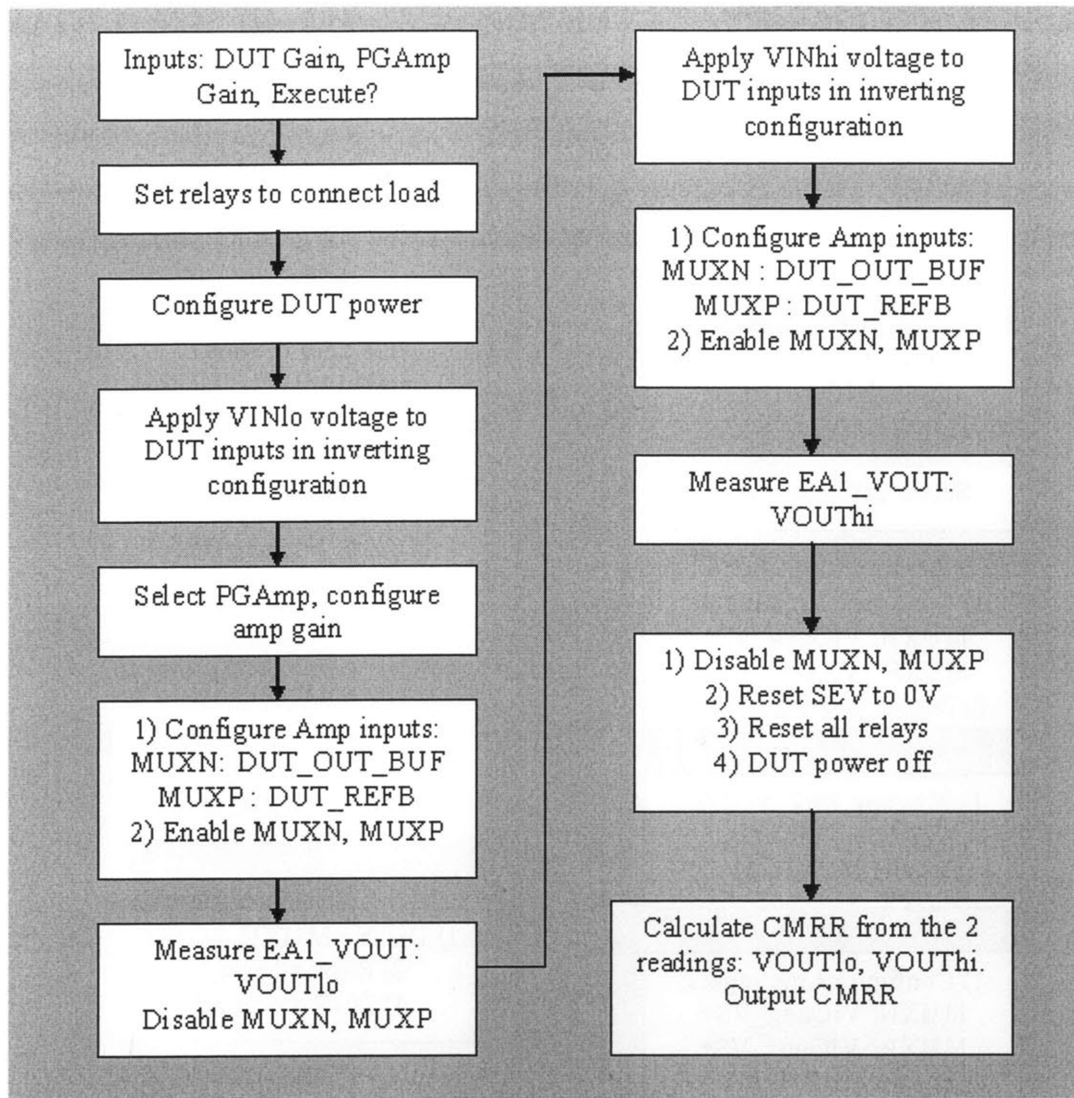

Figure 39. Program flow for the Test CMRR subVI.

4.2.4 The Test IQ SubVI

The Test IQ subVI is used to perform the system configurations and measurements needed to calculate the quiescent current for the positive and negative supplies of an instrumentation amplifier under test. This is a single channel amplifier test performed on the Channel B pins of the DUT interface. The subVI outputs two numbers, one value for each supply. Figure 40 shows the program flow for the Test IQ subVI.

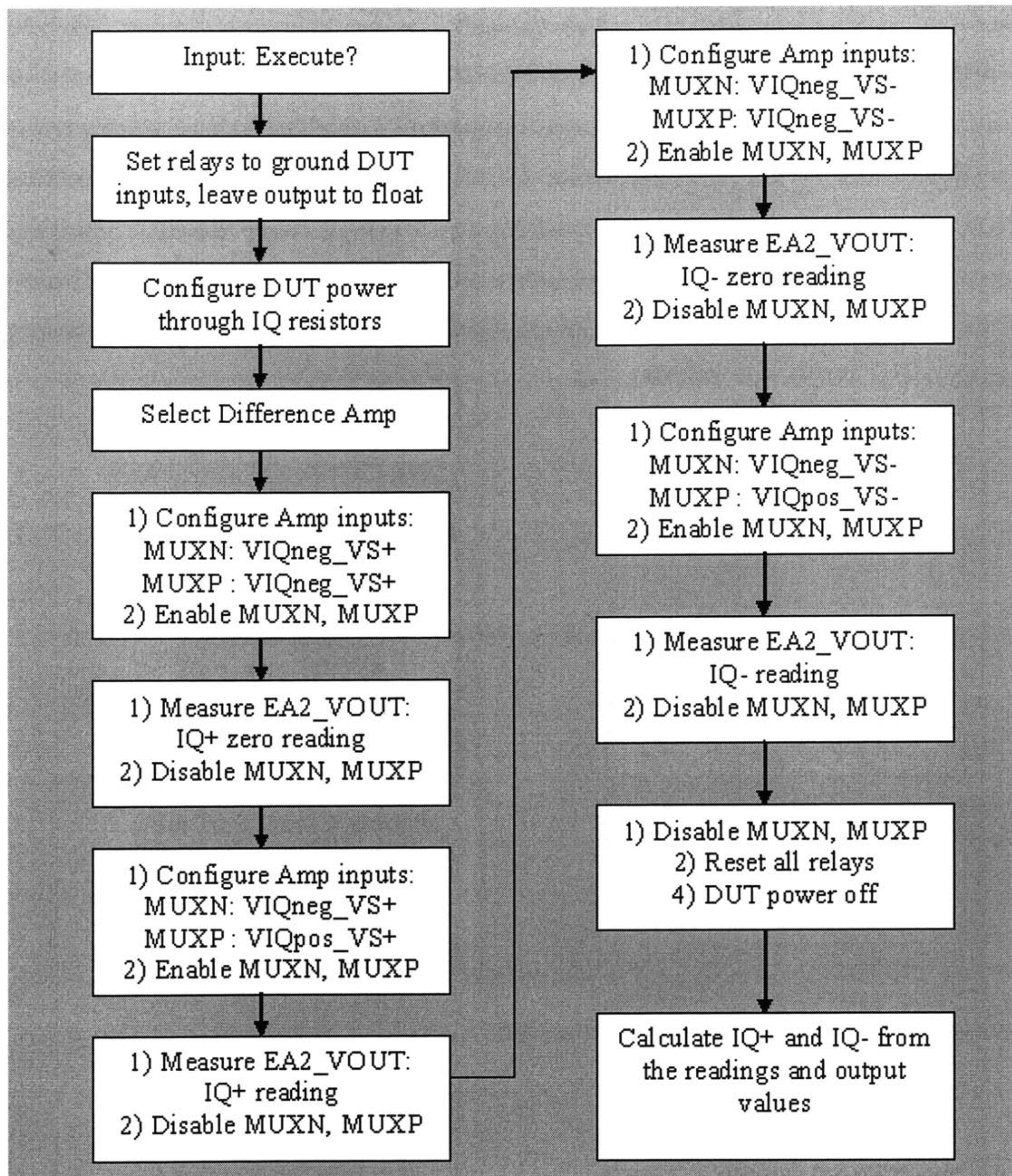

Figure 40. Program flow for the Test IQ subVI.

4.2.5 The Test IB SubVI

The Test IB subVI is used to perform the system configurations and measurements needed to calculate the input bias and input offset currents of an instrumentation amplifier under test. This is a single channel amplifier test performed on

the Channel B pins of the DUT interface. Figure 41 shows the program flow for the Test IB subVI.

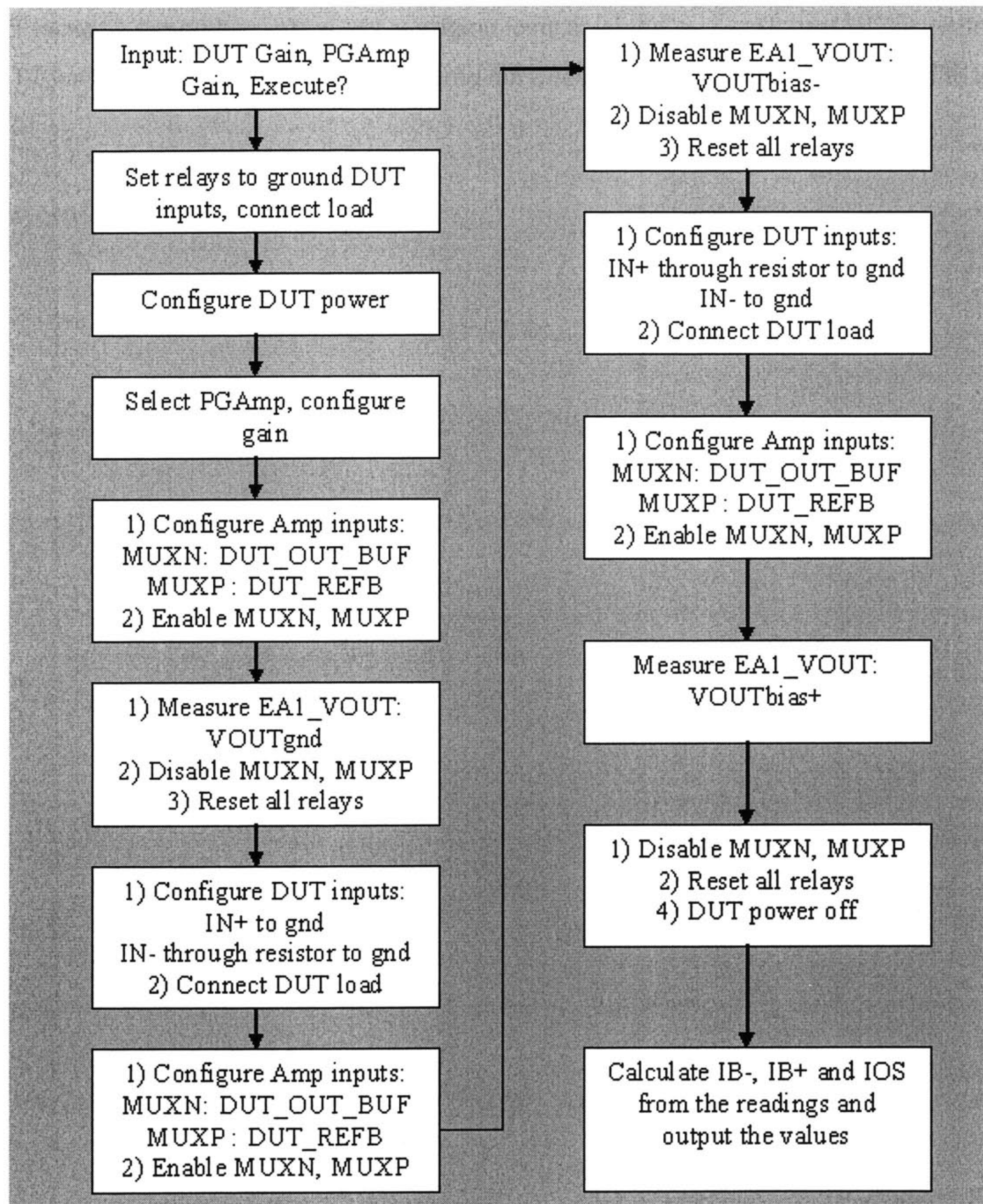

Figure 41. Program flow for the Test IB subVI.

4.2.6 The Test SWING SubVI

The Test SWING subVI is used to perform the system configurations and measurements needed to calculate the output voltage swings of an instrumentation amplifier under test. This is a single channel amplifier test performed on the Channel B pins of the DUT interface. Figure 42 shows the program flow for the Test SWING subVI.

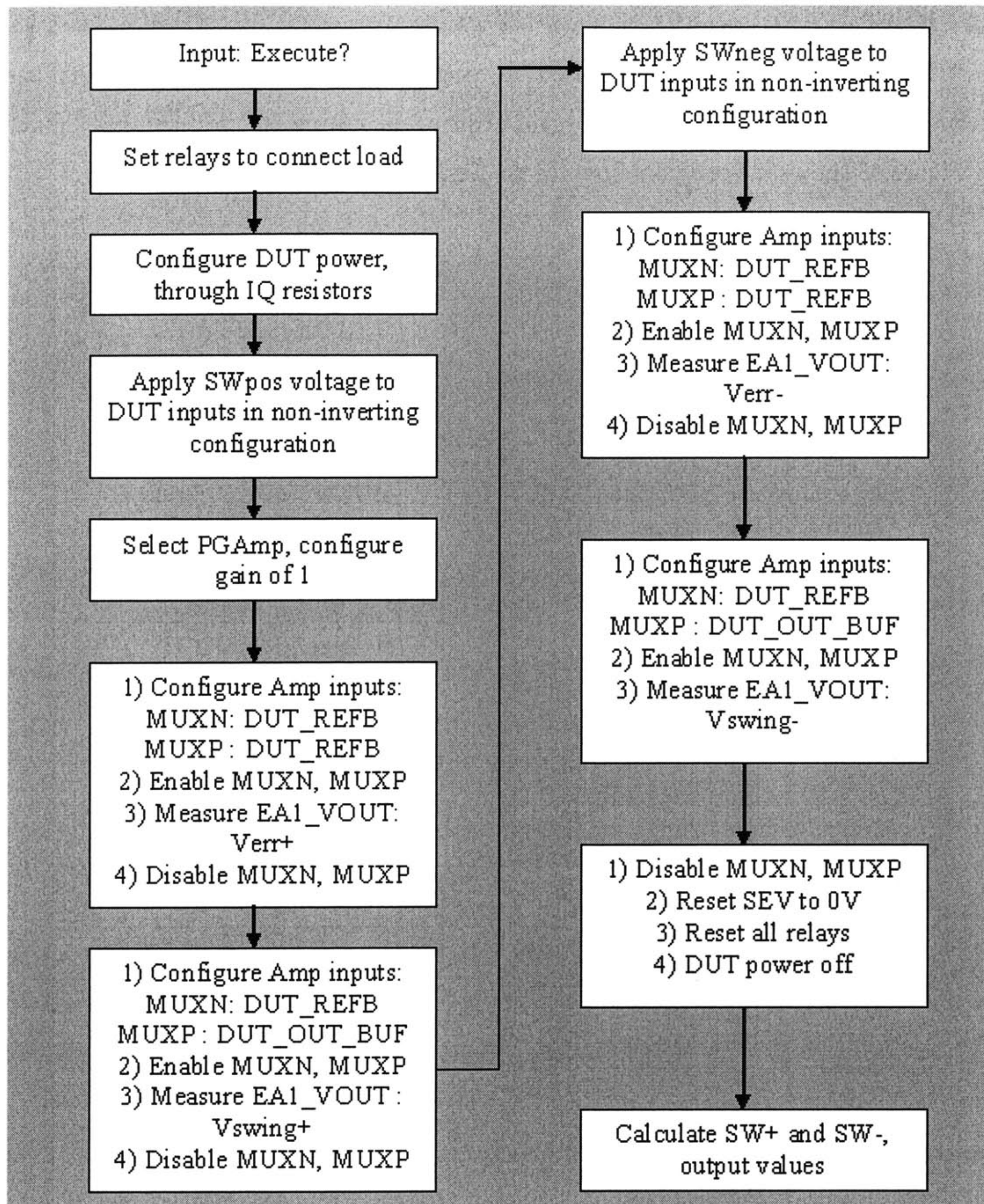

Figure 42. Program flow for the Test SWING subVI.

4.2.7 The Test GERR SubVI

The Test GERR subVI is used to perform the system configurations and measurements needed to calculate the gain error of an instrumentation amplifier under test. Figure 43 shows the program flow for the Test GERR subVI.

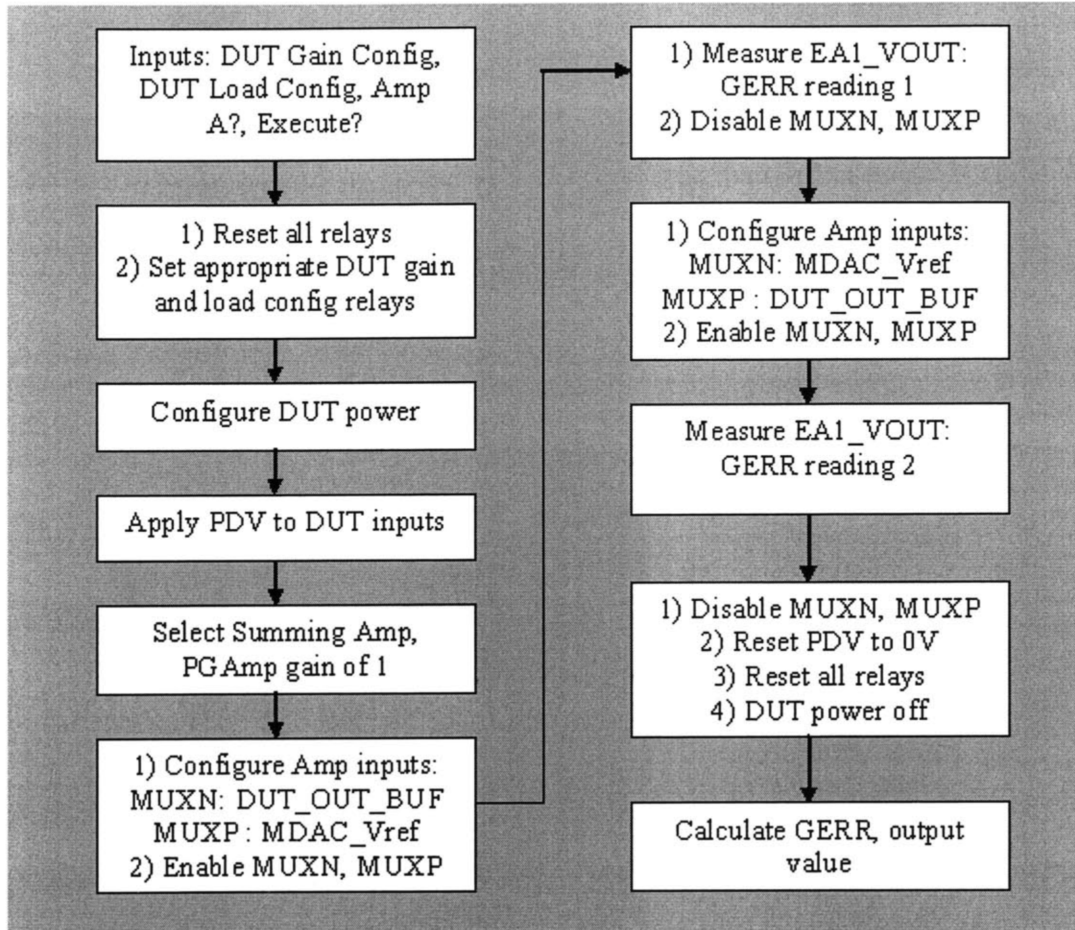

Figure 43. Program flow for the Test GERR subVI.

4.3 The Single Channel Instrumentation Amplifier Test Program

The top level instrumentation amplifier test program appears as the graphical user interface (GUI) shown in Figure 44. The user interacts with the test system via this GUI by changing the DUT identifier in the appropriate box, changing the test temperature to be recorded, and clicking on the TEST button when the device has been placed into the DUT interface. The instrumentation amplifier tests are executed in sequence and the results of the test are shown in the GUI. The GUI displays the value measured for each test parameter, the test limits for each parameter, the units, the pass/fail status for each parameter, and the cumulative pass/fail result for the device. The cumulative result is a pass only if all parameters are passes. The results are also written into an output spreadsheet file, whose name and path can be specified in the GUI window. The results are appended to previous data if the output file already exists, otherwise a new files in created.

The top level test program is written as a Single Channel INA Test Program subVI, which performs the reading and writing of input and output files, global variables and GUI variables. With this subVI, there exists a Single Channel INA Test Sequence subVI which sequences the parameter tests, times the execution of the tests, and outputs the collective results. Header information is written to the file each time the top level program is initiated. The Single Channel INA Test Program subVI is described by the block diagram in Figure 45.

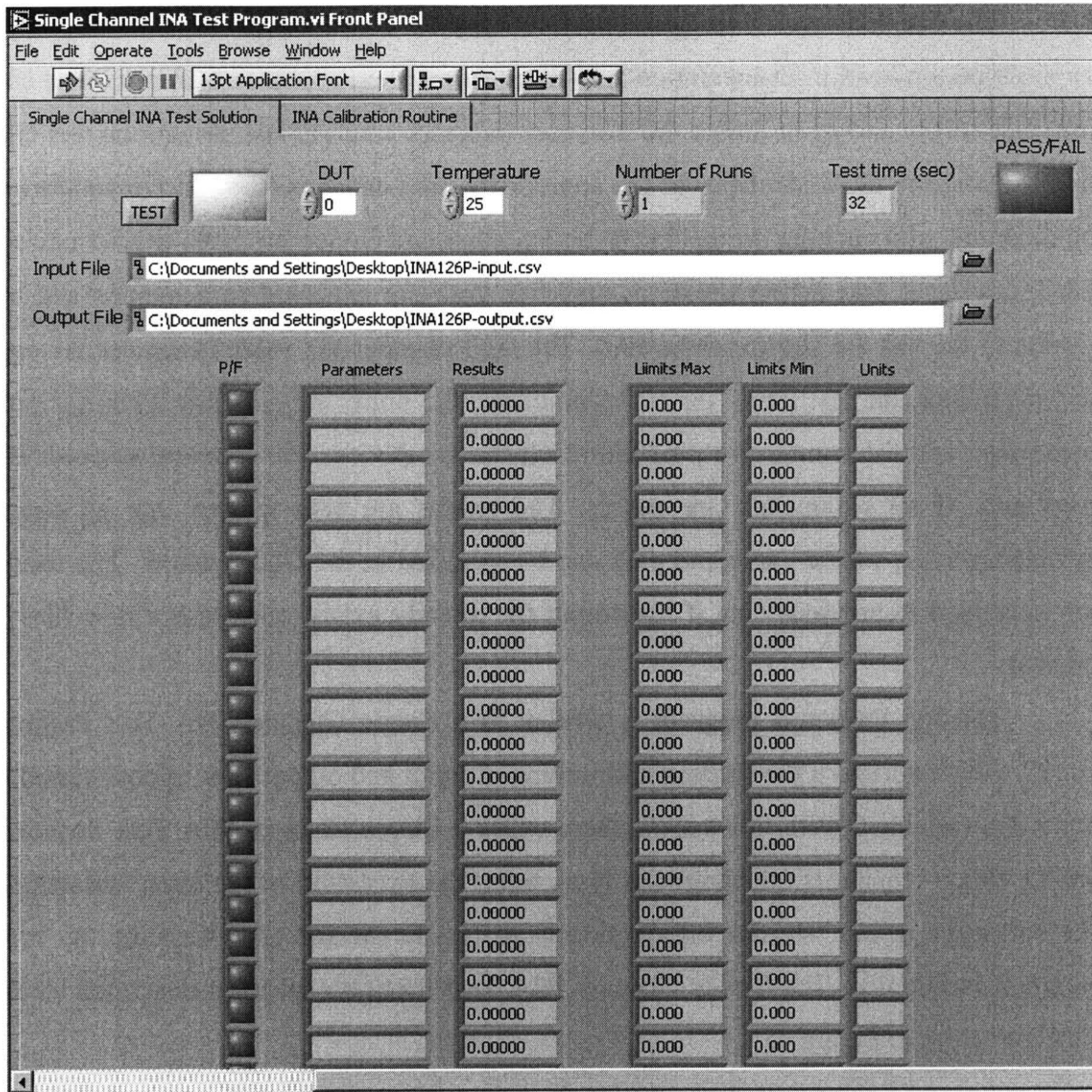

Figure 44. The graphical user interface for the Single Channel INA Test Program.

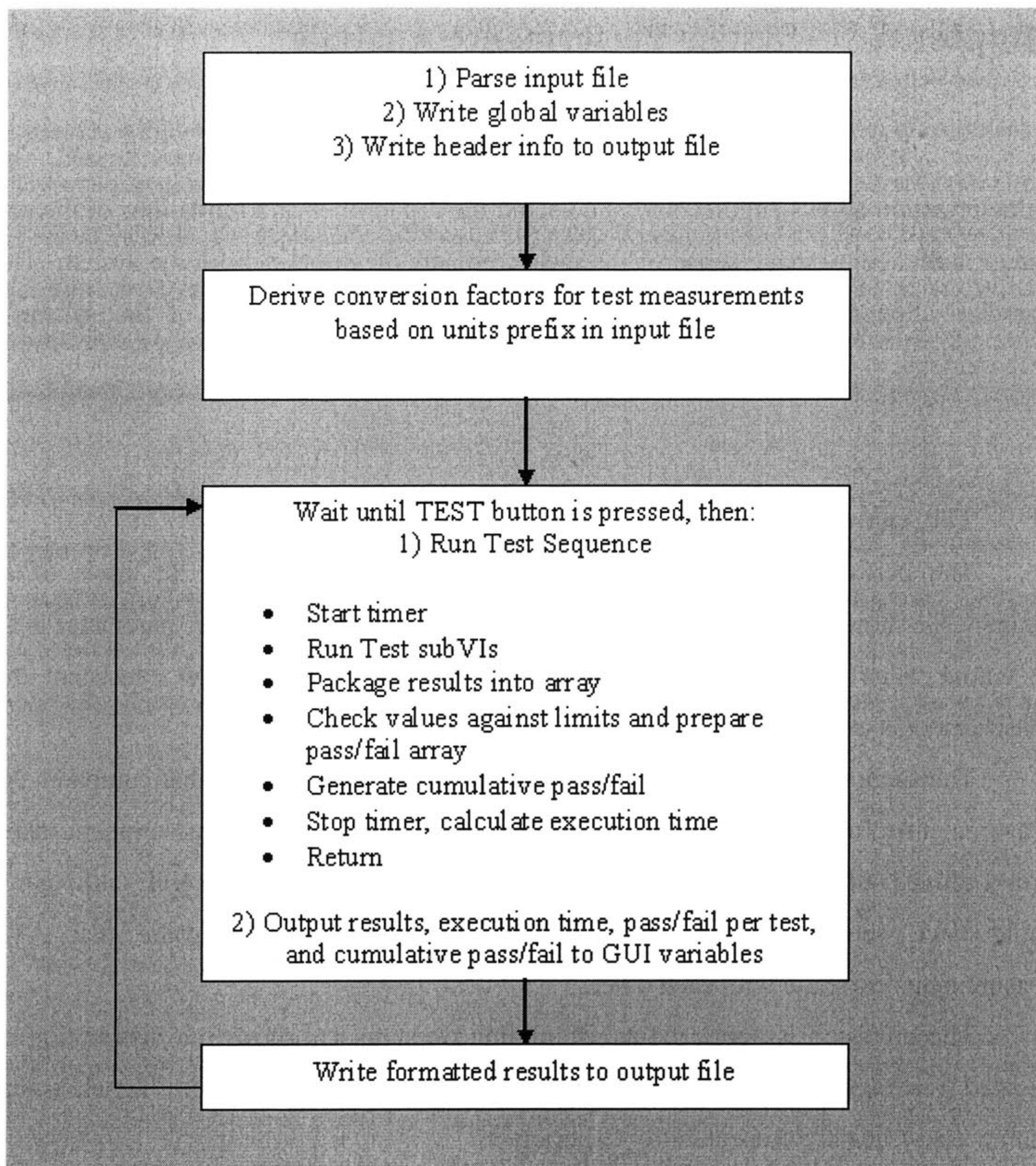

Figure 45. Program flow for the Single Channel INA Test Program subVI.

Chapter 5 System Performance Analysis

For a test system to be useful to engineers, its performance must be characterized. The characterization allows engineers to understand the capabilities and limitations of the test system, and thereby make sense of the measurements they obtain from the system. The characterization of the system defines the precision and accuracy of the system's measurements.

5.1 The Analysis Criteria

The performance of the AutoBench system is analyzed on the basis of a) accuracy, i.e. how close a measurement of an instrumentation amplifier parameter is to the actual value of the parameter, as well as b) precision, i.e. how consistent the measurement is on the system.

The accuracy is appraised by means of a Correlation Criterion that compares the measurement to a trusted value. The trusted value in this case is a measurement taken from a proved ATE system. Single readings are taken per device from ATE, although it would have been better to obtain multiple ATE readings to insure that ATE measurements correlate with each other.

The precision is appraised by examining on statistical terms the distribution of repeated readings of a parameter measurement for a single device. The statistical examination leads to a Repeatability Criterion.

The statistical parameters derived from the AutoBench performance analysis measurements are defined below:

- μABE : the mean of single measurements of a test parameter for 47 different units on the AutoBench system
- σABE : the standard deviation of the single measurements of a test parameter for 47 different units on the AutoBench system
- μATE: the mean of single measurements of a test parameter for 47 different units on the ATE

- σATE: the standard deviation of single measurements of a test parameter for 47 different units on the ATE
- $\mu DELTA$: the mean of differences in the value of a test parameter for measurements made on the ATE and on the AutoBench system
- $\sigma DELTA$: the standard deviation of the differences in the value of a test parameter for measurements made on the ATE and the AutoBench system
- μABE_R: the mean of 34 readings of a test parameter performed on the same device on the AutoBench system
- σABE_R: the standard deviation of 34 readings of a test parameter performed on the same device on the AutoBench system

A range of 6 standard deviations centered on the mean in a Gaussian distribution accounts for 99.73% of the area of the distribution. In other words, the standard deviation of a Gaussian distribution is roughly equal to one sixth of the total variation from the minimum value to the maximum value. Therefore, it is reasonable to assume that a good test system will mostly yield results in the range of the mean – 3sigma to mean + 3sigma. [13]

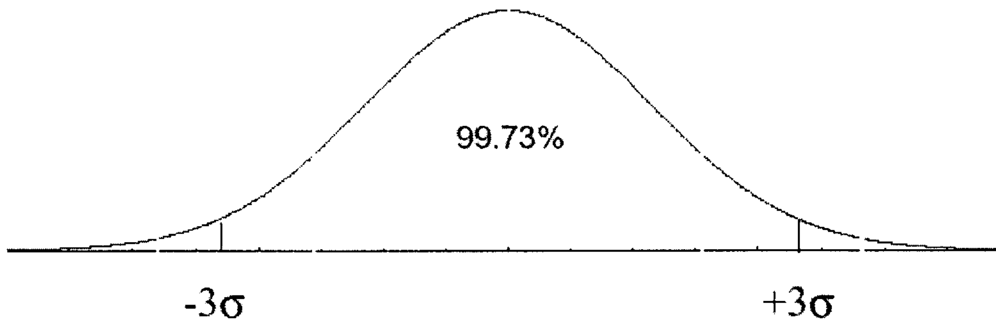

Figure 46. A normal (Gaussian) distribution has 99.73% of its probability within a 6 sigma range centered on the mean.

The variation in the value of a parameter for different devices yields a distribution within ($\mu ABE - 3*\sigma ABE$) to ($\mu ABE + 3*\sigma ABE$). In addition, the repeatability limitations (i.e. the errors due to the measurement system) introduce a variation of $6*\sigma ABE_R$ to each of the values in the range defined above. Hence the total resulting range of a measurement on the AutoBench system will lie in the range ($\mu ABE - 3*\sigma ABE - 6*\sigma ABE_R$) to ($\mu ABE + 3*\sigma ABE + 6*\sigma ABE_R$). We are satisfied with the system's capability when the lower bound of this range is greater than the Lower Test Limit (LTL) specified for the parameter under consideration, and the upper bound of the range is lower than the Upper Test Limit (UTL).

In addition, a variable called the Precision-to-Tolerance ratio (P/T) is often used to specify the acceptability of a measurement system's repeatability. A P/T value of 0.1 is generally regarded as acceptable. This translates to the following: the error due to repeatability limitations does not take up more than 10% of the tolerance range. The P/T for the system is calculated according to Equation 10.

$$\frac{P}{T} = \frac{6\sigma_{ABE_R}}{UTL - LTL}$$

(Eq. 10)

Thus, the Repeatability Criterion can be summarized by the following three requirements:

- Upper Bound Test: ($\mu ABE + 3*\sigma ABE + 6*\sigma ABE_R$) < UTL
- Lower Bound Test: ($\mu ABE - 3*\sigma ABE - 6*\sigma ABE_R$) > LTL
- P/T Ratio: $(6*\sigma ABE_R) / (UTL - LTL) < 0.1$

Similar to the motivation for the Repeatability Criterion, the Correlation Criterion is derived by the need to limit the full reasonable spread (99.73%) of the measurements for a parameter to the range specified for the parameter in the manufacturer's product data sheet. Again the variation in the value of a parameter for different devices yields a distribution within ($\mu ABE - 3*\sigma ABE$) to ($\mu ABE + 3*\sigma ABE$). The departure of the measured value from the actual value (i.e. the accuracy to the gold standard or ATE

measurement) in this case is characterized by another Gaussian distribution with mean and standard deviation equal to $\mu DELTA$ and $\sigma DELTA$ respectively. The departure (or delta) distribution therefore has virtually all of its distribution in the region given by ($\mu DELTA - 3*\sigma DELTA$) to ($\mu DELTA + 3*\sigma DELTA$), centered around the mean $\mu DELTA$. Hence, the departure can add the most extreme error of $\mu DELTA + 3*\sigma DELTA$ on the upper side of the measurement distribution, or $-(\mu DELTA + 3*\sigma DELTA)$ on the lower side of the measurement distribution.

The delta distribution adds on to the distribution for the parameter, and the Correlation Criterion is given by the following three requirements [1]:

- Upper Bound Test: $(\mu ABE + 3*\sigma ABE + \mu DELTA + 3*\sigma DELTA) < UTL$
- Lower Bound Test: $(\mu ABE - 3*\sigma ABE - \mu DELTA - 3*\sigma DELTA) > LTL$
- P/T Ratio: $(\mu DELTA + 3*\sigma DELTA) / (UTL - LTL) < 0.1$

The performance of the AutoBench system for each test parameters is presented in the sections that follow.

5.2 Analysis of VOS measurements

The statistical parameters for the VOS test are derived from the analysis experiments and shown in Table 9. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

Statistical Parameters (VOS)	Values
μABE	14.25
σABE	71.65
μATE	47.98
σATE	72.90
μDELTA	33.72
σDELTA	3.12
μABE_R	18.27
σABE_R	2.61
UTL	250.00
LTL	-250.00

Table 9. Statistical data for the VOS test.

The Repeatability Criterion is applied to the VOS test using the statistical parameters from Table 9. Table 10 shows that all three conditions for the Repeatability Criterion hold. The system is therefore capable of measuring an instrumentation amplifier's VOS repeatedly, without exceedingly the test limits for VOS.

Repeatability Criterion (VOS)		Value	Desired	Status
Upper Bound Test	$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$	244.86	< 250	Pass
Lower Bound Test	$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$	-216.36	> -250	Pass
P/T Ratio	$(6\sigma ABE_R) / (UTL - LTL)$	0.03	< 0.10	Pass

Table 10. The precision of the VOS test.

The Correlation Criterion is applied to the VOS test results as shown in Table 11. The upper limit for the correlation distribution exceeds the specified test limit. The other two conditions hold.

Correlation Criterion (VOS)		Value	Desired	Status
Upper Bound Test	$(\mu ABE + 3*\sigma ABE + \|\mu DELTA + 3*\sigma DELTA)$	272.28	< 250	Fail
Lower Bound Test	$(\mu ABE - 3*\sigma ABE - \mu DELTA - 3*\sigma DELTA)$	-243.78	> -250	Pass
P/T Ratio	$(\mu DELTA + 3*\sigma DELTA) / (UTL - LTL)$	0.09	< 0.10	Pass

Table 11. The accuracy of the VOS test.

The AutoBench VOS test is therefore proved to be precise, but not adequately accurate. Suggestions for improving the accuracy are discussed in the last part of this thesis.

5.3 Analysis of PSRR Measurements

The statistical parameters for the PSRR test are derived from the analysis experiments and shown in Table 12. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

Statistical Parameters (PSRR)	**Values**
μABE	-0.69
σABE	3.13
μATE	-0.62
σATE	3.1
μDELTA	0.07
σDELTA	0.08
μABE_R	0.43
σABE_R	0.04
UTL	15
LTL	-15

Table 12. Statistical data for the PSRR test.

The Repeatability Criterion is applied to the PSRR test using the statistical parameters from Table 12. Table 13 shows that all three conditions for the Repeatability Criterion hold. The system is therefore capable of measuring an instrumentation amplifier's PSRR repeatedly, without exceedingly the test limits.

Repeatability Criterion (PSRR)		**Value**	**Desired**	**Status**
Upper Bound Test	$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$	8.94	< 15	Pass
Lower Bound Test	$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$	-10.32	> -15	Pass
P/T Ratio	$(6\sigma ABE_R) / (UTL - LTL)$	0.01	< 0.10	Pass

Table 13. The precision of the PSRR test.

The Correlation Criterion is applied to the PSRR test results as shown in Table 14. All three conditions hold for the PSRR test, therefore the system is determined to be accurate.

Correlation Criterion (PSRR)		**Value**	**Desired**	**Status**
Upper Bound Test	$(\mu ABE + 3\sigma ABE + |\mu DELTA + 3\sigma DELTA)$	9.01	< 15	Pass
Lower Bound Test	$(\mu ABE - 3\sigma ABE - \mu DELTA - 3\sigma DELTA)$	-10.39	> -15	Pass
P/T Ratio	$(\mu DELTA + 3\sigma DELTA) / (UTL - LTL)$	0.01	< 0.10	Pass

Table 14. The accuracy of the PSRR test.

The AutoBench PSRR test is therefore proved to be adequately precise and accurate.

5.4 Analysis of CMRR Measurements

The statistical parameters for the CMRR test are derived from the analysis experiments and shown in Table 15. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

Statistical Parameters (CMRR)	Values
μABE	-20.77
σABE	26.79
μATE	-18.51
σATE	22.05
μDELTA	2.26
σDELTA	16.33
μABE_R	-18.16
σABE_R	0.27
UTL	70.00
LTL	-70.00

Table 15. Statistical data for the CMRR test.

The Repeatability Criterion is applied to the CMRR test using the statistical parameters from Table 15. Table 16 shows that two of the three conditions for the Repeatability Criterion hold. The results show that the system produces CMRR measurements that spread beyond the lower test limit specified for the CMRR test.

Repeatability Criterion (CMRR)		Value	Desired	Status
Upper Bound Test	$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$	61.22	< 70.00	Pass
Lower Bound Test	$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$	-102.76	> -70.00	Fail
P/T Ratio	$(6\sigma ABE_R) / (UTL - LTL)$	0.01	< 0.10	Pass

Table 16. The precision of the CMRR test.

The Correlation Criterion is applied to the CMRR test results as shown in Table 17. All three bounds are exceeded for the CMRR test, showing that the system measurements are poorly correlated with the ATE measurement that is used as the gold standard.

Correlation Criterion (CMRR)		Value	Desired	Status
Upper Bound Test	$(\mu ABE + 3\sigma ABE + \lvert\mu DELTA + 3\sigma DELTA)$	110.85	< 70.00	Fail
Lower Bound Test	$(\mu ABE - 3\sigma ABE - \mu DELTA - 3\sigma DELTA)$	-152.39	> -70.00	Fail
P/T Ratio	$(\mu DELTA + 3\sigma DELTA) / (UTL - LTL)$	0.37	< 0.10	Fail

Table 17. The accuracy of the CMRR test.

The AutoBench system is determined to be inadequately precise and inadequately accurate for the CMRR test, since neither the Repeatability nor the Correlation Criteria hold completely. Suggestions for improving the AutoBench capability are discussed in the concluding section.

5.5 Analysis of IQ+ measurements

The statistical parameters for the IQ+ test are derived from the analysis experiments and shown in Table 18. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

Statistical Parameters (IQ+)	Values
μABE	172.70
σABE	0.85
μATE	175.55
σATE	1.81
μDELTA	2.84
σDELTA	1.51
μABE_R	173.03
σABE_R	0.14
UTL	200.00
LTL	120.00

Table 18. Statistical data for the IQ+ test.

The Repeatability Criterion is applied to the IQ+ test using the statistical parameters from Table 18. Table 19 shows that all three conditions for the Repeatability Criterion hold. The system is therefore capable of measuring an instrumentation amplifier's IQ+ repeatedly, without exceedingly the test limits.

Repeatability Criterion (IQ+)		Value	Desired	Status
Upper Bound Test	*$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$*	176.09	< 200	Pass
Lower Bound Test	*$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$*	169.31	> 120	Pass
P/T Ratio	*$(6\sigma ABE_R) / (UTL - LTL)$*	0.01	< 0.10	Pass

Table 19. The precision of the IQ+ test.

The Correlation Criterion is applied to the IQ+ test results as shown in Table 20. All three conditions hold for the IQ+ test, therefore the system is determined to be accurate.

Correlation Criterion (IQ+)		Value	Desired	Status
Upper Bound Test	*$(\mu ABE + 3\sigma ABE + \|\mu DELTA + 3\sigma DELTA)$*	182.62	< 200	Pass
Lower Bound Test	*$(\mu ABE - 3\sigma ABE - \mu DELTA - 3\sigma DELTA)$*	162.78	> 120	Pass
P/T Ratio	*$(\mu DELTA + 3\sigma DELTA) / (UTL - LTL)$*	0.09	< 0.10	Pass

Table 20. The accuracy of the IQ+ test.

The AutoBench IQ+ test is hereby shown to be adequately precise and accurate.

5.6 Analysis of IB+, IB- and IOS Measurements

The statistical parameters for the IB+, IB- and IOS tests are derived from the analysis experiments and shown in Table 21. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

	Values		
Statistical Parameters	**IB+**	**IB-**	**IOS**
μABE	9.10	-7.32	1.78
σABE	1.01	1.07	0.15
μATE	10.22	-10.31	-0.09
σATE	1.02	1.05	0.09
μDELTA	1.13	-2.99	-1.87
σDELTA	0.04	0.01	0.12
μABE_R	10.06	-8.38	1.68
σABE_R	0.03	0.13	0.13
UTL	25.00	0.00	2.00
LTL	0.00	-25.00	-2.00

Table 21. Statistical data for the IB+, IB- and IOS tests.

The Repeatability Criterion is applied to the IB and IOS tests using the statistical parameters from Table 21. Table 22 shows that all three conditions hold for the separate IB tests for the inverting and non-inverting amplifier inputs. However, only one of the three conditions for the Repeatability Criterion hold for the combined IOS measurement. The results show that the system produces IOS measurements that spread beyond the upper test limit specified for the IOS test. Also, the variation due to repeatability limitations of the system exceeds 10% of the tolerance range.

Repeatability Criterion for IB+, IB- and IOS		**Values**			**Desired (IOS)**	**Status (IOS)**
		IB+	**IB-**	**IOS**		
Upper Bound Test	$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$	12.31	-3.33	3.01	< 2	Fail
Lower Bound Test	$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$	5.89	-11.31	0.55	> -2	Pass
P/T Ratio	$(6\sigma ABE_R) / (UTL - LTL)$	0.01	0.03	0.20	< 0.1	Fail

Table 22. The precision of the input offset current test.

The Correlation Criterion is applied to the IOS test results as shown in Table 23. Although the individual positive and negative bias current tests show acceptable correlation, the combined input offset current measurement does not. The upper bound of the measurement distribution is exceeded for the IOS test. In addition the variation in IOS measurements occupies over 50% of the tolerance. The results show that the system measurements are poorly correlated with the ATE measurement used as the gold standard.

Correlation Criterion for IB+, IB- and IOS		**Values**			**Desired (IOS)**	**Status (IOS)**
		IB+	**IB-**	**IOS**		
Upper Bound Test	$(\mu ABE + 3\sigma ABE + \mu DELTA + 3\sigma DELTA)$	13.38	-1.08	4.46	< 2	Fail
Lower Bound Test	$(\mu ABE - 3\sigma ABE - \mu DELTA - 3\sigma DELTA)$	4.82	-13.56	-0.90	> -2	Pass
P/T Ratio	$(\mu DELTA + 3\sigma DELTA) / (UTL - LTL)$	0.05	0.12	0.56	< 0.1	Fail

Table 23. The accuracy of the input offset current test.

The AutoBench IOS test is shown to be inadequately precise and inadequately accurate, since neither the Repeatability nor the Correlation Criteria fully hold. Suggestions for improving the AutoBench capability are discussed in the concluding section.

5.7 Analysis of SW+ and SW- Measurements

The performance of the SW+ and SW- tests is not analyzed using the Repeatability and Correlation Criteria as with the other tests. A full analysis is omitted as this is not a test performed on the ATE system used and therefore there was no correlation to be performed.

Rather a test is done to ensure that the output of the amplifier being tested was capable of swinging to within the desired range of the rail voltage.

5.8 Analysis of GERR Measurements

The statistical parameters for the GERR test are derived from the analysis experiments and shown in Table 24. The upper and lower test limits are obtained from the product data sheet and are also included in the table.

Statistical Parameters (GERR)	Values
μABE	-24.45
σABE	15.94
μATE	-28.53
σATE	15.46
μDELTA	-4.08
σDELTA	3.52
μABE_R	-31.09
σABE_R	0.12
UTL	100.00
LTL	-100.00

Table 24. Statistical data for the GERR test.

The Repeatability Criterion is applied to the GERR test using the statistical parameters from Table 24. Table 25 shows that all three conditions for the Repeatability Criterion hold. The system is therefore capable of measuring an instrumentation amplifier's GERR repeatedly, without exceedingly the test limits.

Repeatability Criterion (GERR)		Value	Desired	Status
Upper Bound Test	$\mu ABE + 3\sigma ABE + 6\sigma ABE_R$	24.09	< 100	Pass
Lower Bound Test	$\mu ABE - 3\sigma ABE - 6\sigma ABE_R$	-72.99	> -100	Pass
P/T Ratio	$(6\sigma ABE_R) / (UTL - LTL)$	0.00	< 0.1	Pass

Table 25. The precision of the GERR test.

The Correlation Criterion is applied to the GERR test results as shown in Table 26. All three conditions hold for the GERR test, therefore the system is determined to be well correlated with the ATE measurements as the gold standard.

Correlation Criterion (GERR)		Value	Desired	Status
Upper Bound Test	$(\mu ABE + 3\sigma ABE + \mu DELTA + 3\sigma DELTA)$	38.01	< 100	Pass
Lower Bound Test	$(\mu ABE - 3\sigma ABE - \mu DELTA - 3\sigma DELTA)$	-86.91	> -100	Pass
P/T Ratio	$(\mu DELTA + 3\sigma DELTA) / (UTL - LTL)$	0.07	< 0.1	Pass

Table 26. The accuracy of the GERR test.

The AutoBench GERR test is hereby shown to be adequately precise and accurate.

5.9 Test Duration

The average time for testing an instrumentation amplifier was determined to be 32 seconds. This time was measured from the onset of the first test routine to the end of the last test routine. Although the test time is an order of magnitude larger than that of ATE, the advantages of having a dedicated system for low volume testing tasks outweigh the increased cost in time.

Chapter 6 Future Work and Conclusions

The AutoBench system measurements of the PSRR, IQ+ and GERR parameters are shown to be comparably precise and accurate to the measurements obtained from standard automated test equipment. The PSRR, IQ+ and GERR measurements are therefore the good tests. The VOS test is shown to be adequately precise, but not satisfactorily correlated with the ATE measurements. The CMRR, IB and IOS tests are also shown to perform marginally based on the analysis criteria. The tests are still good enough for general test functions, such as providing rough measurements for corroborating readings on other systems. The software implemented is dedicated to testing a single channel INA126 amplifier, but can be extended to support other instrumentation amplifiers available from Texas Instruments Incorporated.

The automated system saves engineers time in the volume testing of instrumentation amplifiers at quantities of tens to a few hundreds of devices. The system is capable of performing the DC tests for a device in about 30 seconds. Manual testing of an instrumentation amplifier could take minutes per parameter. The AutoBench system provides a consistent way of testing several devices.

The AutoBench system is designed to be extensible for potential future use to test other integrated circuit device families. Although the cost of the system is roughly 2 orders of magnitude lower than the cost of ATE, the potential extensibility of its functions to other device families further improves the cost savings involved with its implementation.

Further work could be done to improve the performance of the marginal DC tests on the automated bench system. Suggestions for such improvements are discussed below.

6.1 Measuring Resistors

The hardware is designed to support the precision measurement of critical resistors on the INA Test Configuration Board. The IQ test accuracy could be improved by calibrating the value of the DUT power supply resistors R17 and R19, and using the calibrated values in the calculation of the current flowing through the resistors. The calibration could be performed by doing a 4-wire resistance measurement with the DMM.

[14] The current AutoBench implementation assumes the two resistors are 100Ω to a high degree of accuracy, which is not necessarily true.

6.2 Result Averaging

The accuracy of the parameter test results could be further improved by repeating each parameter test and averaging the values. The averaging of multiple readings is generally a good way to minimize the effects of sporadic environmental noise that has a good chance of corrupting a single reading.

6.3 Optimization of Delays

Time delays are used in many of the software subVIs written for the system, to allow for signals to attain steady states before they are measured. The time delays are used to avoid measuring unwanted transient effects, since we are interested in the direct current parameters that describe an instrumentation amplifier in steady state operation. Generally, longer time delays are used in the subVIs than necessary for the sake of caution. The longer delays increase the execution time for performing the parameter tests. Optimizing the delays and removing the unnecessary ones could speed up the time for testing a device.

6.4 Correlation to Manual Bench Readings

The AutoBench system's accuracy could be better described by correlating results with readings obtained by manual bench testing of devices. This is however a time consuming process and the improvement in the accuracy specification is not necessarily assured.

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