An Energy Efficient RF Transceiver for Wireless Microsensor Networks

by

Denis Clarke Daly

Submitted to the Department of Electrical Engineering
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Abstract

A wireless microsensor network consists of a group of sensor nodes that are deployed remotely and used to relay sensing data to the end-user. Due to their remote deployment, large scale wireless sensor networks require a low-power, energy efficient transceiver that can operate for years on a single battery. Existing wireless transceivers designed for low-power wireless standards like IEEE 802.15.4 have difficulty meeting such stringent energy requirements. Thus, a custom on-off keying wireless transceiver for sensor networks has been designed in a 0.18-μm CMOS process.

Power savings are achieved by using an envelope detection based architecture that leverages SAW components and through advanced circuit techniques. The transceiver is power-aware, able to scale power consumption in response to operating conditions. Circuit optimizations are made in both high frequency and baseband circuits to minimize the number of off-chip components and to achieve optimal energy efficiency. A thorough comparison of radio-frequency tuned and untuned gain stages shows that untuned gain can offer energy efficiency advantages in many situations. The transceiver operates in the 900 MHz ISM band at a data rate of 1 Mbps. The receiver's sensitivity is scalable from -37 dBm to -71 dBm with power consumption ranging from 500 μW to 2.4 mW. These power levels correspond to an energy per bit ratio of 0.5 to 2.4 nanojoules per bit, more than ten times smaller than the ratio of typical wireless receivers. The transmitter supports output power levels from -10 dBm to -1 dBm and has a maximum power efficiency of 11%.

Thesis Supervisor: Anantha P. Chandrakasan
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Chapter 1

Introduction

1.1 Wireless Microsensor Networks

A microsensor network consists of a group of sensor nodes that are deployed remotely and used to relay sensing data to the end-user. Applications for sensor networks range from military, such as target tracking, to consumer electronics and industrial equipment, such as home lighting or distributed sensing of factory equipment. There has been extensive wireless microsensor network research in the past decade, on topics including networking protocols [2], energy efficient circuits [3], microelectromechanical systems (MEMS) [4], and full system integration [5, 6]. As sensor networks mature, it is expected that nodes will reduce in size and cost, allowing for the emergence of large scale sensor networks consisting of thousands to millions of nodes. Having millions of such 'dust' sized nodes working together would enable a multitude of revolutionary applications [7].

Figure 1-1 shows a typical sensor network scenario involving target tracking. Each node has an acoustic sensor that listens for the specific acoustic signature of a truck. Once this signature is detected, the nodes communicate wirelessly to determine the location and trajectory of the target. This information is then relayed to a base station for processing.

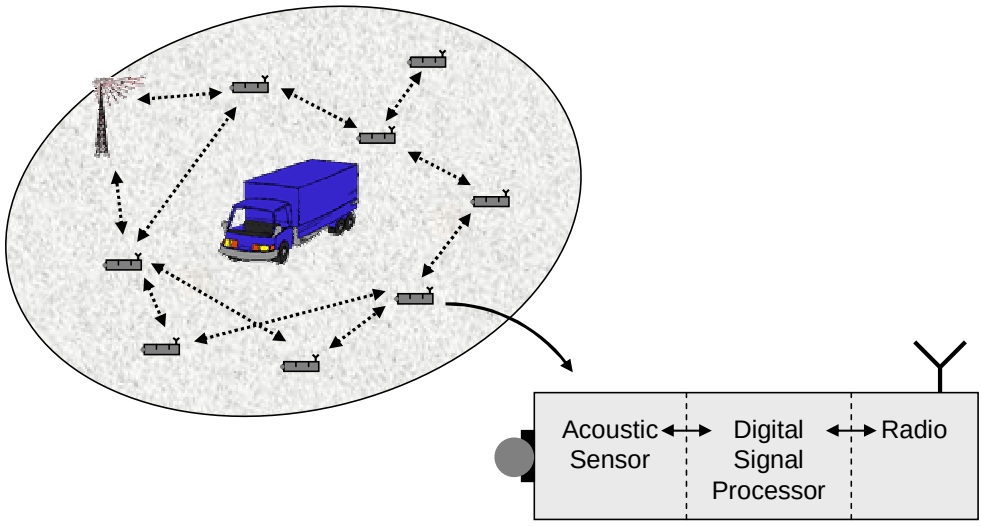


Figure 1-1: A sensor network scenario involving target tracking of a truck

1.2 Breakdown of a Typical Sensor Node

Each sensor node can typically be divided into three key functional blocks: a sensor, a communication device, and a local processing unit. Most sensor nodes rely on both analog and digital circuits to implement these blocks. Analog circuits are well suited for efficiently interfacing with the outside environment whereas digital circuits are better suited for implementing signal processing and communication algorithms. A brief description of a sensor's three key functional blocks follows.

1. Sensor: The sensor's role is to capture data from the environment. For example, an acoustic transducer can be used to 'listen' to the environment for target tracking or vehicle identification. The sensor is often combined with an Analog to Digital Converter (ADC) to convert the analog sensed data to digital data that can be processed by the node.

2. Communication device: The communication device allows the individual nodes to collaborate and form a network. In large scale sensor networks with thousands of nodes, it is often impractical to physically connect each node. Hence, devices must communicate wirelessly, often in the form of radio-frequency or optical communication. This communication does not always need to be bidi-

rectional. Some sensor networks designate nodes as collector nodes that solely sense data and send it to other nodes for processing.

3. Local processing unit: The local processing unit implements the node and network level algorithms. This processing unit is often implemented as a Digital Signal Processor (DSP).

This thesis is focused on the implementation of a communication device for sensor networks. Specifically, it describes the design of an energy efficient wireless transceiver suitable for large scale sensor networks with closely spaced nodes.

1.3 Wireless Transceivers for Sensor Networks

1.3.1 Existing Transceivers

Although wireless technology has existed for almost a century, only in recent years have transceivers appeared suitable for large scale sensor networks [8, 9]. Early transceivers, fabricated with discrete components, were too large and power-hungry. These obstacles have only recently become manageable with the advent of high-speed integrated circuits. Integrated circuits have allowed for radios with high data rates, computationally intensive signal-processing algorithms, and minimal discrete components. The net result of these advances is that wireless transceivers are becoming increasingly energy efficient while at the same time reducing in size.

A key metric for measuring the energy efficiency of wireless transceivers is *energy per bit*, representing the amount of energy required by a transceiver to transmit or receive a single bit of data. To maximize energy efficiency, this ratio should be minimized. Figures 1-2 and 1-3 present the energy per bit values for many low-power radios designed in the past decade. From these figures, we see that energy per bit ratios tend to decrease with increasing data rate, particularly for wireless transmitters. However, higher data rates do not necessarily imply improved energy efficiency. For example, the optimum energy per bit ratio for the receivers presented in Figure 1-3 corresponds to a data rate of 180 kbps.

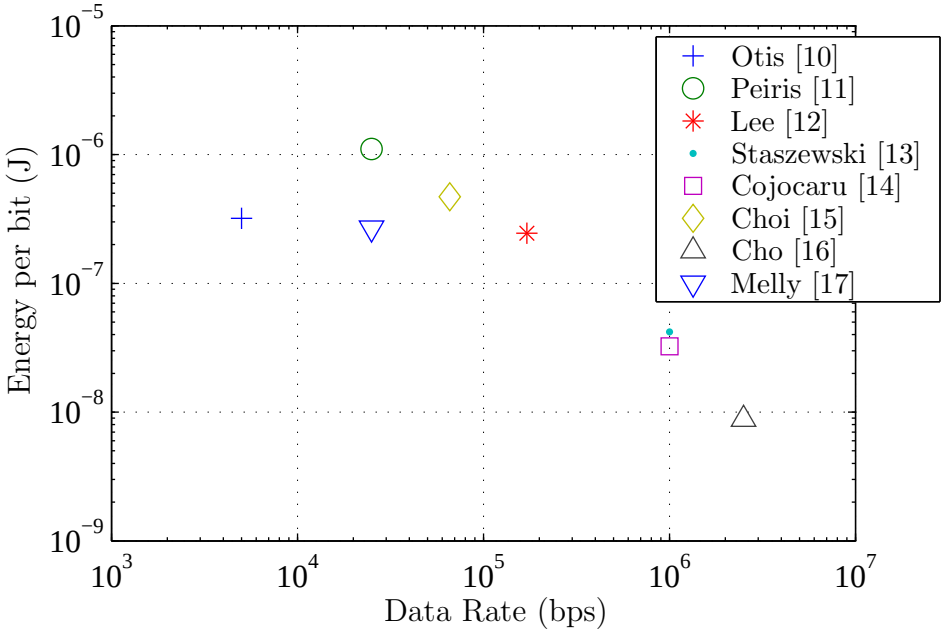


Figure 1-2: Energy per bit ratios for recent wireless transmitters

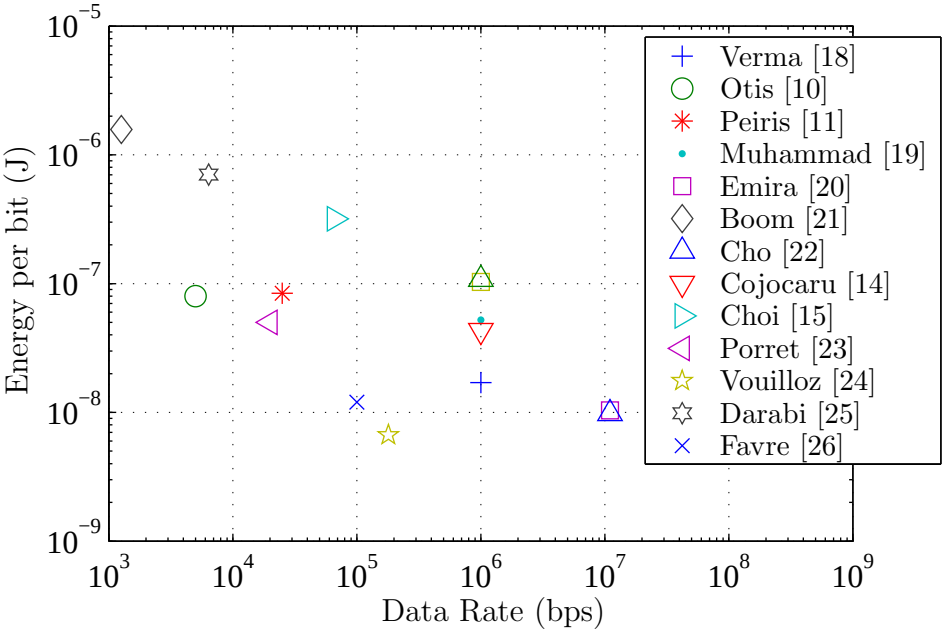


Figure 1-3: Energy per bit ratios for recent wireless receivers

For optimal energy efficiency at low average data rates, a high data rate radio can be duty cycled. In this thesis, duty cycling refers generically to alternating between an active mode and a low-power sleep mode. When a radio is duty cycled, it is important that the sleep mode consumes very little power. Duty cycling allows for a radio with high active mode power consumption to achieve energy efficient operation at a much lower average power level. In practice, however, battery efficiency worsens at higher power levels [27]. For example, if active mode power consumption increases by 2X, then the battery life might decrease by 3X, thereby degrading overall energy efficiency. This effect is particularly noticeable for sensor nodes as they are typically powered by small batteries which cannot efficiently supply large currents. Power-supply capacitors can minimize this problem, but the capacitors increase the cost and size of the sensor node and increase static leakage. Thus, Figures 1-2 and 1-3 only include radios that consume less than 50 mW. For both transmitters and receivers, the lowest energy per bit ratio is approximately 10 nJ/bit.

The energy per bit metric has limitations that must be considered. For the transmitter, the metric does not account for differences in output power and for differences in modulation efficiency. The energy per bit values shown in Figure 1-2 are based on each transmitter's lowest output power level. However, given that the energy per bit metric improves by 100X for high data rate transmitters, the effect of these limitations is not significant enough to change the overall trend.

For wireless receivers, the metric is limited in that it does not account for sensitivity variation. For example, if two radios operate at the same power level and data rate, then they have the same energy per bit ratio, regardless of their respective sensitivities. To a first order, this limitation does not need to be considered because all of the receivers in Figure 1-3 have a good enough sensitivity for short-range sensor applications.

Traditional low-power radios typically can be divided into the following categories: key fobs (e.g. garage door openers), pagers, active Radio Frequency Identification (RFID) tags, low data rate Wireless Local Area Network (WLAN) and Wireless Personal Area Network (WPAN) transceivers and Frequency Modulation (FM) transceivers.

IEEE Standard ***(Industry Name)***	**Purpose**	**Data Rate**
802.11a/b/g	WLAN	$<$ 54 Mbps
802.15.1 *(Bluetooth)*	WPAN	$<$ 1 Mbps
802.15.4 *(Zigbee)*	Low-rate WPAN	$<$ 250 kbps

Table 1.1: IEEE wireless standards for short-range radios

Sensor network radios share many features with the aforementioned radios. Like key fobs and pagers, sensor node radios must operate for months on a single battery and are heavily duty cycled. However, most key fobs and pagers have poor energy per bit ratios, often greater than 100 nJ/bit. There are very few transceivers that are *both* energy efficient and low-power.

1.3.2 Wireless Standards

The IEEE does not have an established standard for wireless sensor networks, however, such a standard would share many features with existing WPAN and WLAN standards. Table 1.1 outlines relevant IEEE WPAN and WLAN standards. The IEEE defines WPANs as having a typical range of 10 meters whereas WLANs can support much larger ranges [28]. Furthermore, WPANs differ from WLANs in that the connections effected via WPANs involve little or no infrastructure.

At the physical layer, the 802.15.4 standard is arguably the most relevant IEEE standard for wireless sensor networks. A key focus of the 802.15.4 standard is low power operation and the ability for low duty cycles. Data rates of 20, 50 and 250 kbps are supported, with 16 channels in the 2.4 GHz Industrial, Scientific and Medical (ISM) band, 10 channels in the 915 MHz ISM band, and 1 channel in the 868 MHz European ISM band. 802.15.4 describes both a physical (PHY) layer of Binary Phase-Shift Keying (BPSK) and Offset Quadrature Phase-Shift Keying (O-QPSK) and a low-level Medium Access Control (MAC) layer including collision avoidance and a handshaking protocol.

Commercial products supporting the 802.15.4 standard have started to be released in the past few years. The ChipCon 2420 radio, released in November 2003, was one

of the first commercial products to support the 802.15.4 standard [29]. The CC2420 is a true single-chip radio based on a low intermediate frequency (IF) receiver and a direct conversion transmitter architecture. It consumes 19.7 mA at ∼3 V in receive-mode and 17.4 mA at ∼3 V in transmit-mode. The CC2420 has been modeled in a sensor network scenario of 1600 nodes, each communicating at 1 kbps, and each node's average power consumption was found to be 211 μW [30]. To achieve such a low average power consumption, the transceiver is aggressively duty cycled, spending 99% of the time in a low-power shutdown mode. In the modeled system, 25% of the total energy is consumed during the contention period. This energy is dominated by the energy associated with turning on and off the receiver. A key conclusion from the paper is that the switching time between transceiver operating modes must be minimized to achieve energy efficient operation.

Despite the promising data reported in [30], the 802.15.4 standard was not designed for networks consisting of hundreds of nodes or networks which require multi-hop communication. Furthermore, the energy per bit ratios of existing 802.15.4 radios is substantially greater than other energy efficient radios. Thus, this thesis proposes a custom wireless architecture for sensor networks that is designed to maximize energy efficiency.

1.4 Microelectromechanical Systems

An area of research that has the potential to revolutionize wireless transceivers for sensor networks is microelectromechanical systems. MEMS devices being developed include low-loss switches, high frequency resonators and filters, and mirrors.

MEMS mirrors could be used in sensor nodes to allow for optical communication. Direct optical communication is extremely energy efficient however directionality is difficult to control. A MEMS mirror could allow for compact, optical communication between two nodes assuming line-of-sight is available [7]. Since optical communication is only suitable for a limited number of applications and not easily compatibility with existing Complimentary Metal Oxide Semiconductor (CMOS) processes, this thesis

focuses solely on Ultra High Frequency (UHF) electromagnetic communication.

1.5 Outline

This thesis describes a custom, energy efficient wireless transceiver designed for sensor network applications. Chapter 2 introduces the proposed architecture and outlines the PHY layer specifications. Next, Chapter 3 describes circuit techniques to maximize the energy efficiency of high frequency gain circuits. Based on the established architecture and using the developed energy efficient techniques, a wireless transceiver is designed in 0.18-μm CMOS. Chapters 4 and 5 outline the design of the receiver and transmitter, respectively. A summary of top-level results along with ideas for future improvements are presented in Chapter 6.

Chapter 2

Transceiver Architecture

2.1 Design Requirements

This thesis proposes custom PHY layer specifications and a custom transceiver architecture, both tailored to the unique requirements facing wireless sensor nodes. Wireless transceivers for sensor networks share many requirements with all electronic circuits including low cost, small size, low power consumption, and energy efficiency. Two additional requirements specific to wireless transceivers are that they be spectrally efficient and be robust to interferers. Since these requirements are often conflicting, it becomes essential to determine their relative value so that appropriate tradeoffs can be made.

For large scale sensor networks to become pervasive, cost is perhaps the most important design requirement. This leads one to a compact, fully integrated node using a standard silicon process. Hence, the size of the integrated circuit and the number of off-chip components must be minimized.

A design requirement that follows from energy efficiency is that the transceiver must be scalable. Since wireless transceivers must operate in widely varying conditions, it is optimal if they can adapt their performance and power consumption to achieve optimal energy efficiency. For example, a sensor node should be able to enter a reduced power 'standby' state in which it only listens for a wake-up signal. A transceiver should also be able to adjust its power consumption in response to the

strength of a communication link.

One of the least important design requirements for many sensor network applications is spectral efficiency. For low data rate applications like acoustic tracking and detection that only require communication at hundreds to thousands of bits per second, the megahertz of bandwidth in the ISM radio bands is ample. By sacrificing spectral efficiency, the transceiver architecture can be greatly simplified and power savings can result.

2.2 Physical Layer Specifications

For a wireless network to properly function, there must exist system specifications that the transceivers conform to. These system specifications exist both at the PHY layer and at a higher, MAC layer. PHY specifications include carrier frequency, data rate, modulation type, sensitivity requirements, and output power limits. MAC specifications include protocol, collision handling and network structure. PHY specifications are much more closely tied to the transceiver's circuit implementation than MAC specifications, and hence, they are the focus of this section.

Physical layer properties of the radios presented in Figures 1-2 and 1-3 are used to help determine optimal modulation and data rate PHY specifications. Tables 2.1 and 2.2 present key PHY properties of the sub 50 mW radios from Figures 1-2 and 1-3.

2.2.1 Carrier Frequency

For commercial acceptance, a wireless transceiver must operate in the ISM radio bands. These radio bands allow for non-commercial as well as license-free wireless communication. In the United States, there are UHF ISM bands from 902 to 928 MHz, 2.400 to 2.4835 GHz, and 5.800 to 5.925 GHz. The 900 MHz ISM band is attractive for wireless sensor networks because of its large bandwidth and relatively low frequency. Transceivers operating at low carrier frequencies typically consume less power than equivalent transceivers at higher frequencies.

Reference	**Type**	**Data Rate (kbps)**	**Power Consumption (mW)**	**Energy per bit (nJ)**
[16]	FSK	2500	22	8.8
[14]	GFSK	1000	32	32
[13]	GFSK	1000	42	42
[12]	GMSK	171	42	246
[17]	FSK	24	6	250
[10]	OOK super-regenerative	5	1.6	320
[15]	GMSK	66	30	455
[11]	FSK/OOK	25	28	1120

Table 2.1: Recent low-power wireless transmitters and their key physical layer specifications

Reference	**Type**	**Data Rate (kbps)**	**Power Consumption (mW)**	**Energy per bit (nJ)**
[24]	OOK super-regenerative	180	1.2	6.7
[26]	OOK super-regenerative	100	1.2	12
[18]	DPSK	1000	17	17
[23]	FSK	24	1	42
[14]	GFSK	1000	43	43
[10]	OOK super-regenerative	5	0.4	80
[11]	FSK/OOK	25	2.1	84
[15]	GMSK	66	21	319
[25]	FSK	6.4	4.5	703
[31]	FM/BPSK	1.2	1.2	1000
[21]	FM	1.3	2	1540

Table 2.2: Recent low-power wireless receivers and their key physical layer specifications

2.2.2 Data Rate

Sensor networks typically have a low average data rate, on the order of hundreds to thousands of bits per second. Low data rate radios have a strong correlation with low power consumption, due to simplified architectures and reduced bandwidths. However, Figures 1-2 and 1-3 show that increased energy efficiency can be achieved by using Mbps data rates and duty cycling the transceiver rather than using kbps data rates [16]. Hence, a data rate of 1 Mbps is proposed. Such a data rate allows for increased energy efficiency while not placing excessive demands on the transceiver. When data rates are too large, the turn-on and turn-off time associated with duty cycling becomes more significant and overall energy efficiency worsens.

2.2.3 Modulation

Traditional cellular systems place a high value on bandwidth efficiency and thus use efficient modulation schemes like Gaussian Minimum-Shift Keying (GMSK) and Differential Quadrature Phase-Shift Keying (DQPSK). A drawback to these modulation schemes is that they typically result in greater transceiver power consumption than less bandwidth efficient modulation schemes like On-Off Keying (OOK) or Frequency-Shift Keying (FSK). OOK and FSK are simpler schemes than GMSK and DQPSK and lend themselves to simpler (and less power hungry) implementations. For instance, an OOK receiver can be implemented using envelope detection, removing the need for a local oscillator and mixer. Figure 2-1 shows a typical OOK signal. A '1' is represented by the carrier being transmitted, whereas a '0' is represented by the absence of the carrier.

An important property of wireless sensor networks is that each node typically operates in receive-mode more often than in transmit-mode. This is due to the bursty nature of communication in sensor networks. Each node must periodically enter receive-mode to see if it needs to receive a packet. Furthermore, each packet transmission requires significant overhead to establish a reliable connection. Thus, for optimal overall energy efficiency of a sensor network, the modulation scheme must

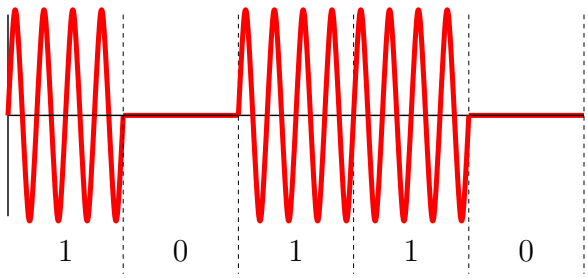


Figure 2-1: 10110 as an on-off keyed signal

minimize receive-mode power consumption.

Based on Table 2.2, OOK and FSK receivers tend to achieve the lowest energy per bit ratios while consuming only a few milliwatts of power. Both OOK and FSK receivers can be implemented in coherent and non-coherent form. A non-coherent, OOK receiver is proposed to enable the use of an envelope detection based receiver. By using a non-coherent receiver instead of a coherent receiver, no oscillator is required for phase synchronization at the receiver. OOK is chosen instead of FSK to allow for a simpler transceiver architecture which only operates at a single frequency.

Two limitations of OOK modulation are that it is spectrally inefficient and that it is strongly susceptible to interferers. The susceptibility to interferers is particularly true with a non-coherent, envelope detection based OOK receiver. It would be trivial to design a jamming circuit to saturate an OOK receiver and prevent it from operating. These two limitations, however, are acceptable given that cost and energy efficiency are the two primary design considerations. For sensor nodes that are deployed in remote environments, there is ample bandwidth available and few interferers.

An additional limitation of OOK modulation is that its ratio of energy per bit (E_b) to noise spectral density (N_0) is 3 dB worse than Phase-Shift Keying. To offset this 3 dB reduction, the receiver's noise figure must reduce by 3 dB. However, for short-range links, it will be shown in Chapter 4 that the receiver is typically not limited by noise but rather by gain. Hence, having noise performance degraded by 3 dB does not significantly affect the overall system and is a worthwhile sacrifice given

the advantages of OOK.

2.2.4 Coding

In an envelope detection based transceiver architecture, coding is typically applied to ensure that the transmitted data has no dc or low frequency components. Otherwise, a one or zero can be repeated indefinitely, potentially causing the receiver to lose synchronization. The receiver also uses these transitions between one and zero to determine the appropriate threshold to differentiate the two signals. Manchester coding is one of many codes that embed the clock in the data to ensure no loss in synchronization and no dc content. Although there exist coding techniques that are more sophisticated and bandwidth efficient that Manchester encoding, we propose using Manchester encoding due to its simplicity and because bandwidth is not a significant constraint.

2.2.5 Transmit Power

The transmit power is defined as the average power into the antenna system of a transceiver. For large scale sensor networks with nodes closely spaced ($\sim$10m), the transmit power need only be a few hundred microwatts to a few milliwatts. Due to the power overhead associated with an oscillator at 915 MHz, it is inefficient to output power less than a few hundred microwatts. The typical transmit power level for 802.15.4 is 1 mW (0 dBm) [32]. Given that a sensor's peak power consumption must be on the order of a few milliwatts, a maximum transmit power level of 0 dBm is proposed. At this transmit power, the power at the receiver can be calculated using the Friis free space equation:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi d}\right)^2 \tag{2.1}$$

In equation (2.1), P_r and P_t represent the power received and transmitted, respectively, G_r and G_t represent the antenna gains, λ represents the wavelength and d

represents the distance between the two antennae. As a conservative estimate, both antenna gains are assumed to be 1. The Friis free space equation assumes that the transmitter and receiver have a clear, unobstructed line of sight between each other. For a transmitter operating at 915 MHz, outputting 0 dBm of power to a receiver spaced 10 meters away, the received power level, P_r is -51.6 dBm. At 20 meters, the received power drops to -57.7 dBm. In practical scenarios there is additional path loss between the transmitter and receiver. This can be modeled by replacing the Friis free space equation with:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi d}\right)^n \tag{2.2}$$

where n represents an empirically determined fitting parameter. After accounting for this additional loss as well as for fading losses, it is reasonable to assume a minimum received power level of -70 dBm for sensor nodes spaced 20 meters at a transmit power of 0 dBm.

2.2.6 Noise Figure

For an OOK waveform at a bit error rate of 10^{-3}, the ratio of energy per bit (E_b) to spectral noise density (N_o) is calculated to be 11 dB [33]. This bit error rate corresponds to the threshold between acceptable and unacceptable performance for a 802.15.1 transceiver [28]. Using the ratio of 11 dB, the required signal-to-noise ratio (SNR) is calculated with the following equation:

$$SNR = \frac{E_b}{N_o}\frac{R}{BW} \tag{2.3}$$

In Equation 2.3, R represents the data rate and BW represents the bandwidth of the signal. For an OOK waveform, $\frac{R}{BW}$ is given to be 0.5 and hence the required SNR is 8 dB [33]. The SNR is reduced further due to the increased bandwidth caused by Manchester encoding, however this effect is ignored. Using the SNR, one can now

Carrier frequency	915 MHz
Data rate	1 Mbps
Modulation	On-Off Keying
Coding	Manchester encoding
Maximum transmit power	0 dBm
Receiver sensitivity	-70 dBm
Maximum receiver noise figure	30 dB

Table 2.3: Summary of physical layer specifications

calculate the maximum noise figure of the receiver using Equation 2.4:

$$P_{r,min} = -174\frac{dBc}{Hz} + 10log(BW_{Hz}) + SNR_{min} + NF \tag{2.4}$$

In equation (2.4), BW represents the noise bandwidth, SNR_{min} represents the minimum SNR required at the output of the receiver, and NF represents the noise figure of the receiver. With a received power level of -70 dBm, a noise bandwidth of 4 MHz for the Manchester encoded OOK signal, and a signal-to-noise ratio (SNR) of 8 dB, one obtains a noise figure of 30 dB. This noise figure is three or four times larger than typical commercial receivers and can be leveraged for power savings.

2.3 Proposed Architecture

In Section 2.2, physical layer specifications for the custom transceiver were proposed. A summary of these specifications is provided in Table 2.3. Based on these specifications, a wireless architecture has been developed (Figure 2-2). The transmitter consists of a Surface Acoustic Wave (SAW) stabilized oscillator, a mixer and a power amplifier. Because the oscillator is stabilized by a SAW resonator, the transceiver only operates at a single carrier frequency. This single channel architecture prevents closely-spaced nodes from transmitting data simultaneously. However, since individual nodes need only communicate at kilobits per second, the 1 Mbps data rate minimizes this limitation. Multiple nodes can share the channel through time-division multiplexing, each communicating at an effective rate of kilobits per second.

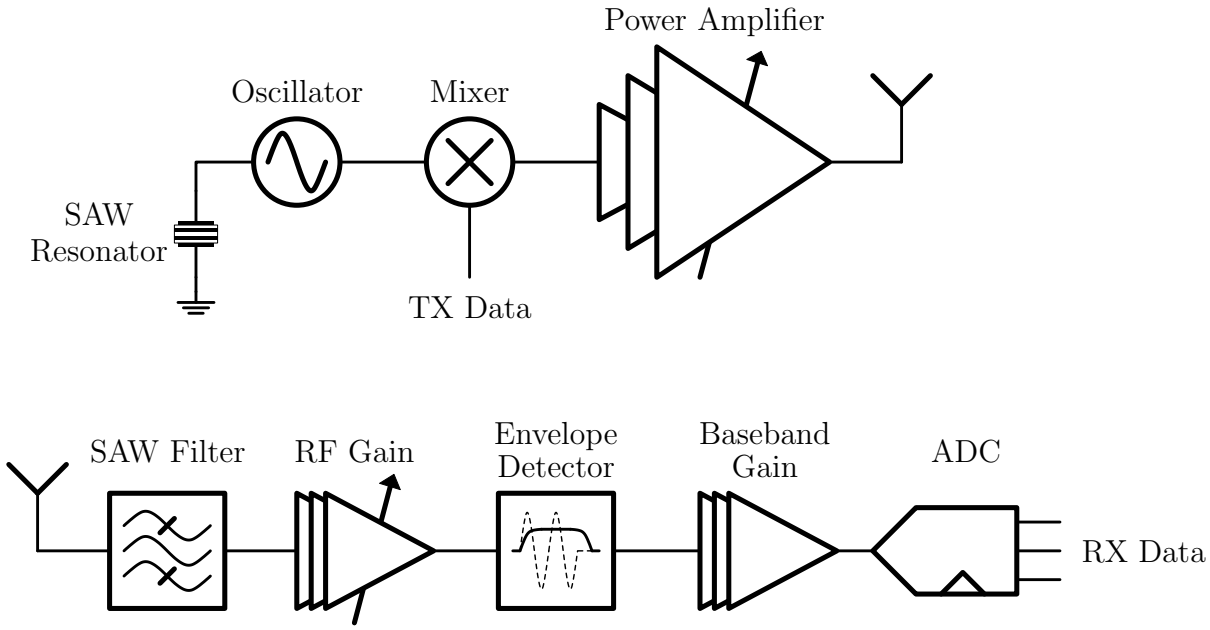


Figure 2-2: Architecture of proposed transceiver

Ideally, the SAW resonator and filter should be replaced by tunable, radio-frequency (RF) MEMS components, however, such components have yet to be realized in a practical form. Even though these components are not yet available, the proposed architecture is still commercially viable for many sensor network applications.

The receiver consists of a SAW filter, a RF gain stage, an envelope detector, a baseband amplifier, and an ADC. The SAW filter is a bandpass filter centered at 915 MHz that serves to filter out interferers. Once interferers have been filtered out, the signal is amplified by RF gain to ensure a sufficient signal swing into the envelope detector. The RF gain is power scalable, able to scale its gain and power depending on the input amplitude. This power scalability allows the receiver to reduce its power consumption when two nodes are spaced closely to one another. Once the envelope of the RF signal has been obtained, it is passed through a baseband amplifier and an ADC. The digital data can then be processed by a baseband processor to recover the data.

2.3.1 Alternate Receiver Architectures

There are many receiver architectures that allow for decoherent OOK reception. This section outlines two alternate architectures, sequential-gain receivers and super-regenerative receivers, and justifies why the continuous-time approach shown in Figure 2-2 is appropriate.

Much like the proposed architecture, sequential-gain receivers extensively leverage SAW components in their design [34, 35]. In a sequential-gain receiver, the RF front-end consists of a SAW filter and RF gain, followed by a SAW delay line and additional RF gain. The SAW delay line allows for the two RF gain stages to be enabled at different times. This sequential-gain approach has two key benefits. First, by having only one of the gain chains active at any time, large RF gain can be achieved with minimal stability concerns. The large RF gain combined with the two SAW filters allows sequential-gain receivers to achieve good sensitivity. Second, by enabling each gain stage for only a part of each bit period, duty cycling is leveraged for power savings.

Super-regenerative receivers have existed since the 1920s and utilize positive feedback to achieve high sensitivity [10, 26, 24]. In a super-regenerative receiver, the RF input is amplified by a positive feedback tuned amplifier that must be periodically quenched. The quench frequency is often many times larger than the data rate of the RF signal. By detecting the envelope of the amplifier's output, the receiver is able to differentiate between a '0' and a '1'.

The primary reason why sequential-gain and super-regenerative architectures are not used in the proposed receiver is that they are more suitable for low data rate, high sensitivity receivers rather than high data rate, low sensitivity receivers. At high data rates, the sequential-gain receiver requires each gain stage to have fast turn on and turn off times, as well as nanosecond level control of the SAW delay line. As the quench rate of a super-regenerative receiver scales with data rate, at high data rates this discrete-time approach becomes challenging. The proposed architecture shown in Figure 2-2 has a continuous-time RF front-end, which scales well to high data rates.

In addition, because the receiver does not require high sensitivity, the architecture does not require such high RF gain that stability becomes a significant concern.

Chapter 3

Energy Efficient RF Gain

3.1 Motivation

Due to their high frequency of operation, RF circuits are rarely biased in the subthreshold region and typically consume a large proportion of power in a wireless transceiver. In the proposed architecture introduced in Chapter 2, RF circuits consist of the RF gain in the receiver and the oscillator, mixer, and power amplifier in the transmitter. In both the receiver RF gain stage and in the transmitter power amplifier, a significant amount of voltage and power gain, respectively, is needed. The receiver RF gain must amplify the input signal to a sufficiently large level such that the envelope detector can function. The power amplifier must buffer the oscillator output such that a 0 dBm on-off keying signal can be transmitted. This chapter introduces circuit techniques to optimize the energy efficiency of RF gain.

3.2 RF Gain Design Considerations

When designing RF gain, there are several design constraints that must be considered including total gain, linearity, and input-referred noise. All of these constraints should be analyzed with a focus on how to maximize energy efficiency.

3.2.1 Total Gain

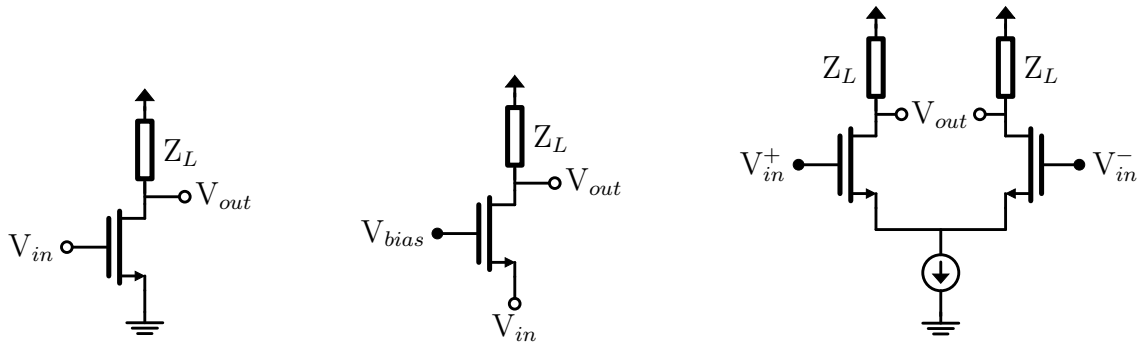
The receiver's requirement for total gain is set by the minimum input power level and the minimum input signal level required by the envelope detector. Based on Chapter 2, the receiver has a minimum OOK input signal level of -70 dBm. A -70 dBm OOK waveform consists of a -67 dBm sinusoid with 50% duty cycle. Assuming the SAW filter has an insertion loss of 3 dB, then the average input signal level drops to -73 dBm. At the antenna's impedance of 50 Ω, this corresponds to a 50% duty cycle sinusoid with an amplitude of 100 μV.

Envelope detectors are typically implemented with a rectifier followed by a peak detector. The minimum signal required by the envelope detector is determined by the implementation of the rectifier. The majority of rectifiers used in envelope detectors are passive, using a *pn* or Metal Oxide Semiconductor (MOS) diode. The envelope detector is designed so that its minimum output swing is 5 mV pk-pk. To achieve such a output swing, the envelope detector requires an input amplitude of approximately 30 mV (This result is derived in Chapter 4).

Based on the minimum input amplitude of 100 μV and the minimum envelope detector input amplitude of 30 mV, the maximum required RF gain is calculated to be 300. The minimum required RF gain is set by the dynamic range specification. For a dynamic range specification of 40 dB, the maximum input signal is -30 dBm, which corresponds to an input amplitude of 10 mV. To meet this dynamic range specification, the minimum required RF gain is 3. To achieve optimal energy efficiency over the wide (40 dB) dynamic range, it is apparent that the RF gain must be scalable. For example, when the input signal is large, RF gain blocks can be disabled to reduce power consumption.

3.2.2 Linearity

In an on-off keying system, linearity is not a significant concern in either the receiver or the transmitter. This is in contrast to transceivers that use multi-level amplitude modulation techniques like 8-Quadrature Amplitude Modulation (QAM), where any



(a) (b) (c)

Figure 3-1: Low-voltage RF gain topologies: (a) common-source amplifier, (b) common-gate amplifier, and (c) differential pair

non-linearity can severely degrade performance. In an 8-QAM transceiver, the voltage supply is often raised to increase the voltage headroom and improve linearity. In an on-off keying system, the voltage supply can be lowered to one Volt with almost no performance penalty.

There are several low-voltage circuit topologies than can be used to implement RF gain. Figure 3-1 shows three possible circuit topologies: a common-source amplifier, a common-gate amplifier and a differential pair.

For all three topologies, the dc voltage drop across the load, Z_L, is 0V or IR depending on whether the load is tuned or untuned, respectively. The additional voltage drop across each transistor, V_{DS}, must be greater than 100 mV for the transistors to remain biased in saturation. Thus, the circuits shown in Figure 3-1(a), Figure 3-1(b) and Figure 3-1(c) have a minimum supply voltage of $V_{DS} + V_{load}$, $V_{DS} + V_{load}$ and $2V_{DS} + V_{load}$, respectively. Even though the differential pair requires a larger supply voltage than the other two topologies, its advantages of improved power-supply rejection and common-mode rejection outweigh the increase in power consumption.

3.2.3 Input-Referred Noise

One difference between envelope detection based receivers and mixer based receivers is that total input-referred noise replaces noise figure as an important metric. This

is because an envelope detector is affected by the sum of noise over all frequencies whereas mixer based receivers translate high frequency noise down to baseband and then filter out unwanted frequency bands. In an envelope detection based receiver, the input-referred noise must be sufficiently small such that it does not result in a bit-error. The input-referred noise can be easily calculated from the required signal-to-noise ratio of 8 dB and the input power level. Given an input power level of -70 dBm at 50 Ω, the total input-referred noise of the RF gain must be less than 20 μV Root Mean Square (RMS).

3.3 Energy Efficiency Metric for RF Gain

A common approach to optimize the energy efficiency of a single gain stage is to minimize power consumption while meeting a minimum gain specification. Such a technique, however, can not be applied to situations when the gain requirement is sufficiently high that multiple stages are needed. To quantify the energy efficiency of gain in such situations, a metric is introduced. A fundamental tenet of the metric is that only the total gain and power consumption affect energy efficiency. Other factors such as the number of gain stages, power supply rejection, input-referred noise and linearity are not modeled in the metric. Given an efficiency metric E, this tenet implies that:

$$E = f(Gain, Power) \tag{3.1}$$

A second tenet of the efficiency metric is the number of times a stage is cascaded has no effect on its energy efficiency. This makes sense because it allows for a fair comparison between different gain blocks, regardless of how many stages are cascaded. Thus, the efficiency metric can be used for both single-stage and multi-stage gain topologies. Given n identical gain stages cascaded, each with gain of G and power P, the second tenet implies that:

$$\frac{dE}{dn} = \frac{df(G^n, nP)}{dn} = 0 \tag{3.2}$$

These tenets are shown graphically in Figure 3-2. The following metric for the energy

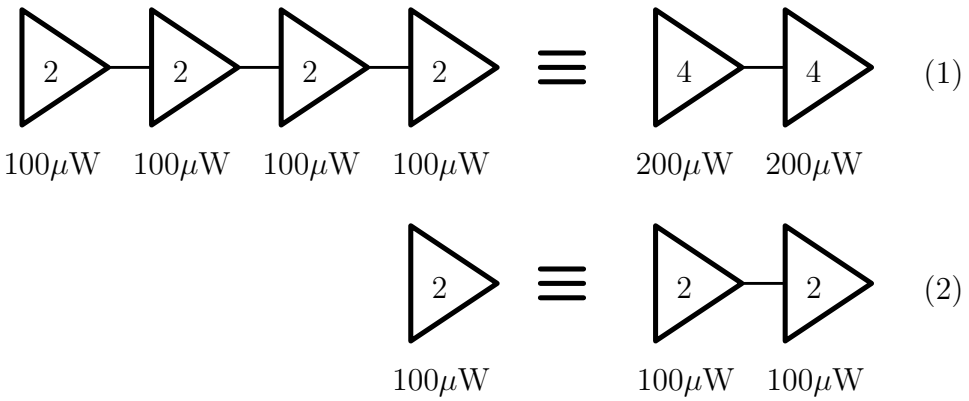


Figure 3-2: Key tenets of efficiency metric

efficiency of gain stages satisfies both tenets:

$$E = f(Gain, Power) = \frac{log(Gain)}{Power} \tag{3.3}$$

This metric can be intuitively explained by noting that for cascaded, identical gain stages, the total gain increases exponentially with the number of stages whereas power consumption increases linearly. Hence, the metric is proportional to the logarithm of gain and inversely proportional to power consumption.

3.4 Tuned vs. Untuned RF Gain

Tuned circuits are used in nearly every radio design as they typically offer better performance than untuned circuits. Tuned circuits are circuits that contain both inductors and capacitors to form a resonant load. Figure 3-3 shows an example of a tuned and an untuned RF gain stage.

In the tuned gain stage shown in Figure 3-3(a), R_1 represents the parallel resistance of the LC tank. The single-ended input-output transfer function is given by the second-order, bandpass equation:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-j\omega g_{M1} L_1}{1 + j\omega \frac{L_1}{R_1} - \omega^2 L_1 C_1} \tag{3.4}$$

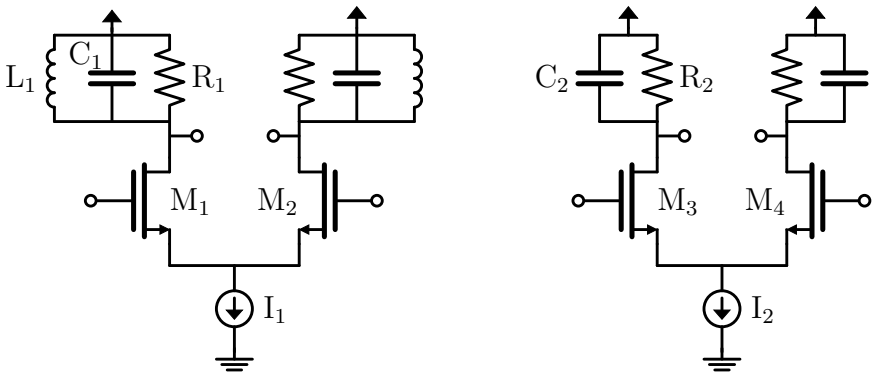


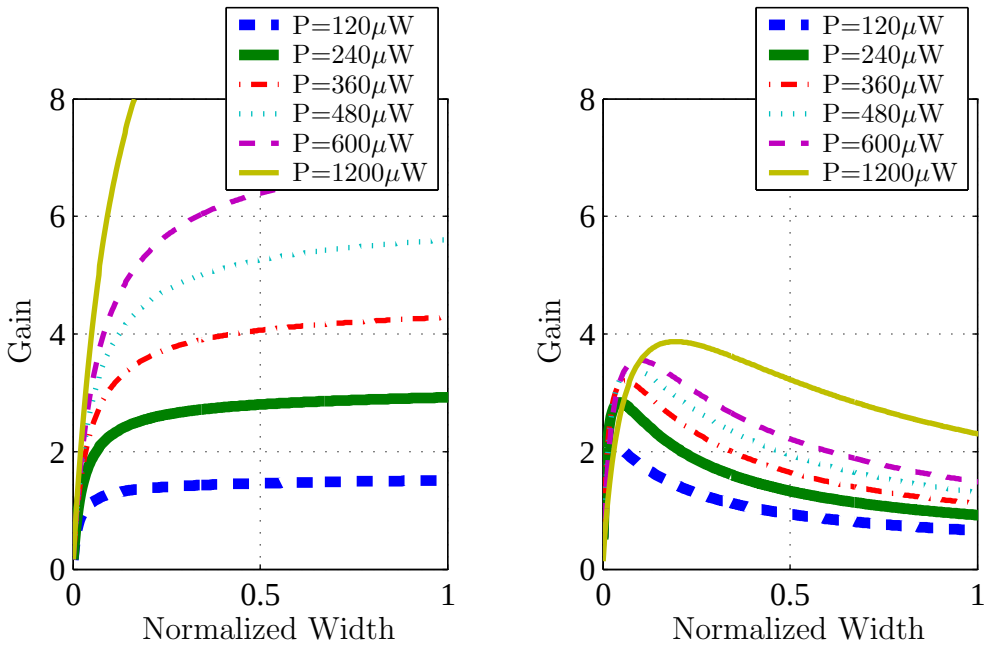
Figure 3-3: (a) Tuned and (b) untuned RF gain circuits

Nearby the resonant frequency $\omega_0 = \frac{1}{\sqrt{L_1 C_1}}$, the gain of the tuned circuit is $-g_{M1}R_1$. Thus, to maximize the magnitude of the tuned circuit's gain, the parallel, parasitic resistance of the LC tank should be maximized. In typical implementations, this resistance is determined by the lossiness of the inductor. 5 nH inductors with quality factors of 4 and 30 at 915 MHz have a parallel resistance of 122 Ω and 863 Ω, respectively. A quality factor of 4 is typical for on-chip inductors at 915 MHz and a quality factor of 30 is typical for off-chip inductors. An additional requirement to maximize gain is that the resonant frequency of the LC tank should be centered at the frequency of operation. As it is difficult to predict the inductance of both on-chip and off-chip inductors, the capacitance often needs to be tunable.

In the untuned gain stage shown in Figure 3-3(b), C_2 represents the capacitance loading the output. It consists of parasitic capacitance of the resistor R_2, the drain capacitance of transistor M_3, wiring capacitance and the input capacitance of the following stage. The single-ended input-output transfer function is given by the first-order, lowpass equation:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_{M3}R_2}{1 + j\omega R_2 C_2} \tag{3.5}$$

Since Equation 3.5 is lowpass, the magnitude of the gain decreases monotonically with frequency. At 915 MHz in the provided 0.18-μm CMOS process, the load capac-



(a) (b)

Figure 3-4: (a) Tuned and (b) untuned gain versus normalized input transistor width

itance C_2 is sufficiently low that the optimum energy efficiency of the untuned gain stage is comparable to the tuned gain stage with a quality factor of 30. The energy efficiency metric proposed in Section 3.3 is used to analyze the energy efficiency of a single gain stage.

To measure the energy efficiency of the tuned gain stage in Figure 3-3(a), the resonant load is assumed to be 800 Ω. A resonant load of 800 Ω corresponds to a tank quality factor of approximately 28 for typical tank configurations. The current I_1 is swept over various values and the width of transistors M_1 and M_2 is also varied. To measure the energy efficiency of the untuned gain stage, a voltage drop of 0.4 V across the load resistors is first assumed. The current I_2 is swept over various values and the width of transistors M_3 and M_4 is varied. To accurately model the capacitive loading at the output of the untuned gain stage, identical untuned gain stages are cascaded. Furthermore, a fixed interconnect capacitance of 50 fF is assumed and the polysilicon resistor parasitic capacitance is included.

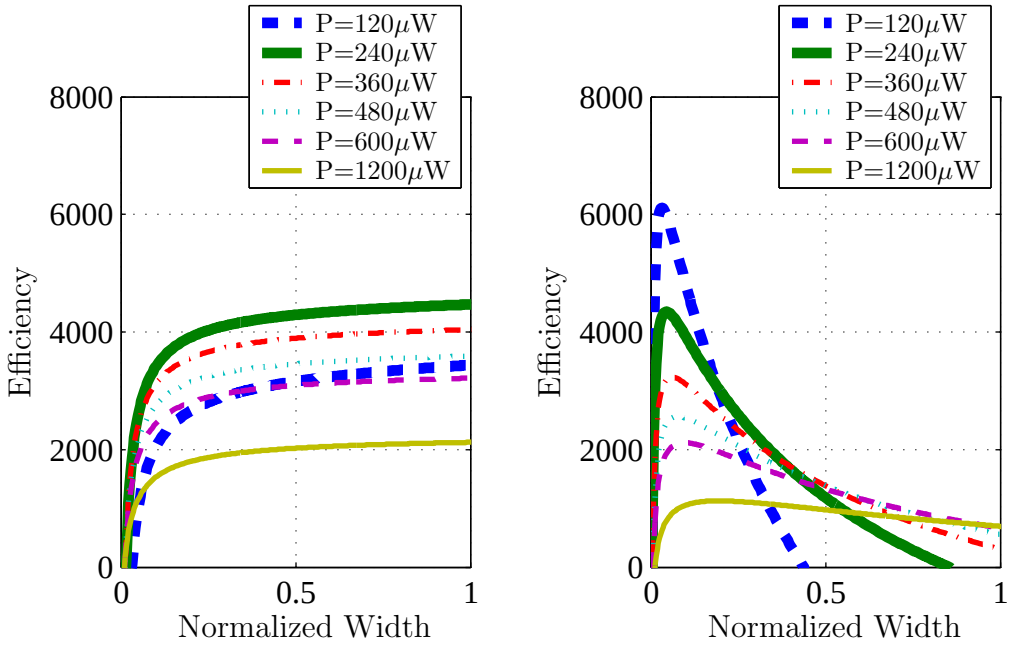


Figure 3-5: Efficiency of (a) tuned and (b) untuned gain versus normalized input transistor width

Figure 3-4 presents the HSPICE simulation results for the tuned and untuned gain. For the tuned gain stage shown in Figure 3-4(a), the gain increases with increasing transistor width. This increased gain is caused by improved transconductance efficiency due to lower current densities. The gain is approximately proportional to power consumption.

The untuned gain results shown in Figure 3-4(b) behave quite differently from the tuned gain. For each power level, there is an optimum transistor width which maximizes the gain. At lower widths, reduced transconductance efficiency lowers the gain. At higher widths, the increased load capacitance lowers the 3-dB frequency and hence the gain. The maximum achievable gain increases with power consumption, but at a much slower rate than the tuned gain.

Using the gain and power consumption data shown in Figure 3-4, Figure 3-5 presents the corresponding energy efficiency of the tuned and untuned gain stages. We see that at 915 MHz in the given 0.18-μm CMOS process, the maximum en-

ergy efficiency of an untuned, resistively loaded differential pair is superior to that of a tuned differential pair with a resonant load of 800 Ω. The maximum efficiency of the tuned gain stage occurs at a power consumption of 240 μW and the maximum efficiency of the untuned gain stage occurs at a power consumption of 120 μW. The maximum efficiency of the untuned gain stage is roughly 35% larger than the maximum efficiency of the tuned gain stage.

Even though untuned gain stages have greater energy efficiency than tuned stages, there are problems that limit their use. Due to process variations like V_T mismatch and temperature variations, the output voltage of an untuned gain stage can be offset from its nominal value. If untuned gain stages are cascaded, this offset can saturate the amplifier. Another problem facing untuned gain stages is that they typically have a higher input-referred noise than tuned gain stages. The higher input-referred noise is caused because an untuned gain stage often has a wider effective bandwidth than a tuned gain stage due to its first-order, RC roll off.

Based on the aforementioned conclusions, two RF gain architectures are proposed. The first architecture consists of a single, tuned gain stage followed by several, offset compensated untuned gain stages. The second architecture consists of alternating tuned and untuned gain stages. The following section outlines the proposed architectures and discusses their advantage and disadvantages.

3.5 Proposed RF Gain Architectures

3.5.1 Cascaded Untuned Gain Stages

As shown in Section 3.4, untuned gain stages offer several advantages over tuned gain stages, most notably improved energy efficiency and reduced area. However, they traditionally suffer from dc offsets and high input-referred noise. One other constraint that limits their use is that their power efficiency significantly degrades if their load capacitance increases.

To minimize the effect of dc offsets, it is possibly to employ offset compensation

techniques. These techniques are typically broken down into four approaches:

1. Continuous-time, input compensation
2. Discrete-time, input compensation
3. Continuous-time, output compensation
4. Discrete-time, output compensation

In a RF receiver front-end where packets can last for microseconds, discrete-time offset compensation is typically impractical because any loss in synchronization can cause a packet loss. This is particular true with high-data rate radios, because there is less time between bit periods to do offset cancellation. Thus, a continuous-time compensation approach is preferred. Input and output compensation are both feasible, but must be designed to minimize the capacitive loading on the output of each stage. A circuit that meets these guidelines is shown in Figure 3-6. The circuit implements continuous-time, input offset compensation by ac coupling the sources of the two input transistors rather than connecting them directly. This causes the circuit to become a bandpass rather than lowpass amplifier. The capacitor C_0 introduces a pole-zero pair into the input-output transfer function, which can be approximated as:

$$H(s) = \frac{V_{out}}{V_{in}} = \left(\frac{-g_M R_L}{1 + j\omega R_2 C_2}\right)\left(\frac{j\omega}{j\omega + \frac{g_M}{2C_O}}\right) \tag{3.6}$$

The capacitor C_0, which is inversely proportional to the pole at $g_M/2C_0$, is sized based on several constraints. The pole must be sufficiently low that it does not reduce gain at 915 MHz. However, if the pole is too small, then the top and bottom-plate parasitic capacitances of C_0 will decrease the high frequency, input common-mode rejection of the circuit. Additionally, the pole cannot be so low that the time-constant of the circuit is exceedingly long.

The noise performance of the proposed amplifier is similar to a common-source amplifier at low frequencies and a differential pair at high frequencies. Thus, the thermal noise and 1/f noise introduced by the current sources I^+ and I^- will appear

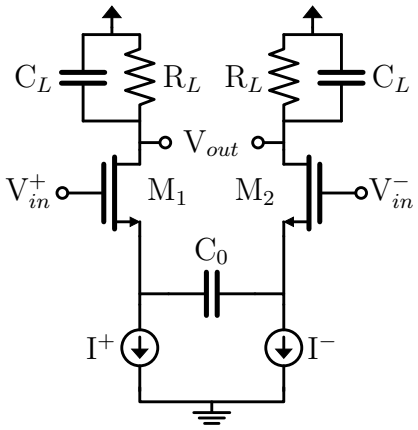


Figure 3-6: Offset compensated RF untuned gain

at the output at low frequencies, but not at high frequencies. The input transistors M1 and M2 will contribute noise to the output at high frequencies but not at low frequencies. The load resistors R_L contribute noise at all frequencies. For a load resistance of 4 kΩ and a total current of 200 μA, the total input-referred noise for the proposed architecture is approximately 500 μV, compared to 250 μV for a traditional differential pair with the same load resistance and total current.

Even though the input-referred noise for a single stage of the proposed amplifier is worse than a traditional differential pair, a single-stage of gain is only needed when the input signal is relatively large and noise constraints can be easily met. For example, a single-stage of gain is used to amplify a 10 mV signal to a 30 mV signal. In this case, the input-referred noise of 500 μV is many times smaller than what is required. At smaller input signal levels, multiple gain stages must be cascaded and the input-referred noise becomes more critical a constraint. Due to the bandpass response of the proposed untuned amplifier, when cascading multiple gain stages, the overall noise performance improves and becomes significantly superior to that of a traditional differential pair. This is because the low frequency noise of early stages is filtered by later stages. In traditional differential pairs, low frequency noise is amplified by later stages, often more so than the high frequency signal of interest. When cascading multiple stages of the proposed circuit, the input-referred noise lowers to approximately 300 μV whereas the input-referred noise of cascaded traditional

differential pairs rises to over a millivolt. Decreasing C_0 has the effect of reducing the effective bandwidth of the amplifier, and input-referred noise decreases monotonically with decreasing C_0. This is because the effective bandwidth of the circuit is reduced as the pole at $g_M/2C_0$ increases.[1]

To meet the sensitivity requirement of -70 dBm, the input-referred noise of the receiver must be less than 20 μV. Clearly, the input-referred noise of the proposed architecture is too large to meet this requirement. One solution is to first amplify the input by a tuned, low-noise amplifier and then cascade multiple untuned gain stages. In this case, the Low Noise Amplifier (LNA) needs to provide at least 23dB of voltage gain to meet the sensitivity requirement. By cascading a tuned amplifier with an untuned differential to single-ended converter, sufficient gain can be achieved to lower the input referred noise to below 20 μV. Figure 3-7 shows a block diagram of the proposed architecture. To minimize the input-referred noise of the chain, additional current is supplied to the differential to single-ended converter than to each of the following untuned gain stages.

The topology shown in Figure 3-7 supports scalability through power gating. At the lowest gain setting, only the LNA is enabled. At higher gain settings, a variable number of untuned gain stages are also enabled. Since the topology has different output nodes depending on which gain setting is enabled, there must be an additional circuit that selects the appropriate output. Implementation details of this topology are presented in Chapter 4.

3.5.2 Alternating Tuned and Untuned Gain

Although the architecture described in Section 3.5.1 demonstrates the feasibility of cascading multiple untuned gain stages, there are several compelling reasons to still use tuned gain. One such reason is that tuned gain can drive large capacitive loads without suffering a degradation in efficiency. If the RF gain must drive a capacitive load of hundreds of fF, then untuned gain no longer becomes more energy efficient.

[1] Actually, at very small values C_0 (tens of fF), the gain of the circuit at 915 MHz becomes so small that the input-referred noise increases

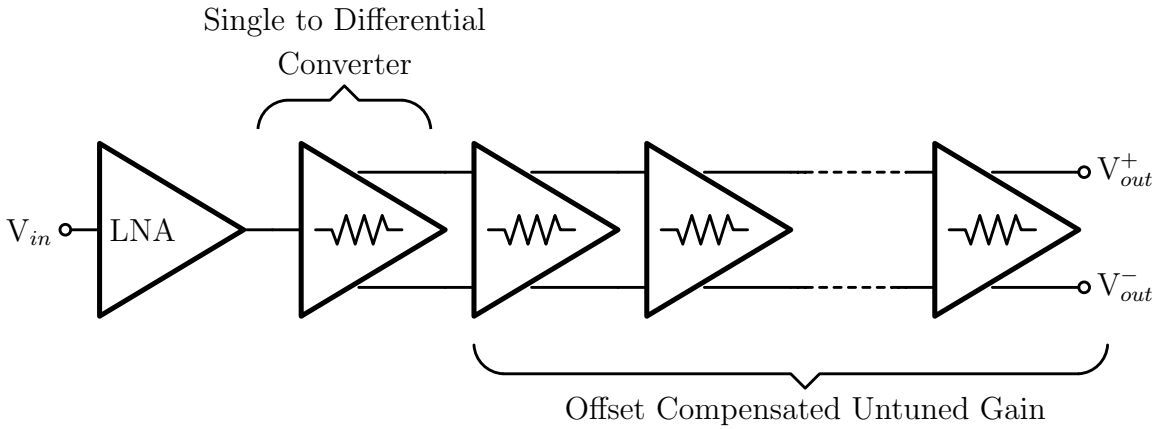


Figure 3-7: Cascaded untuned gain topology

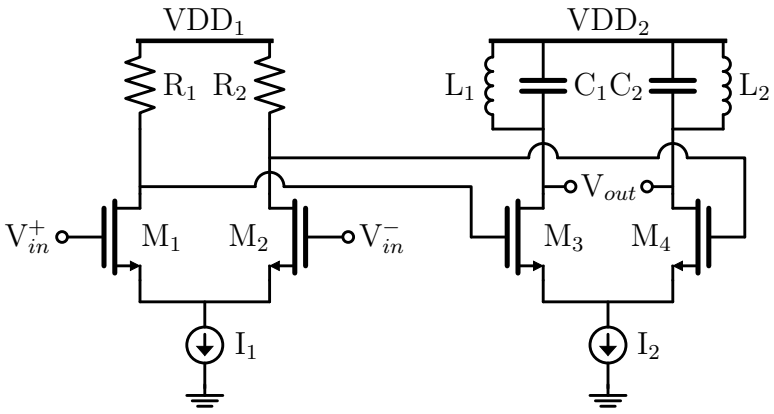


Figure 3-8: Proposed gain stage consisting of tuned and untuned gain

Two additional reasons are the improved noise performance and the inherent output offset cancellation of tuned gain. To combine the advantages of tuned and untuned gain, an architecture of alternating tuned and untuned gain is proposed. Figure 3-8 shows a circuit implementation of alternating tuned and untuned gain.

When alternating tuned and untuned gain, one notes that the input capacitance of the tuned amplifier directly affects the gain of the untuned amplifier whereas the input capacitance of the untuned amplifier has a negligible effect on the tuned amplifier as it is resonated out. Figure 3-9(a) plots the efficiency of the tuned gain versus input capacitance (which is roughly proportional to input transistor width) and Figure 3-9(b) plots the efficiency of the untuned gain versus load capacitance. To vary input capacitance of the tuned gain, the width of transistors M_3 and M_4 was varied. For the

tuned gain, a load impedance of 800 Ω is assumed. To model wiring capacitance for the untuned gain, a fixed 50 fF capacitance is included in parallel with the varying load capacitance. This varying load capacitance is identical to the varying input capacitance of the tuned gain amplifier.

We see that tuned gain increases monotonically with increasing input capacitance. This is due to increased transconductance efficiency with increasing transistor width. In contrast, the untuned gain decreases monotonically with increasing load capacitance. This gain reduction is because the dominant pole lowers in frequency with increasing load capacitance.

To determine the optimal configuration of the untuned and tuned gain, the two efficiency plots of 3-9 can be combined by extending the efficiency metric given in Equation 3.3:

$$\text{Efficiency} = \frac{log(Gain_{tuned} \times Gain_{untuned})}{Power_{tuned} + Power_{untuned}} \tag{3.7}$$

This efficiency metric groups the untuned and tuned gain into a single stage. Using this metric, the optimal capacitance and associated efficiency is found for each current combination for the tuned and untuned gain. The optimal efficiency points are presented in contour form in Figure 3-10, showing that the optimal power per stage is roughly 160 μW for each tuned gain and 240 μW for each untuned gain. This corresponds to an untuned gain of 3 and a tuned gain of 1.7. Hence, 3 stages of cascaded untuned and tuned gain are required to achieve a gain greater than 300. To reduce the number of required stages, the power supplied to the tuned and untuned gain can be increased, thereby increasing the gain per stage, while only reducing efficiency by a small amount.

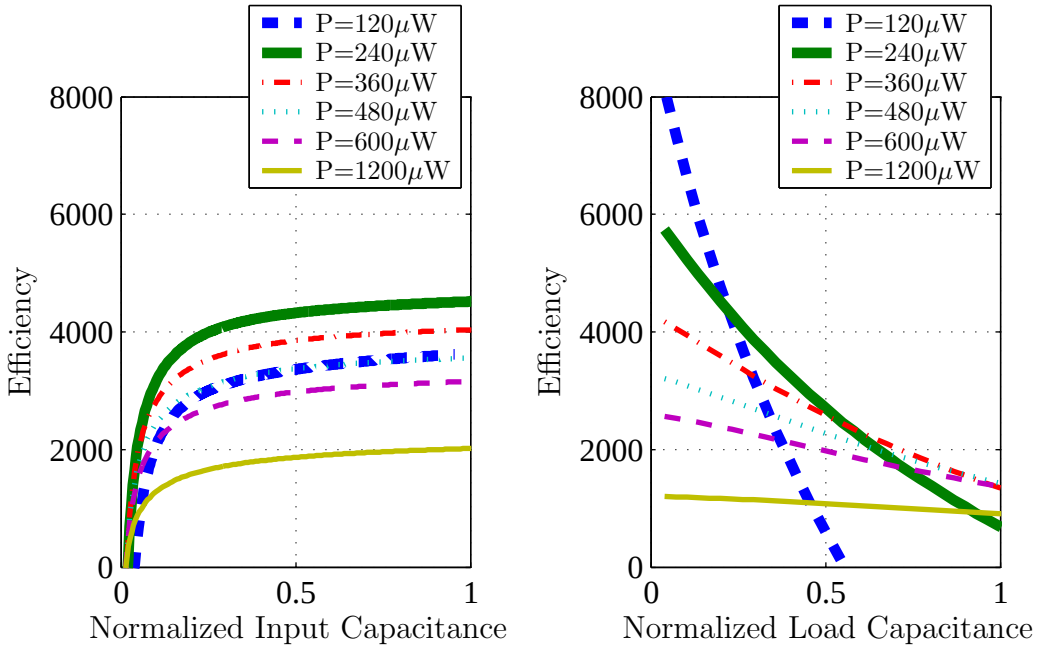


Figure 3-9: (a) Efficiency of tuned gain vs. normalized input capacitance and (b) efficiency of untuned gain versus normalized load capacitance

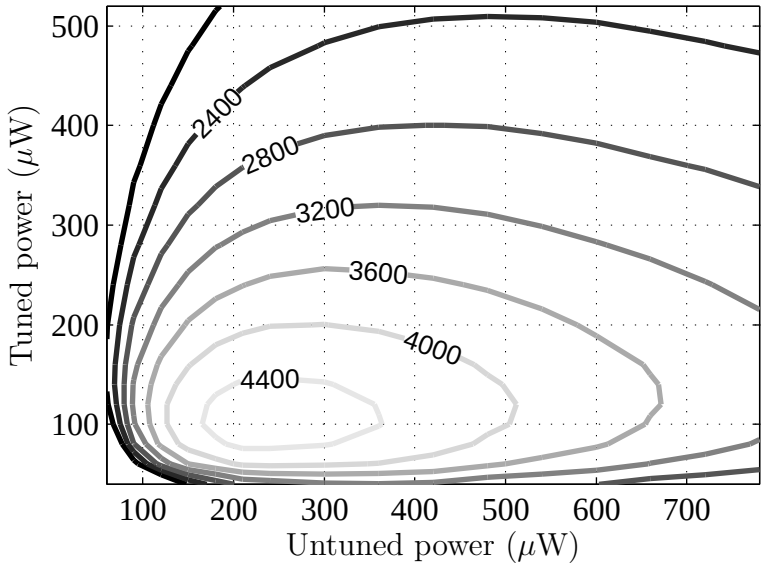


Figure 3-10: Optimal efficiency contours as a function of tuned and untuned power per stage

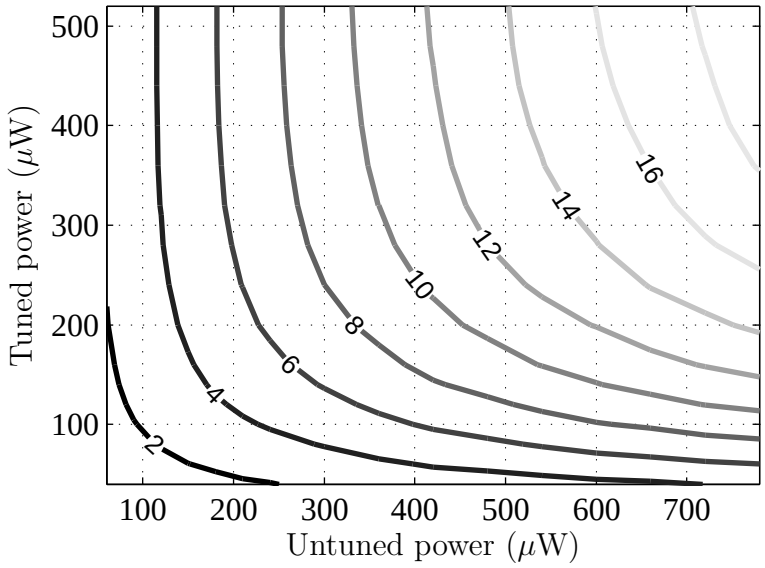


Figure 3-11: Gain corresponding to optimal efficiency contours as a function of tuned and untuned power per stage

Chapter 4

Receiver Implementation

4.1 Overview

A block diagram of the envelope detection based OOK receiver is presented in Figure 4-1. The RF input from the antenna first passes through a SAW filter to attenuate interferers. After the filter, the RF signal is amplified by a LNA and by scalable, untuned gain. Once the OOK signal is sufficiently amplified, it is converted to a baseband signal by an envelope detector. As the envelope detector output swing is nominally only 5 mV, its output is amplified by a three stage, offset compensated baseband amplifier. Finally, the amplified baseband signal is converted to a 3-bit digital signal by a FLASH ADC.

4.2 Low Noise Amplifier

To allow for good receiver sensitivity, the input signal is first amplified by a LNA. The common-gate LNA shown in Figure 4-2 is chosen because at low current levels it is less sensitive to unaccounted parasitics than a common-source LNA [25]. The gain of the LNA can be approximated by the following equation:

$$Gain = R_L\sqrt{\frac{g_{M1}}{50\Omega}} \tag{4.1}$$

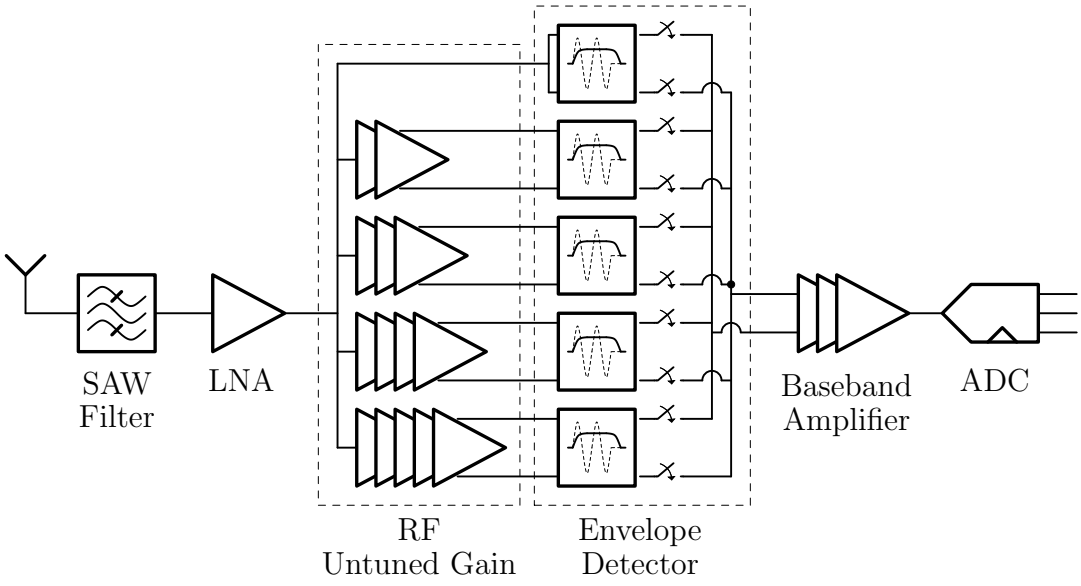


Figure 4-1: Receiver architecture

From Equation 4.1, we see that R_L, the resistance of the load, is the factor with the strongest relationship to gain. To maximize R_L, the load inductor L_3 is implemented as an off-chip, high-Q inductor. This inductance is significantly affected by bondwire and printed circuit board parasitics. Hence, to ensure the LC tank is tuned to 915 MHz, the load capacitor, C_2, must be tunable. To achieve a sufficiently large tuning range with reasonably large quality factor, the load capacitor is implemented as an on-chip accumulation mode capacitor. By adjusting $V_{bias,2}$, the center frequency of the resonant load can be tuned to 915 MHz. Inductor L_2 and capacitor C_1 form a lowpass impedance matching network. They are sized to match the 50 Ω antenna impedance to the $1/g_{M1}$ input impedance of transistor M_1. Capacitor C_1 is an on-chip poly-poly capacitor.

The LNA nominally consumes 400 μA at 0.8 V. The input matching network transforms the 50 Ω input impedance to 150 Ω while achieving a voltage gain of 1.7. In simulation, the LNA load is modeled as an 800 Ω resistor in parallel with an LC tank, corresponding to a tank Q of approximately 28. The LNA has a simulated voltage gain of 17 dB at 915 MHz and a simulated power gain of 6 dB. The total integrated input-referred noise is 10 μV. The 1-dB compression point of the LNA is

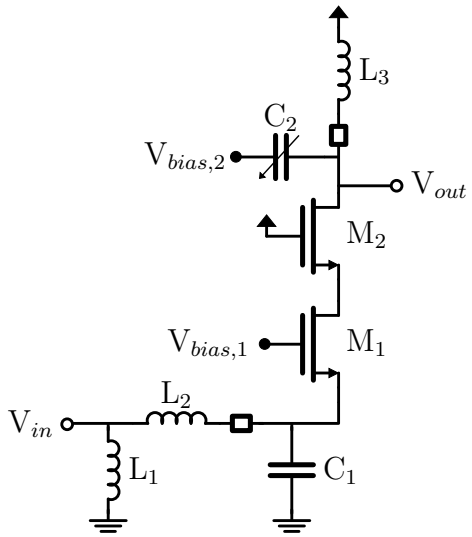


Figure 4-2: Low Noise Amplifier schematic

-10 dBm and the input IP_3 is -1 dBm.

4.3 RF Gain

To minimize the number of off-chip components required, the cascaded untuned gain architecture described in Section 3.5 is implemented. The architecture is scalable to achieve optimal energy efficiency over a large operating range. To reduce power consumption, voltage scaling is leveraged. The LNA is supplied 0.8 V and all untuned amplifiers are supplied 1.2 V. As it is often not possible to support multiple analog supply voltages, the LNA can also operate at 1.2 V with only a small increase in overall power consumption.

The cascaded untuned gain architecture consists an LNA followed by four separate chains of cascaded, untuned amplifiers. The first untuned amplifier in the each chain is a simple differential pair to convert the LNA single-ended output to a differential signal. All of the following untuned amplifiers in the chain are offset compensated, as shown in Figure 3-6. Figure 4-3 presents a block diagram of the architecture. The architecture leverages parallelism to minimize capacitive loading on the untuned amplifiers. Instead of having a single chain of amplifiers and loading each output with

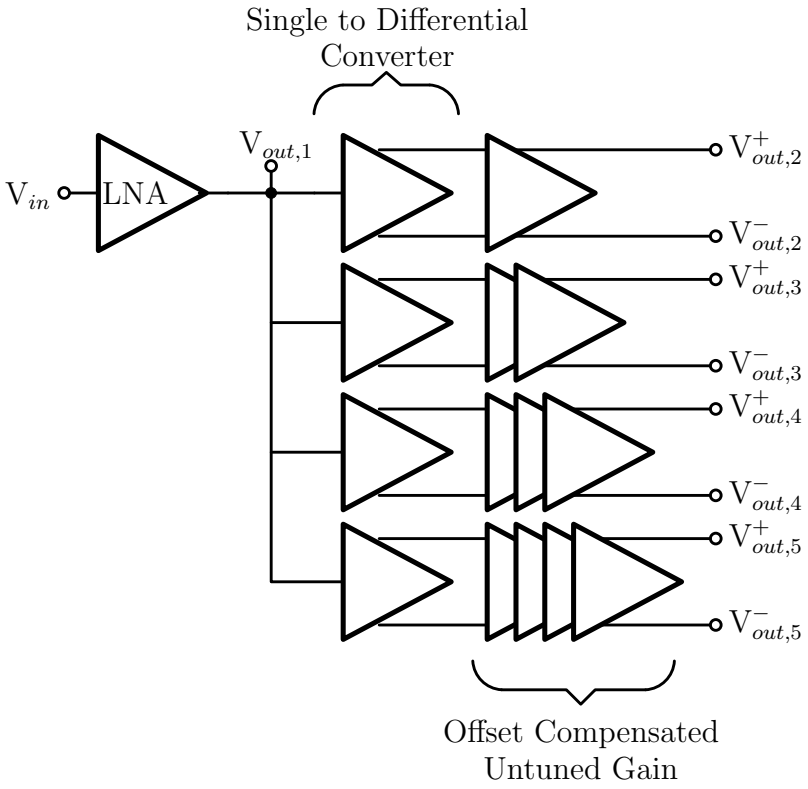


Figure 4-3: RF gain architecture

an envelope detector, multiple chains of amplifiers are used. Only a single chain is active at a given time, depending on how much RF gain is required. The additional capacitive loading on the LNA caused by the many chains is absorbed into its LC tank.

The cascaded architecture supports parallelism because the area required for a single gain stage not including the current source is only 576 μm^2. To further reduce area requirements, current sources are shared between the parallel chains. Figure 4-4 shows how a current source is shared between gain stages of different chains. For example, if the i^{th} chain is enabled, switch S_i is closed and all other switches are open. The total layout area for the LNA and cascaded untuned gain stages is only 250 μm by 250 μm.

The architecture supports a gain scalable from 7 to 890 and at the highest gain setting has an input-referred noise of approximately 18 μV. The power consumption including all bias currents is scalable from 400 μW when only the LNA is active to

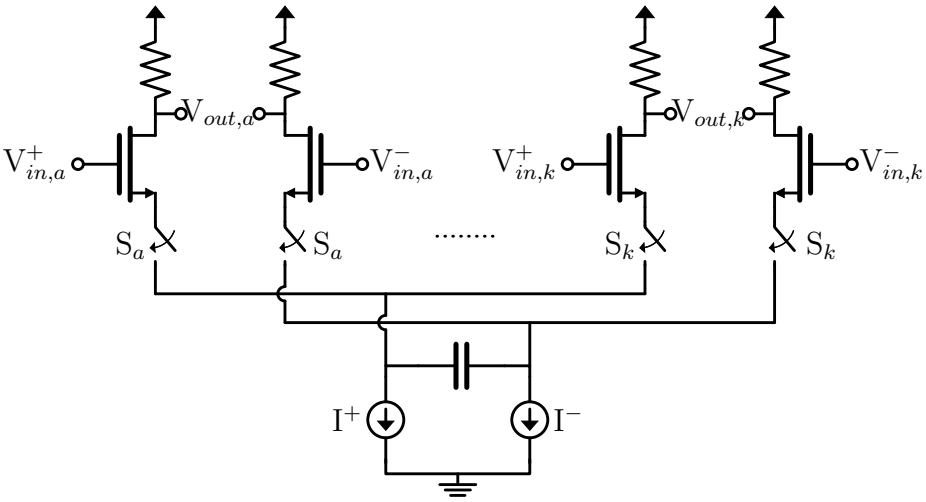


Figure 4-4: Slice of untuned gain

2.3 mW when the highest gain chain is active. All simulation data is from full, *RC* extracted circuits due to the strong effect of parasitic capacitance on the untuned gain stages. Table 4.1 presents the gain and input-referred noise for the five different gain settings. The table also includes the effective noise sensitivity and the effective gain sensitivity. The effective noise sensitivity estimates the minimum input signal that can be received given the noise requirements. It equals the input referred noise in dBm plus the 3 dB SAW filter insertion loss and the 8 dB minimum signal-to-noise ratio. The effective gain sensitivity estimates the minimum input signal that can be received given the gain and the 30 mV input amplitude required by the envelope detector. The actual sensitivity of the receiver is the maximum of both sensitivities. Hence, we see from Table 4.1 that the receiver has a maximum sensitivity of -71 dBm, including the 3 dB loss of the SAW filter.

To maximize the overall sensitivity of the receiver, the chains with high RF gain are supplied additional current to their single to differential converter. This allows the effective noise sensitivity to increase from -64 dBm to -71 dBm. The single to differential converter consumes 200 μA for the second gain setting, 400 μA for the third gain setting, and 800 μA for the fourth and fifth gain settings.

An interesting observation from Table 4.1 is that for input signals less than -64 dBm, the receiver is limited by gain rather than noise. Being gain limited means

Gain	Power Consumption	Input-referred noise	Effective noise sensitivity	Effective gain sensitivity
6.7	400 μW	10 μV	-76 dBm	-37 dBm
40	950 μW	40 μV	-64 dBm	-49 dBm
120	1400 μW	25 μV	-68 dBm	-62 dBm
340	2050 μW	19 μV	-70 dBm	-71 dBm
890	2300 μW	18 μV	-71 dBm	-79 dBm

Table 4.1: Sensitivity of RF gain for each gain setting

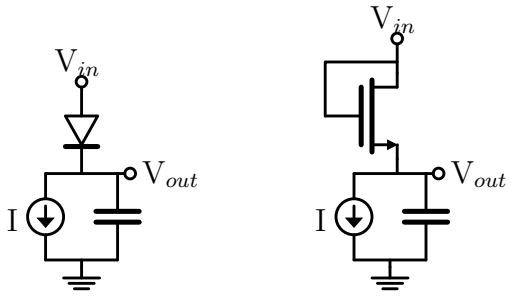
that receiver power must be increased to meet the gain specification rather than the input-referred noise specification. This observation adds weight to the statements in Chapter 2 that the poor noise performance of OOK modulation is acceptable given the architecture simplifications that it enables.

4.4 Envelope Detector

A key design decision for the OOK receiver is how to implement the envelope detector. Super-regenerative receivers use an oscillator that is periodically quenched for envelope detection. This approach is in contrast to continuous-time voltage or current-mode approaches. Although a super-regenerative receiver is energy efficient due to its inherent positive feedback, the quench rate must scale in proportion to the data rate. At high data rates, it becomes challenging for the positive feedback to generate sufficient gain to drive later stages in the receive-chain. Thus, continuous-time voltage-mode or current-mode envelope detectors become more practical.

Envelope detectors are typically implemented with a rectifier followed by a peak detector. The rectifier uses a non-linear response to extract a dc signal from the amplitude of an ac signal. In a standard silicon process, *pn* and MOS diodes are often used to implement a rectifier. Figure 4-5 shows two ideal envelope detectors implemented using a *pn* diode and a MOS transistor for rectification. Equations 4.2 and 4.3 represent the I-V equations for a *pn* and MOS diode, respectively:

$$I_{D1} = I_S(e^{(V_{in}-V_{out})/\phi_T} - 1) \tag{4.2}$$



(a) (b)

Figure 4-5: Envelope detectors with rectifier implemented using (a) a *pn* diode, and (b) a MOS transistor

$$I_{M1} = I_{const} e^{(V_{in}-V_{out})/n\phi_T}(1 - e^{-(V_{in}-V_{out})/\phi_T}) \quad (4.3)$$

$$\approx I_{const} e^{(V_{in}-V_{out})/n\phi_T} \quad (4.4)$$

In the above equations, $\phi_T = kT/q = 26mV$ at 300K. From these equations, one can derive the change in V_{out} in response to varying amplitudes of V_{in}. We will first limit our analysis to the MOS rectifier and assume that the current source I_2 is ideal. Hence, the average current through M_1 must equal I_2:

$$I_2 = \frac{1}{\tau}\int_t^{t+\tau} I_{M1}(t)dt \quad (4.5)$$

We will also assume that V_{out} does not vary with time as long as the amplitude of V_{in} is constant. This is true, as long as the time constant at the output is significantly greater than the period of V_{in}. Given that $V_{in} = V_{in,DC} + Acos(\omega t)$:

$$\begin{aligned} I_2 &= \frac{1}{\tau}\int_t^{t+\tau} I_{const} e^{(V_{in,DC}+Acos(\omega t)-V_{out})/n\phi_T} dt \\ &= \frac{1}{\tau} I_{const} e^{(V_{in,DC}-V_{out})/n\phi_T} \int e^{Acos(\omega t)/n\phi_T} dt \\ &= I_{const} e^{(V_{in,DC}-V_{out})/n\phi_T} B_0(A/n\phi_T) \end{aligned} \quad (4.6)$$

In Equation 4.6, $B_0(A/\phi_T)$ is a modified Bessel function of the first kind. This Bessel function can be considered a current factor, representing how much the current I_2

increases due to the magnitude of the ac signal. If the amplitude A is 0, then the current factor is 1. Since the current I_2 is fixed, when the current factor increases, the voltage V_{out} must decrease. By manipulating Equation 4.6, we can determine the voltage V_{out} in terms of A.

$$V_{out} = -n\phi_T ln\left(\frac{I_2}{I_{const}B_0(A/n\phi_T)}\right) + V_{in,DC} \tag{4.7}$$

Given a change in the amplitude of the ac signal, Equation 4.7 can be manipulated to calculate the change in V_{out}:

$$\begin{aligned} \Delta V_{out} &= V_{out}(A = A_0) - V_{out}(A = 0) \\ &= -n\phi_T ln\left(\frac{I_2}{I_{const}B_0(A_0/n\phi_T)}\right) + n\phi_T ln\left(\frac{I_2}{I_{const}}\right) \\ &= n\phi_T ln(B_0(A_0/n\phi_T)) \end{aligned} \tag{4.8}$$

From Equation 4.8 we see that the change in output voltage of the envelope detector depends only on A, n, and ϕ_T. Using the same method, a similar relationship between A and V_{out} for the pn diode can be determined:

$$\Delta V_{out} = \phi_T ln(B_0(A_0/\phi_T)) \tag{4.9}$$

Figure 4-6 presents a plot showing the relationship between ΔV_{out} and ac amplitude for both the MOS and pn rectifiers. From this plot, we see that small ac amplitudes only cause a small change in the envelope detector output voltage. When the ac amplitude is approximately ϕ_T, the output voltage starts increasing linearly with input amplitude. For the envelope detector output to have a voltage swing of 5 mV, the input amplitude must be 23 mV for a pn diode and 26 mV for a MOS diode..

From Figure 4-6, it seems clear to use pn diodes instead of MOS diodes because they require a smaller input amplitude and hence less RF gain. However, a pn diode has a large voltage drop across it. Given an input dc voltage of 0.8 V, the output voltage is nominally only a few hundred of millivolts from the negative supply voltage.

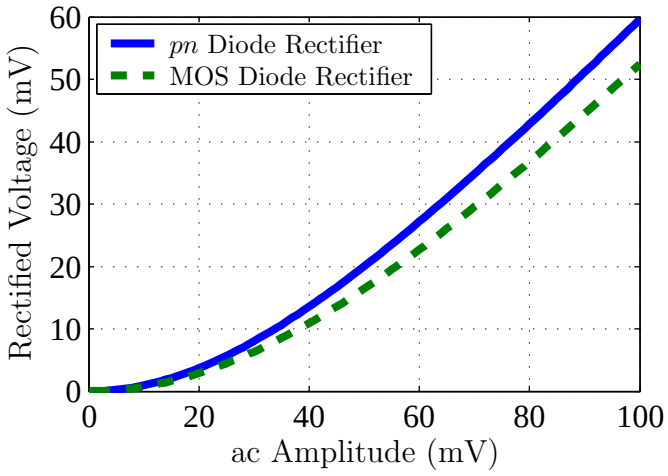


Figure 4-6: Envelope detector output voltage versus input ac amplitude

To avoid such tight margins, MOS diodes are used to implement the rectifier.

The envelope detector schematic is shown in Figure 4-7. The envelope detector is equivalent to a source-follower with a slow time constant at the output. To interface with the multiple outputs from the scalable RF gain, input transistors are switched into and out of the envelope detector. For example, at the minimum gain setting when only the LNA is active, switch S_1 is closed and all other switches are open. At the second smallest gain setting, switches $S_{2,a}$ and $S_{2,b}$ are closed and all other switches are open. Differential inputs are used when available to reduce ripple at the output of the envelope detector. For small input signals, the input transistors behave like diodes with the advantage that no current is sinked from the preceding gain stage. The envelope detector is supplied 0.8 V and requires only a few microamps of current. A pseudo-differential output is generated by a using second envelope detector that has its inputs tied to the positive power supply. Figure 4-8 presents simulated operation of the envelope detector for a manchester encoded RF input.

An interesting feature of the envelope detector is that it can be used as a source-follower for testing purposes. In this test mode, the current increases to 200 μA and only one input of a differential pair is activated. For example, to buffer V_2^+ offchip, switch $S_{2,a}$ closes and all the other switches remain open. Combining the source-follower with the envelope detector has two key advantages: there is less capacitive

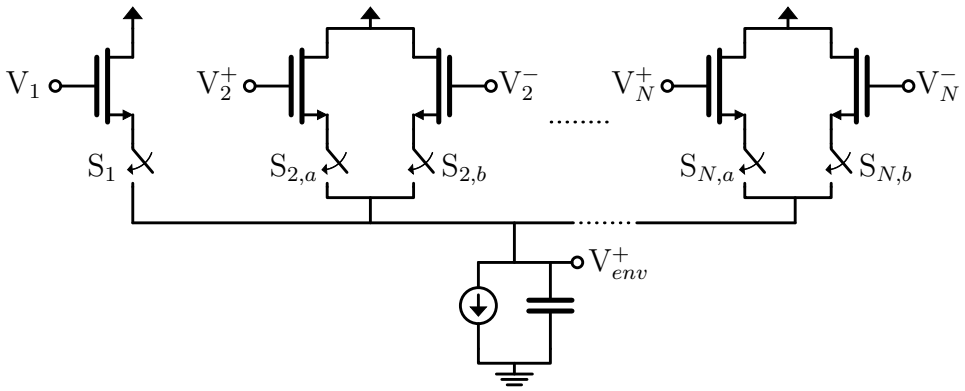


Figure 4-7: Envelope detector schematic

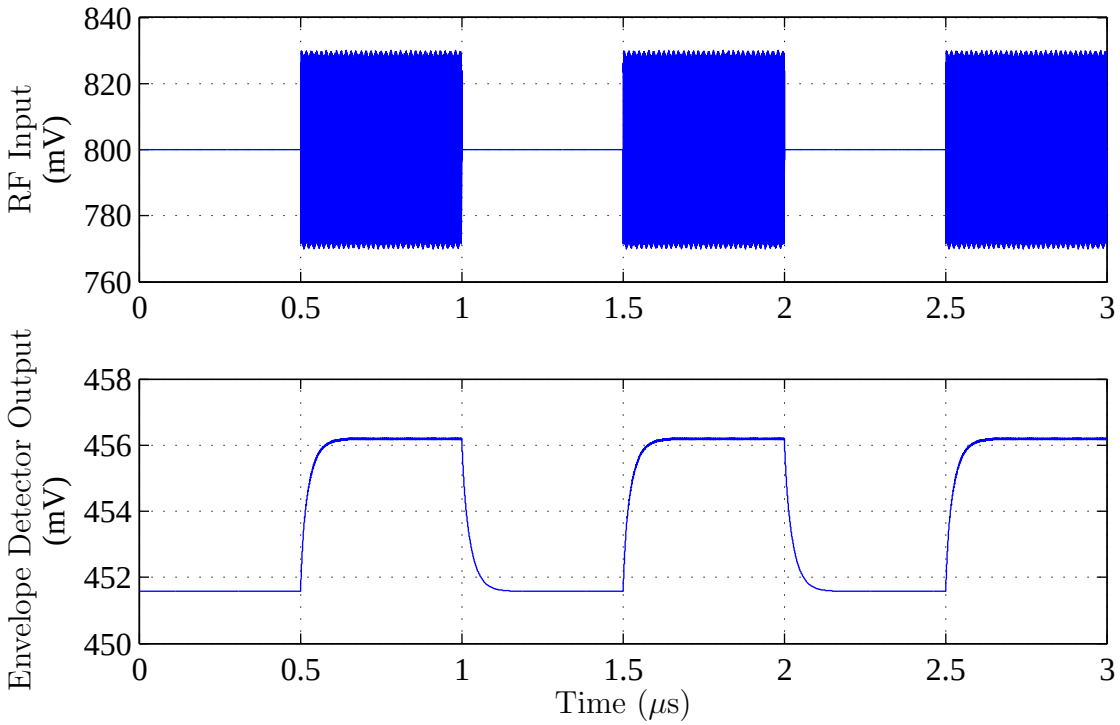


Figure 4-8: Simulated operation of the envelope detector

loading on the sensitive RF gain circuits and there is no need for additional pads on the chip.

4.5 Baseband Amplifier and ADC

The purpose of the baseband amplifier and ADC is to convert the envelope detector output to a digital signal. Due to mismatch and noise induced offsets in ADC latches, it is ideal that a signal be nearly 100 mV above or below a reference voltage to ensure that a latch error does not occur. In a flash ADC with no preamplification, this means that the smallest voltage division should not be less than fifty to one hundred millivolts. Given the requirement of a 3-bit digital output and the rectifier's output swing of 5 mV, it is apparent that the envelope detector output must be amplified before the signal is passed into an ADC.

One limitation of the envelope detector shown in Figure 4-7 is that the common-mode output voltage can vary with time. The dc and low frequency variation in the envelope detector's output occurs due to temperature variations, process variations, and noise. Because the OOK signal has no dc and low frequency content, it is possible to employ offset compensation. As discussed in Section 3.5.1, continuous-time offset compensation is preferred to discrete-time offset compensation due to the long packet length and short bit period. A traditional continuous-time offset compensation technique for baseband amplifiers is to use chopper-stabilization, however, chopper-stabilization results in a significant power overhead [36] We propose implementing continuous-time offset compensation using passive components.

A common problem limiting the use of passive, low frequency offset compensation is that the capacitors and resistors required are extremely large [37]. For a 1 Mbps, pulse-amplitude modulated signal, a lower cutoff frequency of approximately 1 kHz is appropriate [37]. To implement a RC highpass filter with a cutoff frequency of 1 kHz and a series capacitance of 1 pF, the shunt resistor must be 1 GΩ. By employing Manchester encoding, the cutoff frequency of 1 kHz increases significantly, however, even with a cutoff frequency of 100 kHz, the shunt resistance only decreases

to 10 MΩ. Such a resistance would make a low-power implementation impractical, as it would result in substantial parasitic capacitance. High impedance resistors can be implemented using transistors, however, their impedance is typically non-linear over a large voltage range. To overcome this linearity problem, a high impedance resistor is implemented using forward biased MOS diodes. For a small, positive voltage drop across a MOS diode ($0 < V_{ds} < n\phi_T$), the I-V relationship can be approximated as:

$$I = I_{const} e^{V_{ds}/n\phi_T} \left(1 - e^{-V_{ds}/n\phi_T}\right) \tag{4.10}$$

$$I \approx I_{const} \left(1 + V_{ds}/n\phi_T\right) \left(+V_{ds}/n\phi_T\right) \tag{4.11}$$

$$I \approx V_{ds} \frac{I_{const}}{n\phi_T} \tag{4.12}$$

Thus, the effective resistance of a forward biased MOS diode is $n\phi_T/I_{const}$. For negative values of V_{ds}, the current I is negligible and the resistance increases quickly. A PMOS diode can be placed in parallel with an NMOS diode to implement a resistor that is relatively constant over both positive and negative voltages. In the given 0.18-μm CMOS process, the resistance R of a NMOS diode is simulated to be approximately 30 GΩ. Figure 4-9 shows the resistance of a NMOS diode, a PMOS diode and the two diodes in parallel versus the voltage across them. To ensure that the transistor's drain and source voltages remain between the power supplies, the diodes are biased around 0.6 V while the positive and negative supplies are 1.2 V and 0 V, respectively. When the NMOS and PMOS diodes are placed in parallel, they exhibit a resistance varying from 8 GΩ to 17 GΩ over a 200 mV range.

Even though a NMOS and PMOS diode can realize a relatively linear resistor over a 200 mV range, the baseband amplifier requires a linear resistor over a 800 mV range. To achieve a larger linear range, multiple diodes can be stacked in series. Figure 4-10 shows the circuit that is implemented to realize a high impedance resistance with a linear range of 800 mV. Four NMOS and PMOS diodes are stacked in series. The internal nodes of the NMOS and PMOS stacks are connected together to improve transient behavior.

Problems associated with the high impedance diode resistor are its acute sensi-

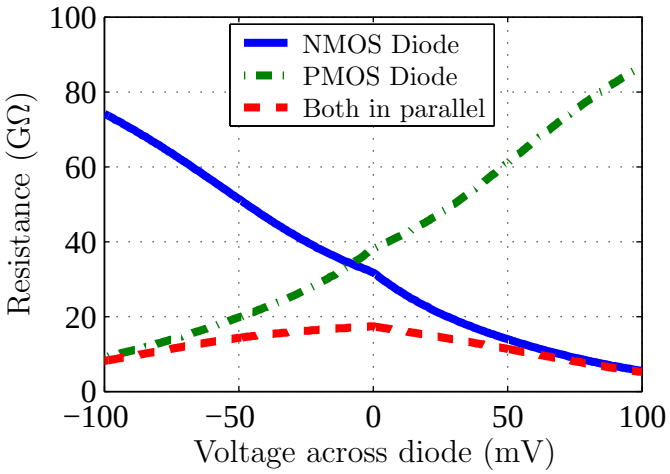


Figure 4-9: Effective resistance of NMOS and PMOS diodes

tivity to process and temperature variation, its slow time constant and that the high resistance node is susceptible to capacitive coupling. To minimize the effect of the slow time constant, a zeroing switch is placed in parallel to the effective resistor to eliminate initial offsets. This switch is a near-minimum sized transistor to minimize its leakage. If the switch's leakage is too large, a non-linearity is introduced into the resistance. The circuit is laid out to minimize the effect of capacitive coupling.

The three stage, continuous-time differential amplifier consumes 30 μW and has a cumulative gain of 75. Each stage consists of a resistively loaded differential pair with input-mode offset compensation using a diode high impedance resistor and a coupling capacitor. The lower and upper 3-dB frequencies are 55 Hz and 4.4 MHz, respectively. Resistive source degeneration is used to limit the gain per stage and to improve linearity. The input-referred noise of the amplifier is approximately 110 μV. The amplifier's later gain stages can be bypassed in the presence of a large envelope detector output.

The amplifier is followed by a 3-bit, 10 MSPS flash ADC. A 3-bit ADC is chosen because it provides sufficient resolution to allow for recovery of the data and for feedback control of the RF gain. The seven reference voltages are generated by a on-chip resistor string. Each comparator consists of a preamplifier followed by a sense-amplifying flip-flop [38]. The schematic of the sense-amplifying flip-flop is shown in

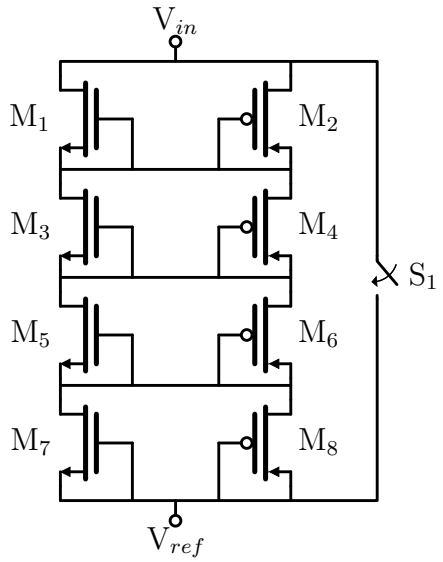


Figure 4-10: Diode connected transistors realizing a high impedance resistor

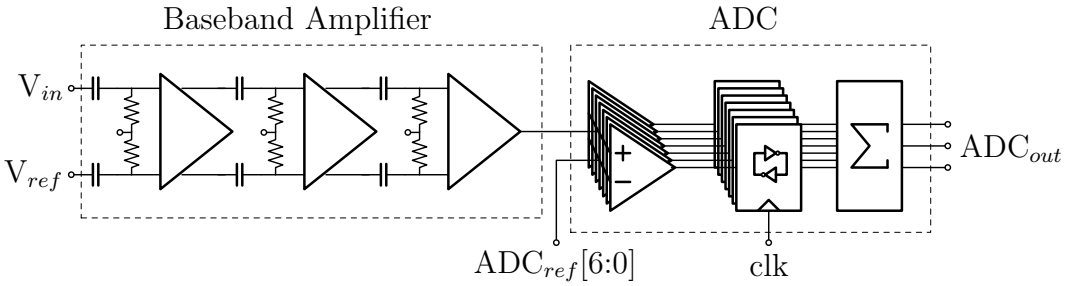


Figure 4-11: Baseband topology

Figure 4-12. The total power required by the ADC is approximately 60 μW, of which 20 μW is drawn by the resistor string and 14 μW is drawn by the sense-amplifying flip-flop. Figure 4-11 presents a block diagram of the complete baseband topology.

4.6 Receiver Simulation Results

Figure 4-13 presents simulated operation of the complete receiver. The RF input signal is a -66 dBm, manchester encoded OOK signal. Due to the 3 dB loss of the SAW filter, this corresponds to a -63 dBm signal at the antenna. The RF gain is set to its third setting, and hence the LNA is followed by three untuned gain stages. The outputs of the LNA and the untuned RF gain are shown on the second and

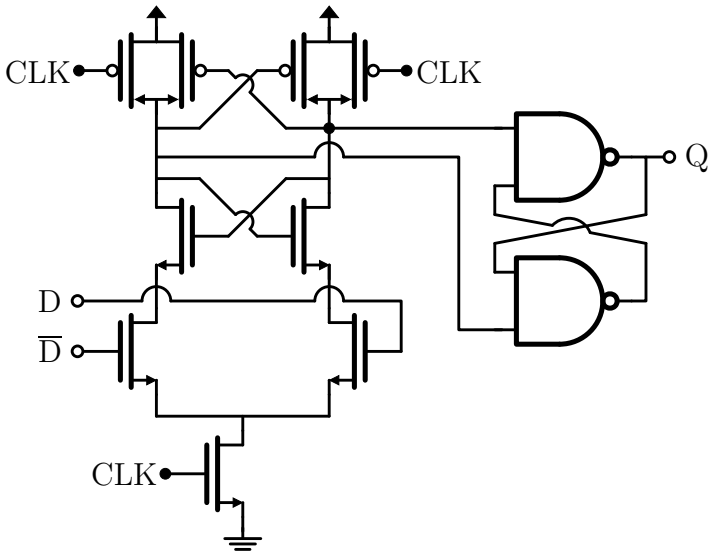


Figure 4-12: Sense-amplifying flip-flop

third rows, respectively. The envelope detector output varies by 5 mV depending on whether a '1' or a '0' is being received. This output is then amplified by the three stage baseband amplifier. The ADC output code is shown on the final row. This code is generated by converting the three-bit output to a single, integer code between 0 and 7 using following equation:

$$\text{Code} = \frac{ADC_{out,1} + 2ADC_{out,2} + 4ADC_{out,3}}{VDD_{digital}} \tag{4.13}$$

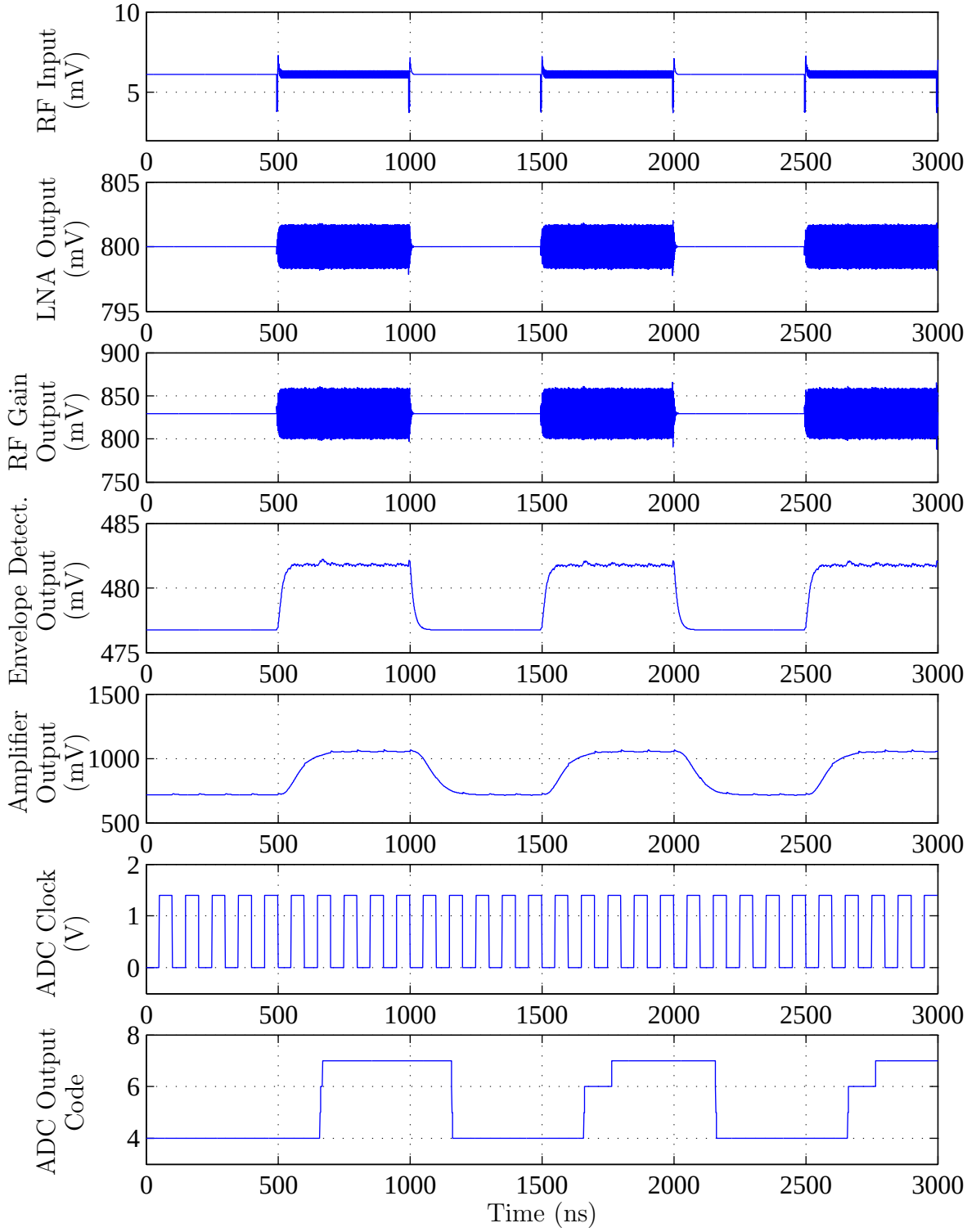


Figure 4-13: Simulated operation of receiver

Chapter 5

Transmitter Implementation

5.1 Overview

A block diagram of the OOK transmitter is presented in Figure 5-1. The oscillator is stabilized to a 915 MHz carrier frequency by a SAW resonator. The oscillator is then buffered and amplified by a three stage power amplifier (PA). The last two stages of the PA also serve as a mixer, turning off and on to transmit a '0' and a '1', respectively. The output of the PA passes through an off-chip balun to convert the differential output to a single-ended signal that drives the antenna. The last stage of the PA is scalable to support output power levels from -10 dBm to -1 dBm.

5.2 Oscillator

To avoid the need for a phase-locked loop, the oscillator is stabilized with a SAW resonator. Although this approach allows for power savings, it limits the oscillator to a single frequency of operation. A SAW resonator is a non-linear device, but to a first-order it can be modeled as a series RLC circuit with an unloaded quality factor of approximately twenty thousand. At its resonant frequency over a narrow bandwidth of a few hundred kilohertz, the SAW resonator has a low impedance of tens of ohms. Away from the resonant frequency, this impedance increases dramatically such that the resonator appears to be an open circuit. However, for a 915 MHz resonator, due

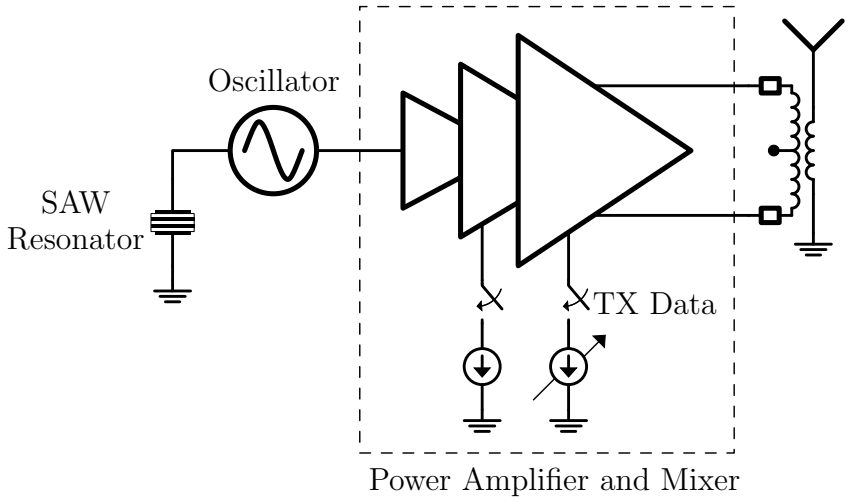


Figure 5-1: Transmitter architecture

to capacitive and inductive parasitics, the impedance of the resonator away from the resonant frequency typically reduces to only a few hundred ohms. These parasitics become increasingly significant at high frequencies such that there are very few one-port SAW resonators available above 1 GHz. Another factor limiting the availability of high frequency SAW resonators is that they become increasing difficult to fabricate due to small width tolerances.

Since SAW resonators can be modeled similarly to crystal resonators, the traditional Colpitts and Pierce oscillator topologies can be used. A Colpitts topology is chosen as this allows for one end of the SAW resonator to be grounded, thereby reducing the effect of package parasitics. A Colpitts topology is also the suggested topology in most of the SAW datasheets. Figure 5-2 shows the circuit diagram of the SAW stabilized oscillator. Capacitors C_1 and C_2 and inductor L_1 form an LC tank that has a center frequency of f_{res}:

$$f_{res} = \frac{1}{\sqrt{L_1 \frac{C_1 C2}{C_1 + C_2}}} \tag{5.1}$$

f_{res} must be set close to the SAW's resonance frequency to ensure that the oscillator will stabilize. Thus, f_{res} is tunable through the use of an on-chip accumulation mode capacitor, C_2. The RO-2144 SAW resonator from RF Monolithics is used to stabilize

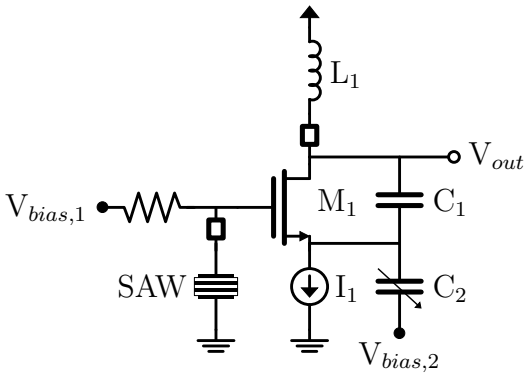


Figure 5-2: SAW stabilized oscillator

Characteristic		**Value**
Nominal Frequency		916.4 MHz
Tolerance		± 95 kHz
Insertion Loss		2.5 dB
Unloaded Q		23509
50 Ω Loaded Q		4000
Equivalent RLC Model	R_M	20.5036 Ω
	L_M	83.704 μH
	C_M	0.3603 fF
	C_P	2.2 pF

Table 5.1: Key specifications of RO-2144A SAW resonator [1]

the oscillator. Table 5.1 presents key specifications for the RO-2144 SAW resonator [1].

Capacitors C_1 and C_2 form a voltage divider with ratio n from V_{out} to the source of M_1:

$$n = \frac{C_1}{C_1 + C_2} \tag{5.2}$$

If one assumes that the capacitive divider is an ideal impedance transformer, one can calculate the requirement for oscillator start-up to be:

$$g_{M1} > \frac{1}{R_{L1}(n - n^2)} \tag{5.3}$$

where R_{L1} represents the parasitic resistance of inductor L_1. For optimal noise performance, n should be approximately 0.2 [8]. However, for minimum power consumption,

the function $n - n^2$ should be maximized over the range $n \in [0, 1]$ resulting in n of 0.5. By setting n to 0.5 instead of 0.2, the minimum required transconductance decreases 35%. Since noise is not a key design constraint, capacitors C_1 and C_2 are sized equally to set n to 0.5. Assuming a parasitic resistance R_{L1} of 800 Ω, the transconductance g_{M1} must be greater than 5 mS. Since it is recommended to choose a transconductance larger than this minimum value, the oscillator is designed to have a small signal transconductance of 18 mS.

The oscillator nominally receives 800 μA at 0.8-V. Because the SAW resonator cannot be accurately modeled in simulation, it is difficult to calculate the turn-on time of the oscillator. Based on application notes, the turn-on time of the oscillator is estimated to be tens of microseconds.

5.3 Power Amplifier

In an on-off keying system, the data modulation can be integrated in the PA with a switch that enables and disables the output stage. This section will refer to the integrated PA and mixer as the PA. The PA has several key constraints that directly impact which architecture to use:

1. The PA must be highly integrated to minimize the number of external inductors and capacitors

2. The PA requires a maximum average output power of 0 dBm, corresponding to a peak output power of 3 dBm. At 50 Ω, this corresponds to a peak-to-peak voltage of 895 mV. Such a voltage swing is within the 0.18-μm CMOS limits and hence the power amplifier does not require a downward impedance transformation from the antenna to the PA output.

3. The on-off keying waveform must be able to quickly turn on and off to support a switching rate of 2 MHz.

Based on these considerations, a three stage power amplifier has been designed and is shown in Figure 5-3. To minimize the number of external components, the first

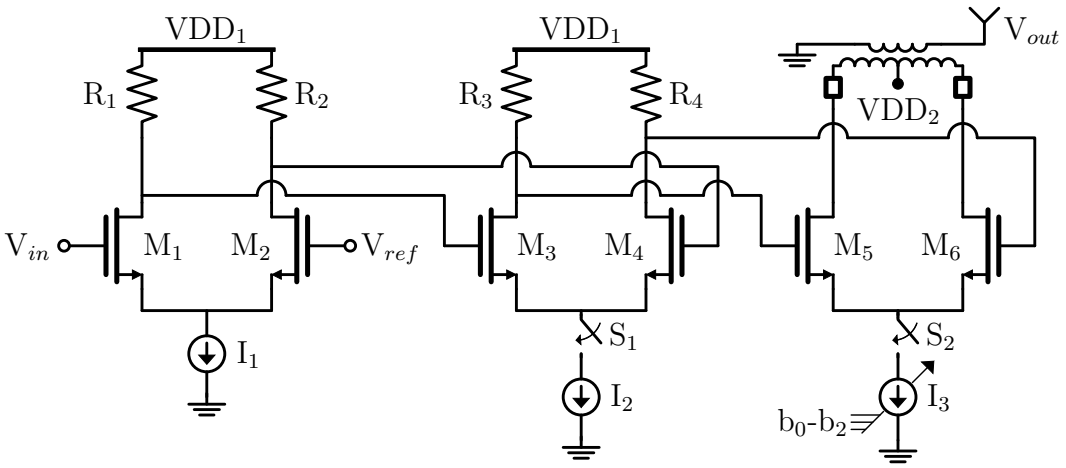


Figure 5-3: Mixer and Power Amplifier

two stages of the PA are resistively loaded differential pairs. As was discussed in Chapter 3, these untuned gain stages have comparable energy efficiency to tuned gain stages without requiring costly inductors or capacitors. Although untuned gain stages typically generate more noise than equivalent tuned gain stages, this is not a problem as signal swings are hundreds of millivolts, well above the total noise level. However, with such large signals the untuned gain stages are non-linear and introduce distortion into the signal. This distortion is not a problem because OOK does not require linear amplification. The distortion is filtered by the final, tuned output stage.

In addition to buffering the oscillator output, the untuned differential pairs act as a single-ended to differential converter. This conversion allows the final stage of the power amplifier to be fully-differential. By using a differential output stage the source nodes of transistors M_5 and M_6 can be considered a virtual ground, which offers two key benefits:

1. Switch S_2 can quickly enable/disable the gain stage without generating much kickback to previous stages

2. For ac inputs, transistors M_5 and M_6 have negligible source degeneration, thereby improving their performance and stability

Due to the slow turn-on time of the oscillator, the oscillator must remain active over an entire packet length. The PA, however, can be disabled when transmitting a '0'. To implement this power gating, switches S_1 and S_2 are open when transmitting a '0' and closed when transmitting a '1'. The first stage of the PA is not power gated because such gating would inject excessive noise into the oscillator and potentially cause the oscillator to lose lock.

The final stage of the PA is designed to drive a differential 200 Ω load. To achieve maximum output power, this load impedance is maximized while still meeting voltage headroom constraints at the drains of transistors M_5 and M_6. The differential PA output is connected to a balun that transforms the differential 200 Ω load to a 50 Ω, single-ended output. This corresponds to an upward impedance transformation from the antenna to the PA output. The balun attenuates out-of-band distortion but has an insertion loss of 1 dB. The power amplifier is supplied 1-V and the bias current I_3 is digitally controlled by b_{0-2} to support power scalability from -10 dBm to -1 dBm (including the 1 dB insertion loss of the balun). Table 5.2 presents the performance of the transmitter for each of the PA power settings. The transmitter achieves an optimal power efficiency of approximately 11% at an output power of -2 dBm. At smaller output power levels, the power consumed by the oscillator and biasing circuits results in excessive overhead. At higher power levels, efficiency is limited by large signal transistor non-linearities as well as parasitic resistances and capacitances. All data is based on full RC extracted simulations, as the output power is significantly affected by parasitic resistances and capacitances.

5.4 Transmitter Simulation Results

Figure 5-4 presents simulated operation of the complete transmitter switching from a '0' to a '1'. Figure 5-4 includes the single-ended oscillator output as well as the differential outputs of each stage of the three stage PA. At $t = 20ns$, the transmitter raises *TX Data* to start transmitting a '1'. This event causes the second and third stage of the PA to turn on. The transmitter is set to power level 4 of 7 (See Table 5.2).

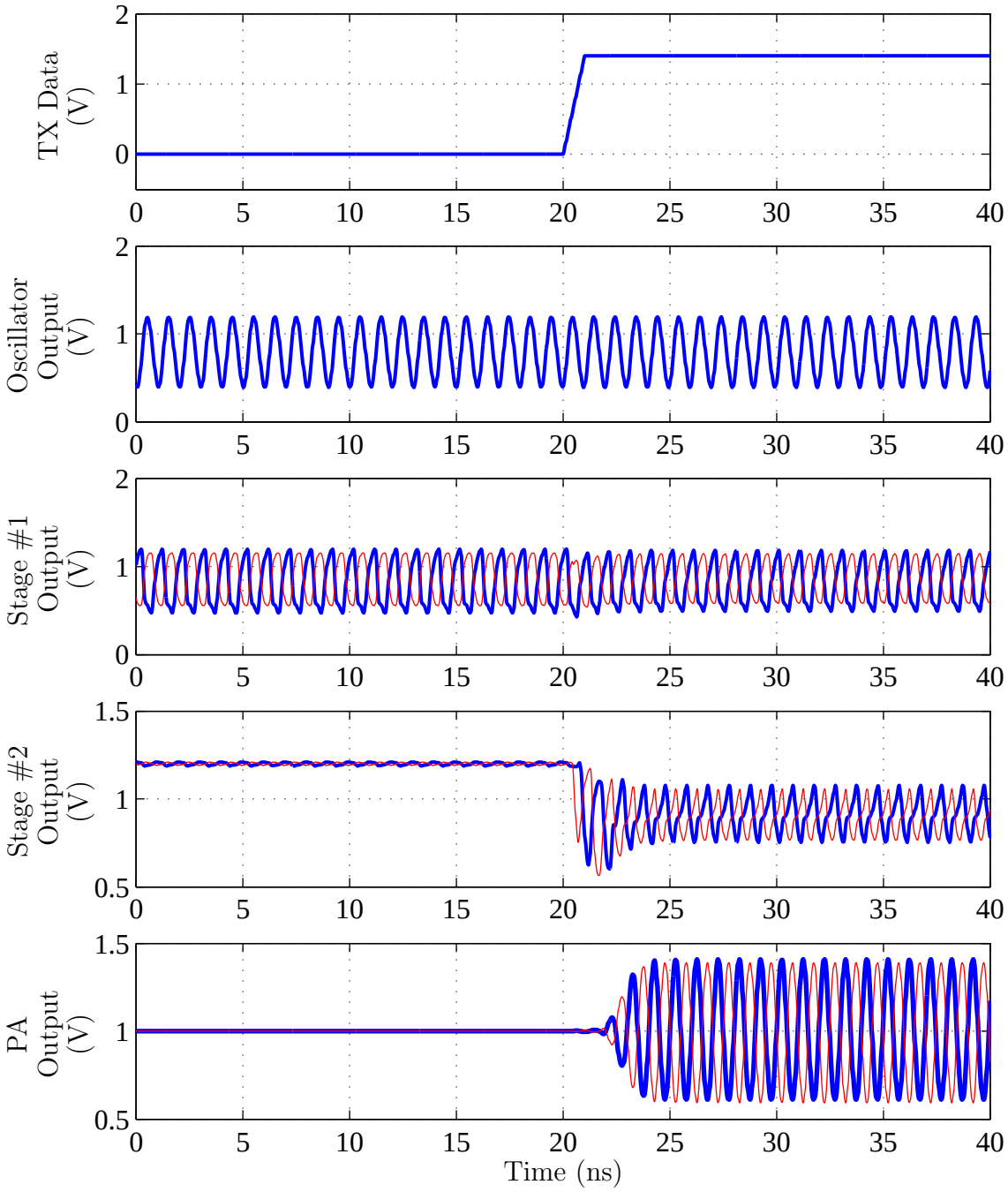


Figure 5-4: Simulated operation of transmitter

Power Setting	**Total Power**	**Output Power (dBm)**	**Efficiency**
1	3.1 mW	-10 dBm	4.2%
2	4.5 mW	-5.3 dBm	8.2%
3	5.8 mW	-3.2 dBm	10.4%
4	7.1 mW	-2.0 dBm	11.0%
5	8.4 mW	-1.5 dBm	10.8%
6	9.5 mW	-1.1 dBm	10.2%
7	10.7 mW	-0.8 dBm	7.7%

Table 5.2: Transmitter power settings

Chapter 6

Conclusions

6.1 Summary of Contributions

A custom wireless transceiver for sensor networks has been designed in a 0.18-μm CMOS process provided by National Semiconductor. Figure 6-1 shows the transceiver's layout. Table 6.1 presents a summary of key transceiver specifications based on full RC extracted simulations. At a data rate of 1 Mbps and a bit error rate of 10^{-3}, the receiver achieves a sensitivity scalable from -37 dBm to -71 dBm. The power consumption of the receiver scales from 500 μW at the lowest gain and sensitivity setting to 2.4 mW at the highest gain and sensitivity setting. The transmitter consumes between 3.1 mW and 10.7 mW, depending on the transmit power level. The transmitter achieves a maximum power efficiency of 11% at a transmit power level of -2 dBm. Both the receiver and transmitter have lower energy per bit ratios than any radio included in Figures 1-2 and 1-3. This improvement in energy efficiency is achieved through architectural and circuit optimizations. Both bandwidth efficiency and receiver sensitivity is sacrificed to achieve power savings.

The RF front-end and the power amplifier extensively leverage untuned gain stages to maximize energy efficiency and minimize the number of external components. Although such an approach becomes less practical at frequencies above a gigahertz, this upper bound will increase with device scaling.

Throughout all RF and baseband circuits, a key emphasis of the transceiver is

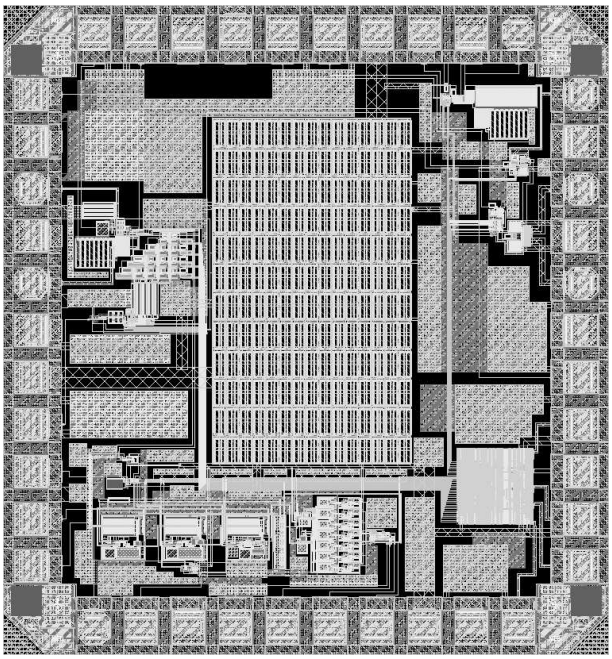


Figure 6-1: Transceiver layout

to use continuous-time rather than discrete-time systems. This technique lends itself well to device scaling, because continuous-time systems are less sensitive to leakage. A second emphasis of the transceiver is to use moderate gain amplifiers (like a differential pair) rather than high-gain operational amplifiers. This technique also should improve with device scaling, as r_{ds} decreases with transistor length.

Technology	0.18-μm CMOS
Die Area	1.2 mm by 1.3 mm
Data Rate	1 Mbps
Receiver sensitivity	-37 dBm to -71 dBm
Receiver power consumption	500 μW to 2.4 mW
Receiver energy per bit	0.5 nJ/bit to 2.4 nJ/bit
Transmitter power consumption	3.1 mW to 10.7 mW
Transmitter energy per bit	3.1 nJ/bit to 10.7 nJ/bit
Transmitter output power	-10 dBm to -1 dBm
Maximum transmitter power efficiency	11%

Table 6.1: Transceiver overall performance

6.2 Future Work

Although the transceiver described in this thesis is extremely energy efficient from an energy per bit metric, the transceiver has not been designed to minimize power consumption. Hence, the radio consumes up to 2.4 mW and 10.7 mW of power in receive-mode and transmit-mode, respectively. Even though these power values are low compared to traditional wireless transceivers, they are still too high for some self-powered applications. Small, energy-harvesting based sensors often do not have the energy capacity to sink milliamps of current for milliseconds at a time [39]. One area for further research is to design a radio that only consumes tens of microwatts of power when active.

A key limiting block to microwatt power operation is the oscillator. One of the lowest power UHF oscillators reported has been a 1.9 GHz oscillator tuned with a high quality factor Bulk Acoustic Wave (BAW) resonator [10]. The oscillator nominally consumes 89 μW. Because this power is consumed regardless of the transmit power level, the transmitter can only efficiently transmit power levels down to approximately one hundred microwatts (-10 dBm). Future research must further reduce oscillator power consumption so that transmit power levels can efficiently scale to tens of microwatts.

To achieve power savings, voltage scaling has been used in this thesis. However, voltage scaling can be much more extensively leveraged, potentially lowering supplies to hundreds of millivolts. Such low-voltage circuits typically have poor dynamic range, common-mode rejection and power-supply rejection as well as high sensitivity to process variations. A low-voltage transceiver would require solutions to these problems, likely at the both the architectural and the circuit levels.

Appendix A

Digital Shift Register

The transceiver is digitally controlled by a 33 bit register. The register is programmed through a five pin serial interface. The serial interface is programmed in Verilog and synthesized using Cadence Design Compiler. Synposys Astro is used for place and route and to verify timing requirements.

The serial interface has five pins: *data_in*, *data_out*, *shift*, *reset*, and *clk*. The interface consists of a shift register and a 33 bit register. When *shift* rises to 1, the existing data inside the 33 bit register is copied into the shift register. Then, on each positive clock edge, data gets shifted into the shift register from *data_in* and data is shifted out from the shift register to *data_out*. When *shift* returns to 0, the data inside the shift register is copied into the 33 bit register. When *reset* is high, the data in the 33 bit register is set to a default state.

Figure A-1 presents a timing diagram for the digital interface. The digital interface is reset at the start of the timing diagram. Hence, the output bits of *data_out* correspond to the default state.

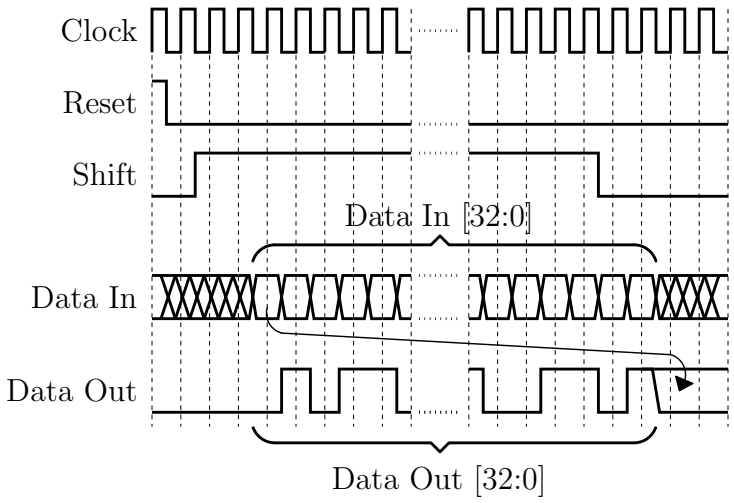


Figure A-1: Timing diagram of digital interface

Appendix B

Acronyms

ADC Analog to Digital Converter

BAW Bulk Acoustic Wave

BPSK Binary Phase-Shift Keying

CMOS Complimentary Metal Oxide Semiconductor

DQPSK Differential Quadrature Phase-Shift Keying

DSP Digital Signal Processor

FM Frequency Modulation

FSK Frequency-Shift Keying

GMSK Gaussian Minimum-Shift Keying

IF intermediate frequency

ISM Industrial, Scientific and Medical

LNA Low Noise Amplifier

MAC Medium Access Control

MEMS microelectromechanical systems

MOS Metal Oxide Semiconductor

OOK On-Off Keying

O-QPSK Offset Quadrature Phase-Shift Keying

QAM Quadrature Amplitude Modulation

PA power amplifier

PHY physical

RMS Root Mean Square

RF radio-frequency

RFID Radio Frequency Identification

SAW Surface Acoustic Wave

SNR signal-to-noise ratio

UHF Ultra High Frequency

WLAN Wireless Local Area Network

WPAN Wireless Personal Area Network

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