A DIGITAL TECHNIQUE FOR PRECISE MEASUREMENT OF CAPACITOR DIFFERENCES, WITH APPLICATION TO CAPACITIVE INTEGRATED SENSORS

by

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(1985)

Submitted to the

Department of Electrical Engineering and Computer Science

In Partial Fulfillment of the Requirements

For the Degree of

Master of Science

at the

Massachusetts Institute of Technology

June 1987

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Department of Electrical Engineering and Computer Science
May 8, 1987

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Abstract

A technique for measurement of capacitor differences has been developed that has its origins in charge redistribution analog-to-digital converters. Effects of parasitic capacitance and MOS switch charge injection are canceled. The capacitance difference can be obtained as a voltage in both digital and analog form with no additional circuitry needed. This makes it ideally suited for digital signal processing. Since the technique can be made relatively insensitive to parasitic capacitance, differences in small capacitances such as capacitive integrated sensors can be measured.

It is shown that measurements on 20 to 100 femtofarad capacitors are possible using this method. Effects of junction leakage, capacitor and transistor hysteresis, comparator offset, MOS switch charge injection, and voltage and temperature coefficients are taken into account. Noise from the comparator, MOS switch, power supplies and clock feedthrough are considered as sources of error and dictate the minimum resolution.

Extensive measurements are made from test chips fabricated in 3 μm CMOS technology. Detection of percent differences of less than 0.5% on 20 to 100 femtofarad capacitors has been successfully demonstrated.

Thesis Supervisors: Hae-Seung Lee and Roger T. Howe
Titles: Assistant Professors of Electrical Engineering and Computer Science

Acknowledgments

During the course of this thesis, numerous colleagues and friends have helped me achieve the results of this work. In the MIT Microsystems Technology Laboratories, I would like to thank Jarvis Jacobs for helping me to understand the intricacies of our computer system, CAF (Computer Aided Fabrication), as well as the many stimulating conversations we have had; Vince McNeil for many interesting conversations on sensors; Jon Wade for insightful discussions on VLSI; Duane Boning for his software package GIRAPHE that helped create some of the graphs in this thesis; Ted Tewksbury for useful discussions on the self-calibration technique, his results on transistor hysteresis, and for the design of the CMOS op-amp; and finally, to my advisors, Hae-Seung Lee and Roger T. Howe. Without their knowledge, careful guidance, patience and support, this thesis would not be possible.

At MIT, I would like to thank Alice Twohig for making the administrative concerns at MIT an easier task to manage. She has made the EECS graduate office a very pleasant stop.

During the course of my life, I have been fortunate to have such a caring and loving family supporting me. This thesis is dedicated to them.

Support for this research was provided in part by the National Science Foundation under Contract No. ECS85-05145, by the Analog Consortium at MIT (Analog Devices, AT&T Bell Labs, General Electric, Digital Equipment Corporation, Texas Instruments), and in part by IBM through an IBM Faculty Development Award held by Roger T. Howe. MOSIS chip fabrication and other support has been provided by DARPA under grant N00014-80-C-0622.

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Symbols

a	diaphragm radius
A	comparator gain
b_i	digital output bit of A/D converter
C	general symbol for capacitance in context
C_0	zero-pressure capacitance
C_{gs0}	gate-to-source overlap capacitance per unit length
C_k	binary-weighted capacitor
C'_{ox}	gate oxide capacitance per unit area
C'_{ox-mp}	metal-to-poly capacitance per unit area
C_{total}	total capacitance on a node in context
C_{unit}	unit capacitor
C_C	coupling capacitor
C_P	parasitic capacitance
C_R	reference capacitor
C_S	sense capacitor
d	diaphragm plate separation
δ	capacitance divider ratio
ϵ_0	free-space dielectric constant
ϵ_k	error in capacitance matching in A/D converters
E	Young's modulus of elasticity
f	frequency (Hz)
h	diaphragm thickness
k	Boltzmann's constant
K_P	SPICE intrinsic transconductance parameter
L	drawn channel length
L_D	lateral diffusion of drain/source below gate
L_{eff}	effective channel length $L - 2L_D$
μ_0	surface mobility
N, M	number of bits in an A/D converter
ν	Poisson's ratio
ξ_{N-i}	summation of all binary terms up to $N - i$ in Gray's A/D converter
$\pi_{\parallel}$	parallel stress component
$\pi_{\perp}$	perpendicular stress component
P	applied pressure to diaphragm
Q	charge on a node in context
$Q_{channel}$	total channel charge

Q_{S3}	charge injected onto isolated node by switch S3
Q_R	residual polarization charge
R	general symbol for resistance in context
R_{on}	on-resistance of the MOSFET
S	zero-pressure plate separation
$\sigma_{\parallel}$	parallel piezoresistive coefficient
$\sigma_{\perp}$	perpendicular piezoresistive coefficient
T	temperature
T_{CC}	temperature coefficient of capacitance
$V_{\epsilon k}$	error voltage caused by ϵ_k in self-calibrating A/D converter
V_{error}	total linearity error in self-calibrating A/D converter
V_{gs}	gate-to-source voltage
V_{in}	input voltage
V_{os}	offset voltage of the op-amp/comparator
V_{out}	output voltage of the op-amp/comparator
V_{ref}	reference voltage
V_x	voltage at the isolated node
V_{CC}	voltage coefficient of capacitance
V_{DAC}	DAC output voltage
$V_{DAC_{cal}}$	DAC calibration voltage
$V_{DAC_{meas}}$	DAC measurement voltage
V_P	parasitic capacitance voltage
V_{R1}	voltage connected to C_R in step 1
V_{R2}	voltage connected to C_R in step 2
V_{S1}	voltage connected to C_S in step 1
V_{S2}	voltage connected to C_S in step 2
V_T	threshold voltage
$\pm\Delta V$	effective resolution of DAC
$w(x,y)$	deflection response of diaphragm to an applied pressure
W	channel width

Acronyms

A/D	Analog-to-Digital
ASIC	Application Specific Integrated Circuits
CMOS	Complementary Metal-Oxide-Semiconductor
CBPM2	MOSIS CMOS Bulk P-well Metal 2 process
D/A	Digital-to-Analog

DAC	Digital-to-Analog Converter
DIP	Dual In-Line Package
EPROM	Erasable Programmable Read Only Memory
GND	reference ground
LSB	Least Significant Bit (may be a number)
MOS	Metal-Oxide-Semiconductor
MOSIS	(MOS Implementation System)
MOSFET	MOS Field-Effect-Transistor
MSB	Most Significant Bit
NMOS	N-channel MOS
PAL	Programmable Logic Array
PMOS	P-channel MOS
S1,2,3	switch labeling convention
SAR	Successive Approximation Register
SPICE	circuit simulation program

Chapter 1

Introduction

Since the introduction of the first microprocessor early 1970's, the increased demand for faster and smaller digital processing elements has spurred the rapid growth of digital technology. Large thrusts were made to make these components both innovative and economical. Today, there are hosts of devices that operate in the digital domain: static and dynamic memories, EPROM's, PAL's, microprocessors and controllers as well as gate-arrays and ASIC's (Application Specific Integrated Circuits). The cost and turn-around time for producing some of these chips is very small. For example, turn-around times for some gate-arrays used for prototyping logic designs can be as little as *one day*.

There still remains a constant demand for faster and smaller digital chips, but the focus is being shifted to interface and sensing technologies. Since large memories and powerful microprocessors are available at low cost, efforts are being made to update interface technology. Analog signals must be converted to digital form, hence the need for fast and efficient analog-to-digital converters as well as digital-to-analog

converters. These comprise the information interface to the real analog world. In addition to the digital processing and data conversion elements, there is a need for more efficient and innovative *sensors* which convert physical or chemical parameters into electrical signals. Just as the digital industry sought for more creative, cheaper designs, the analog and sensor designers did also. The explosive demand for IC's made possible the complex silicon fabrication technology economically attractive. This industry has dictated the direction of both analog circuit and sensor designers. If a design can be implemented using conventional digital IC technology (or by a slight modification), then it is economically advantageous to do so.

This trend can be observed in the frequent use of CMOS technology in analog circuit design, though its origins are in digital design [1]. In this decade, sensor designers have taken advantage of some of the unique processing aspects of silicon [2]. The ability to precisely etch silicon into diaphragms and other structures makes possible total integration of sensor, interface, and information processing on one chip. The economic advantages of system integration are potentially enormous.

There are many research groups working on the development of interface technology (A/D and D/A converters) and sensor technology. Unfortunately, they have tended to be isolated from each other, resulting in sub-optimal sensing systems. Sensor performance depends heavily on the specific data read-out scheme [3]. For example, a circuit may be able to overcome a sensor design problem, and vice versa.

The goals of this thesis project are to approach the sensor read-out problem from a *circuit design* standpoint. The criteria for such a read-out have been established in the literature [4]. Specifically, the goals of this report are

1. Exploration of sense phenomena (mainly piezoresistive and capacitive)

2. Investigation of the capacitive read-out technique

3. Theory behind the charge redistribution technique used as the sense circuitry

4. Study of the system design issues that employ such circuitry

5. Evaluation of prototype performance

There are many macroscopic variables that are detectable as a change in capacitance. For convenience, this thesis concentrates on primarily those that manifest themselves as a force on a movable diaphragm, e.g. pressure or acceleration.

Many mechanical measurements made today involve sensing pressure. Its precise detection is important to the automotive, aerospace, biomedical and microphone industries as well as to acoustical research. Due to the rapid development of the microprocessor, the transducer has become the focus of similar development. There is a growing need to make transducers robust and compatible with microprocessors because of the increased power and decreased cost of the control unit within a measurement system. The micromachining of silicon makes this possible and ideally suited to pressure-sensing applications [2]. Compliant structures can be machined on silicon substrates that sense pressure by deformation or deflection. This relatively new technology bridges the interface between sensor and control, making possible monolithic sensor systems, or so called "smart sensors" [5].

A variety of methods are employed to detect pressure. The major types employ Bourdon tubes, capsules, bellows and diaphragms [6]. The latter is extensively used in silicon pressure sensors. Sensing techniques cover a wide area, including piezoelectric elements, metallic and semiconductor strain gages, potentiometers, variable inductance and capacitance devices, and differential transformers [6]. Most

commonly used in silicon diaphragms are piezoelectric elements, strain gages, and variable capacitance devices [7].

Variable capacitance sensors incorporate microstructures that respond to pressure variations by deformation or deflection. This causes a change in the gap of a capacitor that has one fixed plate and another movable plate or diaphragm. The gap change caused by deformation causes a capacitance change that can be detected and later translated into a corresponding pressure. Advantages of this method over its piezoresistive counterparts are higher sensitivity to pressure and lower sensitivity to temperature variations [3]. Unfortunately, sophisticated read-out circuitry must be employed to detect small capacitance changes in small capacitors in the presence of large parasitic capacitances. The challenge is to design circuitry that is compatible with regular MOS fabrication and silicon micromachining processes, and that can overcome the problems of parasitics and noise. Present systems employ both ac and dc techniques to sense capacitance change. However, the sense capacitors employed in these techniques are usually much greater than the stray parasitics encountered in practice. As silicon diaphragms are scaled, new circuitry must be developed to handle smaller sense capacitors. This is due to the ability of semiconductor processes to scale horizontally across a wafer. If an operational structure can be built smaller, then it is more economical to do so since the processing cost depends on area.

Another key use of the variable capacitance method is measuring deflections of cantilever beams due to *acceleration.* This has been pursued and is ideally suited to the capacitance read-out scheme [8],[9]. Since the detection is due to a deformation, the *cause* of the deformation can be sensed. This could be air pressure, tactile pressure [10],[11], or accelerations. All that is needed is the manifestation of the

parameter of interest as a deflection of a structure. Due to the rapid advancement of silicon micromachining, a variety of sensing structures can be built with precision [2],[12],[13].

Capacitance change in a capacitor is not limited to only deflection changes in its plates. The dielectric media can change in reaction to some external stimuli causing a corresponding capacitance change. This idea has been implemented commercially to monitor epoxy cure cycles [14].

This thesis deals with using a charge redistribution technique in detecting extremely small capacitive differences in fixed value capacitors caused by semiconductor processing. A chip is designed and sent to MOSIS (MOS Implementation System) for fabrication using a 3 μm p-well CMOS process. The test chip is used to determine the effectiveness of the charge redistribution technique in measuring capacitive differences in metal-to-poly capacitors on the order of 20 to 100 femtofarads. This is approximately the size of sense capacitors that would be fabricated on silicon. The effects of MOS switch charge injection and comparator offset are canceled. Other second-order effects are also considered.

The thesis consists of six chapters. Chapter 2 gives the theoretical and historical background on the charge redistribution technique and the calibration scheme. Chapter 3 and 4 deal with the theory and circuit implementation of the technique. Associated problems with noise and fundamental limitations are discussed. Chapter 5 presents experimental results that are correlated with theory. Lastly, Chapter 6 concludes with system issues concerning the mating of this read-out scheme with silicon sensors. Comparisons to other read-out schemes as well as physical limitations of sensitivity and size are given. The Appendix includes sections on the generality of the charge redistribution technique, alternate switching sequences, and

fundamental limitations.

Chapter 2

Theoretical Background

2.1 Force Detection Methods

There are several ways to detect force. In the development stages are optical techniques using interferometry to sense distance changes caused by deflections of structures. These may offer the highest pressure sensitivity and noise immunity. In widespread use today are pressure transducers that exploit piezoresistivity. They employ piezoresistors that convert the strain of a given structure into a voltage that can be detected. Piezo-junction devices, on the other hand, utilize differences in reverse junction leakage current as a measure of the pressure on the material [3]. The latter, however, suffers from instability mechanisms and is effective only at high strain levels that approach the fracture level in silicon. Piezoresistive readout is much more sensitive and stable under normal operating conditions. Capacitive transducers are also widely employed. These detect a change in force by a change in capacitance of a deformable structure. Both the piezoresistive and capacitive

techniques can be adapted to silicon microstructures. Each has its advantages and disadvantages.

2.1.1 Piezoresistive Technique

The phenomena of piezoresistance involves a change in resistance of a material due to an applied stress. For a diffused resistor subjected to parallel and perpendicular stress components $\sigma_{\parallel}$ and $\sigma_{\perp}$ respectively, the resistance change is

$$\frac{\Delta R}{R} = \pi_{\parallel}\sigma_{\parallel} + \pi_{\perp}\sigma_{\perp} \tag{2.1}$$

where $\pi_{\parallel}$ and $\pi_{\perp}$ are the piezoresistive coefficients parallel and perpendicular to the resistor length [3]. The theory of piezoresistivity is not given here. The lattice strain caused by the applied pressure changes carrier scattering behavior and hence affects resistivity. By orienting resistors in a bridge topology, changes in resistance due to an induced strain can be detected as an output voltage. This output voltage can be related to a pressure exerted on a diaphragm. It can be proven that the π coefficients are nearly equal and opposite for orientation of the resistors in the (110) direction [3]. Resistors oriented parallel and perpendicular to a diaphragm edge will experience a resistance change nearly equal and opposite. By use of a full-bridge topology, common-mode errors due to temperature variations can be canceled to first order. However, sensitivity to resistor doping level and temperature is high and cannot be completely ignored.

Placement of piezoresistive elements near the diaphragm or test structure is critical to sensor performance. Sensitivity increases as the resistors are placed near the edges due to increased stress there. Tradeoffs include resistor reproducibility (using large resistors) versus pressure sensitivity (using smaller resistors for higher

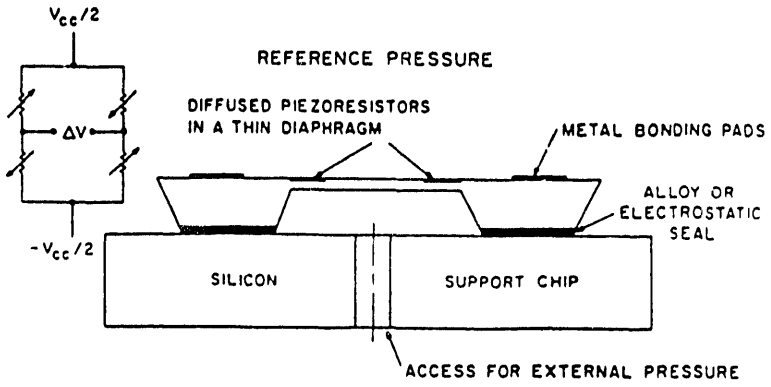

Figure 2.1: Piezoresistive silicon pressure diaphragms (from [3])

average stress), diaphragm size and thickness. All of these factors contribute to a potential decrease in sensitivity and a larger error in the measurement.

This technique is popular as a read-out scheme applied to silicon pressure sensors in spite of large non-linearity for higher-order piezoresistive coefficients and process dependent effects. Temperature coefficients for zero-pressure offset have been reported between 1 and 5 mmHg/°C depending on doping levels [15]. Temperature compensation is used to reduce these effects despite increased costs. This may be due to the lack of alternate methods of pressure detection besides the capacitive method, which until recently required extensive circuitry [15].

Shown in Figure 1 (2-1) is a typical piezoresistive configuration applied to a silicon diaphragm. In recent years, several novel structures have incorporated this method for pressure and acceleration detection [16]–[20]. There have been few improvements in the reduction of temperature sensitivity due to the inherent mechanisms that cause piezoresistivity. This has led others to explore the use of capacitive readout for sensing pressure.

2.1.2 Capacitive Technique

Capacitive pressure sensors detect pressure by a change in capacitance in a deformable structure. There are no less than six temperature mechanisms in piezoresistive sensors, three of which appear in the capacitive sensor: plate deflection temperature sensitivity, packaging stress and gas temperature between capacitor plates. These can be easily reduced and controlled so that capacitive sensors feature low temperature sensitivity [15]. For a capacitive sensor shown in Figure 2 (2-2), the capacitance between the plates is

$$C = \iint \frac{\epsilon_0}{S - w(x,y)}\, dx\, dy \tag{2.2}$$

where ϵ_0 is the free-space dieiectric constant, S is the zero-pressure plate separation, and $w(x,y)$ is the deflection response to the applied pressure [3]. Studies have shown that with a diaphragm of the same thickness, the intrinsic unloaded pressure sensitivity of the capacitive technique is an order of magnitude greater than the piezoresistive technique [3]. However for silicon diaphragms, the zero-pressure capacitance may be quite small (on the order of tenths of a picofarad) which complicates the capacitance detection circuitry. For particular readout circuits, parasitic capacitances cause an error in the measurement. The detection circuitry is of paramount importance to the feasibility of such a scheme.

Because of the increased pressure sensitivity and decreased temperature sensitivity, the capacitive sensor has become a viable alternative to the piezoresistive sensor. A popular detection method utilizes an oscillator which drives a capacitive bridge circuit. A change in capacitance relative to a reference capacitance causes an output voltage (depending on the output scheme) or shift in frequency which can be detected by an external circuit [21]-[26]. The main cause of error is the

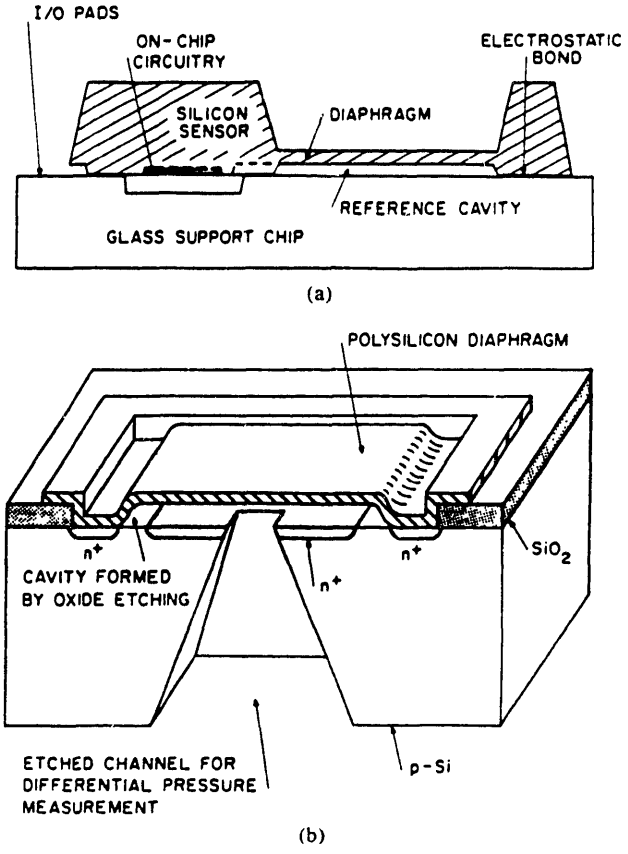

Figure 2.2: Capacitive silicon pressure sensor (from [49])

existence of stray parasitic capacitance. In most of the literature, the sense and reference capacitors are often an order of magnitude *larger* than the parasitics so that errors due to parasitics are either ignored entirely, or are calculated but usually deemed insignificant [22],[24],[26]–[29]. It is unclear what the effect of large parasitic capacitances (when compared to the sense and reference capacitors) will have on these measurement techniques. Major areas of research involve modeling and fabrication of the silicon diaphragms [2],[30]–[32] (for better reproducibility), and the development of capacitance detection methods using oscillator-drive techniques [23],[25],[26],[33]. Recently, the advent of switched-capacitive ideas have led to new and innovative methods of capacitance detection [28],[29],[34]. However, problems appear that are inherent to all switched-capacitive circuits. MOS switch charge injection, clock feedthrough, and circuit noise become a major limiting factor in circuit performance. These problems are not new to the MOS analog circuit designer. Switched-capacitive circuits have been applied to filter design and analog-to-digital converters with great success. A majority of problems have been circumvented or solved using novel circuit methods. Such methods are discussed in the next section.

2.2 Calibration Technique : Historical Origins

As mentioned earlier, the capacitive technique offers substantial gains over the piezoresistive method. Common to most capacitive detection schemes is an oscillator-driven detection circuit. Most information processing is accomplished by a microprocessor so that frequently the analog data from the detection circuitry must be converted externally by a data acquisition system. This system is usually not included as part of the detection scheme, though it plays a key role in sensor sys-

tem performance. The calibration technique addresses problems associated with switched-capacitive circuits while being an integral part of a data acquisition system. Digital and analog data are available as a consequence of the technique so that external data conversion is not necessary. The idea was first utilized in making capacitor mismatch measurements [35], then later extended to analog-to-digital converters employing binary-weighted capacitor arrays [36]. Since its origins lie in and charge-redistribution A/D converters, a brief overview of the relevant topics is given.

As demand increased for precision analog circuits, the switched-capacitive idea emerged in analog-to-digital converter designs [37]. For high-precision A/D converters, individual trimming and component matching are needed. Though this is still the case for extremely high-precision circuits, designers have developed ideas that avoid this costly procedure through clever circuit design. In 1975, a method was presented that measured capacitive mismatches on an IC [35]. It was developed for measuring capacitive mismatches in binary-weighted capacitor arrays because capacitance measurements were inadequate at that time. These arrays were used in a new charge redistribution A/D conversion method [37],[38].

2.2.1 Charge Redistribution A/D Conversion

In Figure 3 (2-3) is a conceptual example of the operation of a five-bit A/D conversion using the charge redistribution technique. The components consist of a binary weighted capacitor array, MOS switches, and a comparator. A/D conversion is achieved in three steps:

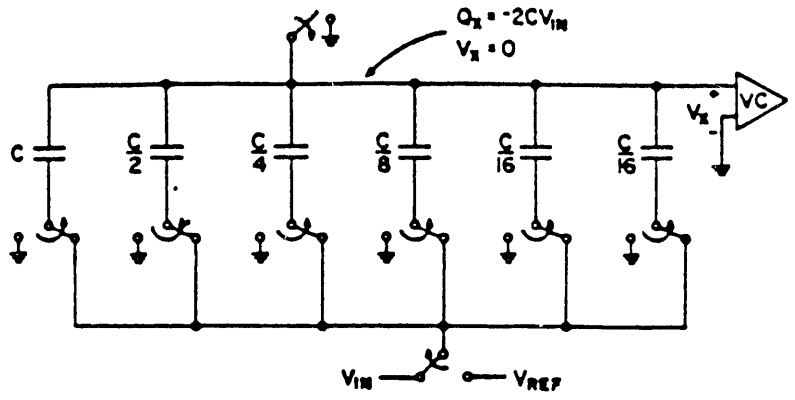

Figure 2.3: Simulation of 5-bit charge redistribution A/D converter (from [37])

1. Ground the top node so that V_x is ground. Set the bottom plates of the capacitors in the array to the input voltage to be converted.

2. Open the top switch so that the top node floats. Connect the bottom plates of the capacitors to ground. These two steps have stored a charge on the top node that is proportional to the binary-weighted sum of the input voltage.

3. Apply a reference voltage V_{ref} to the largest capacitor in the array. The output of the comparator will be the most significant bit of the A/D conversion. If the bit is zero, then return the bottom plate to ground, else continue to the next largest capacitor (C/2) until all N bits have been determined.

To see how these steps are mathematically equivalent to an A/D conversion, consider the charge stored due to the first step. The charge stored is

$$Q_1 = -V_{in}\left[C + \frac{C}{2} + \frac{C}{4} + \frac{C}{8} + \frac{C}{16} + \frac{C}{16}\right] = -2V_{in}C$$

After the top node is isolated, voltages are applied to the bottom plates of the capacitors which will *redistribute the charge on the top node.* If we apply a voltage V_{ref} to the largest capacitor (C), the voltage V_x can be found due to charge conservation, i.e. Q_1 must be equal to any expression of the charge after the top switch is opened. With V_{ref} applied to the largest capacitor C, the expression for charge becomes

$$Q_2 = 2V_xC - V_{ref}C$$

Setting $Q_1 = Q_2$ and solving for V_x yields

$$V_x = -V_{in} + V_{ref}\frac{C}{C_{total}}$$

Notice the extra $\frac{C}{16}$ capacitor in the array. This is used so that the total capacitance on the node is 2C and hence the capacitive divider ratio will always be a *power of 2.* Thus

$$V_x = -V_{in} + \frac{V_{ref}}{2}$$

The comparator senses V_x.

$$\text{If } V_x > 0 \text{ then } V_{in} < \frac{V_{ref}}{2}$$

$$\text{If } V_x < 0 \text{ then } V_{in} > \frac{V_{ref}}{2}$$

More generally, for testing the i^{th} bit in an N-bit conversion, where the LSB is b_0 and the MSB is b_{N-1}, the algorithm is

$$\text{If } V_x > 0 \text{ then } V_{in} < \xi_{N-i} \text{ so set } b_{N-i} = 1 \tag{2.3}$$

$$\text{If } V_x < 0 \text{ then } V_{in} > \xi_{N-i} \text{ so set } b_{N-i} = 0 \tag{2.4}$$

where ξ_{N-i} is given by

$$\xi_{N-i} = \sum_{j=1}^{N-i} b_{N-j}\frac{V_{ref}}{2^j} \tag{2.5}$$

and in actuality, b_{N-i} is set to one (our initial guess), and the comparator will tell us whether to change it to zero or not. This is the key to the A/D conversion. By applying V_{ref} to different binary-weighted values of C, we can either add or subtract these terms to V_x. The comparator will tell us which terms to keep and which to discard. This is exactly the process of successive approximation A/D conversion.

For N-bit resolution, N redistributions are necessary. After conversion, all the charge will remain on the capacitors representing terms that are kept while others are discharged. The digital code can either be stored sequentially from the comparator or can be obtained by looking at the state of the MOS switches after conversion. There are numerous interesting characteristics of this technique. For example, the initial charge sampled on the top node was dependent only on V_{in}. This need not be the case. If additional charge is added by applying V_{ref} to the largest capacitor, then essentially this shifts the value of V_x so that A/D conversion can accommodate negative inputs, where negative inputs are represented by 1's complement [37].

Parasitic capacitance sensitivity is minimized since it normally is not time-varying. It contributes a charge term in all the steps and therefore cancels out. The accuracy of this technique depends on the control of capacitive ratios. This led to the consideration of new and accurate methods of measuring capacitive mismatches since ratio matching determined the resolution.

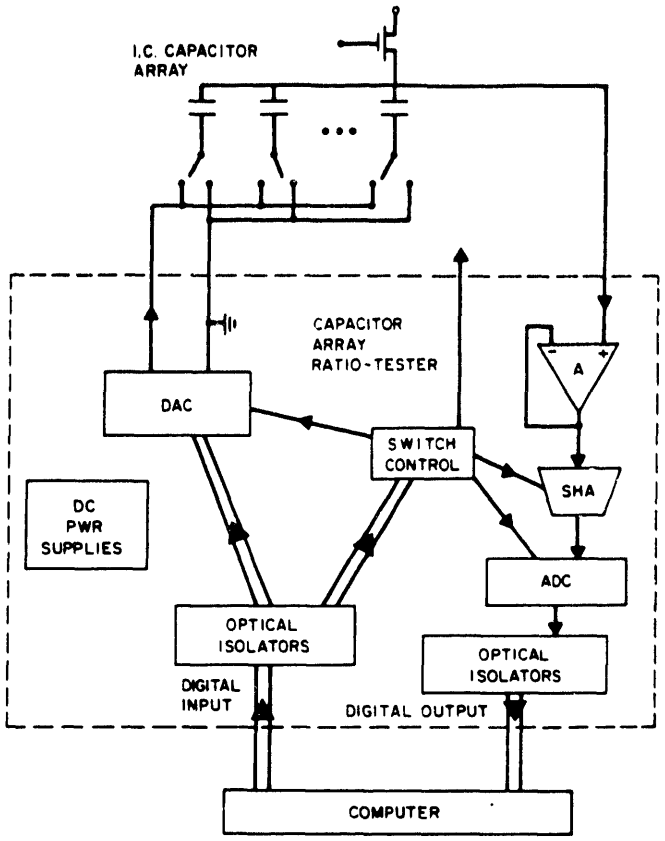

Figure 2.4: Capacitive mismatch system (from [35])

2.2.2 Capacitance Mismatch Measurement in A/D Converters

In 1979, McCreary and Sealer published a paper that demonstrated the use of the charge redistribution technique as applied to capacitive mismatch measurement [35]. Capacitance bridges were initially used to measure the arrays but were inadequate due to large-scale non-linearities of the bridge. An algorithm was developed that allowed calculation of ratio errors. Figure 4 (2-4) shows a typical implementation of the algorithm. In the following discussion, the notation for the capacitors is the

following:

$$C_k = 2^k C, \quad k = 0a, 0b, 1, 2, \cdots, N-1 \tag{2.6}$$

C_k denotes a capacitance that is 2^k times larger than the unit capacitance C, and k will take on values from 0 to $N-1$, where N is the number of bits of the A/D converter that uses this binary array. The unit capacitance C is defined such that the total capacitance is exactly equal to $2^N C$. Notice that there are two capacitors with a value C: C_0^a and C_0^b. For the C_9 capacitor, the ratio of C_9 to the total capacitance should be one-half. C_0^a is the termination capacitor needed to make the capacitive divider ratio always a power of two. In general, the difference between the capacitor C_k and the rest of the array is

$$C_k - \sum_{i=1b}^{k-1} C_i$$

This can be calculated for the k^{th} capacitor in two steps:

1. V_x node is grounded and a voltage V_{ref} is applied to C_k while grounding all others.

2. The top node is isolated, and the voltages on the capacitors are *switched.*

The voltage at the top node is, after step 2,

$$V_x = \frac{V_{ref}}{C_{total}} \left[C_k - \sum_{i=1b}^{k-1} C_i \right] \tag{2.7}$$

Thus the errors due to capacitive mismatches can be found since both V_x and V_{ref} are known.

This technique was implemented to study capacitor mismatch errors that cause linearity errors in charge redistribution A/D converters. Elimination of charge injection sources is crucial in obtaining higher resolution and smaller errors in these

A/D converters. In 1984, Lee extended error-correcting ideas to the above technique in achieving a 15-bit A/D converter [36]. The idea of *self-calibration* allowed higher resolution by eliminating errors caused by component matching and charge injection. It is a powerful concept, and the next chapter is devoted to understanding it. It can be applied to determine precise mismatches of very small capacitors. This is exactly what is needed in capacitive sensor design.

Chapter 3

Self-Calibration Technique : Theory

3.1 Application to A/D Converters

Successive approximation A/D converters require precise component matching to achieve high resolution and good linearity. Their performance is limited by errors in ratio matching. Higher performance converters usually employ a hybrid technology in order to achieve good component matching. Usually thin and thick film technologies in conjunction with laser-trimming can achieve the small tolerances needed in 16-bit converters. This is a costly procedure since each converter must be specially trimmed.

The self-calibration technique avoids this process by calibrating out errors in component matching. Errors are stored in memory, then recalled when a correction

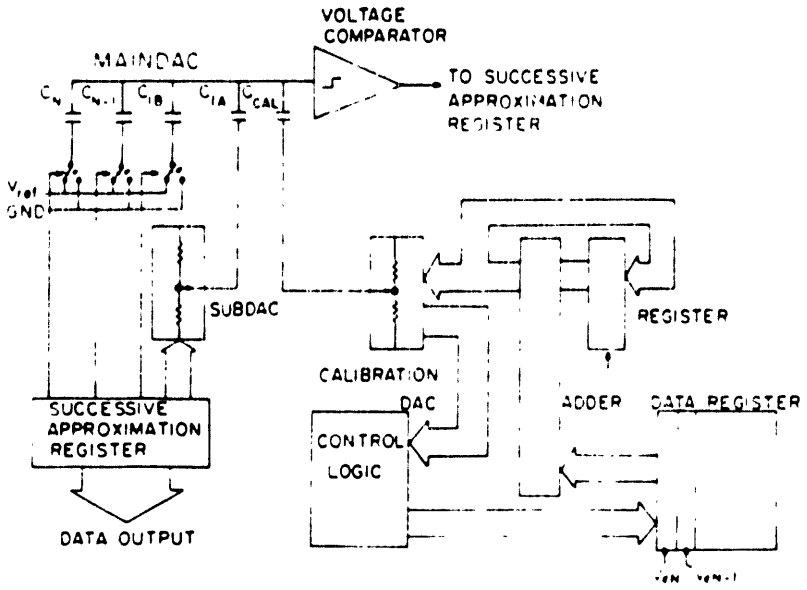

Figure 3.1: Block diagram of self-calibrating A/D converter (from [36])

is needed. Calibration can be done at any time, eliminating long-term drift effects. The technique can be implemented in standard CMOS or NMOS technology.

Figure 1 (3-1) shows the block diagram of the self-calibrating A/D converter. It consists of an N-bit capacitor array main DAC (Digital-to-Analog Converter), an M-bit resistor string sub DAC, and a resistor string calibration DAC. The main DAC and the sub DAC are used as the successive approximation A/D converter, while the calibration DAC is used to find and supply the error-correcting voltages to the main DAC. Since the sub and calibration DAC's have errors, two additional bits of resolution are needed to overcome errors in a 16-bit A/D converter [36]. The total resolution for this A/D converter is $N + M$. The resistor sub DAC is used as the coarse DAC, and the capacitive main DAC is used as the fine-tune DAC. The following discussion focuses on the capacitive main DAC *only* so that any reference to an A/D conversion refers to the main DAC and not the sub DAC.

The calibration cycle computes errors in the mismatch ratio of the capacitor array. In the following discussion, the notation for capacitances is consistent with Section 2.2.3 on capacitive mismatch measurements. It differs somewhat from the original paper by Lee [36]. Assume that each binary-weighted capacitor C_k has an error such that

$$C_k = 2^k C(1 + \epsilon_k), \quad k = 0a, 0b, 1, 2, \cdots, N-1 \tag{3.1}$$

where C has been defined as an *average unit capacitance*. In the charge redistribution A/D conversion cycle, the k^{th} capacitor corresponding to the k^{th} bit determination has a voltage residue on the top node of

$$V_x = -V_{in} + V_{ref}\left[\frac{C_k}{\sum_{i=0a}^{N-1} C_i}\right] \tag{3.2}$$

Substituting C_k from equation (3.1) into equation (3.2) yields

$$V_x = -V_{in} + V_{ref}\left[\frac{2^k C(1+\epsilon_k)}{\sum_{i=0a}^{N-1} 2^i C(1+\epsilon_k)}\right] \tag{3.3}$$

The term added to $-V_{in}$ reduces to

$$V_{ref}\left[\frac{2^k C(1+\epsilon_k)}{2^N C + \sum_{i=0a}^{N-1} 2^i C\epsilon_i}\right] \tag{3.4}$$

The total sum of errors $\sum_{i=0a}^{N-1} 2^i C\epsilon_i$ is *zero* since C is defined such that $2^N C$ is the total capacitance. Thus equation (3.4) reduces to

$$V_{ref}2^{k-N} + V_{ref}2^{k-N}\epsilon_k \tag{3.5}$$

The error due to the capacitive mismatch is the last term. Let this be the error voltage

$$V_{\epsilon k} = V_{ref}2^{k-N}\epsilon_k, \quad k = 0b, 1, 2, \cdots, N-1 \tag{3.6}$$

The subscript k refers to the k^{th} capacitor that is 2^k times larger than the unit capacitor C. It also refers to the k^{th} bit being determined in the A/D conversion,

where N is the number of bits. Total linearity error is

$$V_{error} = \sum_{i=0}^{N-1} b_i V_{ei} \tag{3.7}$$

where b_i represents the i^{th} bit of the digital output code $b_{N-1}b_{N-2}\cdots b_0$. During the calibration cycle, these errors are measured by a calibration DAC and stored in a RAM. During the conversion cycle, when the i^{th} bit is being determined, the calibration DAC subtracts out the error voltage by applying a voltage to a coupling capacitor connected to the capacitor array.

The self-calibrating technique was developed to reduce the errors due to component matching in A/D converters. It was used to calibrate out non-linearity errors. Notice that the idea can be equally applied to measuring capacitive differences and *random or controlled sources of charge injection.* This technique can measure offset errors due to capacitive mismatch, comparator offsets and charge injection and can compensate and/or calibrate a system that has these errors. The technique is ideal for measuring capacitive differences (as in capacitive sensors) and reducing inherent circuit errors. The next section describes in detail the application of this idea to the measurement of capacitive differences.

3.2 Application to Measurement of Capacitive Differences

The basic circuit is shown in Figure 2 (3-2). It consists of the sense and reference capacitors (C_S and C_R), the coupling capacitor (C_C), three MOS switches, a voltage comparator, a digital-to-analog converter (DAC), a successive approximation register (SAR), and a memory register with associated logic capable of signal inversion.

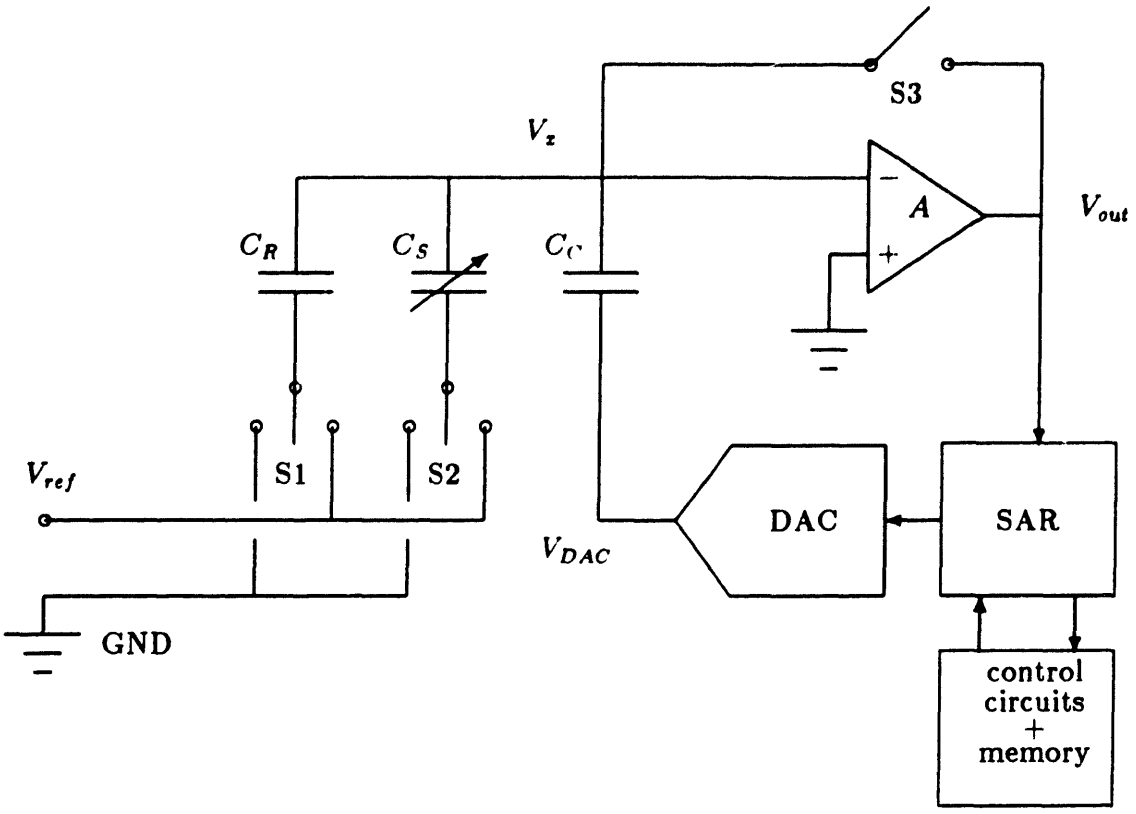

Figure 3.2: Ideal ΔC measurement system

The non-idealities of the circuit appear as the offset of the comparator (V_{os}) and its finite gain (A), parasitic capacitance to ground (C_P), and switch charge injection (Q_{S3}). To better understand how these non-idealities are taken into account, the ideal system in Figure 2 is first analyzed, then second-order effects are added later. In the assumption of an ideal circuit, $V_{os} = 0$, $C_P = 0$, $Q_{S3} = 0$, $A = \infty$, and DAC quantization error is negligible. The measurement technique proceeds in two steps.

Step 1

- Set S3 to closed position so that V_x is at ground potential.
- Set S1 to V_{ref}.
- Set S2 to ground.
- Set V_{DAC} to ground.

The charge at the top node is just $Q_1 = -V_{ref}C_R$. The comparator is implemented with an op-amp so that when the feedback loop is closed with switch S3, V_x is at ground potential.

Step 2

- Set S3 to open position.
- Set S1 to ground.
- Set S2 to V_{ref}.
- Initialize SAR/DAC.

When the successive approximation register is initiated, it outputs a voltage that is one-half the full-scale voltage. V_x responds by either becoming positive or negative relative to ground. The comparator senses this change and output either a one or zero to the SAR. If the output of the comparator is a one, then the SAR keeps that voltage, adds half of the previous voltage, and applies this voltage to C_C. If the output is a zero, then instead of adding half the previous voltage, it subtracts it and

applies it to C_C. This continues until the SAR reaches its quantization limit and stops. If the SAR, DAC, and voltage comparator are ideal, then the voltage from the DAC (V_{DAC}) precisely forces the top node voltage (V_x) to zero. The charge at the top node is thus

$$Q_2 = -V_{ref}C_S - V_{DAC}C_C$$

By charge conservation, $Q_1 = Q_2$ so that

$$-V_{ref}C_R = -V_{ref}C_S - V_{DAC}C_C$$

$$V_{DAC} = \frac{V_{ref}(C_R - C_S)}{C_C} \tag{3.8}$$

The output of the DAC produces a voltage proportional to the capacitive difference of C_S and C_R. Appropriate choices of V_{ref} and C_C can be made so that the maximum dynamic range of the DAC can be utilized. The parameter $\frac{\Delta C}{C}$ can be found by multiplying the numerator and denominator by C_R or C_S and rearranging so that

$$\frac{\Delta C}{C} = \left[\frac{V_{DAC}}{V_{ref}}\right]\left[\frac{C_C}{C}\right] \tag{3.9}$$

where C is a normalizing capacitance and typically is either C_R or C_S. Notice that the result is a product of two ratios: a voltage ratio that can be measured easily, and a capacitive ratio that is equal to the area ratio of the capacitors, given that the dielectric and gap thickness are the same for both capacitors.

3.3 Non-Ideal Effects

In principle, the technique outlined in Section 3.2 should give the difference between two capacitors. However, there are errors introduced when the algorithm is implemented in any practical technology. Limitations due to component design, noise,

and physical phenomena cause errors in the measurement. This section deals with these limitations and determines their effect on practical circuit performance of the algorithm.

Possible causes of error in the practical implementation of the algorithm are :

1. **Circuit Non-Idealities**
   (a) MOS switch charge injection
   (b) Comparator offset with finite gain
   (c) Parasitic capacitance
   (d) SAR/DAC quantization error
2. **Component Non-Idealities**
   (a) Capacitor hysteresis
   (b) Transistor hysteresis
   (c) Junction leakage
   (d) Temperature coefficient of the capacitors
   (e) Voltage coefficient of the capacitors
3. **Noise Sources**
   (a) Switch noise
   (b) Circuit noise
   (c) Clock feedthrough
4. **Other sources of charge injection or depletion**

Item 1 is modeled by a modified ideal circuit block diagram, and the offset calibration algorithm can be applied to eliminate some of these effects. Item 2 represents physical phenomena and their presence is evaluated. Item 3 represents limitations on the practical implementation of the algorithm. Elimination of some but not all of these effects is possible. Finally, Item 4 denotes a random unknown charge generation or recombination factor which could disturb the measurement.

3.3.1 Circuit Non-Idealities

A modified block diagram of the circuit implementation is shown in Figure 3 (3-3). The comparator has an offset V_{os} and a finite gain A while the switch S3 injects a charge Q_{S3} when opened. A parasitic capacitance C_P exists as well as a DAC quantization error of $\pm\frac{1}{2}$LSB. It is found that the algorithm can be implemented in either a closed-loop or open-loop topology. In the closed-loop topology, it is important to note that if the feedback path due to switch S3 must cause $V_x = V_{os}$, the comparator must operate as an op-amp and cannot be a regenerative latch comparator with only high or low digital outputs. When the SAR/DAC feedback loop is initiated, the operation of the comparator can be limited to digital outputs since the SAR/DAC generate the appropriate analog signal to the coupling capacitor as feedback. Usually the comparator can be designed as a high-gain op-amp that can act as a voltage comparator when its output saturates. In the open-loop topology, the feedback loop through S3 is never used so that the comparator may always have digital outputs. Since the analog signal for measurement of small capacitors is usually small, a monolithic preamplifier can be used to buffer the data to an off-chip comparator in this configuration. In the analysis, the closed-loop is considered first, then the open-loop.

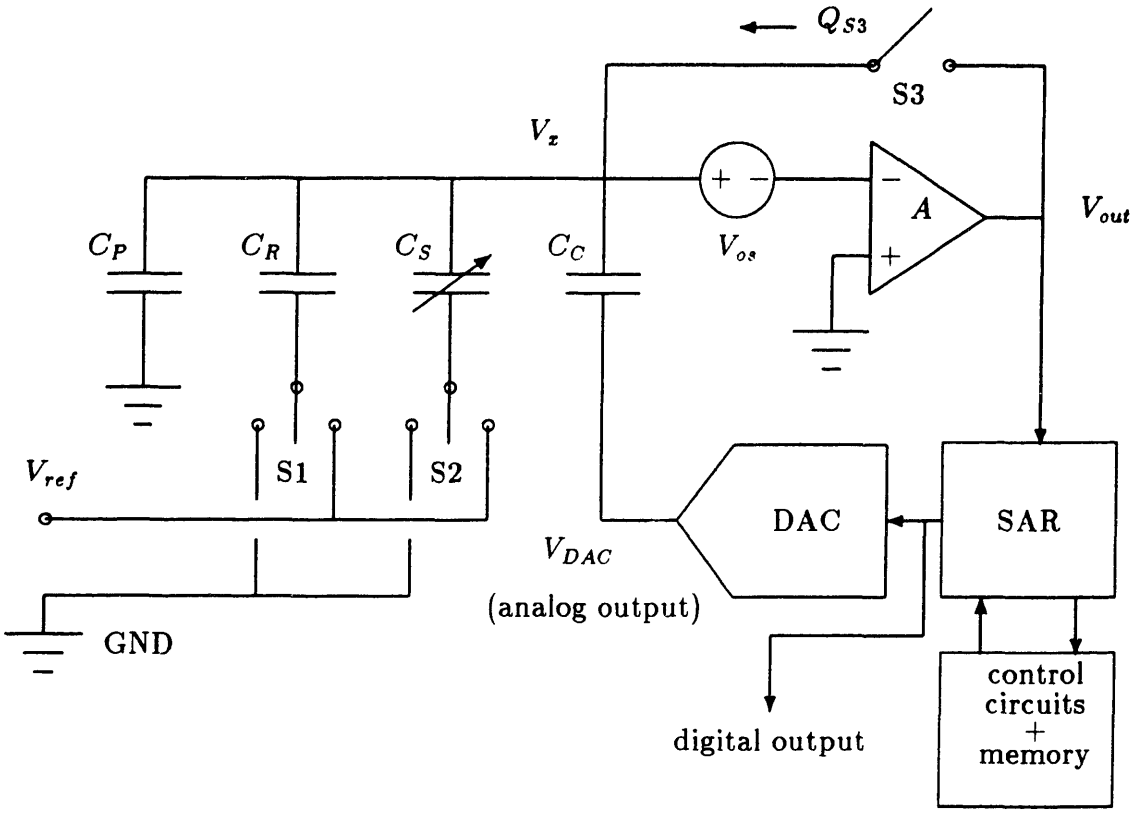

Figure 3.3: Non-Ideal ΔC measurement system

Closed-Loop Topology

Assuming that V_{DAC} is in error, the amount of error transferred to V_x can be easily calculated. Refer to Figure 3 (3-3). A real DAC can typicaliy resolve to $\pm\frac{1}{2}$LSB. Since it has finite resolution, it cannot exactly force V_x to ground. Assuming that V_x is at some voltage V_{os} and all the capacitors are grounded, the initial charge is

$$Q_i = V_{os}(C_P + C_R + C_S + C_C)$$

If $V_{DAC} = \pm\frac{1}{2}$LSB and the node is isolated, the final charge is

$$Q_f = V_x(C_P + C_R + C_S) + (V_x \pm \frac{1}{2}\text{LSB})C_C$$

By charge conservation, $Q_i = Q_f$ so that

$$V_{os}(C_P + C_R + C_S + C_C) = V_x(C_P + C_R + C_S) + (V_x \pm \frac{1}{2}\text{LSB})C_C$$

Solving for V_x yields

$$V_x = V_{os} \pm \frac{1}{2}\text{LSB}\left[\frac{C_C}{C_P + C_R + C_S + C_C}\right] = V_{os} \pm \delta(\frac{1}{2}\text{LSB}) \qquad (3.10)$$

where δ is the capacitive divider ratio

$$\delta = \left[\frac{C_C}{C_P + C_R + C_S + C_C}\right] = \frac{C_C}{C_{total}} \qquad (3.11)$$

Thus any change in voltage ΔV at V_{DAC} results in a change in voltage $\delta\Delta V$ at V_x. This is just a simple capacitive divider as seen from a charge conservation derivation. This introduces an error in the measurement.

Charge injection can be measured using the offset calibration technique. This is called the calibration cycle while the capacitive mismatch measurement is denoted as the measurement cycle. The calibration and measurement cycle inherently eliminate

the comparator offset in the *closed-loop topology*. In the *open-loop topology*, the offset is measured, then eliminated.

Consider the finite gain of the comparator. In the closed-loop topology, it must behave as a high-gain op-amp in Step 1. The output of the op-amp is

$$\begin{aligned} V_{out} &= A(V_{os} - V_{out}) \\ V_{out} &= \left[\frac{A}{1+A}\right] V_{os} \end{aligned}$$

If A is large such that $\frac{A}{1+A} \approx 1$ then $V_{out} \approx V_{os}$. For small input signals, there should be a preamplifier to buffer the chip to another comparator off-chip. The gain of the preamplifier must be large enough to overcome the hysteresis of the off-chip comparator. This is a small and feasible requirement.

The calibration procedure begins by measuring the charge injection. For generality, assume that the limitation of the DAC may be quantization errors or thermal noise such that the effective resolution of the DAC is $\pm\Delta V$.

Step 0A

- Set S3 to closed position. V_x becomes V_{os}.
- Set S1 to ground.
- Set S2 to V_{ref}.
- Set V_{DAC} to ground.

Assuming that the DAC cannot be a ground but is at $\pm\Delta V$, the charge on the top node is

$$Q_{0A} = V_{os}(C_P + C_R + C_S + C_C) - V_{ref}C_S \pm \Delta V C_C$$

Step 0B

- Set S3 to open position.
- Initialize SAR/DAC.

The SAR/DAC forces V_X to $V_{os} \pm \delta\Delta V$. The charge on the top node becomes $Q_{0A} + Q_{S3}$ due to switch injection. After the SAR has finished, the charge can be calculated as

$$Q_{0B} = (V_{os} \pm \delta\Delta V)(C_P + C_R + C_S + C_C) - V_{ref}C_S - V_{DAC}C_C$$

By charge conservation, $Q_{0A} + Q_{S3} = Q_{0B}$. The offset terms and the $V_{ref}C_S$ terms cancel. Replacing δ by equation (3.11) and assuming that in worst case the $\pm\Delta V$ terms add, V_{DAC} becomes

$$V_{DAC_{cal}} = \frac{-Q_{S3}}{C_C} \pm 2\Delta V \tag{3.12}$$

Charge injection must be measured since it upsets the charge conservation assumption made in the earlier ideal circuit analysis. If it is taken into account, charge due to the capacitors can be accurately determined and hence the capacitive difference. Once the switch injection voltage is measured, it can be stored in a RAM. When the *negative* of $V_{DAC_{cal}}$ is applied to the coupling capacitor, a voltage at V_x is created that cancels out the error voltage generated by the switch injection charge. Alternatively, one can think of the DAC as creating a positive charge on the coupling capacitor that is just large enough to cancel the negative switch injection (assuming an NMOS switch) and hence the only charge available for measurement is due to the voltage on the capacitors. The sequence for measurement is

Step 1

- Set S3 to closed position. V_x becomes V_{os}.
- Set V_{DAC} to $-V_{DAC_{cal}}$.
- Set S1 to V_{ref}.
- Set S2 to ground.

Assuming that when we apply $-V_{DAC_{cal}}$ it introduces another error $\pm\Delta V$, the charge at the top node is

$$Q_1 = V_{os}(C_P + C_R + C_S + C_C) - V_{ref}C_R + V_{DAC_{cal}}C_C \pm \Delta V C_C$$

Step 2

- Set S3 to open position.
- Set S1 to ground.
- Set S2 to V_{ref}.
- Initialize SAR/DAC. This forces $V_x = V_{os} \pm \delta\Delta V$.

The charge on the top node becomes $Q_1 + Q_{S3}$ due to switch injection. After the SAR finishes, the charge expression can be written as

$$Q_2 = (V_{os} \pm \delta\Delta V)(C_P + C_R + C_S + C_C) - V_{ref}C_S - V_{DAC}C_C$$

By charge conservation, $Q_1 + Q_{S3} = Q_2$. Replacing $V_{DAC_{cal}}$ with equation (3.12) and δ by equation (3.11) yields similar terms on both sides: the charge injection

terms and the offset terms. The $\pm\Delta V$ terms do not necessarily cancel and in worst case they add. Solving for V_{DAC} yields

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V \tag{3.13}$$

In the calibration and measurement sequences, the errors due to the DAC when $-V_{DAC_{cal}}$ and ground are applied are taken into account. From the calculations made, one can easily deduce that the DAC is used four times, each time introducing an error of $\pm\Delta V$. Thus the worst case error occurs when all the error terms either add or subtract, $\pm 4\Delta V$.

The offset does not effect the technique because it shifts the voltage at V_x to V_{os} and does not change during the calibration and measurement cycles. Time-varying offsets are considered in a later section.

Effects of parasitic capacitance are canceled. It does impose a constraint on the system. A larger C_P causes a reduction in δ. If δ becomes too small, V_x becomes pinned by the large C_P and the DAC is not able to adjust V_x. The $\pm\Delta V$ error becomes limited by the capacitive divider ratio and not the quantization error because the minimum amount of control the DAC has is $\delta(\pm\frac{1}{2}\text{LSB})$ which may be less than the comparator resolution. A smaller C_P reduces δ but increases the kT/C noise so that a trade-off is introduced. This is examined in a later chapter.

Open-Loop Topology

When the measurement technique is done in an open loop configuration as in Figure 4 (3-4), the offset of the comparator is not canceled. This is because the final value of V_x in one step is not the same as the final value of V_x in the other. It

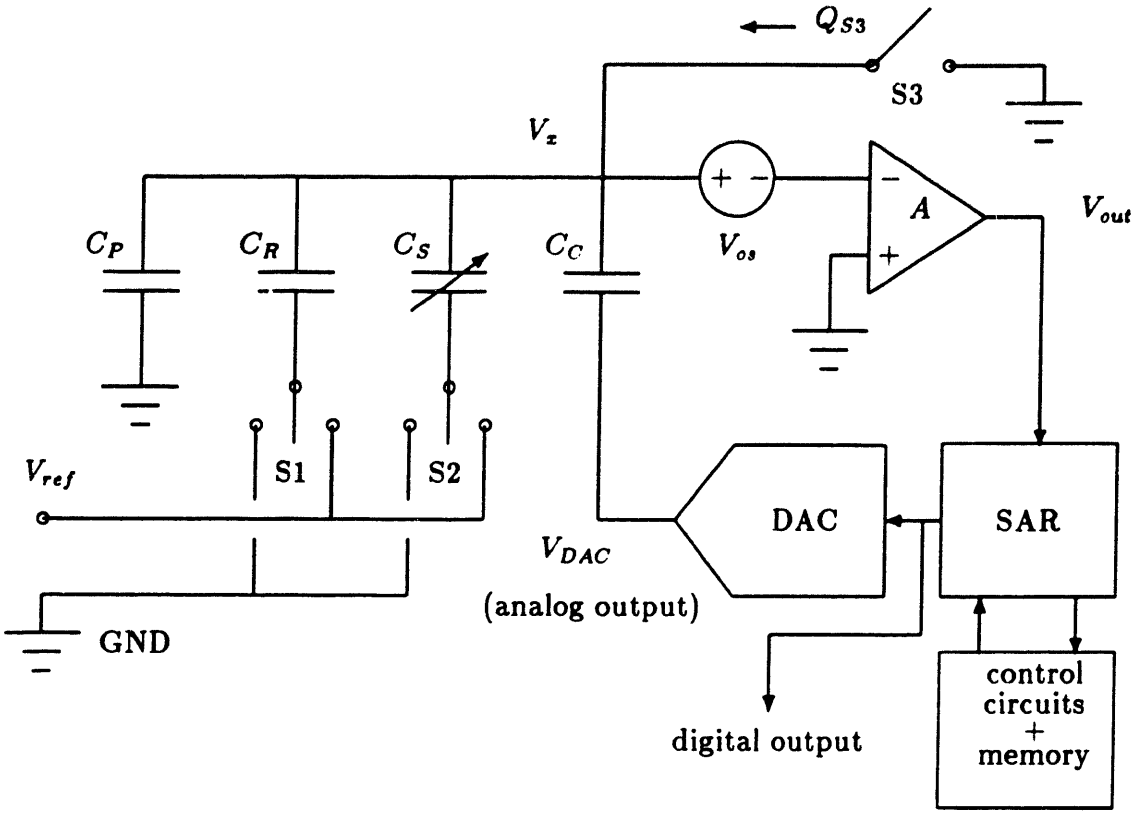

Figure 3.4: Non-Ideal ΔC measurement in open-loop

can be measured and eliminated in the measurement. In this configuration, the comparator does not need to have analog output capability and can act strictly as a voltage comparator with digital outputs. The calibration sequence is

Step 0A

- Set S3 to ground. V_x is zero, *not* V_{os}.
- Set V_{DAC} to ground.
- Set S1 to ground.
- Set S2 to V_{ref}.

The charge on the top plates of the capacitors is

$$Q_{0A} = -V_{ref}C_S \pm \Delta V C_C$$

Step 0B

- Set S3 to open position.
- Initialize SAR/DAC.

After the switch S3 is opened, the charge on the top node becomes $Q_{0A} + Q_{S3}$. The SAR/DAC forces V_x to $V_{os} \pm \delta\Delta V$ since this means a zero voltage at the input of an *ideal* comparator. The charge at the top node can be written as

$$Q_{0B} = (V_{os} \pm \delta\Delta V)(C_P + C_R + C_S + C_C) - V_{ref}C_S - V_{DAC}C_C$$

By charge conservation, $Q_{0A} + Q_{S3} = Q_{0B}$. Solving for V_{DAC},

$$V_{DAC} = \frac{(V_{os} \pm \delta\Delta V)(C_P + C_R + C_S + C_C)}{C_C} + \frac{-Q_{S3}}{C_C} \pm \Delta V$$

$$V_{DAC} = V_{os}\left[\frac{C_P + C_R + C_S + C_C}{C_C}\right] \pm \delta\Delta V\left[\frac{C_P + C_R + C_S + C_C}{C_C}\right] + \frac{-Q_{S3}}{C_C} \pm \Delta V$$

Substituting δ from equation (3.11) into the above yields,

$$V_{DAC_{cal}} = V_{os}\left[\frac{C_P + C_R + C_S + C_C}{C_C}\right] + \frac{-Q_{S3}}{C_C} \pm 2\Delta V \qquad (3.14)$$

This calibration cycle includes the comparator offset voltage because the top node is not returned to ground but rather to V_{os}. The offset can be calibrated out along with the switch injection.

In measurement, the cycle is similar to the closed-loop sequence:

Step 1

- Set S3 to ground. V_x is zero.
- Set $V_{DAC} = -V_{DAC_{cal}}$.
- Set S1 to V_{ref}.
- Set S2 to ground.

The charge on the top node is

$$Q_1 = -V_{ref}C_R + V_{DAC_{cal}}C_C \pm \Delta V C_C$$

Step 2

- Set S3 to open position.
- Set S1 to ground.
- Set S2 to V_{ref}.
- Initialize DAC/SAR. V_z becomes $V_{os} \pm \delta\Delta V$

After the switch S3 opens, the charge on the top node becomes $Q_1 + Q_{S3}$. After the SAR finishes, the charge on the top node is

$$Q_2 = (V_{os} \pm \delta\Delta V)(C_P + C_R + C_S + C_C) - V_{ref}C_S - V_{DAC}C_C$$

By charge conservation, $Q_1 + Q_{S3} = Q_2$. Substituting equation (3.14) for $V_{DAC_{cal}}$, and noticing that the offset terms and the charge injection terms cancel while the $\pm\Delta V$ terms add in worst case, V_{DAC} becomes

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V \tag{3.15}$$

The open-loop measurement yields the same result as the closed-loop. The disadvantage is that a large comparator offset may yield a calibration voltage larger than the DAC maximum and calibration becomes impossible. The closed-loop is preferred if large variations in offset voltage occur in an IC fabrication process. This is normally the case since offsets are almost impossible to control because of random transistor mismatches.

Summary of Important Equations

For open-loop topology,

$$V_{DAC_{cal}} = V_{os}\left[\frac{C_P + C_R + C_S + C_C}{C_C}\right] + \frac{-Q_{S3}}{C_C} \pm 2\Delta V$$

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V$$

For closed-loop topology,

$$V_{DAC_{cal}} = \frac{-Q_{S3}}{C_C} \pm 2\Delta V$$

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V$$

Capacitive mismatch ratio for both topologies becomes

$$\frac{\Delta C}{C} = \left[\frac{V_{DAC_{meas}}}{V_{ref}}\right]\left[\frac{C_C}{C}\right] \pm \left[\frac{4\Delta V}{V_{ref}}\right]\left[\frac{C_C}{C}\right] \tag{3.16}$$

where C is either C_R or C_S. It is the same as equation (3.9) in the ideal circuit case except for the error term,

$$\pm\left[\frac{4\Delta V}{V_{ref}}\right]\left[\frac{C_C}{C}\right] \tag{3.17}$$

This error term determines the minimum resolvable capacitance change. The effect of the parasitic capacitance appears as a constraint on the comparator resolution,

$$\delta = \left[\frac{C_C}{C_P + C_R + C_S + C_C}\right]$$

It should be emphasized that the expression for Q_{S3} is *negative* since it represents *electrons* from the channel of an NMOS switch. A PMOS switch injects *holes* so that the expression for Q_{S3} is *positive*.

In the analysis, the charge injection from the switches S1 and S2 is ignored. These switches cannot inject charge onto the top node, and therefore have no effect on V_x. For increased switching speed, the on-resistance of the MOSFET channels should be low, requiring the W/L ratios to be large. Consequently, S1 and S2 can be made as large as desired. S3 cannot be made too large since Q_{S3} is proportional to W/L. Too large a W/L results in $\frac{-Q_{S3}}{C_t}$ greater than the DAC range, making calibration impossible. Proper design can balance the tradeoffs involved in choosing the components needed in meeting a specific requirement. These design issues are discussed in Chapter 5.

3.3.2 Component Non-Idealities

In the analysis of Section 3.3.1, the components are treated as ideal elements. A voltage across a capacitor induces a charge on its plates, and when discharged, leaves no residual charge on the plates. Similarly, a MOSFET is assumed to have a constant threshold voltage and thus the comparator offset should not vary with time or input signal. This section discusses the non-ideality of the circuit components and their effect on circuit performance.

Capacitor Hysteresis

Capacitor hysteresis occurs because residual charge remains on a capacitor after it is discharged. Charging the capacitor in the forward direction and returning it to zero results in non-zero charge on the plates. Similarly, charging the capacitor in the reverse direction and returning it to zero yields a non-zero charge which may be different than the forward case. The curve is highly time dependent. If enough

time is allowed, the charge may relax to the zero-charge state. Studies have been made on this phenomena in MOS capacitors, and it appears that it is a function of the voltage applied and the stress time at that voltage [39]. Longer times and larger voltages cause the relaxation time of the residual charge to increase. This may be the result of charge-trapping states at typical Si/SiO_2 interfaces.

The hysteresis can be measured using the same charge redistribution technique, and has been used to measure the residual polarization in MOS capacitors [39]. The analysis is an extension of the analysis in Section 3.2. It is assumed that the capacitors have some residual polarization Q_R with zero voltage applied in the time frame of interest. Since the calibration cycle does not involve switching and discharging, the charge measured is only the switch injection. During the measurement when C_S is discharged, the charge at the top node due to C_S is not zero, but Q_R. Similarly, when C_R is discharged, the charge at the top node is Q_R assuming the capacitors share the same process qualities. If we make the analogy that the measurement step for the capacitors is a *calibration step involving residual charges*, then the measurement voltage becomes

$$V_{DAC_{meas}+} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V + \frac{-2Q_R}{C_C} \tag{3.18}$$

where the plus subscript indicates a positive reference measurement (assuming that C_R is greater than C_S). Performing the calibration and measurement cycles again, but with the roles of C_R and C_S *reversed*. $V_{DAC_{meas}}$ becomes

$$V_{DAC_{meas}-} = \frac{V_{ref}(C_S - C_R)}{C_C} \pm 4\Delta V + \frac{-2Q_R}{C_C} \tag{3.19}$$

where the minus subscript denotes a negative reference measurement. Adding the two equations yields

$$V_{DAC_{meas}+} + V_{DAC_{meas}-} = \pm 8\Delta V + \frac{-4Q_R}{C_C} \tag{3.20}$$

Since the residual polarization is common-mode to both positive and negative cycles but the capacitive difference is not, the residual polarization can be measured. If desired, it can be subtracted out of equation (3.18) or (3.19) to obtain an accurate capacitive difference measurement.

The above analysis is applicable to both negative and positive V_{ref} so that Q_R may be determined for both negative and positive biases on the capacitors. Reports show that in MOS capacitors with polysilicon top plates and phosphorus-doped bottom plates, the residual polarization is less than 4 ppm [39]. There are no published results for metal-to-poly capacitors used in this thesis, but results compare favorably with [39].

It is important to note that there are two different switching sequences that can be used to measure differences in capacitance. The analysis has concentrated on only one sequence since the other reverses the role of C_R and C_S. However, in an actual sensor system application, the choice of switching sequence is not arbitrary, and one is preferred over the other. The state of the system while A/D conversion is taking place is crucial. If the switching sequence is chosen such that the sense capacitor has a reference voltage across it while the SAR is operating, then any changes in the sense capacitor during conversion may cause errors. The magnitude of error depends on when the change in sense capacitance occurs. The preferred switching sequence is when the sense capacitor is grounded while the SAR is operating. Any changes in C_S result in almost no change in V_x since the the voltage across the sense capacitor is nearly zero during the entire conversion period. The difference in capacitance that is measured is the difference between the reference capacitor (which we assume is not time-varying) and the value of the sense capacitance *just prior to the point where the voltage on the sense capacitor is switched to ground.* Any changes in

capacitance after this point in time do not affect the A/D conversion. For sensor applications where the sense capacitor is time-varying, the negative measurement (as defined in this section) is always preferred. In this thesis, neither capacitor is time-varying so that this is not an issue.

Transistor Hysteresis

When the gate of a MOSFET in a differential input pair is excited with a narrow pulse, a brief change in threshold voltage may result. This is due to charge carriers trapped and released in the oxide, causing a threshold shift. This shift results in a temporary change in offset voltage. If the offset changes in a cycle less than the calibration or measurement cycle, the assumed constancy of the offset is incorrect and the measurement will include an error term that is proportional to the difference in offset voltages. This can be seen by analogy to the non-ideal open-loop case. The virtual grounds are different in the calibration step, introducing an error $\frac{V_{os}}{\delta}$ in the calibration. This is due to the difference in offsets in the two steps. The measurement introduces another difference in offsets so that the measurement will have a term that includes the offsets in all four steps,

$$V_{DAC_{meas}} = \frac{V_{ref}(C_R - C_S)}{C_C} \pm 4\Delta V + \frac{1}{\delta}(V_{os_{0a}} - V_{os_{0b}} + V_{os_2} - V_{os_1}) \qquad (3.21)$$

If the offsets are all equal, then the error term cancels. If

$$V_{os_{0a}} = V_{os_1}$$

$$V_{os_{0b}} = V_{os_2}$$

then there is no error which is exactly the non-ideal open-loop case. The effective offset in steps 0a and 1 is zero since the top node is grounded. Steps 0b and 2 return V_x to V_{os}.

Data from recent measurements [40] show that transistor hysteresis is not apparent if stress times of less than a microsecond are encountered. The data in this thesis are obtained in a cycle time such that glitches at the input of the CMOS op-amp are no more than 100 nanoseconds in width. Thus transistor hysteresis is neglected.

Junction Leakage

A MOSFET has inherently in its structure two pn junctions. These junctions lie in the region between the source and body and drain and body. In normal operation, the body voltage is set so that both pn junctions are always *reverse-biased.* In an NMOS transistor, the body is set at the most *negative* potential and in a PMOS transistor, the body is set at the most *positive* potential. An MOS switch that is turned off can inject charge from the channel and from the reverse-biased pn junction. The channel charge is significant and is estimated in the next chapter. Normal reverse saturation current from a pn junction is typically 10 nA/cm^2 in MOS processes at room temperature. If the area of the MOS switch source region is 100 μm^2, the reverse leakage current is approximately 10 fA. If the switch is open for 100 microseconds, the charge transferred is approximately *6 electrons.* This effect becomes significant only at low clock frequencies and at elevated temperatures. The leakage current approximately doubles for every 10°C rise in temperature [41]. Leakage current introduces an extra charge source in the measurement and can be measured using this technique if the clock frequency is low enough.

Voltage Coefficient of Capacitance

The voltage coefficient of capacitance is defined as the rate of fractional change in C per unit voltage at some dc voltage V:

$$V_{CC} = \frac{1}{C}\frac{dC}{dV}$$

In MOS capacitors, V_{CC} is a decreasing function of doping [42]. Typical values are +20 to +100 ppm/V while poly-to-poly capacitors exhibit +10 to +20 ppm/V [43]. It is much lower for metal-to-poly capacitors [41]. Only two dc voltages are applied across the capacitors in the capacitive measurement scheme. Both capacitors are subjected to the same sequence of voltages so that any capacitance change due to the different applied voltages will track and therefore cancel. Electro-constriction may occur if the dc reference voltage is large and the capacitor gap is small. This causes an error if the sense capacitor structure is compliant but the reference is not. In this thesis, the capacitors are located in the same location and are nearly identical. Electro-constriction is neglected as well as voltage coefficient.

Temperature Coefficient of Capacitance

The temperature coefficient is defined as the fractional change of total capacitance per unit temperature:

$$T_{CC} = \left[\frac{1}{AC_t}\right]\frac{d}{dT}(AC_t)$$

where C_t is the total MOS capacitance per unit area and A is the plate area. In MOS capacitors, T_{CC} can be resolved into three components: thermal expansion of plates, space charge width, and dielectric constant change. The details of these components are complicated. For Al-to-Si capacitors, T_{CC} increases with increasing

doping and is about 21 ppm/°C at doping levels of 10^{19} cm^{-3} [42]. Typically for MOS and double-poly capacitors, the coefficients are in the range of +20 to +50 ppm/°C [43]. To first order, if the sense and reference capacitors are located close to each other, the effect of T_{CC} is eliminated because the two capacitors track each other in temperature.

3.3.3 Noise

Thermal Noise

In an MOS switch that has a channel, the thermal noise power caused by the resistive channel is given by

$$(V_n)^2_{rms} = 4kTR(\Delta f)_n \tag{3.22}$$

where k is Boltzmann's constant, R is the on-resistance of the channel, and $(\Delta f)_n$ is the noise-power bandwidth of the RC circuit formed by the MOS switch and the total capacitance. In the measurement circuit, C is the total capacitance on the node V_x. For a single-pole low-pass circuit,

$$(\Delta f)_n = \frac{1}{4RC} \text{ Hz} \tag{3.23}$$

Substituting (3.23) into (3.22) yields

$$(V_n)^2_{rms} = \frac{kT}{C} \tag{3.24}$$

This noise is sampled on the capacitors when the switch is turned off. It can be shown that an MOS channel can be treated as a noiseless open circuit when turned off [41]. Increasing C can reduce this noise, but increases the parasitic capacitance if the sense and reference capacitors are already determined to be small. This tradeoff was mentioned earlier in Section 3.3.1 and is addressed later in Chapter 5.

Circuit Noise

The noise due to the operational amplifier or comparator is input-referred noise and $1/f$ noise. The $1/f$ noise is not appreciable at the high frequencies of interest so it can be neglected. Typically, the corner frequency for the transition from dominant $1/f$ noise to thermal noise is 10 kHz [41]. It can be shown that the input referred noise of the comparator is on the order of the thermal noise in closed or open-loop [44]. Shot noise is not appreciable since there is no forward-biased pn junction current flowing anywhere in the circuit.

Clock Feedthrough Noise

Overlap capacitances can cause capacitive coupling of input signals to the output. Capacitive coupling of clock noise from S1 and S2 to V_x is attenuated by a capacitive divider so that noise from the clock is minimal. S3, however, contains a gate-to-drain overlap capacitance that couples directly to the sensitive node, but any noise at the gate is attenuated by another capacitive divider and is small at V_x. Since the overlap capacitances are smaller than the total capacitance on the node by factors of 100 or more, any noise on the clock lines can be ignored. The overlap capacitance also stores channel charge that must be taken into account when estimating Q_{S3}.

Proper care in separating the digital and analog supply and data lines is necessary to insure no extraneous introduction of noise to the sensitive node. Substrate and packaging coupling can cause noise if not attended to. These important design considerations are discussed in more detail in Chapter 4.

3.4 Other Charge Injection Sources

In the event of severe radiation or particle bombardment, the charge injection introduced may be random and unpredictable. Shifts in threshold may be permanent or temporary. The offset calibration scheme can be used to calibrate out long-term drift effects or sudden permanent changes in offset. This makes it useful in space applications where cosmic radiation is abundant. If the frequency of change is high, the technique will not eliminate the errors since they are changing at too fast a rate. If the changes are slow, on the order of seconds, frequent calibration can be done to eliminate offset and charge injection errors.

Chapter 4

Capacitive Measurement System Design

4.1 Test Chip Design

To test the theory of the charge redistribution technique on capacitive difference measurements, a test chip is designed and fabricated at MOSIS (MOS Implementation System) using a 3 μm p-well CMOS technology. Its main purpose is to demonstrate difference measurements of femtofarad capacitance that can only be obtained using IC technology. The technique has already been demonstrated at much higher capacitances [35]. An open-loop topology is used.

Silicon structures suitable as capacitive structures can vary from a few femtofarads to several picofarads in capacitance. Structures in use today usually have capacitances on the order of a picofarad or higher. The lower range of capacitance

has not been explored, therefore test capacitances are chosen in the 100 femtofarad range. Two sets of sense and measurement capacitors are considered. Their sizes are determined by unit capacitors C_{unit1} and C_{unit2} that are 100 μm^2 and 400 μm^2 in area respectively. The MOSIS process specifies a metal-to-poly capacitance (C'_{ox-mp}) between 0.035 and 0.05 $fF/\mu m^2$ so that the unit capacitors are 4 and 16 fF respectively if we assume a value of 0.04 for convenience. This value is used throughout the chapter. Exact areas differ slightly from the numbers given, but for calculational convenience, are used in the following analyses. The smaller set of sense and reference capacitors consist of 5 small unit capacitors while the larger set use the larger unit capacitor. The notation for these are

$$C_{small} = C_{R_{small}} = C_{S_{small}} = 5C_{unit1} \approx 20 \text{ fF}$$

$$C_{large} = C_{R_{large}} = C_{S_{large}} = 5C_{unit2} \approx 80 \text{ fF}$$

Three coupling capacitors are used on-chip. When one is not used, it is grounded and therefore contributes to the parasitic capacitance. These capacitors are determined by careful analysis of the charge injection and worst case offsets.

4.2 Charge Injection Estimation

Switch S3 on the test chip is implemented with n-channel MOSFETs. Switches S1 and S2 are a combination of n-channel and p-channel devices. The expression for the channel charge in an n-channel MOSFET is given by [44]:

$$Q_{channel} = -\frac{2}{3}WL_{eff}(V_{gs} - V_T)C'_{ox} - C_{gs0}WV_{gs} \tag{4.1}$$

W = gate length

L_{eff} = $L_{drawn} - 2L_D$, L_D = lateral diffusion

V_{gs} = gate-to-source voltage

V_T = threshold voltage

C'_{ox} = gate oxide capacitance per unit area

C_{gs0} = gate-to-source overlap capacitance per unit length

The first term represents channel charge due to the inversion layer and the second term represents the charge stored under the overlap of gate and source due to the capacitance there. The drain overlap capacitance is ignored since the drain is connected to a low impedance node (ground) and therefore does not contribute any charge to the source. For a given process, SPICE parameters are usually extracted and can be used to find $Q_{channel}$. In worst case, all of the charge in the channel is injected to the sensitive node. For fast gate turn-off, the charge splits equally between source and drain [45],[46],[47]. The charge pumping phenomena due to the capture of channel charges by interface traps is neglected [48]. W/L ratios of 4/3 and 6/5 are used for switch S3 to minimize charge injection. The on-resistance can be calculated from the equation

$$R_{on} = \frac{1}{(\mu_0 C'_{ox})\left(\frac{W}{L}\right)(V_{gs} - V_T)}$$

In SPICE , the parameter $\mu_0 C'_{ox}$ is called the intrinsic transconductance parameter, K_P and contains the parameter μ_0, (surface mobility) and C'_{ox} (gate oxide capacitance per unit area). This parameter varies from vendor to vendor, but is usually in the range 2×10^{-5} to 5×10^{-5}. K_P is given in A/V^2 and μ_0 in cm^2/V-sec. C'_{ox} can either be obtained from the above information or from knowing the oxide thickness, t_{ox}. The MOSFET SPICE parameters show that the on-resistance of the NMOS switch S3 is well below 10 k-Ω for both W/L ratios used in this study. If the switch is used to ground a node with capacitance of 5 pF, then the minimum switching

time allowed assuming a four-time-constant wait is approximately 200 ns or a maximum switching speed of 5 MHz. This is sufficient for most purposes. Switches S1 and S2 are made large to reduce on-resistance. They do not contribute any injected charge to the isolated node so their size can be made arbitrarily large.

The charge in the channel can be calculated from equation (4.1). The SPICE parameter $C_{g s 0}$ is normally given in F/m and is approximately 5×10^{-10}. Threshold voltages normally range from 0.7 to 0.8 V, and L_D is typically 0.3 μm for a 3 μm CMOS process. V_{g_s} is 5 V. This yields a charge injection of approximately -65 fC for the 6/5 switch and -28 fC for the 4/3 switch.

Total Capacitance Requirement

Since in open-loop the calibration voltage is based on charge injection and comparator offset, both must be considered when choosing a coupling capacitor that can keep the DAC within its range. Two different intentionally placed on-chip parasitic capacitances are chosen at 1pF and 4 pF. They are used to test the insensitivity of the technique to parasitic capacitances one to two orders of magnitude larger than the test capacitors. In addition to the intentional parasitic, there is the unintentional but unavoidable parasitic due to the input of a buffer amplifier that connects the sensitive node on-chip to a comparator off-chip. This adds 1 pF so that the total capacitance is either 2 pF or 5 pF, depending on which parasitic is used.

The design parameter becomes C_C since the total capacitance is determined. Three are chosen: 8 fF, 32 fF, and 64 fF. They are chosen based on the following assumptions:

1. Q_{S3} is either -65 fC or -28 fC worst case.

2. V_{os} of the comparator is ±20 mV worst case.

The comparator is a CMOS differential op-amp. Typical random offsets range from ±1–20 mV. Given the total capacitance on the node as 5 pF, the comparator offset as ±20 mV, and the charge injection as -65 fC, the open-loop calibration measurement from equation (3.14) is

$$\begin{aligned} V_{DAC_{cal}} &= \pm 12.5 + 8.13 \text{ V} \quad C_{C3} = 8 \text{ fF} \\ &= \pm 3.13 + 2.03 \text{ V} \quad C_{C2} = 32 \text{ fF} \\ &= \pm 1.56 + 1.02 \text{ V} \quad C_{C1} = 64 \text{ fF} \end{aligned}$$

It is found that nearly all circuits tested can be calibrated with the 32 fF capacitor.

Five independent circuits are placed on one chip. The circuits tested the effect of parasitic capacitance and switch size on the measurement. The sense and reference capacitors are located as close to each other as possible to avoid errors due to voltage and temperature coefficients of capacitance. The exact absolute values of all the capacitors are unknown since C'_{ox-mp} could be not obtained from the vendor. Layout of the capacitors causes $C_{R_{large}}$ to differ in area from $C_{S_{large}}$. This difference is a convenience since a known geometric mismatch is introduced and can be compared with experimental data. A CMOS differential op-amp is used as the comparator. Gain/bandwidth is not an issue so that an optimized design is not needed.

Figure 1 (4-1) and Figure 2 (4-2) show the layout and die photograph of the test chip respectively. The test chips are packaged in a 28 pin ceramic DIP format.

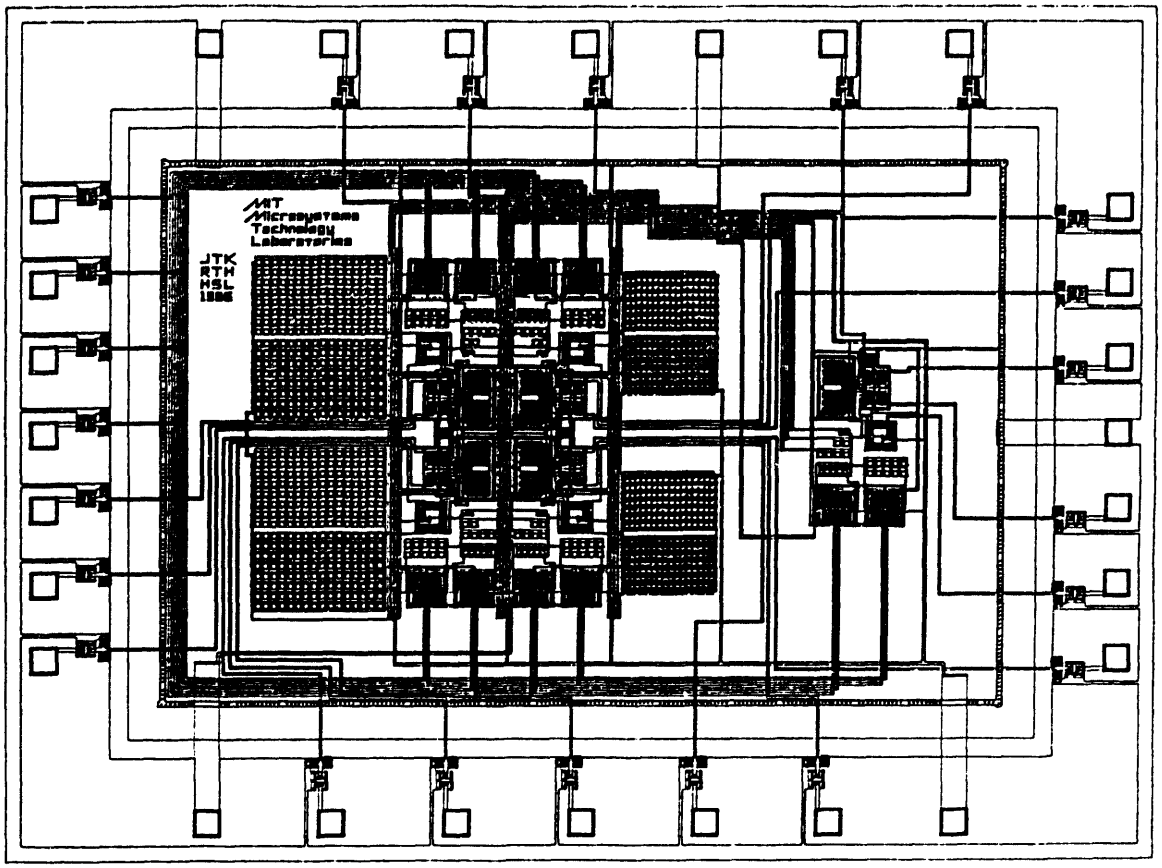

Figure 4.1: Layout of test chip

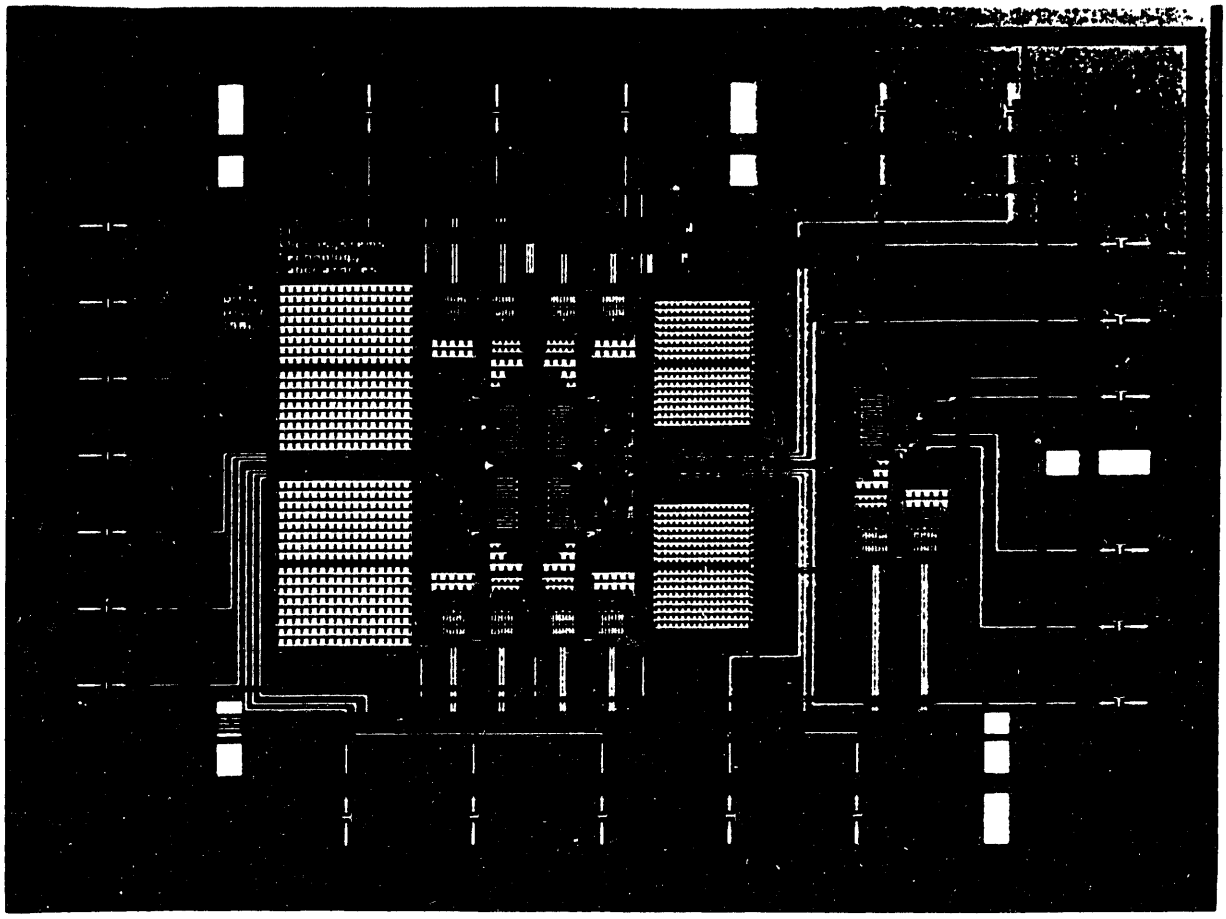

Figure 4.2: Die photograph of test chip

4.3 System Test Equipment

Several digital and analog boards are built to test the test chips. An analog board with copper ground plane is built that houses DIP switches, comparator, and optoisolators. Physical size is kept at a minimum to reduce path lengths and oscillations from the comparator and optoisolators. Power for the analog components is shielded entirely from supply to pin input. Optoisolator power comes from the motherboard which houses the digital control components. The digital supplies are kept isolated from the analog supplies by shielding and distance. For the reference voltage, precision supplies are used at 5.00000 V. All chips are bypassed *at the pin input* with 0.1 pF ceramic capacitors in parallel with 10 μF electrolytics for the digital logic chips and 1000 μF electrolytics for the analog test chip. A 12 bit successive approximation register (SAR) and D/A converter (DAC) are used in the experiment.

All unused pins on the test chip are grounded. Ground loops are avoided when possible, although the copper plane provides excellent conduction paths to ground. The metal tops of the 28 pin DIPs are grounded to prevent external capacitive coupling.

Switching is accomplished using buffered data from an EPROM connected to optoisolators on the analog board. Control comes from an IBM PC XT. An external clock operating at 100 kHz is used in all the measurements. Operating at this frequency minimizes certain errors discussed in Chapter 3. It is possible to control both the reference voltage V_{ref} and the gate voltage V_{gs} on S3 so that several different types of measurements besides capacitive difference can be made.

Chapter 5

Experimental Results

5.1 Capacitive Difference Measurement Data

Three runs using MOSIS are made. Table 1 (5.1) shows the MOSIS information for each run. Test chip Newalpha differs from Delta in switch size in circuit 5. Test chip Xanadu is identical to Delta except it uses different output pads which yield no difference in performance at 100 kHz. Five chips per run are obtained. Since there are 5 circuits on each chip with two sets of sense and reference capacitors for *each* circuit, a large amount of data is obtained. A positive and negative measurement is also made for each set of sense and reference capacitor to test for positive residual polarization (see Section 3.3).

The exact areas and estimated range of capacitance values for all capacitors on chip are shown in Table 2 (5.2). Figure 1 (5.1) shows the positions of the circuits on the test chip while Table 3 (5.3) shows the differences from circuit to circuit and

MOSIS Test Chip Information			
Chip name	Newalpha	Delta	Xanadu
ID number	20843	21293	21722
Project name	cap meas	cap meas	cap meas
Technology	CBPM2	CBPM2	CBPM2
Lambda	1.5 μm	1.5 μm	1.5 μm
Fabrication ID	M68BKA1 (Bette)	M68BKA1 (Bette)	M68CMB1 (Carl)
Mask Vendor	Rockwell	Rockwell	Master Images
Wafer Vendor	Orbit	Orbit	VTI
Packaging Vendor	Pantronix	Pantronix	Halcyon

Table 5.1: MOSIS chip information

Capacitance Areas and Values		
C	Area (μm^2)	Capacitance Range (fF)
$C_{R_{large}}$	2132	74.6–106.6
$C_{S_{large}}$	2120	74.2–106.0
$C_{R_{small}}$	620	21.7–31.0
$C_{S_{small}}$	620	21.7–31.0
C_{C1}	1696	59.4–84.8
C_{C2}	848	29.7–42.4
C_{C3}	248	8.7–12.4
C_{P1}	31744	1111–1587
C_{P2}	108544	3800–5427

Table 5.2: Range of capacitor values

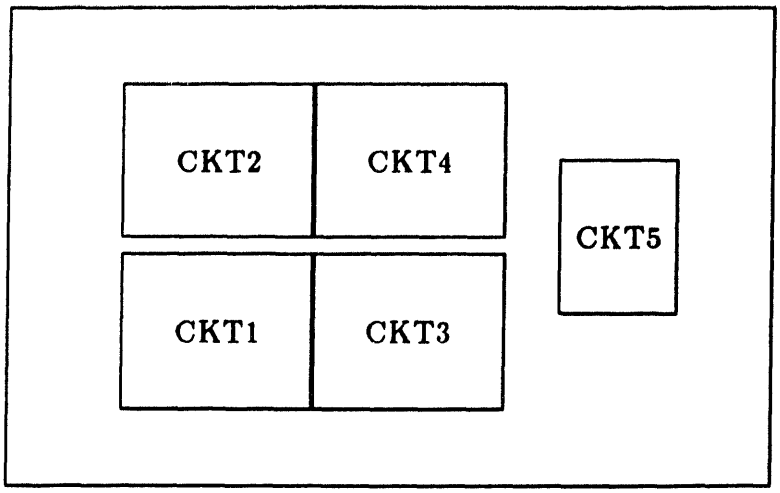

Figure 5.1: Circuit placement on chip

from chip to chip.

The data is organized and presented in tables and graphs. The first set presents data on the effectiveness of the calibration in graph form. The second set of data is classified by chip name and includes measured differences of both large and small capacitor sets and positive and negative measurements. Included in these tables are the resolution, standard deviation of all measurements and residual polarization data. This data typifies a chip from each MOSIS run.

The following graphs show the results of the calibration test. Figure 2 (5.2), Figure 3 (5.3) and Figure 4 (5.4) are graphs of calibration voltage output after cancellation. To measure the success of the calibration technique in eliminating charge injection, a calibration test is used. The calibration voltage is measured 100 times, then averaged. The negative of this value is then applied to the coupling capacitor and the calibration cycle is repeated. Cancellation of the charge injection should result in a DAC output voltage near 0 V. The data for all the chips shows

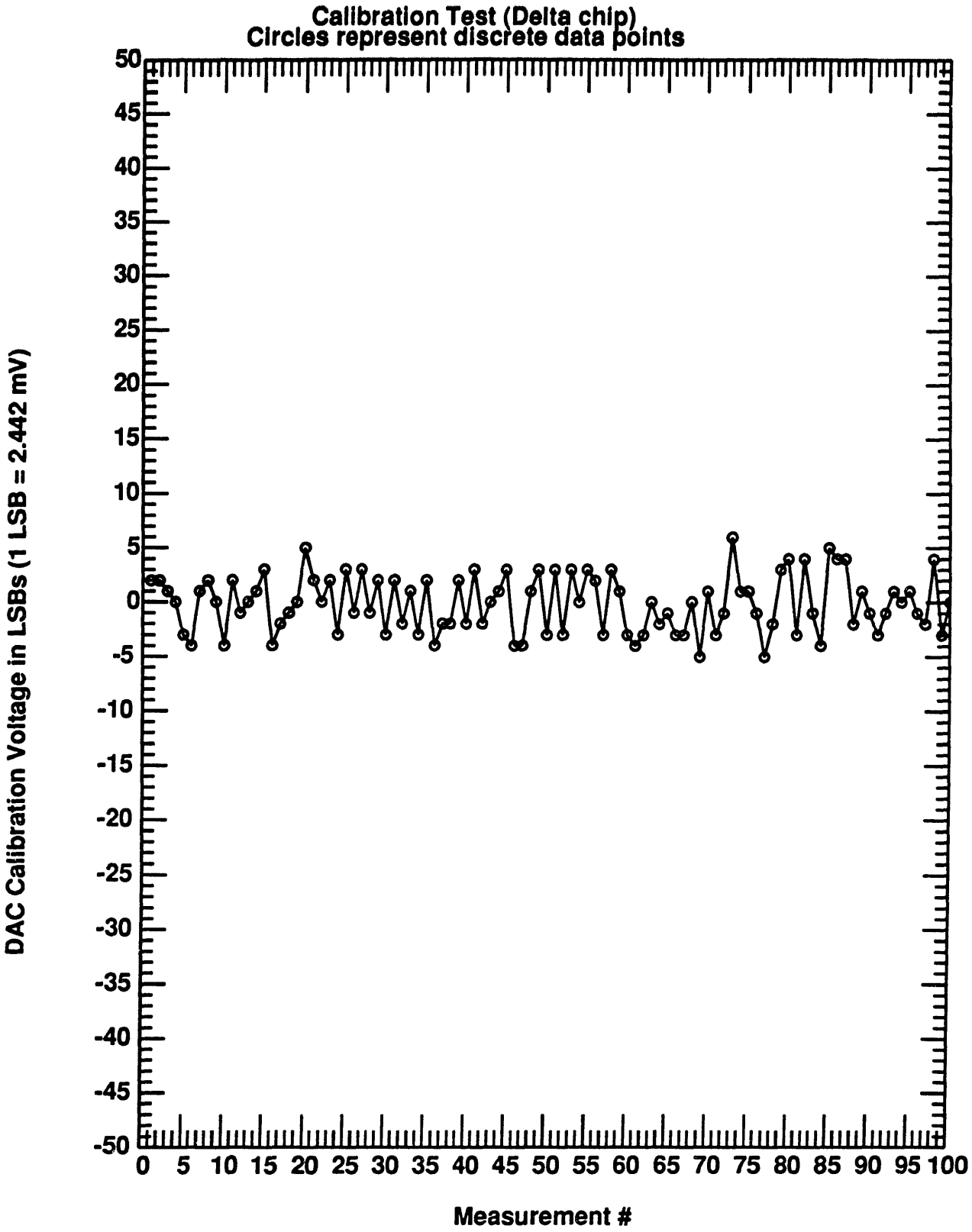

Figure 5.2: Graph of calibration test on Delta chip

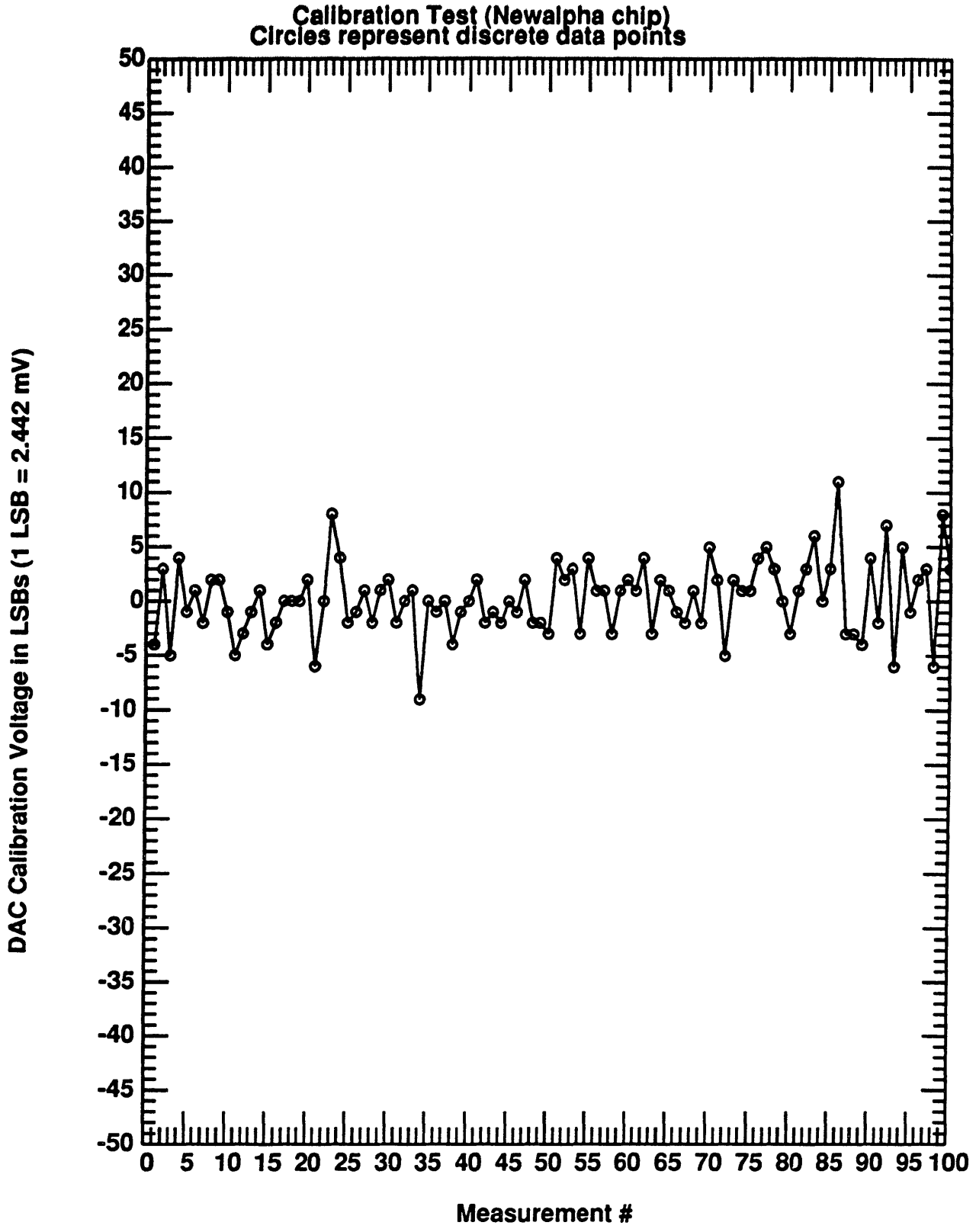

Figure 5.3: Graph of calibration test on Newalpha chip

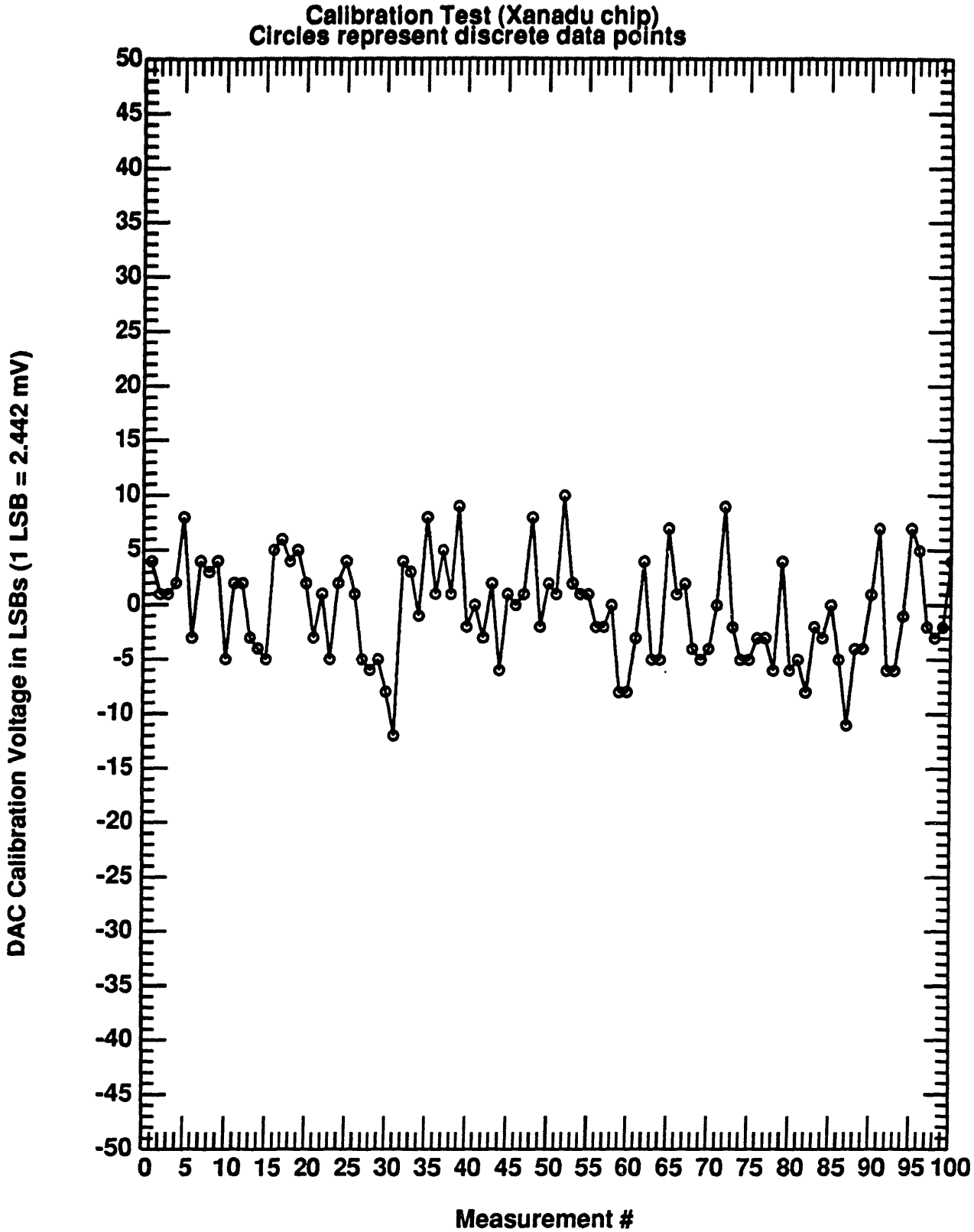

Figure 5.4: Graph of calibration test on Xanadu chip

Test Chip Circuits					
Delta Test Chip	CKT1	CKT2	CKT3	CKT4	CKT5
Intentional parasitic	C_{P2}	C_{P2}	C_{P1}	C_{P1}	0
Buffer amplifier input capacitance	.7 pF	.7 pF	.7 pF	.7 pF	.7 pF
S3 switch size ratio W/L	4/3	6/5	4/3	6/5	6/5
Newalpha Test Chip	CKT1	CKT2	CKT3	CKT4	CKT5
Intentional parasitic	C_{P2}	C_{P2}	C_{P1}	C_{P1}	0
Buffer amplifier input capacitance	.7 pF	.7 pF	.7 pF	.7 pF	.7 pF
S3 switch size ratio W/L	4/3	6/5	4/3	6/5	4/3
Xanadu Test Chip	CKT1	CKT2	CKT3	CKT4	CKT5
Intentional parasitic	C_{P2}	C_{P2}	C_{P1}	C_{P1}	0
Buffer amplifier input capacitance	.7 pF	.7 pF	.7 pF	.7 pF	.7 pF
S3 switch size ratio W/L	4/3	6/5	4/3	6/5	6/5
Total capacitance (All chips)	5.6 pF	5.6 pF	2.3 pF	2.3 pF	1 pF

Table 5.3: Circuit and chip information

that on average, the DAC calibration voltage is less than 1 LSB.

In Table 4 (5.4), Table 5 (5.5) and Table 6 (5.6), the measurement data is presented. Each table summarizes the results for each test chip. For these measurements, the calibration voltage is measured 16 times, then averaged. The measurement cycle uses this value and is run 16 times, then averaged. The results in the tables show averaged values and their standard deviations. From the positive and negative measurements, nearly zero residual polarization is observed. Capacitor hysteresis measurements in the tables are based on the large capacitor measurements in circuit 5. This is due to the low standard deviations in these measurements. Ten positive measurements and ten negative measurements (each averaged 16 times) are used to determine the capacitor hysteresis. Results are added, divided by 20 to determine the average, then divided by 2 to determine the percent hysteresis

contributed by each switching step.

The small capacitors differ by very little, on the order of 0.1–1%. This reaches the limit of minimum resolution. The large capacitors have an average difference of nearly 3% for all chips and runs. Overlap and fringing capacitance causes this difference.

Since the measurements are digitally averaged, system noise effects are reduced. The tables summarize the approximate noise of the system and effects due to the mechanisms described in Chapter 3. Measurement system characteristics are summarized in Table 7 (5.7).

Test Chip Delta											
	CKT1		CKT2		CKT3		CKT4		CKT5		
Parameter Value (fF)	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26
$V_{DAC,ideal}$ (V)	1.44	1.44	-1.11	-1.11	1.85	1.83	2.00	2.01	0.119	0.113
Std. dev. (LSB)	3.13	3.16	2.13	2.52	2.09	2.50	3.13	2.50	2.28	2.00
$V_{DAC+meas}$ (V)	0.415	3.66E-3	0.412	2.76E-2	0.287	7.17E-3	0.318	-4.12E-3	0.258	4.43E-3
Std. dev. (LSB)	3.63	3.38	1.71	3.34	3.14	2.94	2.16	2.81	2.56	2.69
$\frac{\Delta C}{C}$ (%)	3.32	0.100	3.30	0.756	2.30	0.196	2.55	-0.113	2.07	0.121
Std. dev. (%)	0.071	0.23	0.033	0.22	0.061	0.20	0.042	0.19	0.050	0.18
$V_{DAC-meas}$ (V)	-0.418	-2.44E-3	-0.413	-2.53E-2	-0.287	-8.39E-3	-0.319	3.97E-3	-0.257	9.16E-4
Std. dev. (LSB)	2.28	1.63	2.87	1.89	3.00	2.33	1.50	3.27	2.17	1.89
$\frac{\Delta C}{C}$ (%)	-3.34	-6.67E-2	-3.30	-0.693	-2.30	-0.230	-2.55	0.108	-2.05	2.51E-2
Std. dev. (%)	0.045	0.11	0.056	0.13	0.059	0.16	0.029	0.22	0.042	0.13
Cap. hys. (%)	—	—	—	—	—	—	—	—	0.0056	—
kT/C ($(\mu V)_{rms}$)	27		27		42		42		64	
Leakage	Junction leakage error negligible at 100 kHz									
Tran. hys.	Negligible error									
V_{ICC}	Negligible error due to tracking									
T_{ICC}	Negligible error due to tracking									

Table 5.4: Delta chip data

5.2 Charge Injection and Offset Data

Figure 5 (5.5) and Figure 6 (5.6) show the relationship between the DAC calibration voltage and the applied voltage at the gate of S3. It is linear over much of the range. This confirms the form of Q_{S3} as given by equation (4.1). In addition, from these graphs both the offset and the approximate percentage of channel charge injected are roughly determined. In Table 8 (5.8), the computed offset and approximate percentage of channel charge injected are given for each graph. The results agree with reported data [46],[45],[47] on charge splitting for fast gate turn-off. Notice that for both graphs, there is a deviation from linearity from 3 to 3.5 V. This is expected since the channel charge is not linear in gate voltage for lower gate drives. If the method is implemented in the closed-loop topology, an exact measurement of charge can be made. This method of measurement differs from present methods of charge measurement [47],[46] and may be useful in more in-depth studies on channel charge behavior under varying conditions.

5.3 Discussion

In all the data taken (approximately 1 Mbyte), the general trend observed is that the larger parasitic circuits displayed larger standard deviations. This can be explained. A circuit with large parasitic capacitance has a large capacitive divider attenuation factor $\frac{1}{\delta}$. This increases the error in the DAC since the last few bits may have too small an effect on V_x to switch the comparator. A larger C_P causes the sampled thermal noise to decrease, but digital averaging can reduce this by a factor of four (if averaged 16 times). Thus we would expect larger standard deviations with circuits

Test Chip Newalpha										
Parameter	CKT1		CKT2		CKT3		CKT4		CKT5	
Value (fF)	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26
$V_{DAC,cal}$ (V)	2.58	2.59	1.16	1.16	-0.174	-0.170	6.93E-2	7.23E-2	0.260	0.262
Std. dev. (LSB)	1.56	1.33	2.63	2.75	1.53	1.47	2.02	2.11	1.84	2.70
$V_{DAC+max}$ (V)	0.312	1.53E-4	0.612	4.73E-3	8.70E-2	-5.65E-3	0.125	-3.36E-3	7.65E-2	-5.04E-3
Std. dev. (LSB)	1.09	1.58	3.25	3.24	1.80	2.84	2.31	2.16	1.44	2.31
$\frac{\Delta i}{i}$ (%)	4.98	8.34E-3	4.89	0.129	0.696	-0.154	1.00	-9.18E-2	0.612	-0.138
Std. dev. (%)	0.021	0.11	0.063	0.22	0.035	0.19	0.045	0.14	0.028	0.15
$V_{DAC-max}$ (V)	-0.308	-1.37E-3	-0.611	-6.56E-3	-8.52E-2	1.07E-2	-0.127	7.63E-4	-7.02E-2	5.49E-3
Std. dev. (LSB)	1.73	1.34	3.5	2.56	1.95	2.00	1.33	1.59	1.66	2.22
$\frac{\Delta i}{i}$ (%)	-4.94	-7.51E-2	-4.89	-0.180	-0.681	0.292	-1.02	2.08E-2	-0.561	0.150
Std. dev. (%)	0.033	0.089	0.068	0.17	0.038	0.13	0.026	0.11	0.032	0.15
Cap. hys. (%)	—	—	—	—	—	—	—	—	-0.0066	—
kT/C ($(\mu V)_{rms}$)	27		27		42		42		64	
Leakage	Junction leakage error negligible at 100 kHz									
Tran. hys.	Negligible error									
V_{LSB}	Negligible error due to tracking									
T_{LSB}	Negligible error due to tracking									

Table 5.5: Newalpha chip data

Test Chip Xanadu											
Parameter	CKT1		CKT2		CKT3		CKT4		CKT5		
Value (fF)	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26	C_{large} 90	C_{small} 26
$V_{DAC,ideal}$ (V)	3.97	3.97	3.72	3.73	4.69	4.70	3.33	3.33	-3.30E-2	-4.58E-2
Std. dev. (LSB)	4.75	3.05	3.44	3.27	3.25	3.13	3.41	1.61	1.88	3.56
$V_{DAC+,meas}$ (V)	0.495	2.01E-2	0.555	1.89E-2	0.289	1.34E-2	0.334	1.95E-2	0.242	1.01E-2
Std. dev. (LSB)	3.69	4.19	4.38	2.44	2.81	4.38	2.58	2.63	2.23	2.63
$\frac{\Delta C}{C}$ (%)	3.96	0.551	4.44	0.518	2.31	0.367	2.68	0.534	1.94	0.276
Std. dev. (%)	0.072	0.28	0.086	0.16	0.055	0.29	0.050	0.18	0.044	0.18
$V_{DAC-,meas}$ (V)	-0.484	-2.44E-2	-0.545	-1.40E-2	-0.288	-1.18E-2	-0.337	-2.06E-2	-0.241	-8.09E-3
Std. dev. (LSB)	4.75	4.25	2.88	3.78	2.88	3.97	3.77	3.05	2.50	2.96
$\frac{\Delta C}{C}$ (%)	-3.87	-0.668	-4.36	-0.384	-2.31	-0.321	-2.69	-0.564	-1.93	-0.221
Std. dev. (%)	0.093	0.28	0.056	0.25	0.056	0.27	0.074	0.20	0.049	0.20
Cap. hys. (%)	—	—	—	—	—	—	—	—	0.0021	—
kT/C ($(\mu V)_{rms}$)	27		27		42		42		64	
Leakage	Junction leakage error negligible at 100 kHz									
Tran. hys.	Negligible error									
V_{OS}	Negligible error due to tracking									
T_{OS}	Negligible error due to tracking									

Table 5.6: Xanadu chip data

Measurement System Characteristics	
Switching speed	100 kHz
Sucessive Approximation Register	12-bit
Digitial-to-Analog Converter	12-bit
1 LSB	2.44 mV
Conversion speed	120 μsec
Positive analog supply	5 V
Negative analog supply	-5 V
Reference Voltage V_{ref}	+5.00000 V
Temperature	$\approx$ 300°K

Table 5.7: System measurement parameters

Extracted constants from Figs 5.6 and 5.7		
Parameter	Offset (mV)	% Channel charge injected
Fig. 5.6 data	2.08	76.0
Fig. 5.7 data	-14.28	55.6

Table 5.8: Offset and channel charge constants

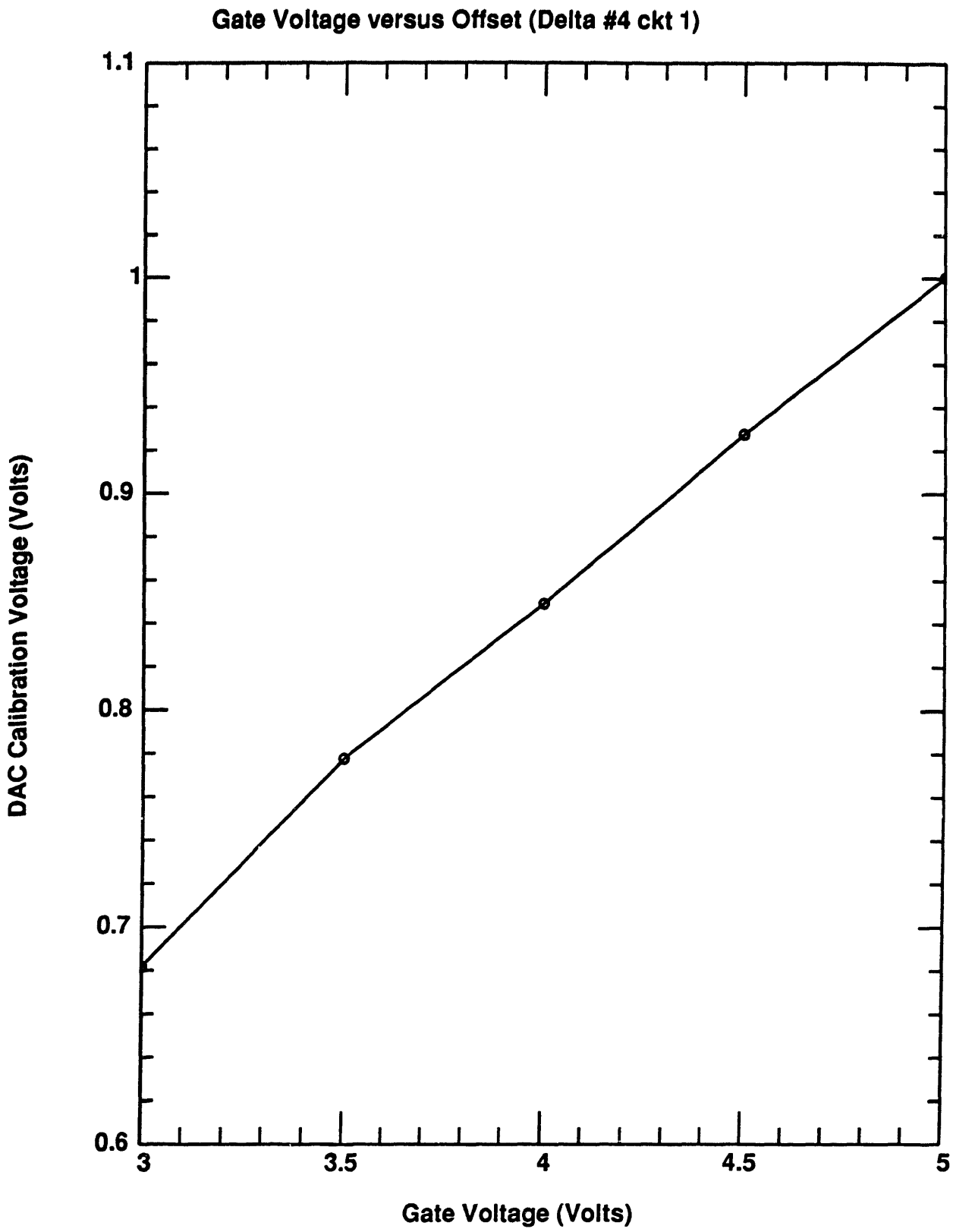

Figure 5.5: Calibration voltage as a function of S3 gate voltage for Delta chip 4 ckt 1

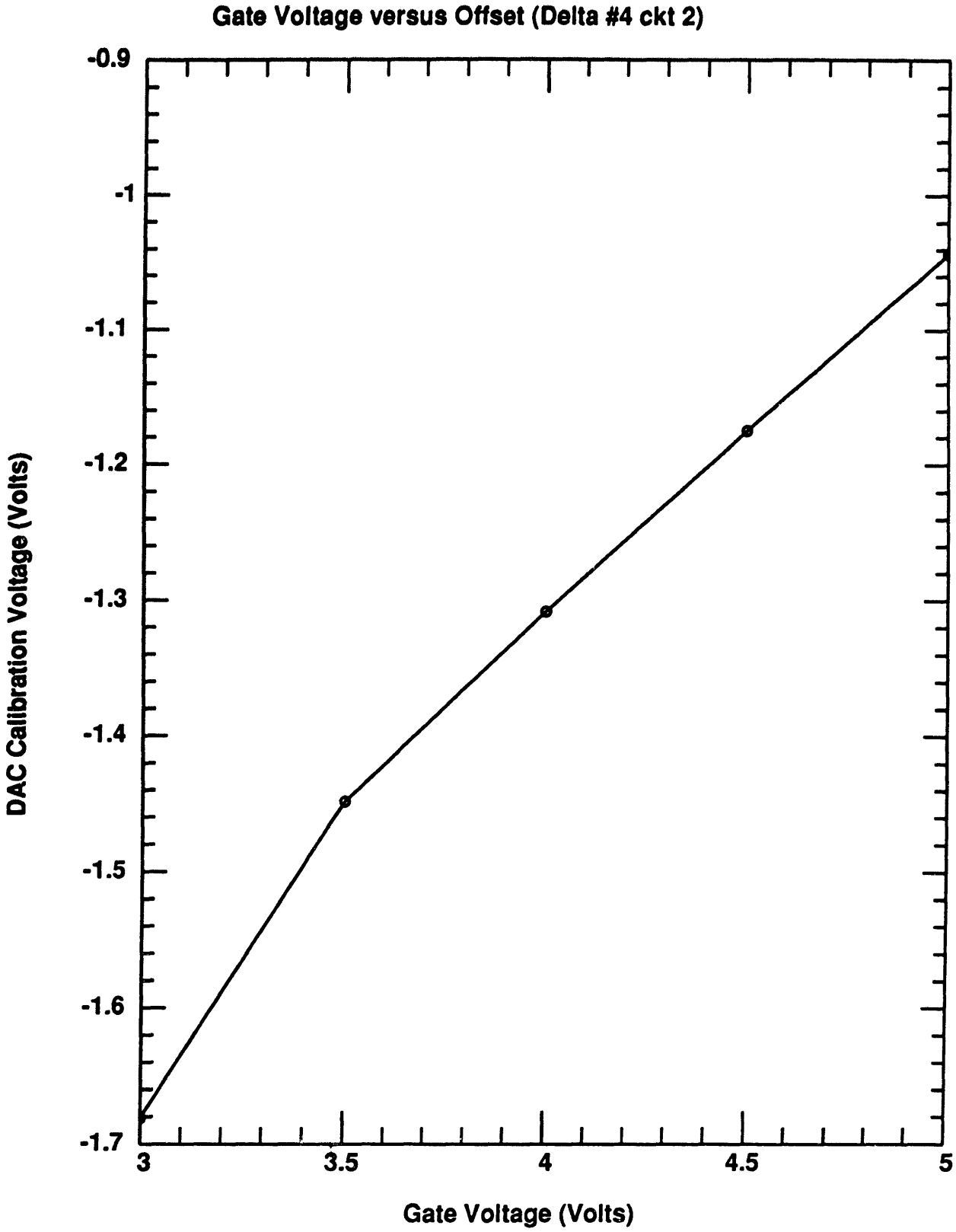

Figure 5.6: Calibration voltage as a function of S3 gate voltage for Delta chip 4 ckt 2

that have a small δ. Recall from equation (3.11) that

$$\delta = \frac{C_C}{C_{total}}$$

where C_{total} is the total capacitance on the sensitive node V_x. One way to increase δ is to increase C_C. In the measurement, several chips are calibrated with a 64 fF coupling capacitor rather than with a 32 fF coupling capacitor. All the voltage measurements decrease by a factor of two as expected. The standard deviation also decreases by a factor of two. However, the percent mismatch error is proportional to C_C and to the standard deviation (or quantization error of the DAC, whichever is larger). Thus the one-half reduction cancels out. The coupling capacitor should be chosen such that the calibration is within the dynamic range of the DAC, and to increase the dynamic range of the final measurement while keeping the capacitive attenuation factor from becoming too large.

There is an inherent error in the DAC so that the average rms error in the final measurement is ± 1 LSB, assuming that in the previous analysis, $\pm\Delta V$ is $\pm\frac{1}{2}$LSB. This error occurs regardless of the value of δ. If δ is so small that the quantization error of the DAC reflects a change at V_x that is smaller than the resolution of the on-chip comparator, then the effective quantization error is larger than $\pm\frac{1}{2}$LSB. In this study, the kT/C noise is not sufficiently large enough at small capacitances to effect the resolution of the comparator. Thus the main source of error is due to a small δ and incomplete cancellation of the sampled noise. The standard deviation for $\Delta C/C$ is obtained by multiplication of the standard deviation of the measurement by the ratio

$$\frac{1}{V_{ref}}\left[\frac{C_C}{C}\right]$$

The standard deviation is approximately the same for the measurement of the small and large capacitors. This agrees with the above argument on the δ dependence

only. But since the ratio of the capacitors in the above equation is different for the two measurements, the relative error in the measurement of the smaller capacitors is larger. The total number of electrons represented by either measurement error, however, is the same as we would expect since the measurement system is the same. Digital averaging can substantially reduce noise errors and DAC quantization errors but at a cost of increased time.

Chapter 6

Conclusions

The charge redistribution technique is highly suitable for sensor applications. Within the method is a powerful way of reducing circuit errors: the offset calibration technique. The charge redistribution technique measures capacitive differences which can be applied directly to sensor design. The capacitive sensor is preferable to the piezoresistive sensor in many aspects so that the scheme is ideally suited for ultrasensitive and ultraminiature silicon sensor designs. Pressure resolution and sensitivity for a capacitive sensor is directly proportional to $\Delta C/C$ so that the sensor becomes heavily read-out dependent. The scaling limit for capacitive pressure sensors appears to be determined by circuit resolution whereas the piezoresistive sensor is determined by offsets and stress averaging. [49].

6.1 Circuitry & Sensor Interfacing Issues

The pressure sensitivity of a capacitive sensor is given by [10],

$$S_{cap} = \frac{\Delta C}{C_0 P} = 0.0625 \frac{1-\nu^2}{E} \left[\frac{a^4}{h^3 d}\right]$$

C_0 = zero-pressure capacitance

P = applied pressure

ν = Poisson's ratio

E = Young'modulus

a, h, d = diaphragm radius, thickness, plate separation

The resolution depends on noise in the sensor and read-out circuitry. Several expressions have been reported but all are dependent on read-out circuitry [10],[50]. For circuit resolution [10],

$$\text{Resolution} \propto \Delta C_{min} \frac{h^3 d^2}{a^6}$$

The main sources of noise in capacitive sensors are circuit dominated. Brownian noise caused by gas molecules impinging on the diaphragm surface has been calculated at below 10^{-3} μmHg for most practical cases and is considered negligible compared with other noise sources [49]. Electrostatic pressure variations due to the measurement system also cause measurement errors. If the applied voltage is large, electrostatic forces can change the plate separation and change the capacitance. For practical voltages and plate separations, the pressure is less than 1 mmHg for frequencies remote from the diaphragm resonance frequency [49]. From the available data on capacitive silicon sensors, it appears that pressure sensors capable of 1 μmHg pressure resolution are possible assuming a minimum resolvable input of 0.1 fF and a minimum resolvable voltage of 0.5 μV [49].

6.2 Comparison of Capacitance Measurement Techniques

In [10], Wise states that the theoretical limit in measuring capacitance difference is 0.1 fF with a 3 V reference voltage (equivalent to a detection of 1875 electrons). The data in Chapter 5 shows that the minimum resolvable *difference* for the 90 fF capacitors is nearly 0.045 fF in the presence of parasitic capacitances an order of magnitude *larger*. It becomes increasingly difficult to achieve this precision with smaller sense and reference capacitors as is shown in Tables 5.5–5.7. The error in the measurement becomes as large as the measured difference. The detection of 1000 or less electrons is certainly possible with this technique.

For a comparison, Table 1 (6.1) and Table 2 (6.2) repeat results presented in [49]. An example of an ultraminiature and ultrasensitive capacitive pressure sensor are presented. Following these tables is another table (Table 3 (6.3)) similar to that presented in [50]. A comparison of minimum resolvable input is made based on the sample data given in [49]. Added to that table are the results of this work as a comparison.

This thesis demonstrates a technique that can measure capacitive differences within a resolution of 0.05 fF on capacitors in the 20 to 100 fF range in the presence of parasitic capacitances nearly 100 times larger. Digital averaging can increase resolution, but increases measurement time. The technique is robust and compatible with IC integration and microprocessor interfacing. This makes it ideally suited for readout in sensor systems.

Ultraminiature Capacitive Sensor				
	A1	A2	A3	A4
Diaphragm Length, 2a (μm)	300	200	100	50
Diaphragm Thickness h (μm)	3	2	1	0.5
Plate Separation d (μm)	1.5	1.0	0.5	0.5
Zero-pressure Capacitance C_0 (pF)	0.53	0.35	0.18	0.044
Pressure Sensitivity (ppm/mmHg)	770	770	770	390
Pressure Range (mmHg)	440	440	440	570
Brownian Noise[1] (mmHg)	$< 10^{-6}$	$< 10^{-6}$	$< 10^{-6}$	$< 10^{-6}$
Broadband kT/C Noise[2] (mmHg)	0.025	0.032	0.049	0.29
Circuit Noise[3] (mmHg)	0.24	0.36	0.73	5.8
Electrostatic Pressure Offset[2] (mmHg)	0.37	0.83	3.3	3.3

1. 100 Hz bandwidth, 760 mmHg on both sides of diaphragm.
2. Capacitor voltage is 5 V dc, stray parasitic capacitance is 0.1 pF in all cases.
3. Minimum resolvable capacitance is 0.1 fF.

Table 6.1: Theoretical performance of the ultraminiature capacitive sensor (from [49])

Ultrasensitive Capacitive Sensor				
	C1	C2	C3	C4
Diaphragm Length, 2a (μm)	1000	1000	1000	1000
Diaphragm Thickness h (μm)	1	1	0.5	0.5
Plate Separation d (μm)	10	5	5	2
Zero-pressure Capacitance C_0 (pF)	0.89	1.8	1.8	4.4
Pressure Sensitivity (ppm/mmHg)	390	770	6200	15000
Pressure Range (mmHg)	12000	4200	2000	140
Brownian Noise[1] (mmHg)	$< 3 \times 10^{-6}$	$< 3 \times 10^{-6}$	$< 3 \times 10^{-6}$	$< 3 \times 10^{-6}$
Broadband kT/C Noise[2] (mmHg)	0.037	0.013	0.0016	0.0015
Circuit Noise[3] (mmHg)	0.29	0.073	0.0091	0.0015
Electrostatic Pressure Offset[2] (mmHg)	8.3	33	33	210

1. 100 Hz bandwidth, 50 μmHg on both sides of diaphragm.
2. Capacitor voltage is 5 V dc, stray parasitic capacitance is 0.1 pF in all cases.
3. Minimum resolvable capacitance is 0.1 fF.

Table 6.2: Theoretical performance of the ultrasensitive capacitive sensor (from [49])

Minimum Resolvable Input[1] (mmHg)		
Sensing Method	Ultraminiature Cap (A1)	Ultrasensitive Cap (B1)
RC Oscillator	0.125	0.190
Current Controlled Oscillator[2]	0.638	0.973
Charge Technique[3]	0.122	0.144

1. 5 V dc bias is used.
2. Depends on circuit configuration (calculation based on [49] and [50]).
3. ΔC_{min} assumed to be 0.05 fF. Averaging can reduce the noise significantly. Minimum resolution of hundreds of electrons is possible so that ΔC_{min} may be much lower.

Table 6.3: Comparison of sensing techniques (adapted from [50])

Appendix A

Generality of Charge Redistribution

A.1 General Applications

The charge redistribution technique is completely general and need not be associated with a particular switching scheme or set of reference voltages. Its application is also completely general in the sense that the difference in capacitance measured could be attributed to a change in three variables rather than only one. A change in dielectric constant, area of capacitor, or capacitor gap, or any combination of the three can cause a capacitance change. This is seen in the experiments. A ten percent mismatch is detected in one of the circuits that had no apparent area difference in the sense and reference capacitors. Since they are spaced close to each other, oxide thickness change is ruled out. Therefore the only reasonable cause for this large difference is variation in oxide composition which would yield a change in

dielectric constant and hence a change in capacitance.

This thesis focuses on the charge redistribution technique and its application to sensing pressure. Pressure detection is an immediate and obvious vehicle for this technique because of its importance and economic significance. It should be stressed that other parameters other than pressure can be measured, as long as they manifest themselves as a change in *capacitance*.

A change in capacitance can manifest itself as a charge difference if an appropriate sequence of voltages are applied to the capacitors of interest. This charge difference can be detected as a voltage and measured. This is the essence of the charge redistribution technique. If this charge can be made such that it is *proportional to the difference of two capacitances*, then a change in capacitance between two capacitors can be detected. In this thesis, two switching sequences are presented, one of which is preferable due to a particular application. It is possible to construct *alternate* sequences consisting of different voltages and different switching steps. All that is required is that the final charge at V_x is proportional to the capacitance difference of C_R and C_S. Thus the voltage measured at V_x is proportional to the capacitive difference.

The offset calibration technique is also very general. Any voltage can be thought of as an *offset* voltage depending entirely on the meaning of the voltage in a certain application. Since the charge injection from switch S3 results in a charge at V_x that is not proportional to the capacitance difference, the voltage it generates at V_x is considered an offset voltage. This voltage can be measured and subtracted from subsequent measurements either within the system (by applying the negative of the offset voltage to the coupling capacitor as is done in the previous analysis) or by subtraction of the digital readout by a microprocessor. Errors caused by

other charge sources can be separately measured and taken into account in the final measurement. Any voltage measured can be thought of as an offset voltage, depending on the application.

As an example, suppose that the parameter of interest happens to be the mismatch of capacitors on a chip. One of the errors involved is the charge from S3 that is *not* proportional to the difference in capacitance of the sense and reference capacitors. To independently measure this error, a switching sequence is devised such that the charge contribution from the difference of the two capacitors is zero. This can be accomplished by not changing the switching sequence before and after S3 is opened. Once this error is measured, it can be subtracted out of the measurement cycle. Furthermore, assume that with the same system, an external stimulus is applied such that the change in capacitance is also due to a *dielectric change.* Also assume that the change caused only by the external stimulus is to be detected. There are now three sources of charge: the charge injection, the charge due to the initial mismatch of the capacitors (with stimulus absent), and the charge due to the change in dielectric constant with stimulus applied. The first two can be independently measured. The two voltages can be subtracted out of the final measurement, yielding only the voltage due to the dielectric change. Thus the first two voltage measurements can be thought of as an offset voltage, and the remaining voltage as the measurement voltage. As long as the error sources can be independently isolated and measured, the offset calibration technique can eliminate their effect in subsequent calculations.

A.2 Alternate Switching Sequences

The switching sequence can be generalized by considering different voltages applied to the capacitors. In the analysis, the switching sequence has been completely generalized. Referring to Figure 1 (A.1) and Figure 2 (A.2), the voltages are

V_P = voltage at bottom plate of C_P

V_{Rn} = voltage at bottom plate of C_R in Step n

V_{Sn} = voltage at bottom plate of C_S in Step n

$V_{DAC_{val}}$ = voltage applied to C_C

V_+ = voltage reference at positive input terminal

V_x = voltage at the sensitive node

V_{os} = offset voltage of the amplifier

In step 1, S3 is closed and the specified voltages are applied. It is assumed that V_+ and V_P never change. With the feedback loop closed, V_x is forced to $V_+ + V_{os}$. In this analysis, the quantization error of the DAC can be easily handled as noted in the previous analyses. It is neglected here, and can be added later with no loss of generality. In step 1, the charge on the top node becomes

$$\begin{aligned} Q_1 &= (V_+ + V_{os} - V_P)C_P + (V_+ + V_{os} - V_{R1})C_R + \\ &\quad (V_+ + V_{os} - V_{S1})C_S + (V_+ + V_{os} - V_{DAC_{val}})C_C \end{aligned}$$

In step 2, the switch is opened and the SAR/DAC feedback loop forces V_x back to $V_+ + V_{os}$. The expression for the charge at the top node becomes

$$\begin{aligned} Q_2 &= (V_+ + V_{os} - V_P)C_P + (V_+ + V_{os} - V_{R2})C_R + \\ &\quad (V_+ + V_{os} - V_{S2})C_S + (V_+ + V_{os} - V_{DAC_{meas}})C_C \end{aligned}$$

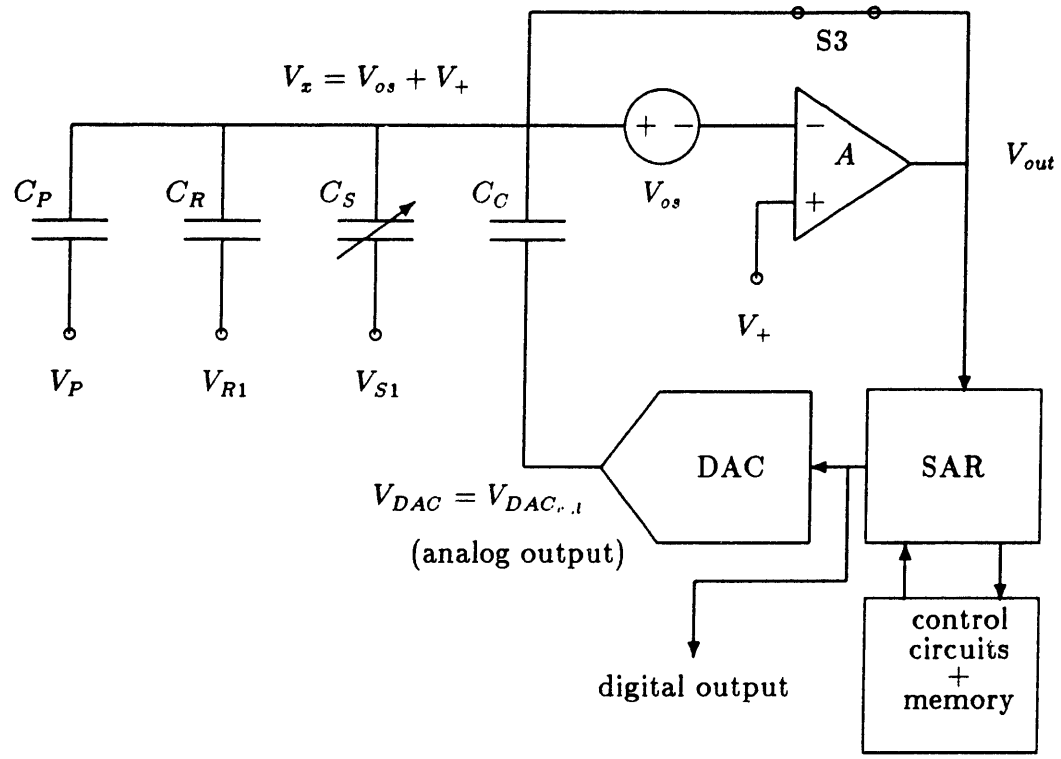

Figure A.1: Generalized Switching Step 1

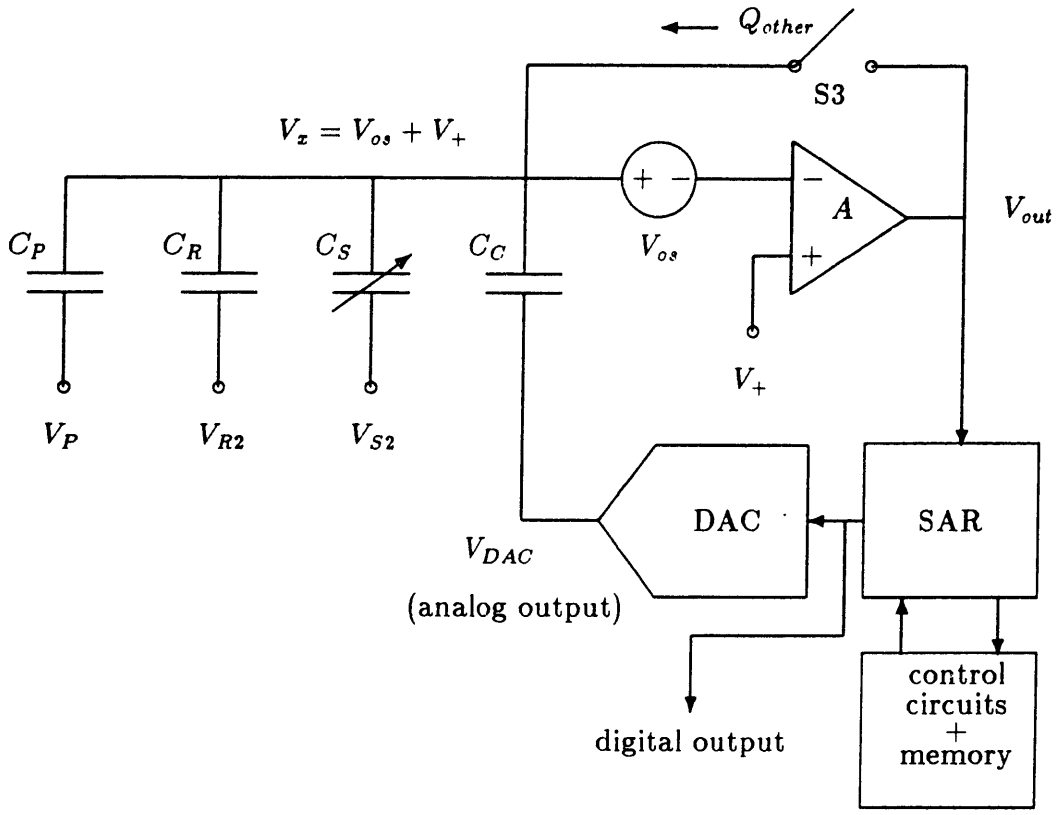

Figure A.2: Generalized Switching Step 2

If additional charge Q_{other} other than from the capacitors is to be taken into account (such as MOS switch charge injection or residual polarization), then by charge conservation,

$$Q_1 + Q_{other} = Q_2$$

It is easily seen that all terms involving C_P, V_{os}, and V_+ *cancel.* Solving for $V_{DAC_{meas}}$ yields

$$V_{DAC_{meas}} = \frac{(V_{R1} - V_{R2})C_R + (V_{S1} - V_{S2})C_S}{C_C} + V_{DAC_{cal}} + \frac{-Q_{other}}{C_C} \qquad \text{(A.1)}$$

This is the general form of the measurement. If DAC error is to be included, then the worst case measurement is

$$V_{DAC_{meas}} = \frac{(V_{R1} - V_{R2})C_R + (V_{S1} - V_{S2})C_S}{C_C} + V_{DAC_{cal}} + \frac{-Q_{other}}{C_C} \pm 4\Delta V \qquad \text{(A.2)}$$

as noted in the previous analyses. If the difference in capacitance between C_R and C_S is desired, then appropriate choices of voltages can be chosen. To eliminate the effect of Q_{other}, $V_{DAC_{cal}}$ must be chosen to equal Q_{other}/C_C. But a priori we do not know Q_{other}. But from equation (A.1), if $V_{DAC_{cal}}$ is set to zero, $V_{R1} = V_{R2}$, and $V_{S1} = V_{S2}$, then we can measure the value $-Q_{other}/C_C$. Setting $V_{DAC_{cal}}$ to the *negative* of this value and choosing appropriate values of V_{R1},V_{R2},V_{S1}, and V_{S2}, equation (A.1) yields a voltage proportional to the difference of C_R and C_S. In fact, $V_{DAC_{cal}}$ can be set to any value. If it is set equal to the negative of the value obtained by measuring the charge injection plus the capacitive mismatch, then cancellation can result, and the measured voltage will be zero! This result is obvious from the equation. If we can independently measure the terms in equation (A.1), then they can each be canceled by adjusting the value of $V_{DAC_{cal}}$. All or some of the terms can be canceled by changing $V_{DAC_{cal}}$.

Equations (3.18) and (3.19) can easily be derived from the general form of equation (A.1). For the measured DAC voltage to be proportional to the difference in

Switching Sequences				
Sequence number	V_{R1}	V_{S1}	V_{R2}	V_{S2}
1	0	V_{ref}	V_{ref}	0
2	0	0	V_{ref}	$-V_{ref}$
3	0	0	$-V_{ref}$	V_{ref}
4	0	$-V_{ref}$	$-V_{ref}$	0
5	V_{ref}	0	0	V_{ref}
6	V_{ref}	$-V_{ref}$	0	0
7	$-V_{ref}$	V_{ref}	0	0
8	$-V_{ref}$	0	0	$-V_{ref}$
9	V_{ref}	$-V_{ref}$	$-V_{ref}$	V_{ref}
10	$-V_{ref}$	V_{ref}	V_{ref}	$-V_{ref}$

Table A.1: Alternate switching sequences

C_R and C_S, the following relation between the applied voltages must be true:

$$(V_{R1} - V_{R2}) = -(V_{S1} - V_{S2}) \neq 0 \tag{A.3}$$

Given that the only voltages available are $\pm V_{ref}$ and 0, the total possible number of switching sequences is ten. Table 1 (A.1) shows different values of $V_{R1,2}$ and $V_{S1,2}$ so that a difference in capacitance can be measured. Notice that sequences 1–8 yield the same form as equations (3.18) and (3.19). Sequences 9 and 10 have an extra constant of 2 since both $\pm V_{ref}$ are used throughout the steps. Each sequence has a dual so that residual polarization can be measured. In Table A.1, the dual sequences are (1,5), (2,6), (3,7), (4,8) and (9,10).

A.3 Fundamental Limitations

In the present algorithm, the fundamental limitation is the sampled noise from the switch S3. This noise manifests itself as a random variation in charge injection

to the sensitive node. The calibration test proved that this noise is random in nature since averaging nearly eliminates it. In the algorithm, the charge injection is measured, then canceled assuming that it is the same in the next sampling. Due to noise, it is not identical, so that some error is introduced. However, since the noise is random in nature, on average the error caused by the statistical variation of charge injection is zero. Comparator noise is a factor, but with sufficient power, a large g_m can yield very low noise and not be the dominant factor.

A slight modification of the algorithm can yield similar results *without averaging.* Averaging is required because the exact value of the injected charge is unknown *during the measurement cycle.* For each calibration cycle, the charge injection measured is exact, however. It includes the sampled kT/C noise of the system. There is no error in the measurement if the calibration step is accomplished *during* the measurement cycle because the charge measured is exactly the charge caused by the injection in the measurement. Referring again to Figures A.1 and A.2, the modified sequence is

Step 1

- Close switch S3 so that $V_x = V_{os}$
- Set S1 to V_{R1}
- Set S2 to V_{S1}
- Set V_{DAC} to GND

In all the analyses done so far, we assume that the charge injected when S3 is opened is the same *every time the switch is opened.* The kT/C noise prevents

this assumption from being true, and there is an error since the charge cannot be exactly determined during the measurement cycle. But during the calibration cycle, the charge is exactly known. Thus if the two steps are *merged*, then the charge can be exactly canceled. The next steps are

Step 2

- Open switch S3
- initialize SAR/DAC

These steps are identical to the calibration cycle steps 0A and 0B mentioned previously. The offset is measured and stored in memory as before.

Step 3

- Set S1 to V_{R2}
- Set S2 to V_{S2}
- Initialize SAR/DAC again

Instead of closing S3, opening it and canceling the charge injection by applying an offset voltage to the coupling capacitor C_C similar to the previous algorithm, the switch S3 is never closed and the measurement cycle is merged into the calibration cycle. The DAC measures a voltage $V_{DAC_{meas}}$ identical to equation (A.2). This includes a voltage due to the capacitive difference and a voltage due to other injected

charge sources (kT/C noise included). But Q_{other} has already been measured in step 2, and it is exactly this same charge that gives rise to the term in equation (A.2). The offset voltage measured earlier can be subtracted out *digitally* from the final measurement rather than subtracted in the analog domain. This modification in the algorithm cancels out the error due to noise. The disadvantage is that it has doubled the time for a measurement. But it is still much shorter than averaging and still short enough to avoid junction leakage errors. The number of electrons that can be detected is limited by the noise of the comparator, the parasitic capacitance, the accuracy of the reference voltages, the DAC quantization error, and the speed of the measurement. For realistic values of these parameters, the minimum resolution is on the order of *tens of electrons or less without averaging.* Since all charge sources and sinks must be taken into account for an accurate measurement, the practical resolution of this technique is limited by the effects of unknown sources or sinks of charge and DAC quantization error.

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