Development of Three-dimensional Passive Components for Power Electronics

by

Pádraig J. Cantillon-Murphy

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

As component and power densities have increased, printed circuit boards (PCBs) have taken on additional functionality including heatsinking and forming constituent parts of electrical components. PCBs are not well suited to these tasks. A novel fabrication method is proposed to develop an enhanced circuit board fabrication approach which overcomes this problem. This method uses a photoresistive scaffold and subsequent metallization to realize the proposed structures. These structures are suitable as heatsinks, inductor windings, busbars and EMI shields among other applications.

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Electrical Engineering and Computer Science

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I would like to thank a number of people without whom this achievement would not have been possible. Firstly, to Dave for investing so much time and effort in me over the past two years, for being patient throughout and for always encouraging me to go the extra yard. To Professor Kassakian; for affording me the opportunity to work at his laboratory, for always making me feel welcome and for having the common touch.

Thank you to all the lads at L.E.E.S.; for making me feel at home, never getting mad, always helping me out and never letting me down. Sláinte agus póg mo thóin! Special mention should go to Josh, who was especially tolerant of my stupdity. To Vivian, for everything only Vivian can do and to Wayne for the help and advice. A special acknowledgement is due to Kurt Broderick for his moments of inspiration.

I want to thank Aubs, (for teaching me how to dream) Ciar and Gobs, Maur and Bill, and Anne and Paddy, (for all the support you give, in many, many ways) and, in particular, Mamie...because you'll never let my feet get off the ground!

Finally Éamonn and Micheál cause you're the greatest friends a brother could wish for; and Dad and Mam; for everything. You're the greatest!

And finally, finally to St. Teresa of Avila because:

"Patience obtains all"

"Despite the uncertainties and the labor which every attempt to interpret reality entails – not only in the sciences, but also in philosophy and theology – the paths of discovery are always paths towards truth. And every seeker after truth, whether aware of it or not, is following a path which ultimately leads to God, who is Truth itself."

Joannes Paulus PP. II

His Holiness Pope John Paul II.
Address to the Pontifical Academy of Sciences.
November 8, 2004.

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Chapter 1

Introduction

As component and power densities have increased, printed circuit boards (PCBs) have taken on additional functionality. This includes acting as the principal means of conducting heat away from electronic components (heatsinking), carrying high power and high frequency signals (busbars and transmission lines) and forming constituent parts of electrical components (e.g. forming printed windings for "planar" inductors and transformers). Conventional circuit board technology is not well suited for realizing this additional functionality, and is increasingly imposing limitations on the achievable size and performance of electronic equipment.

In order to better understand the work carried out here, it is useful to explore the standard industry approach to PCB fabrication. A PCB comprises a sheet of insulating material (typically laminate) with a thin layer of copper foil (typically between 18 and 180 μm thick) bonded to one or both sides and etched to form a desired interconnect pattern [1, 2]. Connections between the two sides are formed by drilling holes in the board and plating them through. Multi-layer boards are fabricated by stacking up multiple board layers and connecting them appropriately. The resulting sandwich structure of thin copper layers and laminate is highly effective for providing medium-density interconnections among components at low cost (though cost tends to rise rapidly as the number of layers is increased).

While the structure of conventional PCBs is effective for mounting and interconnecting circuit components, other functions important in modern electronic circuits are not well served by this structure. For example, the PCB structure is not very effective at transferring heat from components to the environment [1], necessitating the use of large circuit board areas and/or mounted heatsinks to meet thermal requirements. Similarly, conventional PCB technology is not ideal for forming busbars or the windings of magnetic components. As a result, power density suffers because of the geometric constraints imposed by the planar printed traces. In these and other regards, conventional PCB technology is imposing limitations on the achievable size and performance of electronic equipment. These limitations are becoming more important as component and power densities continue to increase.

This thesis investigated an enhanced circuit board fabrication approach that provides three-dimensional patterning of one or both of the outside layers of circuit boards, and enables greatly improved realization of these structures and functions. With further work, this three-dimensional circuit board (3DCB) technology has the potential to overcome the limitations of existing PCB technology at low cost, while preserving much of the conventional manufacturing framework. It is anticipated that 3DCB technology will benefit a wide range of electronics applications, particularly those where size and power density are important, including power supplies, radio-frequency and microwave circuits, and portable electronics.

1.1 Three-dimensional Patterning

To realize three-dimensional surface patterning, this technique uses photolithography in conjunction with commercially-available ultra-thick photoresists. Such three-dimensional patterning techniques have been widely explored for fabricating micro-electromechanical (MEMS) devices [6], and can be readily adapted to the present application. One available photoresist system that has been exploited in the past

and that we propose to use here is SU-8 [9, 10]. This negative[1] photoresist can be used to fabricate structures with heights exceeding 1 mm and aspect ratios of more than 18 [9], thus providing feature heights on par with typical circuit components and feature resolution as good as that found in most PCB designs. The approach used to fabricate these structures makes use of a "scaffold" technique.

1.1.1 The Scaffold Technique

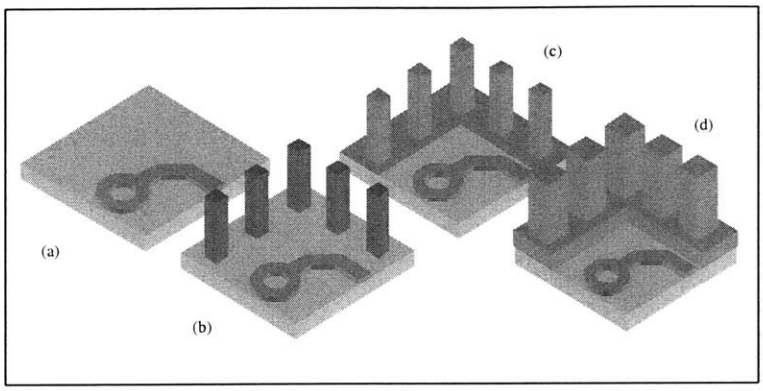


Figure 1-1: A simplified illustration of a scaffold fabrication approach. (a) The surface layer of the circuit board is coated and patterned to reveal only desired conductor areas. (b) Ultra-thick photoresist is deposited, exposed, and developed to form a three-dimensional scaffold. (c) A thin seed-layer of conductor is deposited and patterned. (d) A heavier copper layer is electroplated over the seed layer, completing the structure.

While the scaffold technique could be used in a number of distinct ways, highlighted in Fig. 1-1 is the easiest and most cost effective approach. A thin photoresist is first applied to the circuit board and patterned, leaving only desired conductor areas exposed (Fig. 1-1a). Ultra-thick photoresist is then deposited, exposed, and developed to form a three-dimensional scaffold (Fig. 1-1b). Next, the entire surface (including the scaffold) is covered with a thin conductive seed layer and patterned (Fig. 1-1c). A much heavier layer of conductor is then electroplated over the seed-layer, completing

[1] In negative photoresists, the mask exposes the areas which will be retained after development.

the three-dimensional structure (Fig. 1-1d). A key step in this process is depositing and patterning the seed-layer which is accomplished by sputtered metal deposition.

The proposed scaffold fabrication approach is particularly advantageous when a structure having a high exposed surface area is desired (e.g., for heat sinking or to reduce high-frequency resistance). A key advantage of all of the methods used is that they are compatible with existing PCB fabrication processes and are fundamentally inexpensive.

1.2 Current Technology

There have been a number of patents granted for work completed on three-dimensional circuit structures in recent years, although none have been found to replicate the scaffold technique discussed here. Alford et al. [3] fabricated a three-dimensional inductor coil on a semiconductor substrate by sequential deposition and etching of photoresistive layers and by electroplated metal deposition to produce a multi-loop inductor coil. Hirsch and Lin's [5] invention is a method for fabricating a high-aspect ratio, freestanding microstructure using SU-8 photoresist. Cylindrical cavities with aspect ratios of 8:1 are claimed. Finally, Warren [4] describes a technique for patterning electroless plated metal on a polymer substrate. The substrate is then complexed with a noble metal compound, such as palladium, selectively irradiated to form the desired conductor pattern, before etching to reveal the desired conductor pattern. Electroless plating is used to form the final metal pattern.

While not using photolithographic methods, there is a company in Germany fabricating 3D device contours with the use of laser technology. "LPKF Laser & Electronics AG"[2] have developed a process that uses laser-sensitive plastic substrates to fabricate laser-written circuit patterns directly from computer generated layout. The substrate consists of an injection-molded plastic doped with a metal-based organic

[2]LPKF Laser & Electronics AG, Osteriede 7 D-30827, Garbsen, Germany. (http://www.lpkf.com)

compound that undergoes a local physiochemical reaction upon laser activation. This exposes metal atoms along the intended circuit path. Finally, the actual circuitry is deposited in an electroless plating step. The technique is highlighted in Fig. 1-2. While the technique allows trace resolution down to 100 μm with 150 μm spacings, it uses a non-standard substrate.

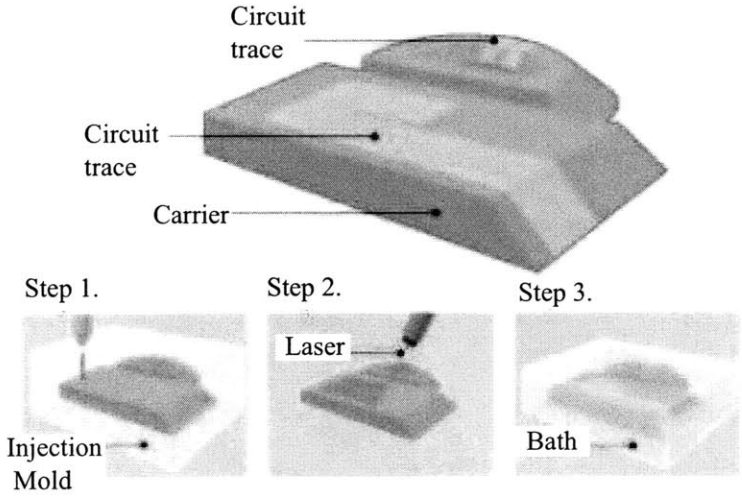


Figure 1-2: Laser direct structuring, a new way of creating molded interconnect devices, uses laser energy to activate those portions of injection-molded carrier that correspond to the deposited circuitry.

1.3 Circuit Structures

The scaffold technique enables the fabrication of a wide range of valuable three-dimensional structures. For example, pin-fin heatsinks can be directly fabricated as part of a circuit board with the proposed technology (Fig. 1-1d). One would expect this heatsink to greatly improve heat transfer to the surrounding air and allow for a corresponding reduction in the board area needed for this function. In many contemporary PCB designs, large copper plane areas are dedicated solely to heat sinking. Accordingly, this application was explored in some detail. While 1 mm pin-

fin heatsinks were successfully fabricated and tested, the devices failed to show any improvement over a comparable plane area heatsink, due to cracking of the electroplated copper at the recessed corners of the pin-fin structures. However, a successful technique to fabricate high-aspect ratio SU-8 structures has been successfully demonstrated and with further investigation it is possible that these pin-fin structures can show significant improvement over planar heatsink areas.

1.4 Thesis Organization

The thesis is divided into five chapters, this first one being the introduction. Chapter 2 details the preparation and setup work undertaken before the scaffolding fabrication process could begin. In Chapter 3, an investigation of power applications is presented. This focusses on heatsink structures and examines the performance of viaed heatsinks. This chapter offers the pretext for the fabrication of pinfin heatsink fabrication using scaffolding.

The next chapter deals with the SU-8 processing from deposition through to development. In Chapter 4, the process of metal deposition is discussed while Chapter 5 outlines the tests undertaken on the pinfin heatsinks fabricated using the scaffolding process. Finally, the conclusions of Chapter 6 are intended to synopsize the work undertaken and offer direction for any subsequent investigations.

Chapter 2

Preparation

2.1 Overview

The first step in manufacturing the proposed three-dimensional (3D) structures is creating a scaffold. In our experimental process, this is achieved by pouring SU-8 onto an FR4 substrate, pre-baking it to drive out the solvent and then patterning the poured structure through photolithography. Here we describe the apparatus and methods developed to create pre-baked SU-8 structures of relatively uniform thickness (up to 1mm) that are suitable for subsequent photo-processing.

In order to achieve effective pouring of the SU-8 photoresist onto the FR4 substrate, a simple mechanical structure has been designed and constructed. This structure facilitates the controlled pouring of SU-8 onto the substrate and the subsequent pre-bake process.

Obviously, the most critical requirement of the structure is to prevent the photoresist from leaking onto the hotplate on which it rests. To this end, a four-layer sandwich is arranged consisting of the hotplate, the substrate and teflon and aluminum rings.

The apparatus consists of a square hotplate, measuring 10 inches in length, onto which is clamped an aluminum plate, with 16 bored and tapped screw-holes. This

was thought to be a more practical approach to simply boring into the hotplate. The interface between the plate and sheet was thermally greased and clamped firmly. up to four unclad FR4 substrates rest on the sheet, such that there is a screw hole adjacent to, but not covered by, each substrate corner. The FR4 substrates were purchased from the Injectorall Corp. Each square board measures 3 inches in length and 120 mil in thickness. Enclosing each substrate is a square ring of teflon® which fences in the outer perimeter of the FR4 without overlapping the screw-holes in the aluminum plate. Finally, each teflon® ring is clamped in contact with the substrate by a square aluminum ring on top. Each of these aluminum rings has 4 bored corner holes allowing it to be screwed into the aluminum baseplate.

This sandwich structure, detailed in Fig. 2-1 and photographed in Fig. 2-2 is effective in restricting all of the poured SU-8 to an enclosed square of FR4 substrate, measuring 2.5 inches in length.

2.2 Pouring Equipment

A Dataplate® digital hotplate has been purchased from Omega Engineering Inc. This 100 sq. inch hotplate is equipped with a timer, automatic turn-off and "ramp per hour" settings as well as closed-loop plate temperature control.

The aluminum baseplate has been cut to fit flush over the hotplate top surface. Each of its tapped screw holes were chosen to fit a 5/8 inch 10-32 size screw which links it to the aluminum rings. The hotplate was thermally greased before the baseplate was clamped onto its corners.

The baseplate is also been drilled so that beneath the center of each FR4 substrate was a narrow vacuum vent. Each of the vent-passages leads to the edge of the baseplate where sealed, male-pipe to barbed adapters are attached to each. Flexible vacuum tubing feeds to 4 ball valves with *Swagelok*[1] tube fittings. Finally, each

[1]Available from McMaster-Carr at http://www.mcmaster.com

valve connects to a 4-way manifold which passes to the vacuum pump. The pump is an oilless vacuum pump from Gast Manufacturing Inc., capable of supplying a 10 psi vacuum. It is connected to the mains via a heavy-duty switch with an indicator lamp. This vacuum assembly is necessary to ensure uniform clamping of the substrate to the levelled hotplate. Unlevel substrates would result in significant height variations in the SU-8 structures after development. The vacuum is also important in the initial alignment of the substrate within the teflon® and aluminum clamps.

The 4 square teflon® ring-clamps were fabricated using an abrasive water-jet cutter. Teflon® was chosen in this application because of its minimal moisture absorption and low friction coefficient[2]. The diameter of the teflon® ring-clamps was such as to fence in the outer perimeter of the FR4 substrate without overlapping the screw-holes.

The 4 square aluminum ring-clamps, also cut using water-jet, were of slightly longer length to overlap with the underlying baseplate screw holes. These were drilled at each corner with a 10-32 size through-hole, so that the aluminum ring could be fastened to the baseplate, clamping the substrate and the teflon® ring in between.

2.3 Preparation

The room where pouring took place was fitted with UV-light filters, effective below wavelengths of 500nm, to avoid interference with the subsequent SU-8 exposure. The room was also equipped with a dehumidifier system, which maintained humidity below 45%, regardless of ambient conditions. This was to counter the adverse effect of high humidity on SU-8 adhesion, which is well understood [7]. The preparatory rinsing cleaning and drying of the FR4 substrates was conducted in an acid-hood. A 2-hp air compressor with a detachable air-gun has been purchased to allow rapid drying of the substrates after ethanol and deionized water rinsing. Finally, a controllable

[2]http://www.dupont.com/teflon/af/unique.html

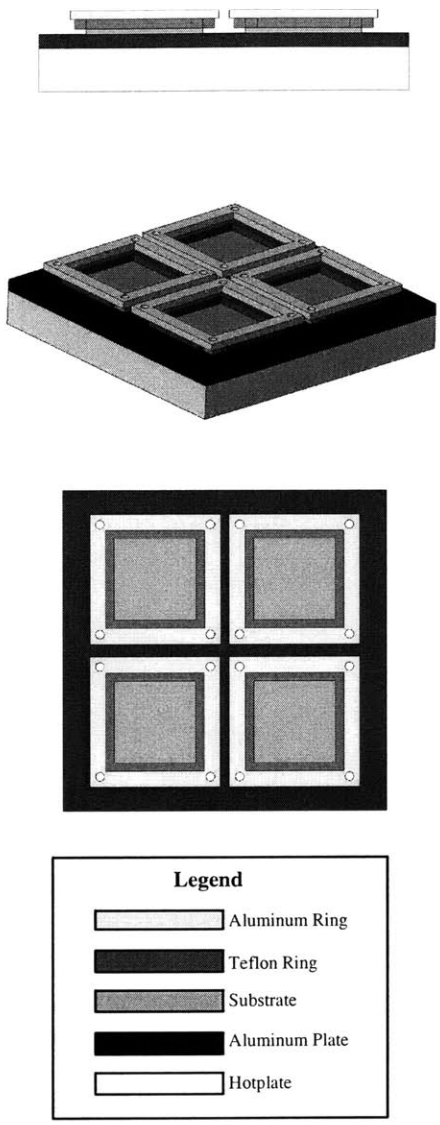
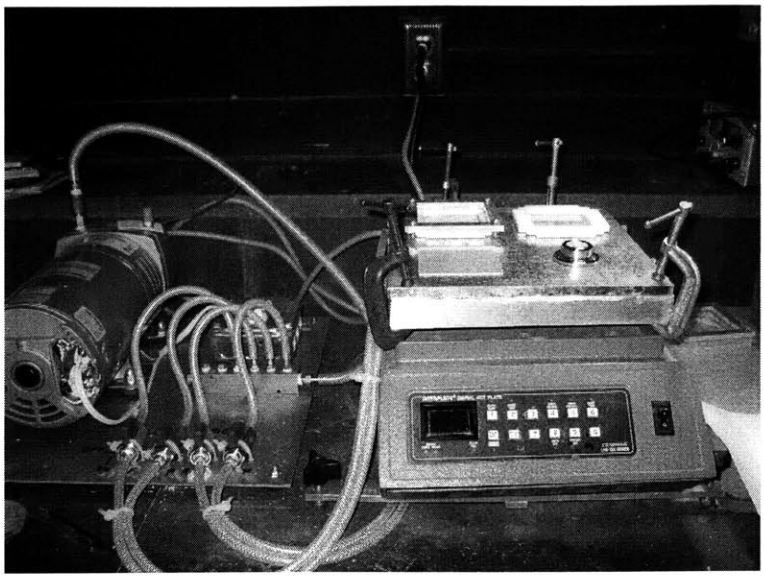


Figure 2-1: Drawing detailing the sandwich structure used to effective SU-8 pouring.

high-temperature oven is used to remove any excess moisture still present after blow-drying. The oven temperature is maintained at 180°C.

Critical to attaining structures of uniform height is correct levelling of the hotplate. This is achieved with the aid of a "bulls-eye" level. However, it is difficult to achieve perfect levelling at the micron scale. So the structure heights (e.g. 800μm and 1mm) achieved reflect the average height over the entire board rather than the exact height of each individual structure.



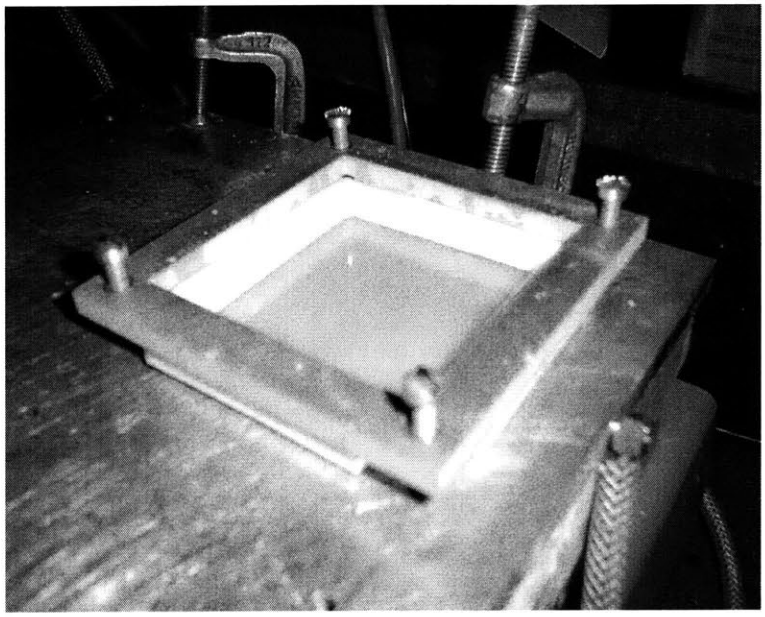


Figure 2-2: Photographs of the apparatus used for pouring

Chapter 3

Thermal Analysis

In the investigation of fabrication techniques suitable for use in power electronics, it was decided that heatsinking structures would be the application to explore. The dissipation of heat from both passive and active components has long been an important focus of the power electronics industry. Heat dissipation has become more challenging in light of increasing power densities. Coupled to this is the critical emphasis on low cost devices which further complicates the challenge. This chapter outlines the experimental testing and modelling of viaed boards investigate the effect of increased viaed cooling area on heatsink performance.

Demonstration of the approach is focussed primarily on heat removal from a TO-220 device package. This package is ubiquitous in the power electronics sector, as well as the general electronics area, housing, for example, diodes, MOSFETs and, power resistors. A practice of manufacturers has been to include a curve in the component's datasheet [20], similar to that in Fig. 3-1. The curve relates steady-state power dissipation in the device to the required cooling area. This assumes that the designer has allocated enough space on either the bottom or top surface of the PCB to allow effective device cooling. Clearly, this constrains the designer's use of space. The cooling effect, due almost entirely to convection, increases as the area is made larger. So an intuitive approach to increasing area would be to use a PCB with plated vias

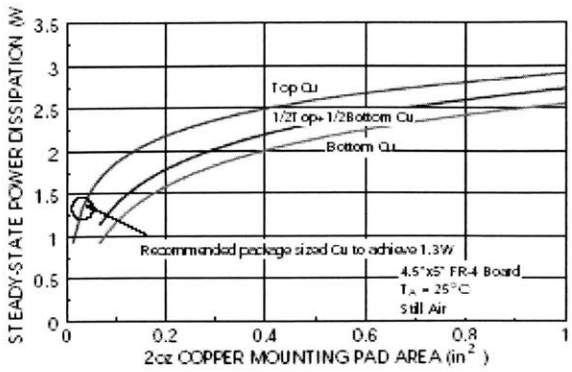


Figure 3-1: Maximum power dissipation curve for the SOT-223 power MOSFET from *Fairchild Semiconductor [20]*

so as to increase the effective cooling area and promote increased convective airflow. Elementary mathematical analysis shows that the vias' radii should be less than twice the total board thickness to result in an increase in the overall cooling area. This is seen by comparing the curved surface inside the via to the area of a circle with the via's radius. To test this hypothesis, a series of experimental tests and supporting analytical study were undertaken.

The general procedure for experimental testing was to fasten a TO-220 resistor to the heatsink structure and observe temperature rise as the input power is varied. However before any particular conclusions could be drawn regarding the effectiveness of various techniques, it was thought prudent to investigate some ancillary issues which might give rise to future concern.

3.1 Ancillary Issues

The first of these effects is radiative heat transfer from the PCB surface. This was analyzed by spraying the heatsink surface with black paint. Therefore, should there be significant radiated heat transfer from the heatsink surface to the ambient environment, then this would be reflected in a lower device operating temperature for

the blackened surface. Since the general Stefan-Boltzmann expression for radiative heat transfer from a surface shows that transfer is linearly proportional to the fourth power of temperature, radiative effects are not expected to be significant [14].

The second consideration investigated at this point is the effect of the direction of unforced airflow over the board surface. This is investigated by turning the entire board heatsink on its side so that any flow which was parallel to the surface of the flat board is now perpendicular to the surface of the turned board. Again, any significance would be evident in the temperature measured at the thermocouple.

Finally, the effect of greasing the interface between the resistor and the board was investigated by comparing thermocouple readings with and without greasing.

At this point it should be noted that the position of the thermocouple for the purpose of temperature measurement is critical to the understanding of the heat flow that takes place. In this initial investigation, two thermocouples were positioned on the heatsink, on either side and half way between the resistor's center and the board's edge. The average reading of the two was recorded in each case. However, upon some consideration, it is evident that a more efficient heatsink (yielding lower device temperature) can result in a higher temperature on the board surface, away from the device, for a given power level. This is because a lower thermal resistance to conduction across the board will have a correspondingly lower temperature drop across it if the power source is constant.

It is helpful to think of this in terms of circuit theory, where the power input corresponds to a current source and the temperature drop across a thermal resistor is analogous to a voltage drop across an ohmic resistor [21]. The situation investigated might be modelled in terms of a finite convective and conductive thermal network as shown in Fig. 3-2. Clearly, the resistance between the resistive device of the TO-220 and the package case, as well as the convective resistance between the case and the ambient environment are beyond immediate control. However, if the board's conductive resistance is increased, then the temperature at a point half-way between

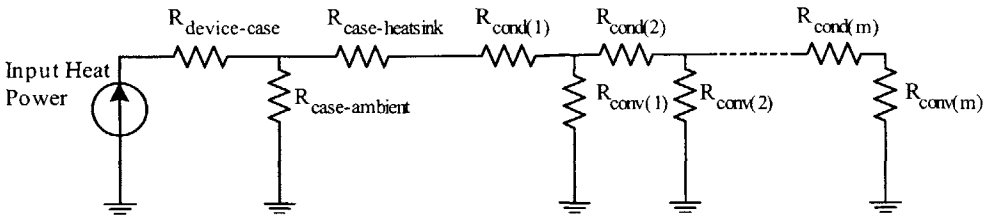


Figure 3-2: Equivalent thermal resistor network for the TO-220 heatsink. The horizontal thermal resistances, R_{cond}, reflect conduction through the board, while the vertical resistors, R_{conv}, reflect heat removal through convection from the board.

the heat source and the board edge will show an increase, and not a decrease, in temperature.

A more intuitive thermocouple position is on the TO-220 case. A thermocouple on the case will record a lower temperature for a more effective heatsink. In the initial investigation described below, the thermocouple is on the heatsink, so that higher temperature (on the board away from the TO-220) signifies more efficient heat transfer. Subsequent tests measure performance with the thermocouple fastened to the TO-220 case. Note that there is a slight difference in temperature between the plastic case of the TO-220 and the tab. However, this difference has never been seen to exceed 2% of the absolute tab temperature and can not be considered significant since all measurements are made in the same manner. Therefore, for ease of attachment to the device, the thermocouple was epoxied to the plastic case rather than the tab itself.

The test boards are 2 single layer PCBs with 2 square inches of 1 oz. plated copper on one or both sides and central plated holes for attaching TO-220 5.1Ω resistors. Each board has an inline arrangement of 0.06 inch diameter vias, positioned in two rectangular areas surrounding the resistor, as illustrated in Fig. 3-4. Four such boards were ordered and the boards were labelled A to D for clarity. The details of each are outlined in Table 3.1.

Board B is is used to investigate the effect of radiation, while the boards labelled C and D are used to examine board orientation and the effects of greasing the board-

Board	*Single-side Plating*	*Double-side Plating*	*Painted Black*	*Turned on Side*	*Greased Interface*
A1	√	×	×	×	×
A2	×	√	×	×	×
B1	√	×	√	×	×
B2	×	√	√	×	×
C1	√	×	×	√	×
C2	×	√	×	√	×
D1	√	×	×	×	√
D2	×	√	×	×	√

Table 3.1: Details of boards used to investigate ancillary issues. A check mark indicates that the board has a specific characteristic.

package interface respectively. The *A* board is used as a benchmark. The number index, *1* or *2*, refers to whether or not the board is single-side or double-side plated. The results for each board are plotted in Fig. 3-3.

The first clear result is that the effect of radiation is negligible. This is seen by comparing the plots for the *A* and *B* boards. These are virtually identical within the bounds of experimental error. Accordingly, radiation is clearly not significant and is not considered further in the analysis.

The plot leads to further interesting results. Since the highest surface temperature is recorded on the *C* boards with the greased interface, we conclude that this is the most effective heatsink, as reasoned previously. All subsequent investigation was undertaken with the interface between the heatsink and the TO-220 lightly greased. Also, the effect of turning the board is noticeable but not overly significant. This is evident from comparison of results for boards *A* and *D*. The effect of the vias is more perceptible if the board is oriented vertically and, while noteworthy, this result is not applicable in a general case since board orientation and airflow direction will vary with the application and ambient conditions. In each case, the addition of plating on the bottom of the board acts to increase the temperature observed for a given input power. As outlined previously, this indicates a more effective method of heat

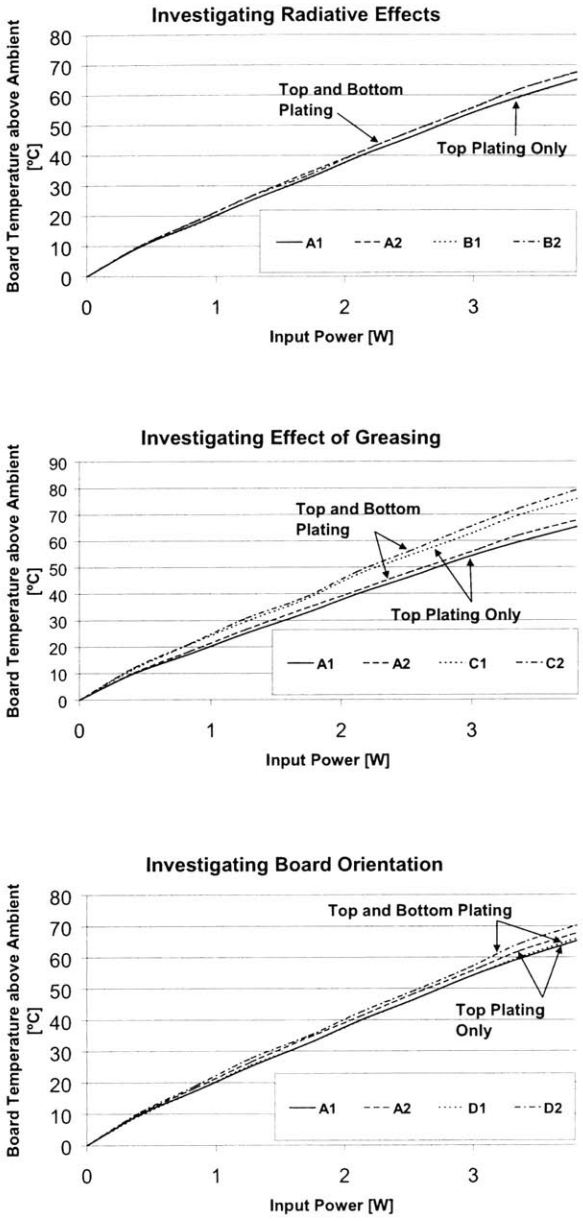


Figure 3-3: Investigation of Ancillary Issues related to heatsink optimization

Board	*Total Number of Vias*
1	0
2	92
3	109

Table 3.2: Details of boards used to investigate the effect of vias

transfer to the environment, as one would expect with the addition of a high thermal conductivity copper path on the board's underside.

3.2 The Effect of Vias

This preliminary investigation concluded, attention was now turned to the effect on cooling of a viaed PCB. Thermal vias are a frequently used technique to quickly and efficiently transfer heat from the source, usually for conduction to a nearby cooling plane. [16, 17, 18]. This experiment is intended to investigate their effectiveness for convection in the absence of any forced airflow and compare performance with an unviaed PCB over a relatively large cooling area.

To test the efficiency of vias an additional set of circuit boards was employed, with temperature measurements taken at the device case. Each test-board is a single-layer PCB with 4 sq. inches of 1oz. plated copper. The details of each board are outlined in Table 3.2. The vias on boards *2* and *3* are packed inline and arranged in rectangular squares around the resistor. The arrangement is detailed in Fig. 3-4.

Board *1* has no vias and is used for comparison purposes. Similar to the previous test the input power was increased from zero and the corresponding temperature rise noted. In these tests, however, the thermocouple was epoxied to the TO-220 package itself. As mentioned previously, this proves a more appropriate measurement of performance, where lower case temperature indicates more effective cooling at a given input power level. The results of the test are shown in Fig. 3-5. Board *1* is labelled "No Vias" while boards *2* and *3* are labelled "Low Density Vias" and "High

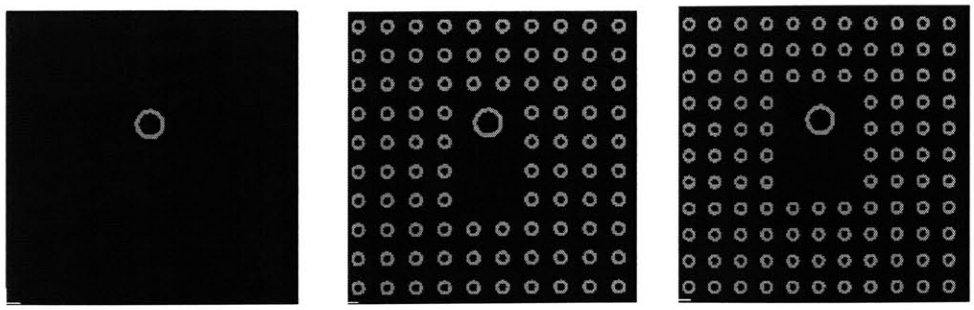


Figure 3-4: Investigation of increasing heatsink area with vias

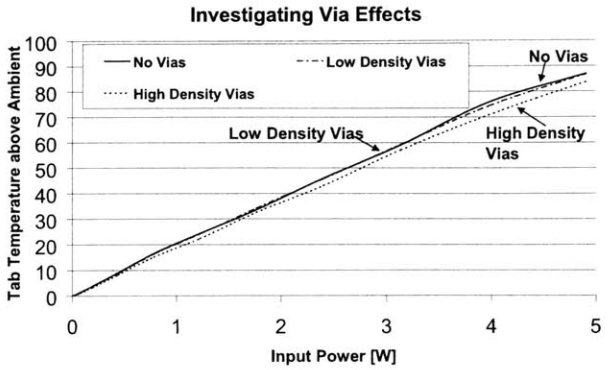


Figure 3-5: Investigating the effect of vias on heatsinking

Density Vias" respectively. All three boards show remarkably similar results although Board *3* shows slightly improved performance. The reasons for this are explored in the analysis that follows.

3.3 Theoretical Analysis

By way of explaining the experimental data from the test on viaed board cooling, a theoretical analysis was undertaken. This was not an attempt to directly replicate any experimental results with an analytical model. Rather, its aim was to provide an intuitive appendix to the actual results and help broaden the understanding of the data recorded. This analysis draws heavily on the standard tools of heat transfer

theory [14]. Since the goal is not a detailed model but simply a means to better understand the test results, the approach taken is deemed sufficient for this work.

In comparing boards 1, 2 and 3 from Table 3.2, the analysis examines the temperature distribution in one dimension along the plane of the PCB. One-dimensional analysis considerably simplifies the complexity of the problem and eases the capacity for an intuitive understanding. The analysis relies on the fin approximation of heat transfer from extended structures. An involved discussion of this theory can be found in any heat transfer text (e.g. [14]) and is not considered here. Suffice to note that the approximation supposes that heat gradient in one direction (x in this case) sustains the heat transfer by conduction internally, while at the same time, there is energy transfer from the surface, principally by convection. The PCB lies in the $\{x,y\}$ plane such that its edge is parallel to the z axis and the dominant conduction path is along the x axis. The temperature distribution along the y plane, which points into the board, is assumed negligible compared to that along the x axis. This assumption is one that is generally acceptable in a thin board and with the addition of vias, there is no danger of this temperature distribution being significant. Temperature distribution along the z axis is not considered either. The infra-red photograph of Board *1*, taken at an input power of 4.5W, shows that these approximations are reasonable. Furthermore, any inaccuracies associated with the method are not considered pivotal to the understanding of the test results.

By application of the fin approximation, the board is decomposed into 4 parallel-connected fins, each an isosceles triangle of height equal to half the board's length. Their tips meet at the board's center so that each triangle has base angles of 45^o. and a tip angle of 90^o. One such fin is highlighted in Fig. 3-6. The complete "Mathematica"[1] source code for the analysis of the boards *1* and *2* is included in Appendices *A* and *B*. Since this includes a detailed explanation of all the relevant assumptions associated

[1] *Mathematica* is an extensive mathematical and engineering simulation package available from *Wolfram Research, Inc.*, Champaign, Illinois, USA. (http://www.wolfram.com) The version used in this analysis is *Mathematica 4.1*

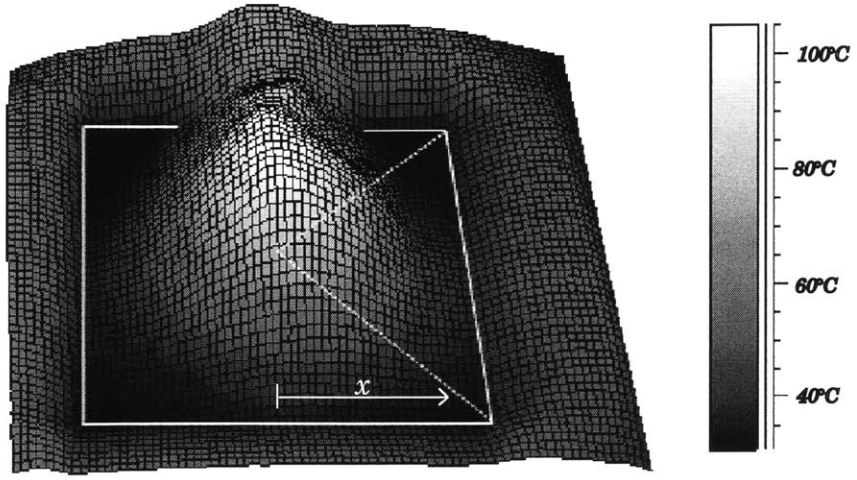


Figure 3-6: Thermal IR profile of Board *1* at an input power of 4.5W

with the analysis, it is not examined in depth here.

Suffice to note that each fin is further decomposed into a ladder network corresponding to Fig. 3-2, where conductive resistance is given by Equation 3.1 and convective resistance by Equation 3.2. In this case, l is the incremental distance of each element in the x direction, kA is the effective product of thermal conductivity (in W/mK) and cross-sectional area in each element, A_s is the surface area available for convective heat transfer from each element and h is the coefficient of convective heat transfer from the board.

$$R_{cond} = \frac{l}{kA} \tag{3.1}$$

$$R_{conv} = \frac{1}{hA_s} \tag{3.2}$$

Fixing the conductive resistance from the device to case and the convective loss from the the case to the ambient, an expression is developed for the case temperature

as a function of input power. Evaluation of the ladder network now allows the curves of Fig. 3-7 to be plotted corresponding to boards *1* and *2*. The viaed board shows slightly improved performance, reflecting the actual results of Fig. 3-5. However, the performance of the viaed boards, in both simulation and experiment, depend hugely on h. Its value for a flat board is estimated from the expression relating Reynolds *(Ren)* and Nusselt *(Nu)* numbers in laminar free convection, repeated in [14] and given in Equation 3.3.

$$Nu = 0.54 Ren^{0.25} \tag{3.3}$$

The Reynolds number, a dimensionless physical function of board parameters and ambient conditions, relates inertial to viscous flow effects and is estimated from Equation 3.4, where:

g = acceleration due to gravity in m/s^2

T_s = surface temperature in K

T_o = air temperature in K

$\beta = \frac{T_s - T_o}{2}$

ν = kinematic viscosity of air in m^2/s

α = thermal diffusivity of air in m^2/s

l = board length in m

$$Ren = \frac{g\beta[T_s - T_o]l^3}{\nu\alpha} \tag{3.4}$$

Finally, Equation 3.5 relates the Nusselt number to the effective coefficient of heat transfer over the entire board area, where k is the thermal conductivity of the air, dependent on the board's surface temperature.

$$h = \frac{kNu}{l} \tag{3.5}$$

Evaluating this expression for a 4 sq. inch board, at a board temperature of 78°C

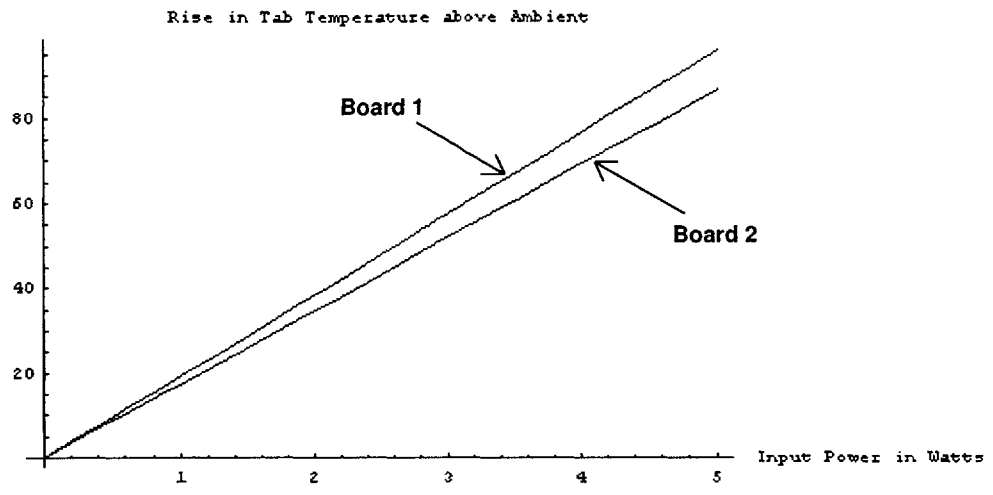


Figure 3-7: Results of modelling investigation comparing flat and viaed heatsinks

(350K), leads to a value of 14.35 W/m^{2}K for h, where the thermophysical properties of air, as a function of temperature, are available from the National Institute of Standards and Technology[2] as well as most heat transfer texts[14]. The value of 78°C was chosen as typical of the normal operating temperature in many power electronics applications. Also, since the variations in the thermophysical properties are not significant over temperature compared to the quadratic dependence on board length, this is judged a reasonable approximation. This value, calculated for the case of a flat board, will not be true for a viaed board, so its value is altered, as outlined in Appendix *B*, to account for this discrepancy and the recorded results for the viaed board.

While the addition of vias to the board results in some improvement in both the experimental and theoretical analysis, it is clear that the effect is minimal and certainly not sufficient to justify it as a design tool in most applications. Also of note is the fact that the addition of vias, while increasing the area available for convective

[2]http://www.nist.gov/srd/materials.htm

heat dissipation, severely limits the lateral conductive heat path across the board by disrupting the high thermal conductivity copper path that exists on the top surface of the flat board. Accordingly, the arbitrary introduction of more vias will not result in any significant improvement in performance and instead leads to poorer heat transfer from the source.

Although not a general result, this investigation is interesting in its justification of a physical result. It also provides the motivation to identify fresh techniques of increasing cooling area that will have a significant impact on device temperature. One such approach is a pinfin heatsink, where the vias might be replaced with pinfins on the PCB surface.

Chapter 4

SU-8 Processing

The scaffolding process is thought to be suitable for the fabrication of a variety of structures with applications in the power electronics sector. These include busbars, planar inductor windings, EMI shields and heatsinks. Heatsinking was chosen as the initial avenue of exploration for a number of reasons, but most notably because there exists the possibility of an optimum design exists for specific applications. Also, the techniques applicable to fabricate 3D heatsink structures should be readily applicable to other structures. This chapter outlines the photolithographic procedures of the scaffolding process, from SU-8 deposition through to the development of structures up to 1.2 mm. Apart from the poured deposition step, all of the work took place at the Microsystems Teaching Laboratory (MTL) at M.I.T.

4.1 SU-8 Applications to 3D PCBs

The general target of the PCB application is "vertical wall" structures of up to approximately 1 mm in height and as high an aspect ratio as is feasible (e.g. in excess of 4:1). Such structures will be suitable for heatsinks and many other applications. In keeping with standard practice in the PCB industry, the substrate used is FR4. The board substrate used in these prototypes and experiments measures 9 sq. inches.

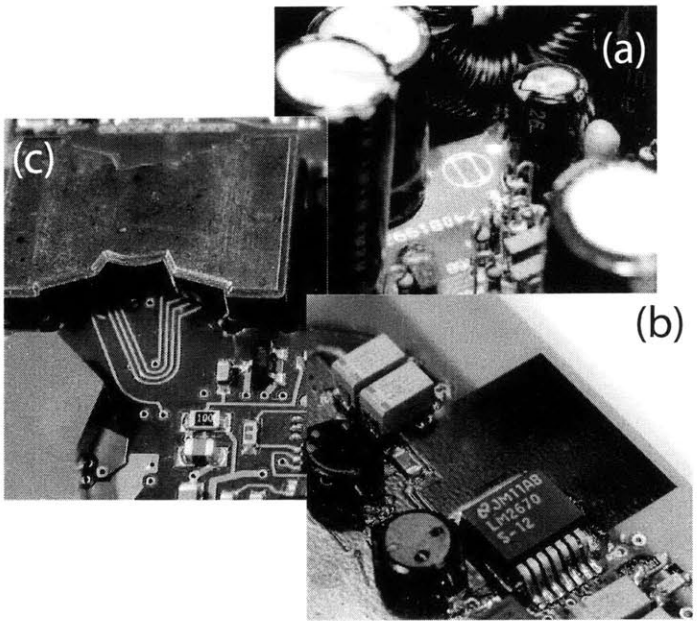


Figure 4-1: Highlighting the increased functionality associated with recent PCB technology.

In general, there is a vast amount of vacant volume on the surface of a PCB, because the board packaging will be determined by whatever component stands highest off the board, as shown in Figs. 4-1 (a) and (b). Even in the most recent power converters, planar inductors can rarely be made lower than 1mm, leaving at least that much space for exploitation. This is seen in Fig. 4-1 (c). Therefore, the goal of this investigation is to explore structures of SU-8 up to 1mm.

While the current practice is to spin-coat the photoresist onto the substrate, such an approach would not be expected to be commercially viable in this case. Multiple coatings would be required to reach 1mm and there may be concerns relating to the integrity of the bonding between coatings. Therefore a different approach is proposed. Instead of spin-coating, the photoresist is poured onto the substrate with a pipette. Clearly, if we want to accurately measure the poured volume, the SU-8 solution will need to be of relatively low viscosity. The solution selected was *SU-8 2005*, which

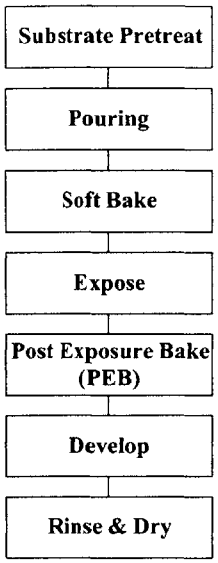


Figure 4-2: SU-8 Process Flowchart

was supplied by the Microchem Corp.[1] of Newton, MA. *SU-8 2005* is a negative radiation sensitive resist supplied in a 45% cyclopentanone solvent solution[12]. The entire SU-8 process is outlined in Fig. 4-2 and outlined in detail in the following sections.

Following numerous iterations, an effective pouring recipe was eventually arrived upon. This was developed by a combination of references [7, 8, 12], other students' work and the author's experience in the field. The recipe outlined here produced a 800μm layer of cured SU-8 on an area of 6.25 sq. inches. While the overall board area is 9 sq. inches, the bounding teflon ring eliminates some of this.

4.1.1 Substrate Preparation

To begin, the FR4 substrate is rinsed in isopropyl alcohol (IPA) to remove any surface dust or contaminants remaining after manufacturing, followed by a rinsing with

[1]Microchem Corp., 1254 Chestnut Street, Newton, MA 02464 (http://www.microchem.com)

deionized water. After blow-drying any surface moisture from the surface, it is placed in a temperature-controlled oven at 130°C for 30 minutes to remove any remaining moisture or dampness.

Once dry, the surface is micro-roughened to improve adhesion between the substrate and the SU-8. This is accomplished by placing the FR4 in an oxygen plasma environment for 10 minutes. The *asher*, which is a "Plasmod" from the Tegal Corp. is a 100 W, 13 MHz RF device used at 60% of its rated power under a vacuum of 350 mT. The *ashing* process is critical to achieving satisfactory adhesion between the FR4 substrate and the SU-8 after curing. The process is thought to relate to three principle mechanisms; (i) mechanical keying or interlocking, (ii) molecular forces and dipole interactions and (iii) chemical bonding[19]. These mechanisms contribute either alone or in combination to produce the necessary bond. The rule of thumb is the higher the surface energy of the substrate, the higher the wettability and the associated improvement in adhesion. To correlate with this theory, a wettability test was undertaken, in order to estimate the relative wettabilities of the ashed and unashed boards. This test, the "Accu Dyne Test", available from Diversified Enterprises[2], estimates wettability[3] in dynes/cm. The result is that the unashed board was estimated at 56 dyne/cm while the ashed board was found to lie above the testing range, which extended to 60 dyne/cm.

4.1.2 SU-8 Pouring and Pre-bake

Once ashing is complete, the substrate is removed immediately to the hotplate where the SU-8 is poured. It is important to limit the time that the substrate is exposed to the atmosphere after ashing so as to minimize the ambient moisture that may absorbed.

To make sure that thermal equilibrium is maintained over the entire surface of the

[2]Diversified Enterprises, 101 Mulberry Street, Suite 2N, Claremont, NH 03743.
[3]1 dyne/cm = 10^{-5} N/cm.

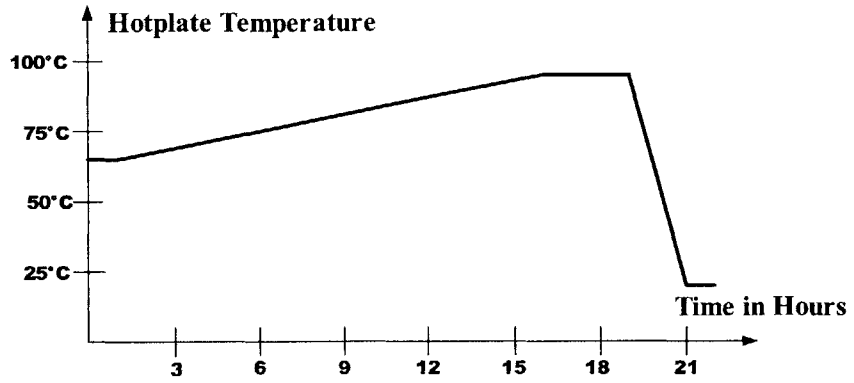


Figure 4-3: Pre-bake heating profile for the 800μm SU-8 process.

board, the FR4 is preheated to 65°C on the hotplate for 30 minutes before pouring. At this point, 10ml of *SU-8 2005* formulation is pipetted onto the board. The SU-8 is prevented from flowing off the substrate by the boundary of teflon around its perimeter. It has been found that a slow pre-bake is critical to the successful expulsion of all the solvent in the SU-8 [12]. Accordingly, the temperature is raised at a rate of 2°C per hour for 15 hours, until the temperature reaches 95°C. The temperature is maintained at 95°C for 3 hours before the hotplate is switched off. Again, the board remains on the hotplate until temperature has returned to room level, so that sudden changes in temperature are avoided upon cooling. This usually takes about 2 additional hours. A plot of the entire heating profile is included in Fig.4-3. Now the aluminum clamp can be unscrewed and the teflon clamp carefully prised away. At this point, we immediately begin the exposure process.

4.1.3 Exposing SU-8

It has been shown that high dosages of UV power below 350nm can result in over-exposure of the top portion of the photoresist [12]. Therefore, the 400 ultraviolet mJ/cm^2 source[4], measured with an i-line (365nm) probe and scope is filtered below

[4]The UV source is a "Karl Suss MJB3 Mask Aligner", known as *Broadband* at MTL.

350nm using a glass slide filter with a 40% transmission efficiency. This effectively reduces the UV source to about 230 mJ/cm^2 and accounts for the long exposure time required: 30 minutes. Placing a transparent film mask over the SU-8 during exposure will allow the subsequent development of the desired three-dimensional pattern. The masks were manufactured by the "Pageworks Company" of Cambridge, MA[5] on high resolution 5080 dpi transparent film. The mask is maintained in contact with the pre-baked SU-8 during exposure.

After exposure is complete, the substrate is immediately removed to a hotplate for the post-exposure bake (PEB). Again, it is imperative to minimize the delay in transferring from exposure to PEB and so ensure uniformity in the density of the cross-linking SU-8 chains [9, 12]. The substrate is baked at 65°C for 15 minutes, before being ramped at 180°C per hour to 95°C where it is maintained for an additional 3 hours. Experience has shown that the adhesion between the final SU-8 structure and the FR4 substrate improves with PEB time. The two-step PEB is designed to minimize substrate stress, wafer bowing and resist cracking. After completing the PEB, the board is removed from the hotplate and allowed to cool slowly in air. Again, this limits the stress associated with abrupt cooling. This usually takes 30 minutes, after which, the development step can begin.

4.1.4 Developing SU-8

After cooling, the SU-8 is placed in a beaker of MicroChem's SU-8 Developer[6]. Development time will vary, depending on the pattern exposed but is usually between 1 and 1.25 hours for 800μm high structures. The development can be shortened by heating the developer above room temperature, uniform agitation of the beaker and changing the developer solution mid-way through the process. However, careful at-

[5]PageWorks, 501 Cambridge Street, Cambridge, MA 02141 (http://www.pageworks.com)

[6]MicroChem's SU-8 Developer is effectively a solution of standard PM Acetate (Propylene Glycol Methyl Ether Acetate).

tention is paid during the final stages of development to avoid over-development of the structure. This would lead to undercutting of the final SU-8 mold and adhesion failure. The problem of under-development, which is the shown in Fig.4-4, is also to be avoided. To complete the process, it may be necessary to squirt additional developer in areas where the photoresist is slow to etch off. This is particularly the case for intricate structures. A final rinse with IPA followed by a rinse with deionized water completes development. The board can be blow-dried with air to remove any surface moisture that remains.

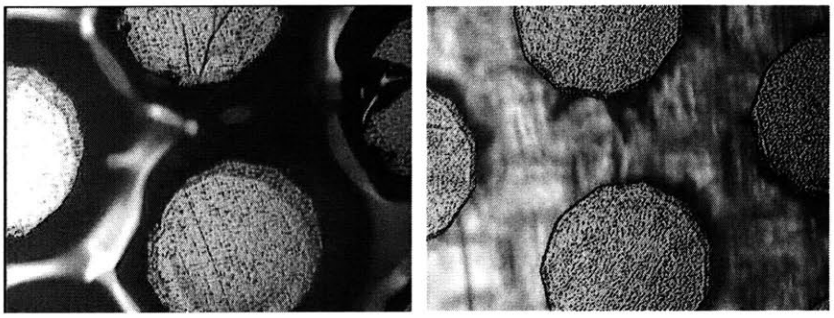


Figure 4-4: Comparing microscopic appearances of (left) underdeveloped and (right) correctly developed 800μm SU-8 pins

A selection of 800μm SU-8 structures are included in Fig.4-5. Successfully fabricated structures include pinfin arrays and inductor windings. These structures exhibit good adhesion to the FR4 substrate, sharp side-wall profiles and excellent material integrity.

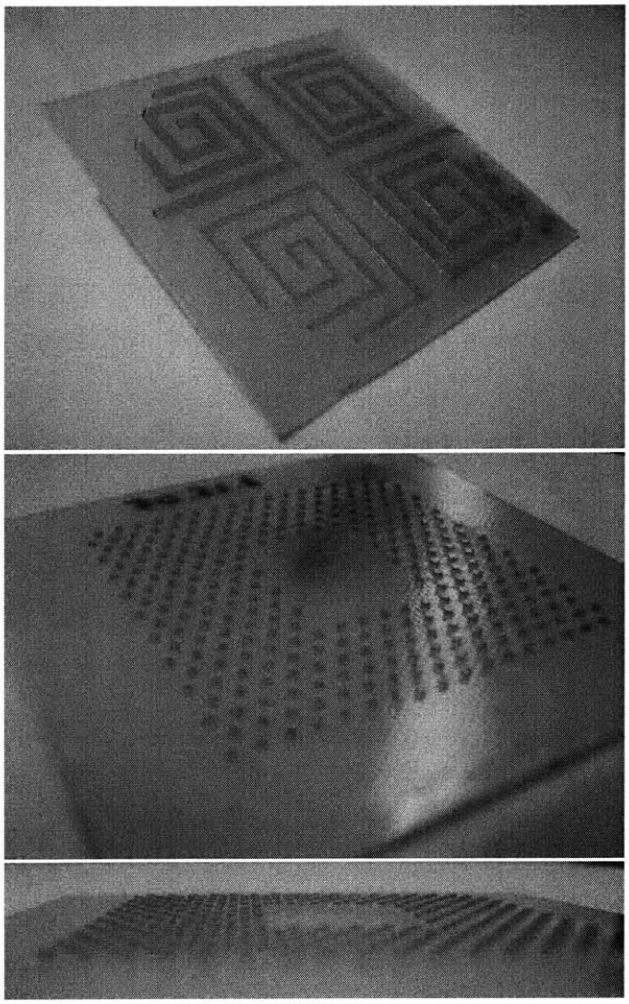


Figure 4-5: A selection of fabricated 800μm SU-8 structures.

Structure Height	*800μm*	*1mm*
Poured SU-8 Volume	10ml	12ml
Soft Bake time at 95°C	3 hrs.	6 hrs.
Exposure Time	30 mins.	35 mins.
Development Time	1-1.25 hrs.	1.25-1.5 hrs.

Table 4.1: Recipes for varied SU-8 structure heights.

4.2 Higher Structures

Having completed an initial investigation of structures up to 800μm, the next step was to increase the structure heights. A target was set at 1mm structures. This proved achievable, but required a number of changes from the 800μm recipe. The two procedures are outlined in Table 4.1. The pre-bake process is identical to Fig.4-2 over the first 19 hours. However, for 1mm structures, the plate temperature is maintained at 95°C for an additional 3 hours, in order to expel all the solvent present before returning to room temperature as before. Exposure and development times are also increased as outlined in Table 4.1. While structures up to 1.2mm have been successfully fabricated, it becomes increasingly difficult to expel all the solvent during the pre-bake without the mold becoming so brittle that it cracks on removal from the teflon ring.

Having found the expected linear relation between poured volume of SU-8 and the subsequent structure heights, an attempt was undertaken to quantify this mathematically. Critical to this analysis is the estimation of the densities of *SU-8 2005* before and after curing. Since this data was not readily available, it was estimated by mass and volume measurements of the board before and after the pre-bake. The result is

that the density increases from 995.2 kg/m^3 beforehand to 1283.8 kg/m^3 after. The relationship between poured volume and structure height is examined in Equations 4.1 through 4.5, where:

v_{poured} = volume of SU-8 poured before pre-bake in m^3

v_{cured} = volume of SU-8 after pre-bake in m^3

m_{poured} = mass of SU-8 poured before pre-bake in kg

m_{cured} = mass of SU-8 after pre-bake in kg

ρ_{poured} = density of SU-8 poured before pre-bake = 995.2 kg/m^3

ρ_{cured} = density of SU-8 after pre-bake = 1283.8 kg/m^3

A_{board} = board area available for pouring = 0.00403 m^2

h = cured structure height in m

As outlined in [12], the solid content of *SU-8 2005* is 45% by mass. So assuming all the solvent is expelled during the pre-bake, then the mass decreases to 45% of its original value.

$$v_{cured} = \frac{m_{cured}}{\rho_{cured}} \tag{4.1}$$

$$v_{cured} = A_{cured} * h \tag{4.2}$$

$$\Rightarrow h = \frac{m_{cured}}{\rho_{cured} * A_{cured}} \tag{4.3}$$

$$h = \frac{0.45 * m_{poured}}{\rho_{cured} * A_{cured}} \tag{4.4}$$

$$h = \frac{0.45 * v_{poured} * \rho_{poured}}{\rho_{cured} * A_{cured}} = 86.51 * v_{poured} \tag{4.5}$$

Estimating Equation 4.5 for 10ml and 12ml leads to theoretical structure heights of 865μm and 1.038mm respectively, which is resonably close to the values measured with a micrometer; 800μm and 1mm respectively. It should be noted, however, that

it is extremely difficult to attain constant structure height over the entire surface due to imperfect levelling of the hotplate prior to pouring. While every effort is made to level the hotplate, through the use of bulls-eye levels, this is only sufficient to ensure an an estimated accuracy of $\pm 10\mu$m.

4.3 Failure Mechanisms

Initially, the most common source of failure during SU-8 processing was due to wet or humid weather affecting the adhesion between the SU-8 and the FR4 substrate. High humidity makes it quite difficult to expel all of the solvent from the SU-8, presumably due to the higher water content of the environment. This results in an epoxy that is very tacky, difficult to expose and does not adhere to the FR4 substrate. The addition of a dehumidifier to the room where the pre-bake took place practically eliminated this effect. However, it is worth noting that the majority of this work took place between the months of October and March, when ambient humidity in Boston is generally low anyway.

Failure to insert the glass slide filter during exposure will result in SU-8 that is extremely tacky and generally the substrate becomes inseparable from the transparent slide mask. If the soft-bake time is too short, then one encounters "drift" of the exposed features during the PEB stage, as shown in Fig.4-6. This phenomenon is thought to result from excess solvent at the SU-8/FR4 interface which was not expelled during the pre-bake, returning to an aqueous state and destabilizing the overhead pattern.

Under-development of the SU-8 structures is an obvious mistake to be avoided. However, after rinsing the board with IPA, it is generally clear with the naked eye whether or not more development is required. Over-development is a more difficult issue to resolve. This requires an understanding of the specific process since more intricate features require more time to develop. Copious squirting of developer into

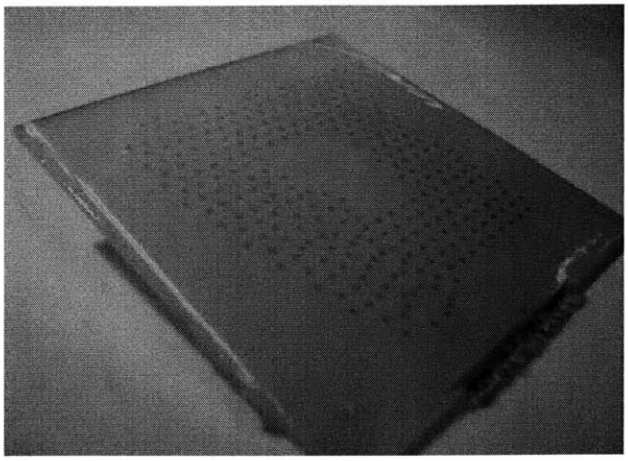


Figure 4-6: An example of "drift" failure in the SU-8 strucures observed during the PEB stage.

the more hard-to-reach features of the design will help to alleviate the problem of non-uniform development over the board's surface. Over-development generally results in widespread adhesion failure at the SU-8/FR4 interface, which would generally occur in the course of blow-drying the board after development is complete.

Chapter 5

Metal Deposition

Having completed the fabrication of SU-8 structures on FR4, the next step is metal deposition. This takes place in two steps. Firstly, a very thin seed-layer of sputtered metal is deposited on the area as needed, and then, electroplating is used to increase the thickness as desired. There is also the option of patterning the deposited metal for applications such as inductor windings. This chapter details the methods and processes used in metal deposition on the SU-8 structures described previously. Possible patterning techniques are discussed in Appendix C.

5.1 Sputtering

Sputtering is a process of using a plasma to bombard a metal target and transfer a film of material onto a substrate or onto the component which is to be coated. It is an example of a physical vapor deposition (PVD). An electric field (either AC or DC) is first applied and then Ar ions are accelerated towards the target. When the Ar ions strike the target, their kinetic energy is transferred to the target material and particles are ejected. One advantage of sputtering over, for example, electron beam evaporation, is that the Ar ions strike the target as well as the substrate. This can be beneficial for adhesion between the substrate and the deposited material but

may also lead to excess heating of the substrate. For this reason, a practice of pulsed deposition was employed. This pulsing, at low power, allowed the substrate time to cool after each period of deposition. This limited the stress in the metal film which arises due to the mismatch of coefficients of thermal expansion (CTE) between the metal and either the substrate or the SU-8. Stresses due to CTE mismatch can induce bending moments in the metal film.

While electroless plating is a standard PCB technique used for seed-layer deposition, it was not used in this investigation. There is evidence that the adhesion between electroless copper and FR4 is significantly worse than it is with sputtered copper and FR4 in the absence of a thorough pre-treatment process [22]. This pre-treatment may affect the SU-8 structures already fabricated on the substrate and so, sputtered seed-layer deposition was the route chosen.

5.1.1 Improving Adhesion

In keeping with current practice in the PCB industry, the metal deposited on the fabricated SU-8 structures was copper (Cu). Cu has extremely high electrical and thermal conductivities, (5.98×10^7 S/m and 390 W/mK respectively [21]) making it ideal for circuit board applications involving electrical conduction and/or heat dissipation. Initially, it was attempted to deposit sputtered copper directly onto the substrate but this proven unsuccessful, with widespread adhesion failure exhibited at the copper/substrate interface during the subsequent electroplating step. Failure of adhesion usually propagated from the point of electrical contact to the current source and was evidenced by blistering beneath the electroplated copper. Inspection revealed that the problem lay at the interface between the sputtered copper and the FR-4. An example of this failure mechanism is included in Fig. 5-1.

To alleviate this problem, an initial deposition of titanium (Ti) was used. Ti has excellent adhesion properties and is often used as an underlayer for subsequent Cu deposition [23].

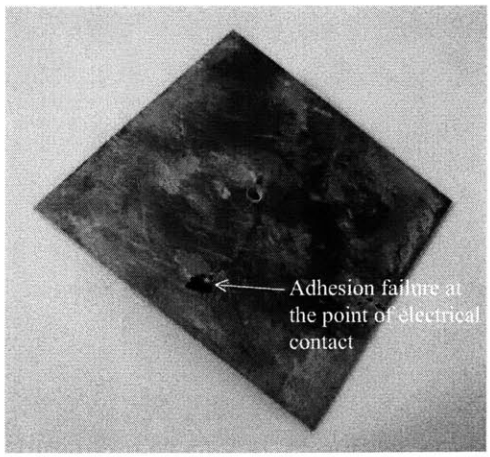


Figure 5-1: An example of adhesion failure at the FR4/copper interface after electroplating.

Copper Weight in oz./ft²	*Thickness in μm*
0.5	18
1	36
2	71
4	142

Table 5.1: Correlation between copper weight and thickness.

5.1.2 Sputtering Procedure

The aim was to replicate plating thicknesses in commercial applications. This is usually specified in copper weight per square foot and the relative thicknesses of some common weights are included in Table 5.1. The aim was to plate to thicknesses comparable with 1 and 2 oz. commercial copper deposition.

The procedure followed for the sputtering of the seed-layer was identical regardless of the SU-8 structure height or the desired plating thickness. The sputtering system was maunfactured by Materials Research Furnaces of Suncook, NH[1]. Once

[1]Materials Research Furnaces Inc.,Route 28 & Lavoie Drive, Suncook, NH 03275. Phone: (603) 485-2394

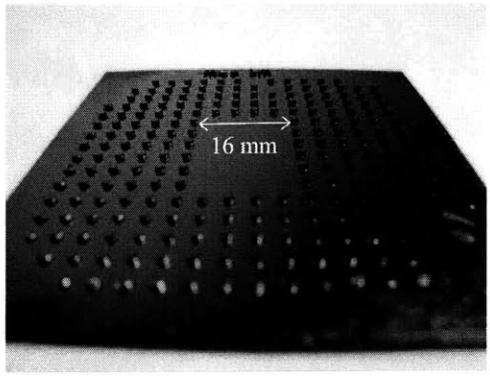


Figure 5-2: An example of successful copper seed-layer deposition by sputtering.

the substrate was placed in the chamber, the pressure was dropped below 3 $\times 10^{-6}$ Torr. After cleaning both the Ti and Cu targets, to ensure no contamination from previous processing, the board was "ashed" in the same way as before the SU-8 processing stage, but this time with Ar instead of O_2. This is thought to remove any moisture adhering to either the FR4 or SU-8 while not affecting the adhesion at the interface between the two materials. The process takes 10 minutes at an RF input power of 150 W. The next step is the sputtered deposition of Ti. This is done at 350 W using alternating pulsing of the sputterer: 1 minute on, one minute off. The total "on" time is 10 minutes so that the process takes 20 minutes in total. The thickness of Ti deposited in this time was measured to be 250 $\mathring{A}$ [2].

The Cu seed-layer is deposited next. This takes place in the same "one-minute on, one-minute off" manner, with a total "on" time of 20 minutes. The input power is lowered to 150 W in this case. This led to a measured copper thickness of 4000 $\mathring{A}$. Once deposition of the Cu was complete, the chamber was restored to room pressure and the boards removed immediately to the plating bath for electroplating. An example of successfully sputtered 800μm SU-8 structures is shown is Fig. 5-2.

[2] $1\mathring{A} = 1 \times 10^{-10} m$.

Parameter	*Nominal*	*Range*
Cu concentration	17 g/L	15-19 g/L
Cu sulfate	67 g/L	59-75 g/L
Sulfuric acid	170 g/L	150-225 g/L
Chloride Ions	70 mg/L	50-90 mg/L
Temperature	24°C	21-27°C

Table 5.2: Operating conditions for *Cu* plating.

5.2 Electroplating

Electroplating is the coating of one metal on the surface of another using electrolysis. Electroplating makes use of an electrolytic cell where electrical charge is used to bring about a chemical change. This electroplating bath is a commercial solution purchased from *Enthone Inc.*[3] The solution is commonly used for semiconductor applications in which high aspect ratio plating is desired. The solution operating conditions are detailed in Table 5.2.

The solution contains less than 80% water, less then 20% sulfuric acid and less than 10% copper sulphate. Organic additives in the solution are proprietary to *Enthone.* For *Cu* sulphate solutions, a phosphorized *Cu* anode (0.04 to 0.06% *P*) is required. Larger anode-to-cathode spacing gives better uniformity of deposition [26]. The spacing in this bath is approximately 20 cm. The single anode is placed in a woven polypropylene anode bag in order to prevent *Cu* chips and particles from the anode from contaminating the bath. The bath is shown in Fig. 5-3. A secondary container was used, for safety purposes, to contain the entire setup. For the power supply, a dc current source, supplied by "Tektronix" and capable of sourcing a maximum of 2 A is used.

With an acid bath, the electrodes are placed in the aqueous solution of $CuSO_4$ and the power supply drives electrons from anode to cathode. The SO_4^{-2} ions migrate to the anode and resist oxidation because they are polyatomic ions. Since the anode

[3]http://www.enthone.com

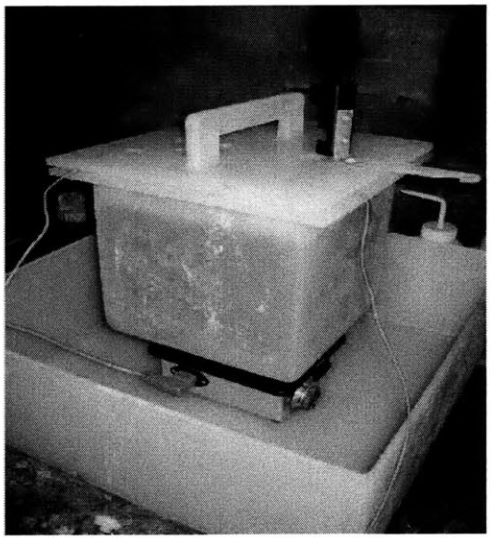


Figure 5-3: The electroplating bath was contained in a teflon container.

is not inert, but is pure copper, it undergoes oxidation. Cu^{+2} ions from solution migrate to the cathode, undergo reduction, and deposit on the sputtered substrate. The arrangement is highlighted in Fig 5-4.

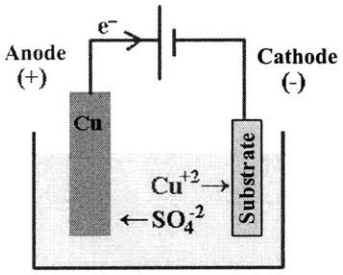


Figure 5-4: Illustration of sulfuric acid bath electroplating with active copper electrodes.

By elementary stoichiometric analysis of the chemical reactions involved, the approximate thickness of deposited copper can be estimated. Such analysis is found in any electrochemistry text (e.g. [25], [24]) and is not included in full here. Instead, the effective chemical reaction at the cathode is summarized in Equations 5.1 and 5.1,

where each Cu atom from the anode loses two electrons and the positively charged Cu ions migrate to the cathode where they are deposited as solid Cu. The thickness of the Cu deposition is given by Equation 5.3, where:

t = Cu thickness in cm

M_w = atomic weight of Cu = 63.55 g

n = number of electrons per mole $CuSO_4$ = 2

F = Faraday constant = 26.8 Ampere-hours

A = Surface plating area in cm^2

D = Density of Cu = 8.92 g/cm^3

I = Current source in Amps

dt = Elemental plating time in hours

Anode Reaction:

$$Cu^0(s) - 2e^- \rightarrow Cu^{+2}(aq) \tag{5.1}$$

Cathode Reaction:

$$Cu^{+2}(aq) + 2e^- \rightarrow Cu^0(s) \tag{5.2}$$

$$t = \frac{M_w}{nFAD} \int Idt \tag{5.3}$$

Following extensive investigation of different current densities, a final a value of 450 mA was found to be appropriate. This corresponds to a current density per unit plating area of 0.775 A/dm^2. Higher densities were found to cause "current crowding" at the contact point of the board and subsequent etching of the deposited metals. Lower densities, while also successful, prolonged the plating process unnecessarily. Plating at 450 mA for 5 hours results in a theoretical plating thickness of 55 μm (as calculated from Equation 5.3) and later investigation showed that this estimation

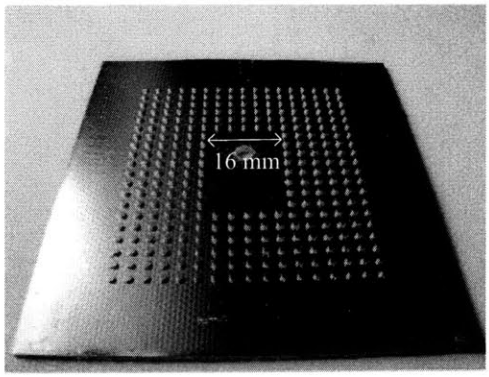


Figure 5-5: An example of successful electroplating of the board from Fig. 5-2.

was relatively accurate, within 10 or 15 μm. Upon completion of plating, the board is removed, rinsed thoroughly with deionized water and methanol and quickly blow-dried.

The bath was continually stirred during plating with a teflon-coated stirrer. The "Corning PC-310 Magnetic Stirrer" used has a stirring range between 150 and 1800 rpm. Typical stirring frequency was 150 to 200 rpm in this application. Agitation distributes ions more uniformly throughout the solution and promotes more uniform corrosion of the anode [25]. Another point worth noting is that the current source needs to be turned on before the board is immersed in the bath to prevent immediate etching of the copper by the acid solution. Successful electroplating to an estimated thickness of 55 μm of the board from Fig. 5-2 is shown in Fig. 5-5. Once electroplating is complete, boards are ready for subsequent testing and analysis.

Chapter 6

Pinfin Heatsink Testing

Having established that viaed heatsinks do not offer any significant improvement in performance over flat planar heatsinks, this chapter examines the performance of the pinfin heatsinks fabricated using the scaffolding technique. A matrix of heatsinks with varying heights, spacing and packing arrangements were investigated and their performance compared to a flat heatsink using the same approach in Chapter 3.

6.1 Optimized Pinfin Heatsinks

Numerous works have investigated optimal arrangements for cooling applications using pinfin heatsink arrangements [27]-[30]. However, none of these investigations focus on *Reynolds'* numbers in the range relevant to this investigation; estimated to lie between 50 and 150[1]. For example, the results outlined in [27] are true for a Reynolds' numbers in the range from 5×10^3 to 5.4×10^4, where the most general definition of the Reynolds' number is defined for by Equation 6.1 and where:

G_{max} = maximum mass flow rate per unit area in kg/m^2s

μ_{air} = dynamic viscosity of air in $Pa \cdot s$

[1]This is the range of "local" Reynold's number and is not to be confused with the "average" Reynold's number for an entire flat board which is given by Equation 3.4

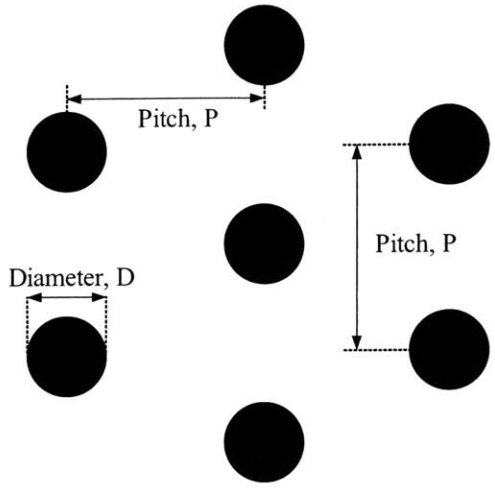


Figure 6-1: Hexagonally packed cylindrical pinfins. The optimal arrangement from [27] is when P = 2.5 D

D = pinfin diameter in m

$$Re = \frac{G_{max} D}{\mu_{air}} \tag{6.1}$$

This analysis ([27]) concludes that the optimal design for pinfin heatsinks is a hexagonal packing arrangement with an interfin spacing equal to 2.5 times the pinfin diameter. This means that arrangements similar to that shown in Fig. 6-1 are most desirable.

This is the approach taken in the experimental analysis that follows, although an inline packed board was also fabricated for comparison. Furthermore, since the conductive thermal resistance along each pinfin is designed to be negligible compared to the that along the plane of the board, the pins' height is maximized. Two heights were investigated: 800 μm and 1 mm, where it is to be expected that the higher pinfins will result in a lower thermal resistance. To test this, a TO-220 resistor is fastened to the board's center, as was shown previously in Fig. 3-4.

Board	*Packing*		*Pitch* [mm]			*Pin height* [mm]	
	Inline	Hex	2.75	3	3.25	0.8	1
J	×	×	×	×	×	×	×
K	×	√	×	√	×	√	×
L	√	×	×	√	×	√	×
M	×	√	√	×	×	√	×
N	×	√	×	×	√	√	×
O	×	√	×	√	×	×	√

Table 6.1: Details of boards used to investigate pinfin heatsink optimization. A check mark indicates that the board has a specific characteristic. Board J is a simple flat heatsink.

6.2 Testing

In total, six boards were investigated to analyze the effect of:

1. Packing: Hexagonal and Inline.

2. Pinfin height: 800 μm and 1 mm.

3. Pinfin pitch: 3 mm, 2.75 mm and 3.25 mm.

In each case, the ratio of pin pitch to diameter is 2.5 and the specific boards' characteristics are given in Table. 6.1. Board J is a flat heatsink, used as a benchmark for the remaining boards. Each board is electroplated for an equal amount of time (5 hours) with an identical current of 450 mA. The estimated thickness of copper on each is 55 μm, as estimated by Equation 5.3. Each board is fastened with a 5.1 Ω TO-220 resistor and the input power is increased from 0 to 4 W. The interface between each resistor and heatsink is thermally greased and the temperature of the TO-220 case is recorded for each board. The results are shown in Fig. 6-2.

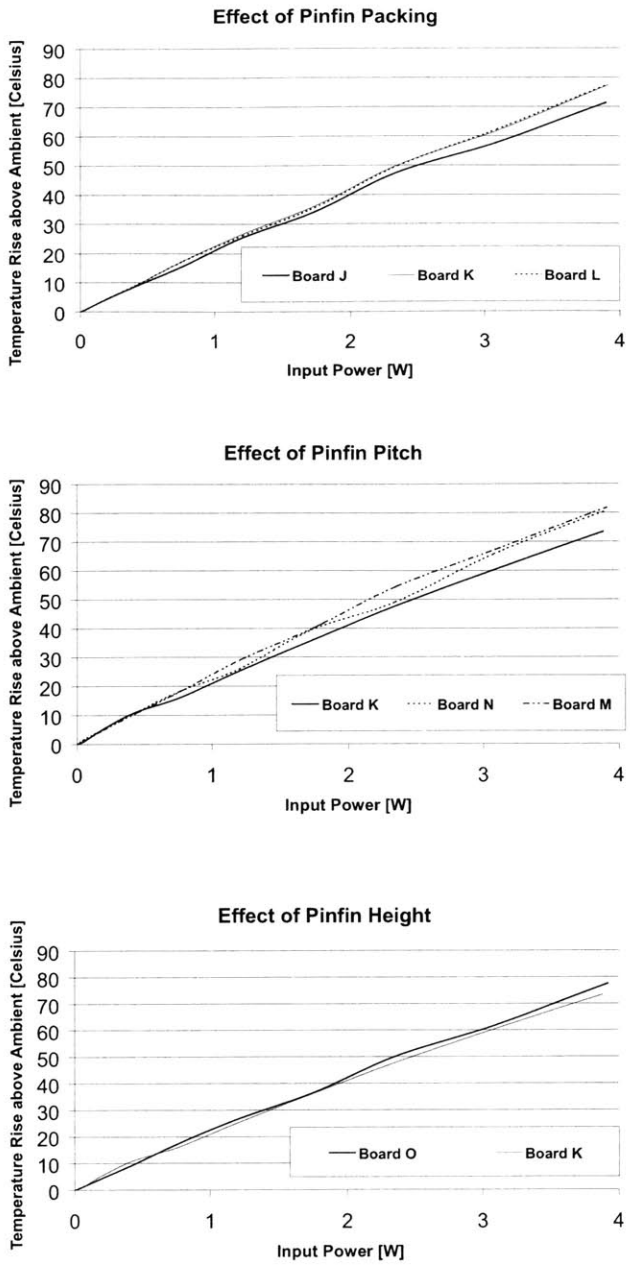


Figure 6-2: Results of the investigation of pinfin heatsinks. The results are counter-intuitive because the flat heatsink outperforms all the pinfin heatsinks.

6.3 Results Analysis

The first plot of Fig. 6-2 examines the effect of pinfin packing on heatsink performance. It is obvious that the hexagonally-packed *Board K* and the inline-packed *Board L* display almost identical performance. From this we might conclude that the packing arrangement of pins at this scale did not have a significant impact on heatsink performance. However, for reasons to be discussed, this can not be taken as a general conclusion. It should be noticed that the temperature of the resistor on the flat *Board J* is almost 10% lower than either of the pinfin heatsinks, although *Board K* has more available area for convective cooling. The reasons for this puzzling phenomenon are discussed in due course. Suffice to point out at this stage that an increase in cooling area resulting in poorer cooling effect is a counter-intuitive result.

The second plot investigates the effect of the pin pitch spacing, as highlighted in Fig 6-1. The lowest temperature resistor in this case is fastened to *Board K*, with a pitch of 3 mm. The next best is *Board N* (with a pitch of 3.25 mm), which shows marginally lower temperature than *Board M* (with a pitch of 2.75 mm) at the maximum input power level of 4 W. While subsequent analysis reveals that plating defects play a significant role in these results, this particular plot would lead one to conclude that there is an optimal pitch for each application. This coincides with our intuitive understanding that, as the pin pitch decreases the area available for convection increases. However, decreasing the pitch further will begin to impede the airflow in between the pinfins. This would lead to a shrouding effect where most of the air flows over the top of the pinfins and not through the space between them. In this analysis, the optimal spacing turns out to be 3 mm, with a corresponding pin diameter of 1.2 mm (given by $P = 2.5D$, as cited in [27])

The final plot examines the effect of pinfin height and, again, this plot is not what is expected. The higher 1 mm pinfins of *Board O* result in a higher temperature at the resistor case than the 0.8 mm pinfins of *Board K*, albeit a marginal difference

of 4-5% at maximum power. This is in spite of the fact that *Board O* results in an increase in the available area for convective cooling compared to *Board L*. Clearly further investigation was necessary to investigate the anomalies associated with these results.

6.4 Investigation of Anomalies

As part of an investigation into the anomalies highlighted in the previous analysis, a second electroplating step was attempted. This involved the selection of *Board J* (the flat heatsink), *Board L* (inline-packed 0.8 mm high pinfins) and *Board O* (hexagonally-packed 1 mm high pinfins). These three boards were electroplated to double their copper thickness, from an estimated 55 μm to 110 μm. This was accomplished with an identical current density of 0.775 A/dm^2, as in the previous plating step. Following this procedure, the performance of these three heatsinks was compared with their performance before the second plating step and the results are shown in Fig 6-3

After the second plating step, the *Boards J* and *O* show a marked improvement in heatsink performance. However, the 0.8 mm inline-packed heatsink of *Board L* shows little or no change, even with a doubling of the copper thickness on the surface.

In an attempt to investigate this unexpected result, these three heatsinks were die-sawed through across their diameter. This allowed for the examination of the structures under a microscope. The flat *Board J* revealed minor defects at the interface between the copper and the FR4 substrate but nothing significant or unusual. However, *Board O*, included in Fig. 6-4, showed significant cracking of the electroplated copper, especially at the recessed corners of the pinfins. The electroplated copper is clearly contracting on deposition and, while not entirely understood, this may be a result of the reduced charge densities in these areas. This is the converse of the "lightning rod" effect, where charge is seen to accumulate at convex corners. The photograph also allowed the verification of plating thickness, comparison to the

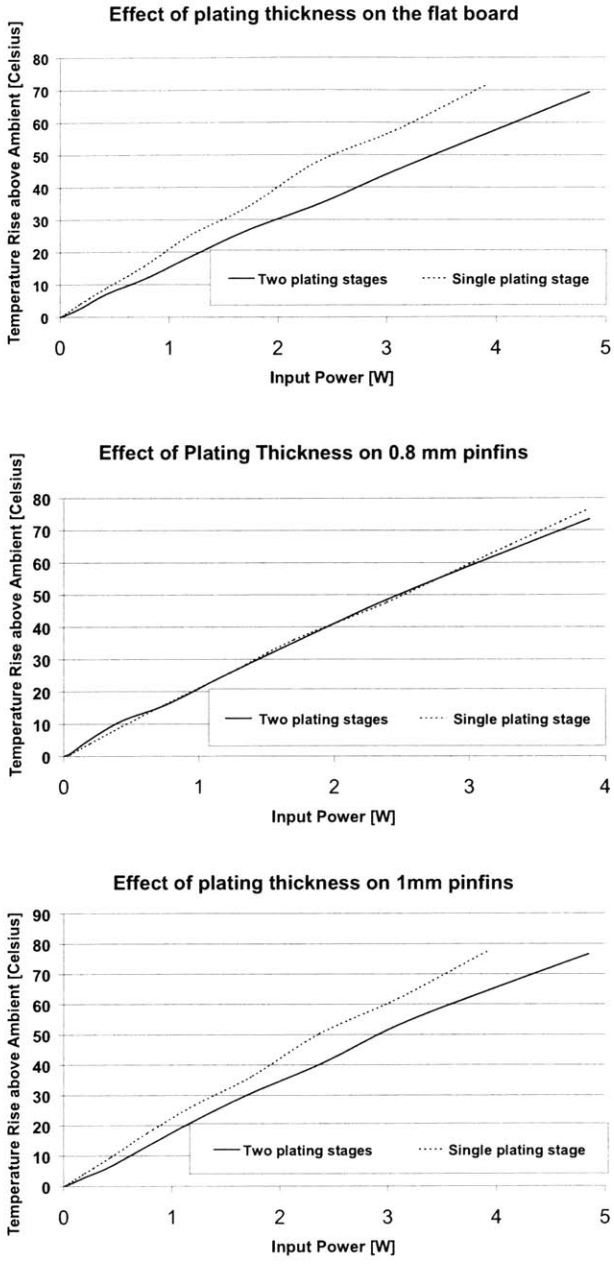


Figure 6-3: The effect of a second electroplating step on three of the boards was investigated. The selected heatsinks were *Boards J*, *L* and *O* from the previous investigation.

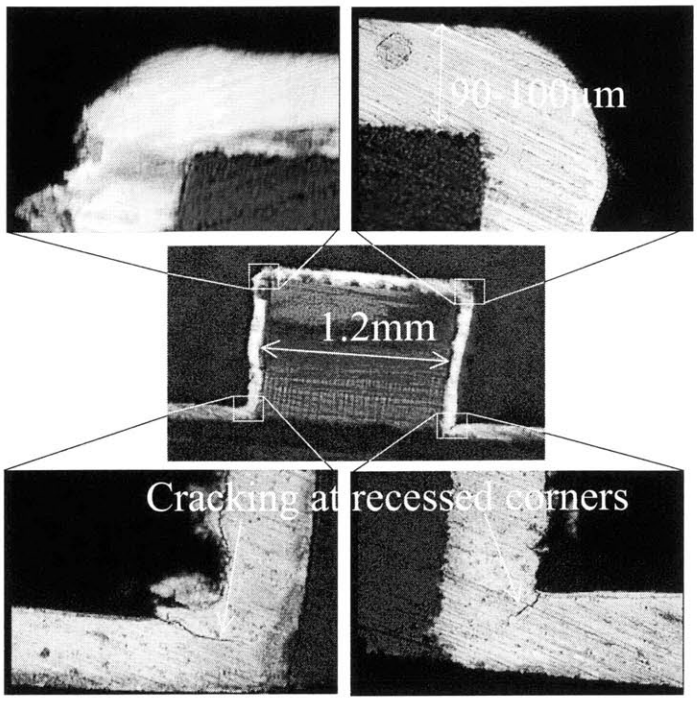


Figure 6-4: Examination of *Board O* after the second plating step. This shows significant cracking at recessed corners.

known pinfin diameter of 1.2 mm. The thickness, although it varied up to 30% in places, generally lay in the range of 90 to 100 μm after the second plating step. *Board O* also showed some adhesion failure between the two electroplated copper layers and examples of this are included in Fig. 6-5. However, the effect was isolated and is not thought to be as significant as the cracking in affecting heatsink performance.

A similar investigation of *Board L* was undertaken and the results, shown in Fig. 6-6 were quite enlightening. The cracking observed at the recessed corners of *Board O* is significantly worse on *Board L*. Also, cracking is not confined to the recessed corners, but is also present (albeit not as pronounced) at the convex corners at the top of the pinfins. A second effect that is noticeable on *Board L* is that the electroplated copper "creeps" under the SU-8 at the base of the pinfins, prising the SU-8 from the

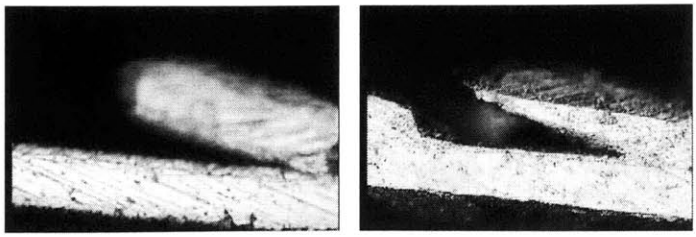


Figure 6-5: Adhesion failure between the two copper layers of *Board O* after the second plating step.

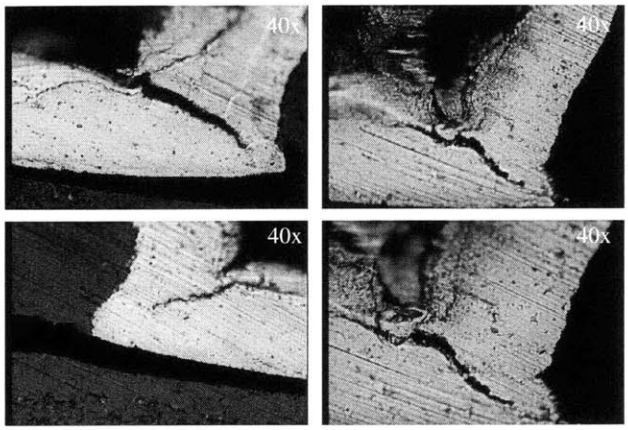


Figure 6-6: Failure mechanisms in the electroplated copper of *Board L* after the second plating step.

substrate as it does so. A clear void is visible in Fig. 6-7 between the SU-8 and the FR4. Finally, there is evidence of the adhesion failure at the SU-8/FR4 interface propagating along the board, as shown in Fig 6-8, and leading to further voids along the copper/FR4 interface. These defects help explain the menial improvement in heatsink performance of *Board L* after the second plating step.

It would appear that in the case of both the pinfin heatsinks examined, there are varying degrees of cracking at the recessed corners of the pinfins. On *Board L* this accounted for up to an 80% reduction in the cross-sectional area available for conduction of heat up the pinfin. This effect means that, in some cases, the pinfins

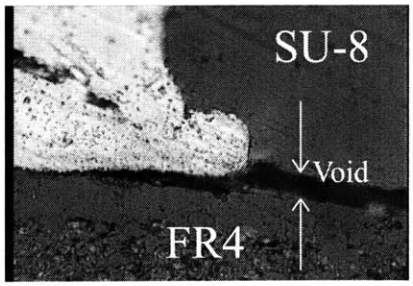


Figure 6-7: "Creep" of electroplated copper lifts the SU-8 from the substrate.

are virtually isolated (electrically as well as thermally) from the flat portion of the board so that the pinfins are inhibiting, rather than aiding, the conductive heat flow across the heatsink. This is why the flat *Board J*, which does not suffer from these cracking defects, consistently outperforms the pinfin heatsinks in this application.

Having concluded the investigation of the pinfin heatsinks fabricated using the scaffolding process, we have clearly not demonstrated the full potential of the technique in the application. However, the presence of defects arising during the electroplating step should not be expected in a commercial plating process and the problem might well be remedied by the replication of industry practices. These include "pulse-reverse copper plating"([31], [32]) and the use of multiple cathode connections. It is still to be expected that, in the absence of the plating defects that have been encountered, the pinfin heatsinks will offer significant improvement over the flat device at dissipating heat from the board's surface.

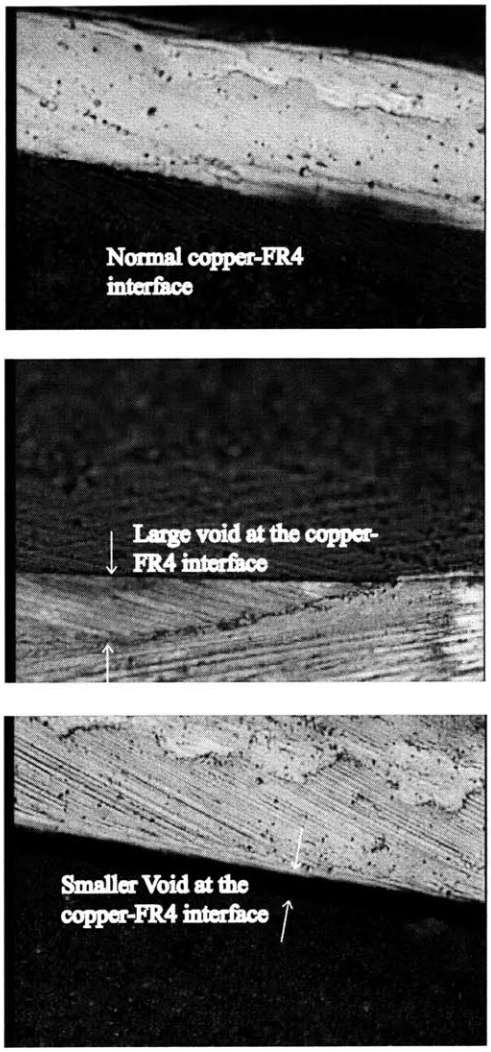


Figure 6-8: Propagation of adhesion failure along the copper/FR4 interface.

Chapter 7

Conclusions

7.1 Accomplishments

The purpose of this thesis was to investigate a new technique that enables the fabrication of ultra-high passive components for power electronics applications. These components are fabricated using a scaffolding technique which employs photolithographic and metal deposition procedures.

The scaffolding technique uses SU-8, an ultra-thick photoresist developed for high aspect ratio MEMS applications, as a 3D scaffold for electroplated passive structures. Structures where scaffolding is thought appropriate include heatsinks, inductor windings, EMI shielding and busbars. After poured deposition of the SU-8, there follows a standard photolithographic process of exposure and development with intermittent baking. Development of structures with heights exceeding 1 mm was accomplished. Metal deposition took place in two stages, (i) seed-layer deposition and (ii) electroplating. The seed-layer, which was copper, was deposited by pulsed sputtering action, with an initial layer of titanium used to improve adhesion to the substrate. The electroplating stage increased the copper thickness to a level suitable for power electronics applications.

The principle application explored in the thesis was the use of the developed

structures as heatsinks for passive power electronics components. In particular, the heatsinking of a TO-220 resistor package was investigated in depth. Since the principal means of heat dissipation from a heatsink is by convection, the heatsink's performance can be improved in one of two ways; firstly, by increasing the coefficient of convective heat transfer, h (for example by the addition of forced airflow) and secondly, by increasing the surface area available for convection. This investigation focusses on the second approach and looks at two means of increasing the cooling area; (i) vias and (ii) pinfins.

The effectiveness of viaed heatsinks is analyzed in depth in Chapter 2. The application focussed on the case temperature of the TO-220 resistor and examined how this changed with input power into the device. The conclusion of this analysis is that the addition of area by the introduction of vias does not offer a significant advantage over a flat board. This is because the vias impede the conductive heat flow across the board to the degree that this effect almost outweighs the benefit of increasing the area available for convection. This conclusion is supported by a combination of modelling and experimental results.

Having established that viaed heatsinks offer only minimal improvement in performance over a flat board, the investigation turned to the use of pinfin heatsinks. These heatsinks were fabricated using the scaffolding technique outlined in Chapters 4 and 5. An array of pinfin heatsinks were constructed and their performance compared to that of a flat board in the same manner as the viaed boards. An optimal pinfin pitch of 3 mm was established and the effect of packing arrangement was found to be negligible. However, the flat board outperformed all of the fabricated pinfin heatsinks, a result that correlated with neither our model or our intuition. Upon further investigation, it was found that the source of this anomaly lay in the presence of widespread cracking defects at the base of the pinfins. These defects resulted in a significant decrease in the cross-sectional area available for conduction up the pinfins, thus negating any advantage accruing from the extra area added by the pinfin

sidewalls. While this problem has yet to be resolved, it is not thought that it is significant enough to impede the application of scaffolding to heatsink applications in power electronics. It is still to be expected that, in the absence of the plating defects that have been encountered, the pinfin heatsinks will offer significant improvement over the flat device at dissipating heat from the board's surface.

7.2 Future work

Clearly, there is outstanding work needed to resolve the plating defects which mitigated against the pinfin structures offering any improvement in the heatsinking application that was investigated. This work might include the use of "pulse-reverse copper plating" ([31], [32]) and multiple cathode connections. It should not be expected that these defects would occur in a commercial plating process.

The scaffolding technique would appear an excellent approach for the fabrication of other structures that were previously only manufactured on the board's surface. As mentioned previously, these include EMI shielding, inductor windings for planar magnetics and busbars. For example, busbars might be developed with sidewalls so that they represent a smaller footprint on the circuit board. Finally, with the onset of integrated passive components, such as capacitors and air-core inductors, into multilayer printed circuitry, smaller component size will be the overriding industry concern. We might conclude by noting that the scaffolding technique is a promising addition to the circuit designer's toolbox in accomplishing this goal.

Appendix A

Thermal Resistance of a Flat 2 Sq. Inch Board.

This notebook file was generated in **Mathematica 4.1**, available from Wolfram Research. It has been modified from its original formatting for the purposes of presentation.

We begin by defining the constants relevant to the flat board of Fig. 3-4. All distance dimensions are in *S.I.* units. L is the board length in meters and A is the board area.

```
L = 2*0.0254;
A = L^2;
```

The Convective Heat Transfer Coefficient, h has been estimated from examination of the board and ambient conditions. Its calculation is detailed in the thesis.

```
h = 14.35;
```

Copper plating thickness and the FR4 thickness are recorded.

```
tcopperTop = 5.588*10^-5;
tFR4 = 0.0015875;
```

The coefficients of conductive heat transfer are available in any Heat Transfer text.

```
kcopper = 400;
kFR4 = 0.800;
kair = 0.024;
```

Each board is decomposed into 4 parallel-connected fins, each an isosceles triangle of length $\frac{L}{\sqrt{2}}$. Their tips meet at the board's center so that each triangle has base angles of 45^o and a tip angle of 90^o. The board lies in thc $\{x,\ z\}$ plane, where the dominating heat path is assumed to lie in the x axis, pointing from the board's center and bisecting the board's edge at right angles. The temperature variations along each fin's z axis is not considered.

Each fin in then divided into serial sections, numbered **1** to **Num**, where section 1 is nearest to the center and **Num** lies at the board edge. Each section has a length **ls**. Each section has a conductive resistance in the x direction and a convective resistance to the ambient. The conductive resistance is estimated at the mean length along the section, while the convective resistance assumes all the surface area is available for convection. The resulting resistance, seen at the board's center *(x=0)* is estimated from the general form for a ladder network.

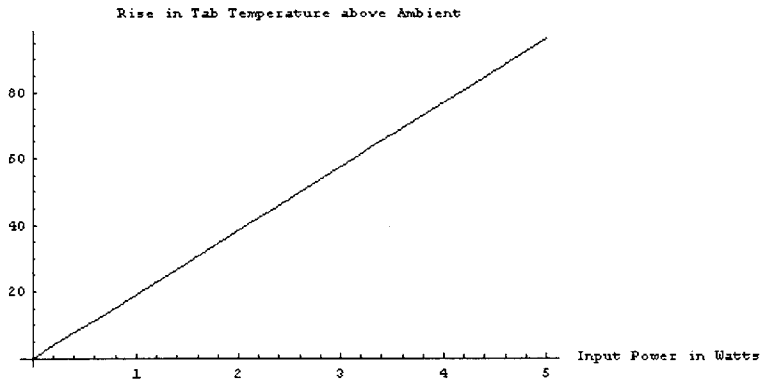
```
Clear[i, R, Rconv, Rcond, Num];
Num = 10000;
ls = L/(2*Num);
Rcond[i_]:= 1/((2i - 1)*(tcopperTop*kcopper + tFR4*kFR4));
Rconv[i_]:= 1/(h*ls^2*(2i - 1));
R[Num] = Rcond[Num] + Rconv[Num];
```

```
For [i = Num, i > 0,
R[i - 1] = Rcond[i - 1] + (Rconv[i-1]*R[i])/(Rconv[i-1]+R[i]);
i-- ]
Rboard = R[1]/4
```

Output ***82.016***

Having estimated the board's thermal resistance to the ambient temperture, the TO-220 tab temperature can be estimated, where the thermal resistance due to losses is estimated to be 25°C/W to coincide with experimental results. The resistance from the case to the heatsink is estimated to be 1°C/W. This is a conservative estimate for a greased interface, based on the work in [15]. The purpose is not an absolute model but a means of comparing a flat and viaed board.

```
Clear[PowerIn, RcaseAmb, RsinkAmb, Tcase];
Rlosses = 25;
RcaseSink = 1;
Tcase = (Rlosses*(RcaseSink+Rboard))/(Rlosses+(RcaseSink+Rboard)) * PowerIn;
p1 = Plot [Tcase, {PowerIn, 0, 5},
PlotLabel -> ''Rise in Tab Temperature above Ambient'',
AxesLabel -> {''Input Power in Watts'', '' ''} ];
```


Rise in Tab Temperature above Ambient
80
60
40
20
1
2
3
4
5
Input Power in Watts

Appendix B

Thermal Resistance of a Viaed 2 Sq. Inch Board.

Similarly to the file of Appendix A, this notebook file was generated in **Mathematica 4.1**. The general constants are the same as for the flat board case, with the addition of the plating thickness in the via. This information was detailed by the supplier.

```
L = 2*0.0254;
A = L^2;
```

Convective Heat Transfer Coefficient:

```
h = 14.35;
```

Copper plating thickness and the FR4 thickness are recorded.

```
tcopperTop = 5.588*10^-5;
tcopperVia = 2.54*10^-5;
tFR4 = 0.0015875;
```

The coefficients of conductive heat transfer are available in any Heat Transfer text.

```
kcopper = 400;
kFR4 = 0.800;
kair = 0.024;
```

Each board is decomposed into 4 parallel-connected fins, as for the flat board case and each fin in then divided into serial sections, numbered **1** to **Num**, like before. In this case, however, the incremental conductive and convective resistances are not continuous functions of x, as was the case for the flat board. Instead, the function will change in passing from viaed to unviaed sections of the board. Lengths **l1** to **l9**, are used to define these discontinuities.

```
l1 = 6.858*10^-3;
l2 = l1 + 1.524*10^-3;
l3 = l2 + 3.556*10^-3;
l4 = l3 + 1.524*10^-3;
l5 = l4 + 3.556*10^-3;
l6 = l5 + 1.524*10^-3;
l7 = l6 + 3.556*10^-3;
l8 = l7 + 1.524*10^-3;
l9 = l8 + 1.778*10^-3;

Clear[i, R, Rconv, Rcond, Num];
Num = 10000;
ls = L/(2*Num);
DFR4 = 0.003556 - 2*2.54*10^-5;
Acopper = 2*(tcopperTop + tFR4) + 2*(tcopperVia*DFR4);
```

```
AFR4 = DFR4*tFR4;
```

Next, the discontinuous expressions for the conductive and convective resistances in each section are defined.

```
Rcond[i_] := Which[
IntegerPart[2*Num*l1/L] < i <= IntegerPart[2*Num*l2/L],
3*ls/((kcopper*Acopper) + (kFR4*AFR4)),
IntegerPart[2*Num*l3/L] < i <= IntegerPart[2*Num*l4/L],
5*ls/((kcopper*Acopper) + (kFR4*AFR4)),
IntegerPart[2*Num*l5/L] < i <= IntegerPart[2*Num*l6/L],
7*ls/((kcopper*Acopper) + (kFR4*AFR4)),
IntegerPart[2*Num*l7/L] < i <= IntegerPart[2*Num*l8/L],
9*ls/((kcopper*Acopper) + (kFR4*AFR4)),
True,
1/((2i-1){(kcopper*tcopperTop) + (kFR4*tFR4)})
]
```

For the case of the convective resistances, the values are related to the coefficient of heat transfer, h, for the case of the flat board. However due to the reduced top area as well as the lower air turbulence within the vias, its value is expected to be significantly lower for the viaed board. To correlate with the observed results, the value is chosen to be half the original value (from the flat board) on the top surface and quarter the original value in the vias.

```
As = 2*ls(tFR4 + tcopperTop) + ls(DFR4 + 2*tcopperVia);
Rconv[i_] := Which[
IntegerPart[2*Num*l1/L] < i <= IntegerPart[2*Num*l2/L],
```

```
1/(h/4*As*5),
IntegerPart[2*Num*l3/L] < i <= IntegerPart[2*Num*l4/L],
1/(h/4*As*7),
IntegerPart[2*Num*l5/L] < i <= IntegerPart[2*Num*l6/L],
1/(h/4*As*9),
IntegerPart[2*Num*l7/L] < i <= IntegerPart[2*Num*l8/L],
1/(h/4*As*11),
True,
1/((2i-1)h/2*ls^2)
]
```

As in the case of the flat board, the resistance seen from the TO-220 case is seen by evaluation of the ladder network and the overall board resistance is found by the parallel combination of 4 fins.

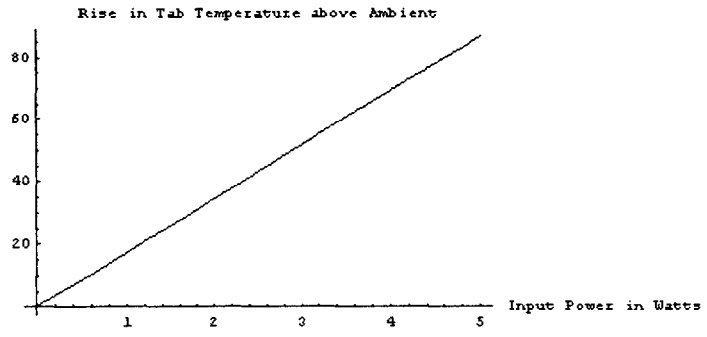
```
R[Num] = Rcond[Num] + Rconv[Num];
For[i = Num, i > 0,
R[i - 1] = Rcond[i - 1] + (Rconv[i-1]*R[i])/(Rconv[i-1]+R[i]);
i--]
Rboard = R[1]/4
```

Output ***55.6423***

As in the case of the flat board, thermal resistance due to losses is estimated to be 25°C/W to coincide with experimental results and the resistance from the case to the tab is estimated to be 1°C/W.

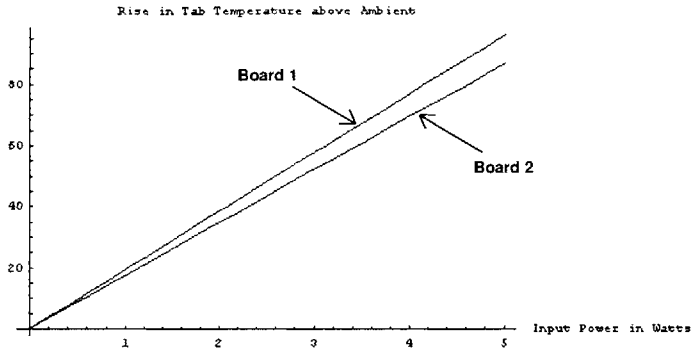
```
Clear[PowerIn, RcaseAmb, RsinkAmb, Tcase];
```

```
Rlosses = 25;
RcaseSink = 1;
Tcase = Rlosses*(RcaseSink+Rboard)/Rlosses+(RcaseSink+Rboard) * PowerIn;
p2 = Plot [Tcase, {PowerIn, 0, 5},
PlotLabel -> ''Rise in Tab Temperature above Ambient'',
AxesLabel -> {''Input Power [W]'', '' ''} ];
```



Combining plots, we can directly compare the power-temperature curves for the two boards with the lower plot corresponding to the viaed board. Clearly, the viaed board is fractionally better at dissipating the generated heat and this correlates closely with the recorded results. However, the approach is only applicable in niche applications, particularly with high volume airflow perpendicular to the board surface, which would make full use of the vias. The effect of the increased via density of Board *3* is investigated by increasing the available surface area for convection and further limiting the conductive path in the x direction. This analysis was not included in the plot because there was very little difference in the plots corresponding to Boards *1* and *2*.

```
Show[p1, p2]
```


Rise in Tab Temperature above Ambient
Board 1
Board 2
80
60
40
20
1
2
3
4
5
Input Power in Watts

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