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The Fabrication and Market Analysis of Lattice Mismatched Devices

by

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Submitted to the Department of Materials Science and Engineering and the Sloan School of Management in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Materials Science and Engineering
and
Master of Science in Management
at the
Massachusetts Institute of Technology
June 2004

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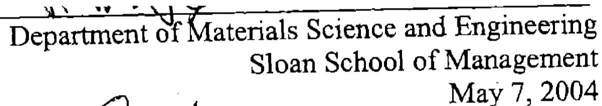
Signature of Author: 
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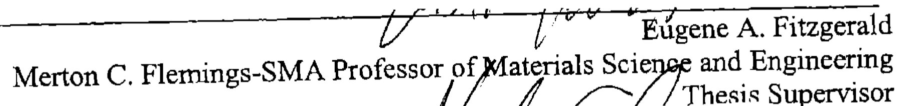
Certified by: 
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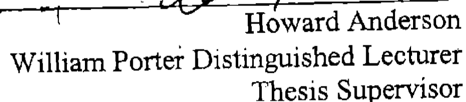
Certified by: 
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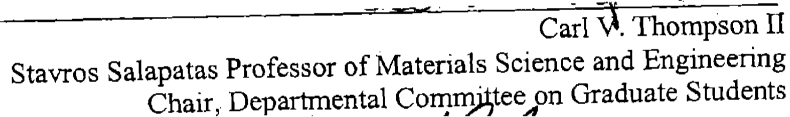
Accepted by: 
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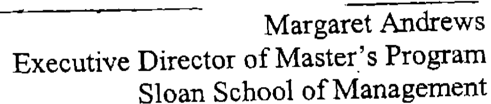
Accepted by: 
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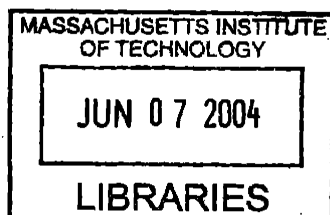
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The Fabrication and Market Analysis of Lattice Mismatched Devices

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ABSTRACT

Lattice mismatched semiconductor substrates provide a platform for higher performance semiconductor devices. Through epitaxial growth on GaAs, the lattice constant of the film can be expanded resulting in a desired $In_xGa_{1-x}As$ film on which devices can be fabricated. The resulting device exhibits enhanced performance characteristics not achievable on the initial substrate. A self-aligned mesa structure process was developed to fabricate a prototype HBT device utilizing an $In_xGa_{1-x}As$ lattice mismatched semiconductor substrate. The self-aligned mesa process eliminated the need for complicated metal etch steps by using a lift-off process and deposited contact metal as an etch mask. Selecting etches that highlight the selectivity of the device layers was critical to the success of the process.

In addition to developing a process to fabricate a device, a market analysis is performed of the possible application space of the technology and derived products. In assessing the feasibility of the possible products, two main areas were addressed, the markets and the competition within each market.

The technology innovation has the ability to attract a variety of markets already served by compound semiconductors. The possible markets and the competition, companies and other materials, already serving the markets are identified and characterized. To determine what markets would be attractive, the full landscape of semiconductor applications is developed. After which we were able to list the specifications and customer needs of each application as well as what materials and what companies were serving these markets. The expected performance for the innovation was then benchmarked against what we projected for the current providers in each application space. Through the benchmarking process we were able to highlight markets in which we had a clear performance and cost advantage.

Thesis Supervisor: Eugene A. Fitzgerald
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Section 1: Introduction

In the past, semiconductor companies have relied upon advancements in photolithography tools to meet new technology specifications. Next generation photolithography tools allowed companies to continue to use existing materials and processes with only moderate modifications to meet next generation device specifications. As the critical dimensions of devices continued to decrease, the needed wavelengths from the photolithography tools also must decrease. Despite much disagreement, the industry appears to be rapidly approaching the point where next generation photolithography tools will not be able to provided the needed critical dimensions. A radical solution is therefore needed to continue to meet the device performance of next generation technologies. This has led to the research in material changes/enhancements to meet the next generation device requirements. University researchers and company R & D departments are now engineering materials to introduce into semiconductor technologies that will achieve the performance specifications, hopefully with the use of standard photolithography processes.

This thesis addresses the continued need for increased performance in the high frequency semiconductor industry, typically dominated by compound semiconductors, and the elimination of costs associated with new tooling for larger sized wafers and new substrate materials. Given the new innovation, the thesis answers to what markets is the innovation most attractive.

Through forecasting the development of competitive material technologies and companies, attractive markets are highlighted as well as the advantages in cost and performance in those markets. In defining attractive markets and applications, a

comparison was made between existing technologies serving the particular space as well as possible future competing materials. To verify our performance advantage, a physical device was fabricated to measure the performance enhancements of the material innovation.

It was found that in order to avoid the penetration of silicon based processes our technology needs to focus on the high performance millimeter wave market. Silicon processes such as SiGe, CMOS, and Si BiCMOS processes are continually extending into higher frequency applications. The main driver for this penetration is cost. Silicon devices can be provided at much lower material and processing costs. At millimeter wave frequencies, performance is the driver. The presented technology outperforms silicon and gallium arsenide based technologies today and in the future.

Section 2: Epitaxial Growth of Lattice Mismatch InGaAs

To transition from a GaAs substrate to the InGaAs devices layers, we utilized a relaxed graded buffer technology developed in our research lab. This section describes the fundamentals of the growth process.

2.1 Lattice Mismatched Epitaxy

Through epitaxial growth, the lattice constant of the GaAs substrate is relaxed by incrementally increasing the In content in the deposited film. The deposited film is strained to match the lattice constant of the underlying film. The deposited film is characterized as either coherent, totally elastically strained, or some of the strain is accommodated by a misfit dislocation at the interface. The misfit, f, is defined[1] as

$$f = \frac{a_s - a_f}{a_f} \tag{2.1}$$

where a_s and a_f are the lattice parameters of the substrate and film, respectively. As a result, f can be either positive or negative. A negative f corresponds to compressive strain in the film and a positive f indicates tensile strain. The misfit is further defined as

$$f = \varepsilon - \delta \tag{2.2}$$

where ε is the amount of lattice mismatch accommodated through elastic strain of the film, and δ is the amount accommodated through plastic strain of the film. Plastic strain accommodation is through dislocation nucleation. In a totally elastically strained film $\varepsilon = f$ and in a relaxed film $\delta = f$. Figure 2.1 demonstrates the incorporation of a misfit into the epitaxial film.

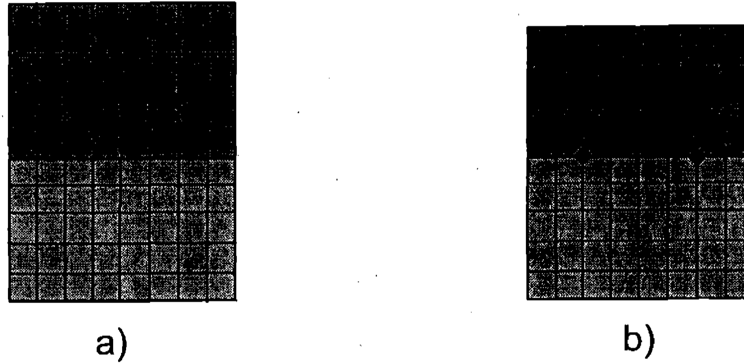


Figure 2.1: a) Fully strained epitaxy, and b) partially relaxed epitaxy, $a_s < a_f$.

Energy is needed to form a misfit, therefore there must be a favorable environment in order to form a misfit dislocation. It follows that there is a region where there is not sufficient enough energy to nucleate a misfit. Above a critical thickness, h_c, the film will begin to deform plastically to relieve the strain through the formation of misfit dislocations. The dislocations are formed along the film interface with the substrate. Below h_c, the film will be completely strained to match the lattice parameters of the substrate. This critical thickness has been theoretically defined to be

$$h_c = \frac{D\left(1 - \nu\cos^2\alpha\right)\left(b/b_{eff}\right)\left(\ln\frac{h_c}{b} + 1\right)}{Yf} \tag{2.3}$$

where D is the average shear modulus of the interface, ν is the Poisson ratio of the film, b is the magnitude of the Burgers vector of the dislocations, α is the angle between the Burgers vector and the dislocation line, and Y is the film's Young's modulus[2]. The critical thickness is explicitly defined as the thickness at which the strain energy released by misfit dislocations equals the energy required to form the misfit dislocations. Due to the recursive nature of the equation, the critical thickness is only determined through iterative experimentation.

Misfit dislocations in a film act to degrade electrical transport of carriers in both the vertical and parallel directions to the interface. Historically, mismatched epitaxial films have been used for the mismatched interface or as a template for subsequent mismatched device layers. Our research is interested in the second application. In these device applications, threading dislocations is of primary concern. Since a dislocation cannot terminate within a crystal, dislocations will propagate through the film to its surface, forming threading dislocations. These threading dislocations can thus propagate up to the active device layers resulting in a degradation of device performance. Threading dislocations densities on the order of 10^6 cm^{-2} or less are required for sufficient optical device performance. Therefore, the ability to control misfit dislocation during epitaxy of mismatched layers is critical to achieve acceptable device performance. Figure 2.2 illustrates threading dislocations.

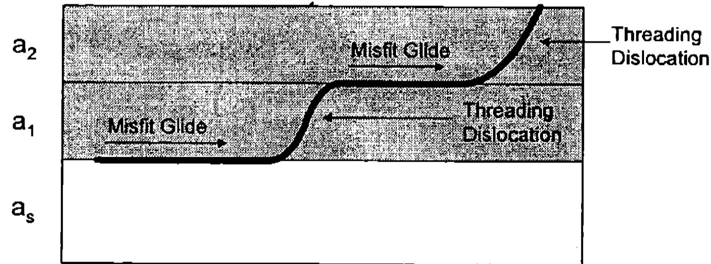


Figure 2.2: Misfit dislocation glide and threading dislocation propagation.

In our material system of interest, III-V semiconductors, the crystal system is a zinc-blend where the dislocation slip system is {111}<110>. Our system is fabricated on a <100> growth direction. Therefore, misfit dislocations will be in the <110> directions on the (100) interface plane. Optically this results in a crosshatch pattern in the heteroepitaxial layers in thicknesses above the h_c. In structures with a low misfit (< 2%), 60° dislocations are dominant. These dislocations are so-called 60° dislocations because their Burgers vector is 60° from the <110> interface dislocation line. In high misfit

systems, edge dislocations, 90° dislocations, form at the interface. Given the (100) mismatch interface, one would have expected the Burgers vector of these dislocations to be along the interface and perpendicular to the dislocation line. This is not the case because the edge dislocation's glide plane does not correspond to the primary zinc-blend slip system[2].

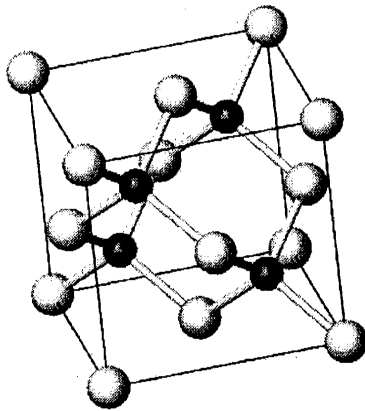


Figure 2.3: Zinc-blend crystal system

2.2 Dislocation Nucleation

In order to control the misfit dislocation, one must understand the nucleation of the dislocations. Here I offer a brief introduction to the four types of dislocation sources: fixed defects, heterogeneous and homogeneous surface half-loop nucleation, and dislocation interactions and multiplication[3,4].

- Fixed Defects: Existing fixed defects in the substrate will nucleate dislocations in the deposited film. Such defects include particulates, impurities, or scratches present prior to growth. Fixed defects typically scale with the area of the growth surface. Threading dislocations from pre-deposited films will also act as fixed defect sources and will be translated into the newly deposited layer. As noted earlier in this section, dislocations cannot terminate within a crystal[3].

- Heterogeneous and Homogeneous Half-Loop Nucleation: Heterogeneous and homogeneous sources can also occur on the substrate surface and induce the nucleation of a dislocation. A heterogeneous source would be a particulate from the reactor that has landed on the substrate before growth. A homogeneous source would be similar but would match the growth material system.
- Dislocation Interactions and Multiplication: In high misfit systems, dislocations are likely to have the same sign 60° Burgers vector. In this case the two dislocations will repel each other increasing the threading dislocation density. Alternatively, dislocations with complementary 60° Burgers vectors will combine to form a new threading dislocation. This new threading dislocation is likely to become a permanent threading dislocation. The previous two scenarios describe dislocation interactions. Dislocation multiplication will increase both threading and misfit dislocation densities. Perpendicular misfit dislocations with the same Burgers vector will create two threading dislocations. The created threading dislocations can then create misfit dislocations on the interface[3,5].

2.3 Relaxed Graded Buffers

If a deposited film and substrate have a large lattice mismatch, a large number of dislocations will form to accommodate the strain. To avoid a large dislocation density, a method was developed to accommodate the strain through several deposited epitaxy interfaces.

The method known as relaxed, graded buffer epitaxy incrementally varies the composition of the deposited film from the substrate (or pre-deposited film) to maximize strain accommodation at each layer. During growth of the relaxed graded buffer,

dislocations already in the substrate will act as misfits to relieve strain at the mismatch interface. These misfit dislocations then propagate up through the film and terminate at the surface. These dislocations may also terminate at the free surface at the edge of the substrate. The threading dislocations that terminate at the surface then serve as the needed dislocations to relieve the strain in the next epitaxial layer. The theory is that the existing dislocations can accommodate the strain in the next epitaxial layer and no new dislocations are formed. The resultant glide of the misfit dislocations at the mismatch interface result in the crosshatched pattern, seen in Figure 2.3, characteristic of a relaxed, graded buffer.

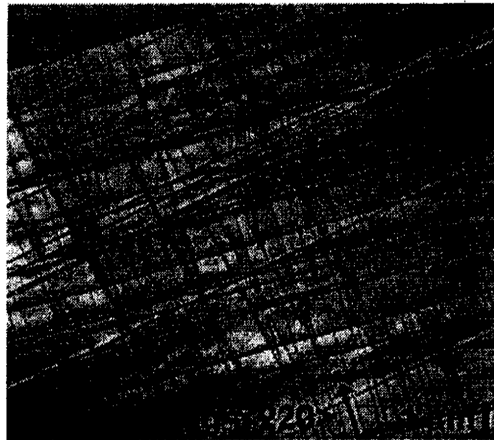


Figure 2.4: PVTEM of an InGaP graded buffer misfit dislocation array.[6]

2.4 Material System

We have decided to grade $In_xGa_{1-x}As$ on GaAs substrates. Figure 2.5 shows the grading path from GaAs to InAs along with the resultant energy gap and lattice constant. By increasing the In content in the GaAs, we are increasing the bad offset at the interface. Once the desired In content is reached, the device layers will be grown through lattice

matched epitaxy. Lattice matched devices such as these are called metamorphic structures since the lattice constant of the device layers differs from the substrate. I further describe metamorphic devices and design in Section 3.

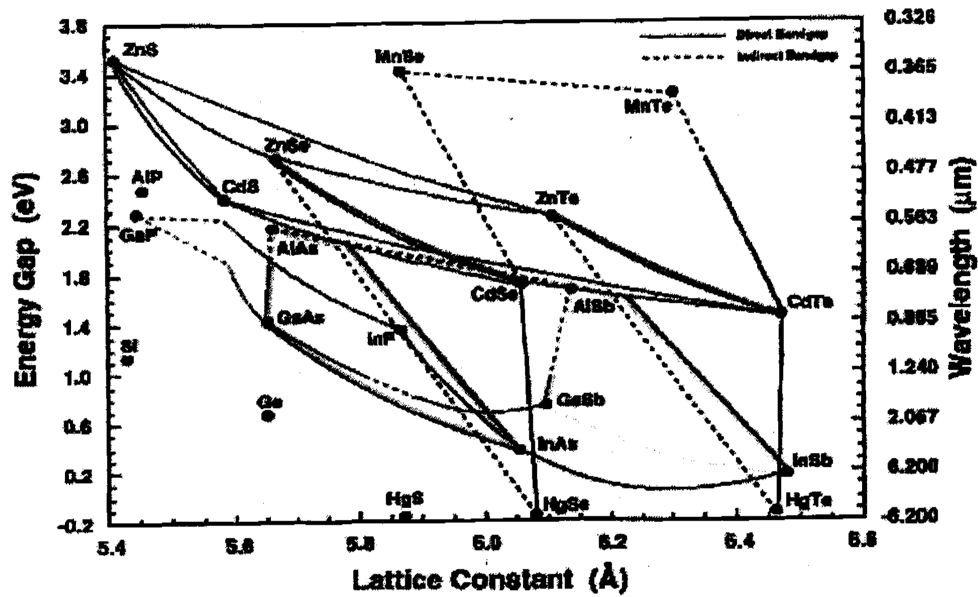


Figure 2.5: Energy band gap vs. lattice constant (Keremidas and Nahory, Bell Labs).

Section 3: Heterojunction Bipolar Transistors

The heterojunction bipolar transistor (HBT) is a very similar to the well known bipolar transistor (BJT). Each device structure is made up of an emitter region and a collector region that sandwich a base region to create two p-n junctions. Both types of devices are fabricated in either NPN or PNP configurations. From here forth, we will be focusing on the NPN transistors where electrons are the conducting carriers. This section assumes an earlier exposure to semiconductor devices and theory. There are many references available on this subject if more information is required. The author recommends Semiconductor Device Fundamentals by Robert F. Pierret.

3.1 HBT Basics

In a BJT, the device layers are made of the same material. Alternatively, HBTs utilize varying bandgap materials. In an HBT, the emitter has a wider bandgap than the base material. This characteristic results in improved electron injection from the emitter to the base and allows the base to be doped much greater than the emitter. A highly doped base reduces the base resistance and decreases the transit time through the base, improving electrical performance. A lightly doped emitter minimizes the base-emitter capacitance. These improvements and the improvement on device performance are discussed later in the section.

Typical operation of the transistor is in forward-active mode, where the base-emitter junction is forward biased ($V_{BE} > 0$) and the base-collector junction is reverse biased ($V_{BC} < 0$). Electrons are injected from the emitter into the base, diffuse through the base, and are then swept into the collector by the electric field at the base-collector junction. The base material in the HBT is intentionally thin to ensure that all of the

electrons injected into the base are swept into the collector, eliminating any recombination. The base-emitter voltage V_{BE} controls the electrons injected independent of the base-collector voltage V_{BC}, as long as the junction is reversed biased. Therefore, the collector current is controlled by the base-emitter voltage and unaffected by the base-collector voltage. The result is that a small change in V_{BE} of base current has a large effect on the injected electron density and hence the collector current. The input signal is amplified.

Figure 3.1 shows the typical band structure for an NPN HBT in the forward-active mode. The figure depicts the major current flows along with the subcomponents as well as energy band offsets. The figure further illustrates the heterojunction at the base-emitter junction; note the larger energy gap emitter material. The use of a larger band gap emitter material reduces the hole back-injection from the base. The holes in the base traveling to the emitter see a much larger energy barrier than the electrons injected from the emitter to the base. Also depicted in the figure is a discontinuity in the conduction band at the base-emitter junction, labeled ΔE_C. This discontinuity is the result of an abrupt junction between the base and emitter materials. Since different bandgap materials are used, the bands do not match up at the interface like seen in homojunctions. The ΔE_C drives greater energy to inject the electrons into the base. The voltage required to begin electron injection into the base is called the turn-on voltage. By grading the material junction, the offset can be eliminated or reduced.

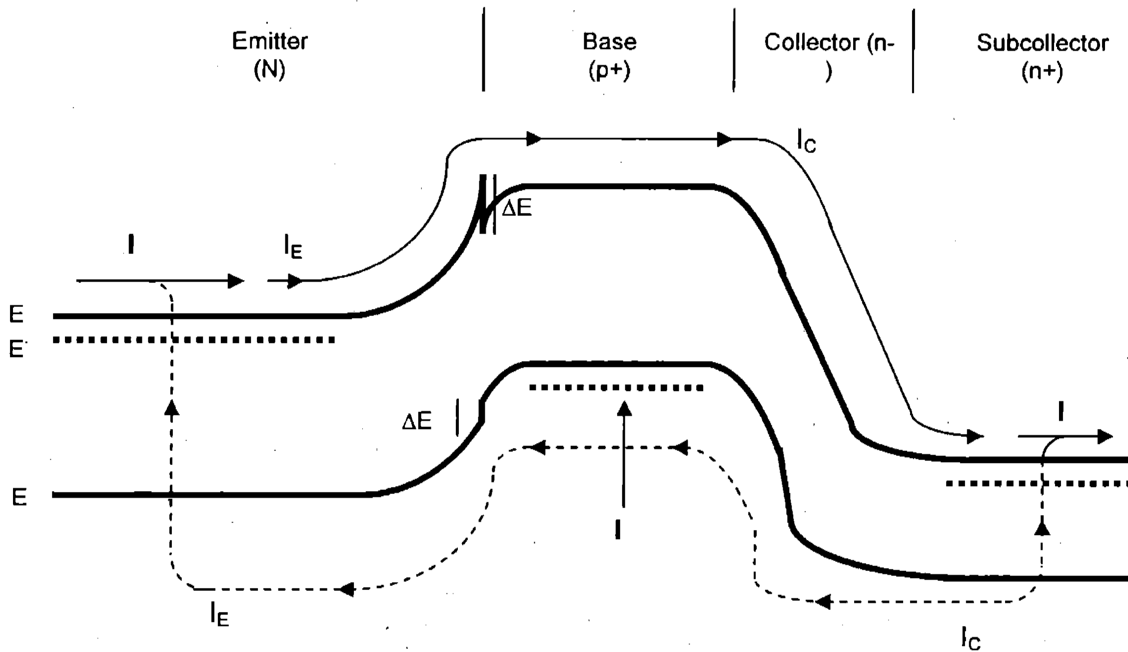


Figure 3.1: Energy band diagram for an NPN HBT with an abrupt emitter-base heterojunction in the forward-active region.

Implicitly in an HBT, it is understood that the base-collector junction is a homojunction though a base-collector heterojunction can be used. Devices utilizing heterojunctions at both interfaces are called double HBTs (DHBT).

3.2 DC Characteristics

The current gain (β) of a transistor is defined as the ratio of the collector current (I_C) to the base current (I_B). Each of these currents is made up of various components. In particular, I_B is the sum of the back hole injection current (I_{Bp}), the base surface recombination current ($I_{B,surf}$), recombination current at the base contact ($I_{B,cont}$), bulk recombination in the base region ($I_{B,bulk}$), and the space-charge recombination region ($I_{B,scr}$). Figure 3.2 illustrates the physical location and flow of each component[7].

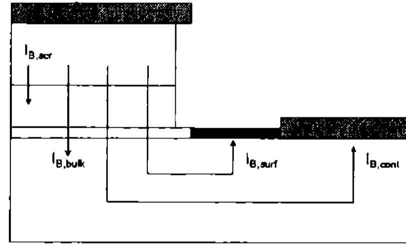


Figure 3.2: Schematic of the four main base current components

- $I_{B,surf}$ is a major component of the base current in small devices with large perimeter-to-area ratios, especially in material with high surface recombination velocity.
- $I_{B,cont}$ is usually lower than $I_{B,surf}$ as a result of its physical location outside of the based exposed surface region. The excess carrier concentration decreases rapidly from the intrinsic base region to the extrinsic area. Like $I_{B,surf}$, this component is proportional to the periphery of the device.
- $I_{B,bulk}$ does not appear on the surface like the previous two examples but is found in the base bulk layer. The base bulk layer is the region under the emitter, the active area of the base region. Electrons and holes recombine to reestablish thermal equilibrium when it is disturbed in the base.

Recombination in the base bulk region is composed of three major mechanisms: radiative recombination, Shockley-Read-Hall recombination, and Auger recombination. In III-V semiconductors with direct bandgaps such as our material system, radiative recombination dominates. This is when an electron in the conduction band and a hole in the valence band recombine with out an intermediate state. The three recombination mechanisms combine to define an effective minority electron recombination lifetime (τ_n). The overall recombination rate (U) is related to τ_n in the following manner[7]:

$$U = \frac{\Delta n}{\tau_n} \tag{3.1}$$

where Δn is the excess electron concentration compared to the thermal equilibrium electron concentration.

When $I_{B,bulk}$ is the major component to the base current, the gain can be stated as[7]

$$\beta = \frac{I_C}{I_{B,bulk}} = \frac{\tau_n}{\tau_b} \tag{3.2}$$

where τ_b is the minority carrier transit time across the base. τ_n is a material parameter that can vary slightly with increased base doping. τ_b can be increased or reduced easily by varying the base thickness.

3.3 High Frequency Response of HBTs

The two most important figures of merit used to describe a transistors high-frequency performance are the cutoff frequency, f_T, and the max oscillation frequency, f_{max}. f_T is defined when the small-signal current gain $|h_{21}|$ drops to unity. f_{max} is defined when the small signal power gain drops to unity. The cutoff frequency is also often defined as when the a.c. current gain becomes unity. Under this definition, f_T will vary given a specific small signal voltage across the base-collector junction.

The f_T is the inverse of the time an electron travels from the emitter to the collector. The total emitter to collector time, τ_{ec}, is defined using f_T as follows[8]:

$$\tau_{ec} = \frac{1}{2\pi f_T} = \tau_e + \tau_b + \tau_{sc} + \tau_c \tag{3.3}$$

The first term, the emitter charge time, is the time required to change the base potential by charging up the capacitances through the differential case emitter junction resistance. This charging time has an inverse dependence on the collector current such that at low

current levels this term is the dominant component to the overall emitter-collector transit time. The second term, τ_b, is the base transit time. This is defined as the time required to discharge the excess minority carriers in the base through the collector current. The space-charge transit time, τ_{sc}, is the transit time for the carriers to drift through the depletion region of the base-collector junction. The last term is the collector charging time and depends greatly on the parasitic emitter resistance. A change to these parameters either through device layout or structure will affect the cutoff frequency.

The max oscillation frequency is given by[8]

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{3.4}$$

where R_B and C_{BC} are the total base resistance and collector capacitance, respectively. What is important to note is that the base resistance R_B and the base-collector capacitance C_{BC} must be minimized in order to obtain a high $f_{\max}$.

3.4 Device Design Optimization

Between the three device parameters described in the previous section, gain, f_T, and $f_{\max}$, there exists a number of trade-offs in the design of the HBT device between them. In the laboratory, HBTs are often designed to target DC or high frequency performance measurements. In designing a device layout and layer structure, the designer must consider these various trade-offs. Figure 3.3 illustrates the critical dimensions of an HBT device.

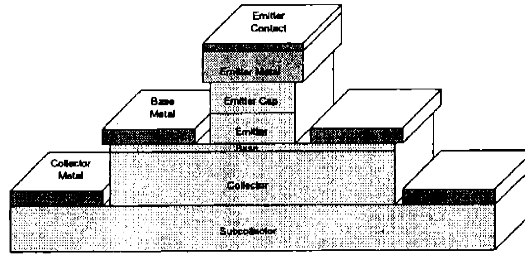


Figure 3.3: Cross-section of a typical self-aligned HBT.

In the forward active mode, electrons are injected across the entire emitter area into the base. At this point the electrons diffuse through the base to the collector, where they are swept into the subcollector by the reverse-biased base-collector junction. The active area is thus defined by the area under the emitter since there is little spread of the electrons through the base. The flow of electrons through the active region makes the device performance very sensitive to the size and doping of the region.

The main trade-offs in f_T and f_{max} involve the base and collector thicknesses. An increase in either thickness results in a decrease in the base resistance and the base-collector capacitance, increasing the f_{max}. This also causes an increase in the base and collector transit times, decreasing the f_T. An increase in the doping in the base will decrease the base resistance and increase f_{max}. Below, Table 3.1 summarizes some of the effects device structure and layout have on the device performance.

Device Parameter	**Change**	**Primary Effects**	**Gain**	f_T	f_{max}	**Breakdown Voltage**
Emitter Thickness	↓	Emitter Resistance ↓↓	↓	↑	↑	-
Emitter Doping	↓	Base-Emitter Cap. ↓↓	↓	↑	↑	-
Base Thickness	↓	Base Transit time ↓↓, Base Resistance ↑↑	↑↑	↑↑	↓	-
Base Doping	↑	Base Resistance ↓↓	↓	↓	↑↑	-
Collector Thickness	↑	Base-Collector Cap ↓↓	-	↓↓	↑↑	↓
Collector Doping	↓		-			↓↓
Emitter Width	↓	Emitter Resistance ↑, Base Resistance ↓, B-C Cap, B-E Cap ↓	↓	↑	↑	↓↓
Emitter Length	↑	Emitter Res. ↓, Base Res. ↓, Collector Res. ↓, B-C Cap, B-E Cap ↑	-	-	-	↑↑
Extrinsic Base Width	↓	B-C Cap ↓↓, Base Res. ↑	-	↑	↑↑	-

Table 3.1: Effects of altering device parameters and layout feature size of an HBT[9].

The HBT layer structure can also be optimized for increased performance. A graded emitter-base junction will reduce the ΔE_C and result in a lower turn-on voltage and thus less power consumption. Graded bases can also be used to decrease the base transit time, thus an increase in f_T. Large band gap collectors can be used to increase the breakdown voltage of the collector.

Section 4: Experimental Procedure

The growth and processing of the prototype device was a complicated processes. This section describes the process of growth of the graded buffer layer, the fabrication of the prototype HBT device, and the physical and electrical characterization methods used.

4.1 Material Growth

The buffer layer was grown in a Thomas Swan Metal Organic Chemical Vapor Deposition (MOCVD) reactor. MOCVD growth is a non-equilibrium process of flowing precursor gases over a heated single-crystal substrate. Within the heated reactor chamber, the precursor gases dissociate and deposit the either a group III or a group V element, depending on the gas, on the substrate. The ratios of the precursor gases in the reactor are changed to result in the desired film composition.

After the desired In content was reached, the device layers were deposited. Zinc and Si were used as the p-type and n-type dopants in the process, respectively. Figure 4.1 shows the targeted thickness and doping levels for the device stack.

Layer	Material	Thickness (Å)	Type	Doping (cm^{-3})
Emitter Cap	$In_{0.3}Ga_{0.7}As$	2000	n+	2 E+19
Emitter Cap	$In_{0.8}Ga_{0.2}P$	700	N+	2 E+19
Emitter	$In_{0.8}Ga_{0.2}P$	1500	N	5 E+17
Spacer	$In_{0.3}Ga_{0.7}As$	100	i	
Base	$In_{0.3}Ga_{0.7}As$	600	p+	1.5 E+19
Collector	$In_{0.3}Ga_{0.7}As$	5000	n-	5 E+16
Etch-Stop	$In_{0.8}Ga_{0.2}P$	200	n+	2 E+19
Subcollector	$In_{0.3}Ga_{0.7}As$	5000	n+	2 E+19
Graded Buffer	$In_{X=07\ 3}Ga_{1-X}As$	~6000	i	
Substrate	GaAs		Semi-insulating	

Figure 4.1: Prototype Device Layer Stack

4.2 Device Processing

The substrate was patterned using a self-aligned mesa process. The benefit of this process is that the contact metal deposited is used as the etch mask for each layer, eliminating the need for an additional lithography step. The complete process is made up of three lift-off steps accompanied by the necessary patterning and etching steps.

The photolithographic techniques used were conventional processes available in the Technology Research Laboratory of the Microsystems Technology Laboratory at MIT. Small 2 cm x 2 cm pieces from the 2" wafers grown were used in the processing. The remaining pieces of the wafer were used in the physical characterization of the buffer and the device epilayers. A detailed schematic of the device processing is offered in Appendix A.

4.2.1 Lift-Off Process

In order to avoid patterning and then etching deposited metal, a lift-off process was selected to create the metal contacts. In a lift-off process, photoresist is first patterned using typical photolithography steps. The result pattern leaves areas where metal is desired exposed. Metal is then deposited, covering the entire sample. In a lift-off process, there is a discontinuity it the metal around the exposed area in the resist as a result of the step. The figure below demonstrates the discontinuity in metal.

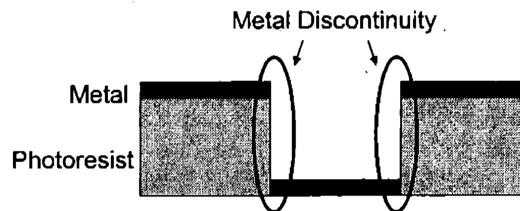


Figure 4.2: Deposited metal discontinuity as a result of patterned photoresist in a lift-off process.

The sample is then soaked in a solution that removes the resist and thus the metal on top of the resist. The metal on top of the resist is able to be removed because it is not in contact with the metal in the resist opening. The metal in the opened area remains. This process greatly reduces the complexity of defining the contact metal by eliminating the need to etch metal away.

The same process was used for depositing metal for each device layer. The material pieces were initially baked in a pre-bake HMDS oven. After baking, pieces were spin-coated with 1 micron of AZ 5214E image-reversal photoresist and post-baked to cure the resist. Coated pieces were then loaded into an alignment tool for exposure. After exposure, the piece was post-baked and then subjected to a flood exposure. This step was necessary because the photoresist being used was an image-reversal resist. The piece was then developed using the AZ 422 developer. Ti/Pt/Au contact metal was then

deposited using evaporative deposition. To complete the lift-off process, the piece was soaked in acetone to remove the resist and thus the excess metal deposited on top of the resist.

4.2.2 Self Aligned Mesa Structure

After the lift-off step is complete, the remaining metal serves as an etch mask used to define the device. Using selective etches, material is removed around the metal. The etch will stop at the next material change. The etch will not laterally etch the material under the metal. As a result, a mesa of material is left behind. This mesa defines the geometry for that device level. The resultant device is a three tiered mesa structure. The figure below demonstrates the self aligned mesa process.

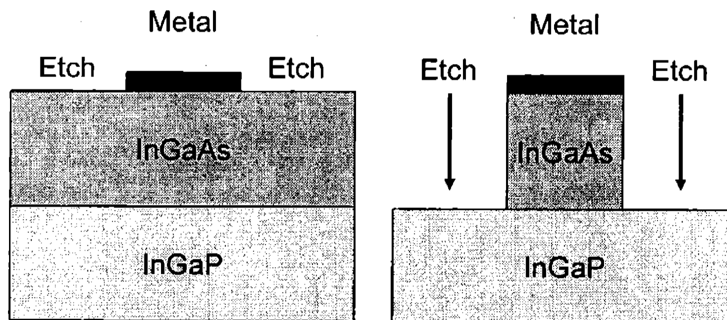


Figure 4.3: Self-aligned mesa formation using selective etching

The process described was used to define the emitter, base, and subcollector regions. To etch the InGaAs layers, an H_2SO_4: H_2O_2: H_2O (3: 1: 100) etch was used. To etch the InGaP layers, an HCl: H_3PO_4: H_2O (1: 1: 50) etch was used. Each etch was selective to the specified material. Below is a summary table of the selectivity generated during the etch selection process. Etch rate experiments were run on undoped InGaAs and InGaP samples similar to the composition noted in the device.

	H_2SO_4: H_2O_2: H_2O (3: 1: 100)	HCl: H_3PO_4: H_2O (1: 1: 50)
InGaAs 70 % In	0.5 Å/sec	negligible
InGaP 16 % Ga	negligible	50 Å/sec

Table 4.1: Etch rates for each device layer

4.2.3 Mask Design

The mask was designed to capture four emitter area sizes, 60 x 60 um, 80 x 80 um, 120 x 120 um, and 180 x 180 um. Each device is a self-aligned mesa structure. The figure below shows the combined mask design for the three device levels.

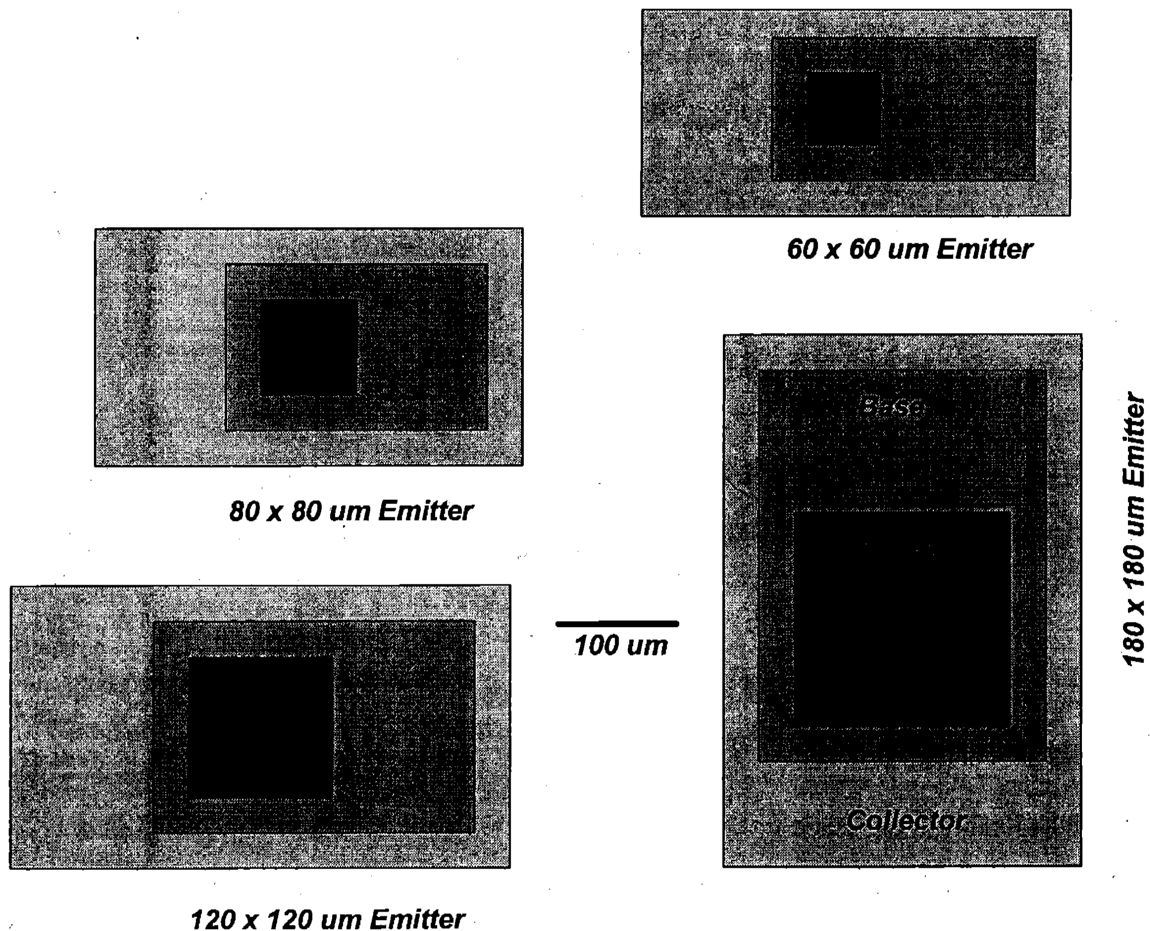


Figure 4.4: Emitter, Base, and Collector Mask Layout

4.3 Physical Characterization

The thicknesses of the graded buffer and the device layers were resolved using transmission electron microscopy (TEM). Pieces of the wafer not used for device prototyping were prepared for TEM by Nate Quitoriano.

The doping profile of the device was determined using Secondary Ion Mass Spectrometry (SIMS).

Images of the fabricated prototype device were obtained through optical microscopy and scanning electron microscopy (SEM).

Section 5: Results of Processing and Growth

Presented in this section are the results of two growth and processing experiments. Each growth process features adjustments to the process that provided varying results in the device structure and the subsequent processing. A discussion is provided on the results after each growth experiment and processing.

5.1 Device Stack Characterization

The graded buffer and the device layers were grown in an MOCVD reactor by Nate Quitoriano of MIT's Fitzgerald Research Group. The growth process involved with forming the device used in this research was a combination of complicated processes including temperature monitoring, gas venting and flowing, and timing. In addition, the device being utilized, the HBT, is sensitive to a number of the properties of the epitaxial layer. It is imperative to understand the quality of material being used prior to device fabrication.

5.1.1 Epilayer Characterization

Before the process of defining the device, the thickness and quality of the epitaxial layers of the wafer were documented. The following figures are TEMs of the first growth.

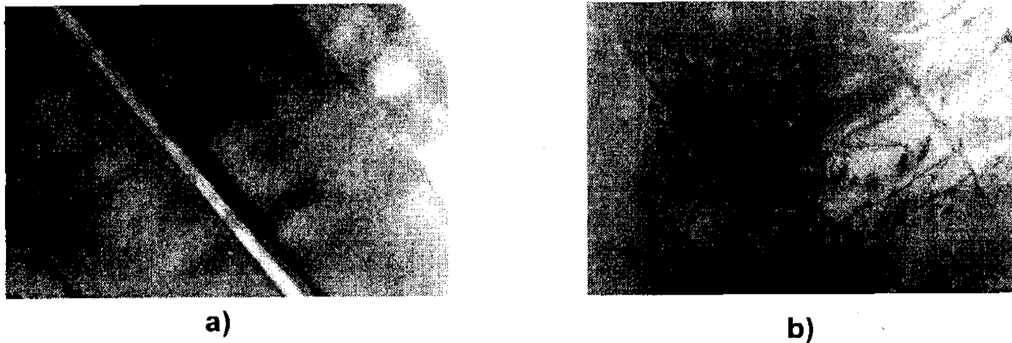


Figure 5.1: TEM of device epilayers showing a) planer device epilayers and b).rough non-planer layers found in areas on the wafer. (courtesy of N. Quitoriano)

Figure 5.1 (a) demonstrates the planar layers in the device stack. Note in the TEMs, the color distinction between the InGaP and InGaAs layers. InGaP appears darker in TEM. Figures 5.1 (b) depicts a roughness in the device layers that was seen in other areas of the wafer. This raises concerns about whether some layers of the device are continuous throughout the wafer. Discontinuous layers would impact the performance of the device and possibly further processing. Due to the complexity of the device epilayer growth, it is not known what caused the roughness in some areas. It is likely a result of the inexperience associated with the difficult growth procedure.

Table 5.1 compares the actual on wafer thickness to the targeted thicknesses of each layer and Figure 5.2 indicates the device layers.

Layer	Target Thickness (nm)	On Wafer Thickness (nm)
Emitter Cap	270	266
Emitter	150	200
Spacer	10	17
Base	60	97
Collector	500	801
Etch-Stop	20	66
Subcollector	500	837

Table 5.1: Design vs. On-wafer thicknesses for epilayers.

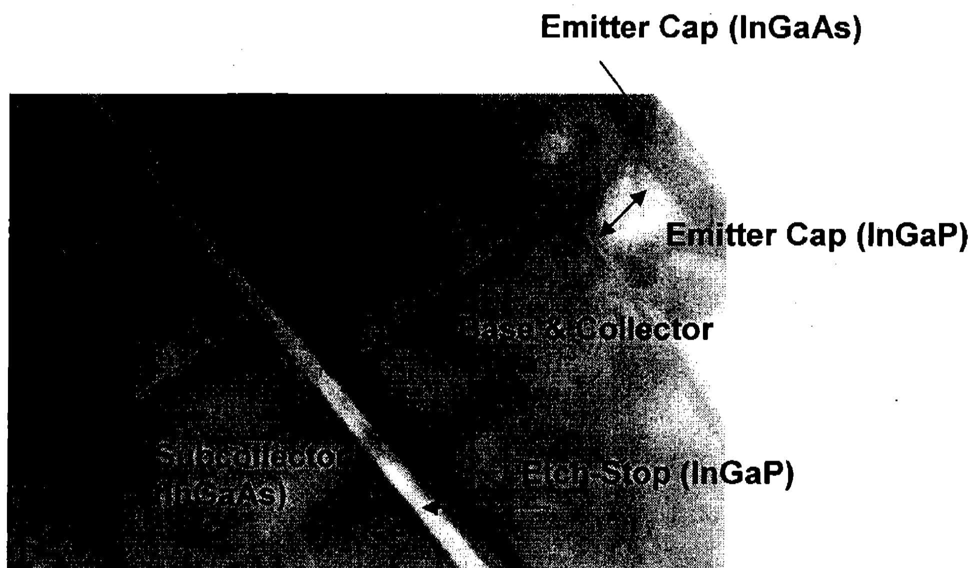


Figure 5.2: Labeled TEM of Device epilayers (courtesy of N. Quitoriano)

Below the device epilayers is the graded buffer. Figure 5.3 is a TEM of the graded buffer. The TEM captures the GaAs substrate and the transition to $In_{0.3}Ga_{0.7}As$. Prominently seen in the TEM are the threading dislocations throughout the graded buffer.

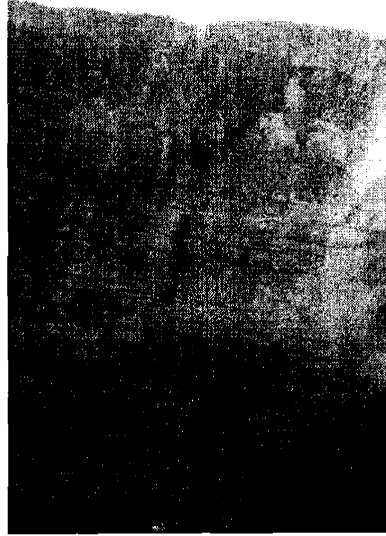


Figure 5.3: TEM of the graded buffer. The final composition is $In_{0.3}Ga_{0.7}As$. (courtesy of N. Quitoriano)

5.1.2 Composition and Doping Characterization

In addition to physical images of the device stack, it is important to determine the doping profile and doping levels. The figure below is the SIMS analysis for the first sample and labels the appropriate device layer and the targeted doping. Silicon and Zinc were used as the n and p type doping, respectively. Overlapped with the doping elements are the Phosphide and Arsenide traces to help in determining the regions of the device, these traces are on a different concentration scale.

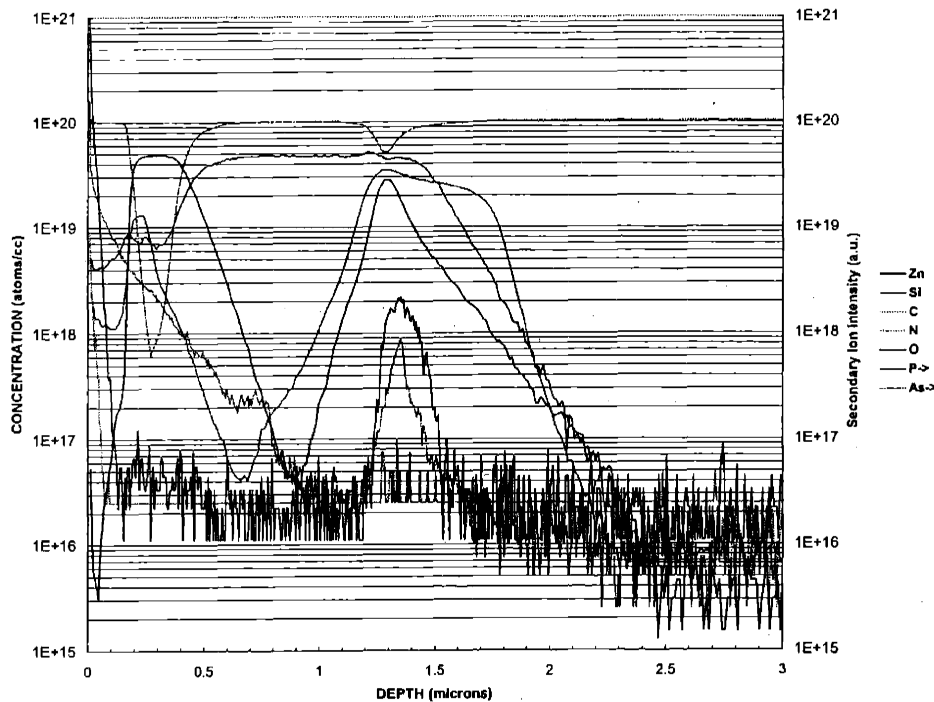


Figure 5.4: SIMS analysis for first growth

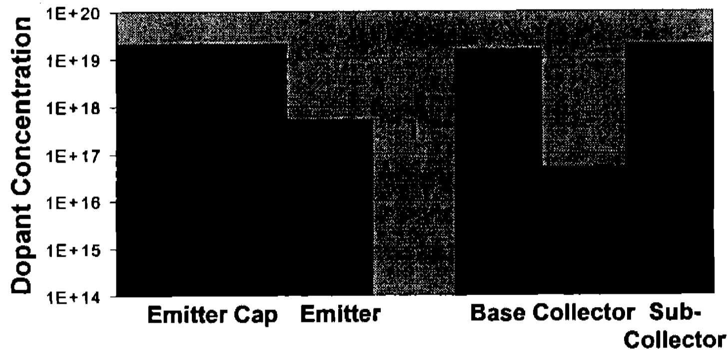


Figure 5.5: Ideal doping concentration of the device layers.

Two major observations are made from the SIMS analysis regarding the device layers and the Zn doping. The InGaP and InGaAs regions are identifiable as they were in the TEMs. The Zn doping is not concentrated in the base InGaAs region as it should. Instead, the Zn dopant has traveled into the n-type doped collector. As a result, a decrease in collector doping will decrease in the breakdown voltage of the device.

5.2 Device Processing

The initial growth sample was processed through to the emitter etch and then pulled out to observe the results. The sample was processed as described in Section 4.2. After completing the emitter etch step, the profilometer was used to determine the success of the lift-off procedure and the emitter etch processes.

5.2.1 Emitter Etch Results

The profilometer scan revealed over 6 microns of material was removed as a result of etching. The floor the material was extremely rough with peak to valley measurements as great as 1 micron. It was expected that the combined etch steps would remove the emitter cap and emitter layers, about 250 nm of material. Since the two etches were done in succession without analysis in between, it is impossible to determine which of the two etches removed the material.

5.2.2 Emitter Contact Metal

Under an optical microscope, the emitter contact metal appeared pitted and rough around the edges. This would indicate that the etches used were attacking the contact metal. Profilometry scans of the emitter metal displayed a rough surface with peak to valley measurement on the order of 0.5 microns.

5.3 Adjustments to the Process

The first pass on the growth and the processing revealed many points of discussion moving forward for the technology. Below is a summary of these discussions and the corrective action taken.

5.3.1 Growth Conditions

The most alarming result of the initial pass on growth was the travel of the Zn dopant. After researching the phenomenon, it was found that Zn diffusivity in an HBT is greatly affected by undesirable nonequilibrium concentrations of interstitials. Some believe it is a result of the presence of a highly doped emitter cap layer separated by an emitter layer greater than 100 nm. Kurishima and Gösele concluded that it is actually the n+ subcollector that is the main cause of the Zn diffusion. They propose two ways to suppress the Zn diffusion. The first is to interrupt the growth for a sufficient period of time before growing the base layer. During the growth interruption, the excess interstitials should diffuse partly into the crystal and partly to the surface. The second provision is to grow the subcollector at higher temperatures. The elevated growth temperature will increase the rate of point-defect generation and migration. It is important in order to suppress the affect of the n+ subcollector to reach point-defect equilibrium before growing the base[10].

The subsequent growth incorporated these fixes. Prior to growing the base, the process was interrupted for a 30 min., 625 °C anneal and the emitter and emitter cap were grown at 500 °C. Also, the base was changed to intrinsic doping to further reduce the impact of the Zn diffusion. This last change will have a minor impact on the DC performance of the HBT but has a greater impact on the RF performance. There were other minor adjustments to the growth procedure that are typical with the learning from one growth to the next.

5.3.2 Epilayer Characterization of Second Growth

Below is a TEM of the second growth iteration.

Figure 5.6: TEM of device epilayers from the second growth experiment. The process incorporated the process changes to suppress Zn diffusion. (courtesy of Nate Quitoriano)

The device epilayers show signs of a polycrystalline nature. It was later realized that the calibration for the growth temperature of 625 °C was for a different location in the reactor than where the wafer was placed. This may lead to unexpected compositions and film properties.

Table 5.2 summarizes the device epilayer thicknesses for the second growth iteration.

Layer	**Target Thickness (nm)**	**On Wafer Thickness (nm)**
Emitter Cap	249	200
Emitter Cap	73	70
Emitter	237	220
Base	81	70
Collector	703	570
Etch-Stop	23	20
Subcollector	594	500

Table 5.2: Design vs. On-wafer thicknesses for device epilayers for the second growth iteration.

The changes in the growth procedure were mostly directed towards controlling the Zn doping. The figure below is the SIMS analysis for the second growth iteration.

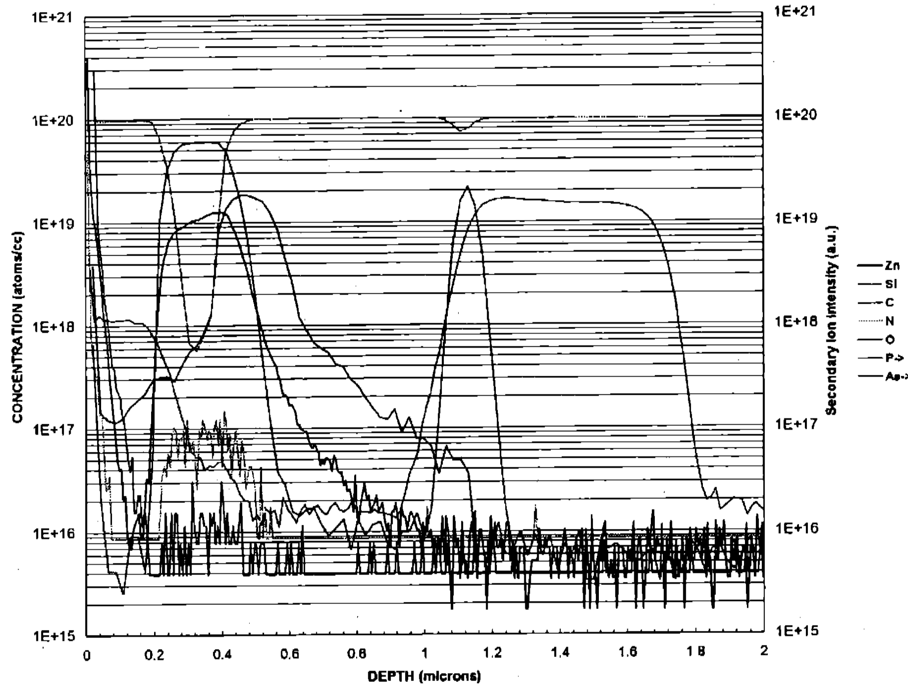


Figure 5.7: SIMS analysis of 2nd growth iteration

The SIMS analysis shows a tremendous improvement in the doping profile. The Zn peak is located in the appropriate device layer. The n-type dopant profile is improved as well. The Si peaks are well located within the appropriate device layer.

It was the thought that improved epitaxial layer and doping profile would help to control the emitter etch problem. Therefore, the samples from the second growth iteration were processed through the emitter etch step. The resultant profilometry scan returned similar results. The etch removed about 7 microns of material. The floor of the material was extremely rough with large peak to valley differences. Since the device layers were continuous and of proper thicknesses, the investigation focused on the

selectivity of the etches and the affect of doping levels of the etch rate. The initial etch test samples were undoped leaving the question of etch rate dependence on doping open.

5.3.2 Processing Changes

No adjustments were made to the process outside of verifying the selectivity and the etch rates for both emitter etches. It was thought that the discontinuity of some of the device layers caused the etches to be in contact with compositions that it would etch. The verification process of the etches included confirming the selectivity of the etches at the appropriate compositions and the etch rate dependence on doping levels in InGaAs.

Section 6: Product Overview

The technology developed in the preceding chapters provides both performance and cost benefits over existing GaAs and InP platforms to customers. Initial cost benefits are realized through the economies of scale associated with the use of larger diameter wafers. Through the flexibility in providing a variety of wafer sizes, the technology can integrate with and extend the life of existing manufacturing tool sets in a fabrication facility. The enhanced electrical performance allows designers to reach next generation performance specifications with current generation tooling and designs. The technology allows the customer to pull next generation material designs forward without changing over their manufacturing toolset thus, providing a performance edge over their competitors.

6.1 Product Benefits

Our technology allows the customer to realize cost and performance benefits based on a number of our product features later discussed in Section 6.3. These features solve many of the problems faced by leaders in high frequency semiconductor products. Companies such as these need to support costly development projects to create their next generation technology and processes. Our technology provides a materials solution that avoids the large capital expenditures required in next generation technologies.

Current high-performance devices are grown on GaAs substrates. GaAs has long been the most economical high-performance semiconductor material. Its stronghold is in handset power amplifiers. Due to the momentum of the tremendous knowledge base behind silicon, Si based SiGe and Si BiCMOS processes are not far behind. In the future, experts are readying next generation high-performance semiconductor devices to be grown on InP substrates. The most common size of InP substrates is a 2" diameter wafer.

The downturn in the semiconductor industry beginning in 2001 has caused many firms to cut their long-term development projects for InP. Our technology enables InP like performance on larger GaAs wafers ranging from 4" to 6" in diameter. What is important is that these wafer sizes are already being used by most companies in the high-performance semiconductor industry. The benefits of using larger wafer sizes are well known to the semiconductor industry. The larger wafer sizes add no extra processing steps and reduce the total processing time of a job because fewer wafers are needed to achieve the needed number of die. The added cost of more processing time of a larger wafer such as longer soak times to get to temperature are offset by the reduced number of wafers processed through the fab. The figure below diagrams the benefit of increased usable area in using larger sized wafers.

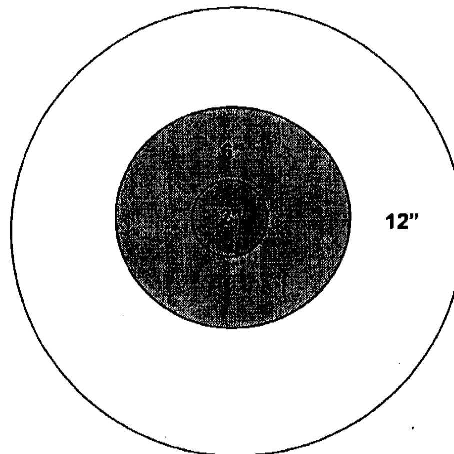


Figure 6.1: Diagram showing the difference in usable area between 2", 6", and 12" wafers.

Not only are economies of scale realized with the use of increased wafer sizes but companies will also benefit from the cost difference between a GaAs wafer and an InP wafer. 2" diameter InP wafers are quoted to cost $\$50/\ \text{in}^2$ while 6" GaAs wafers are quoted to cost as little as $\$15/\ \text{in}^2$ [11]. The cost of our enhanced wafer will likely be ~$30/ in[12], resulting in 40% savings over InP wafers. The figure below shows a cost per unit

area comparison between a similar devices processed using InP wafers and metamorphic wafers. Our product would be considered a metamorphic wafer.

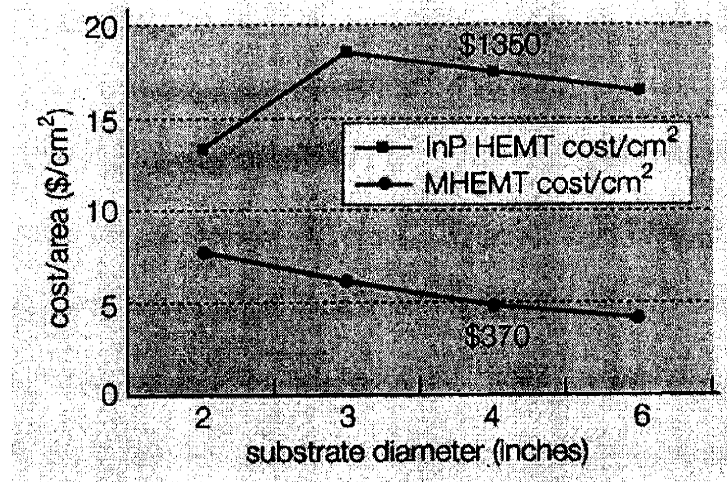


Figure 6.2: Cost per cm^2 of metamorphic HEMTs (M-HEMTs) devices grown on GaAs is much lower compared to similar devices on bulk InP wafers[12].

With InP like performance on a GaAs wafer, companies can begin to design next generation devices utilizing the enhanced GaAs wafers. In essence, our technology allows companies to pull forward their adoption of InP without making the necessary capital investments into a new toolset. A company's existing GaAs toolset can be used to process the enhanced substrates. No new equipment is needed to process the enhanced wafers.

Companies unwilling to adopt InP because of the negative industry buzz surrounding the costs of InP can view the enhanced wafers simply as an upgrade to the GaAs wafers already being processed in their fab. These companies will benefit from performance enhancements over their customers such as higher frequency performance and operation and lower power consumption. The added cost of the enhanced wafers will

be out weighed by performance enhancements that open new market opportunities and advantages.

6.2 Technology

The value of the technology is a result of the research groups' ability to grow a high quality graded buffer on a GaAs substrate and the commonality between the materials used.

Many other research facilities, both university and corporate, are using this technique with limited success. The main quality measurement of this material is the number of defects in the material created through this process. Our company's unique ability to reduce the defects incorporated through this process by two orders of magnitude result in a higher quality substrate than our competitors. Our research group has extensive knowledge in enhanced substrates, including strained silicon. This wide knowledge base results in better techniques and understanding in the fundamental process.

The GaAs substrate serves as the foundation to grow the graded buffer grown on through to growing successive layers of $In_xGa_{1-x}As$. Each successive layer of $In_xGa_{1-x}As$ has an increasing amount of In content. The final layer grown results in an enhanced substrate with better electrical performance than the initial GaAs substrate. Among the enhancements of the new substrate are the electron mobility of devices that would be grown on the new substrate and a decreased band gap that would reduce the turn-on voltage of a device. An increase in electron mobility would increase the maximum operating frequency and the speed of the device over a device grown on a normal GaAs substrate. The reduced turn-on voltage results in needing less voltage to achieve the

needed current level. This advantage can be thought of as extending the battery life of the end product because the device requires less power to operate.

GaAs and InP are very similar compounds, both are known as III-V semiconductors because Ga and In are Group III elements in the periodic table and As and P are Group V elements. A result of this commonality is the resultant enhanced substrate can be processed using the same tools as those used to process the initial GaAs substrate.

6.3 Product Features

The features of the technology can be divided into two basic categories: features for reducing cost of technology advancement and features for enabling technology advancement today.

Features that allow customers to reduce costs of next generation technologies:

- Compatibility with existing manufacturing tools
- Available in 4" and 6" diameter wafers
- Commonality of materials
- GaAs based substrates
- Robustness of GaAs based substrates

Features that allows customers to begin to design for next generation applications today:

- Increased speed of devices
- Increased operating frequency of devices
- Reduced power consumption

6.4 Integrating the Technology

The commonality between the GaAs and InP material system make integrating the technology simple. The enhanced wafer can be run along side with the existing wafers and processes being used in the manufacturing facilities. Since the enhanced wafers are available in various sizes, the customer can select the size that fits the current wafer chucks being used in their manufacturing facility. If an InP wafer were used instead, a new toolset would need to be purchased in order to process the InP wafer. Our technology eliminates this need further extending the life of the existing tool set.

One major hurdle in incorporating new materials into semiconductor processing is possible contamination. The presence of atoms from certain materials can result in product failures or yield loss through processing. Therefore, before new materials are brought into the fab and used during processing, the new material must be approved. Once approved, the material is often times restricted to certain areas to reduce the possible spreading of material. The commonality between an enhanced substrate and the existing GaAs or InP production lines eliminates any possible contamination problems.

If a company running a 6" GaAs line wanted to incorporate InP into the fab, the company would need to purchase additional equipment in order to do so. The main reason for this required investment in capital equipment is the difference in wafer diameter. Each tool used in semiconductor manufacturing uses a specific sized chuck. The chuck holds the wafer while it is being processed with in the tool. Existing 6" chucks cannot accommodate the 2" wafers. Therefore, 2" InP wafers cannot be processed on 6" GaAs wafer chucks. New chucks or possibly new tools will need to be purchased. Since our enhanced substrate can be developed on 6" diameter wafers, or any

other sized wafer, the added capital equipment is not needed. Our enhanced wafer will be completely compatible with the existing chuck sizes used in a fab.

6.5 Extending the Technology

As a platform technology, the innovation can be extended to serve other applications outside the immediate target industries. As acceptance of the enhance substrate grows, the technology may begin to serve as the vehicle to implement InP into the high performance semiconductor market.

6.6 Status of Development

Devices using the first enhanced substrate are being processed in order to undergo DC performance testing to verify the reduction in turn-on voltage. Subsequent iterations of the material and devices utilizing the material are forthcoming. The initial material verification is being performed on $In_XGa_{1-X}As$, not InP as the product will feature.

Section 7: Market Definition

Given the advantages of the product, the technology innovation is applicable to all semiconductor markets. This section summarizes the possible markets for the innovation. Each market is characterized by current state, future need, and possible integration issues.

7.1 Semiconductor Market Overview

The semiconductor industry can be thought of as divided into 6 basic market technology segments: logic, memory, analog/mixed-signal (AMS), radio frequency (RF) transceivers, power amplifiers, and millimeter wave. The first two, logic and memory, are technologies dominated by silicon. Logic products can be generally thought of as the technology behind the microprocessor in laptop and desktop computers. Memory products encompass DRAM and non-volatile memory products. These two applications are mature industries served by silicon. Since price is a significant driver in these two markets, silicon will be the material of choice for many next generation technologies. The remaining four technologies, AMS (0.8-10 GHz), RF transceivers (0.8-10 GHz), power amplifiers (0.8-10 GHz), and millimeter wave (10-100 GHz), are high frequency market applications that would be attractive to our technology[13].

The level of attractiveness for our technology to the remaining markets is their dependence on the materials systems being used in each. RF and AMS technologies are becoming critical technologies to the success of the semiconductor market. The importance of these technologies arises because they serve the rapidly growing wireless communications market. In this instance, some of the materials are compatible with the common complementary metal oxide semiconductor (CMOS) process and others are not

compatible. The ability to be compatible with silicon CMOS processes becomes a driver for these markets in order to suffice the ever growing price pressure in the wireless communications industry. This is especially true in the 0.8-10 GHz application range where elemental semiconductors (silicon based) are beginning to capture market share from compound semiconductors. Within this frequency range, the performance of the elemental semiconductors is rapidly increasing and approaching the performance of the once dominant compound semiconductors. The area between 10 GHz and 40 GHz is expected to be the battle ground between elemental and compound semiconductors. The space above 40 GHz is dominated by compound semiconductors.

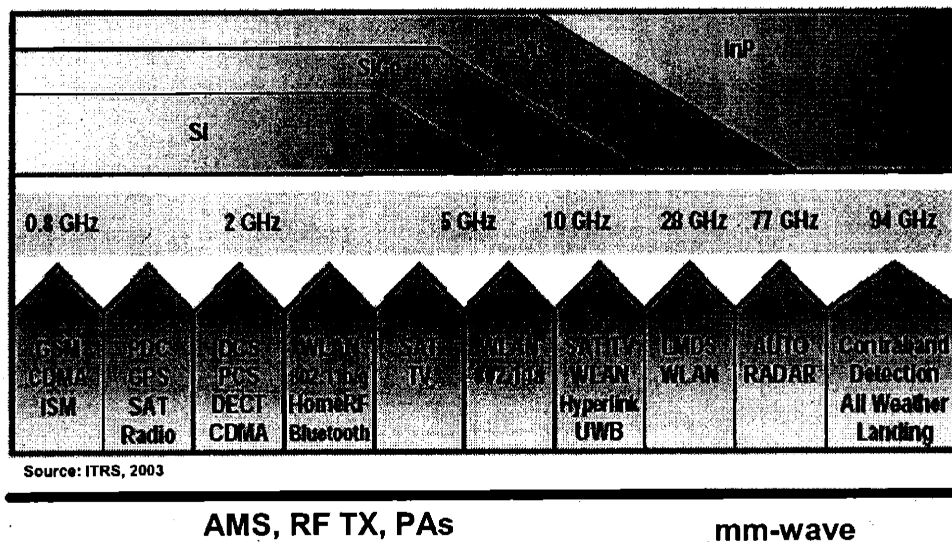


Figure 7.1: Application frequency and market for major semiconductor materials.

Figure 7.1 lays out the commercial wireless applications, the frequency of these applications, and the elemental and compound semiconductors that are most likely to serve these areas. The material boundaries are likely to change over time as a result of the various market drivers. In commercial wireless communications, cost is a key driver and is likely to drive the boundary between Si, SiGe and GaAs to higher frequencies.

Alternatively, as the frequency increases performance becomes a stronger driver and the boundary between high frequency materials may adjust down to lower frequencies. In the future, the boundaries between the materials are less likely to be frequency dependent because each technology is rapidly increasing their application frequency. Performance parameters such as noise frequency, power added efficiency, linearity, and output power are likely to determine what material will be used. Therefore, two technologies might serve one application but are favored over one another for a specific performance parameter. It is generally accepted that performance and cost between the materials increases in the following order: Si CMOS, SiGe, GaAs, InP. An increase in RF performance for silicon is typically achieved through geometrical scaling, photolithography advancements. Conversely, increased RF performance for compound semiconductors is obtained through material optimization or bandgap engineering.

Complicating the analysis of the technical drivers for each application are the other existing non-technical drivers. Among these are government regulations that determine frequency availability and standards and protocols that determine frequency channels and their bandwidths. Government regulations and standards and protocols are likely to vary regionally and nationally creating international differences in technology uses and requirements. Also, these regulations are often altered under industry pressure creating a dynamic competition environment. An example of the impact of regulatory change occurred in the United Kingdom. In October of 2002, UK regulators gave into market demand and allowed the 3.5 GHz fixed wireless band to be used for backhaul cellular networks and broadband access services. The major backhaul spectrum had been 24.5-26.5 GHz but now operators in the 3.5 GHz spectrum will be able to serve both

markets. Companies developing 24 GHz capability are now facing an entirely new set of competitors and technologies. The landscape completely changed with the new regulation[14].

7.2 Analog and Mixed-Signal

Analog refers to circuits using only analog (no digital) circuitry and mixed-signal contains both analog and digital circuitry. Analog circuits include operational amplifiers and mixed signal chips include analog-to-digital, digital-to-analog converters and digital signal processors. Like most industries, analog/mixed-signal (AMS) applications are moving towards higher frequencies. This is a result of the post signal processing performance requirements which continues to be the main commercial application driver. In the future, the AMS market will be completely dominated by the elemental (Si based) semiconductors rendering our technology unattractive to this market space.

7.3 Radio Frequency Transceivers

RF transceivers include the circuitry from the low noise amplifier or power amplifier back at the antenna to the signal converter at the baseband end of a wireless device (possibly include a figure). Applications for RF Transceivers are low noise amplifiers, voltage controlled oscillators, driver amplifiers, and filters. The use of wireless RF transceivers is growing rapidly and is quickly becoming a technology driver for advanced semiconductors. Located in the 800 MHz to 10 GHz frequency range, the products include local and wide area standards. A list of these standards include: GSM, CDMA, 802.11, and UWB. The primary performance parameters are the figures of merit discussed in Chapter 2, f_T and f_{MAX}, and noise figure. These products also consider the trade-offs between power, noise, and linearity. Currently, CMOS and Si or SiGe

BiCMOS technologies are the dominant processes used in RF Transceivers and will likely remain to be in the future. Thus, our technology is not attractive to this technology space.

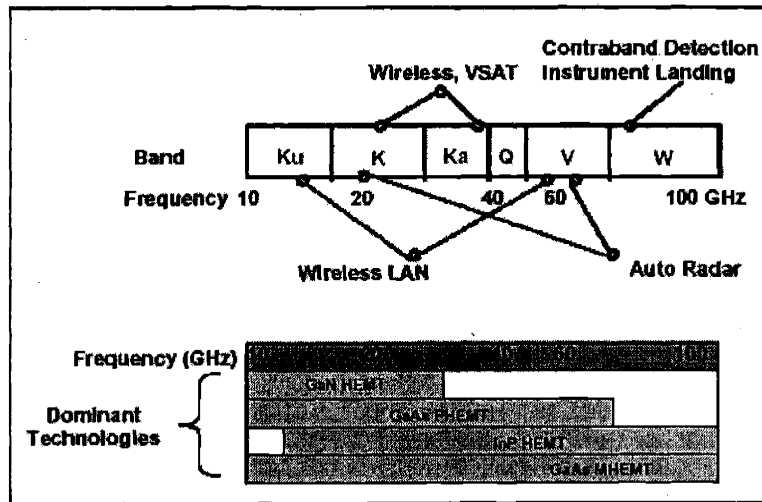
7.4 Power Amplifiers

GaAs heterojunction bipolar transistors (HBTs) currently dominant the consumer market for power amplifiers. These markets include radio frequency integrated circuits (RFICs) and modules for cellular handsets. The cellular handset is the largest driver due to its rapidly increasing volumes. Also, wireless LAN applications are beginning to become another significant driver. Both of these applications have very specific technology requirements but the volumes drive extremely sensitive price and performance trade-offs. To address this trade-off, designers are moving towards more integrated low-cost system level solutions. The market is driving for a more integrated module that will deliver a complete amplifier solution containing other components to reduce the RF component count in assembly. The projected RF modules will try to integrate the matching networks, power management, filtering, RF switches for both transmit/receive and band selection. The RF power amplifier is becoming the first true RF commodity component. In the cellular handset, the GaAs HBT is the lone remaining compound semiconductor component in an otherwise elemental semiconductor (silicon) dominated device. Therefore, the GaAs HBT PA is under tremendous price pressure and will be replaced as soon as a suitable silicon based PA is available. Although our technology may provide a performance enhancement to the power amplifier, the commodity nature of the power amplifier market makes it unattractive to our technology.

7.5 Millimeter Wave

This market, 10-100 GHz, is dominated by compound semiconductors and is the focus market for our technology. Most devices used are composed of epitaxial layer stacks that are composed of ternary compounds derived from Group III and V elements of the periodic chart. Device properties and performance are critically dependent on the materials used and the layer thickness and doping. These parameters tend to be manufacturer specific and proprietary resulting in a wide variety of device design and performance. What drives such variety in performance are the numerous trade-offs between power, efficiency, noise, breakdown, and linearity in mm-wave devices. The trends in performance of these devices are driven by trade-off manipulation and bandgap engineering of the epitaxial layer stack. This is in contrast to logic and memory performance trends that are driven by lithography advancements. This is not to say lithography advancements are not used to boost performance in mm-wave devices. Lithography is a significant driver in meeting high frequency figures of merit, f_T and f_{mas}. In the end, companies in this space are competing on the quality of their product and the performance. Suppliers boast low defect levels, high electrical performance, and advanced materials. Since high commercial volume products have not reached this space yet, cost is not the number one driver in this space.

Figure 7.2 shows the variety of applications in the mm-wave frequency range and the devices likely to serve the applications. As mentioned in Section 7.5, there will be instances were multiple technologies and devices will be available for one application.



Source: ITRS, 2003

Figure 7.2: Millimeter wave commercial applications and likely materials and devices used.

The next sections highlight some of the possible millimeter wave markets.

7.6 Local Multipoint Distribution Service (LMDS)

LMDS is a broadband wireless point-to-multipoint communication system operating above 20 GHz (depending on country of licensing) that can be used to provide digital two-way voice, data, Internet, and video services. Figure 7.3 shows a typical LMDS system[15].

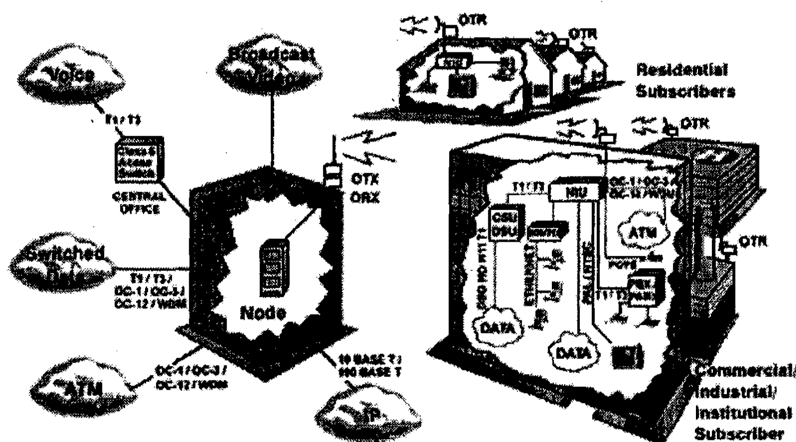


Figure 7.3: Sample LMDS system

Point-to-point fixed wireless networks have been commonly deployed to offer high-speed dedicated links between high-density nodes in a network. Moreover, since a large part of a wireless network's cost is not incurred until the customer premise equipment is installed, the network service operator can time capital expenditures to coincide with the signing of new customers. LMDS provides an effective last-mile solution for the incumbent service provider and can be used by competitive service providers to deliver services directly to end users. Benefits can be summarized as follows:

- lower entry and deployment costs
- ease and speed of deployment (systems can be deployed rapidly with minimal disruption to the community and the environment)
- fast realization of revenue (as a result of rapid deployment)
- demand-based buildout (scalable architecture employing open industry standards ensuring services and coverage areas can be easily expanded as customer demand warrants)
- cost shift from fixed to variable components (with traditional wireline systems, most of the capital investment is in the infrastructure, while with LMDS a greater percentage of the investment is shifted to customer-premise equipment [CPE], which means an operator spends dollars only when a revenue paying customer signs on)
- no stranded capital when customers churn
- cost-effective network maintenance, management, and operating costs

7.7 Forward Looking and Short Range Radar Sensors

Among all of the future car accessories under development, the mm-wave radar-based sensor is now well advanced, and is becoming one of the main applications for GaAs-based MMICs. As shown in figure 7.4, the radar network configuration around the car is relatively complex, with more than eight sensors providing short- or medium-range detection.

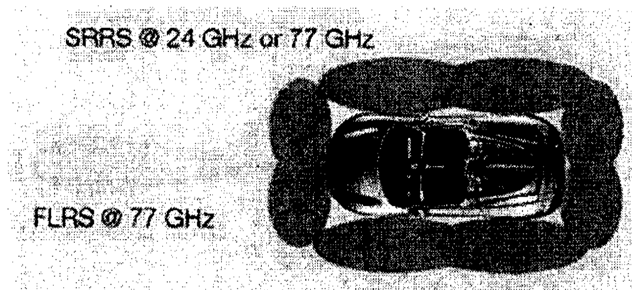


Figure 7.4: Radar Network Configuration around a car. (Compound Semiconductor, May 2003)

The forward-looking radar system (FLRS) at 77 GHz allows a detection of objects 1-200 m in front of the car. The angular coverage is around ±5°. The commercially available versions are limited to the detection of moving objects. They are called autonomous cruise control (ACC) radars and are sold as comfort systems. The challenging next development steps consist of adding the detection and classification of fixed objects in order to build real collision warning and avoidance systems. These new generations require better performance including sensitivity and angular resolution, and higher architecture complexity to give multiple channels and fusion with different sensor technologies.

Short-range radar sensors (SRRS), also based on mm-wave radar, are put all around the car. The detection range is 0.1-20 m. The standard frequency for SRRS has yet to be decided due to important requirements on bandwidth (2-4 GHz). The most

commonly used frequency is 24 GHz, but 77 GHz is also being considered. These sensors cover a range of applications such as parking and reversing aids (as fulfilled today by ultrasonic sensors), but also side object detection and the "stop and go" function for moving the vehicle forward in slow-moving traffic queues.

The main challenge to implementing MMIC-based automotive radar is to find a cost-effective solution fulfilling the following constraints:

• Operation at very high frequency;

• Solutions for high-volume production that do not need post-assembly tuning;

• Ability to withstand the harsh environmental conditions for automotive applications such as vibration, humidity and wide temperature variations;

• High integration level for building very small sensors;

• Relatively high level of performance.

7.8 Millimeter Wave Devices

The devices most commonly used for the millimeter wave (mm-wave) application are divided into two major types field effect and bipolar transistors. It is not necessary to focus on specific device for an application as a result of the technology being able to be used in all of these device types.

Field effect transistors (FETs) are majority carrier devices where electron transport is in a thin layer parallel to the wafer surface. The major types of FETs include:

- MESFETs: Metal-Semiconductor-Field-Effect-Transistor. These devices are homogeneous layers in which the electron transport occurs in an intentionally doped layer.

- HEMTs: High electron mobility transistors. These devices are composed of layers of different bandgap materials on a lattice matched substrate.
- PHEMTs: Psuedomorphic high electron mobility transistors. These devices are composed of layers with different bandgap material son a substrate in which the lattice constant of the layers are close, but not matched, to the lattice constant of the substrate.
- MHEMTs: Metamorphic high electron mobility transistors. These devices are composed of layers of different bandgap materials on a substrate in which the lattice constants of the layers are mismatched to the substrate. The resulting strain is taken up by the specially designed buffer layer. MHEMTs offer the highest degree of flexibility in design in mm-wave performance.

Heterojunction bipolar transistors (HBTs) are minority carrier devices in which carrier transport is perpendicular to the wafer surface. The major types are discussed below:

- InP HBTs are composed of ternary and quaternary layers in a number of III-V elements [In, Ga, As, Sb, P] that are closely lattice matched to InP substrates. GaAs HBTs are generally used below 10 GHz.
- SiGe HBTs are composed of a single crystal mixture of Si and Ge on a Si substrate.

Section 8: Competition

This section reviews the competition faced by our innovation. Competition in the case is two fold. The innovation faces competition from existing companies serving the market or those targeting to enter the market in the future. The other form of competition is silicon based semiconductor processes and GaAs based processes. The development of these technologies continues to increase performance. Currently, these technologies have begun to capture the low end of the frequency and performance band. In the future, the silicon based processes will look to capture higher and higher frequency applications.

8.1 Existing Companies

There are many companies in the semiconductor space and more specifically the high frequency space. The companies reviewed below are likely to serve the high performance millimeter wave market now or in the future. These companies may be developing their own technology either through advancing their existing processes or developing new materials. Conversely, many of these companies may be possible customers looking to either purchase wafers or license our technology.

The companies discussed below are only companies that possess the ability to manufacture semiconductor products not so called "fabless" semiconductor companies.

TriQuint Semiconductor, Inc (NASDAQ: TQNT)

TriQuint Semiconductor operates a 6" fab utilizing gallium arsenide (GaAs) instead of silicon as the substrate (base) for its analog, digital, and mixed-signal integrated circuits (ICs). TriQuint's GaAs ICs are used in cell phones, fiber-optic and satellite telecom equipment, data networking devices, and aerospace gear. TriQuint's high frequency product offerings extend into the LMDS market at 38 GHz.

TriQuint offers diversified millimeter wave GaAs processes for both aerospace and commercial communications markets. These processes include the MESFET, 0.25-micron pHEMT, HFET, and HBT supporting both defense and emerging commercial applications.

The millimeter wave division is an industry leader in GaAs MMIC technology for 10 to 60 GHz applications ranging from high-performance, advanced phased-array radars for defense and space applications, very high frequency radios including LMDS commercial point-to-multipoint and point-to-point communications market, and 10 Gbps to 40 Gbps transceivers for fiber optic communications.

Below is chart displaying some of the product offerings from TriQuint in the high frequency regime. As the chart shows, TriQuint is well positioned up to 45 GHz in the power amplifier product area.

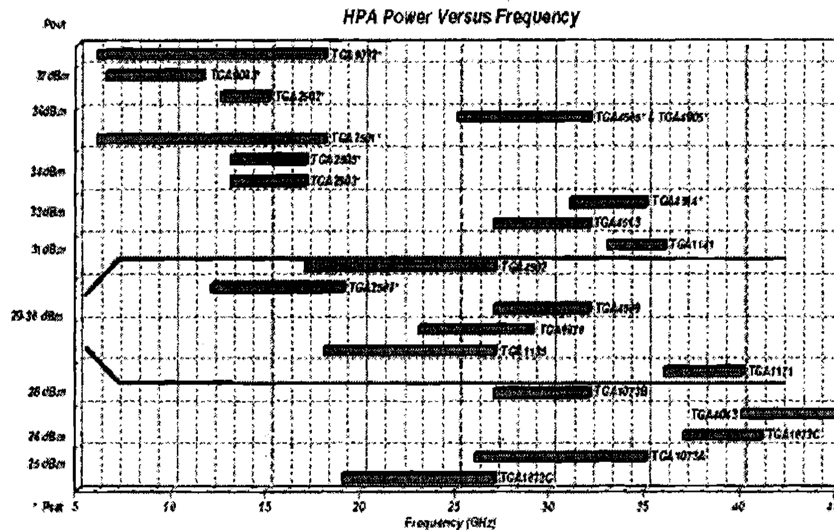


Figure 8.1: Triquint's High Power Amplifier (HPA) product offerings (Triquint).

Triquint's existing position in high frequency applications and knowledge of GaAs processes make it an important possible customer/ competitor. The company is not

familiar with Si based processes and would benefit from the ease of integration of our product with its exiting GaAs fab.

Bookham Technology, PLC (NASDAQ: BKHM)

Bookham mainly utilizes two technologies, GaAs and InP. The company produces high frequency and high speed products based on the technology of the semiconductor GaAs with its inherent high electron-mobility. GaAs based products range from satellite communications, military radar systems and commercial wireless networking. Bookham's InP process is used to manufacture optoelectronic components.

Bookham has recently made acquisitions of optoelectronics divisions of Nortel and Marconi as well as small optical companies such as Ignis Optics. This solidifies their position in the optoelectronic industry and thus the InP industry. Bookham's knowledge of both InP processes and high frequency applications makes them a competitor in the market space we are targeting.

Celeritek, Inc. (NASDAQ: CLTK)

Celeritek designs and manufactures GaAs semiconductor components and GaAs-based subsystems used in defense applications and commercial communications networks. Their GaAs-based subsystems are designed for missile guidance, radar applications and electronic countermeasures. The GaAs semiconductor components primarily consist of transmit solutions, including power amplifiers, control devices, gain blocks and millimeter wave devices for use in defense and commercial applications. Commercial applications include wireless communications networks and satellite systems.

Vitesse Semiconductor Corp. (NASDAQ: VTSS)

Vitesse offers products utilizing both GaAs and InP. The primary markets for the company are communications and storage. Vitesse's products are suited for a variety of existing and next-generation Enterprise, Access, Metro and Core applications. Products are manufactured using CMOS (over 95% of all new designs), InP, SiGe, and GaAs. The CMOS and SiGe work is outsourced to foundry companies such as IBM, TSMC, and UMC. Vitesse has made a strategic move to keep InP and GaAs manufacturing in-house, realizing that knowledge of these processes is highly valued. Vitesse's existing use of high performance materials positions the company as a major competitor to our technology.

ANADIGICS, Inc. (NASDAQ: ANAD)

Anadigics is a leading supplier of gallium arsenide integrated circuits (GaAs ICs) for communications markets. The company designs and manufactures radio frequency integrated circuit (RFIC) products for growing broadband and wireless communications markets. Anadigics is a pure-play RFIC Company featuring III-V GaAs technologies, InGaP HBT and 6-inch GaAs fab and module manufacturing.

RF Micro Devices, Inc. (NASDAQ: RFMD)

RF Micro Devices (RFMD) makes a variety of radio-frequency (RF) integrated circuits such as amplifiers, attenuators, mixers, modulators, and transceivers for wireless communications devices such as cellular phones and base stations, wireless LANs, and cable TV modems. Most of the company's chips are made from gallium arsenide (GaAs). The company's GaAs chips are manufactured through a licensing agreement with Northrop Grumman. The company operates one 4" GaAs fab and is beginning to ramp

up a 6" GaAs fab. RFMD also manufactures silicon germanium, silicon CMOS, silicon BiCMOS, GaAs MESFET, InGaP HBT, and InGaAs pHEMT products.

Velocium

Velocium is a subsidiary of Northrop Grumman that manufactures microwave and millimeter wave monolithic integrated circuits, including power amplifiers, low-noise amplifiers, broadband amplifiers, mixers. The MMIC product offerings range in operating frequency for DC to 100 GHz. The company also offers InP and GaAs foundry services. The company operates 3" and 4" wafer fabrication facilites.

8.2 Financial Comparison

To understand our competition, it is worthwhile to briefly review the size and financial position of each. The compound semiconductor industry has recently suffered from a market correction. Many companies over invested in compound semiconductor capacity and development programs only to have the industry almost collapse. To date there is a continued negative buzz around the industry but companies are beginning to recover. Below is a brief comparison of financial data for the companies described above. The point is to show the market history for these companies to get a sense of possible development efforts. Also to notice is the varying size of the companies in this space. Anadigics, the pure-player in the relevant market, is set in the middle of the pack behind the larger companies such as RFMD, Vitesse, and Triquint. Anadigics is considered a pure-player because all of the other companies are involved in silicon based processing as well as GaAs.

Revenue ($MM)

	1998	1999	2000	2001	2002
Anadigics	86,075	131,159	172,268	84,765	82,564
RF Micro Devices	45,350	152,852	288,960	335,364	369,308
Skyworks	112,271	216,415	378,416	260,451	
Triquint	209,305	263,939	460,590	334,972	172,197
Vitesse	181,169	281,669	441,694	383,905	151,738
Celeritek	56,317	41,128	48,211	85,062	57,050

Net Income ($MM)

	1998	1999	2000	2001	2002
Anadigics	(9,558)	2,588	18,892	(107,120)	(55,886)
RF Micro Devices	(523)	19,521	50,094	34,974	(20,584)
Skyworks	(23,064)	(318,924)	(66,479)	(14,915)	
Triquint	22,250	55,640	150,693	(26,211)	(158,560)
Vitesse	48,634	61,151	27,889	(111,875)	(883,526)
Celeritek	3,991	(7,538)	(6,824)	(10,602)	(22,618)

Total Shareholders Equity ($MM)

	1998	1999	2000	2001	2002
Anadigics	137,807	276,649	328,832	226,636	171,088
RF Micro Devices	66,763	230,906	303,153	376,498	389,685
Skyworks	187,196	275,568	466,416	287,661	
Triquint	231,492	460,315	674,123	682,774	525,672
Vitesse	361,646	502,381	1,105,402	1,329,005	482,705
Celeritek	-	-	-	170,525	139,688

Table 8.1: Financial Comparisons for Competitors

The data above illustrate the market boom in 2000-2001 and the subsequent market correction. All of the companies saw a spike in revenue, net income, and shareholder equity in that period. This allowed these companies to begin development projects on advanced semiconductor materials such as GaAs and InP. There was a sense that there would be a large market blossoming and each wanted to be positioned to service the new market. The market never reached the speculated level and many companies were left with significant loses. Many companies had to build new capacity to handle the expected volumes; they were now left with excess capacity and needed to sell off assets. Table A.2 lists recent fabrication facility closings or purchases.

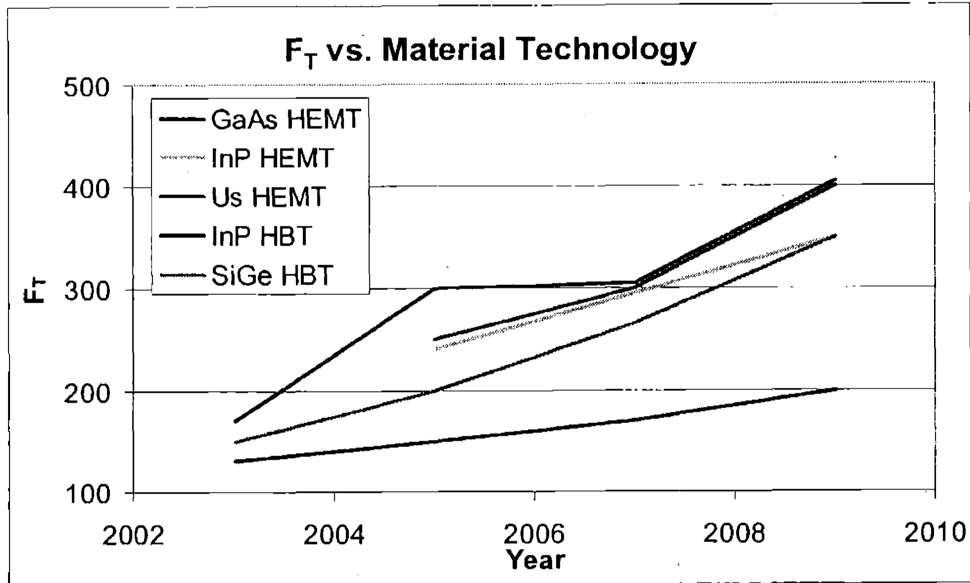
Company	Action
Vitesse	Closing 6" Fab
Infineon	Closing 6" Fab Sold 6" Fab to Triquint
Nortel	Closing 6" Fab (no more capacity)
Skyworks	Closing 4" Fab
Filtronic	Closing 6" Fab
Agilent	Closing 6" Fab

Table 8.2: Fabrication Facility Closings and Purchases[17]

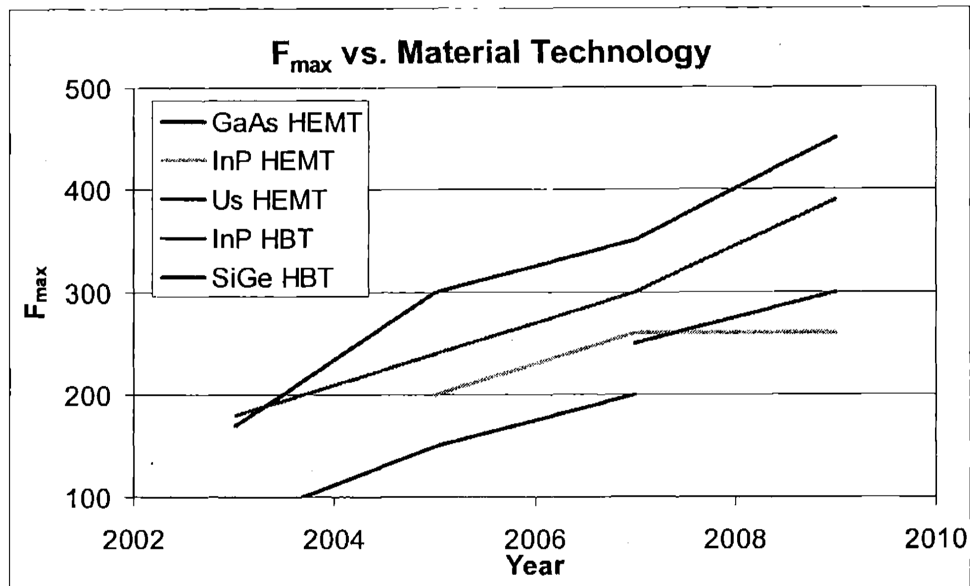
8.3 Material Competition

There are three basic sources of materials competition for our innovation; Si based processes (Si CMOS, SiGe), GaAs, and InP. The competition between the materials is focused around performance, cost, and the trade-off between these two. Of these three, the Si based processes pose the greatest threat because of industry knowledge and momentum. In this section, I compare the advantages and disadvantages for each material.

Much of the competition between devices fabricated on the various substrates is on two device parameters, f_T and f_{max}. These two figures of merit are always stated with a new device introduction. The two figures below forecast the future increase in these two device parameters. The figures compare various devices made from variety of processes. The InP HBT is consistently the top performing material-device combination.



a)



b)

Figure 8.2: Future trend in a) f_T and b) f_{max} for HEMTs and HBTs fabricated on GaAs, InP and SiGe.

Industry consortiums predict a similar trend in material-device performance. The International Technology Roadmap for Semiconductor group published the figure below to represent the future trend in performance.

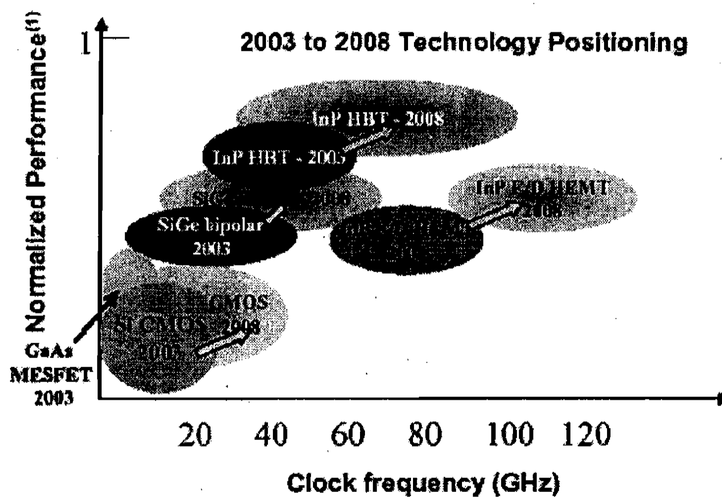


Figure 8.3: Future Performance for varying device technologies (ITRS 2003).

As is seen in almost all performance based technology trend figures, InP outperforms each available technology. What is usually missed is the progress the Si based processes (SiGe, CMOS) are making towards the higher performance technologies.

Silicon Based Processes

Silicon, representing over 95% of the semiconductor market, is the material of choice. Companies and research labs are working feverishly to improve the performance of Si based processes. Evident of that is the emergence of SiGe and Si BiCMOS processes. Si BiCMOS processes integrate the analog and RF functions of SiGe devices with the digital functions of CMOS[18]. The intent is to integrate what were once multiple chips in a device into one single silicon chip. What separates Si from the other semiconductor materials is the ability to integrate quality analog devices and passive elements.

Applications in the 1-5 GHz range, such as small signal functions, can be effectively implemented in SI BiCMOS but high power blocks (HPAs and antenna switches) benefit from the maximum voltage increase and cutoff frequency of GaAs. RF

CMOS plays a role in simple modulations where ultimate analog performance is not required (e.g. short range radio). At frequencies between 5-10 GHz, SiGe favorably competes with GaAs devices for broadband low-noise amplifiers and high speed mixed mode circuitry. Within in this frequency range, power devices still benefit from GaAs. Above 10 GHz, there are no commercially available Si processes[19].

The momentum behind the desire for Si based processes is simple and obvious. Many companies have already made significant investments in silicon processing, silicon is the cheapest semiconductor material, silicon has the largest knowledge based of any of the other materials, and silicon is available in larger wafer sizes. Any comparable semiconductor device made on silicon will be at a significant cost reduction to GaAs or InP.

Cost: Silicon is by far the cheapest material set. Compound semiconductors may have a performance edge over Si in speed, noise figure, and PAE, but Si benefits from higher levels of integration and greater economies of scale[18]. Products using Si can be produced cheaper that GaAs because of lower substrate costs, lower costs due to high volume processing, and lower production costs associated with using 8" and 12" wafers. SiGe benefits from its compatibility with Si CMOS processes and the economies of scale that are associated with these technologies.

Future: The main obstacle for high performance RF systems in Si CMOS is overcoming the poor quality of integrated passive components. In RF circuits the matching and quality of the surrounding passive component network are more important than in digital circuitry[20]. In 2002, compound semiconductors had 1.2% and SiGe had

0.2% of the total semiconductor market. In 2007, it is predicted that GaAs increase to 1.6% and SiGe to 0.8%[18].

Gallium Arsenide

Our innovation has significant performance advantages but GaAs will come in at a lower cost. In applications where performance can be sacrificed for cost, GaAs will be the material of choice. Most likely, GaAs will also be in facilities using our enhanced substrate. Since the materials are completing compatible, fabrication facilities will be les likely to discontinue their pure GaAs processing. Swapping between the two materials will be seamless for these companies.

Cost: GaAs processes are not as complicated as Si base processes. This is a result of fewer device and metal levels, thus fewer masks. Conversely, GaAs' lower thermal conductivity results in longer soak times than Si for high temperature processing steps[18]. In processing, many steps are conducted at elevated temperatures and these steps are not performed until the wafer reaches the desired temperature uniformly across the wafer. This longer soak time is a major contributor to the added processing costs associated with GaAs.

Growth: Industry surveyors predict GaAs microelectronic devices to grow at a CAGR of 11% until 2006. The devices include discretes, digital ICs, and MMICs.

Indium Phosphide

With respect to performance, InP poses the greatest threat. If the costs associated with the fabrication of InP (raw materials and processing) were to decrease, the material would become a serious competitor. Costs must decrease by at least a factor of 10. After the downturn in the compound semiconductor market, development of applications for

InP have significantly decreased. Most companies are adverse to spending money on InP again. Currently, InP is used in applications that require the highest performance and that are not sensitive to costs. Many industry representatives would if InP will ever challenge GaAs except where InP is the only choice because of performance requirements. Most industry experts feel metamorphic technologies, such as the one presented here, will supply the necessary performance gains at a lower cost than InP[21].

Performance: After cost, power consumption is the most important metric. At a given device speed, SiGe has four times the power consumption of an InP device. For a given power consumption specification, a designer can operate a 1000 InP gates versus 100 SiGe gates. At application frequencies greater than 50 GHz, the dominant constraint is power. The main driver for this disparity is InP's lower turn-on voltage. InP is quoted as having a turn-on voltage of 0.75V as compared to 0.95V for SiGe[22]. For a handset application, these power saving directly translate to into longer battery life.
InP benefits from the existing GaAs knowledge base in manufacturing processes and advancements. However, both technologies are generations behind Si in critical lithography dimensions. One might think this will limit InP's ability to compete in performance since Si gate sizes are considerably smaller. This is not true. A SiGe HBT with 0.13 um emitter cannot compete electrically with InP devices with ten times the emitter size[23].

Future: A representation from InPhi, a fabless semiconductor company specializing in InP, predicts the 40 Gb/s market is 3 years away. What is in question is whether or not companies will simply elect to upgrade their existing 10 Gb/s systems to

make them more robust. The InPhi representative noted recently seeing more activity in the 40Gb/s space[22].

Sources from Velocium suggest that the company will be using InP power amplifiers in wideband-CDMA handsets and MMICs for other wireless systems. Other industry sources are hesitant about pushing InP into the cost competitive wireless power amplifier market. InP is recommended for higher frequency applications where you need volts not just speed, SiGe is unable to provide both. The source also contradicts InPhi in that Velocium sees the 40 Gb/s adoption continually moving out. Customers are content with their current 10 Gb/s systems[22]. The implication to our product is that sales would rely on replacements of old systems and not adoption of new technologies. The growth in these two situations is completely different.

Section 9: Conclusions & Suggestions for Future Work

9.1 Process Summary

A self-aligned mesa process was developed to fabricate a prototype device. The benefit of this process is that the contact metal deposited is used as the etch mask for each layer, eliminating the need for an additional lithography step. The complete process was made up of three lift-off steps accompanied by the necessary patterning and etching steps. In order to avoid patterning and then etching deposited metal, a lift-off process was used to create the metal contacts. After the lift-off step was complete, the remaining metal serves as an etch mask used to define the device. Using selective etches, material was removed around the metal. The etch will not laterally etch the material under the metal. As a result, a mesa of material is left behind. This mesa defines the geometry and contact area for that device level. The resulting device is a three tiered mesa structure. This process greatly reduces the complexity of defining the contact metal by eliminating the need to etch metal away. Due to the problems encountered with identifying selective etches, the device was not fully processed through to the collector level. The process was proven to work on the emitter level of the device.

Future work should focus on processing a device through the collector level. One of the obstacles in the process that still needs to be proven is the subsequent metal depositions and etches. Multiple metal depositions may affect the contact resistance. For example, the emitter will undergo three metal depositions. Within the scope of this thesis, we were targeting DC measurements and contact resistance would not have greatly affected the results. Other work should also be focused on addressing improvements in

RF performance. The mesa device is not optimal for RF measurements. Therefore, an improved device would need to be used in order to obtain meaningful RF measurements.

9.2 Market Analysis Summary

The technology and derived products offered customers significant cost saving and performance enhancements over existing products and technologies. The ability for the technology to be produced in a variety of wafer sizes allows the technology to be integrated with and extend the life of existing manufacturing tool sets in a fabrication facility. The enhanced electrical performance allows designers to reach next generation performance specifications with current generation tooling and designs. The technology also allows the customer to pull next generation material designs forward without changing over their manufacturing toolset, providing a performance edge over their competitors.

The market analysis yielded the millimeter wave market, 10-100 GHz, as the focus market for our technology. Most devices used are composed of epitaxial layer stacks that are composed of ternary compounds derived from Group III and V elements of the periodic chart. Device properties and performance are critically dependent on the materials used and the layer thickness and doping. These parameters tend to be manufacturer specific and proprietary resulting in a wide variety of device design and performance. What drives such variety in performance are the numerous trade-offs between power, efficiency, noise, breakdown, and linearity in mm-wave devices. The trends in performance of these devices are driven by trade-off manipulation and bandgap engineering of the epitaxial layer stack. In the end, companies in this space are competing on the quality of their product and the performance. Suppliers boast low

defect levels, high electrical performance, and advanced materials. Since high commercial volume products have not reached this space yet, cost is not the number one driver in this space. Therefore, the added cost of our technology is overcome by the enhanced performance and by the economies of scale associated with using larger wafers.

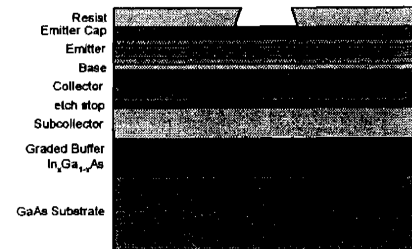
Competition for the technology was identified on two fronts. The innovation faces competition from existing companies serving the market or those targeting to enter the market in the future. The other form of competition is silicon based semiconductor processes and GaAs based processes. The development of these technologies continues to increase performance especially in the case of silicon based processes. The Si based processes will prove to be the greatest threat to our technology. There is great incentive within the semiconductor industry to develop high performance Si based processes. The main drivers for this are the low costs associated with Si processes and the large existing knowledge and capital equipment base of Si processes.

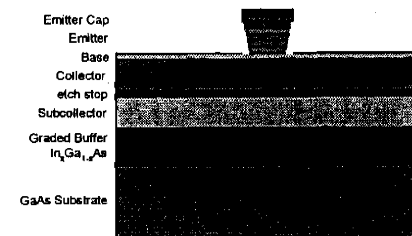
Once the DC and high frequency device enhancements have been characterized, research should continue to develop a specific market and application for the technology. Customers are going to need to be educated about the benefits and ease of integration associated with the technology.

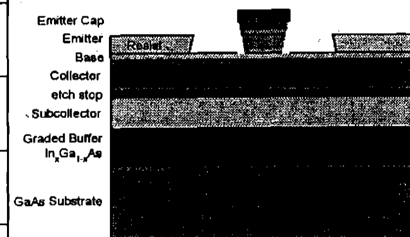
Appendix A: HBT Process Flow

The following is the detailed process flow developed to fabricate an HBT device.

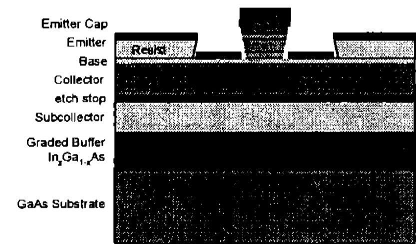
Process Step	Location/ Tool	Description
Clean/ Rinse	TRL acid-hood	Initial Clean of wafer
Growth	MOCVD	Growth of graded buffer layer
Rinse/ Clean	TRL acid-hood	
Pre-Bake	TRL HMDS	HMDS Pre-Bake
Spin On Resist	TRL Coater	AZ 5214E Image Reversal resist
Cure Resist	TRL Pre-Bake	Follow AZ 5214E recipe
Litho	TRL EV1	Follow AZ 5214E recipe
Develop	TRL	AZ 422
Evap Dep	TRL eBeamAu	Deposit Emitter metal Ti/Pt/Au as per recipe
Strip Metal and Resist	TRL Photo-wet-Au	Acetone – complete liftoff
Rinse	TRL acid-hood	Clean surface
Wet Etch	TRL acid-hood	H_3SO_4: H_2O_2: H_2O (3:1:100) Remove Emitter Cap
Rinse	TRL acid-hood	Clean
Wet Etch	TRL acid-hood	HCl: H_3PO_4: H_2O (1:1:50) Remove Emitter
Rinse	TRL acid-hood	Clean
Pre-Bake	TRL HMDS	HMDS Pre-Bake
Spin On Resist	TRL Coater	AZ 5214E Image Reversal resist
Cure Resist	TRL Pre-Bake	Follow AZ 5214E recipe
Litho	TRL	Follow AZ 5214E

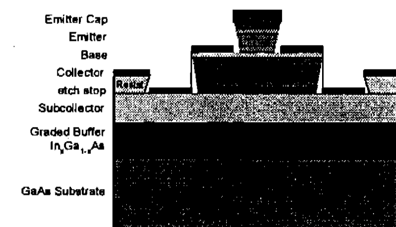






	EV1	recipe
Develop	TRL	AZ 422
Evap Dep	TRL eBeamAu	Deposit Base metal Ti/Pt/Au as per recipe
Strip Metal and Resist	TRL Photo-wet-Au	Acetone – complete lift off
Rinse	TRL acid-hood	Clean surface
Wet Etch	TRL acid-hood	H_3SO_4: H_2O_2: H_2O (3:1:100) Remove Spacer, Base, and Collector
Rinse	TRL acid-hood	Clean
Pre-Bake	TRL HMDS	HMDS Pre-Bake
Spin On Resist	TRL Coater	AZ 5214E Image Reversal resist
Cure Resist	TRL Pre-Bake	As per AZ 5214E recipe
Litho	TRL EV1	Follow AZ 5214E recipe
Develop	TRL	AZ 422
Evap Dep	TRL eBeamAu	Deposit Collector metal Ti/Pt/Au as per recipe
Strip Metal and Resist	TRL Photo-wet-Au	Acetone
Rinse	TRL acid-hood	Clean surface





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