

**Active Filters for 1 MHz Power Circuits
Under Strict Ripple Limitations**

by

Leif E. LaWhite

Submitted in Partial Fulfillment of
the Requirements of the Degrees of

Bachelor of Science and Master of Science
in Electrical Engineering and Computer Science

at the

Massachusetts Institute of Technology

February 1987

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Abstract:

Recent advances in MOSFET technology have moved the switching frequencies of power circuits into the mega-Hertz range. The drive to these higher switching frequencies is motivated entirely by the smaller energy storage elements that supposedly result. Unfortunately, at these very high frequencies, the allowable ripple levels on the input and output of the power circuits are often much lower than they are at lower frequencies. This then requires greater ripple attenuation which means that all of the desired energy storage reduction cannot be achieved. As switching frequencies are pushed higher, the passive filtration elements often come to dominate the size and cost of the converter.

In many cases, however, some of the large, costly, passive filter elements can be replaced with small, simple, active circuits. The result is savings in cost, size, and weight, of the overall filter. It is the purpose of this thesis to outline these cases and develop these active circuits.

The thesis first describes the situations in which these active filters find their greatest import. It then moves on to developing the theory and evaluation criteria surrounding these filters. After discussing in depth, the various filter topologies, and available active devices, it presents a working circuit which was constructed in the lab. The performance of this circuit agrees quite closely with both theory and simulation, verifying all of the previous analysis.

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Acknowledgements

I owe thanks to many people for their help in the research and writing of this thesis. Foremost is my advisor Marty Schlecht, for his interest, unending guidance, and helpful prodding during the long research and construction stages of this work.

Also Anne Grossetête receives many thanks for all the hours she put into proofreading, checking equations, and commenting on the many rough drafts.

Andy Goldberg, Barry Culpepper, Leo Casey, and Chris Wright have all helped out when in a pinch I needed a few electrical components or bits of inspiration.

Last I'd like to thank my parents for their patience through this whole endeavor.

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Chapter 1

Introduction

The drive to higher switching frequencies in power circuits is motivated entirely by the smaller energy storage elements that result. For the same allowable ripple levels at the input and output of a power circuit, an increase in the switching frequency of a factor of ten should reduce the energy storage requirements, and hence the size of the filter elements, by the same factor. As a result, switching frequencies are now being pushed into the mega-Hertz range.

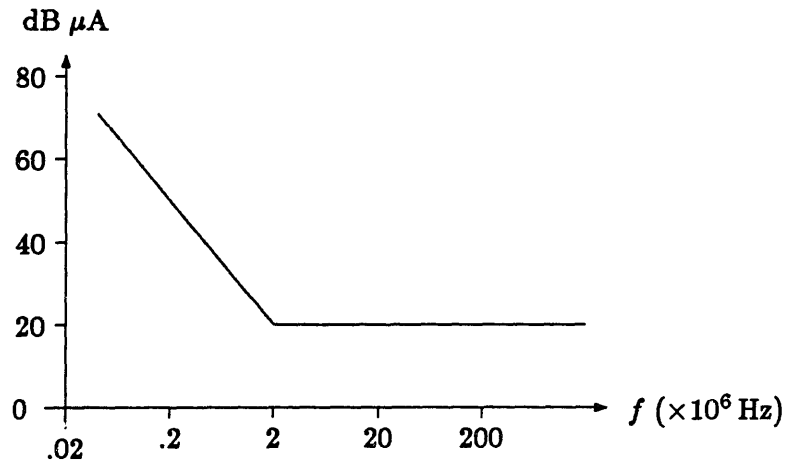


Figure 1.1: MIL-STD-461B CE03 Current Ripple Specification

Unfortunately, because of increasingly strict EMI/RFI limitations imposed by both commercial and military standards in this frequency range, much of the desired energy storage reduction cannot be achieved. For example, under MIL-STD-461B CE03, a military current ripple specification shown in Fig. 1.1, the allowable input ripple current decreases at 30 db/decade until 2 MHz where it levels off at 10 μ A. Thus, a 2nd order LC filter designed to work at 100 KHz would exceed this specification by only 10 db at 1 MHz. This corresponds to an energy storage reduction in the filter elements of only

1.8, instead of the factor of 10 that was anticipated.

Furthermore, under this specification the allowable ripple levels are mandated as an absolute, rather than a relative value. A converter drawing 5 A at 1 MHz would therefore need an input ripple current attenuation of over 100 db to meet this specification.

In order to use reasonably sized filter elements and still achieve these high attenuation levels, fourth-order LC filters are necessary. This more complex filter design makes control of the power circuit very difficult however, especially when one is present at both the input and output ports of the converter.

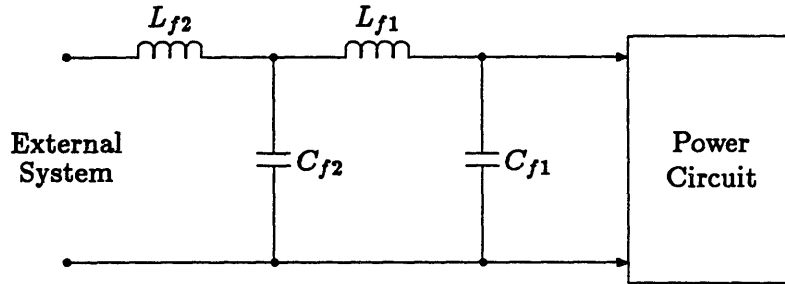


Figure 1.2: Power Circuit with Fourth-Order Ripple Filter

If the 5 A, 1 MHz converter mentioned above was supplied from a 60 V bus through a fourth-order input filter as shown in Fig. 1.2, the outer three filter elements would handle very small ripple energies. They would all have to be sized to handle the full dc energies of the converter, however. In this simple example, the dc-energy to ripple-energy ratio for C_{f2} is more than 5×10^6 .

Since the ripple energies associated with these outer elements are so small, it should be feasible to replace them with active circuits that provide the necessary high-frequency impedance. Because they can be integrated, these active circuits should be smaller, lighter, and cheaper than the passive components they replace. These active filter circuits would be constructed such that they handle only the ripple energies associated with the component they replace. Although they would then dissipate these energies, the loss would be acceptable in return for the savings in size, weight, and cost that result.

Though such active filters could always have been built, they are just now becoming feasible because of higher switching frequencies in power circuits. At 100 kHz and below, the allowed ripple levels are generally quite large, so that any active filters would dissipate objectionable amounts of power. Now that 1 MHz power circuits are being made and subject to extremely stringent ripple specifications, these active filters could have tremendous practical import.

1.1 Outline

The purpose of this thesis is to investigate the design and implementation of practical active filter circuits for such applications. The document is divided into 7 chapters. Chapters 1 and 2 introduce the topic and explain where and why active filters are useful for high-frequency power circuits.

Chapter 3 is an overview of some of the desirable and undesirable parameters concerning the design of suitable active filters. Analysis in Chapter 3 is based entirely on generalized circuit elements and serves to identify some of the useful (and useless) circuit topologies.

Chapter 4 specializes the results of Chapter 3 by using a still-general three-terminal model as a building block for those circuits of Chapter 3. Chapter 5 further specializes the analysis by adapting the earlier three-terminal model, first to bipolar transistors, and then to field-effect transistors. The analysis in these two chapters is used to select 'the best' active filter topologies for our purposes.

Chapter 6 investigates some of the other topics associated with actually constructing useful active-filter circuits. It then presents a design that was actually built, and evaluates its performance in terms of a comparison to theoretical performance, and utility as a ripple-filter for power circuits.

Chapter 7 is a conclusion which summarizes this piece of research and suggests directions for future work.

1.2 Previous Work in This Area

The idea of using linear active circuits to aid in eliminating the noise generated by switching circuits is not new. Indeed, any standard linear voltage regulator can be thought of as working in this area, as it generally attempts to, with the aid of a large filter capacitor, smooth the output of a diode bridge.

Unlike linear voltage regulators, however, these circuits are designed to be used *with* high-frequency switching converters. In addition, these circuits will be constructed to see only the ripple-energies associated with a given converter. In this way they will be valuable for use with very-high-voltage and very-high-current converters while maintaining minimal power dissipation. This, along with the difference in operating frequencies, will make these circuits very distinct from those typically found in linear voltage regulators.

In his Master's Thesis [9], George Yundt proposed using active smoothing circuitry on the output of switching amplifiers to simultaneously achieve the high-efficiency of a switching amplifier, and the low noise of a linear amplifier. His work too, differs from this work in that his active circuitry was designed to follow varying output voltages, and his switching frequencies were at least a factor of ten below those I am considering.

J. Walker [10] has considered this subject. His circuits, though, are also designed for frequencies ten times lower than what I'm considering, and he only achieves what will come to be called, a capacitor-enhancement, or gain, of about 4.

Chapter 2

Ripple Filters for Power Circuits

A power circuit normally has a ripple filter at both its input and output. These filters are of two types: Current-filters prevent large ripple currents, generated within the power circuit, from reaching the external source or load. Voltage-filters do likewise with large ripple voltages.

2.1 Second-Order Filters

Second-order versions of each type of filter are illustrated in Fig. 2.1.

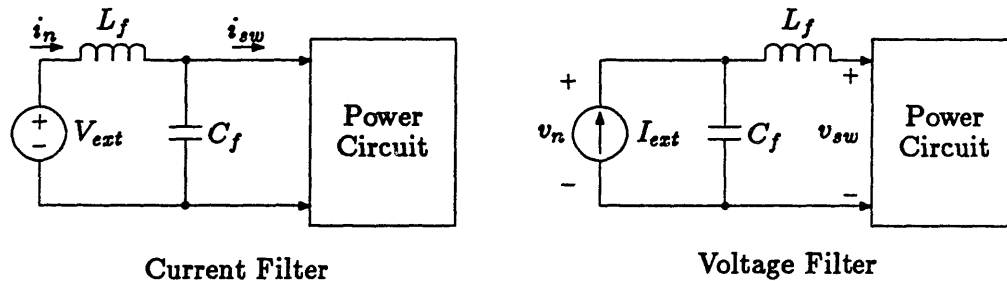


Figure 2.1: Filters for Power Circuits

Standard circuit analysis yields:

$$\frac{i_n}{i_{sw}} = \frac{v_n}{v_{sw}} = \frac{1}{s^2 L_f C_f + 1} \quad (2.1)$$

The resonant frequency of the filter is $\omega_o = 1/\sqrt{L_f C_f}$. For good filtration, the switching frequency of the power circuit is generally well above ω_o . In this situation (2.1) is simplified and re-arranged to:

$$L_f C_f \approx \frac{1}{s^2} \frac{i_{sw}}{i_n} \approx \frac{1}{s^2} \frac{v_{sw}}{v_n} \quad (2.2)$$

Thus, if the allowable ripple levels remain the same, an increase in the switching frequency of the power circuit allows L_f and C_f to be made proportionately smaller. Because these passive filter elements represent a significant portion of the total size, weight, and cost of the power circuit, reducing their value is of great importance. This is the motivation behind the drive to high switching frequencies in power circuits. As discussed in the introduction, however, the allowable ripple level is often more stringent at higher frequencies. In fact, the necessary filtrations are often so large that these second-order filters are not practical at all. In this situation, higher-order filters are necessary.

2.2 Fourth-Order Filters

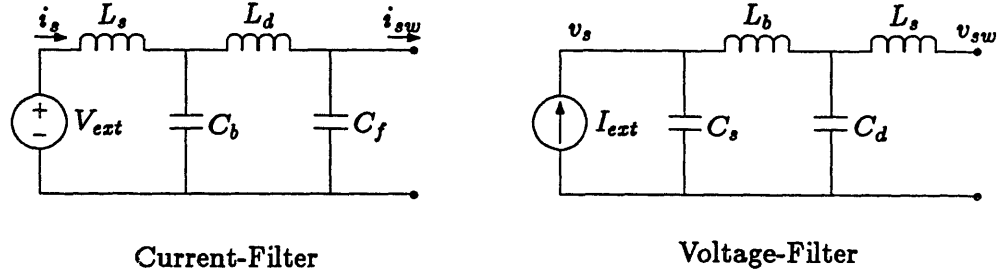


Figure 2.2: Fourth Order Passive Filters

Fourth-order versions of the two filter types are shown in Fig. 2.2. These can be evaluated on the basis of how much ‘better’ they perform than the second-order filters they replace. In the current-filters, for example, the fourth-order filter can be formed by starting with the second-order version from Fig. 2.1. C_f is left unchanged while L_f is split into two separate inductors L_s and L_d such that $L_s + L_d = L_f$. An additional element, C_b in this case, is then added between the two L ’s to complete the formation. An exactly dual transformation is carried out to form the fourth-order passive voltage-filter.

For the fourth-order passive filters above resonance:

$$\begin{aligned} \frac{i_s}{i_{sw}} &\approx \frac{1}{s^4 L_s L_d C_b C_f} = \frac{1}{s^2 L_{eff} C_f} \\ \frac{v_s}{v_{sw}} &\approx \frac{1}{s^4 C_s C_d L_b L_f} = \frac{1}{s^2 C_{eff} L_f} \end{aligned} \quad (2.3)$$

where

$$\begin{aligned} L_{eff} &\doteq s^2 L_s L_d C_b \\ C_{eff} &\doteq s^2 C_s C_d L_b \end{aligned} \quad (2.4)$$

The latter relation in each line of (2.3) looks exactly like the second-order relations from eq. (2.1) with L_f and C_f replaced by L_{eff} and C_{eff} . Thus, the gain of these

fourth-order over second-order filters could be defined as:

$$\begin{aligned} \text{gain}_{pass} &\doteq \frac{L_{eff}}{L_f} = \frac{s^2 L_s L_d C_b}{L_f} \\ \text{gain}_{pass} &\doteq \frac{C_{eff}}{C_f} = \frac{s^2 C_s C_d L_b}{C_f} \end{aligned} \quad (2.5)$$

Recalling that $L_s + L_d = L_f$ and $C_s + C_d = C_f$, and defining

$$L_p \doteq L_s || L_d = \frac{L_s L_d}{L_s + L_d} \quad \text{and} \quad C_p \doteq C_s \uparrow C_d = \frac{C_s C_d}{C_s + C_d} \quad (2.6)$$

the gains of the fourth-order filters can be re-written as:

$$\begin{aligned} \text{Current Filter:} \quad \text{gain}_{pass} &= s^2 L_p C_b \\ \text{Voltage Filter:} \quad \text{gain}_{pass} &= s^2 C_p L_b \end{aligned} \quad (2.7)$$

These ‘gains’ were achieved at the ‘cost’ of an extra element in both filters. The active filters to be described later will also achieve their gain at the cost of additional components. A basis for judgement of the active filters will, therefore, be the relative cost of these extra components.

Also, in situations where the equations are of an appropriate form, the gain of an active filter will be compared to the gain of these fourth-order passive filters. The emphasis here will be to show that active filters provide many times *more* gain to second-order filters than is possible with a simple transformation to a fourth-order filter.

Chapter 3

Active Filters - Overview

In the last chapter, 2nd-order filters were modified by splitting one of the elements and adding a new element. The resulting circuit performed better than the original. In this chapter, active filter circuits will be formed by again starting with a 2nd-order filter, splitting one element and adding active circuitry. The active circuitry for the current and voltage filters will be developed separately. There are several different topologies for each type of filter. The first will be developed in detail, subsequent ones will be just summaries of the resulting equations.

3.1 Inductor-Enhanced Current-Filters

In the active current-filter, C_f is left unchanged while the inductor L_f is split in two. Active circuitry, rather than a passive capacitor, is then added to make these two inductors appear larger. The factor by which the two inductors are made to appear larger will be referred to as the 'gain' of the active filter circuit.

3.1.1 Inductor-Enhanced Filter with Standard Drive

Consider the 2nd-order inductor-enhanced filter shown in Fig. 3.1. The amplifier is characterized by its input-impedance $Z_{in}(s)$, gain $A(s)$, and output-impedance $Z_{out}(s)$. Though these parameters, and many others to come, are functions of s , the (s) will typically be omitted from the equations for compactness.

The external-source ripple-current, i_s , flowing through L_s and Z_{in} creates a voltage across the amplifier input. This voltage is amplified and placed across L_d with polarity such that i_s will be driven to zero. If A were infinite, then the filter would be perfect and i_s would be equal to zero, as desired. A will not, however, be infinite, so a more quantitative derivation is necessary.

Gain Calculation

To determine the inductor-enhancing gain, the effective impedance Z_{eff} is defined as the ratio of the filter-capacitor ripple-voltage, v_r , to the external-source ripple-current,

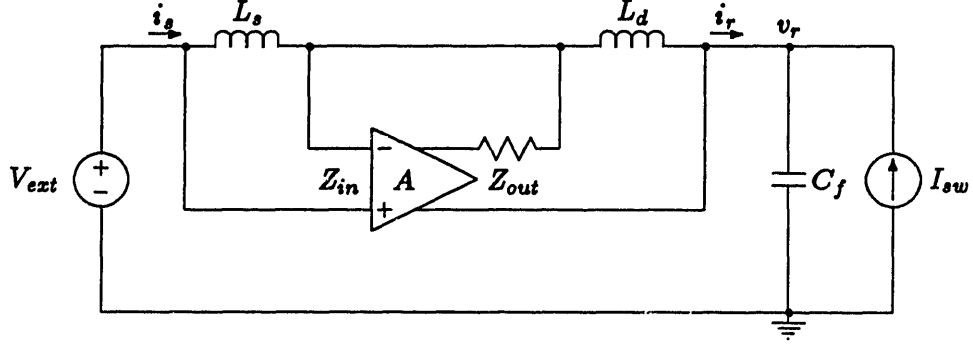


Figure 3.1: An Inductor-Enhanced Current-Filter Circuit

i_s . In this case, since $i_s = i_r$ and the V_{ext} source is an incremental short, Z_{eff} is the Thevenin-impedance seen to the left of C_f . The exact relation for Z_{eff} is:

$$Z_{eff} = \frac{v_r}{i_s} = \frac{s\{sL_sL_d[(A+1)Z_{in} + Z_{out}] + (L_s + L_d)Z_{in}Z_{out}\}}{(sL_s + Z_{in})(sL_d + Z_{out})} \quad (3.1)$$

Making the substitutions:

$$\begin{aligned} L_p &\doteq L_s || L_d = \frac{L_s L_d}{L_s + L_d} \\ \omega_s &\doteq \frac{Z_{in}}{L_s} \\ \omega_d &\doteq \frac{Z_{out}}{L_d} \end{aligned}$$

and re-arranging yields:

$$Z_{eff} = \frac{s\{sL_p[(A+1)Z_{in} + Z_{out}] + Z_{in}Z_{out}\}}{L_p(s + \omega_s)(s + \omega_d)} \quad (3.2)$$

L_{eff} is defined as Z_{eff}/s and is the effective inductance of L_s , L_d , and the amplifier. This L_{eff} could be used in (2.1) to find the attenuation for this filter.

$$L_{eff} = \frac{sL_p[(A+1)Z_{in} + Z_{out}] + Z_{in}Z_{out}}{L_p(s + \omega_s)(s + \omega_d)} \quad (3.3)$$

The inductor enhancement, or gain, of the circuit is then $L_{eff}/(L_s + L_d)$. Making this substitutions gives:

$$\text{gain} = \frac{L_{eff}}{(L_s + L_d)} = \frac{sL_p[(A+1)Z_{in} + Z_{out}] + Z_{in}Z_{out}}{L_s L_d (s + \omega_s)(s + \omega_d)} \quad (3.4)$$

For any reasonable amplifier gain A , the '+ Z_{out} ' term in the numerator can be neglected and the relation can be simplified to:

$$\text{gain} \approx (A+1) \left(\frac{Z_{in}}{L_s + L_d} \right) \frac{s + \omega_s}{(s + \omega_s)(s + \omega_d)} \quad (3.5)$$

where

$$\omega_x \doteq \frac{Z_{out}}{(A+1)L_p}$$

For future reference, re-substituting for ω_x , ω_s and ω_d gives:

$$\text{gain} \approx \frac{Z_{in}[sL_p(A+1) + Z_{out}]}{(sL_s + Z_{in})(sL_d + Z_{out})} \quad (3.6)$$

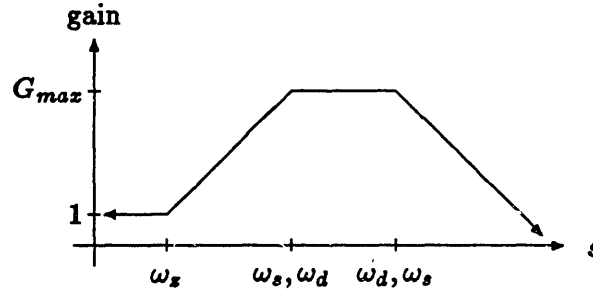


Figure 3.2: Bode-Plot of Gain for Inductor-Enhancing Circuit

A Bode-plot of this expression, assuming that A , Z_{in} , and Z_{out} are real, is shown in Fig. 3.2. The value of G_{max} depends on the relative values of ω_s and ω_d . The two possibilities are:

$$\begin{aligned} \omega_s < \omega_d & \quad G_{max} = (A+1) \frac{L_d}{L_s + L_d} \frac{Z_{in}}{Z_{out}} = (A+1) \frac{L_s}{L_s + L_d} \frac{\omega_s}{\omega_d} \\ \omega_s > \omega_d & \quad G_{max} = (A+1) \frac{L_s}{L_s + L_d} \end{aligned} \quad (3.7)$$

Notice that these two look identical except for the factor of ω_s/ω_d in the first. ω_s/ω_d in this region is ≤ 1 , though, so the highest gain is achieved by using $\omega_s \geq \omega_d$. In this realm, this circuit makes L_s and L_d appear larger by a factor on the order of A .

Maximum Effective Inductance

Another important feature to notice is that, for a given working frequency ω_{wf} , there is a fundamental limit on the maximum effective inductance, $L_{eff,max}$, that can be created with this circuit. Qualitatively, this can be understood by working backwards from the standard gain derivation. From (3.4), $L_{eff} = \text{gain} \times (L_s + L_d)$ which indicates that L_{eff} is linear in $(L_s + L_d)$. Unfortunately, increasing L_s and L_d arbitrarily does not result in correspondingly large values for L_{eff} because the gain is a function of L_s and L_d .

As L_s and L_d are raised in an *attempt* to raise L_{eff} , ω_s and ω_d of the gain relation are correspondingly lowered. As the higher of ω_s or ω_d crosses below the working frequency, the gain starts to roll-off with increasing L_s or L_d . In this region L_{eff} will

stop increasing with L_s and L_d , and instead will hold constant at a value given by the gain relation (3.6) above both ω_s and ω_d .

From (3.28), when ω_{wf} is greater than ω_s and ω_d :

$$L_{effmax} = (A + 1) \frac{Z_{in}}{\omega_{wf}} \quad (3.8)$$

which is no longer a function of L_s or L_d .

Thus, though this circuit provides inductor-enhancement, or gain, for values of L_s and L_d which cause the operating frequency to be between the two poles, there is a maximum value for the effective-inductance it can produce even when L_s and L_d are made very large. This may prove to be a serious problem if the applicable ripple-specification and power circuit demand an inductance in the current-filter which is above L_{effmax} .

The Loop-Transmission

The active filter circuit is a feedback structure, and as such has an associated loop transmission (LT). The characteristics of the LT govern the stability of the filter circuit.¹ Generally, the loop transmission will be closely related to the gain, and will have magnitude much greater than 1 at the circuit's working frequency. The frequency at which the $|LT| = 1$ is commonly known as the 'unity-gain-crossover' (UGC). Bear in mind though, that the 'gain' in the UGC is really a misnomer, for in these circuits the gain and the LT are quite distinct.

Above the working frequency, the LT will have to be 'rolled-off' so as to make the UGC occur before the angle of the loop-transmission, ($\angle LT$), is equal to 180° . The most sure-fire way to accomplish this is to roll-off the LT with a *single* 'dominant' pole and force *all* other poles to be above the UGC.

Gain/LT Figure-of-Merit Since the LT roll-off is being accomplished with a single dominant pole, there is a definite relationship between the UGC and the maximum possible value for the LT at the working frequency (LT_{wfmax}):

$$LT_{wfmax} = \frac{UGC}{\omega_{wf}} \quad (3.9)$$

All the parasitic poles of the circuits must be above the UGC, however, so raising the UGC will be difficult in practical implementations. To achieve a given gain, therefore, the circuit which has the lowest UGC will undoubtedly be the easiest circuit to successfully implement. Since $LT_{wfmax} \propto UGC$, the circuit with the lowest LT_{wf} will also be the one with the lowest UGC. The objective then is to construct active filter circuits with the highest possible gain/ LT_{wf} ratio. The gain/LT will, therefore, become a general figure-of-merit for comparing various active filter circuits.

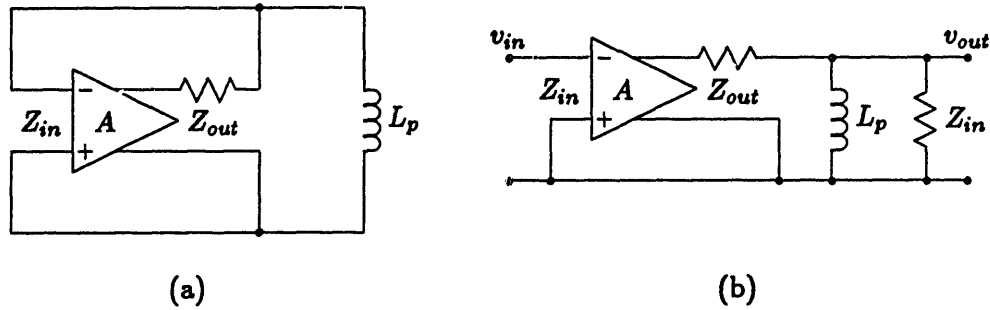


Figure 3.3: Circuits for LT Derivation

LT Derivation The LT is found by incrementally shorting both C_f and V_{ext} . The resulting circuit, shown in Fig. 3.3a, is then ‘broken’ and ‘loaded’ to become that of Fig. 3.3b. The v_{out}/v_{in} relation is then the LT for the original circuit.

A short derivation yields:

$$LT \doteq -\frac{v_{out}}{v_{in}} = A \left(\frac{Z_{in}}{Z_{in} + Z_{out}} \right) \frac{sL_p}{sL_p + Z_p} \quad (3.10)$$

where

$$Z_p \doteq \frac{Z_{in}Z_{out}}{Z_{in} + Z_{out}} \quad \text{and} \quad \omega_p \doteq \frac{Z_p}{L_p}$$

A bode plot of this simple relation, again assuming real amplifier parameters, is shown in Fig. 3.4.

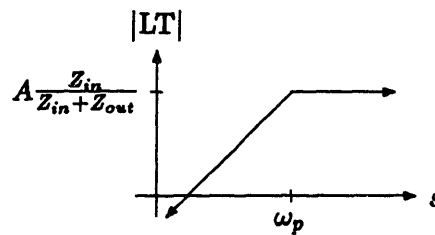


Figure 3.4: Bode-plot of Loop Transmission

Notice that this LT rises with a slope of 1 until ω_p where it levels off at a value of $AZ_{in}/(Z_{out} + Z_{out})$. To accomplish the LT roll-off discussed above, a pole will have to be *added* to the LT by modifying $A(s)$. This pole can theoretically be placed anywhere that adequately rolls-off the LT to keep the UGC below the parasitic poles of $A(s)$. Bear

¹See [4], Chapters 1-4, for a complete discussion of the LT, its identification, and its implications on the stability of feedback circuits.

in mind, however, that a pole in $A(s)$ to roll-off the LT, will also appear as a pole in the gain expression, eq. (3.5). To maintain maximum gain, therefore, it will generally be desirable to place this additional pole at, or just above, the circuit's working frequency.

Gain/LT Calculation

The figure-of-merit is the gain/LT ratio. Well above the zero in (3.6):

$$\frac{\text{gain}}{\text{LT}} \approx (Z_{in} + Z_{out}) \frac{sL_p + Z_p}{(sL_s + Z_{in})(sL_d + Z_{out})} \quad (3.11)$$

It is easy to show that the zero in this expression is *always* between the two poles. A bode-plot, therefore, looks like the one shown in Fig. 3.5.

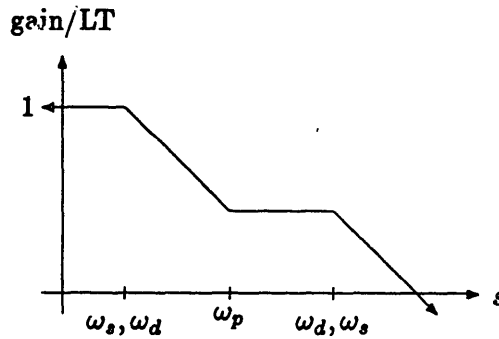


Figure 3.5: Bode-plot of gain/LT

From this simple analysis, it appears that the best performance will be obtained by operating below all the poles and zeroes of the gain/LT expression. This corresponds to the slope=+1 section of Fig. 3.2, so for maximum gain, ω_s and ω_d should be placed just above the operating frequency.

Even so, the gain/LT ratio for this circuit has a maximum value of 1. Thus, from (3.9), this circuit has a maximum gain:

$$\text{gain}_{max} = \text{LT}_{\omega_{fmax}} = \frac{\text{UGC}}{\omega_{wf}} \quad (3.12)$$

as dictated by the maximum value for the UGC which is still below all the parasitic poles of $A(s)$. For circuits intended to work at 1 MHz and above, this becomes a definite limitation on the gain; pushing the UGC, and hence all the parasitic poles significantly above 50 MHz can be quite difficult.

3.1.2 An Alternate Inductor-Enhancing Drive Topology

For a way to overcome this maximum gain limitation, the inductor-enhanced current-filter circuit shown in Fig. 3.6 is proposed. This circuit is obtained from the general

inductor-enhanced circuit in Fig. 3.1 by sliding the negative output lead of the amplifier through the filter capacitor, C_f , to ground.

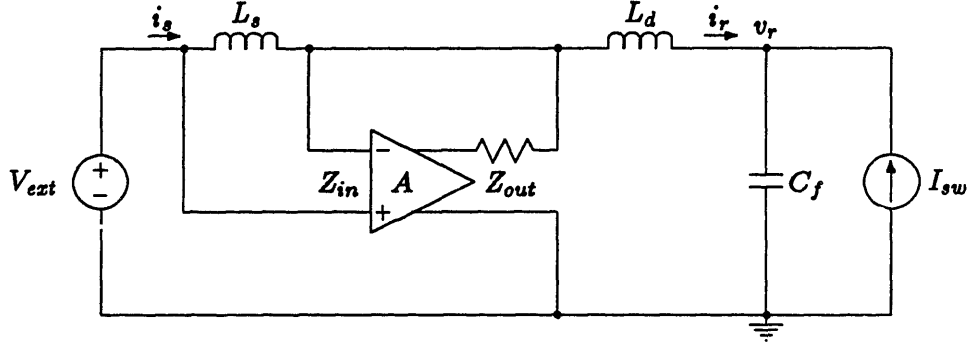


Figure 3.6: Alternate Drive for Inductor-Enhanced Circuit

A qualitative explanation of the difference between this and the previous circuit follows. The previous inductor-enhanced circuit can be thought of as imposing a non-zero voltage across L_d so as to *cancel* v_r and leave the ‘middle node’ at incremental ground. This circuit, on the other hand, can be thought of as trying to directly *hold* the ‘middle node’ at incremental ground. While the amplifier output voltage used to be approximately v_r plus the voltage on Z_{out} , it is now only the voltage on Z_{out} . The current through, and hence voltage across, Z_{out} is roughly the same in both. The output voltage of the amplifier is also related to i_s by the same equation in both. Thus, for the same v_r this latter approach ought to yield a smaller i_s . This translates into larger L_{eff} and therefore a larger gain.

Gain Calculation

For a quantitative derivation, the first thing to realize is that i_s does not equal i_r anymore. Thus $Z_{eff} \doteq v_r/i_s$ is no longer the Thevenin-impedance as seen from C_f . Instead,

$$Z_{eff} = s(L_s + L_d) \frac{Z_{out} + (A+1)Z_{in}}{Z_{out}} \frac{\left[sL_p + \frac{Z_{in}Z_{out}}{Z_{out} + (A+1)Z_{in}} \right]}{(sL_s + Z_{in})} \quad (3.13)$$

which has a single pole and a single zero. The gain is again $Z_{eff}/s(L_s + L_d)$:

$$\text{gain} = \frac{Z_{out} + (A+1)Z_{in}}{Z_{out}} \frac{\left[sL_p + \frac{Z_{in}Z_{out}}{Z_{out} + (A+1)Z_{in}} \right]}{(sL_s + Z_{in})} \quad (3.14)$$

For any reasonable amplifier gain A , the ‘ $Z_{out}+$ ’ terms should be negligible compared

to the $(A + 1)Z_{in}$ terms. Making this simplification yields:

$$\text{gain} = \left(\frac{Z_{in}}{Z_{out}} \right) \frac{sL_p(A + 1) + Z_{out}}{sL_s + Z_{in}} \quad (3.15)$$

Notice that this relation looks much like (3.6), the only difference being the absence of $'sL_d+'$ in the denominator here. A bode plot of this expression is shown in Fig. 3.7.

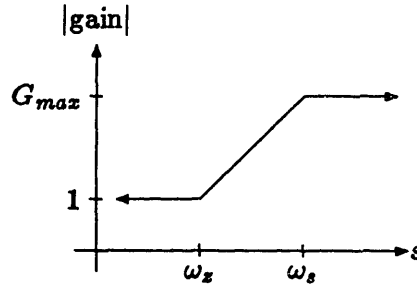


Figure 3.7: Bode plot of gain

Above both the pole and the zero the gain is maximized at

$$\text{gain}_{max} = (A + 1) \frac{L_d}{L_s + L_d} \left(\frac{Z_{in}}{Z_{out}} \right) \quad (3.16)$$

which looks exactly like the $\omega_s < \omega_d$ relation in (3.7). Thus at a first glance it appears as though this circuit is no better than the circuit from Fig. 3.1. Closer investigation, however, shows that the gain of this circuit can be made quite large by making Z_{out} small. On the other hand, making Z_{out} small in the previous circuit lowers ω_d until the assumption that $\omega_s < \omega_d$ is violated. Once this happens, the gain of the previous circuit stays at the $\omega_s > \omega_d$ value while the gain of this circuit keeps increasing as Z_{out} is made smaller.

Maximum Effective Inductance

This circuit has the added benefit of having no fundamental limit on the maximum effective inductance it can create. This fact can easily be seen by starting with the working frequency, ω_{wf} , in the high gain region defined above, and substituting $L_{eff} = \text{gain} \times (L_s + L_d)$ into (3.16):

$$L_{eff} = (A + 1) \frac{Z_{in}}{Z_{out}} L_d \quad (3.17)$$

The important difference here is that increasing L_d does indeed keep increasing L_{eff} proportionately because L_d is not associated with any gain-killing pole.

LT Analysis

The LT is again found by incrementally shorting both C_f and V_{ext} . This results in the *same* LT circuit as in Fig. 3.3, so the LT is the same as in (3.10).

Gain/LT Calculation

The general figure-of-merit is again the gain/LT ratio:

$$\frac{\text{gain}}{\text{LT}} = \left(\frac{Z_{in} + Z_{out}}{Z_{out}} \right) \frac{\left(sL_p + \frac{Z_{out}}{A+1} \right) (sL_p + Z_p)}{(sL_p)(sL_s + Z_{in})} \quad (3.18)$$

This expression has a pole at the origin, two zeroes, and another pole. Substituting the old definitions for ω_z , ω_s , and ω_p yields:

$$\frac{\text{gain}}{\text{LT}} = \left(\frac{Z_{in} + Z_{out}}{Z_{out}} \right) \left(\frac{L_d}{L_s + L_d} \right) \frac{(s + \omega_z)(s + \omega_p)}{s(s + \omega_s)} \quad (3.19)$$

A Bode-plot of this expression looks like Fig. 3.8.

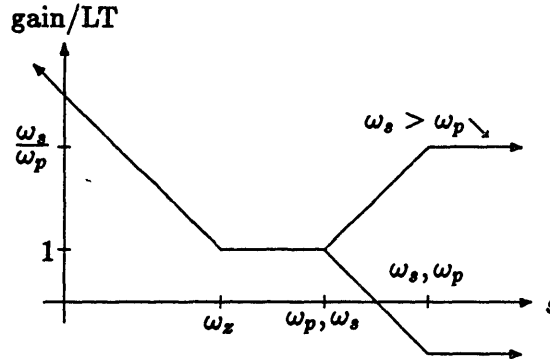


Figure 3.8: Bode-Plot of Gain/LT

From this Bode-plot, we see very quickly that if $\omega_s > \omega_p$ this topology can indeed yield $\text{gain/LT} > 1$ by operating *above* all the poles and zeroes. In the previous topology, the gain/LT was always ≤ 1 . Maximum gain/LT is achieved by making:

$$\frac{\omega_s}{\omega_p} = \left(\frac{Z_{in} + Z_{out}}{Z_{out}} \right) \left(\frac{L_d}{L_s + L_d} \right) \gg 1 \quad (3.20)$$

The region below ω_z also looks tempting for $\text{gain/LT} > 1$, but closer inspection of (3.15) reveals that the $\text{gain/LT} = 1$ in this region, so it is not of particular value.

Using a small L_s and a large Z_{in} to raise ω_s almost to the operating frequency, and a large L_d and small Z_{out} to lower ω_p yields:

$$\frac{\text{gain}}{\text{LT}} \approx \frac{Z_{in}}{Z_{out}} \quad (3.21)$$

which might be 10 to 100. Also under these conditions:

$$\text{gain} = (A + 1) \frac{Z_{in}}{Z_{out}} \left(\frac{L_d}{L_s + L_d} \right) \approx A \frac{Z_{in}}{Z_{out}} \quad (3.22)$$

which can easily be in the 1000 range. Thus, this circuit allows for quite high gains with reasonable UGC's, and it therefore seems to be superior to the earlier circuit. The requirements of a particular application, however, may alter that conclusion. For example, if the DC bus voltage of the power circuit is to be very high, it might be much easier to let the active-filter circuit 'hang from the bus', as in Fig. 3.1, than it is to place the amplifier output across the bus, as in the circuit of Fig. 3.6.

Consideration of Z_{out}

At present, the output of the amplifier in this circuit is connected through Z_{out} directly across the (potentially very high voltage) DC bus. In most cases, this mandates that Z_{out} contain *at least* a DC blocking capacitor. This capacitor sees the full DC bus voltage and is hence considered 'expensive' and should be made as small as possible.

The above equations, however, call for a low Z_{out} at the working frequency to achieve high gains. This factor will undoubtedly determine how small the DC blocking capacitor can be. Assuming that Z_{out} looks predominantly capacitive, ($Z_{out} = 1/sC_b$) as would be the case for a 'small' DC blocking capacitor, the gain can be derived to be:

$$\text{gain} = \frac{s^2 L_p C_b (A + 1) Z_{in} + s L_p + Z_{in}}{(s L_s + Z_{in})} \quad (3.23)$$

Because A in the s^2 term is quite large, the zeroes are a 'lightly damped' complex pair. A typical pole-zero plot is shown in Fig. 3.9.

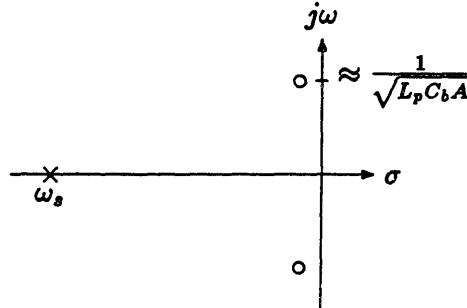


Figure 3.9: Pole-Zero Plot for gain with $Z_{out} = 1/sC_b$.

Here there is no maximum gain; even above the pole the gain continues increasing with slope=1. Above the complex zero pair, but below the pole at ω_s , the gain can be simplified to:

$$\text{gain}_{act} \approx s^2 L_p C_b (A + 1) \quad : \quad \frac{1}{\sqrt{L_p C_b A}} < s < \omega_s \quad (3.24)$$

Bear in mind that this relation is only valid where Z_{out} looks predominantly capacitive. At and above some frequency, the 'real' output impedance of any practical amplifier will come to again dominate Z_{out} . Whether this analysis, assuming capacitive Z_{out} , or the previous analysis, assuming real Z_{out} , is valid is determined by the operating frequency relative to this 'drive pole.'

Comparison to Fourth-Order Passive Filters: If Z_{out} does indeed look capacitive at the operating frequency, then it is beneficial to make the following observation. The gain of this improved circuit was achieved at the cost of the active circuitry plus that of C_b . Similarly the gain of a fourth order passive filter, (2.7), was obtained at the cost of just C_b . Thus, the gain of this active filter compared to the gain of the fourth-order passive filter gives a measure of the relative worth of the active circuitry. Dividing (3.24) by (2.7) gives:

$$\frac{\text{gain}_{act}}{\text{gain}_{pass}} \approx A + 1 \quad (3.25)$$

Thus, for the same C_b , this active filter circuit has $A + 1$ times *more* gain than the fourth-order passive filter.

3.1.3 Alternate Inductor-Enhancing Sense Circuit

There is a similar transformation for the sense leads of the amplifier. Shown in Fig. 3.10, this new topology is obtained by sliding the left input lead of the amplifier in Fig. 3.1 through the incrementally shorted V_{ext} .

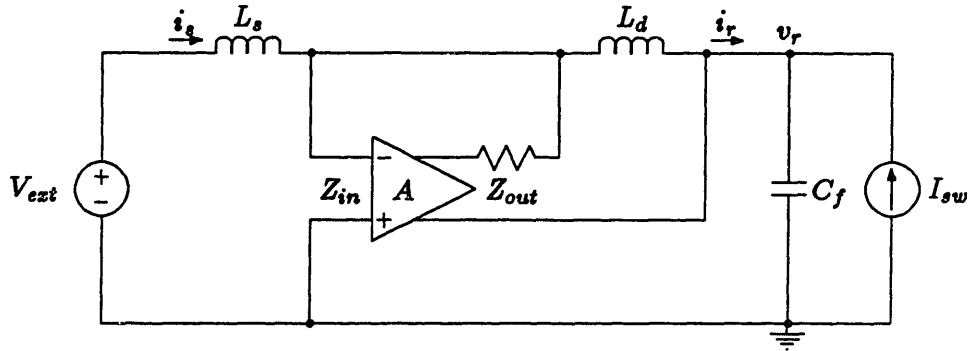


Figure 3.10: Alternate Sense for Inductor-Enhanced Circuit

This simple transformation results in a couple of important differences to the circuit's operation. First, note that the amplifier input-current no longer flows through V_{ext} . Under most circumstances, this should be beneficial for it should serve to reduce i_s .

The most important difference, though, is what might happen if V_{ext} were *not* an incremental short. Ordinarily, this would be considered good, for the ripple current

drop across that non-short would add to the drop across L_s and yield a larger sense voltage. If, however, V_{ext} looked capacitive, there exists a series LC circuit on the left-hand side of the filter. If that C happens to resonate with L_s *anywhere* near the switching frequency, i_s could be huge with no detectable voltage at the input-terminals of the amplifier. For this reason, this alternate sense topology is considered too prone to failure to use.

3.2 Capacitor-Enhanced Voltage-Filters

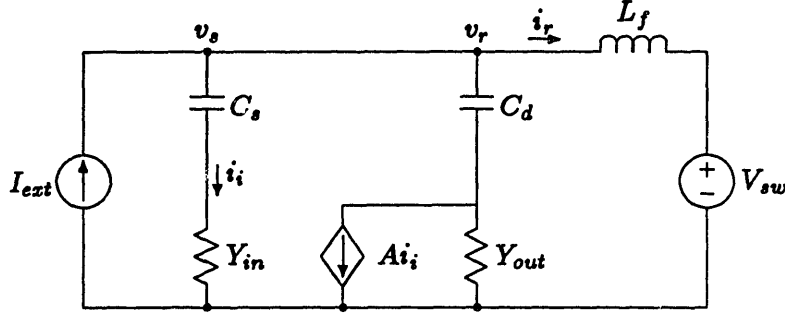


Figure 3.11: Capacitor-Enhancing Circuit with Standard Drive

As could be expected, the analysis of the capacitor-enhanced voltage-filter circuits is very much the dual of the analysis for the inductor-enhanced circuits. Capacitor-enhanced circuits are constructed from the 2nd order voltage-filter of Fig. 2.1. L_f is left unchanged, while C_f is split into C_s and C_d . Active circuitry is then added to make C_s and C_d appear larger.

3.2.1 Capacitor-Enhancing with Standard Drive Method

One possible arrangement is shown in Fig. 3.11. (Note that the amplifier is a current-in/current-out amp). The amplifier input-current, i_i is due to the ripple-voltage at the external-source, v_s . This current is amplified by a factor of A and drawn from the external-source terminals so as to drive v_s to zero. Again, if A were infinite, v_s would equal zero, as desired.

Gain Derivation

The effective-admittance, Y_{eff} , is defined as the inductor ripple current i_r over the external-source ripple voltage v_s . Since $v_r = v_s$ in this case, it is also the Norton-admittance. The exact solution for Y_{eff} is:

$$Y_{eff} = \frac{i_r}{v_s} = \frac{(sC_s + Y_{in})sC_d Y_{out} + sC_s Y_{in} Y_{out} + (A + 1)sC_s sC_d Y_{in}}{(sC_s + Y_{in})(sC_d + Y_{out})} \quad (3.26)$$

which is *exactly* the dual of (3.1).

Defining

$$\begin{aligned} C_p &\doteq \frac{C_s C_d}{C_s + C_d} & \omega_s &\doteq Y_{in}/C_s \\ \text{gain} &\doteq \frac{Y_{eff}}{s(C_s + C_d)} & \omega_d &\doteq Y_{out}/C_d \\ & & \omega_z &\doteq Y_{out}/(A + 1)C_p \end{aligned} \quad (3.27)$$

and performing an analysis very dual to that in the inductor-enhancing discussion yields:

$$\text{gain} \approx \frac{Y_{in}[sC_p(A+1) + Y_{out}]}{(sC_s + Y_{in})(sC_s + Y_{out})} = (A+1) \left(\frac{Y_{in}}{C_s + C_d} \right) \frac{s + \omega_z}{(s + \omega_s)(s + \omega_d)} \quad (3.28)$$

The bode plot of this expression looks exactly like Fig 3.2. The two possible values for G_{max} are:

$$\begin{aligned} \omega_s < \omega_d \quad \text{gain} &\approx (A+1) \frac{C_d}{C_s + C_d} \left(\frac{Y_{in}}{Y_{out}} \right) \\ \omega_s > \omega_d \quad \text{gain} &\approx (A+1) \frac{C_s}{C_s + C_d} \end{aligned} \quad (3.29)$$

Again, the maximum gain is obtained by working in the $\omega_s > \omega_d$ region.

An important special case of this equation is the result obtained by assuming that the current source in the amplifier is 'good'. Under this assumption $Y_{out} \approx 0$ and the gain relation, (3.28), further simplifies to:

$$\text{gain} \approx \left(\frac{C_s}{C_s + C_d} \right) \frac{(A+1)Y_{in}}{sC_s + Y_{in}} \quad (3.30)$$

Maximum Effective Capacitance

An argument exactly the dual of that used in section 3.1.1 holds here regarding the maximum effective capacitance that this circuit can create at a given working frequency. The maximum effective capacitance is found by substituting $C_{eff} = \text{gain} \times (C_s + C_d)$ into the gain relation and evaluating above both poles:

$$C_{eff_{max}} = (A+1) \frac{Y_{in}}{\omega_{wf}} \quad (3.31)$$

LT Analysis

The LT of this circuit is found by incrementally opening both the input and output ports. The LT circuit looks like Fig. 3.12.

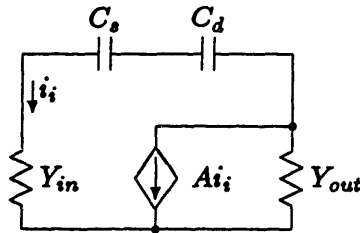


Figure 3.12: LT Circuit

After a bit of derivation, the exact dual to (3.10) appears:

$$LT = A \left(\frac{Y_{in}}{Y_{in} + Y_{out}} \right) \frac{sC_p}{sC_p + Y_p} \quad (3.32)$$

where

$$Y_p \doteq \frac{Y_{in}Y_{out}}{Y_{in} + Y_{out}}.$$

Gain/LT Calculation

Since the gain and the LT relations exactly dual those from the inductor-enhancing analysis, the gain/LT does so, as well. These equations, therefore, are presented only as a quick reference. Again, assuming that we are well above the zero in the gain expression,

$$\frac{\text{gain}}{LT} = \frac{(sC_p + Y_p)(Y_{in} + Y_{out})}{(sC_s + Y_{in})(sC_d + Y_{out})} \quad (3.33)$$

The Bode-plot of this looks exactly like Fig. 3.5. As before, the best performance is obtained by placing all the poles and zeroes of the gain/LT expression slightly above the working frequency, and again the gain/LT has a maximum value of 1.

3.2.2 Alternate Capacitor-Enhancing Drive Circuit

Also by duality, there exists an alternate drive topology for the capacitor-enhancing circuits which overcomes the above gain/LT limitation. It is shown in Fig. 3.13.

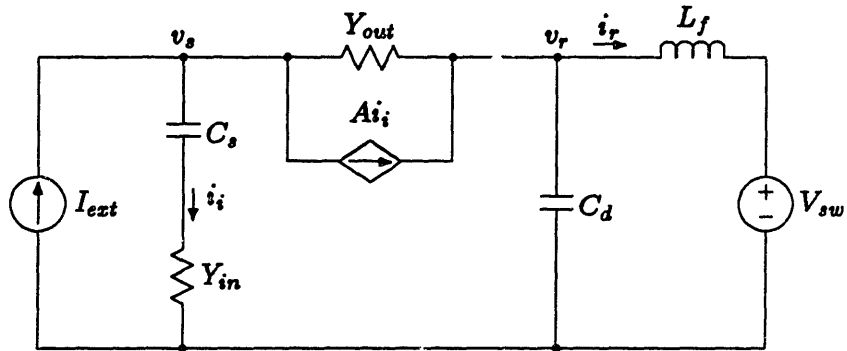


Figure 3.13: Alternate Drive for Capacitor Enhanced Filters

The relations for this circuit exactly dual those from the inductor-enhancing alter-

nate drive. They are:

$$\begin{aligned}
Y_{eff} &= \frac{i_r}{v_s} \approx s(C_s + C_d) \frac{sC_p[(A+1)Y_{out} + Y_{in}] + Y_{out}Y_{in}}{Y_{out}(sC_s + Y_{in})} \\
\text{gain} &= \frac{Y_{eff}}{s(C_s + C_d)} \approx \frac{Y_{in}}{Y_{out}} \frac{sC_p(A+1) + Y_{out}}{sC_s + Y_{in}} \\
\text{gain}_{max} &\approx (A+1) \frac{C_d}{C_s + C_d} \frac{Y_{in}}{Y_{out}} \\
\text{LT} &= A \left(\frac{Y_{in}}{Y_{in} + Y_{out}} \right) \frac{sC_p}{sC_p + Y_p} \\
\frac{\text{gain}}{\text{LT}} &= \left(\frac{Y_{in} + Y_{out}}{Y_{out}} \right) \left(\frac{C_d}{C_s + C_d} \right) \frac{(s + \omega_s)(s + \omega_p)}{s(s + \omega_s)}.
\end{aligned} \tag{3.34}$$

The Bode-plot for the gain/LT looks exactly like Fig 3.8. Again, it appears that this topology is superior to the standard topology because its gain/LT can easily be greater than 1.

Consideration of Y_{out}

If the exact dual of the alternate-drive inductor-enhancing circuit is used, as shown in Fig. 3.13, Y_{out} will have to carry the full DC bus current. To avoid excessive power dissipation, therefore, Y_{out} must be made to be at least partly inductive. Again, this inductor is considered expensive and should be made as small as possible. If this inductor is sufficiently small, then Y_{out} will look inductive at the working frequency and this will affect the gain derivation. Assuming, then, that $Y_{out} = 1/sL_b$ the gain relation in (3.34) becomes:

$$\text{gain} = \frac{s^2 L_b C_p (A+1) Y_{in} + s C_p + Y_{in}}{s C_s + Y_{in}} \tag{3.35}$$

In this situation, the gain has no theoretical maximum and the DC power dissipation in Y_{out} is zero. Because A is large, the zeroes are again 'lightly damped' as in section 3.1.1.

Comparison to Fourth-Order Passive Filters Above the zeroes, but below the pole in the gain, a clean active to passive gain comparison can be made. The gain in this region simplifies to:

$$\text{gain} = s^2 L_b C_p (A+1) \tag{3.36}$$

so that, just as with the inductor-enhanced alternate drive

$$\frac{\text{gain}_{act}}{\text{gain}_{pass}} \approx (A+1) \tag{3.37}$$

Thus, for the same inductor L_b , this circuit provides A times *more* gain than does the fourth-order passive circuit.

LT with Inductive Y_{out} It is also valuable to consider the LT when Y_{out} looks inductive. Substituting $Y_{out} = 1/sL_b$, the LT expression becomes:

$$LT = \frac{AY_{in} s^2 L_b C_p}{(sL_b Y_{in} + 1)(sC_p + Y_p)} \quad (3.38)$$

above the zeroes in the gain, the numerators in the gain and the LT are identical. The gain/LT ratio above the gain zeroes is therefore:

$$\frac{\text{gain}}{LT} \approx \frac{(sL_b Y_{in} + 1)(sC_p + Y_p)}{sC_s + Y_{in}} \quad (3.39)$$

Notice that this ratio increases with a slope of 1 above all of the poles and zeroes. Thus, this circuit can achieve high gain/LT when operated well above all the poles of the LT. In this region, the gain is still increasing with a slope of 1 and the LT is level. An additional compensation pole in A , just below the operating frequency, will serve to level off the gain to a constant value (if that is desired) and start the LT roll-off.

3.3 Effects of External-Source Impedance

In the calculation of the LT for all these circuits, the 'external-source' was always assumed to be either an incremental short for inductor-enhancing, or an incremental open for capacitor-enhancing circuits. Unfortunately, in arbitrary installations this may not be a perfect assumption so there is some concern as to the effects of these imperfections.

If these imperfections are small, they should not substantially affect the gain of any circuit, but they may be responsible for introducing a high frequency pole to the LT. If not accounted for, this extra pole in the LT could cause the circuit to be unstable.

Effects on the Loop Transmission

Recall that for both inductor and capacitor enhancing circuits, the standard drive and alternate drive topologies had the same loop transmission. Modifying the incremental impedance of the external-source will not change the fact that the loop transmissions for the different drive topologies are the same.

Assuming that V_{ext} of the current-filter looks like an inductor L_x , instead of being an incremental short as before, the loop-transmission of the inductor-enhanced circuit is:

$$LT^* = \frac{AZ_{in} s L_s L_d}{s^2 L_s L_d L_x + s[Z_{out} L_s (L_d + L_x) + Z_{in} L_d (L_s + L_x)] + (L_s + L_x + L_d) Z_{out} Z_{in}} \quad (3.40)$$

Similarly, assuming that I_{ext} of the voltage-filter looks like a capacitor C_x instead of being incrementally open gives:

$$LT^* = \frac{AY_{in} s C_s C_d}{s^2 C_s C_d C_x + s[Y_{out} C_s (C_d + C_x) + Y_{in} C_d (C_s + C_x)] + (C_s + C_x + C_d) Y_{out} Y_{in}} \quad (3.41)$$

for the loop-transmission of the capacitor enhanced circuit.

There are several points to notice here:

1. These two are exact duals of each other, as would be expected.
2. They each agree with (3.10),(3.32) in the limit $L_x, C_x \rightarrow 0$.
3. The extra element has *introduced* an additional pole to each LT relation.

It is this last property which is potentially *very* harmful. Recall that $A(s)$ contains an appropriate LT roll-off pole. Thus, if this new pole occurs below the UGC, the circuit will become unstable.

To investigate this new pole further, first assume that the extra element is a circuit parasitic. As such it will be much less than other comparable circuit elements. In this case, the two LT poles lie on the negative real axis:

$$\begin{aligned} L_x \ll L_s, L_d & \quad \omega_{p1} = \frac{Z_p}{L_p} & \quad \omega_{p2} = \frac{Z_{in} + Z_{out}}{L_x} \\ C_x \ll C_s, C_d & \quad \omega_{p1} = \frac{Y_p}{C_p} & \quad \omega_{p2} = \frac{Y_{in} + Y_{out}}{C_x} \end{aligned} \quad (3.42)$$

In both relations ω_{p1} is the old LT pole at ω_p , and the ω_{p2} is the pole introduced by the new element. Notice that ω_{p2} is a factor *like* L_p/L_x or C_p/C_x higher than ω_{p1} . Since $|LT|$ is generally quite large at ω_p it is still possible that ω_{p2} will occur below the UGC and hence cause the circuit to be unstable.

The only solution to this problem seems to be to add extra L_x or C_x to the circuit and try to move ω_{p2} down to be the dominant LT roll-off pole. This further requires removing the old LT roll-off pole from $A(s)$, or at least moving it to above the UGC.

In practice, this would require a fairly large L_x or C_x . As such, it would be significantly larger than other comparable circuit elements. With this in mind (3.40) and (3.41) simplify to:

$$\begin{aligned} L_x \gg L_s, L_d & \quad LT^* = \frac{AZ_{in}sL_sL_d}{L_x[s^2L_sL_d + s(L_sZ_{out} + L_dZ_{in}) + Z_{out}Z_{in}] \\ C_x \gg C_s, C_d & \quad LT^* = \frac{AY_{in}sC_sC_d}{C_x[s^2C_sC_d + s(C_sY_{out} + C_dY_{in}) + Y_{out}Y_{in}]} \end{aligned} \quad (3.43)$$

The denominators of these can be easily factored to yield:

$$\begin{aligned} L_x \gg L_s, L_d & \quad LT^* = \frac{sAZ_{in}}{L_x(s + \omega_s)(s + \omega_d)} \\ C_x \gg C_s, C_d & \quad LT^* = \frac{sAY_{in}}{C_x(s + \omega_s)(s + \omega_d)} \end{aligned} \quad (3.44)$$

Thus, making L_x or C_x large has moved the two poles of the LT, ω_{p1} and ω_{p2} , to the standard old ω_s and ω_d . It should be noted that for the first time, the LT explicitly *contains* its roll-off pole. A bode plot of this LT looks much like Fig. 3.2, rather than Fig. 3.5.

Effects on Gain

New values for the effective-inductance, L_{eff}^* , and effective-capacitance C_{eff}^* are:

$$\begin{aligned} L_{eff}^* &= L_x + L_{eff} = L_x + \text{gain}(L_s + L_d) \\ C_{eff}^* &= C_x + C_{eff} = C_x + \text{gain}(C_s + C_d) \end{aligned} \quad (3.45)$$

Thus, until L_x or C_x get to be on the order of L_{eff} or C_{eff} (hopefully very large), their addition will not appreciably effect L_{eff}^* or C_{eff}^* . On the other hand, L_x and C_x are 'costly' elements, so the gain should be re-defined:

$$\begin{aligned} \text{gain}^* &\doteq \frac{L_{eff}^*}{L_s + L_d + L_x} \approx \frac{L_{eff}}{L_x} \\ \text{gain}^* &\doteq \frac{C_{eff}^*}{C_s + C_d + C_x} \approx \frac{C_{eff}}{C_x} \end{aligned}$$

Re-deriving the four gain relations gives and assuming operation above ω_x gives:

	Standard Drive	Alternate Drive	
gain* \approx	$\frac{sZ_{in}A}{L_x(s + \omega_s)(s + \omega_d)}$	$\frac{sZ_{in}AL_d}{Z_{out}L_x(s + \omega_s)}$	(3.46)
gain* \approx	$\frac{sY_{in}A}{C_x(s + \omega_s)(s + \omega_d)}$	$\frac{sY_{in}AC_d}{Y_{out}C_x(s + \omega_s)}$	

Effects on Gain/LT Ratio

Dividing (3.46) by (3.44) gives the general figures-of-merit.

Standard Drive	$\frac{\text{gain}^*}{LT^*} = 1$	
Alternate Drive	$\frac{\text{gain}^*}{LT^*} = \frac{(s + \omega_d)}{\omega_d}$	(3.47)

The latter relation is flat at unity out to ω_d where it starts increasing with a slope of 1. Thus, even when adding large amounts of L_x or C_x , the alternate drive topology can provide gain/LT in excess of 1 for operating frequencies above ω_s and ω_d .

Conclusions

In those situations where the impedance of the external-source is unknown, or where it is known to be undesirably capacitive or inductive, the active filter circuits may have to be modified to keep them stable. Though this modification generally has detrimental effects on the gain, it does not make the filters useless. In fact, the alternate drive circuits can still achieve gain/LT ratios significantly greater than unity.

3.4 Summary

Before moving on, it is valuable to restate some of the key points in the development thus far.

1. There are two different drive topologies for both inductor-enhancing and capacitor-enhancing filter circuits for a total of four active filters under consideration.
2. Both topologies have the potential to provide reasonably high gain.
3. The alternate drive topology can achieve $\text{gain/LT} > 1$ in both inductor and capacitor-enhancing circuits.
4. There is no fundamental limit on L_{effmax} or C_{effmax} using the alternate drive topology.
5. External-Source impedance could make the filters unstable unless specifically accounted for.

Chapter 4

Practical Circuit Considerations

Thus far, the development of inductor-enhanced and capacitor-enhanced active filter circuits has been centered around generic amplifier modules characterized by their input/output relations. Voltage-in/voltage-out amplifiers were used for the inductor-enhanced filters while current-in/current-out amplifiers were used for the capacitor-enhanced filters. The development achieved large gains in both a 'standard' and an 'alternate' drive topology for each filter type. The only task remaining is to develop 'optimal' implementations of these amplifier modules.

To be considered a worthwhile endeavor, these active filter circuits ought to exhibit gains in excess of 100 at their 1 MHz nominal operating frequency. Since the gain of these circuits is generally close to the amplifier gain A , gain-bandwidths in the 100 MHz region are required. Also, though the amplifier in these circuits operates at a gain of A , the outer feedback loop in all the circuits imposes unity-gain-feedback stability constraints on the amplifier.

This gain-bandwidth specification far exceeds what is available with generic op-amps. Special high-speed high-gain op-amps may be able to provide the desired gain-bandwidth, but they cannot be compensated for unity-gain-feedback. Thus commercially available op-amps are not suitable for this application.

Instead, special purpose amplifiers will have to be constructed from discrete elements such as bipolar transistors and FET's.

4.1 Three Terminal Active Device Model

A characteristic of the available discrete elements is that they all have three terminals. As such, relations developed on the basis of a *general* three-terminal device model can be easily adapted to the characteristics of a particular device by choosing appropriate values for the model parameters.

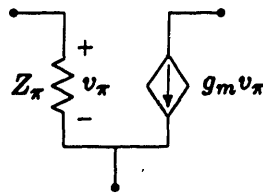


Figure 4.1: General Three-Terminal Model

A simple but adequate three-terminal model is shown in Fig. 4.1. It is a simplified version of the well known hybrid- π model. Because this model does not completely represent the terminal characteristics of the real devices, it will be used only for making rough comparisons between different amplifier and active filter topologies.

4.2 Single Active-Device Filter Circuits

Active filters can be made using a single active device as the amplifier. Though their gain is limited by their utter simplicity, they can still be of use in some applications. There are six ways to connect an active device as the amplifier in each of the four filter circuits under consideration. Fortunately, one connection in each provides higher gain than all the others and is therefore clearly superior. The 'good connection' for each of the four active filters is shown incrementally in Fig. 4.2.

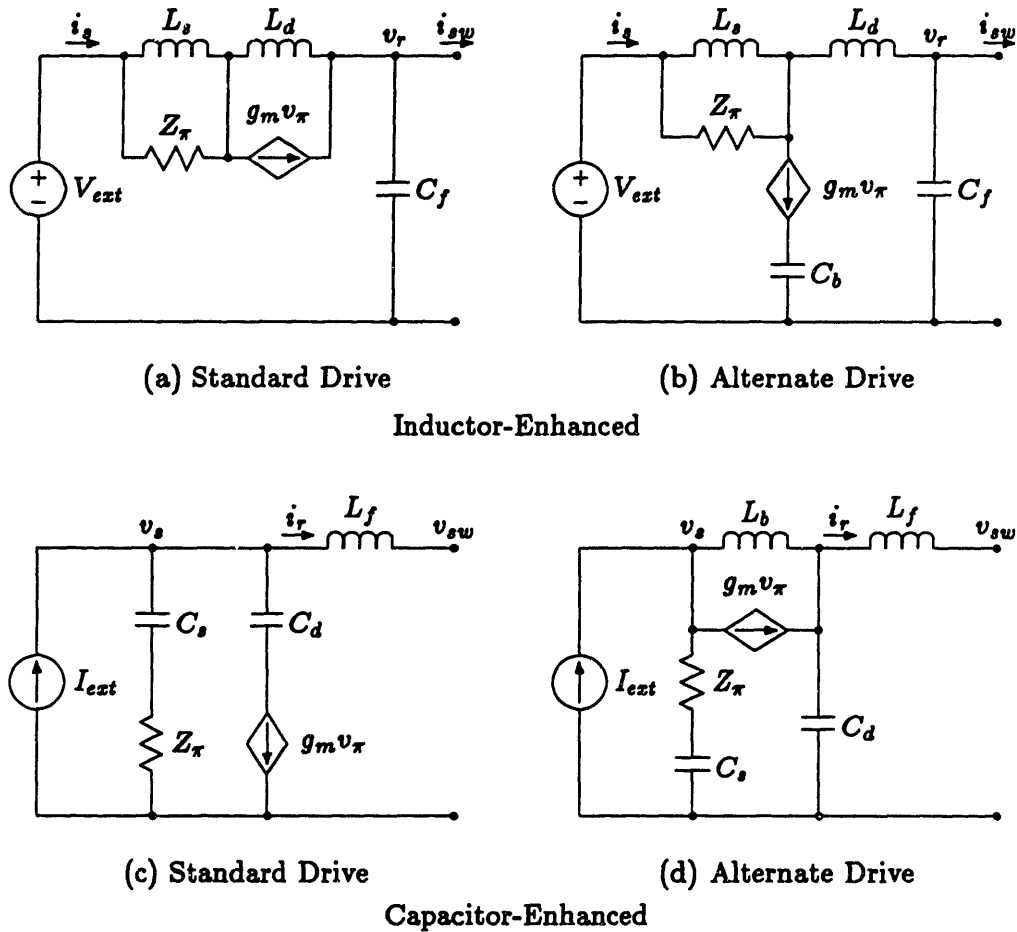


Figure 4.2: Four Simplest Active Filters

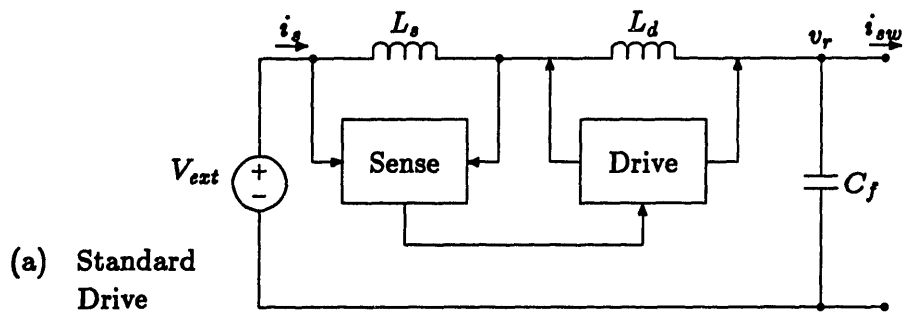
The gain for each is:

$$\begin{array}{ll}
 \text{gain} = & \text{gain}_{max} = \\
 \text{(a)} \quad \frac{sL_p(g_m Z_\pi + 1) + Z_\pi}{sL_s + Z_\pi} & \frac{L_d}{L_s + L_d}(g_m Z_\pi + 1) \\
 \text{(b)} \quad \frac{sL_p(g_m Z_\pi + 1) + Z_\pi}{sL_s + Z_\pi} & \frac{L_d}{L_s + L_d}(g_m Z_\pi + 1) \\
 \text{(c)} \quad \frac{C_s}{C_s + C_d} \frac{g_m Z_\pi + 1}{sC_s Z_\pi + 1} & \frac{C_s}{C_s + C_d}(g_m Z_\pi + 1) \\
 \text{(d)} \quad \frac{s^2 C_p L_b (g_m Z_\pi + 1) + s C_p Z_\pi + 1}{s C_s Z_\pi + 1} & \frac{C_d}{C_s + C_d}(g_m Z_\pi + 1) \frac{s L_b}{Z_\pi}
 \end{array} \tag{4.1}$$

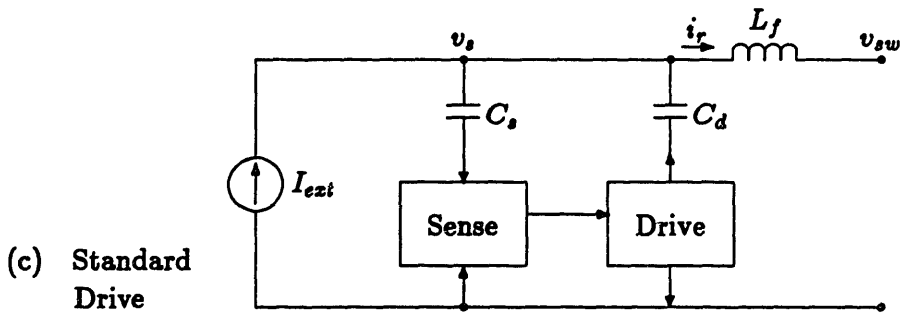
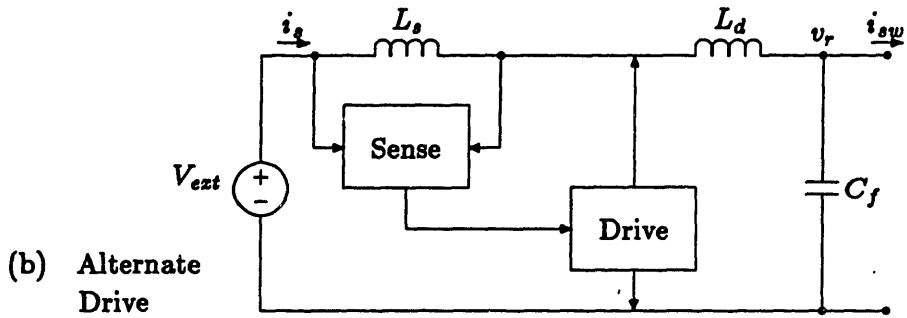
There are several things to notice here:

1. The relations for inductor-enhanced and capacitor-enhanced circuits are no longer duals of each other. This is due to the non-duality of the active device used to create both types.
2. The gain expressions for the capacitor-enhanced circuits look very much like those from Chapter 3 with $Y_{out} = 0$.
3. The gain expressions for the inductor-enhanced circuits can be made to look like those of Chapter 3 by letting $Z_{out} \rightarrow \infty$, $A \rightarrow \infty$, and $Z_{out}/A \rightarrow G$.
4. The equations for the two inductor-enhanced circuits are the same.
5. The gain_{max} column assumes that g_m and Z_π look resistive.
6. The gain_{max} column is applicable only in certain regions of operation for each circuit.

For bipolar transistors, for example, $g_m Z_\pi \doteq \beta_f \approx 100$. Thus, active filters with gains in the 100 region should be achievable with a single bipolar transistor and associated support components. High-frequency compensation of these simple filters should also be very easy for the number of parasitic poles is kept to an absolute minimum. In practice, the required support and bias circuitry would tend to reduce the gain by a small amount, but for many applications these filters may be quite valuable due to their utter simplicity. In other applications, even more gain is desirable so the analysis continues with multiple active-device filters.



Inductor
Enhanced



Capacitor
Enhanced

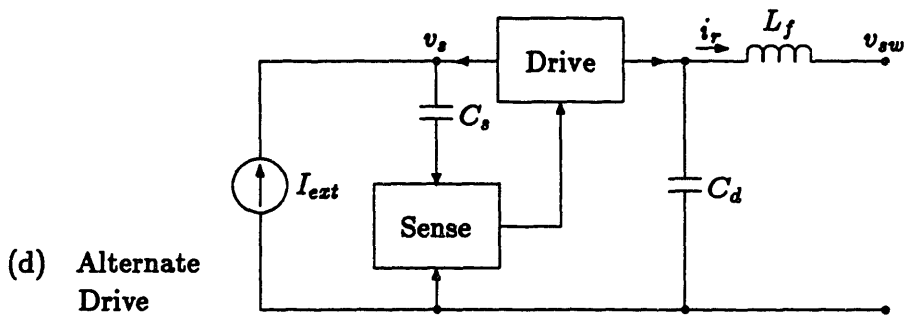


Figure 4.3: Block Diagrams of Four Active Filters

4.3 Multiple Active-Device Filter Circuits

In general, an increase in the number of active devices would lead to an increase in the maximum achievable gain. Unfortunately, each additional active device will also add a parasitic pole or two to the LT. All these parasitic poles must still be kept above the UGC. As a result the limit on the maximum achievable gain very soon comes not from how many active devices are used, but from how many poles can be pushed significantly above a usefully high UGC. It is felt that two active devices provides the best tradeoff between number of poles and high gain. Henceforth the development of the active filters will concern itself with two-device circuits.

4.3.1 Separation into Sense and Drive

To facilitate further development, each filter circuit will be divided into two sections; 'sense' and 'drive'. Block diagrams of the four active filters developed in Chapter 3 separated into their sense and drive sections are shown in Fig. 4.3. Since each filter will be composed of two active devices, each section will contain a single active device and associated passive components.

4.3.2 Inductor-Enhancing Filter Circuits

Sense Circuits

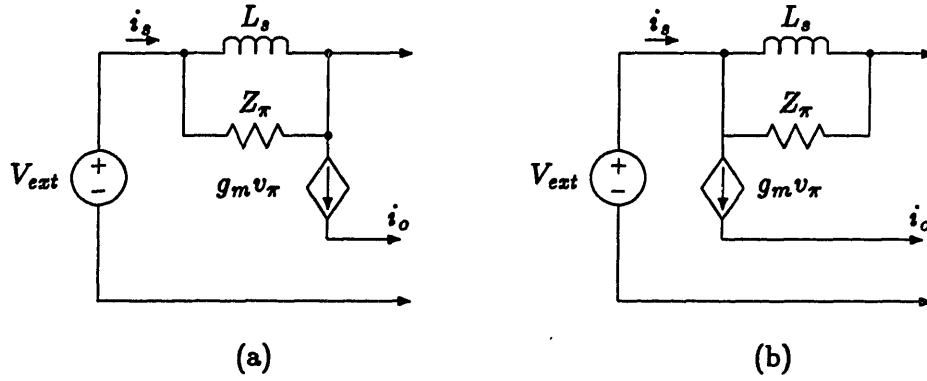


Figure 4.4: Two Good Sense Connections

There are a total of six ways to connect the three terminal element across a sense-inductor. Fortunately, only the two shown in Fig. 4.4 are of any value. The output of each of these is a current. Quantitatively:

$$\begin{aligned}
 \text{(a)} \quad \frac{i_o}{i_s} &= -g_m Z_\pi \left(\frac{sL_s}{sL_s + Z_\pi} \right) \\
 \text{(b)} \quad \frac{i_o}{i_s} &= g_m Z_\pi \left(\frac{sL_s}{sL_s g_m Z_\pi + Z_\pi} \right)
 \end{aligned} \tag{4.2}$$

Notice that the signs of these two transfer relations differ. This will become very important when selecting appropriate drive circuits.

A closer examination of (4.4) shows that while in (a), i_o/i_s becomes as high as $g_m Z_\pi$, in (b), i_o/i_s is always ≤ 1 . Thus it seems that (a) is immediately superior to (b). Approach (b) should not be discarded yet though, for in both of these i_o does not depend upon the load impedance that the sense circuit sees. If working into a high load impedance, (b) might actually 'perform better' than (a) due to miller characteristics. Also the LT characteristics, or sign of i_o/i_s , of (b) might make it very desirable.

Drive Circuits

As before there are six different connections for an active device in each of the standard and alternate drive topologies. Again, only two in each of the drive topologies are of any value. The four viable drive circuits are shown in Fig. 4.5.

It would be hard to define a *meaningful* transfer relation with which to compare these various drives as pictured. For an intuitive feel, however, if C_f to the right of the drive is considered an incremental-short and the sense circuitry to the left an incremental open, then the inductor-current, i_{L_d} , can be derived:

$$\begin{aligned} \text{(d),(e)} \quad \frac{i_{L_d}}{i_i} &= (g_m Z_\pi + 1) \\ \text{(c),(f)} \quad \frac{i_{L_d}}{i_i} &= -g_m Z_\pi \end{aligned} \tag{4.3}$$

The most important thing to notice is that, just as with the sense circuits, the signs of these relations differ.

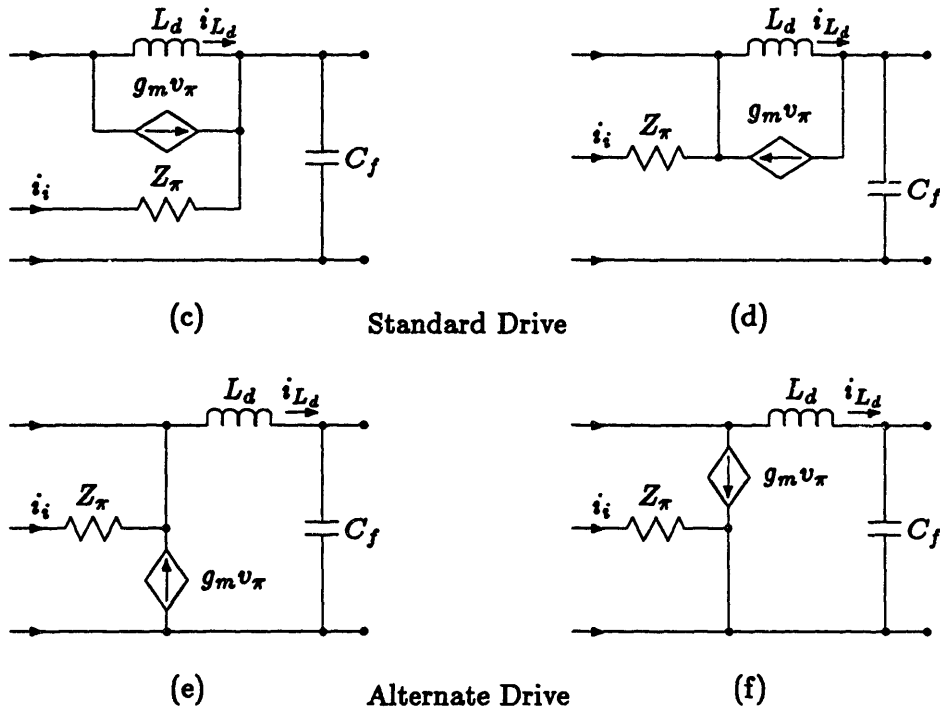


Figure 4.5: Four Drive Arrangements

Total Inductor-Enhancing Filter Circuits

Great care must be taken to observe the signs of the transfer relations when connecting various sense and drive circuits. To result in a stable circuit, (have negative feedback) the product of the signs of the sense and drive should be positive. Thus, though there are four viable drive circuits and two viable sense circuits, there are only four viable connections of the two types instead of eight. The other four possible connections are fundamentally unstable. With the 'standard drive' topology the good connections could be known as (ac) and (bd), and with the 'alternate drive' topology, the viable connections are (af) and (be). The four viable inductor-enhancing circuits, without C_f , are shown in Fig. 4.6.

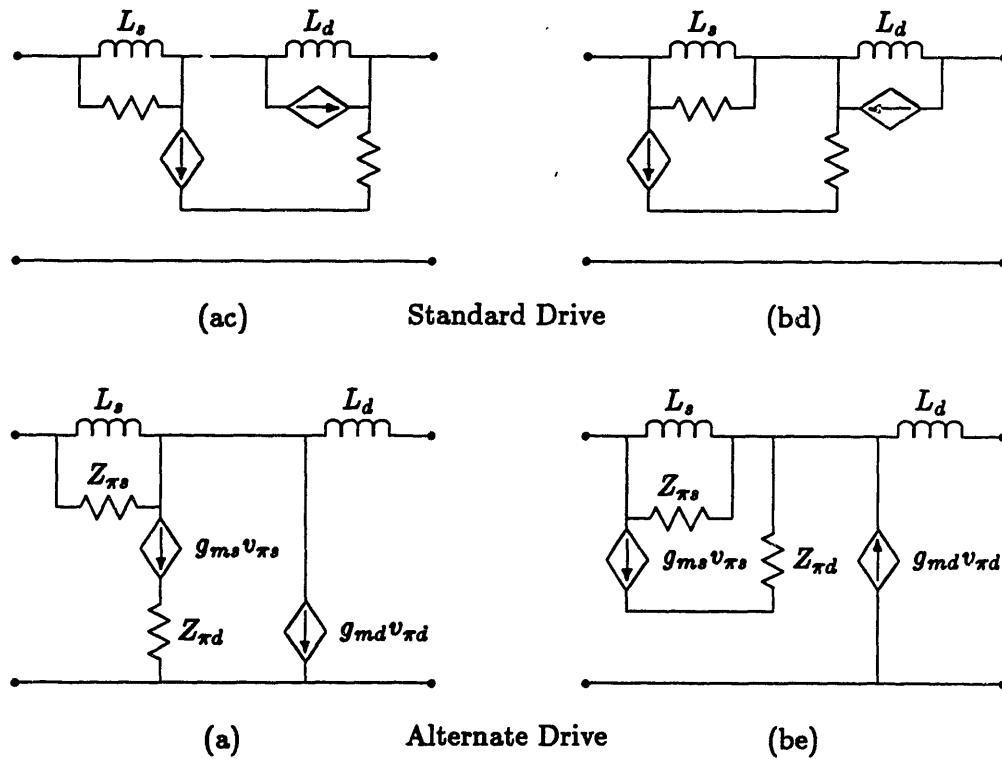


Figure 4.6: Four Inductor-Enhancing Circuits

Gain Calculation: It turns out that the gain equations for (af) and (ac), are identical. Likewise the relations for (be) and (bd) are also identical:

$$\begin{aligned}
 \text{(af),(ac)} \quad \text{gain} &= \frac{s L_p [(Z_{\pi d} g_{m d} + 1) g_{m s} Z_{\pi s} + 1] + Z_{\pi s}}{(s L_s + Z_{\pi s})} \\
 \text{(be),(bd)} \quad \text{gain} &= \frac{s L_p [(Z_{\pi d} g_{m d} + 1) g_{m s} Z_{\pi s} + 1] + Z_{\pi s}}{[s L_s (g_{m s} Z_{\pi s} + 1) + Z_{\pi s}]}
 \end{aligned} \tag{4.4}$$

Which are still *exact*. Defining the unitless quantity $\beta = g_m Z_{\pi}$, and making some very valid simplifications gives:

$$\begin{aligned}
 \text{(af),(ac)} \quad \text{gain} &\approx \frac{s L_p \beta_s \beta_d + Z_{\pi s}}{(s L_s + Z_{\pi s})} \\
 \text{(be),(bd)} \quad \text{gain} &\approx \frac{s L_p \beta_s \beta_d + Z_{\pi s}}{(s L_s \beta_s + Z_{\pi s})}
 \end{aligned} \tag{4.5}$$

The only difference between these two is that (be) and (bd) roll off β_s sooner than do (af) and (ac). A Bode-plot of these two looks like Fig. 4.7. Notice that in circuits (ac) and (af) the gain can be on the order of $\beta_s \beta_d$. For bipolar transistors, this could easily be greater than 1000.

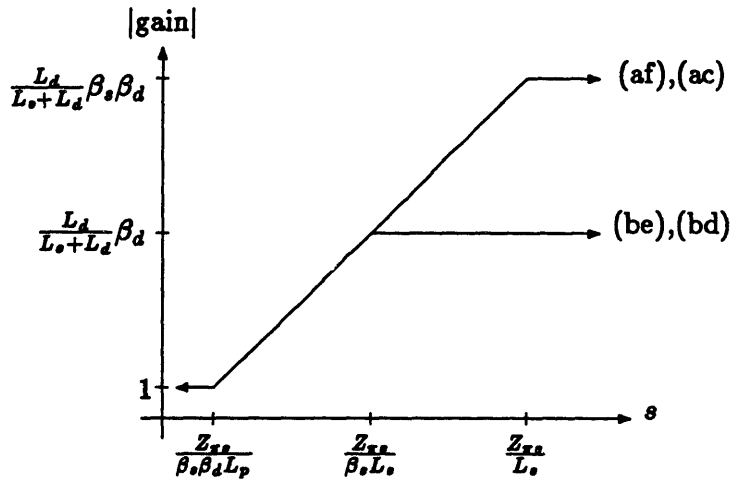


Figure 4.7: Bode-Plot of Gain for Four Inductor-Enhancing Circuits

Also notice the lack of anything which looks like ω_d in these gain expressions. This is due to the drive element being modeled as a perfect current-source. As Z_{out} from the previous chapter went to infinity, so did ω_d .

Since there is no ω_d associated with these circuits, raising L_d arbitrarily, will never cause the gain to roll-off for a given $\omega_{w f}$ as it did previously. Recalling that $L_{eff} = \text{gain}(L_s + L_d)$, this corresponds to there being no fundamental limit on L_{eff} .

LT Calculation: The loop-transmission is found by incrementally shorting both the input and output 'ports'. Under this condition, the standard and alternate drive circuits are identical, as they were for the LT derivation in Chapter 3. With this in mind, there are only two different circuits for which to derive the LT, as shown in Fig. 4.8.

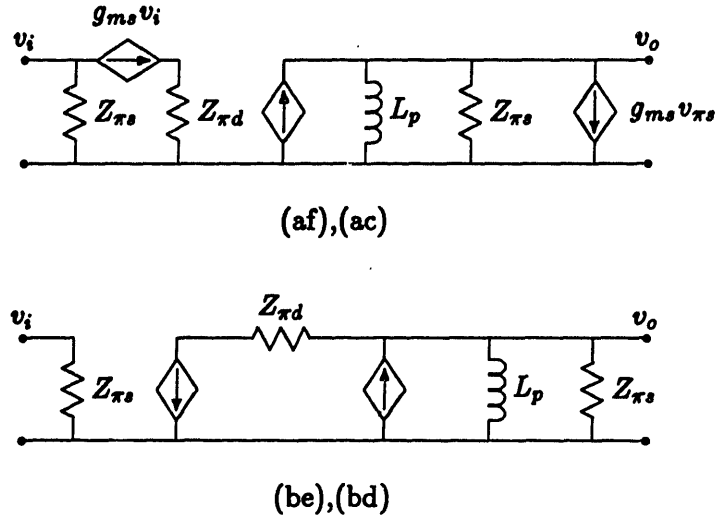


Figure 4.8: Two Different LT Circuits

Deriving the LT relation for each yields:

$$\begin{aligned}
 \text{(af),(ac)} \quad \text{LT} &= -\frac{v_o}{v_i} = \frac{s L_p \beta_s \beta_d}{s L_p (\beta_s + 1) + Z_{\pi s}} \\
 \text{(be),(bd)} \quad \text{LT} &= -\frac{v_o}{v_i} = \frac{s L_p \beta_s (\beta_d + 1)}{s L_p + Z_{\pi s}}
 \end{aligned} \tag{4.6}$$

Notice that the LT for (af) and (ac) levels off β_s sooner and to a level β_s lower than it does for (be) and (bd). Recalling that it is desirable to have large gain with small LT, it does indeed appear that (af) or (ac) will be the circuits to use. It is important to keep in mind that a pole is going to have to be added to these circuits to accomplish the necessary LT roll-off.

Gain/LT Calculation: The general figure-of-merit is, as usual, the gain/LT ratio. Performing the respective divisions and simplifying yields:

$$\begin{aligned}
 \text{(af),(ac)} \quad \frac{\text{gain}}{\text{LT}} &= \frac{(s L_p \beta_s \beta_d + Z_{\pi s})(s L_p \beta_s + Z_{\pi s})}{s L_p \beta_s \beta_d (s L_s + Z_{\pi s})} \\
 \text{(be),(bd)} \quad \frac{\text{gain}}{\text{LT}} &= \frac{(s L_p \beta_s \beta_d + Z_{\pi s})(s L_p + Z_{\pi s})}{s L_p \beta_s \beta_d (s L_s \beta_s + Z_{\pi s})}
 \end{aligned} \tag{4.7}$$

A Bode-plot of the equations in (4.7) is shown in Fig. 4.9.

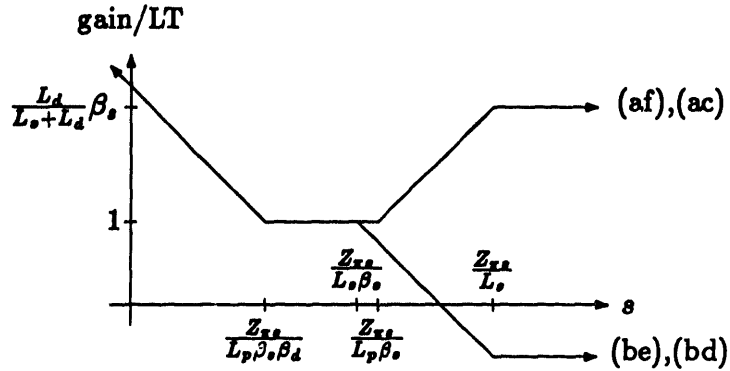


Figure 4.9: Bode-plot of gain/LT for Four Inductor Enhancing Circuits

Notice how similar this looks to Fig. 3.8. In fact, identifying the parameters:

$$\beta_d = A \quad Z_{\pi s} = Z_{in}' \quad \frac{Z_{\pi s}}{\beta_s} = Z_{out} \quad (4.8)$$

makes all the previous relations in this section look exactly like their counterparts from Chapter 3.

Summary of Inductor-Enhancing Circuits

Operation of these different circuits seems divided entirely by the type of sense they employ and not at all by the type of drive. Summarizing the results:

1. Circuits with type (a) sense can achieve gains of $\sim \beta^2$.
2. Circuits with type (b) sense achieve gains of only $\sim \beta$.
3. Loop-transmission for (a) sense is lower by a factor of β than that of (b) sense.

From this early analysis, circuits with type (a) sense appear to be clearly superior to those with type (b) sense.

4.3.3 Capacitor-Enhancing Filter Circuits

The development here is very much the dual of that in the previous section. As such, several of the intermediate steps will be omitted.

Sense Circuits

As before, there are six possible sense circuits of which only two are of any value. The two good ones look like Fig. 4.10. Again, their respective signs differ.

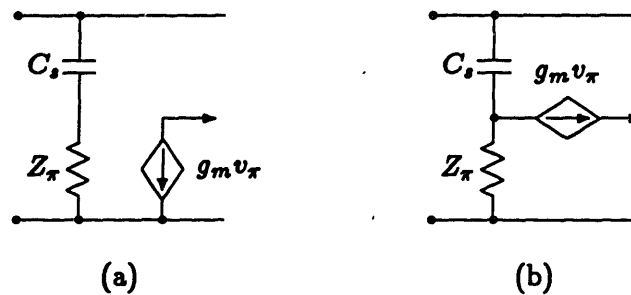
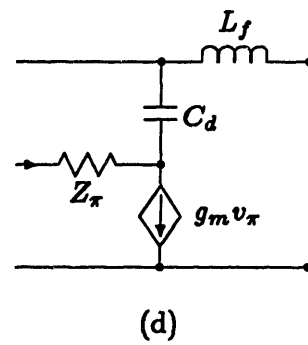
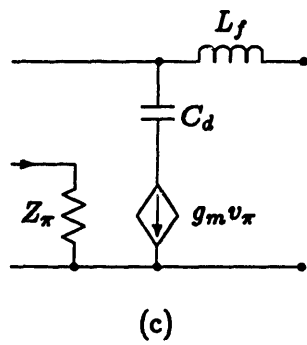


Figure 4.10: Two Good Sense Circuits

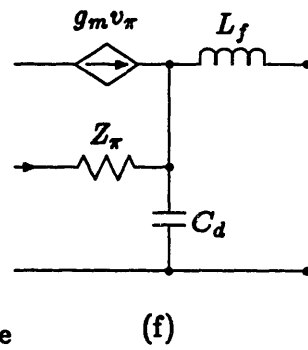
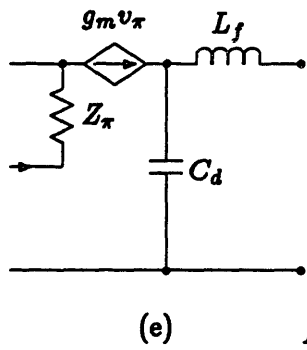
Drive Circuits

Here there is, just as before, a standard topology and an alternate topology. There are two good connections from each topology for a total of four drive circuits. The four are illustrated in Fig. 4.11

It suffices to say, without derivation, that the 'signs' of these four drives differ. (c) and (e) are of one sign while (d) and (f) are of the other. A very important subtlety, though, is that if one of these drives is flipped top for bottom, its sign changes. Thus there are flipped versions of these four drives, where (d) and (f) are of one sign while (c) and (e) are of the other, for a grand total of *eight* viable drive circuits.

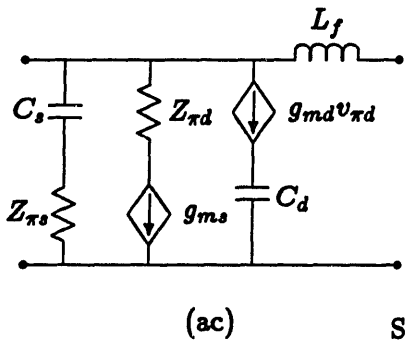
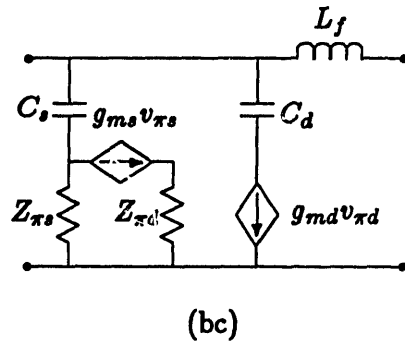
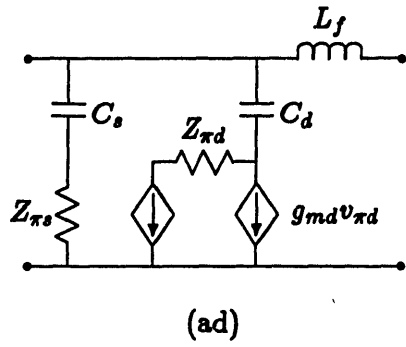


Standard Drive

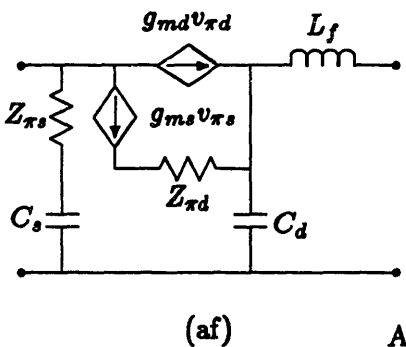
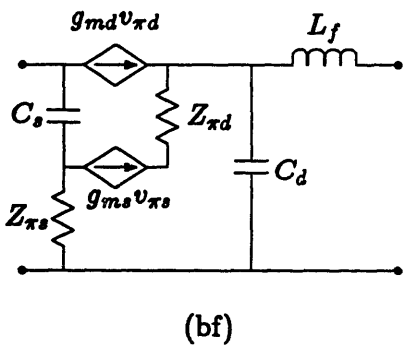
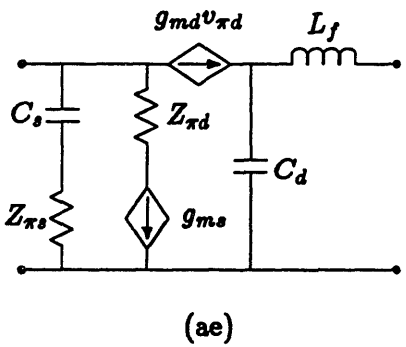
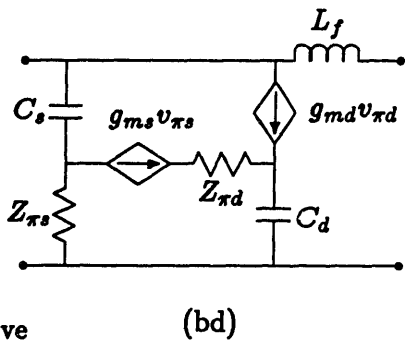


Alternate Drive

Figure 4.11: Four Drive Circuits



Standard Drive



Alternate Drive

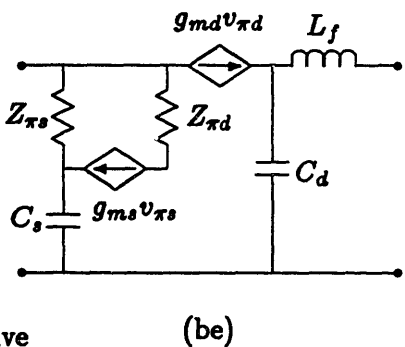


Figure 4.12: Eight Capacitor-Enhancing Circuits

Total Capacitor-Enhancing Filters

With eight viable drives, four of each sign, and two viable sense circuits, one of each sign, there are eight viable capacitor enhancing circuits to be evaluated. They are shown in Fig. 4.12.

It is also important to point out that there are truly eight inductor-enhancing circuits as well. The other four are again formed by flipping a drive circuit top for bottom, and connecting to the other polarity sense circuit. This means, though, that there is an inductor in series with both the 'high-voltage' bus line *and* the 'ground' line. Although this may be acceptable in some situations, the majority of power systems must keep at least one 'ground reference' continuous and so cannot utilize the flipped drives. Thus, the other four inductor-enhancing circuits were not developed.

There is a dual problem, by the way, with these eight capacitor enhancing circuits. In four of the above circuits, (ad), (bc), (af), and (be), both active devices are connected to the same bus line. All connections to the other bus line are via capacitors C_s and C_d , which serve to isolate the active circuitry from the high DC bus voltage. In the other four circuits, (ac), (bd), (ae), and (bf), however, each active device is connected directly to a different bus line. With these circuits, a means, other than C_s and C_d , will have to be supplied to isolate the active circuitry from the high voltage DC bus. Though this is no problem in principle, this isolation might cost an additional capacitor which would have to be included in the gain calculation.

LT Calculation: The LT calculation for these eight is very straightforward. It turns out that all the circuits with type (a) sense have the same LT, as do those with type (b) sense.

$$\begin{aligned}
 \text{(ac),(ad),(ae),(af)} \quad LT &= \beta_s(\beta_d + 1) \approx \beta_s\beta_d \\
 \text{(bc),(bd),(be),(bf)} \quad LT &= \frac{\beta_s\beta_d}{\beta_s + 1} \approx \beta_d
 \end{aligned} \tag{4.9}$$

Notice that the LT in all of these is a very simple constant. Thus the LT roll-off will have to be accomplished by *adding* a pole to one of the β 's. The gain derivations and evaluations for the two drive topologies are sufficiently different, though, to warrant separate developments.

Gain Calculations for Standard Drive: The gain derivation for the standard drive is quite straightforward. The relations for (ac) and (ad) turn out to be the same, as do the relations for (bc) and (bd).

$$\begin{aligned}
 \text{(ac),(ad)} \quad \text{gain} &= \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s(\beta_d + 1) + 1}{sC_s Z_{\pi s} + 1} \approx \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s \beta_d}{sC_s Z_{\pi s} + 1} \\
 \text{(bc),(bd)} \quad \text{gain} &= \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s(\beta_d + 1) + 1}{sC_s Z_{\pi s} + \beta_s + 1} \approx \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s \beta_d}{sC_s Z_{\pi s} + \beta_s}
 \end{aligned} \tag{4.10}$$

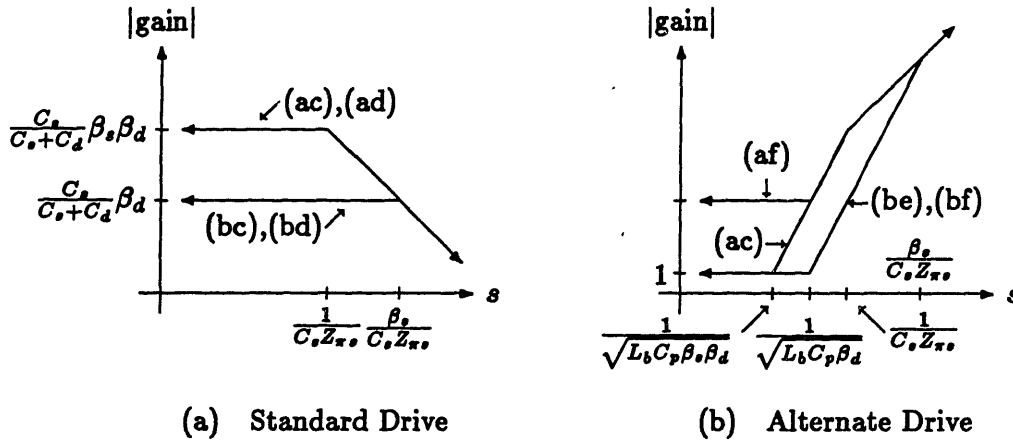


Figure 4.13: Bode Plot of Gains for Capacitor-Enhancing Circuits

A Bode plot of these relations appears in Fig. 4.13a. Notice that there is no pole at anything related to an ω_d in any of these relations. This is because the drive device in all is assumed to be a perfect incremental current-source and $Y_{out} = 0$. Thus, $\omega_d \rightarrow 0$ and the gain of all four is constant out to a single pole at ω_s . For maximum gain, therefore, the circuits should be operated below the pole. In this region:

$$\begin{aligned}
 \text{(ac),(ad)} \quad \text{gain}_{max} &\approx \left(\frac{C_s}{C_s + C_d} \right) \beta_s \beta_d \\
 \text{(bc),(bd)} \quad \text{gain}_{max} &\approx \left(\frac{C_s}{C_s + C_d} \right) \beta_d
 \end{aligned} \tag{4.11}$$

Circuits with type (a) sense achieve gain of $\sim \beta^2$ while those with type (b) sense achieve gain of only $\sim \beta$. It seems therefore, that just as with the inductor-enhancing circuits, the (a) sense method is superior. Without going into the development, the (a) type sense will have a miller pole a factor of β_s lower than will the (b) sense. With reasonable transistors, though, this ought not be a problem, and gains of β^2 ought to be achievable using the (a) sense.

There is also a definite maximum value on the effective capacitance at a given ω_{wf} with these circuits. As in section 3.2.1, maximum effective capacitance is obtained by

making C_s large enough to force the pole at ω_s to be below ω_{wf} . In all four cases, $C_{eff_{max}}$ is:

$$C_{eff_{max}} \approx \frac{\beta_s \beta_d}{\omega_{wf} Z_{\pi s}} \quad (4.12)$$

For typical bipolar transistors at 1 MHz, this is about 3 μ F.

Taking a quick glance at the gain/LT:

$$\begin{aligned} \text{(ac),(ad)} \quad \frac{\text{gain}}{\text{LT}} &\approx \frac{C_s}{C_s + C_d} \frac{1}{sC_s Z_{\pi s} + 1} \\ \text{(bc),(bd)} \quad \frac{\text{gain}}{\text{LT}} &\approx \frac{C_s}{C_s + C_d} \frac{1}{sC_s Z_{\pi s} / \beta_s + 1} \end{aligned} \quad (4.13)$$

which are always ≤ 1 .

Thus these circuits are limited in their maximum effective capacitance and have a gain/LT less than 1. For a way around these limitations look to the alternate drive topology.

Gain Calculations for Alternate Drive: All the alternate drive circuits, (-f) and (-e), again have a current-source directly in series with the main bus line. This current source will undoubtedly have to be bypassed with an inductor L_b as it was in the section on output-admittance in Chapter 3. For that reason, L_b will be included across the drive source in all the alternate-drive calculations.

$$\begin{aligned} \text{(ae)} \quad \text{gain} &= \frac{s^2 L_b C_p [\beta_s (\beta_d + 1) + 1] + s C_p Z_{\pi s} + 1}{s C_s Z_{\pi s} + 1} \\ \text{(bf)} \quad \text{gain} &= \frac{s^2 L_b C_p [\beta_s (\beta_d + 1) + 1] + s C_p Z_{\pi s} + \beta_s + 1}{s C_s Z_{\pi s} + \beta_s + 1} \\ \text{(af)} \quad \text{gain} &= \frac{s^2 L_b C_p [\beta_s (\beta_d + 1) + 1] + s C_p Z_{\pi s} + \frac{(\beta_s + 1) C_s + C_d}{C_s + C_d}}{s C_s Z_{\pi s} + 1} \\ \text{(be)} \quad \text{gain} &= \frac{s^2 L_b C_p [\beta_s (\beta_d + 1) + 1] + s C_p Z_{\pi s} + \frac{(\beta_s + 1) C_d + C_s}{C_s + C_d}}{s C_s Z_{\pi s} + \beta_s + 1} \end{aligned} \quad (4.14)$$

Assuming that L_b is large enough to cause the two zeroes to be 'lightly damped' in all of these as in Fig. 3.9, and that β is $\gg 1$, these can be simplified to:

$$\begin{aligned} \text{(ae)} \quad \text{gain} &\approx \frac{s^2 L_b C_p \beta_s \beta_d + 1}{s C_s Z_{\pi s} + 1} \\ \text{(bf)} \quad \text{gain} &\approx \frac{s^2 L_b C_p \beta_s \beta_d + \beta_s}{s C_s Z_{\pi s} + \beta_s} \\ \text{(af)} \quad \text{gain} &\approx \frac{C_s}{C_s + C_d} \frac{s^2 L_b C_d \beta_s \beta_d + \beta_s}{s C_s Z_{\pi s} + 1} \\ \text{(be)} \quad \text{gain} &\approx \frac{C_d}{C_s + C_d} \frac{s^2 L_b C_s \beta_s \beta_d + \beta_s}{s C_s Z_{\pi s} + \beta_s} \end{aligned} \quad (4.15)$$

An approximate Bode-plot of these is shown in Fig. 4.13b. Notice that in all of these, the gain is increasing with slope=1 at high frequencies. Thus, it would appear that best operation of these circuits would occur when all the poles and zeroes are as low as practical, hence making the operating frequency as far above them as possible.

Comparison to Fourth-Order Passive These alternate drive circuits all contain L_b , as do the fourth order passive filters from Chapter 2. For a clean active-to-passive comparison, above the two zeroes but below the pole, these simplify to:

$$\begin{aligned} \text{(ae),(af)} \quad \text{gain}_{act} &\approx s^2 L_b C_p \beta_a \beta_d \\ \text{(be),(bf)} \quad \text{gain}_{act} &\approx s^2 L_b C_p \beta_d \end{aligned} \quad (4.16)$$

Dividing these by (2.7) gives:

$$\begin{aligned} \text{(ae),(af)} \quad \frac{\text{gain}_{act}}{\text{gain}_{pass}} &\approx \beta_a \beta_d \\ \text{(be),(bf)} \quad \frac{\text{gain}_{act}}{\text{gain}_{pass}} &\approx \beta_d \end{aligned} \quad (4.17)$$

In this region, the active circuitry provides 'gains' of β^2 with the (a) sense and β with the (b) sense, over that which would be provided by the passive circuitry alone.

LT Calculation Near the working frequency, sL_b may be on the order of other circuit impedances. Well above that, however, where the LT roll-off is of concern, sL_b will undoubtedly be much larger than other circuit impedances. As such, the previous LT derivation, which did not consider L_b , is still valid for use with these circuits. Using the above LT relations and working above the zeroes in the gain, the gain/LT is:

$$\begin{aligned} \text{(ae),(af)} \quad \frac{\text{gain}}{\text{LT}} &\approx \frac{s^2 L_b C_p}{s C_s Z_{\pi s} + 1} \\ \text{(be),(bf)} \quad \frac{\text{gain}}{\text{LT}} &\approx \frac{s^2 L_b C_p}{s C_s Z_{\pi s} / \beta_s + 1} \end{aligned} \quad (4.18)$$

which can easily be made greater than 1.

Maximum Effective Capacitance Note also that here is no fundamental limit on the maximum effective capacitance since the gain is linear with L_b . Making L_b arbitrarily large will result in correspondingly large values for C_{eff} . It appears, then, that these circuits are valuable for creating large capacitors, while the standard topology versions are more valuable (they're simpler) for creating smaller capacitors.

Summary of Capacitor Enhancing Circuits

Just as with the inductor-enhancing circuits, those with type (a) sense provided more gain than did those with type (b) sense. Hence the (a) senses seem superior.

Unlike the inductor-enhancing, though, these circuits also differ according to the type of drive they employ. In particular, those with the standard drive exhibit a definite maximum value for gain, and a maximum value for C_{eff} . Those with the alternate drive, however, can be made to have arbitrarily large gain (by increasing L_b) and they exhibit no maximum for C_{eff} .

Also, The standard drive circuits have a gain/LT which is always less than unity, while the alternate drive have a gain/LT which can easily be made greater than unity.

Bearing all this in mind, the (a) sense, alternate drive, (ae) or (af), seem to be the most promising capacitor-enhancing circuits.

Chapter 5

Applied to Real Devices

Although there are many viable active-devices with which to construct these filter circuits, they can all be broken into two groups: bipolar transistors and field-effect transistors. Analysis of the filter circuits continues by adapting the previous three terminal model to the particular characteristics of bipolars and FETs.

5.1 Bipolar Implementations

5.1.1 Modifications to the Three-Terminal Model

The previous analysis characterized a three-terminal active device with two linear parameters; Z_π and g_m . Bode-plots and preliminary conclusions were generally made with the assumption that these model parameters were real. To re-cast the resulting equations to fit more closely the characteristics of bipolar transistors, complex values for Z_π and g_m should be used. An accepted set of parameters is for Z_π to look like a resistor in parallel with a capacitor, while g_m remains unchanged at a real conductance. β is also re-defined to be its previous value evaluated at DC. Quantitatively this means:

$$Z_\pi \doteq R_\pi \parallel \frac{1}{sC_\pi} = \frac{R_\pi}{sR_\pi C_\pi + 1} \quad \text{and} \quad \beta \doteq g_m R_\pi.$$

The three terminal model, redrawn to show the different elements, is shown in Fig. 5.1.

For good RF “radio-frequency” bipolars at typical operating points, the pole in Z_π at $1/R_\pi C_\pi$ occurs in the tens of mega-Hertz range. For operation around 1 MHz, therefore, the previous analysis, assuming that Z_π was real, will apply fairly well.

The previous analysis has shown that, in all cases circuits with sense-type (a) were superior to those with sense-type (b). Those circuits with (b) sense will hence be discarded as inferior. Extensive, and quite parallel to those upcoming, calculations to justify this exclusion have been carried out, but will not be included here to avoid tedium.

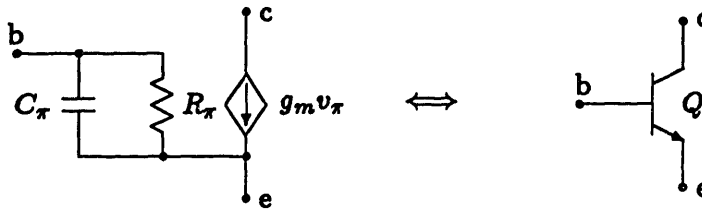


Figure 5.1: Model for Bipolar Transistors

5.1.2 Values for Model Parameters

The values for the model parameters, g_m , R_π , and C_π are highly dependant on the quiescent operating point of the transistor and can be derived from device physics.¹ An accepted value for g_m is:

$$g_m = \frac{q}{kT} I_c \approx 40 I_c \quad (5.1)$$

for operation at room temperature.

I_c is the quiescent collector current of the transistor. Typically, small signal discrete bipolars are biased for collector currents of between 1 and 10 mA. High-speed RF bipolars are biased slightly stronger; collector currents of between 5 and 20 mA for optimal operation. This translates to typical values for g_m of:

$$\begin{aligned} \text{Standard Bipolars:} & \quad 0.04 \leq g_m \leq 0.4 \text{ U} \\ \text{RF Bipolars:} & \quad 0.2 \leq g_m \leq 0.8 \text{ U} \end{aligned} \quad (5.2)$$

R_π is defined as β_f/g_m . For standard bipolars, β_f is typically ~ 100 and for RF bipolars it is typically ~ 50 . This translates to:

$$\begin{aligned} \text{Standard Bipolars:} & \quad 2500 \geq R_\pi \geq 250 \Omega \\ \text{RF Bipolars:} & \quad 250 \geq R_\pi \geq 62 \Omega \end{aligned} \quad (5.3)$$

The value for C_π is not so easily determined without knowing the details of the construction of the particular device. C_π is instead generally found by measurement or published specifications. Around typical operating points, C_π *might* be something like:²

$$\begin{aligned} \text{Standard Bipolars:} & \quad C_\pi \approx 25 \times 10^{-9} I_c \quad \text{so that} \quad 25 \leq C_\pi \leq 250 \text{ pF} \\ \text{RF Bipolars:} & \quad C_\pi \approx 1.6 \times 10^{-9} I_c \quad \text{so that} \quad 8 \leq C_\pi \leq 32 \text{ pF} \end{aligned} \quad (5.4)$$

¹See [5], section 6.5, for a derivation of these model parameters.

²From [13], pp. 33

5.1.3 Limitations of the Model

The three terminal model in use is a simplified version of the accepted hybrid- π linear model for bipolar transistors. The most significant simplification here is the elimination of C_μ , the capacitance between base and collector. Also called the miller-capacitor, C_μ , is typically much smaller than C_π . Thus this *seems* like a valid simplification, at least for obtaining a general feel as to the operation of different circuits.

Miller-Pole Discussion: In some topologies, however, C_μ becomes definitely more important than C_π through what is called the miller-pole.³ A low miller-pole is generally formed when a transistor is operated in a common-emitter configuration, and the base is driven from a relatively high impedance. The effect is that C_μ is made to look larger by a factor of the voltage gain. In this way, C_μ comes to dominate over C_π as the dominant-pole placing capacitor.

One would normally expect that with both C_π and C_μ there would be two poles to worry about. It turns out, however, that the second pole is at very high frequencies even with a low miller-pole. In this situation C_π can be replaced with C_{tot} where:

$$C_{tot} = C_\pi + (\text{voltage gain}) \times C_\mu$$

which can easily be much larger than C_π . Thus, though C_μ may affect the *placement* of the dominant pole, it will not *add* another pole below the UGC which would cause the amplifier to be unstable. In this light, analysis without C_μ continues.

High-Frequency Model Limitations: One common specification for comparing various bipolars is the published f_t . f_t is generally defined as the frequency at which the magnitude of the base current *would be* equal to that of the collector current. With the simple model above:

$$f_t \approx \frac{1}{2\pi} \frac{g_m}{C_\pi} = \frac{1}{2\pi} \frac{\beta}{R_\pi C_\pi}$$

which is truly *very* high. Generic bipolars have f_t 's in the 100-500 MHz region while good RF bipolars have f_t 's in the 4 GHz region. It should be noted, though, that f_t can not be actually measured because the simple model used here, and even the more complete hybrid- π model, are **definitely not valid** in this frequency range. f_t is instead calculated by extrapolation of measurements taken at much lower frequencies. A published value for f_t is often used in the above equation to arrive at a value for C_π .

5.1.4 Inductor-Enhancing Circuits

Bipolar versions of the two (a) sense inductor-enhancing circuits, completely devoid of any bias circuitry, are shown in Fig. 5.2. It should be pointed out that the polarity of bipolars in Fig. 5.2 does not matter, except to the bias circuitry. The polarities shown

³See [3], section 14.6, for a discussion of the miller-pole.

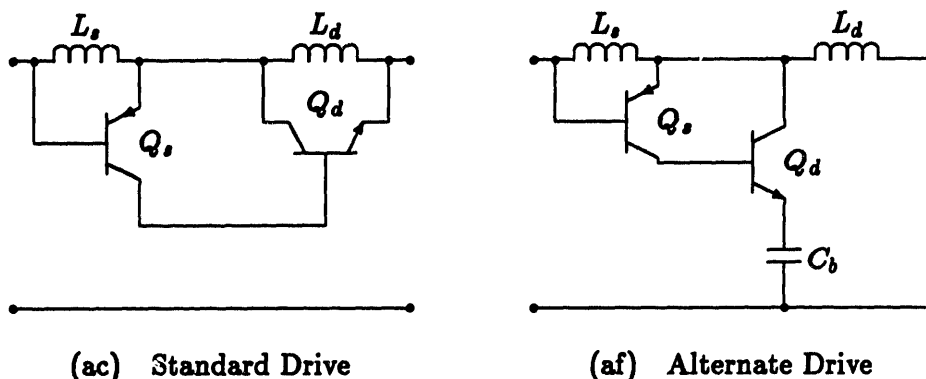


Figure 5.2: Bipolar Implementation of Inductor-Enhancing Circuits

are only to help the reader visualize the operation of the circuits. Re-grinding (4.4) with the new model parameters gives:

$$\text{gain} \approx \frac{sL_p H(s) + R_{\pi s}(sR_{\pi d}C_{\pi d} + 1)}{(sR_{\pi d}C_{\pi d} + 1)[sL_s(sR_{\pi s}C_{\pi s} + 1) + R_{\pi s}]} \quad (5.5)$$

where

$$H(s) \doteq s^2 R_{\pi s} R_{\pi d} C_{\pi s} C_{\pi d} + s(\beta_s + 1)R_{\pi d}C_{\pi d} + \beta_s \beta_d + 1$$

for the gain of both circuits.

Instead of making the numerator into a full cubic in s and then trying to factor it into individual zeroes, a quick examination of $H(s)$ is valuable. If both transistors are identical, the roots of $H(s)$ are at:

$$\omega_H = (-1 \pm j\sqrt{3}) \frac{\beta}{2R_{\pi}C_{\pi}}$$

which is near f_t and in the invalid region for the model. With this in mind, analysis significantly below f_t can assume that

$$H(s) = \beta_s \beta_d + 1 \approx \beta_s \beta_d$$

Similarly, the [] term in the denominator is the sense impedance. Assuming that

$$\frac{R_{\pi s}}{L_s} < \frac{1}{R_{\pi s}C_{\pi s}}$$

(which should be a good assumption) the denominator can be factored to yield:

$$\text{gain} \approx \frac{s(\beta_s \beta_d L_p + R_{\pi s} R_{\pi d} C_{\pi d}) + R_{\pi s}}{(sR_{\pi d}C_{\pi d} + 1)(sR_{\pi s}C_{\pi s} + 1)(sL_s + R_{\pi s})} \quad (5.6)$$

This can be further simplified by ignoring the $+R_{\pi s} R_{\pi d} C_{\pi d}$ term in the numerator. A Bode-plot of this looks like Fig. 5.3. Below the pole at $s = 1/R_{\pi d}C_{\pi d}$, this looks exactly the same as Fig. 4.13.

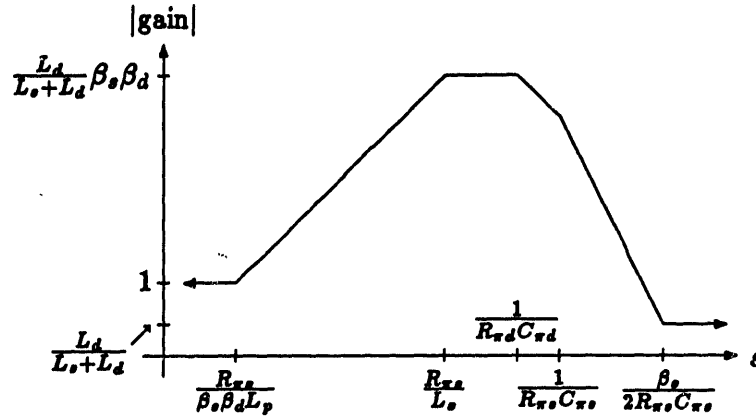


Figure 5.3: Bode-plot of Gain for Bipolar Inductor-Enhancing Circuits

The maximum gain of these circuits is $\frac{L_d}{L_s + L_d} \beta_s \beta_d$ and they exhibit no limit on the maximum effective-inductance. With β 's of only 50 then, gains greater than 1000 ought to be achievable.

Maximum gain is achieved by operating above the pole at R_{π_s}/L_s . For a 1 MHz operating frequency, and R_{π_s} of 100 Ω , L_s should be greater than 16 μH . If L_s and L_d are then both picked to be 16 μH , a gain of 1000 would create an effective inductance of 32 mH. This is a rather large inductor, especially for most 1 MHz filter applications, so these bipolar circuits seem to be able to provide *plenty* of inductance. Any inductance smaller than this 32 mH can of course be created by shrinking either L_s , L_d , or both, but the circuit may not work with gain of 1000 under those conditions.

The ease of successfully achieving this gain is governed, of course, by the loop-transmission. From (4.6), the LT for these circuits is:

$$\text{LT} = \frac{sL_p \beta_s \beta_d}{(sR_{\pi_d} C_{\pi_d} + 1)[sL_p (sR_{\pi_s} C_{\pi_s} + \beta_s + 1) + R_{\pi_s}]} \quad (5.7)$$

Making the same assumptions as in (5.6) simplifies this to:

$$\text{LT} \approx \frac{sL_p \beta_s \beta_d}{(sL_p + R_{\pi_s}/\beta_s)(sR_{\pi_d} C_{\pi_d} + 1)(sR_{\pi_s} C_{\pi_s} + \beta_s)} \quad (5.8)$$

In this LT equation, the pole at $R_{\pi_s}/\beta_s L_p$ occurs first and serves to level off the LT from the zero at zero. Next will be the pole at $1/R_{\pi_d} C_{\pi_d}$ and it will have to serve as the dominant LT roll-off pole. The region of maximum gain, and hence desired working frequency for the filter, occurs just below the $R_{\pi_d} C_{\pi_d}$ pole. The LT in this region can be seen to be simply β_d .

For guaranteed stability, the third pole, at $\beta_s/R_{\pi_s} C_{\pi_s}$, will have to occur above the UGC. This third pole is at f_z though, so quantitative calculations of the LT or gain don't mean much in this range.

Dividing the (5.5) by (5.7) to arrive at the figure-of-merit gives:

$$\frac{\text{gain}}{\text{LT}} \approx \frac{(s\beta_s\beta_d L_p + R_{\pi_s})(sL_p\beta_s + R_{\pi_s})(sR_{\pi_s}C_{\pi_s} + \beta_s)}{s\beta_s^2\beta_d L_p(sL_s + R_{\pi_s})(sR_{\pi_s}C_{\pi_s} + 1)} \quad (5.9)$$

A Bode-plot of both of this looks just like Fig. 4.9 up to the pole at $s = 1/R_{\pi_s}C_{\pi_s}$.

Miller-Pole Considerations: Without going too far into the derivation, (ac) will experience a low Miller-pole while (af) will not. This can be seen qualitatively, by realizing that in (ac), the miller-capacitor of Q_s sees roughly v_r (which is comparatively large). The current flowing through this capacitor subtracts from the transistor's base drive current reducing the circuit's gain. In (af), on the other hand, neither of the miller-capacitors see a voltage as large as v_r . For the same v_r then, the transistors in (af) will have larger base current and hence larger gain.

If this miller pole is kept above the working frequency, then there is no real difference between the circuits. If, alternatively, the miller pole in (ac) occurs below the working frequency, then (af) is the circuit to use.

5.1.5 Capacitor-Enhancing Circuits

There are four capacitor-enhancing circuits from Chapter 3 with type (a) sense. Bipolar versions of them are depicted in Fig. 5.4.

Making the same assumptions as used in the preceding bipolar inductor-enhancing circuits, to the capacitor-enhancing relations, (4.10) and (4.15), gives the gain for each of these:

$$\begin{aligned} \text{(ac),(ad)} \quad \text{gain} &\approx \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s\beta_d}{(sR_{\pi_d}C_{\pi_d} + 1)[s(C_s + C_{\pi_s})R_{\pi_s} + 1]} \\ \text{(ae)} \quad \text{gain} &\approx \frac{s^2 L_b C_p \beta_s \beta_d + s(R_{\pi_s}C_{\pi_s} + R_{\pi_d}C_{\pi_d}) + 1}{(sR_{\pi_d}C_{\pi_d} + 1)[s(C_s + C_{\pi_s})R_{\pi_s} + 1]} \\ \text{(af)} \quad \text{gain} &\approx \left(\frac{C_s}{C_s + C_d} \right) \frac{s^2 L_b C_d \beta_s \beta_d + s\beta_s R_{\pi_d} C_{\pi_d} + \beta_s}{(sR_{\pi_d}C_{\pi_d} + 1)[s(C_s + C_{\pi_s})R_{\pi_s} + 1]} \end{aligned} \quad (5.10)$$

In general, C_{π_s} will be much less than C_s , so the denominators of these can be simplified by ignoring C_{π_s} . For the standard drive circuits, maximum gain is achieved by operating *below* both of the poles, while for the alternate drive circuits, the maximum gain is achieved *above* all the poles and zeroes. Under these conditions:

$$\begin{aligned} \text{(ac),(ad)} \quad \text{gain}_{\text{max}} &\approx \left(\frac{C_s}{C_s + C_d} \right) \beta_s \beta_d \\ \text{(ae),(af)} \quad \text{gain}_{\text{max}} &\approx \left(\frac{C_d}{C_s + C_d} \right) g_{ms} g_{md} \frac{L_b}{C_{\pi_d}} \end{aligned} \quad (5.11)$$

Note that while the standard drive circuits are limited to gains on the order of $\beta_s\beta_d$ (a very large number), the alternate drive circuits can achieve extremely high gains by increasing L_b . With the typical values mentioned in section 5.1.2 and $L_b = 10 \mu\text{H}$, for example, gains on the order of 10^5 should be achievable.

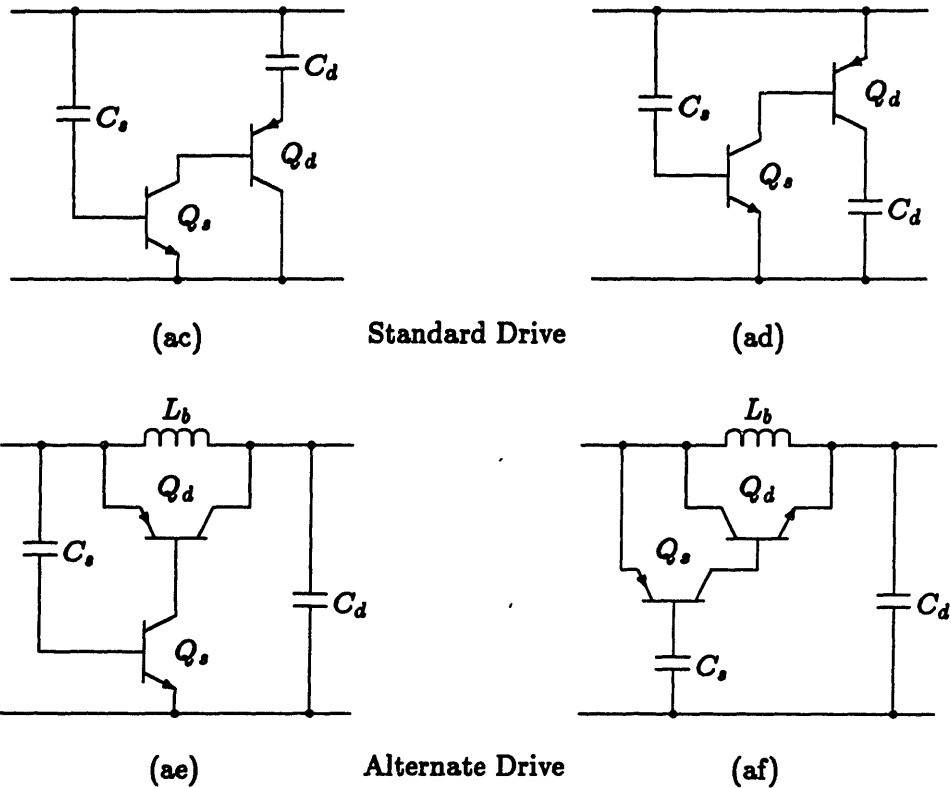


Figure 5.4: Four Bipolar Capacitor-Enhancing Circuits

LT Analysis: From equation (4.9), the LT for all these circuits can be re-derived to be:

$$LT \approx \frac{\beta_s \beta_d}{(sR_{\pi s} C_{\pi s} + 1)(sR_{\pi d} C_{\pi d} + 1)} \quad (5.12)$$

Which can immediately be seen to be extremely troublesome. This LT equation has its two poles at roughly the same frequency. Without modification, this will result in an unstable system. The only solution to this problem is to add more capacitance to either $C_{\pi s}$ or $C_{\pi d}$ to make one of them into the dominant LT roll-off pole. Given that the LT below this roll-off pole is $\beta_s \beta_d$, and that the other LT pole cannot occur until above the UGC, the selected capacitor will have to be increased by a factor like $\beta_s \beta_d$.

This is a huge increase in capacitance and care must be taken so as to decrease the gain as little as possible. Examination of (5.10) shows that, while $C_{\pi d}$ directly affects a pole in the gain, $C_{\pi s}$ does not affect the gain until $C_{\pi s} \approx C_s$. Thus, adding extra capacitance to $C_{\pi s}$ will have less influence on the gain than will adding capacitance to $C_{\pi d}$.

Increasing $C_{\pi s}$ by a factor of $\beta_s \beta_d$ will make $C_{\pi s}$ much larger than C_s . Making this

substitution in (5.10) gives:

$$\begin{aligned}
\text{(ac),(ad)} \quad \text{gain} &\approx \left(\frac{C_s}{C_s + C_d} \right) \frac{\beta_s \beta_d}{(sR_{\pi d}C_{\pi d} + 1)(sC_{\pi s}R_{\pi s} + 1)} \\
\text{(ae)} \quad \text{gain} &\approx \frac{s^2 L_b C_p \beta_s \beta_d + sR_{\pi s}C_{\pi s} + 1}{(sR_{\pi d}C_{\pi d} + 1)(sC_{\pi s}R_{\pi s} + 1)} \\
\text{(af)} \quad \text{gain} &\approx \left(\frac{C_s}{C_s + C_d} \right) \frac{s^2 L_b C_d \beta_s \beta_d + s\beta_s R_{\pi d}C_{\pi d} + \beta_s}{(sR_{\pi d}C_{\pi d} + 1)(sC_{\pi s}R_{\pi s} + 1)}
\end{aligned} \tag{5.13}$$

All of these now have a pole at $\omega = 1/R_{\pi s}C_{\pi s}$, which will certainly be below the operating frequency. With this in mind, and assuming that $R_{\pi s} \approx R_{\pi d}$, these equations can be made to look like:

$$\begin{aligned}
\text{(ac),(ad)} \quad \text{gain}_{max} &= \left(\frac{C_s}{C_s + C_d} \right) \frac{UGC}{\omega_{wf}} \\
\text{(ae),(af)} \quad \text{gain}_{max} &= UGC^2 L_b C_p
\end{aligned} \tag{5.14}$$

where

$$UGC \leq \frac{1}{R_{\pi d}C_{\pi d}}$$

Notice that in (ac) and (ad), the gain is limited (to a rather low value) by the pole at $1/R_{\pi d}C_{\pi d}$. In (ea) and (af), however, the gain is still linear in L_b .

Since the alternate drive circuits use the extra inductor L_b , they can be better evaluated by performing an active-to-passive gain comparison as done several times previously. Dividing this last equation by (2.7) gives:

$$\text{(ae),(af)} \quad \frac{\text{gain}_{act}}{\text{gain}_{pass}} = \frac{UGC^2}{\omega_{wf}^2} \tag{5.15}$$

Thus, the alternate-drive circuits achieve the square of the 'gain' of the standard-drive circuits. If the $R_{\pi d}C_{\pi d}$ pole is at 20MHz and the working frequency is 1MHz, then these alternate-drive circuits could provide about 400 times the gain of a fourth-order-passive filter, for the same L_b and C_p . Conversely, under the same conditions, the standard drive circuits could only provide a capacitor-enhancement of roughly 20.

5.2 FET Implementations

There are several types of field-effect transistors. Fortunately, the incremental model for all of them is essentially the same. Junction field-effect transistors (JFETs) will be generally considered here, because discrete RF FETs are more available as JFETs than as other types of FETs. The equations to be developed below will, however, apply equally well to other types of FETs with appropriate values for the model parameters.

5.2.1 Modifications to the Three-Terminal Model

To make the three-terminal from Chapter 3 fit the characteristics of field-effect transistors, Z_π is made to look like a capacitor C_{gs} while g_m is again left as a pure transconductance. The resultant model is shown in Fig. 5.5.

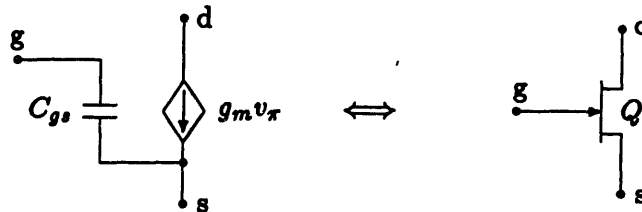


Figure 5.5: Model for Field-Effect Transistors

5.2.2 Values for Model Parameters

Typical values for the model parameters RF JFETs at reasonable bias levels are:⁴

$$\begin{aligned} 1 &\leq g_m \leq 10 \text{ mU} \\ 2 &\leq C_{gs} \leq 5 \text{ pF} \end{aligned} \quad (5.16)$$

Note that g_m for FETs is roughly a factor of 80 below that for good RF bipolars, and C_{gs} for FETs is a factor of about 8 below the C_π of bipolars.

FETs are rated with f_t in the same manner as are bipolars. For a FET,

$$f_t = \frac{g_m}{C_{gs}} \quad (5.17)$$

Thus f_t for FETs is found to be a factor of approximately 10 below that for good RF bipolars. Later this will be a telling parameter.

⁴From [14], pp. 30

5.2.3 Inductor-Enhancing Circuits

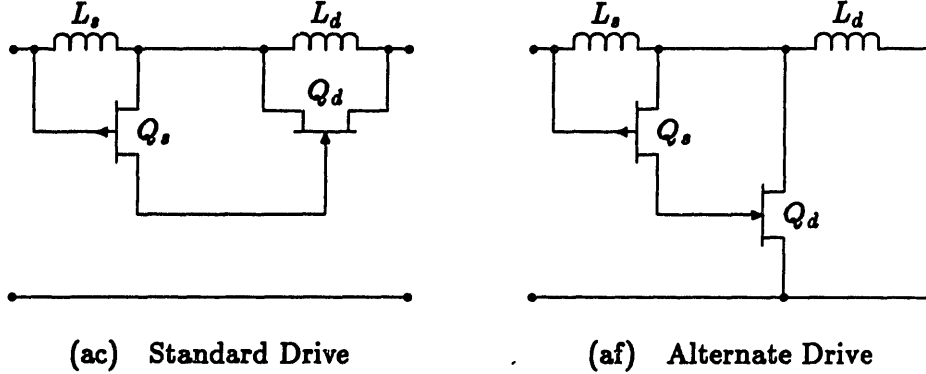


Figure 5.6: JFET Implementation of Inductor-Enhancing Circuits

The two type (a) sense, inductor-enhancing circuits from Chapter 3 implemented with JFETs are shown in Fig. 5.6. Substituting the above model parameters into the gain relations for these two, (4.4), gives:

$$\text{gain} = \left(\frac{L_p}{C_{gsd}} \right) \frac{s^2 C_{gs} C_{gsd} + s C_{gsd} g_{ms} + g_{ms} g_{md} + \frac{C_{gsd}}{L_p}}{s^2 L_s C_{gs} + 1} \quad (5.18)$$

For typical values, $g_{ms} g_{md} \gg C_{gsd}/L_p$, so the C_{gsd}/L_p term in the denominator can be ignored. If both FETs are identical, then the complex zeroes of this gain expression are at:

$$\omega_z = (-1 \pm j\sqrt{3}) \frac{g_m}{2C_{gs}} \approx (-1 \pm j\sqrt{3}) 50 \text{ MHz} \quad (5.19)$$

for typical JFETs. Since these are well above the proposed working frequencies, the numerator can be kept flat at $g_{ms} g_{md}$ through the range of interest. Keep in mind, though, that there are really two VHF zeroes in the following gain expressions. With these simplifications, the gain expression becomes:

$$\text{gain} \approx \left(\frac{L_p}{C_{gsd}} \right) \frac{g_{ms} g_{md}}{s^2 L_s C_{gs} + 1} \quad (5.20)$$

An approximate Bode-plot of (5.20) looks like Fig. 5.7. In the low frequency region, below all the poles and zeroes, the gain is maximized:

$$\text{gain}_{\text{max}} \approx g_{ms} g_{md} \frac{L_p}{C_{gsd}}, \quad (5.21)$$

For the small-signal JFET parameters mentioned above, this maximum gain is in the vicinity of 100. Thus, while bipolars could theoretically provide gains of 1000, JFETs in similar circuits can provide gains of only around 100. The difference lies mainly in the relative g_m for bipolars and FETs.

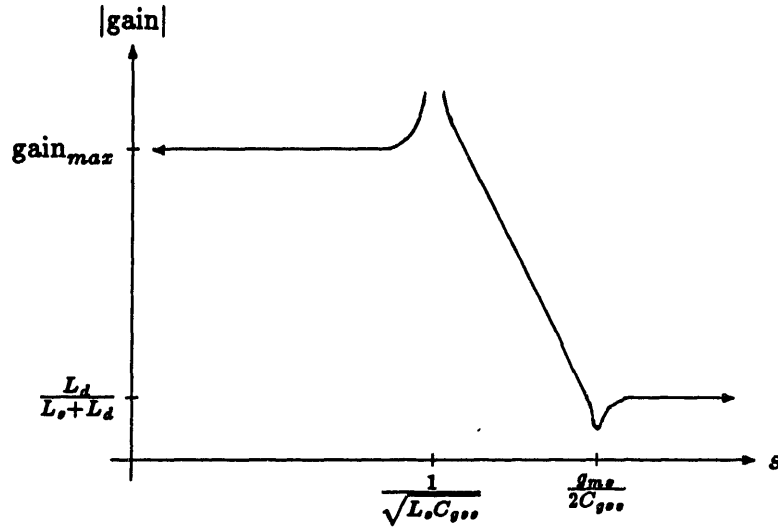


Figure 5.7: Bode-plot of Gain for JFET Inductor-Enhancing Circuits

LT Discussion: Making the same FET parameter substitutions in (4.6) gives the LT for these circuits:

$$LT = \left(\frac{L_p}{C_{gsd}} \right) \frac{g_{ms}g_{md}}{sL_p(g_{ms} + sC_{gss}) + 1} \quad (5.22)$$

The poles are real and widely separated, so the denominator can be re-factored to be:

$$LT \approx \left(\frac{L_p}{C_{gsd}} \right) \frac{g_{ms}g_{md}}{(sL_p + 1/g_{ms})(sC_{gss} + g_{ms})} \quad (5.23)$$

Just as with the bipolar implementations, this has the nice dominant roll-off pole at $1/L_p g_{ms}$, and high UGC-limiting pole near f_t .

Dividing (5.20) by (5.23) below f_t , gives the gain/LT:

$$\frac{\text{gain}}{LT} = \frac{sL_p g_{ms} + 1}{s^2 L_s C_{gss} + 1} \quad (5.24)$$

A bode-plot of this looks like Fig. 5.8

Thus, for reasonable operation, the circuits ought to be operated above the LT roll-off pole at $1/L_p g_{ms}$, but somewhat below the imaginary gain poles at $1/\sqrt{L_p C_{gss}}$. For high gain/LT, the circuit could be operated above this imaginary pole pair, but the gain is falling off rapidly in this region, so it is of no real value.

If the working frequency is again considered to be 1 MHz, and a g_m of 4 mS is assumed, then in order to operate above the LT pole, $L_p > 40 \mu\text{H}$. In order for the imaginary pole pair to be above 1 MHz, with $C_{gs} = 4 \text{ pF}$, L_p should be less than 6 mH. In general, it is desirable to operate with a fairly large gain/LT so a value for L_p in the milli-H region seems appropriate.

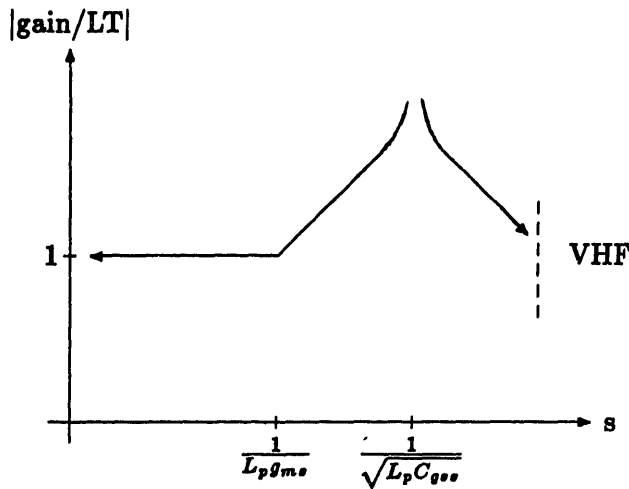


Figure 5.8: Bode-plot of Gain/LT for FET Inductor-Enhancing Circuits

This is, however, a *very large* inductor. When multiplied by the gain of the circuit (~ 100), the effective-inductance would be in the 0.1 H region. Only in special cases is an inductor of 0.1 H called for, so this seems a bit excessive. Notice that for attempting to make more reasonably sized inductors, the gain/LT is decreasing, and in fact, when trying to make inductors of less than about 4 mH, the gain/LT is unity.

Thus, while bipolar inductor-enhancing circuits appear to be able to provide gains of 1000 over a wide range of useful effective-inductances, FET inductor-enhancing circuits can only provide gains around 100, and seem best suited for producing rather large inductors. With this in mind it seems that bipolar implementations are more generally useful than are FET implementations.

5.2.4 Capacitor-Enhancing FET Circuits

LT Discussion: The four capacitor-enhancing circuits, implemented with JFET's, are shown in Fig. 5.9. Substituting the FET model parameters from (5.16) into the capacitor-enhancing loop-transmission relations, (4.9) gives:

$$LT = \frac{g_{ms}g_{md}}{s^2C_{gs}C_{gd}} \quad (5.25)$$

which has the immediate problem of having two poles at the origin. This loop-transmission indicates that the closed loop system will definitely be unstable. Thus, it seems that two FETs cannot be used to construct one of these active filters. A possible fix to this problem would be to add a resistor across the $g - s$ terminals of one of the FETs. This would move one of the poles from the origin to $1/RC_{gs}$. As long as this pole was above the UGC (the remaining pole at the origin would serve to roll-off the LT) the system would be stable.

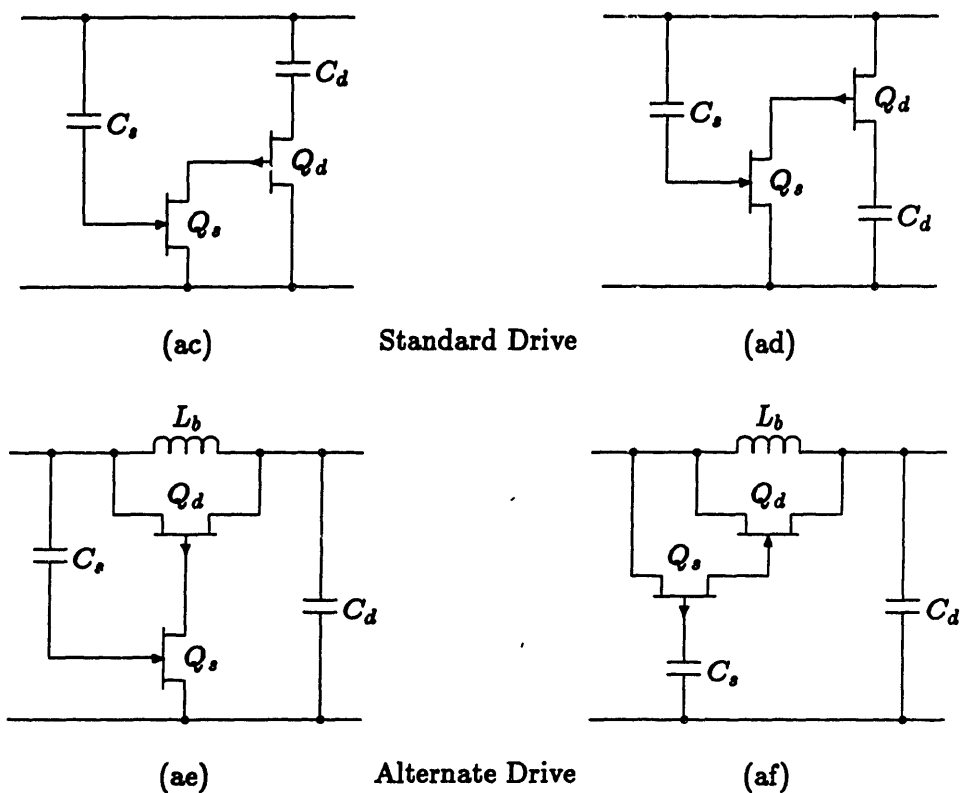


Figure 5.9: Four FET Capacitor-Enhancing Circuits

Adding this resistor has made this FET look exactly like a bipolar transistor, however. It can be shown that, since the g_m 's of bipolars are greater than those of FETs, replacing this FET with a real bipolar will provide more gain than simply adding a resistor to the FET. Thus FETs seem inferior to bipolars for constructing the capacitor-enhancing circuits.

5.3 Conclusions

The most important conclusion reached through this development is that in both the inductor and the capacitor-enhancing circuits, bipolar implementations achieved higher gains and more useful operating areas than did FET implementations. Hence, from here forward, only the bipolar implementations will be developed.

For inductor-enhancing circuits, there again appeared to be no fundamental differences between the standard-drive and the alternate-drive circuits except for the miller-pole in the standard-drive. To avoid possible gain limitations due to this miller-pole, the alternate-drive, bipolar circuit seems to be the best of all the inductor-enhancing circuits.

With capacitor-enhancing circuits, the alternate-drive version was definitely better than the standard-drive version. Here too, the alternate-drive, bipolar, capacitor-

enhancing circuit seems to be the one to pursue.

Chapter 6

Filter Implementation

The previous analysis has shown that active inductor-enhancing and capacitor-enhancing filter circuits, using only two bipolar transistors each, should be able to achieve gains of nearly 1000. Now comes the challenge of actually designing and constructing *useful* filters which achieve these high gains. To maintain completeness, both types of filter circuits will continue to be developed, but to save time, only an inductor-enhancing circuit will actually be constructed. Before designing any circuit, however, the goals of the design must be more formally defined.

6.1 Goals of the Design

The purpose of these active filters is to allow a given power circuit to meet an applicable high-frequency noise specification, with a 'minimum-cost' filter network.

6.1.1 Power Circuit Specifications

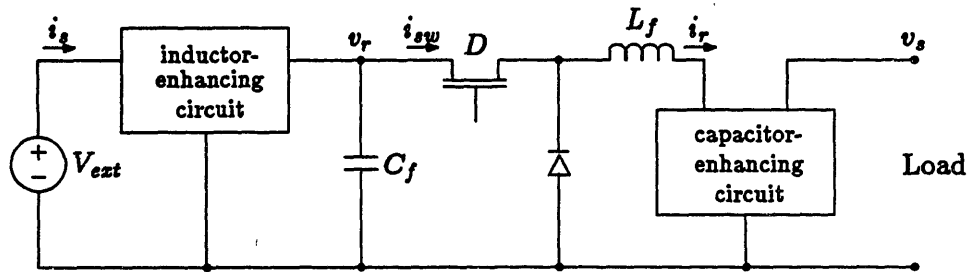


Figure 6.1: Prototype Power Circuit and Filters

The power circuit, at least initially, will be a basic down-converter. It, along with both of its ripple filters, is shown in Fig 6.1. Specifications for the converter are:

1. Switching frequency: 1 MHz nominal
2. Input voltage range: 40 - 80 V
3. Input current (DC) range: 0 - 5 A
4. Output voltage: 30 V nominal
5. Output current range: 0 - 7 A

Optimal design of an active filter circuit must consider the peak currents and voltages which it will see. The inductor-enhancing circuit will, in general, have to see the full DC supply-voltage of 80 V and the full DC input-current of 5 A. The capacitor-enhancing circuit sees the full output voltage of 30 V and the full output current of 7 A.

Based on these requirements, the design criteria for the two filters are somewhat different. While the inductor-enhancing circuit certainly needs to be isolated from the input bus for both current and voltage, there is the possibility that the capacitor-enhancing circuit could withstand the output voltage directly. If this converter was to have lower output voltage, like 5 V, then the capacitor-enhancing circuit would almost certainly be designed to utilize this by powering itself directly from the output bus.

6.1.2 Noise Specifications

The noise specifications are chosen to comply with the most stringent standards in common use.

For current-ripple from a low-impedance source, the most stringent specification seems to be that from MIL-STD-461B CE03, as shown in Fig 1.1. At the nominal 1 MHz switching frequency of the above converter, the allowable ripple-current is 25 dB μ A, or 20 μ A. The specification continues to decrease until 2 MHz where it levels off at 20 dB μ A, or 10 μ A.

For voltage-ripple from a high-impedance source, an applicable specification is found in DEC-STD 103.[12] Compliance with DEC STD 103 also insures compliance with applicable FCC (United States) and VDE (European) standards. At 1 MHz, the ripple-voltage limitation is 48 dB μ V, or 250 μ V.

Required Ripple-Attenuation

The design of filters to meet these specifications will concern itself with only the *fundamental* sine-wave component of the input-current and output-voltage. The input current to the converter will be assumed to be a square-wave from zero to a maximum of 7 A. Assuming that the duty cycle is 50% (a worst case assumption), the fundamental component of this current will be

$$\frac{4}{\pi} 3.5 A \approx 4.5 A_{peak} = 3.2 A_{RMS} \quad (6.1)$$

The MIL-STD specifies a maximum ripple-current of 25 μ A RMS at 1 MHz, so this converter needs an input ripple-current attenuation of 150×10^3 .

Similarly, the output voltage of the converter is assumed to be a square-wave from zero to a maximum of 80 V. This yields a fundamental component of

$$\left(\frac{4}{\pi}\right) 40 \text{ V} \approx 51 V_{peak} = 36 V_{RMS} \quad (6.2)$$

The DEC STD limits the voltage-ripple to $250 \mu\text{V}$ so an attenuation of about 150×10^3 is again required.

6.2 Passive Filters to Achieve the Required Filtration

As a basis for comparison, an adequate second-order passive LC filter, like those in Fig. 2.1 should be designed to provide the required attenuation of 150×10^3 . Substituting this attenuation, and the 1 MHz operating frequency, into eq. (2.1) gives:

$$L_f C_f \approx 3.8 \times 10^{-9}$$

As a further criterion for selecting L_f and C_f , the quiescent energy of the capacitor and the inductor are often set equal:

$$L_f I_{DC}^2 \approx C_f V_{DC}^2$$

assuming a quiescent operating point of 40 V and 3.5 A, this relationship gives:

$$\frac{L_f}{C_f} \approx 130$$

Solving these two simultaneously:

$$\begin{aligned} C_f &= 5.6 \mu\text{F} \\ L_f &= 725 \mu\text{H} \end{aligned} \quad (6.3)$$

Though rather large and impractical, these can still be used as a basis for comparison. Anyone designing a *practical* passive filter for this application would undoubtedly use a fourth-order filter, as was illustrated in Fig. 2.2. Following the procedure outlined above, the filter elements for either fourth-order voltage or current filters are:

$$\begin{aligned} C_f &= 0.28 \mu\text{F} \\ L_f &= 36 \mu\text{H} \end{aligned} \quad (6.4)$$

which are much more reasonably sized. These fourth-order filters contain two of both C_f and L_f . Thus the total capacitance used in the fourth-order filter is $0.56 \mu\text{F}$ and the total inductance is $72 \mu\text{H}$. Note that each of these is exactly a factor of 10 below that used in the 2nd order filter above.

6.3 Amplifier Topologies

Within the constraints of all the previous analysis, which considered only small-signal behavior, there are still several possible amplifier configurations to be considered. The actual configuration will determine the biasing scheme, power dissipation, and complexity of the overall circuit. The different configurations can be loosely grouped by the 'class' of their output stage¹.

6.3.1 Class A, Single-Ended

The class A amplifier is the simplest. Its output stage consists of a single active device biased to conduct at all times. The bias current through, and voltage across, the active device are therefore greater than the peak current and voltage to be supplied by the amplifier. Furthermore, the current through the active device at one of the signal peaks is greater than twice the amplifier output current. The class A amplifier, therefore, exhibits an internal power dissipation which is larger than the power it supplies to the load ($\eta < 50\%$) and it is generally used for low-level amplifiers where this dissipation is not objectionable.

6.3.2 Class B, Push-Pull

The class B, push-pull amplifier uses at least two active devices which alternately amplify the positive and negative portions of the signal. They are generally biased to just begin conducting at the midpoint of the signal and as such the amplifier exhibits very low (ideally zero) quiescent power dissipation. Furthermore, each output device carries a peak current only slightly greater than the peak output current. These output stages, then, are generally used in higher-power, linear amplifiers where efficiency or power dissipation is of concern.

For our prototype application, a class A amplifier will be used for its simplicity. Though quite feasible, it is felt that the complexities associated with biasing and controlling two output devices for the push-pull stage would unnecessarily hamper the project.

6.3.3 Power Dissipation vs. High Gain

For the *same* allowable ripple at a filter's output, raising the gain of an active filter circuit will result in more power dissipation. To see this, consider the two inductor-enhancing circuits shown in Fig. 5.2. In both, it is easy to show that $i_{cd} \propto \text{gain} \times i_s$.

Thus, with the class A output stage, raising the gain necessitates that the bias current and hence the quiescent power dissipation also be raised. At 1 MHz this soon becomes the limiting factor in how large the gain can be. Continuing the inductor-enhancing example, if i_s is allowed to be $20 \mu\text{A}$ per MIL-STD-461B at 1 MHz, then at a gain of 500, i_{cd} must be biased at nearly 10 mA. Though 10 mA is not too large, orders

¹The classes are based in antiquity. See [8] pp. 13-23 for a discussion

of magnitude more gain can certainly not be handled with this simple class A output stage. This limitation can be overcome, to a certain extent, by moving to a push-pull output stage. Even so, currents in excess of 100 mA are going to be difficult to handle with good RF bipolar transistors.

Potential for Higher Frequency Operation

For the same LT roll-off criteria, as the desired operating frequency of these filters is raised, the achievable gain ought to be lowered proportionately. Since power dissipation is proportional to gain, raising the operating frequency will lower the power dissipation. Thus, if the operating frequency is raised significantly above 1 MHz, excessive power dissipation will no longer be the gain limiting factor. If gains of 1000 at 1 MHz are impractical due to excessive power dissipation, then gains of 100 ought to be achievable at 10 MHz with no worry about power dissipation. These reasonably high gains at 10 MHz are potentially very valuable for very-high switching frequency power circuits.

6.4 Low Frequency Roll-Off of the Loop-Transmission

Much attention has been given to the high-frequency LT roll-off. Making the $|LT|$ decrease through unity before the $\angle LT = 180^\circ$ is necessary for the amplifier to be stable. Just as vital, is consideration of the LT 'roll-on' at low frequencies. At DC the LT of all these circuits is zero. For stability, it is *also* necessary that the $\angle LT$ be less than 180° when the $|LT|$ passes through unity at low frequencies.

This has not been a topic of discussion previously because, unlike the high-frequency roll-off whose limitations are governed largely by circuit parasitics, the low-frequency roll-off is entirely controlled by finite sized, tangible, circuit elements. Thus the low-frequency LT poles and zeroes are entirely within the control of the circuit designer.

Recalling the high-frequency roll-off criteria, it would obviously be desirable to accomplish the low-frequency roll-on with a single zero near DC and single pole below the circuit's working frequency. As such, the angle of the LT would never exceed 90° and the circuit would be guaranteed stable.

From the analysis of Chapter 3, the LT in all the circuits had a single zero at DC and pole as desired. This means, however, that to satisfy the above stability condition, the amplifier gain, $A(s)$, must be *constant* at low (and even very-low) frequencies. Thus the amplifier must be 'DC coupled'. At least for inductor-enhancing circuits this is a very difficult requirement, for the inductor across the amplifier input will not allow any quiescent amplifier bias voltage, and the amplifier must have a truly differential input. This requires, in turn, that the input stage to the amplifier contain *at least two* active devices and a much more complicated bias structure.

This additional complexity can be avoided, however, by relaxing the single zero and pole requirement, and instead using lead-lag techniques and careful pole placement to construct a stable amplifier. Again, this rule relaxation was *not* allowed on the high-frequency end, because many of the roll-off characteristics there are governed by unpredictable and largely uncontrollable circuit parasitics.

6.5 An Input Current-Ripple Active Filter

As presented in the previous discussions, the ripple-filters will be '2nd order' in that they will have one 'large' passive filter element (L_f or C_f) and one 'active element'. This active element will contain two bipolar transistors and several 'small' passive components. As such, the response of the entire filter will probably not be that of a passive filter, but it will be evaluated, in terms of gain at 1 MHz, as if it were a second-order passive filter.

An input current-ripple filter is composed of a filter capacitor, C_f , and inductor-enhancing circuit. The circuit will be of type (af) and will attempt to achieve an inductor-enhancement, or gain, of around 500 at 1 MHz, or 50 at 10 MHz. The amplifier stage output will be 'class-A' and biased at roughly 10 mA so that this circuit will be 'optimized' for meeting MIL-STD-461B at 1 MHz.

6.5.1 Low-Frequency LT Consideration

The first step in designing a *real* active filter circuit is to investigate some of the appropriate bias topologies. The low-frequency LT characteristics are going to play a major part in the selection of an appropriate bias topology as discussed above.

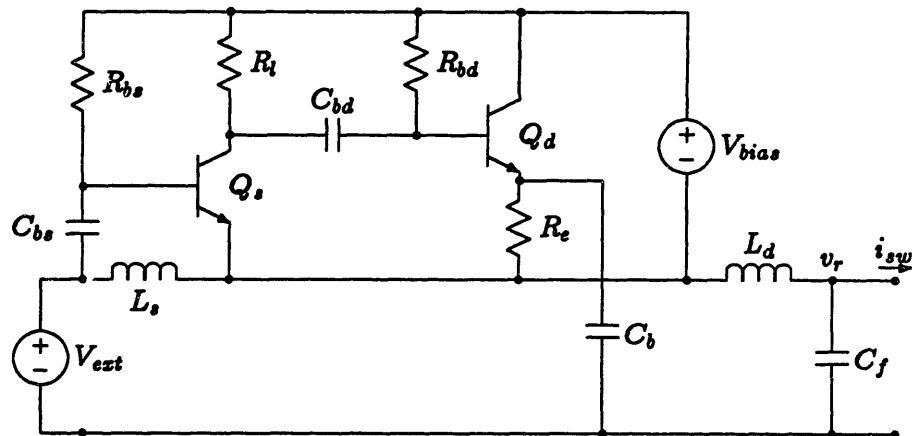


Figure 6.2: Biased Input Current-Ripple Filter

A very simply biased circuit of type (af) is shown in Fig. 6.2. Though the bias point of Q_d is regulated quite nicely by R_e , the bias point of Q_s is largely unregulated and subject to variations with temperature and individual device characteristics. Except for a small change in the gain though, bias variations of Q_s will not affect critical circuit parameters, so this simple bias circuitry may be entirely adequate.

If deemed inadequate, however, the bias point of Q_s can easily be stabilized by

moving R_{b_s} to the collector of Q_s instead of V_{bias} , and adding an additional resistor across C_{b_s} . Notice that stabilizing the bias point with an emitter degeneration resistor and capacitor would add another pole and zero to the low-frequency LT. This is potentially troublesome and is therefore avoided.

With two inductors and three capacitors, a manual analysis of the fifth-order LT of this circuit is rather cumbersome. Here, general purpose circuit simulators like SPICE can be used to great advantage. A linearized incremental circuit for the LT of the above is shown in Fig. 6.3. In this circuit, the parallel combination of C_f and the power-circuit has been assumed to be an incremental short. Thus both inductors appear in parallel and are collectively referred to as L_p .

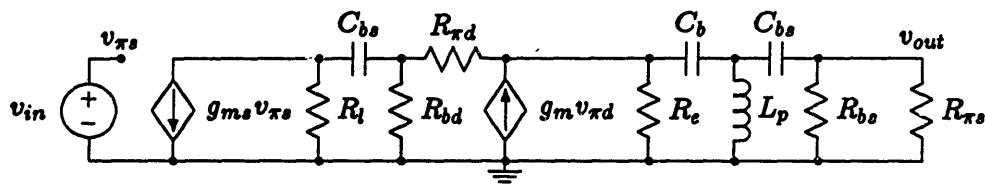


Figure 6.3: Small-Signal Loop Transmission Circuit

Assume, for now, the following nominal component values are used for 1 MHz operation:

$$\begin{aligned} C_{b_s} &= 0.01 \mu\text{F} & C_e &= 0.1 \mu\text{F} \\ C_{b_d} &= 0.02 \mu\text{F} & L_p &= 12.5 \mu\text{F} \\ R_l &= 100 \Omega & R_e &= 390 \Omega \end{aligned}$$

and the parameters of good RF-bipolar transistors, as discussed in Chapter 5 are:

$$\beta = 50 \quad g_m = 0.4 \text{ U} \quad R_\pi = 150 \Omega$$

The SPICE output for this circuit in Appendix A.1 shows us that with these component values, the circuit will be low-frequency unstable because the magnitude of the LT is well above unity when the angle of the LT crosses 180° . If we increase C_{b_s} to $10 \mu\text{F}$ and re-run SPICE, however, the magnitude is very close to unity when the angle crosses 180° as shown in Appendix A.2. This says that with $C_{b_s} = 10 \mu\text{F}$, this circuit will probably be stable, but it is still too close to call.

Now let the inductors have a small amount of parasitic resistance. If we assume a copper resistance in each inductor of 0.1Ω , a third SPICE run verifies that this circuit will be quite stable indeed. Appendix A.3 shows that as the angle of the LT passes through 180° , the $|LT|$ is below $1/1000$.

This parasitic resistance of the inductors is in line with what could be expected in real inductors. Hence, this is deemed an appropriate bias topology. This biasing method could be further complicated, though, by adding an emitter degeneration resistor and

bypass capacitor to Q_d , to stabilize the bias point. This would add yet another low-frequency pole-zero pair and for the purposes of our proto-typical circuit, would only unnecessarily complicate the low-frequency stability issues.

6.5.2 Gain and High-Frequency LT Calculations

As the circuit is now quite complex and we desire, for the first time, fairly accurate predictions of gain and LT parameters, SPICE will continue to be the dominant analysis tool.

After choosing R_{b_s} and R_{b_d} so that both transistors are biased at roughly 10 mA, and choosing SPICE's Gummel-Poon bipolar model parameters² so that they give appropriate hybrid- π parameters, a SPICE run on the circuit of Fig. 6.2 indicates that with the component values mentioned earlier, the gain is only about 250. This is not high enough and must be improved.

It is quickly found that the values of C_b and R_e do not affect the gain too much. The gain does depend on R_i , but only up to a certain point. Also, the gain does depend on β_d but not too much on $C_{\pi d}$. It seems then, that raising R_i and selecting Q_d for high β rather than for low C_{π} is in order. With this in mind a SPICE run with:

$$R_i = 470\Omega \quad \beta_d = 50 \quad g_{md} = 0.4\text{U} \quad R_{\pi d} = 310\Omega$$

yields a gain of over 500 which is deemed acceptable.

Now comes that challenge of reasonably compensating the circuit without destroying the gain. A capacitor across R_i is an appropriate way to compensate this circuit. By trial and error with SPICE, it is found that $C_{comp} \approx 500 \text{ pF}$ will roll-off the LT to a UGC of about 35 MHz while still leaving the gain at around 500. A SPICE run of this circuit is given in Appendix A.4.

As such it seems that we have a circuit which has reasonable LT characteristics at both high and low frequencies and achieves a gain on the order of 500 at 1 MHz.

6.5.3 The Real Circuit

A complete schematic of the implemented circuit is shown in Fig. 6.4. Component values are given in Table 6.1. A photograph of the circuit, without C_f , is shown in Fig. 6.5. Notice that Q_d is a PNP 2N3906 instead of an NPN as considered previously. The change does not affect the preceding analysis at all.

²See [7], section 1.4 for a discussion of the Gummel-Poon Bipolar Transistor Model

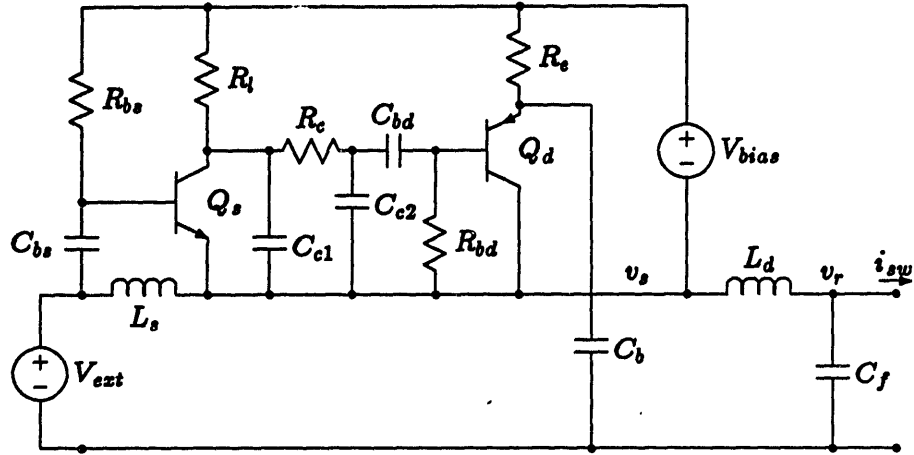


Figure 6.4: Complete Input Current-Ripple Active Filter

$C_f = 0.3 \mu\text{F}$	$L_s = 25 \mu\text{H}$	$L_d = 25 \mu\text{H}$
$C_{bs} = 10 \mu\text{F}$	$C_{be} = 0.02 \mu\text{F}$	$C_b = 0.1 \mu\text{F}$
$C_{c1} = 470 \text{ pF}$	$C_{c2} = 330 \text{ pF}$	
$R_{bs} = 100 \text{ K}\Omega$	$R_{bd} = 68 \text{ K}\Omega$	$R_l = 470 \Omega$
$R_e = 390 \Omega$	$R_c = 27 \Omega$	$V_{bias} = 15 \text{ V}$

Table 6.1: Component Values for Current-Ripple Filter

Bias Point

With these component values, both transistors are biased at $I_c \approx 10 \text{ mA}$. At this bias point the transistors can be roughly characterized as:

$$\begin{aligned}
 Q_s \text{ BFR-90 } \beta \approx 50 \quad & g_m = 0.4 \text{ U} \\
 & R_\pi = 125 \Omega \\
 & C_\pi = 25 \text{ pF} \\
 & C_\mu = 1 \text{ pF} \\
 \\
 Q_d \text{ 2N3906 } \beta \approx 125 \quad & g_m = 0.4 \text{ U} \\
 & R_\pi = 310 \Omega \\
 & C_\pi = 100 \text{ pF} \\
 & C_\mu = 4 \text{ pF}
 \end{aligned} \tag{6.5}$$

The total current drawn from V_{bias} is about 20 mA. With $V_{bias} = 15 \text{ V}$, the quiescent power dissipation is an acceptable 0.3 W.

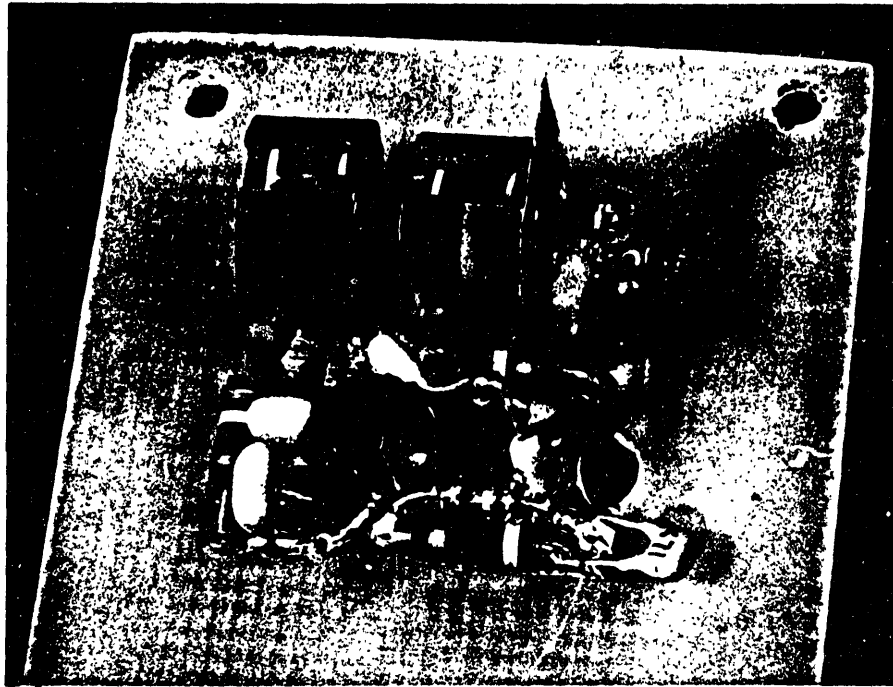


Figure 6.5: Photograph of the Current-Ripple Filter Circuit

The Inductors

The inductors are the weak part of the design for they are under-designed by about a factor of two. Both inductors consist of 25 turns of 26 AWG solid magnet wire on a Ferroxcube 905PA40-4C4 pot core. This core material was chosen for its good high-frequency characteristics and widespread availability. At full input current of 5 A the core flux density in the core is 4700 Gauss which is somewhat beyond saturation.

The mean length of a single turn is 0.75 in, so the length of wire in each inductor is roughly 19 in. This translates to a copper resistance 0.06Ω and a DC power dissipation of 1.5 W at rated current. At this current level, the inductors will have to be fan cooled, as will the rest of the power circuit.

If this circuit were to be re-built, these inductors should be constructed on the next larger size core to reduce both the flux density and the conduction losses. At present, they are only really acceptable if the converter is used at half rated input current or less. Notice, by the way, that this conduction loss is several times greater than the quiescent power dissipation of the entire active circuit. Even with a larger core, this conduction loss will dominate the power dissipation of the circuit.

More on Compensation

The amplifier was initially built with only the dominant LT roll-off pole formed by C_{e1} and R_l as discussed above. With these components, the UGC was observed to be about 30 MHz with plenty ($> 65^\circ$) of phase margin. Still, when the feedback loop was

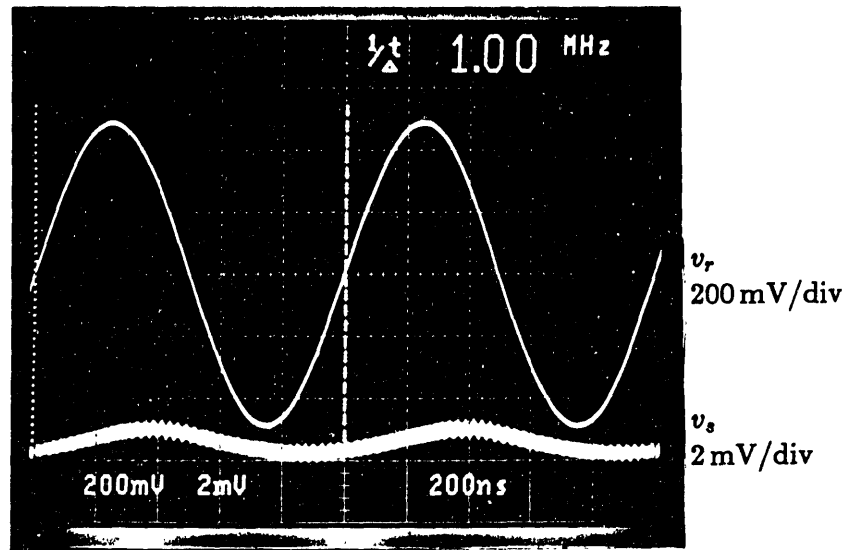


Figure 6.6: Sinusoidal Response at 1 MHz.

closed, the circuit exhibited a high-frequency instability. It was then observed that the amplifier contained a couple of zeroes in the 30–60 MHz range. These zeroes, due to parasitics, are not predicted in the above SPICE simulations and bring the $|LT|$ back above unity at very high frequencies. To correct this, C_{c2} and R_c were added to create an additional LT roll-off pole at 25 MHz. This worked fine and stabilized the circuit.

Experimental Results

Fig. 6.6 shows the circuit in sinusoidal operation at 1 MHz. The large trace is the voltage v_r at 200 mV/div being supplied by a signal generator. It is essentially the voltage across L_d . The small trace is v_s , the resultant voltage across L_s , at 2 mV/div. The two voltages differ in magnitude by a factor of about 1250 and in phase by about 90° .

Measurement of the external-source ripple-current, i_s , would be extremely difficult. The magnitude of the current is very small, in the $20 \mu\text{A}$ range, and the circuit is constructed far too compactly to accept a current probe. A fairly accurate value can be predicted by SPICE though.

A SPICE run of the complete circuit shown in Fig. 6.4 is given in Appendix A.5. This indicates that at 1 MHz, the ratio of v_r to v_s ought to be about 1200:1. This agrees, to within 5%, to the traces in Fig. 6.6, so I feel confident that SPICE's simulation of the circuit is fairly accurate. From the same line of Appendix A.5, SPICE predicts the external-source ripple-current to be $6.1 \mu\text{A}$ for $v_r = 1 \text{ V}$ at 1 MHz. This corresponds to an effective-inductance of:

$$L_{eff} = \frac{v_r}{s i_s} = \frac{1}{6.28 \times 10^6 \times 6.1 \mu\text{A}} = 26 \text{ mH} \quad (6.6)$$

The total inductance used in the circuit is $50\mu\text{H}$, so this circuit is operating at an inductor-enhancement, or gain, of

$$\text{gain} = \frac{L_{eff}}{L_s + L_d} \approx 520 \quad (6.7)$$

Signal Handling Capability:

As the magnitude of v_r is increased, more current flows through L_d and therefore through Q_d . When the peaks of this current become equal the bias current of Q_d , Q_d will momentarily saturate and the circuit will lose regulation of i_s . This will result in excessive noise being conducted back to the external source V_{ext} . To prevent this, the magnitude of v_r must be kept sufficiently small.

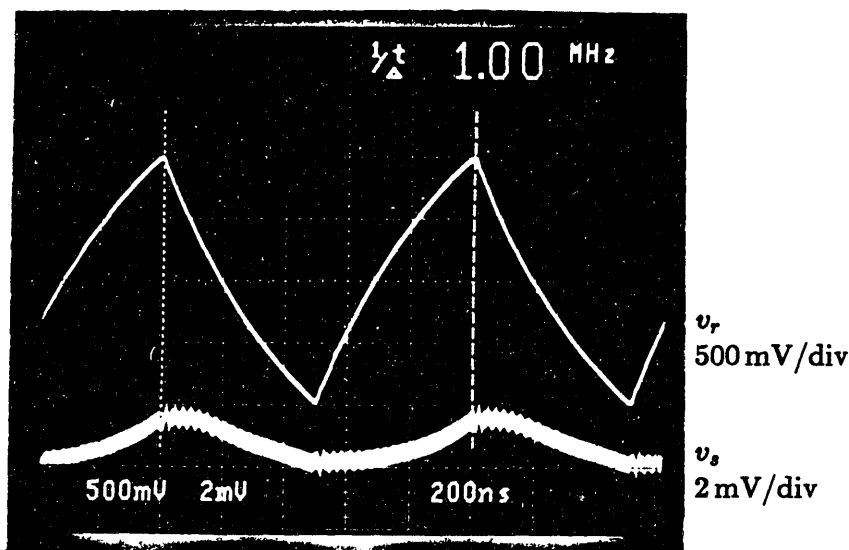


Figure 6.7: Operation with 'Normal' v_r

For a given converter, switching frequency, and filter capacitor C_f , v_r will be essentially triangular, with amplitude inversely proportional to the size of C_f . Circuit operation with an imposed 1 MHz 'triangular' v_r is shown in Fig. 6.7. The amplitude of v_r was adjusted to be somewhat below that which caused the amplifier to become non-linear. This 2 V p-p is considered a practical value for v_r and leaves some overhead for momentary converter overloads or transients.

Compared to v_r , v_s is negligible and we can easily calculate the magnitude of the quadratic current through L_d . Using:

$$|i_{L_d p}| = \frac{K}{L_d} \frac{t^2}{2} \Big|_0^T \quad (6.8)$$

where

$$\begin{aligned}K &= 1/250 \times 10^{-9} \text{ V/sec} \\L_d &= 25 \mu\text{H} \\T &= 250 \times 10^{-9} \text{ sec}\end{aligned}$$

yields

$$|i_{L_d}| = 5 \text{ mA} \quad (6.9)$$

which is roughly half of the bias current in Q_d .

Note also from Fig. 6.7 that the smaller waveform is similar to that in Fig. 6.6. This indicates that i_s is on the order of the $6.1 \mu\text{A}$ that SPICE had predicted for the earlier sinusoidal case and is well below the $25 \mu\text{A}$ specification in MIL-STD-461B. Thus, at 1 MHz, this circuit is limited by its output stage bias-current and not by the MIL-STD noise specification.

Assuming that the converter is operating at its full output-current of 7 A, and 50% duty cycle as shown, C_f will be charging and discharging at 3.5 A. To stay within the 2 V p-p value for v_r :

$$C_f \geq \frac{\Delta T}{v_{r\text{-p-p}}} I_{\text{charge}} = \frac{0.5 \mu\text{sec}}{2 \text{ V}} 3.5 \text{ A} \approx 0.88 \mu\text{F} \quad (6.10)$$

At 1 MHz the required value for C_f could be reduced, of course, by either biasing this circuit more heavily, or moving to a push-pull output stage in the amplifier. Staying at the same gain of 520, C_f could be reduced by roughly a factor of four in this manner before the MIL-STD would become the limitation at 1 MHz.

C_f could also be reduced by moving to yet higher converter switching frequencies. The required value for C_f goes down linearly with frequency, and with this circuit the MIL-STD would be met for all switching frequencies within reason.

Impedance Seen by the Converter

It is very important to realize that, looking back into this active circuit from C_f , the impedance seen is not that of the 26 mH L_{eff} derived above. Because v_s is very small, the impedance seen by the converter is essentially only that of L_d . The converter, therefore, sees its source as coming through a 2nd-order LC filter composed only of C_f and L_d . The converter's control circuit must, therefore, be designed with the realization that the self-resonant frequency of this filter is 35 times higher than that which would be obtained by using a true 26 mH inductor in the input filter. In reality this is no problem, for with the above component values the self-resonance is at about 34 KHz. For 1 MHz power circuits not subject to extremely stringent noise requirements, this would be considered a 'rather normal' self-resonant frequency for the circuit's input filter.

Comparison to a Fourth-Order Passive Filter

This active circuit utilizes $50 \mu\text{H}$ of high-current inductance and roughly $1 \mu\text{F}$ of high-voltage capacitance to exceed MIL-STD-461B by roughly a factor of four at 1 MHz. If

the same total inductance and capacitance were used in a fourth-order passive ripple filter, the ripple attenuation would be 240×10^3 or sufficient to beat the MIL-STD by a factor of 2. Thus, it seems at first, that all the active circuitry herein is for nought.

The fourth-order filter, though, has associated fourth-order dynamics. When used with such a filter on both its input and output, the resulting eighth-order filter dynamics would make compensation of the converter's control circuit very difficult indeed. This active filter, however, looks like a 2nd-order system. When used on both the input and output of a converter, the resulting fourth-order filter dynamics will be *much* easier to work with than the eighth-order dynamics of the passive filter.

Transient Response

As the load or supply to the switching converter changes with time, the converter's control circuit will modify the duty cycle to compensate. Response of this circuit to those changes, and response of the controller to the dynamics of this circuit must be understood in order to obtain a well designed system.

The analysis of transients in this circuit has to be divided into two different sections: that for large transients, and that for small transients.

Large Transients: In general, when this circuit is subject to a large transient, the amplifier will either saturate or cut-off. This in no way damages the amplifier, but leaves the active filter circuit looking like a series combination of the two passive inductors L_s and L_d . Thus the dynamics of the filter response during this transient are different than those during normal operation.

The saturated or cut-off transient condition will exist until the bias point of the amplifier settles again. The time required for this depends on the type, direction, magnitude, and duration of the transient. A general feeling for this time can be obtained from the low-frequency poles and zeroes of the LT expression.

For example, a voltage pulse across L_s , as caused by a load current change, will knock the bias point of Q_s . If the load current tries to increase, v_s will go momentarily negative. This will cause Q_s to saturate, and its B-E junction will start discharging C_{b_s} rather quickly. When the pulse goes away Q_s will become cut-off and will remain so until C_{b_s} is re-charged through R_{b_s} .

This is a *very slow* relaxation, with time-constant $\tau = 1/R_{b_s}C_{b_s} = 1$ sec. The number of τ this relaxation requires is dependent on how much the base of Q_s discharged C_{b_s} during the negative pulse of v_s . If the v_s pulse was relatively short, this relaxation should require well under 1τ , but even this is forever in electrical terms. There are several ways to speed up this relaxation, the simplest being to modify the values of R_{b_s} and C_{b_s} . These values determine many of the low-frequency LT characteristics though, so they should be modified with caution. Another potential method is to re-bias Q_s by tying its base directly to L_s and using an emitter degeneration resistor and capacitor to provide the input offset.

The other direction of load current change is not nearly so harmful. If the load current tries to decrease suddenly, v_s will go positive, and Q_s will be immediately cut-

off. C_{b_s} will then charge very slowly through R_{b_s} . When the transient is over and v_s falls again, Q_s will momentarily saturate as its base, rather quickly, removes the small amount of excess charge on C_{b_s} . In general, this 'polarity' transient will recover much faster than the previous transient, at least as far as Q_s is concerned. These large swings in Q_s 's collector current are wreaking havoc with the bias point of Q_d , but because C_{bd} and C_b are so much smaller than C_{b_s} , the time constants associated with Q_d 's bias are generally much faster than those of Q_s 's bias.

In general, the methods introduced above to accelerate the previous relaxation tend to slow this relaxation. It might be considered 'optimal' if the bias structure of the circuit were re-worked to make these two relaxations comparable. In this way the total 'drop-out' time might be minimized.

Other types of large transients, changes in V_{ext} for example, will have different but comparable effects on the circuit. Presenting even a qualitative discussion of them would be rather lengthy, and will be avoided here.

One very important point to be noted, is that during these transients, switching ripple-current filtration is not being accomplished and switching noise is being transmitted back to the source. In some applications, this may be unacceptable and the amplifier may have to be designed with sufficient 'headroom' to avoid clipping during any foreseeable transient.

Small Transients: Small transients are defined as those which do not cause the amplifier to become non-linear. In addition to being small, these transients could also just be slow enough that the bias point of the amplifier 'tracks' the transient and the amplifier never clips.

Though these transients may cause changes in the bias point of the amplifier, the fundamental operation of the circuit will remain the same throughout the transient. In particular, no huge burst of switching noise will be conducted back to the external source.

For most applications, it is obviously desirable to design the amplifier so that *most* transients are considered small. This requires building the amplifier with sufficient headroom. This circuit, C_f , and converter, for example, are designed with a factor of 2 (see above Signal Handling Capability section) allowance in v_r for headroom. This is probably adequate for most applications. If inadequate, however, the headroom can easily be expanded by increasing either C_f or the bias current in Q_d .

6.6 Summary

This chapter has developed an actual, working, active filter circuit for use with a given switching converter. Compared to a second-order passive filter, this active circuit achieved an inductor-enhancement, or gain, of about 520. This was sufficient to exceed the applicable ripple specification, MIL-STD-461B CE03 shown in Fig 1.1, by roughly a factor of four.

Circuit 'cost' and ripple filtration were comparable to that of a fourth-order passive

filter, but the resulting filter dynamics were only 2nd-order instead of fourth-order. This factor alone makes these active filter circuits very valuable, for it greatly simplifies compensation of the converter's control circuit.

Chapter 7

Conclusions

This thesis has presented the foundations for the design of active filters for power circuits. It has developed much of the background theory and relevant criteria, described and compared different filter topologies, compared the different active devices, and finally designed and constructed an actual, working, active filter circuit. This work should enable future researchers or circuit designers to quickly achieve useful, cost and space-efficient, practical, ripple filters for high frequency power circuits.

Inevitably, power circuits will soon be operating at frequencies well in excess of 1 MHz. Though this work was centered around 1 MHz, many of the circuits and conclusions developed herein are applicable at much higher frequencies. In particular, many of these circuits are limited, not in the gain they can achieve at 1 MHz, but in their allowable power dissipation. As these active filters are applied to power circuits working at yet higher frequencies, the power dissipation will decrease proportionately and the circuits will be able to fully utilize their potential gain.

7.1 Future Work

Though this thesis has laid the groundwork, there are still several open topics in this field. The foremost of these is the increase in performance, or decrease in cost, to be obtained by integrating these filter circuits. In this way, much of the active circuitry could be made extremely inexpensive, small, and fast.

At the time of this writing, these filter circuits have not been used *with* an actual power circuit. Though first-order theory predicts no complications when used with power circuits, this has yet to be experimentally verified.

The working circuits in this thesis were designed for their simplicity and ease of construction and analysis. Their intent was only to show feasibility of the concept and applicability of the theory. They were not designed to be suitable for immediate industrial application. Before these circuits are ready for industry, several practical issues have yet to be explored. Among these are: Protection of the active circuitry from line transients, and allocation of sufficient amplifier overhead to avoid clipping during reasonable transients.

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Appendix A

SPICE Runs

A.1 First SPICE Run

```
*****12-DEC-86 ***** SPICE 2G.5 (10AUG81) *****16:34:47*****
```

```
SPICE RUN #1
```

```
**** INPUT LISTING TEMPERATURE = 27.000 DEG C
```

```
*****
```

```
VIN 1 0 AC 1
```

```
RDUM 1 0 1MEG
```

```
GMS 2 0 1 0 0.4
```

```
RL 2 0 100
```

```
CC 3 2 0.02U
```

```
RBD 3 0 48K
```

```
RPID 3 4 300
```

```
RE 4 0 390
```

```
GMD 0 4 3 4 0.4
```

```
CE 4 5 0.1U
```

```
CB 5 6 0.05U
```

```
LS 5 0 12.5U
```

```
RPIS 6 0 100
```

```
EINV 0 7 6 0 1
```

```
RSTUP 7 0 1MEG
```

```
.WIDTH OUT=80
```

```
.AC DEC 10 1 100MEG
```

```
.PRINT AC VM(7) VP(7)
```

.END

*****12-DEC-86 ***** SPICE 2G.5 (10AUG81) *****16:34:47*****

SPICE RUN #1

**** AC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ	VM(?)	VP(?)
1.000E+00	1.849E-16	-1.815E-01
1.259E+00	4.643E-16	-2.285E-01
1.585E+00	1.166E-15	-2.877E-01
1.995E+00	2.930E-15	-3.621E-01
2.512E+00	7.359E-15	-4.559E-01
3.162E+00	1.848E-14	-5.739E-01
3.981E+00	4.643E-14	-7.225E-01
5.012E+00	1.166E-13	-9.096E-01
6.310E+00	2.929E-13	-1.145E+00
7.943E+00	7.357E-13	-1.441E+00
1.000E+01	1.848E-12	-1.814E+00
1.259E+01	4.640E-12	-2.284E+00
1.585E+01	1.165E-11	-2.874E+00
1.995E+01	2.924E-11	-3.617E+00
2.512E+01	7.336E-11	-4.550E+00
3.162E+01	1.839E-10	-5.721E+00
3.981E+01	4.608E-10	-7.189E+00
5.012E+01	1.152E-09	-9.024E+00
6.310E+01	2.874E-09	-1.131E+01
7.943E+01	7.141E-09	-1.413E+01
1.000E+02	1.764E-08	-1.759E+01
1.259E+02	4.319E-08	-2.177E+01
1.585E+02	1.045E-07	-2.672E+01
1.995E+02	2.484E-07	-3.240E+01
2.512E+02	5.782E-07	-3.869E+01
3.162E+02	1.313E-06	-4.535E+01
3.981E+02	2.904E-06	-5.205E+01
5.012E+02	6.263E-06	-5.848E+01
6.310E+02	1.322E-05	-6.438E+01
7.943E+02	2.742E-05	-6.964E+01
1.000E+03	5.616E-05	-7.422E+01
1.259E+03	1.140E-04	-7.819E+01
1.585E+03	2.299E-04	-8.165E+01
1.995E+03	4.618E-04	-8.473E+01

2.512E+03	9.248E-04	-8.756E+01	
3.162E+03	1.848E-03	-9.027E+01	
3.981E+03	3.685E-03	-9.300E+01	
5.012E+03	7.332E-03	-9.588E+01	
6.310E+03	1.455E-02	-9.904E+01	
7.943E+03	2.878E-02	-1.026E+02	
1.000E+04	5.662E-02	-1.068E+02	
1.259E+04	1.106E-01	-1.116E+02	
1.585E+04	2.136E-01	-1.173E+02	
1.995E+04	4.071E-01	-1.237E+02	
2.512E+04	7.628E-01	-1.309E+02	
3.162E+04	1.404E+00	-1.387E+02	<== LF UGC
3.981E+04	2.545E+00	-1.470E+02	
5.012E+04	4.579E+00	-1.555E+02	
6.310E+04	8.311E+00	-1.646E+02	
7.943E+04	1.566E+01	-1.751E+02	
1.000E+05	3.217E+01	1.694E+02	
1.259E+05	7.357E+01	1.353E+02	
1.585E+05	9.336E+01	7.076E+01	
1.995E+05	6.638E+01	3.810E+01	
2.512E+05	5.293E+01	2.511E+01	
3.162E+05	4.654E+01	1.812E+01	
3.981E+05	4.316E+01	1.365E+01	
5.012E+05	4.125E+01	1.051E+01	
6.310E+05	4.012E+01	8.197E+00	
7.943E+05	3.944E+01	6.438E+00	
1.000E+06	3.902E+01	5.078E+00	<== 1 MHz
1.259E+06	3.876E+01	4.016E+00	
1.585E+06	3.860E+01	3.181E+00	
1.995E+06	3.850E+01	2.522E+00	
2.512E+06	3.843E+01	2.001E+00	
3.162E+06	3.839E+01	1.589E+00	
3.981E+06	3.837E+01	1.261E+00	
5.012E+06	3.835E+01	1.002E+00	
6.310E+06	3.834E+01	7.955E-01	
7.943E+06	3.834E+01	6.318E-01	
1.000E+07	3.833E+01	5.019E-01	
1.259E+07	3.833E+01	3.986E-01	
1.585E+07	3.833E+01	3.166E-01	
1.995E+07	3.833E+01	2.515E-01	
2.512E+07	3.833E+01	1.998E-01	
3.162E+07	3.833E+01	1.587E-01	
3.981E+07	3.833E+01	1.260E-01	
5.012E+07	3.833E+01	1.001E-01	
6.310E+07	3.833E+01	7.953E-02	
7.943E+07	3.833E+01	6.317E-02	

FREQ	VM(7)	VP(7)
1.000E+00	3.397E-14	-5.397E-01
1.259E+00	9.286E-14	-6.794E-01
1.585E+00	2.335E-13	-8.553E-01
1.995E+00	5.859E-13	-1.077E+00
2.512E+00	1.472E-12	-1.356E+00
3.162E+00	3.696E-12	-1.707E+00
3.981E+00	9.283E-12	-2.148E+00
5.012E+00	2.331E-11	-2.704E+00
6.310E+00	5.854E-11	-3.404E+00
7.943E+00	1.470E-10	-4.284E+00
1.000E+01	3.688E-10	-5.392E+00
1.259E+01	9.250E-10	-6.784E+00
1.585E+01	2.318E-09	-8.533E+00
1.995E+01	5.803E-09	-1.073E+01
2.512E+01	1.449E-08	-1.347E+01
3.162E+01	3.608E-08	-1.690E+01
3.981E+01	8.940E-08	-2.116E+01
5.012E+01	2.198E-07	-2.641E+01
6.310E+01	5.344E-07	-3.282E+01
7.943E+01	1.278E-06	-4.051E+01
1.000E+02	2.987E-06	-4.956E+01
1.259E+02	6.775E-06	-5.989E+01
1.585E+02	1.480E-05	-7.132E+01
1.995E+02	3.098E-05	-8.347E+01
2.512E+02	6.190E-05	-9.589E+01
3.162E+02	1.181E-04	-1.081E+02
3.981E+02	2.156E-04	-1.196E+02
5.012E+02	3.792E-04	-1.300E+02
6.310E+02	6.468E-04	-1.391E+02
7.943E+02	1.078E-03	-1.469E+02
1.000E+03	1.767E-03	-1.534E+02
1.259E+03	2.862E-03	-1.588E+02
1.585E+03	4.601E-03	-1.631E+02
1.995E+03	7.359E-03	-1.667E+02
2.512E+03	1.173E-02	-1.695E+02
3.162E+03	1.866E-02	-1.719E+02
3.981E+03	2.966E-02	-1.738E+02
5.012E+03	4.710E-02	-1.753E+02
6.310E+03	7.476E-02	-1.767E+02
7.943E+03	1.187E-01	-1.778E+02
1.000E+04	1.885E-01	-1.789E+02
1.259E+04	2.996E-01	-1.798E+02
1.585E+04	4.769E-01	1.792E+02
1.995E+04	7.610E-01	1.782E+02

<== LF Angle Crossover

2.512E+04	1.219E+00	1.770E+02	<== LF UGC
3.162E+04	1.966E+00	1.756E+02	
3.981E+04	3.203E+00	1.739E+02	
5.012E+04	5.312E+00	1.716E+02	
6.310E+04	9.075E+00	1.682E+02	
7.943E+04	1.634E+01	1.627E+02	
1.000E+05	3.236E+01	1.518E+02	
1.259E+05	7.193E+01	1.229E+02	
1.585E+05	9.526E+01	6.242E+01	
1.995E+05	6.803E+01	3.027E+01	
2.512E+05	5.377E+01	1.848E+01	
3.162E+05	4.699E+01	1.273E+01	
3.981E+05	4.342E+01	9.311E+00	
5.012E+05	4.141E+01	7.042E+00	
6.310E+05	4.022E+01	5.429E+00	
7.943E+05	3.950E+01	4.234E+00	
1.000E+06	3.906E+01	3.325E+00	<== 1 MHz
1.259E+06	3.879E+01	2.622E+00	
1.585E+06	3.861E+01	2.073E+00	
1.995E+06	3.851E+01	1.642E+00	
2.512E+06	3.844E+01	1.302E+00	
3.162E+06	3.840E+01	1.033E+00	
3.981E+06	3.837E+01	8.201E-01	
5.012E+06	3.835E+01	6.511E-01	
6.310E+06	3.834E+01	5.171E-01	
7.943E+06	3.834E+01	4.106E-01	
1.000E+07	3.833E+01	3.261E-01	
1.259E+07	3.833E+01	2.590E-01	
1.585E+07	3.833E+01	2.058E-01	
1.995E+07	3.833E+01	1.634E-01	
2.512E+07	3.833E+01	1.298E-01	
3.162E+07	3.833E+01	1.031E-01	
3.981E+07	3.833E+01	8.191E-02	
5.012E+07	3.833E+01	6.506E-02	
6.310E+07	3.833E+01	5.168E-02	
7.943E+07	3.833E+01	4.105E-02	
1.000E+08	3.833E+01	3.261E-02	

A.3 Third SPICE Run

*****12-DEC-86 ***** SPICE 2G.5 (10AUG81) *****16:23:42*****

SPICE RUN #3

**** INPUT LISTING

TEMPERATURE = 27.000 DEG C

VIN 1 0 AC 1

RDUM 1 0 1MEG

GMS 2 0 1 0 0.4

RL 2 0 100

CC 3 2 0.02U

RBD 3 0 48K

RPID 3 4 300

RE 4 0 390

GMD 0 4 3 4 0.4

CE 4 5 0.1U

CB 5 6 10U

LS 5 8 12.5U

RS 8 0 0.05

RPIS 6 0 100

EINV 0 7 6 0 1

RSTUP 7 0 1MEG

.WIDTH OUT=80

.AC DEC 10 1 100MEG

.PRINT AC VM(7) VP(7)

.END

SPICE RUN #3

**** AC ANALYSIS

TEMPERATURE = 27.000 DEG C

FREQ	VM(7)	VP(7)
1.000E+00	2.354E-11	-9.045E+01
1.259E+00	4.696E-11	-9.057E+01
1.585E+00	9.369E-11	-9.071E+01
1.995E+00	1.869E-10	-9.090E+01
2.512E+00	3.730E-10	-9.113E+01
3.162E+00	7.441E-10	-9.142E+01
3.981E+00	1.484E-09	-9.179E+01

5.012E+00	2.961E-09	-9.225E+01
6.310E+00	5.906E-09	-9.284E+01
7.943E+00	1.178E-08	-9.357E+01
1.000E+01	2.348E-08	-9.449E+01
1.259E+01	4.679E-08	-9.565E+01
1.585E+01	9.315E-08	-9.711E+01
1.995E+01	1.852E-07	-9.893E+01
2.512E+01	3.676E-07	-1.012E+02
3.162E+01	7.273E-07	-1.041E+02
3.981E+01	1.432E-06	-1.076E+02
5.012E+01	2.800E-06	-1.119E+02
6.310E+01	5.418E-06	-1.172E+02
7.943E+01	1.032E-05	-1.234E+02
1.000E+02	1.925E-05	-1.306E+02
1.259E+02	3.492E-05	-1.387E+02
1.585E+02	6.126E-05	-1.474E+02
1.995E+02	1.036E-04	-1.561E+02
2.512E+02	1.686E-04	-1.644E+02
3.162E+02	2.653E-04	-1.717E+02
3.981E+02	4.065E-04	-1.776E+02
5.012E+02	6.127E-04	1.782E+02
6.310E+02	9.183E-04	1.756E+02
7.943E+02	1.381E-03	1.744E+02
1.000E+03	2.093E-03	1.741E+02
1.259E+03	3.205E-03	1.744E+02
1.585E+03	4.956E-03	1.750E+02
1.995E+03	7.720E-03	1.756E+02
2.512E+03	1.210E-02	1.762E+02
3.162E+03	1.903E-02	1.768E+02
3.981E+03	3.002E-02	1.771E+02
5.012E+03	4.745E-02	1.774E+02
6.310E+03	7.510E-02	1.776E+02
7.943E+03	1.190E-01	1.776E+02
1.000E+04	1.888E-01	1.775E+02
1.259E+04	2.998E-01	1.773E+02
1.585E+04	4.770E-01	1.769E+02
1.995E+04	7.610E-01	1.763E+02
2.512E+04	1.219E+00	1.755E+02
3.162E+04	1.965E+00	1.744E+02
3.981E+04	3.201E+00	1.729E+02
5.012E+04	5.308E+00	1.707E+02
6.310E+04	9.065E+00	1.675E+02
7.943E+04	1.631E+01	1.621E+02
1.000E+05	3.225E+01	1.512E+02
1.259E+05	7.132E+01	1.224E+02
1.585E+05	9.446E+01	6.251E+01

<== LF Angle Crossover

<== LF UGC

1.995E+05	6.786E+01	3.038E+01	
2.512E+05	5.372E+01	1.853E+01	
3.162E+05	4.697E+01	1.275E+01	
3.981E+05	4.341E+01	9.322E+00	
5.012E+05	4.140E+01	7.048E+00	
6.310E+05	4.022E+01	5.432E+00	
7.943E+05	3.950E+01	4.235E+00	
1.000E+06	3.906E+01	3.325E+00	<== 1 MHz
1.259E+06	3.879E+01	2.622E+00	
1.585E+06	3.861E+01	2.073E+00	
1.995E+06	3.851E+01	1.642E+00	
2.512E+06	3.844E+01	1.302E+00	
3.162E+06	3.840E+01	1.033E+00	
3.981E+06	3.837E+01	8.201E-01	
5.012E+06	3.835E+01	6.511E-01	
6.310E+06	3.834E+01	5.171E-01	
7.943E+06	3.834E+01	4.106E-01	
1.000E+07	3.833E+01	3.261E-01	
1.259E+07	3.833E+01	2.590E-01	
1.585E+07	3.833E+01	2.058E-01	
1.995E+07	3.833E+01	1.634E-01	
2.512E+07	3.833E+01	1.298E-01	
3.162E+07	3.833E+01	1.031E-01	
3.981E+07	3.833E+01	8.191E-02	
5.012E+07	3.833E+01	6.506E-02	
6.310E+07	3.833E+01	5.168E-02	
7.943E+07	3.833E+01	4.105E-02	
1.000E+08	3.833E+01	3.261E-02	

A.4 Fourth SPICE Run

*****14-DEC-86 ***** SPICE 2G.5 (10AUG81) *****10:40:02*****

INDUCTOR-ENHANCING ACTIVE FILTER CIRCUIT. RUN 4

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

```
.MODEL MODN2 NPN BF=125 CJE=2P VJE=0.75 MJE=0.33 TF=0.25N CJC=2P
+ VJC=0.5 MJC=0.5 RE=2 RB=25
.MODEL MODN NPN BF=50 CJE=2P VJE=0.75 MJE=0.33 TF=0.09N CJC=2P
+ VJC=0.5 MJC=0.5 RE=2 RB=15
```

* BIAS SUPPLY FOR CIRCUIT

VCC 1 0 15V
VEXT 4 8 0
VR 8 10 AC 1
RBS 1 2 70K
RBD 1 5 130K
RL 1 3 470
RE 6 0 390

* VARIOUS CAPACITORS

CBD 3 5 0.02U
CBS 2 4 10U
CB 6 8 0.1U
CCOMP 3 1 500P

* INDUCTORS AND THEIR PARASITIC RESISTANCES

LS 4 7 25U
RLS 7 0 0.1
LD 0 9 25U
RLD 9 10 0.1

* THE TRANSISTORS

Q2 1 5 6 MODN2
Q1 3 2 0 MODN

* COMMANDS FOR SPICE

.WIDTH OUT=80
.OPTION LIMPTS=1001
.AC DEC 5 1K 100MEG
.PRINT AC IM(VR) IM(VEXT) VM(4)
.END

*****14-DEC-86 ***** SPICE 2G.5 (10AUG81) *****10:40:02*****

INDUCTOR-ENHANCING ACTIVE FILTER CIRCUIT. RUN 4

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

	Q2	Q1
MODEL	MODN2	MODN
IB	7.90E-05	2.02E-04
IC	9.87E-03	1.01E-02

```

VBE      0.855      0.858
VBC      -10.265    -9.395
VCE      11.120     10.252
BETADC   125.000    50.000
GM       3.82E-01   3.91E-01
RPI      3.28E+02   1.28E+02
RX       2.50E+01   1.50E+01
RO       1.00E+12   1.00E+12
CPI      9.89E-11   3.87E-11
CMU      4.31E-13   4.50E-13
CBX      0.00E+00   0.00E+00
CCS      0.00E+00   0.00E+00
BETAAC   125.000    50.000
FT       6.11E+08   1.59E+09

```

*****14-DEC-86 ***** SPICE 2G.5 (10AUG81) *****10:40:02*****

INDUCTOR-ENHANCING ACTIVE FILTER CIRCUIT. RUN 4

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

FREQ	IM(VR)	IM(VEXT)	VM(4)	
1.000E+03	2.672E+00	2.699E+00	5.024E-01	
1.585E+03	1.842E+00	1.886E+00	5.059E-01	
2.512E+03	1.192E+00	1.265E+00	5.147E-01	
3.981E+03	7.290E-01	8.505E-01	5.384E-01	
6.310E+03	3.935E-01	6.111E-01	6.085E-01	
1.000E+04	8.234E-02	5.725E-01	9.007E-01	
1.585E+04	1.361E+00	1.075E+00	2.678E+00	
2.512E+04	3.204E-01	6.912E-02	2.727E-01	
3.981E+04	1.727E-01	1.336E-02	8.350E-02	
6.310E+04	1.038E-01	3.174E-03	3.143E-02	
1.000E+05	6.434E-02	8.366E-04	1.312E-02	
1.585E+05	4.032E-02	2.446E-04	6.062E-03	
2.512E+05	2.538E-02	8.067E-05	3.149E-03	
3.981E+05	1.599E-02	3.005E-05	1.829E-03	
6.310E+05	1.009E-02	1.263E-05	1.171E-03	
1.000E+06	6.364E-03	6.180E-06	8.287E-04	<== 1 MHz
1.585E+06	4.015E-03	3.698E-06	6.556E-04	
2.512E+06	2.533E-03	2.733E-06	5.745E-04	
3.981E+06	1.598E-03	2.361E-06	5.390E-04	
6.310E+06	1.008E-03	2.233E-06	5.239E-04	
1.000E+07	6.363E-04	2.229E-06	5.167E-04	

1.585E+07	4.015E-04	2.337E-06	5.113E-04
2.512E+07	2.533E-04	2.619E-06	5.031E-04
3.981E+07	1.598E-04	3.186E-06	4.873E-04
6.310E+07	1.009E-04	4.150E-06	4.597E-04
1.000E+08	6.364E-05	5.596E-06	4.228E-04

A.5 Full SPICE Run

*****14-DEC-86 ***** SPICE 2G.5 (10AUG81) *****07:32:05*****

INDUCTOR-ENHANCING ACTIVE FILTER CIRCUIT. THE REAL THING.

**** INPUT LISTING TEMPERATURE = 27.000 DEG C

.MODEL MODP PNP BF=280 CJE=2P VJE=0.75 MJE=0.33 TF=0.25N CJC=2P
+ VJC=0.5 MJC=0.5 RE=2 RB=10
.MODEL MODN NPN BF=53 CJE=2P VJE=0.75 MJE=0.33 TF=0.09N CJC=2P
+ VJC=0.5 MJC=0.5 RE=2 RB=10

* . BIAS SUPPLY FOR CIRCUIT

VCC 1 0 15V
VEXT 4 8 0
VR 8 10 AC 1
RBS 1 2 68K
RBD 6 0 270K
RL 1 3 470
RE 7 1 390
RC 3 5 27

* VARIOUS CAPACITORS

CBD 5 6 0.02U
CBS 2 4 10U
CB 7 8 0.1U
CC1 3 0 430P
CC2 5 0 310F
CPROB 0 4 30P

* INDUCTORS AND THEIR PARASITIC RESISTANCES

LS 4 11 25U
RLS 11 0 0.05
LD 0 9 25U
RLD 9 10 0.05

* THE TRANSISTORS

```

Q2 0 6 7 MODP
Q1 3 2 0 MODN
* COMMANDS FOR SPICE
.WIDTH OUT=80
.OPTION LIMPTS=1001
.AC DEC 5 1K 100MEG
.PRINT AC IM(VR) IM(VEXT) VM(4)
.END

```

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**** BIPOLAR JUNCTION TRANSISTORS

	Q2	Q1
MODEL	MODP	MODN
IB	-3.73E-05	2.08E-04
IC	-1.04E-02	1.10E-02
VBE	-0.856	0.861
VBC	10.060	-8.960
VCE	-10.917	9.820
BETADC	280.000	53.000
GM	4.03E-01	4.26E-01
RPI	6.94E+02	1.24E+02
RX	1.00E+01	1.00E+01
RO	1.00E+12	1.00E+12
CPI	1.04E-10	4.19E-11
CMU	4.35E-13	4.60E-13
CBX	0.00E+00	0.00E+00
CCS	0.00E+00	0.00E+00
BETAAC	280.000	53.000
FT	6.13E+08	1.60E+09

**** AC ANALYSIS TEMPERATURE = 27.000 DEG C

FREQ	IM(VR)	IM(VEXT)	VM(4)
1.000E+03	3.018E+00	3.049E+00	5.025E-01
1.585E+03	1.944E+00	1.994E+00	5.063E-01
2.512E+03	1.217E+00	1.298E+00	5.161E-01
3.981E+03	7.293E-01	8.649E-01	5.425E-01
6.310E+03	3.809E-01	6.271E-01	6.222E-01

1.000E+04	5.166E-02	6.253E-01	9.826E-01
1.585E+04	1.113E+00	7.475E-01	1.861E+00
2.512E+04	3.119E-01	5.983E-02	2.360E-01
3.981E+04	1.713E-01	1.187E-02	7.422E-02
6.310E+04	1.035E-01	2.817E-03	2.790E-02
1.000E+05	6.427E-02	7.295E-04	1.144E-02
1.585E+05	4.030E-02	2.069E-04	5.133E-03
2.512E+05	2.537E-02	6.649E-05	2.601E-03
3.981E+05	1.599E-02	2.499E-05	1.528E-03
6.310E+05	1.009E-02	1.120E-05	1.047E-03
1.000E+06	6.363E-03	6.083E-06	8.287E-04
1.585E+06	4.014E-03	4.023E-06	7.336E-04
2.512E+06	2.533E-03	3.188E-06	6.957E-04
3.981E+06	1.598E-03	2.930E-06	6.859E-04
6.310E+06	1.008E-03	3.060E-06	6.963E-04
1.000E+07	6.362E-04	3.696E-06	7.374E-04
1.585E+07	4.013E-04	5.447E-06	8.519E-04
2.512E+07	2.531E-04	1.046E-05	1.164E-03
3.981E+07	1.597E-04	1.969E-05	1.469E-03
6.310E+07	1.009E-04	1.584E-05	7.676E-04
1.000E+08	6.366E-05	1.299E-05	4.039E-04

<== 1 MHz