

# A High-Speed, Folding, Analog-to-Digital Converter

by

Paul Louis Mangione

Submitted to the Department of Electrical Engineering and Computer Science  
in partial fulfillment of the requirements for the degrees of

Bachelor of Science

and

Master of Science

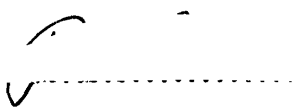
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
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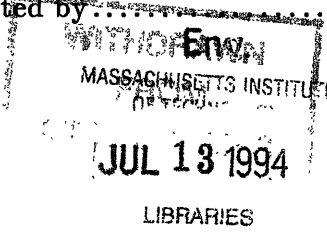
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## **Abstract**

The standard architecture for a high speed analog-to-digital converter(ADC) is the flash architecture which requires  $2^n - 1$  comparators for an  $n$ -bit digital output. The flash architecture is therefore very costly in terms of power dissipation and die area. However, by providing some clever analog preprocessing to a flash converter, the number of comparators can be significantly reduced.

“Folding” is one such analog preprocessing technique consisting of folding amplifiers and interpolation circuits. The technique allows every comparator of the ADC to be reused several times over the full scale input range. This is an improvement over the flash ADC where each comparator is used only once over the full scale input range. Because of this reuse, the number of comparators of a folding ADC will be less than that of a flash ADC with equal resolution.

The application of the folding technique resulted in the design of a high speed, 6-bit folding ADC which required only 19 comparators. The overall power dissipation of the folding ADC is about half that of a flash ADC. The folding ADC architecture also allowed the die area of the converter to be reduced. The converter was designed, simulated and laid out in a  $0.5\mu m$  BiCMOS technology. Simulation results show that the converter operates at clock frequencies up to  $180 MHz$ .

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# Chapter 1

## Introduction

### 1.1 Data Acquisition Systems

Data acquisition and conversion systems interface between the real world of physical entities, which are analog and the discrete world of digital computation. Modern trends are towards the processing of signals partially in the analog domain and partially in the digital domain with the boundary between the analog and the digital sections placed in the most appropriate position in the processing chain. This location is dependent on the complexity of the processing functions and the features of the processing technology. The devices which perform the interfacing function between these analog and digital domains are analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). They are collectively known as data converters.

Data converters are prevalent in all types of integrated systems including video signal processing systems, sampled data control systems and pulse code modulated communication systems. One important application of data converters is reading from physical recording media such as magnetic disks and tapes. Such an application was the motivation for this research. An ADC was needed to aid in the conversion of an analog signal produced by the read head of a hard disk drive.

A modern data reading system is detailed in Fig. 1-1. It uses a method called partial response/maximum likelihood (PRML) detection [1]. PRML detection is an improvement over the established peak detection method which differentiates the analog waveform produced by the disk head and checks for zero crossings. The system makes use of a digital filter and Viterbi decoder to achieve a high data transfer rate. A Viterbi decoder is a finite state machine that monitors data

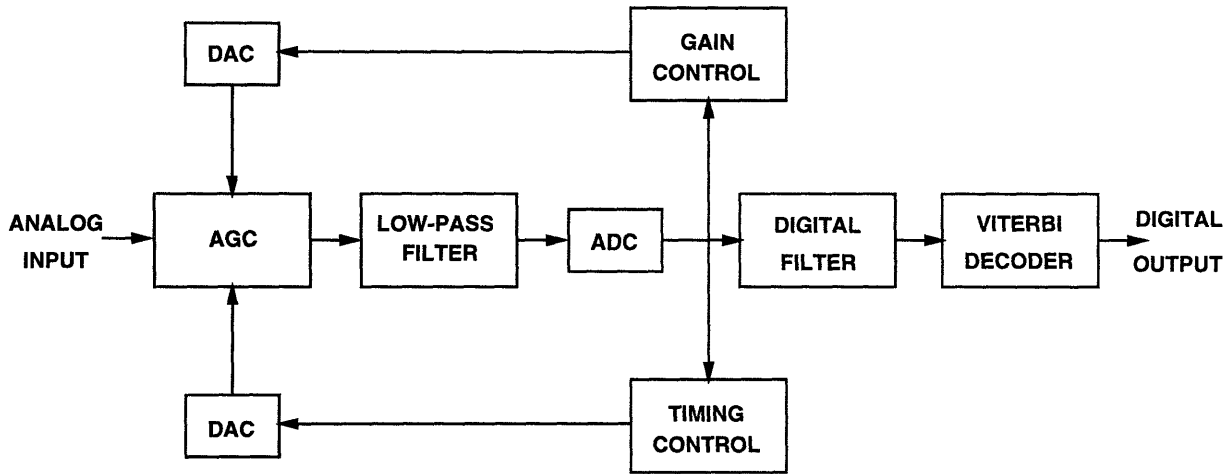


Figure 1-1: A Typical Partial Response/Maximum Likelihood System

transitions and uses that history to predict and correct current transitions. The system also makes use of active feedback to improve the input signal to the ADC. The primary role of the ADC is to provide the digital filter with a multi-bit resolution, (typically 6-bit) digitized sample of the analog input waveform at the Nyquist rate. The digital filter and Viterbi decoder process this sample and compare it with previous samples to determine what the sample represents. It is important to realize that even though the ADC provides a 6-bit sample, only 1-bit of information is made available per sample at the output of the PRML system. The ADC provides increased accuracy and flexibility in the system, so that it is easier to determine the correct data. This advantage allows the system to read disks with higher areal bit densities.

Currently, data rates as high as  $100Mb/s$  are available. For this thesis, a target data rate of  $180Mb/s$  has been selected for future applications. This rate is equivalent to the transmission of an 8-bit word or byte and 1 parity bit every  $50ns$ . Thus, for every byte of information acquired, 9 bits have to be read from the disk. The effective data transfer rate is  $180Mb/s \frac{1byte}{9bits} = 20Mbyte/s$ . To provide this high data transfer rate, the ADC must be designed with adequate bandwidth. Determining this bandwidth is illustrated in Fig. 1-2. The analog input signal is shown at the top of the diagram and the effective digital output is at the bottom. A bit can be detected at every zero-crossing. Assuming the data transfer rate was at its maximum,  $180Mb/s$ , and the digital

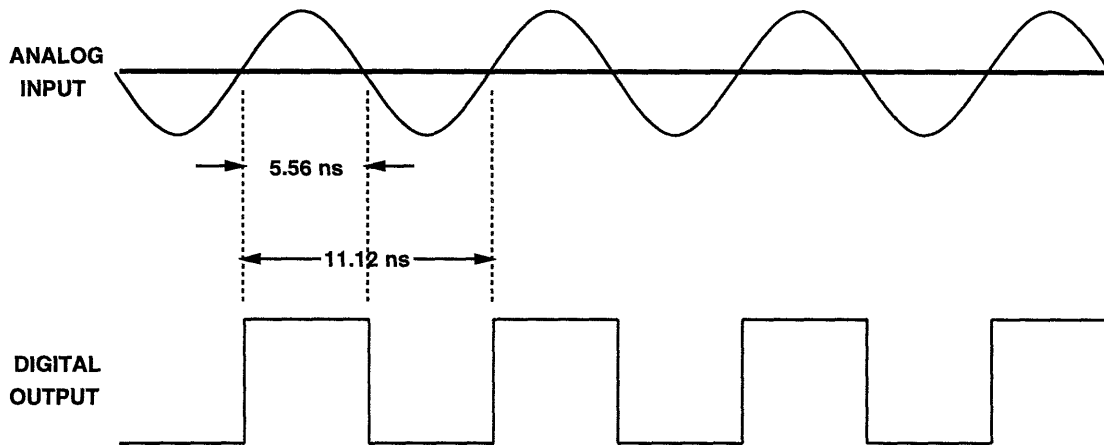


Figure 1-2: Determining the ADC Bandwidth for a  $180\text{Mb/s}$  Data Rate

sequence that had been recorded onto disk was 1010101010..., the input analog waveform would look like a sine wave with its zero-crossings spread  $\frac{1}{180(10)^6}\text{s}$  or  $5.56\text{ ns}$  apart. Since it takes  $11.12\text{ ns}$  for the signal to complete two zero crossings and return to its original starting place, the *period* of the input analog signal is  $11.12\text{ ns}$  and the frequency is  $\frac{1}{11.12\text{ ns}}$  or  $90\text{ MHz}$ . Thus, the ADC must work relatively well at  $90\text{ MHz}$  for the entire system to work. To avoid aliasing, the ADC has to sample the input at double the maximum input frequency (Nyquist rate). Therefore to maintain the  $20\text{Mbyte/s}$  data transfer rate with one additional bit of parity, the ADC has to be clocked at  $180\text{ MHz}$ .

Two important characteristics of the ADC design - conversion time and resolution - need to be determined. The conversion time required for this design is one clock cycle or  $5.56\text{ ns}$ , since a new digital output is required at every clock cycle to provide a  $180\text{Mbit/s}$  data rate. The resolution selected is 6 bits. This amount of resolution is adequate for the PRML system to work accurately. This tradeoff between high-resolution and high-speed is the most fundamental tradeoff involved in data converter design. It allows the designer to choose the type of architecture that is to be used in the data converter. These tradeoffs are further described in the following section which gives a description of various converter architectures and discusses how each is a compromise between conversion time and resolution.

## 1.2 Analog-to-Digital Conversion Techniques

### 1.2.1 Dual-Slope Integrating ADCs

The dual-slope integrating converter [2] shown in Fig. 1-3 provides high accuracy, but requires a long conversion time. This converter operates by an indirect conversion method. The unknown voltage is converted into a time period which is then measured by a clock and counter. Conversion begins when the unknown input voltage,  $V_{in}$ , is applied to the integrator input through a switch. At the same instant, the counter begins to count clock pulses and counts up to overflow. The voltage across the capacitor ramps with a slope proportional to the input until the counter reaches a set maximum value  $D_{max}$ . At this point, the voltage on the capacitor is:

$$V_c = -\frac{(V_{in}T_cD_{max})}{RC} \quad (1.1)$$

where  $T_c$  is the period of the clock signal. After the counter reaches its maximum value, the control circuit switches the integrator to the negative reference voltage. The voltage on the capacitor ramps back toward zero with a constant slope set by the reference. The counter is again active and measures the number of clock cycles that occur during this process. The conversion is completed when the comparator detects a zero output after time:

$$T = T_cD_{out} = RC\frac{V_c}{V_{ref}} \quad (1.2)$$

Substituting the value of  $V_c$  obtained when charging the capacitor, the equation becomes:

$$\frac{D_{out}}{D_{max}} = -\frac{V_{in}}{V_{ref}} \quad (1.3)$$

Thus the digital output represents the ratio of the input voltage to the reference voltage.

Dual-slope conversion has several important features. First, conversion accuracy is independent of the stability of the clock, integrating capacitor or resistor so long as they are constant during the conversion period. Accuracy depends only on the reference accuracy. Another feature is that the noise rejection of the converter can be nearly infinite for frequencies that are multiples of  $\frac{1}{D_{max}T_c}$ .

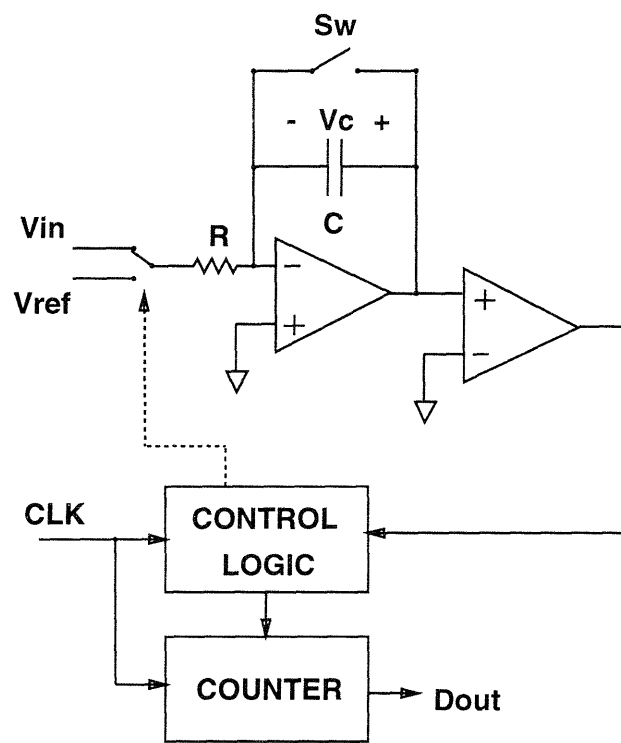


Figure 1-3: A Dual-Slope Integrating Analog-to-Digital Converter

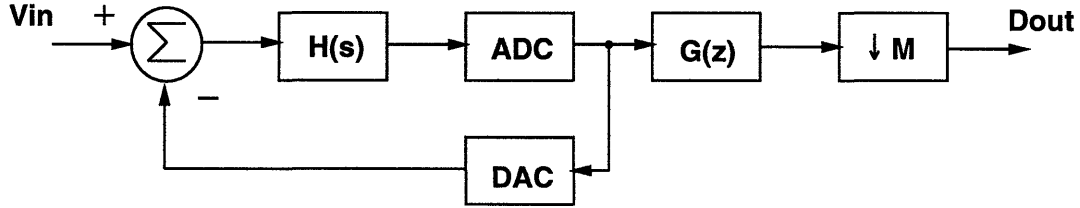


Figure 1-4: A Sigma-Delta Modulator

### 1.2.2 Sigma-Delta Converter

The sigma-delta modulator [3] is another low speed, high resolution converter architecture. As shown in Fig. 1-4, the converter consists of several analog and digital subsystems. The approach in this system is to perform a high speed low resolution conversion and then gain more resolution with digital filtering. This type of converter is frequently called an oversampling ADC because the input sampling rate is much higher than the Nyquist rate.

The analog portion consists of a feedback loop with a filter followed by an ADC in the feedforward path. Provided that this converter is fast enough compared to the final output rate, its resolution can be as low as a single bit. This eliminates the problem of converter linearity. The feedback path consists of a DAC.

When the ADC is modeled as an uncorrelated additive noise source, as in Fig. 1-5, the real benefit of the converter is apparent. The transfer function from input to output is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1 + H(s)} \quad (1.4)$$

The transfer function from quantization noise to output is:

$$\frac{V_{out}(s)}{E_q(s)} = \frac{1}{1 + H(s)} \quad (1.5)$$

The filter is designed so that in the signal band the transfer function from input to output is approximately unity and the transfer function from noise to output is small. This is reversed in the stop band. The effect is that most of the quantization noise energy is pushed out of the passband

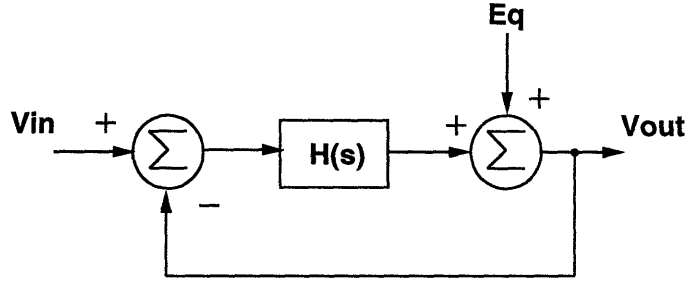


Figure 1-5: Modeling the ADC as a Noise Source

into the stopband. The order of the analog filter determines how well this action is performed. The digital portion of the system removes the higher frequency noise and decimates the signal (by a factor of  $M$ ) to the final output rate. Since most of the quantization noise energy has been removed, the effective resolution of the converter is much higher than that of the actual ADC in the system.

### 1.2.3 Tracking ADCs

The tracking ADC [2] usually provides less accuracy than a dual-slope or sigma-delta ADC, but is somewhat faster. As shown in Fig. 1-6, the tracking ADC uses a DAC. The converter compares the unknown input voltage with the output of the DAC. If the output of the DAC is greater than the analog input voltage, the control logic signals the counter to decrement. If the analog input is greater than the output of the DAC, the counter is signalled to increment.

The advantage of the tracking ADC is that it can continuously follow the input voltage. If the input voltage only varies by a few least significant bits (LSBs) then the conversion time can be quite small. The resolution of this converter is limited by the quality of the DAC and the comparator.

### 1.2.4 Successive-Approximation ADCs

A popular ADC architecture for medium to high speed applications is the successive-approximation type [2]. As seen in Fig. 1-7, the architecture employs a DAC in a feedback loop allowing an  $n$ -bit conversion to take place in  $n$  clock cycles. In the first cycle, the successive-approximation register sets the most-significant bit (MSB) high and all other bits low. If the analog input is greater than the DAC output, the bit remains high, otherwise it is set low. This process continues for the next



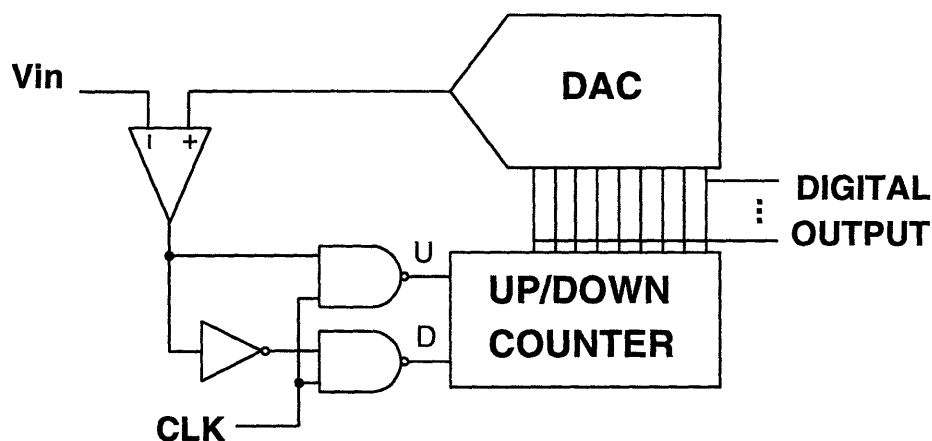


Figure 1-6: A Tracking Analog-to-Digital

most significant bit. The MSB-1 bit is set high and the remaining lower bits are set low. The conversion is complete when all of the bits have been tested. Thus, the output of the DAC approaches the unknown input voltage in steps that are reduced by a factor of 2 every cycle. After  $n$  cycles, the input to the DAC is available as the ADC output.

As with the tracking ADC, the accuracy of the converter is limited by the DAC in the feedback loop. As one would believe, the successive-approximation type converter will have a shorter conversion time for highly varying signals than the tracking ADC because the successive-approximation converter makes signal changes with order of magnitude ( $2^n$ ) steps while the tracking ADC output changes by 1 LSB at a time.

### 1.2.5 Flash ADCs

The ADC architecture that provides rapid conversions with low-to-medium accuracy is the flash ADC architecture [2]. As shown in Fig. 1-8, this converter type uses a separate comparator with a fixed reference for every quantization level from zero volts to the full scale voltage. If the desired resolution of the converter is  $n$  bits, then the converter will require  $2^n - 1$  comparators. The reference voltages to the comparators are produced by the resistive voltage divider shown in the figure. When the input voltage  $V_{in}$  is applied to the non-inverting terminal of the comparators, the comparators with reference voltages below the input voltage will have a digital ONE output. Those

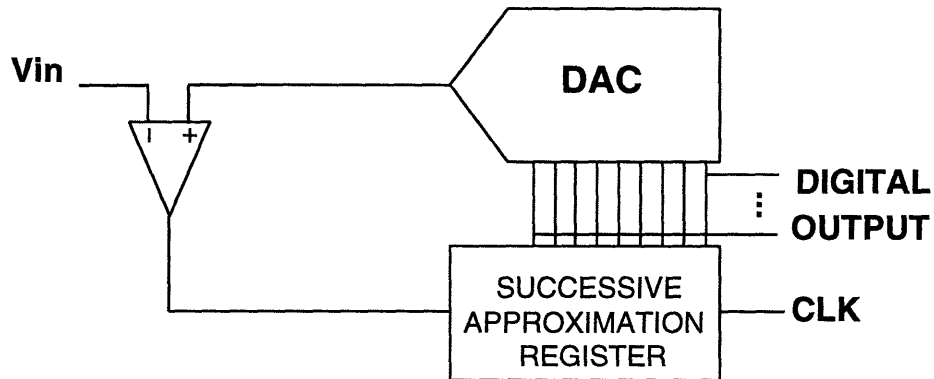


Figure 1-7: A Successive-Approximation Analog-to-Digital Converter

Table 1.1: Speed/Resolution Tradeoff Summary for Various ADC Architectures

ADC Architecture	Speed	Resolution
Dual Slope	Low (1-100 Hz)	High (14-16 bits)
Sigma-Delta	Low-Med. (100 Hz to 20kHz)	High (14-20 bits)
Tracking	Medium (100 kHz to 1 MHz)	Medium (8-12 bits)
Successive Approx.	Medium (100 kHz to 1 MHz)	Medium (8-12 bits)
Flash	High (1 MHz to 500 MHz)	Low-Med. (6-8 bits)

comparators with reference voltages above the input voltage will have a digital ZERO output. The output of the comparator array is known as thermometer code because the digital ONE outputs resemble the mercury in a thermometer rising and falling in response to a changing temperature. This code is converted to a digital output with several NAND gates and a PLA. The details will be described later.

### 1.2.6 Summary of ADC Architectures

Table 1.1 shows a summary of the various ADC architectures which have been discussed [4]. It presents the trade off between speed and resolution.

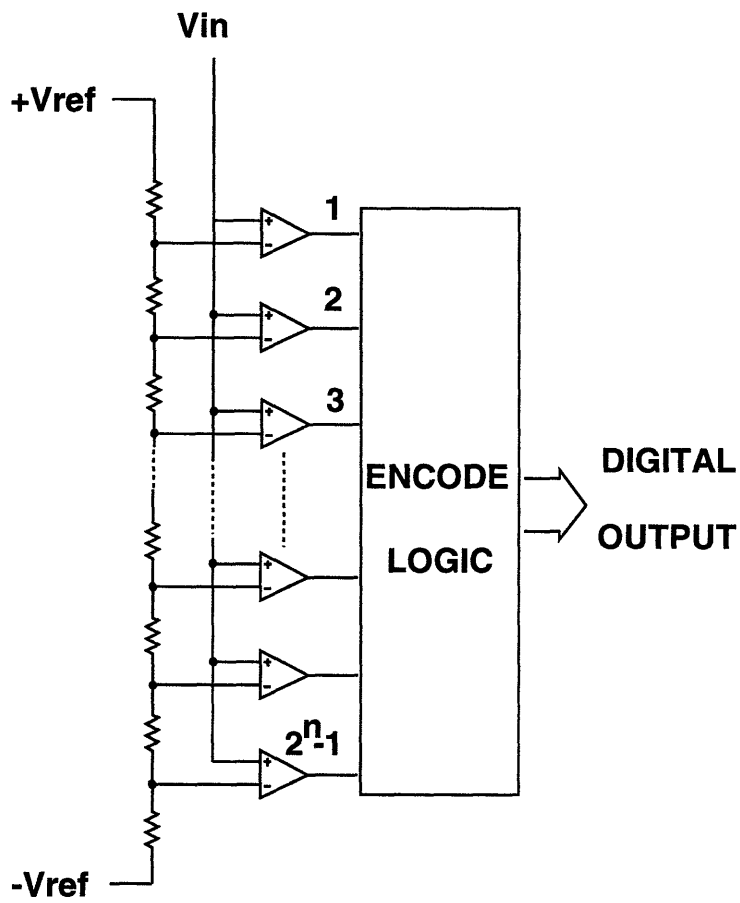


Figure 1-8: An n-bit Flash Analog-to-Digital Converter

### 1.3 Quantization Theory

In addition to studying the various types of converter architectures, it is also necessary to understand the nature of quantization in order to complete a successful converter design.

Analog-to-digital conversion is a process of sampling, quantizing and coding. Quantization begins with the availability of an analog sample. This sample can take on any of a continuum of amplitude values ranging from  $-\infty$  to  $+\infty$ . The function of the quantizer is to replace each of these sample values with an output which is an approximation of the original amplitude. Each output value is one of a finite set of real numbers [5]. This set contains  $2^n$  states for a converter coding the input signal into an  $n$ -bit output. The larger the set of output states, the more resolution the converter is said to have.

The transfer function of a 3-bit ADC, which shows the set of output states, is pictured in Fig. 1-9. Since the ADC has a resolution of 3 bits, it converts the input signal into one of  $2^3$  or 8 output states. The output states are assigned binary numbers from 000 to 111. The analog input range for this quantizer is 0 to 1 V.

The transfer function contains  $2^n - 1$  analog decision points (or threshold levels). These points are at the voltages +.0625, +.1875, +.3125, +.4375, +.5625, +.6875 and +.8125. The decision points must be precisely set in a quantizer in order to divide the analog voltage range into the correct quantized values.

The voltages +.125, +.250, +.375, +.500, +.625, +.750 and +.875 are at the center of the range of each output state. The analog decision points are precisely halfway between these center points. The staircase function formed by the analog decision points is the best approximation that can be made for a straight line drawn through the origin (or 0 V) and the full-scale range of 1 V. Note that this line passes through all of the center points of the different output states [2].

For any part of the input range of the quantizer, there is a small range of analog values within which the same output code word is produced. This small range is the voltage difference between any two adjacent decision points and is known as the analog quantization size, or *quantum*,  $Q$ . In Fig. 1-9, the quantum is .125 V and is given by:

$$Q = \frac{FSR}{2^n} \quad (1.6)$$

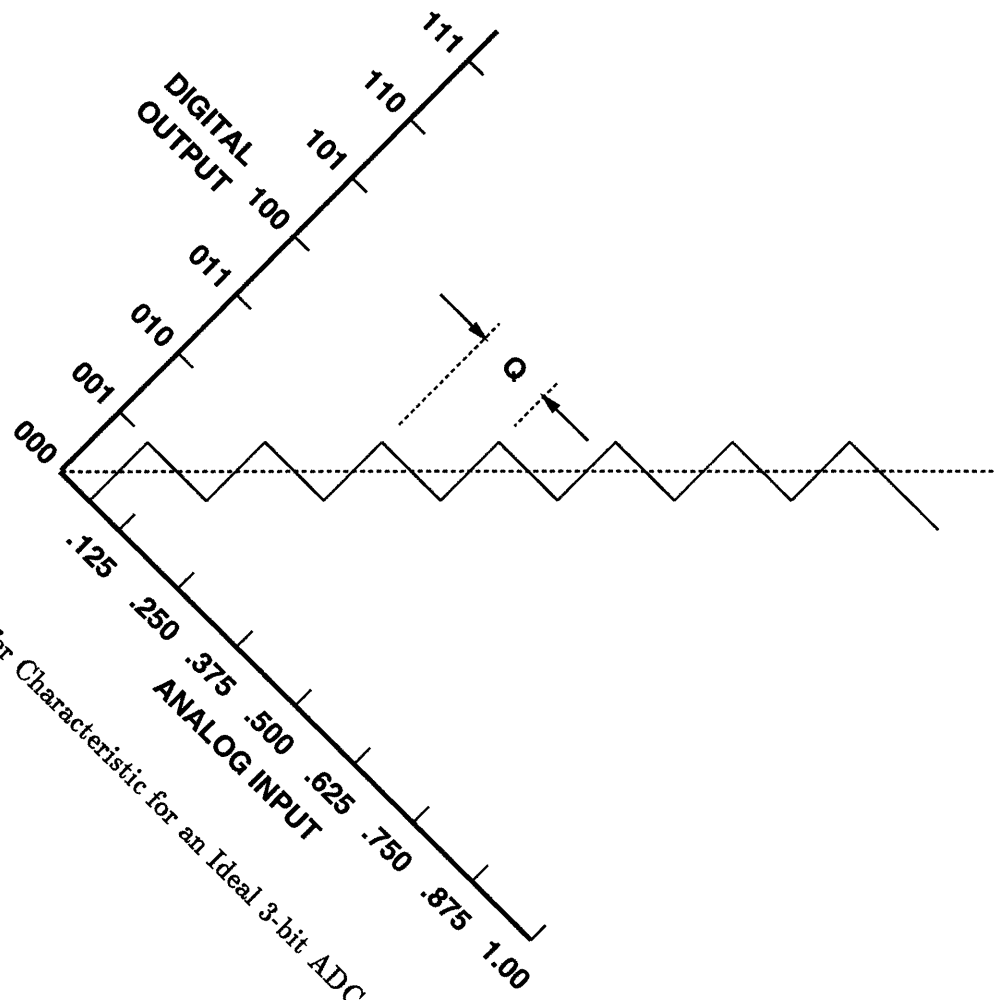


Figure 1-9: Transfer Characteristic for an Ideal 3-bit ADC

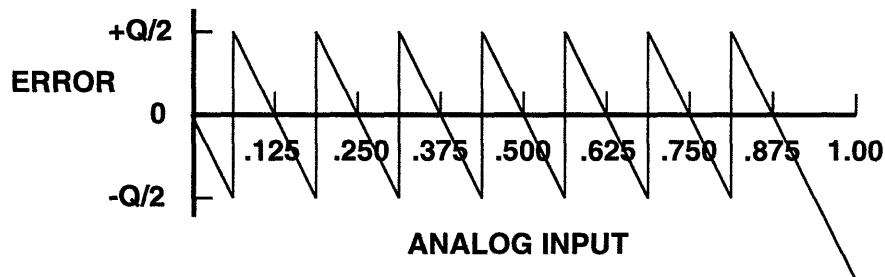


Figure 1-10: Quantization Error for an Ideal 3-bit ADC

where  $FSR$  is the full-scale range (1 V in this case).  $Q$  is the smallest analog difference that can be resolved or distinguished by the quantizer.

If the ADC input is ramped through its entire range of analog values and the difference between the quantized output and input is measured, a sawtooth error function, shown in Fig. 1-10, results. This function is called the quantizing error. It is the irreducible error that results from the quantizing process. It can only be reduced by increasing the number of output states of the quantizer, thereby increasing the resolution of the ADC. The quantization error varies between  $-\frac{Q}{2}$  and  $+\frac{Q}{2}$ . The output of the quantizer can be modeled as the analog input with the quantization error added to it. The quantization error is considered to be *noise* in this model and it is sometimes referred to as *quantization noise*. This noise has a peak-to-peak value of  $Q$  and an average value of zero. The RMS value is computed to be  $\frac{Q}{\sqrt{12}}$ .

## 1.4 ADC Nonidealities

### 1.4.1 Error Types

In addition to the irreducible quantization error that is introduced during the conversion process, real ADCs can exhibit other errors that appear as departures from the ideal transfer function. These departures include offset, gain and linearity errors. To further complicate matters, the errors can be dependent on analog input frequency and temperature.

Offset error is defined as the analog value by which the transfer function fails to pass through

zero. It is usually expressed in volts. The net effect of this error on the transfer function of an ideal ADC is a horizontal shift.

Gain error, or scale factor error, is defined as the difference in full scale values between the ideal and the actual transfer functions when the offset error is zero. It is expressed in percent. If a line was drawn through all the center points of the different output states for a ADC with gain error, the slope of the line would be larger or smaller than that of a similar line drawn for an ideal ADC.

### 1.4.2 Differential Linearity Error

Linearity error, or nonlinearity, is a difficult type of error to deal with. This error is grouped into two types of error: differential and integral. Differential linearity error, also called differential nonlinearity (DNL), is the amount of deviation of any quantum from its ideal value. The DNL for every quantum level can be found using the following equation:

$$DNL_i = \frac{2^n(Q_{i+1} - Q_i)}{FSR} - 1 \quad (1.7)$$

where  $DNL_i$  is the differential nonlinearity measured in LSBs of the  $i_{th}$  quantization level,  $Q_i$  and  $FSR$ , the full scale range. Fig. 1-11, illustrates the DNL of a 3 bit ADC. If a converter has  $\pm\frac{1}{2}$  LSB of maximum differential nonlinearity, the actual size of any quantization level will be between  $\frac{1}{2}$  and  $1\frac{1}{2}$  LSBs. Notice that if the differential nonlinearity is equal or greater than 1 LSB, the set of valid outputs will be missing states.

### 1.4.3 Integral Linearity Error

The second type of linearity error is integral linearity error, or integral nonlinearity (INL). Integral linearity error is due to the curvature of the transfer function resulting in departure from an ideal straight line. The INL can be obtained using the following equation:

$$INL_i = \sum_{n=0}^i DNL_n = \frac{2^n}{FSR}(Q_{i+1} - Q_0) - i - 1 \quad (1.8)$$

As Fig. 1-12 shows, the quoted integral linearity error for an ADC will be the maximum distance (in LSBs) between the ideal straight line and the center of the range of each output state when the offset and gain error is zero.

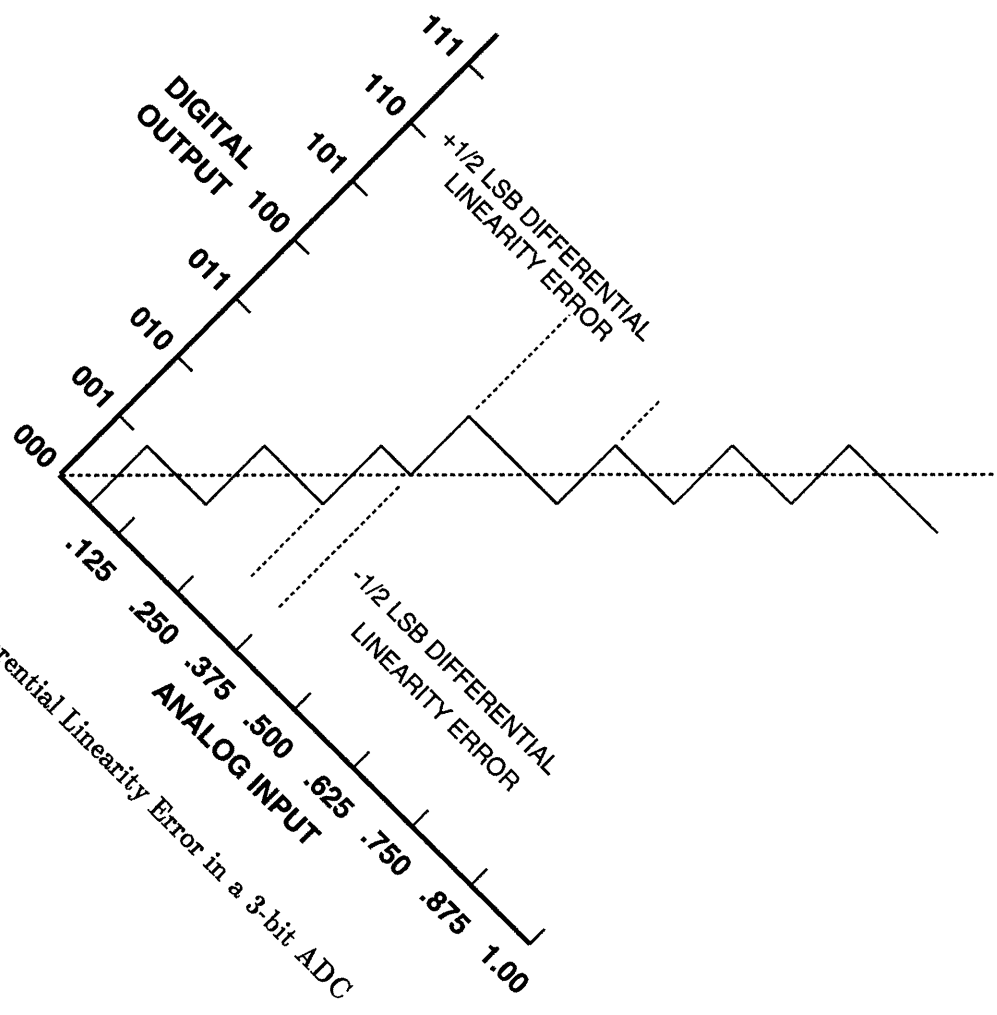


Figure 1-11: Differential Linearity Error in a 3-bit ADC



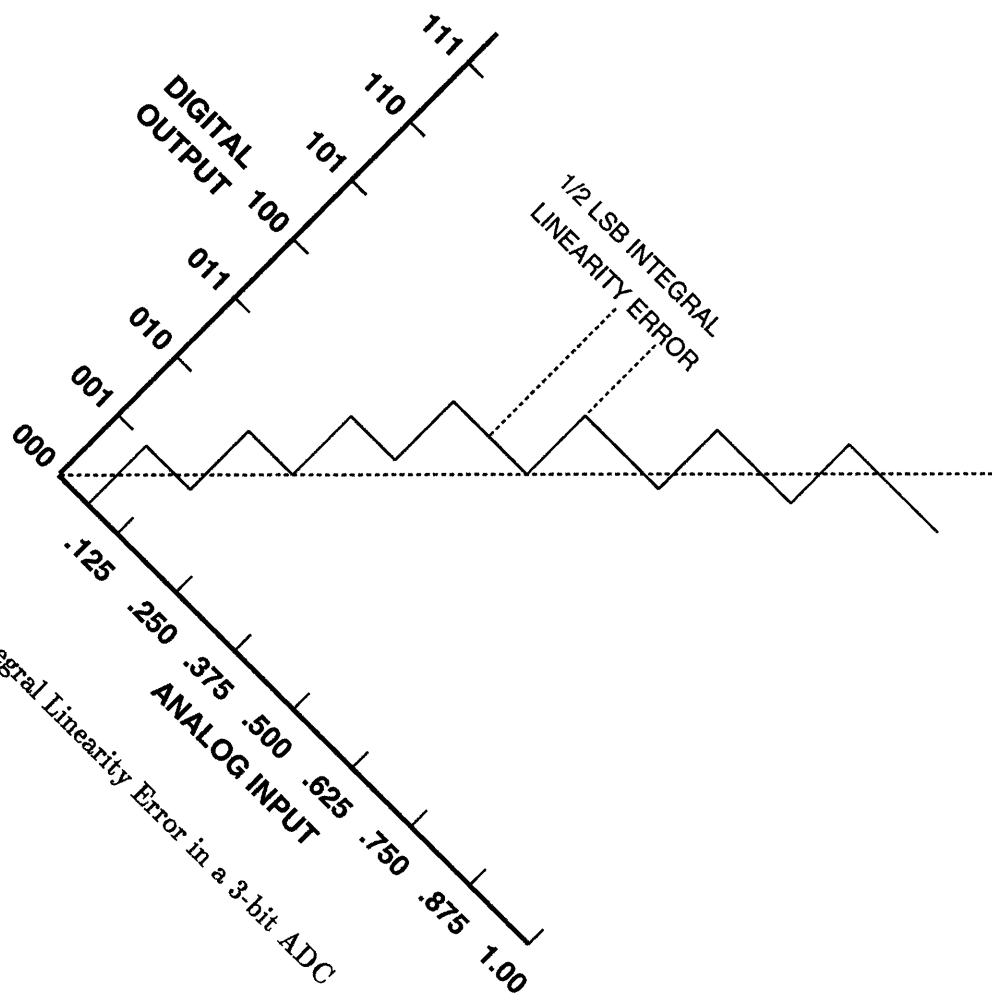


Figure 1-12: Integral Linearity Error in a 3-bit ADC

## 1.5 Research Objectives

The flash ADC, described in Subsection 1.2.5, is the conventional architecture for a high speed, medium resolution data converter. This architecture is extremely fast. It is limited in speed only by the reaction time of the comparators and the decoding logic. However, the amount of componentry required rises exponentially ( $2^n$ ) with the number of bits encoded [7]. Thus, the die area and power dissipation of a high speed ADC employing the flash architecture increase exponentially with the system resolution. This results in an increase in the cost of the system. The system cost increases because chip yield falls as the die area increases. A second reason for the increased cost is that the high power dissipation will require the use of additional equipment to keep the system temperature at an optimal level.

The purpose of this research was to develop an ADC architecture that required fewer than  $2^n - 1$  comparators to perform an  $n$ -bit conversion (where  $n=6$ ) at sampling rates comparable to those of typical flash ADCs. It was realized that the number of required comparators could be reduced by a factor of 3 to 4 by performing a type of analog preprocessing, called folding [6], on the input signal. To show that such an architecture is feasible, a 6-bit converter with a sampling rate of  $180MHz$ , input range of  $\pm 0.5V$  and a power supply voltage of  $3.3V$  was designed, simulated and laid out in a  $0.5\mu m$  BiCMOS process.

## Chapter 2

# Architecture and Reduction Techniques

### 2.1 Folding Architecture

The architecture of a 6-bit, folding ADC is illustrated in Fig. 2-1. This architecture has some similarities with the second stage of the ADC described in [8]. The conversion is performed in two parallel stages. The upper section of the architecture is involved in determining the most significant bit (MSB) of the 6-bit digital output. The lower sections, folding circuitry and resistive interpolation, determine the least significant bits (LSBs). Both MSB and LSB sections include an array of high speed comparators which provide amplification and sampling of the analog input signal. Some overlap between the MSB and LSB range is required for performing digital error correction on the sampled signal. Error correction is necessary due to timing and gain mismatches between the MSB and LSB stages.

Both the MSB and LSB stages use folding amplifiers to aid in the conversion process. The MSB stage uses folding amplifiers in the cycle encoder to provide several quantization threshold levels. These levels can be used to perform a coarse analog-to-digital conversion. The LSB stage also uses folding amplifiers to drive a resistive interpolation network. This interpolation network acts as a resistive voltage divider to provide more quantization threshold levels than are available from the MSB stage. The LSB stage therefore provides the additional resolution required to perform a 6-bit conversion. The outputs of the comparator arrays from the MSB and LSB sections are then

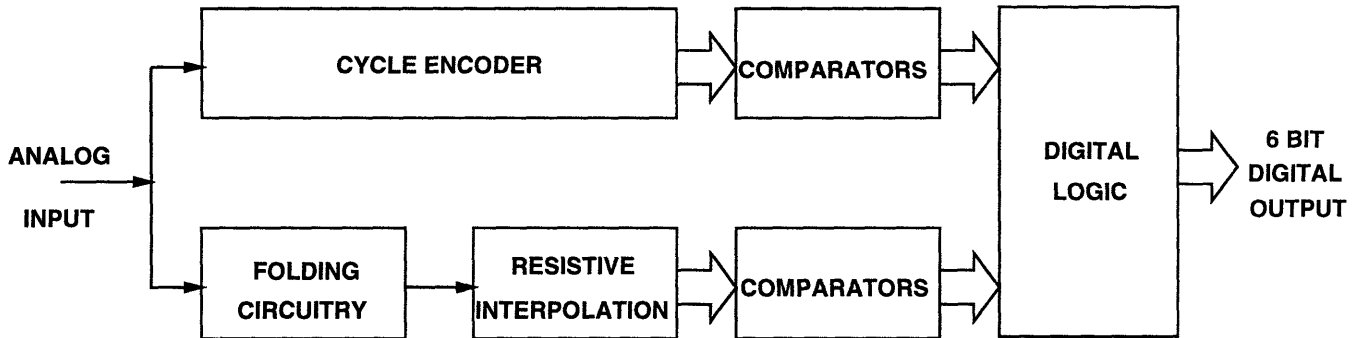


Figure 2-1: A 6-Bit Folding Analog-to-Digital Converter

processed by the digital logic to perform error correction. The 6-bit digital output is available from the digital encoding section after one clock cycle.

## 2.2 Reduction Techniques

As previously mentioned, the folding architecture used in this design reduces the number of comparators required for a 6-bit conversion by a factor of three to four. This reduction comes from the use of two analog techniques - folding and resistive interpolation.

### 2.2.1 Folding Technique

The folding technique, as the name implies, folds the input signal. Fewer comparator latches are needed because they are used in a far more efficient way [9]. Fig. 2-2 shows a system that uses folding. A folding amplifier has been inserted between five differential amplifiers and a sample latch. The differential amplifiers provide the inputs to the folding amplifier. The output of the folding amplifier can be stored on the sample latch when the clock line goes high.

Each differential amplifier compares the analog input voltage with one of the five DC reference voltages attached to the system -  $V_a, V_b, V_c, V_d, V_e$ . When the analog input voltage is less than a DC reference voltage, the output of the differential amplifier is a negative voltage. When the input voltage rises above the DC reference voltage, the differential amplifier's output becomes positive. The transitions from negative to positive voltages at the differential amplifier outputs are used to

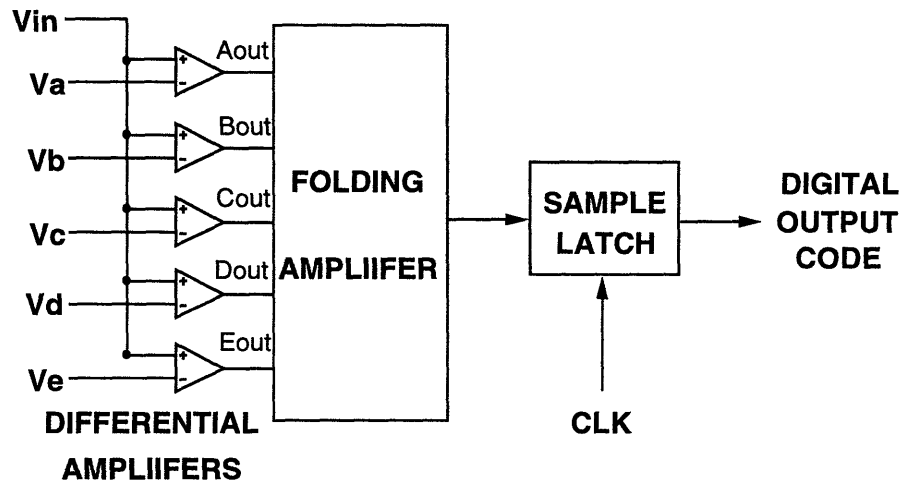


Figure 2-2: Using the Folding Technique for Comparator Reduction

control the folding amplifier. Fig. 2-3 shows that as the analog input voltage increases from 0 to the full scale voltage, the differential amplifier outputs will change from negative to positive values. The net effect is that the folding amplifier output crosses the zero axis several times (5, this case) over the full scale range of the input voltage. The output signal of the folding amplifier shows that the zero-crossings occur when the input voltage reaches the DC reference voltage values. In this way, the sample latch is provided with more than one differential amplifier output signal and will handle more quantization levels over the full scale voltage. This is an improvement over the flash ADC architecture. In a flash ADC, every sample latch can only handle one quantization level. This concept of latch reuse is what allows the folding ADC to perform a high speed  $n$ -bit conversion with less than  $2^n - 1$  latches. However, it is critical that the DC reference voltages are sufficiently far apart to prevent the output signals ( $A_{out}$ -  $E_{out}$ ) from affecting one another.

### 2.2.2 Resistive Interpolation

The preceding section explained how the number of sample latches required for a high speed conversion can be reduced. However, for a 6-bit conversion the number of differential amplifiers is still large. Every latch will require a folding amplifier with five differential amplifiers. The

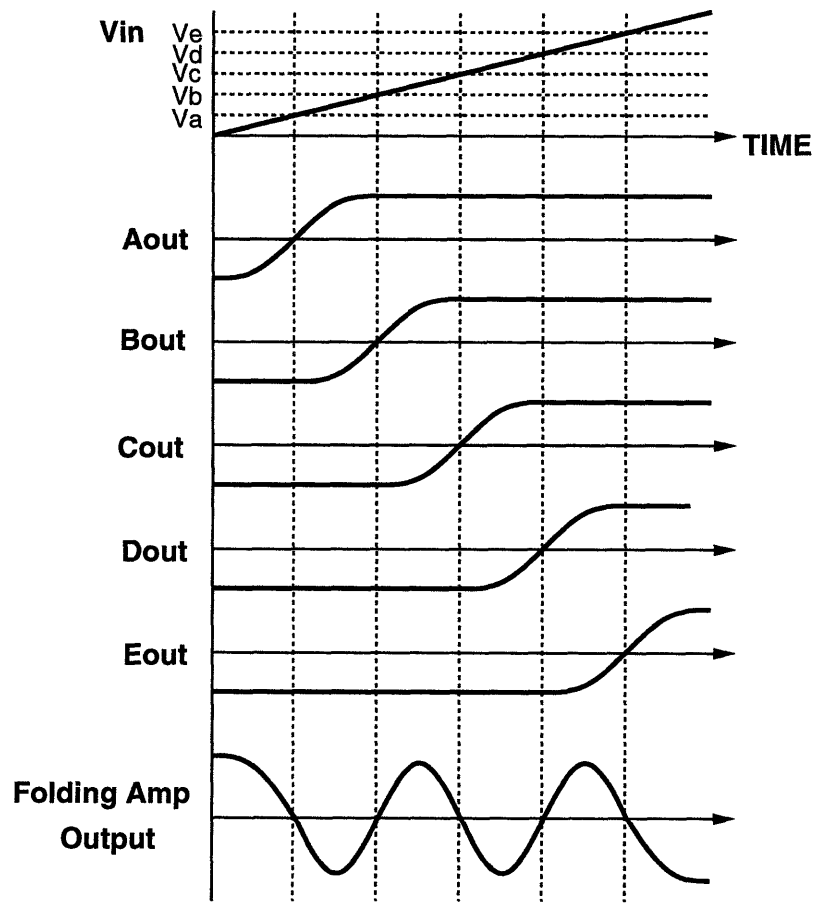


Figure 2-3: Waveforms Describing the Folding Technique

transfer characteristics of these folding amplifiers would be shifted along the horizontal axis to provide additional zero-crossings. This is illustrated in Fig. 2-4. Folding amplifier outputs  $I$ ,  $X$  and  $Q$  intersect the horizontal axis at several places providing quantization levels that can be used in a high-speed conversion. This design with multiple folding amplifiers uses approximately the same number of differential amplifiers required in the flash architecture, so no significant savings in terms of power dissipation and die area will result. However, savings can be achieved by deriving additional folded waveforms from the output of existing folding amplifiers by resistive interpolation. Fig. 2-5 demonstrates this technique. The outputs of two folding amplifiers,  $I$  and  $Q$ , are used to determine a third folded waveform. The third waveform, labeled  $\frac{I+Q}{2}$ , is created by connecting two equal-valued resistors in series at the outputs of the  $I$  and  $Q$  amplifier outputs as shown in Fig. 2-6. The third waveform is available at the center tap of the resistors and can be described as the average of the  $I$  and  $Q$  waveforms,  $\frac{I+Q}{2}$ . The signal distortion suffered by the interpolated waveform is not of any importance. As long as the zero-crossings are correct, the latch connected to the resistor tap will sample the correct value. Also notice that the zero crossings points of the third folded waveform occur at the same input voltages as the  $X$  waveform from Fig. 2-4. Thus, additional quantization levels can be sampled by using a passive resistive network rather than adding folding amplifiers.

The location of the zero-crossings of the interpolated waveform are determined by the resistive interpolator. The zero-crossing points of the interpolated waveform in Fig. 2-5 are halfway between those of the  $I$  and  $Q$  waveforms. This is because the interpolator that derives this waveform uses equal-valued resistors. Additional zero crossings between the  $I$  and  $Q$  waveforms can be generated by using unevenly weighted averages of the two waveforms. These additional zero crossings must be spread at single LSB intervals over the entire full scale input voltage in order to provide a conversion with a 6-bit resolution.

Thus, the principle of the interpolation technique is to reduce the number of differential amplifiers by simply omitting several differential amplifiers and recovering the missing signals by resistive interpolation between the output signals that are still available. Although performing this recovery may seem trivial, the principle makes use of the fact that the differential amplifiers are nonideal. Instead of switching from low to high instantaneously when the input voltage exceeds the reference voltage, they follow the input over a limited range in a more or less linear way. This property of

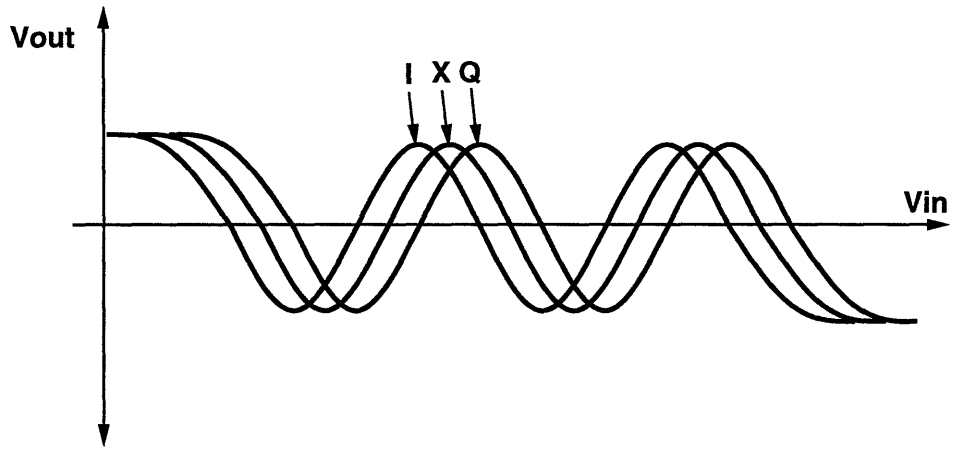


Figure 2-4: Several Folding Amplifier Transfer Characteristics

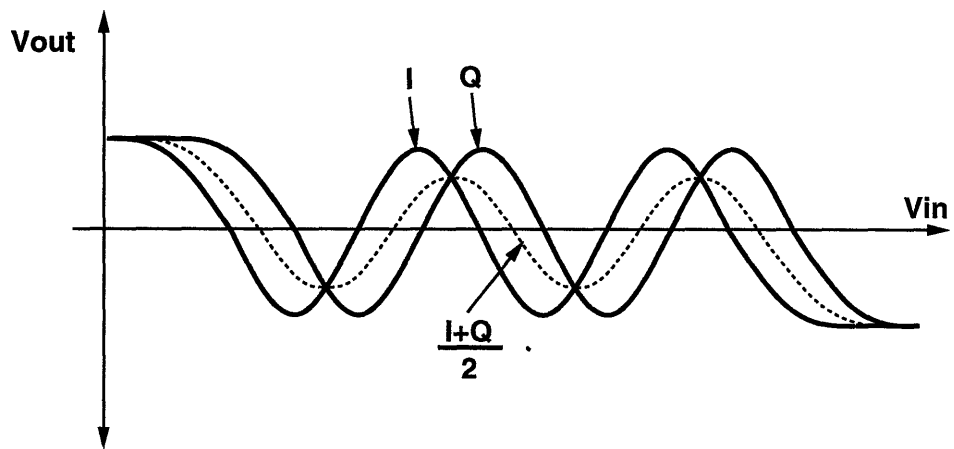


Figure 2-5: Creating an Additional Folded Waveform Through Resistive Interpolation



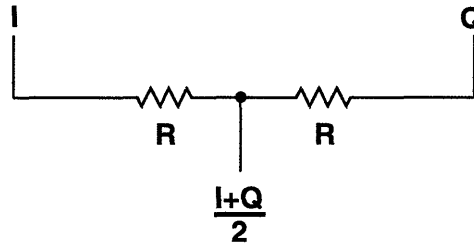


Figure 2-6: A Simple Resistive Interpolator

practical differential amplifiers allows for the interpolation mentioned above. Since the information contained in the differential amplifier output signals is not affected as long as the position of the zero-crossing of the output signal remains unchanged, the resolution of the converter is not compromised [9].

## 2.3 Section Descriptions

The folding ADC architecture pictured in Fig. 2-1 is divided into two sections that determine the LSBs and MSB of the 6-bit sample. The reduction techniques are used extensively in each section.

### 2.3.1 LSB Section Specification

The LSB section is made up of two fully-differential folding amplifiers, a resistive interpolation network and 16 high speed comparators. The folding amplifiers are driven by 20 taps of a high-speed fully-differential buffer. This buffer couples the differential input across the output taps. Each tap has a different DC component associated with it. The exact connections between the taps and folding amplifiers will be described in the following chapter. The waveforms produced by the combination of the buffer and the folding amplifiers are shown in Fig. 2-7.

The fully-differential waveforms  $I - \bar{I}$  and  $Q - \bar{Q}$  span the input range of  $-0.5 V$  to  $+0.5 V$ . The two transfer functions are described as being  $90^\circ$  out of phase with each other [10]. An important feature to recognize is that the order and relative distances between the zero-crossings in the range

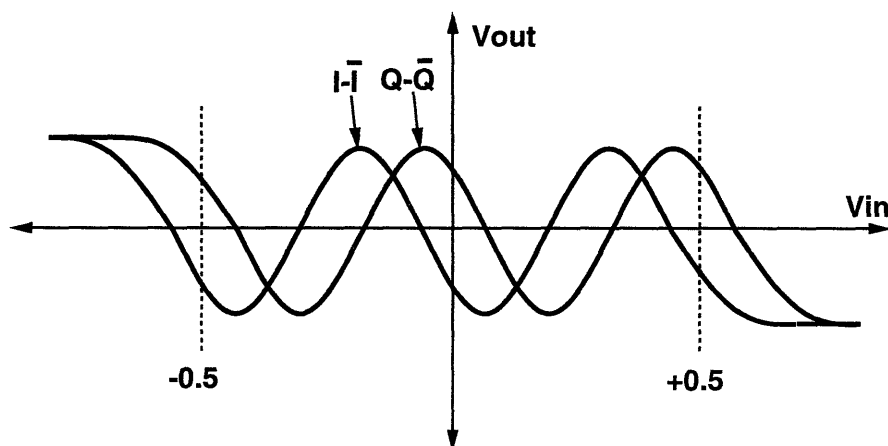


Figure 2-7: Folded Waveforms

from  $-0.5\text{ V}$  to  $0.0\text{ V}$  and from  $0.0\text{ V}$  to  $+0.5\text{ V}$  are the same. For this reason, the folding ADC can be referred to as cyclical. The output codes of the LSB section will be repeated in regular cycles over the input voltage range. This idea of cyclical codes is important to the functionality of the folding ADC. As described in Section 2.1, the MSB section of the folding ADC determines the most significant bit of the sampled voltage. The MSB section uses this information to determine which cycle the input voltage is located. If the MSB is a logical ZERO, then the input voltage is in the lower cycle or the range between  $-0.5\text{ V}$  and  $0.0\text{ V}$ . If the MSB is a logical ONE the input voltage is in the upper cycle, ranging between  $0.0\text{ V}$  and  $0.5\text{ V}$ . Each of these cycles must be able to determine the remaining 5 bits of the desired 6-bit sample. Therefore, both the upper and lower cycles are divided into 32 quantum levels or LSBs. But from Fig. 2-7, we see that the folded waveforms  $I - \bar{I}$  and  $Q - \bar{Q}$  only provide 4 quantization points (zero-crossings) in each cycle. The additional zero-crossings are determined with resistive interpolation.

Each cycle of the input range is divided into 32 quantum levels of  $15.625\text{mV}$  each by 33 zero-crossings. To accomplish this, 7 additional zero-crossings need to be interpolated between each of the zero-crossings of  $I - \bar{I}$  and  $Q - \bar{Q}$ . Note that only zero-crossings inside the shaded region of Fig. 2-8 can be determined this way. The zero-crossings required in the unshaded regions can be interpolated between the  $I - \bar{I}$  and  $\bar{Q} - Q$  waveforms shown in Fig. 2-9.

The required number of zero-crossings can be achieved by interpolating 14 additional waveforms. Seven waveforms are interpolated from  $I - \bar{I}$  and  $Q - \bar{Q}$ . The other seven waveforms are interpolated from  $I - \bar{I}$  and  $\bar{Q} - Q$ . The total number of folded waveforms is  $16 - 2$  folding amplifier waveforms

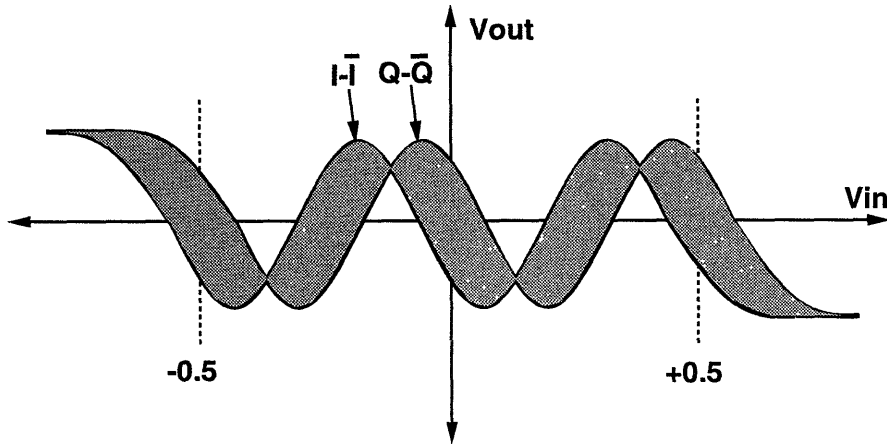


Figure 2-8: Interpolation Regions Between  $I - \bar{I}$  and  $Q - \bar{Q}$

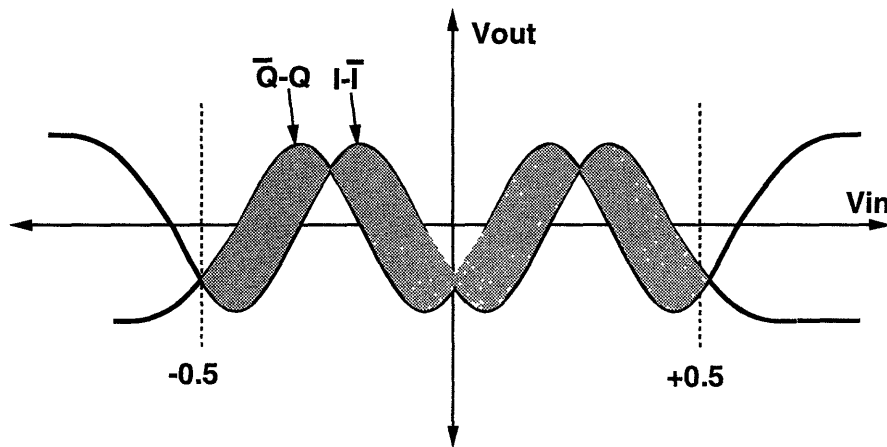


Figure 2-9: Interpolation Regions Between  $I - \bar{I}$  and  $\bar{Q} - Q$

and 14 interpolated waveforms. Each of these waveforms needs to be sampled with a separate latch. Thus, the LSB stage requires 16 latching comparators. The combination of the resistive interpolation network and the latching comparators is pictured in Fig. 2-10.

The network is driven by the fully-differential folding amplifier outputs  $I$  and  $Q$ . The interpolated waveforms are available at output taps of the resistor divider strings. These waveforms act as the comparator inputs of the LSB section of the converter. By making a connection to its local tap and the tap diametrically across from it, each comparator receives a fully-differential input signal. The comparator outputs are processed by the decode logic and determine the 5 low order bits of the 6-bit output. The most-significant-bit is determined by the cycle encoder of the MSB section.

### 2.3.2 MSB Section Specification

The most-significant-bit of the 6-bit sample is determined by the cycle encoder of Fig. 2-1. The MSB will equal a digital ZERO if the analog input is less than  $0V$ . If the analog input is greater than  $0V$ , the MSB will equal a digital ONE. A folding amplifier with the transfer characteristic of  $A$  in Fig. 2-11 could be used to determine the MSB. However, to provide for error correction caused by delay mismatch between the LSB section and the MSB section, three folding amplifiers are used. The additional folding amplifiers provide more resolution which facilitates the error correction.

The transfer characteristics ( $A$ ,  $B$ ,  $C$ ) of the three folding amplifiers used by the cycle encoder are pictured in Fig. 2-11. The waveforms from the outputs  $A$ ,  $B$  and  $C$  are then sampled by latched comparators. The comparator outputs ( $ABC$ ) can have 6 possible combinations over the analog input range: 000, 001, 011, 111, 101, 100. The advantage of this coding scheme is that as the input voltage rises, only one digit of the 3 digit code changes at a time. This feature, similar to that of Grey codes, prevents sparkle codes from occurring. The comparator outputs can then be used to determine the MSB with the digital logic circuitry.

### 2.3.3 Digital Logic Section Specification

The digital logic circuitry processes the comparator outputs from the LSB and MSB sections to produce the 6-bit output. The conversion is completed in several steps. First, any errors that have occurred in the conversion are detected and then corrected. Included in these errors are bubble errors, similar to those in flash ADCs, and errors due to timing mismatch between the LSB

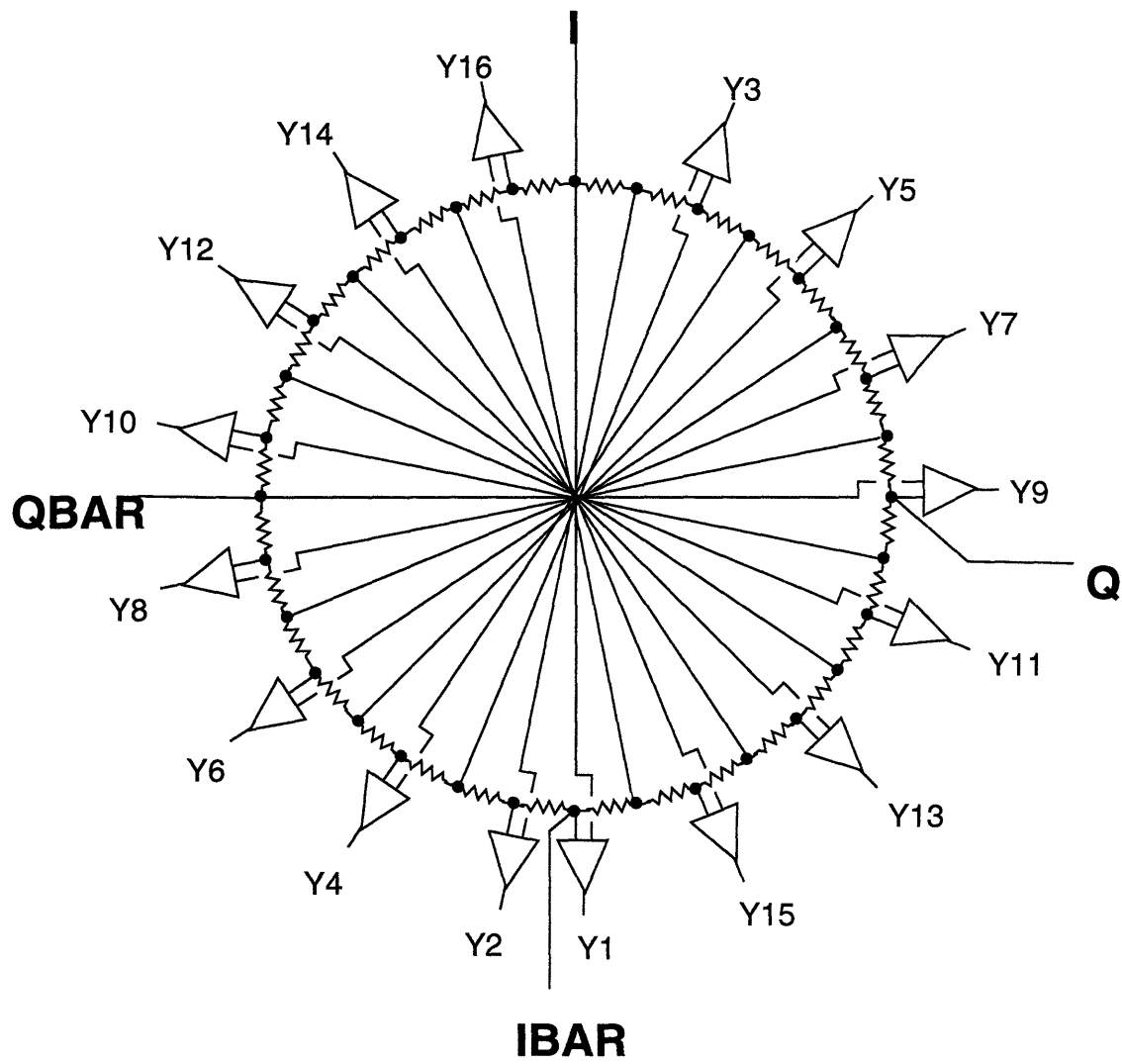


Figure 2-10: Interpolation Ladder and Comparators

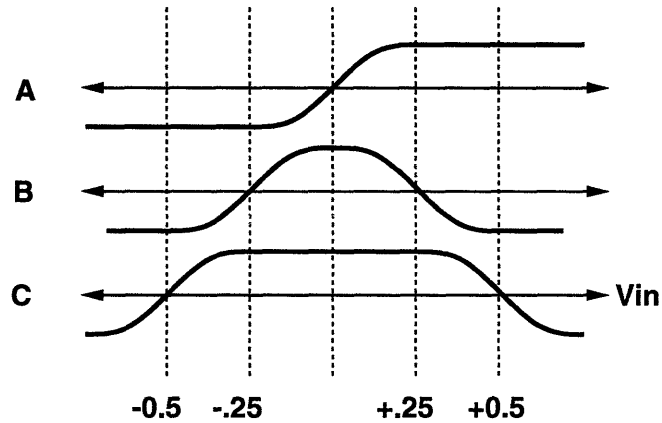


Figure 2-11: Cycle Encoder Folded Waveforms

and MSB sections. (The error correction circuitry will be described in detail in Chapter 4). The second step in the conversion is to detect for overflow (*OF*) or underflow (*UF*) conditions. These conditions occur when the analog input voltage is out of the converter range. For this design, the converter's usable input range is  $\pm 0.5 V$ . If the analog input voltage is greater than  $+0.5 V$  then the *OF* flag is raised and the 6-bit output is set to 111111. With the input less than  $-0.5 V$ , the *UF* flag is raised and the output is set to 000000.

The final step in the conversion process is determining the 6-bit output from the LSB and MSB comparator values. The digital hardware to accomplish this will be described later. The functionality of this hardware is summarized in Table 2.1. In the table, moving from the left to the right represents an increase in the analog input voltage. The MSB and LSB comparator values, *A*, *B*, *C* and  $Y_1 - Y_{16}$  respectively, are displayed versus the analog input voltage. As the table shows, for every possible combination of the LSB and MSB comparator values within the usable analog input range, there is a unique 6-bit binary output  $D_5 - D_0$ . The analog and digital circuits involved in completing the conversion are described in detail in the following chapters.

Vin	-0.5 V	-0.25 V	0.0 V	+0.25 V	+0.5 V
A	0000	0000000000000000	0000000000000000	1111111111111111	1111111111111111
B	0000	0000000000000000	1111111111111111	1111111111111111	0000000000000000
C	0000	1111111111111111	1111111111111111	1111111111111111	1111111111111111
Y1	0000	000000000001111	111111111110000	000000000001111	111111111110000
Y2	1000	000000000000111	111111111111000	000000000000111	111111111111000
Y3	1100	000000000000011	111111111111100	000000000000011	111111111111100
Y4	1110	000000000000001	111111111111110	000000000000001	111111111111110
Y5	1111	000000000000000	111111111111111	000000000000000	111111111111111
Y6	1111	100000000000000	011111111111111	100000000000000	011111111111111
Y7	1111	110000000000000	001111111111111	110000000000000	001111111111111
Y8	1111	111000000000000	000111111111111	111000000000000	000111111111111
Y9	1111	111100000000000	000011111111111	111100000000000	000011111111111
Y10	1111	111110000000000	000001111111111	111110000000000	000001111111111
Y11	1111	111111000000000	000000111111111	111111000000000	000000111111111
Y12	1111	111111100000000	000000011111111	111111100000000	000000011111111
Y13	1111	111111110000000	000000001111111	111111110000000	000000001111111
Y14	1111	111111111000000	000000000111111	111111111000000	000000000111111
Y15	1111	111111111100000	000000000011111	111111111100000	000000000011111
Y16	1111	111111111110000	000000000001111	111111111110000	000000000001111
D5	0000	000000000000000	000000000000000	111111111111111	111111111111111
D4	0000	000000000000000	111111111111111	000000000000000	111111111111111
D3	0000	000000011111111	000000011111111	000000011111111	000000011111111
D2	0000	000011110000111	000011110000111	000011110000111	000011110000111
D1	0000	001100110011001	001100110011001	001100110011001	001100110011001
D0	0000	01010101010101	01010101010101	01010101010101	01010101010101

Table 2.1: Functional Description of Digital Logic

## Chapter 3

# Analog Circuit Design

The previous chapter explained the overall architecture of the folding ADC and the techniques that are used to reduce the number of comparators required for the conversion. This chapter describes the analog circuit blocks required to implement the folding ADC design. These blocks include the folding amplifier, input buffer, resistive interpolation ladder and high-speed comparators.

### 3.1 Folding Amplifier Design

The folding ADC architecture requires fewer comparators than a flash ADC because it provides subranging between a coarse and fine quantizer to attain hardware economy [8]. However, rather than using a coarse quantizer (ADC) and subtraction element to obtain the periodic residue characteristic, a nonlinear analog element with a sawtooth transfer characteristic (as shown in Fig. 3-1) is used. The coarse quantizer detects which cycle the analog input voltage lies, while a fine quantizer uses information from the nonlinear analog element to encode the output. The overall quantizer combines the outputs from the fine and coarse quantizer to produce the final output.

In practice, however, it is difficult to implement a fast, open loop amplifier with a periodic sawtooth transfer characteristic, good linearity and sharp corners [6]. A transfer curve with sinusoid-like characteristics is easier to implement. Bipolar circuits can approximate sinusoid characteristics very well [11] [12]. These circuits make use of emitter coupled pairs to produce the folded waveforms.

The emitter coupled pair differential amplifier is shown in Fig. 3-2. The amplifier consists of



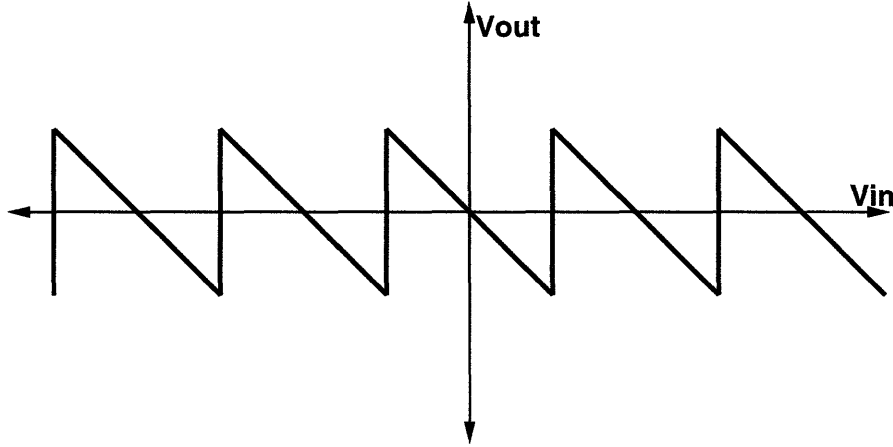


Figure 3-1: A Nonlinear Analog Element Sawtooth Transfer Characteristic

two identical bipolar transistors with the emitters connected to a common current source and the collectors connected to the power supply through equal valued resistors. A DC analysis of the circuit presented in [13] shows that:

$$I_{C1} = \frac{\alpha_F I_{ee}}{1 + e^{\left(-\frac{V_{id}}{V_T}\right)}} \quad (3.1)$$

$$I_{C2} = \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{id}}{V_T}\right)}} \quad (3.2)$$

where  $V_{id} = V_{i1} - V_{i2}$ . The two current waveforms are shown as functions of  $V_{id}$  in Fig. 3-3 with  $V_T = 26mV$ ,  $I_{ee} = 300\mu A$ ,  $\alpha_F = .99$ . With two identical transistors, the current waveforms will cross each other at  $V_{id}=0$ . If some DC bias voltage was introduced at either one of the transistor bases, then the point where the two current waveforms crossed will change. For example, if  $V_{i2}$  was set to  $V_{REF}$  and  $V_{i1}$  varied over the analog input range, then  $V_{id}$  would equal  $V_{i1} - V_{REF}$ . The resulting current waveforms are pictured in Fig. 3-4 with  $V_{REF} = 0.1V$ . This ability to choose the DC crossover point is essential to the design of the folding amplifiers.

Folding amplifiers used in this ADC design have five folds and therefore require five emitter

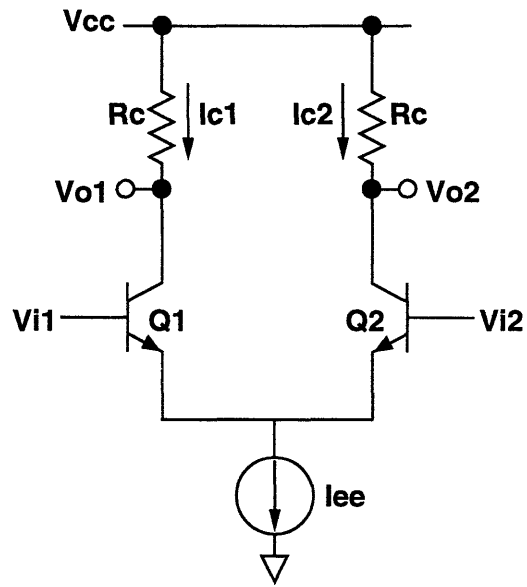


Figure 3-2: An Emitter Coupled Pair Differential Amplifier

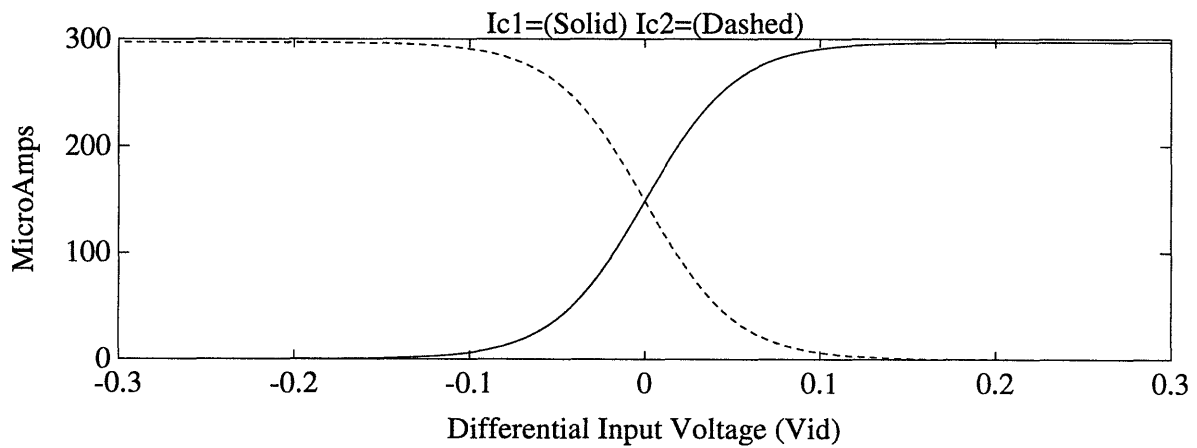


Figure 3-3: Emitter Coupled Pair Collector Currents as a Function of Differential Input Voltage

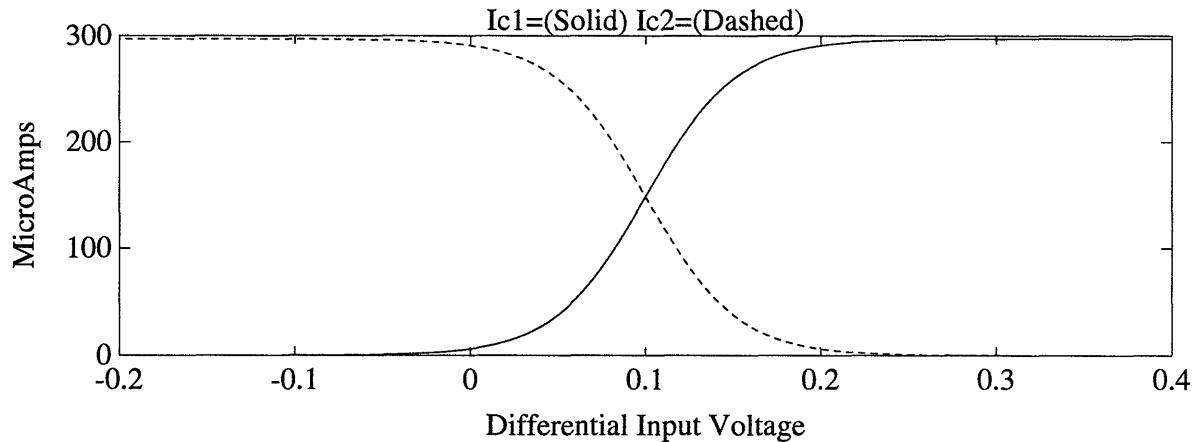


Figure 3-4: Shifted Emitter Coupled Pair Collector Currents

coupled pair amplifiers. These amplifiers are pictured in Fig. 3-5. The base of the left transistor of each amplifier is connected to the input voltage,  $V_{in}$ . The other transistor bases are connected to different DC bias voltages -  $V_1, V_2, V_3, V_4$  and  $V_5$ . The current waveforms that result from this circuitry are illustrated in Fig. 3-6. By summing the appropriate combinations of collector currents, a folded current waveform can be achieved. For example, if the currents  $I_{C1}, I_{C4}, I_{C5}, I_{C8}$  and  $I_{C9}$  are added together, the resulting current waveform varies between  $2I_{ee}$  and  $3I_{ee}$  (as shown at the bottom of Fig. 3-6). The sum of the remaining collector currents will provide the complement of this waveform.

The current summing operation to provide the folded waveform can be implemented with the circuit shown in Fig. 3-7. The circuit consists of five differential pairs whose collectors are combined with alternating polarity to implement a folded transfer characteristic. These alternating connections provide the desired current summing described above. If the base currents of  $Q_{13}$  and  $Q_{14}$  are ignored, we see that:

$$I_{CA} = I_{C1} + I_{C4} + I_{C5} + I_{C8} + I_{C9} \quad (3.3)$$

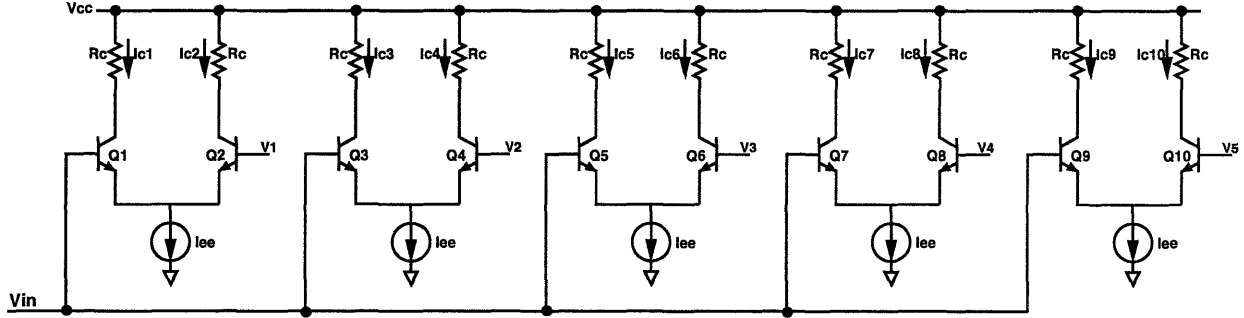


Figure 3-5: Five Emitter Coupled Pair Amplifiers

$$I_{CB} = I_{C2} + I_{C3} + I_{C6} + I_{C7} + I_{C10} \quad (3.4)$$

Substituting equations 3.1 and 3.2 for the collector currents gives

$$I_{CA} = \frac{\alpha_F I_{ee}}{1 + e^{-\left(\frac{V_{in} - V_1}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{in} - V_2}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{-\left(\frac{V_{in} - V_3}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{in} - V_4}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{-\left(\frac{V_{in} - V_5}{V_T}\right)}} \quad (3.5)$$

$$I_{CB} = \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{in} - V_1}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{-\left(\frac{V_{in} - V_2}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{in} - V_3}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{-\left(\frac{V_{in} - V_4}{V_T}\right)}} + \frac{\alpha_F I_{ee}}{1 + e^{\left(\frac{V_{in} - V_5}{V_T}\right)}} \quad (3.6)$$

With these currents, we can now compute the output voltages, since

$$V_{outp} = V_{CC} - I_{CA} R_C - V_{BE13} \quad (3.7)$$

$$V_{outn} = V_{CC} - I_{CB} R_C - V_{BE14} \quad (3.8)$$

Thus, assuming  $V_{BE13} = V_{BE14}$  the fully differential out voltage is

$$V_{outp} - V_{outn} = (I_{CB} - I_{CA}) R_C \quad (3.9)$$

Substituting equations 3.5 and 3.6 into the above equation along with the use of the hyperbolic

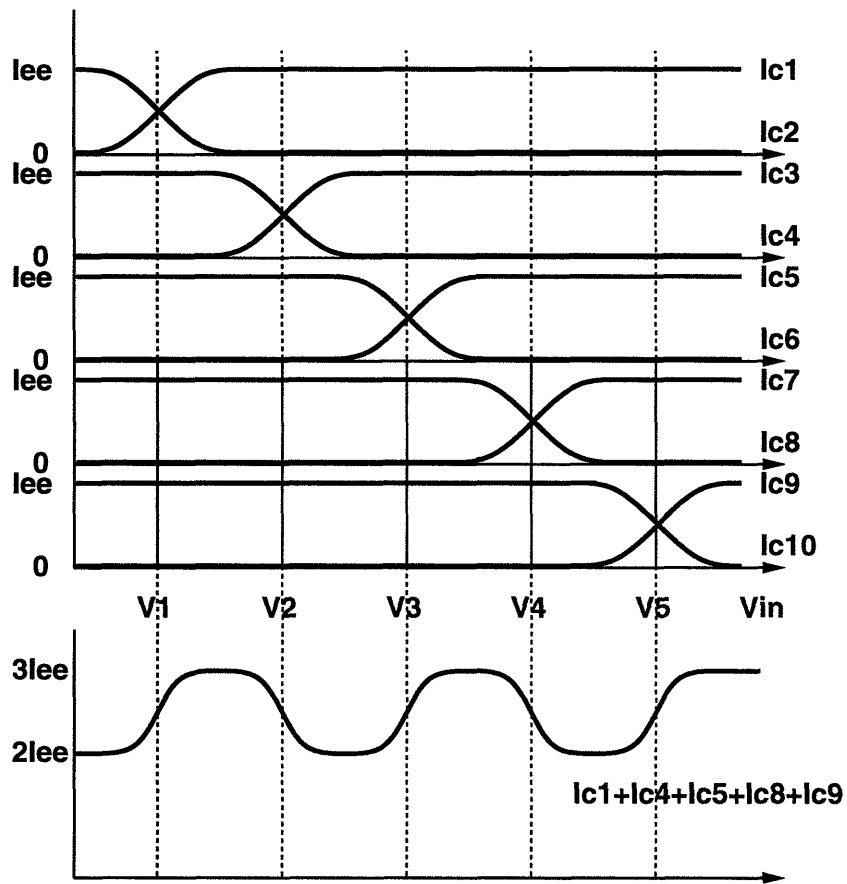


Figure 3-6: Current Waveforms from Biased Emitter Coupled Pair Amplifiers

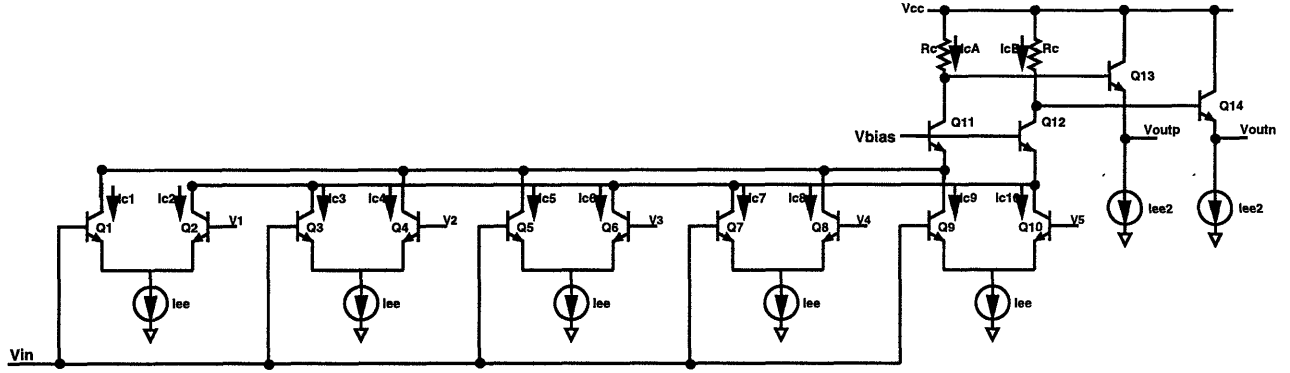


Figure 3-7: Current Summing Folding Amplifier

tangent identity yields

$$\begin{aligned}
 V_{outp} - V_{outn} = & \alpha_F I_{ee} R_C [-\tanh(\frac{V_{in} - V_1}{2V_T}) + \tanh(\frac{V_{in} - V_2}{2V_T}) \\
 & -\tanh(\frac{V_{in} - V_3}{2V_T}) + \tanh(\frac{V_{in} - V_4}{2V_T}) - \tanh(\frac{V_{in} - V_5}{2V_T})] \quad (3.10)
 \end{aligned}$$

The ideal transfer characteristic for the folding amplifier based on this equation is shown in Fig. 3-8 where  $V_T = 26mV$ ,  $I_{ee} = 300\mu A$ ,  $\alpha_F = .99$ ,  $R_C = 1K$  and  $V_1$  through  $V_5$  equal  $-0.5V$ ,  $-0.25V$ ,  $0V$ ,  $+0.25V$ ,  $+0.5V$  respectively.

It is demonstrated in [9], that the high speed response of the circuit undergoes little distortion. The ideal characteristic is compressed vertically and shifted horizontally at high speed. However, since the mutual distance of the zero crossings are unchanged, the folding amplifier performance at  $90 MHz$  is almost as good as it is for low frequency signals. Cascode connected transistors  $Q_{11}$  and  $Q_{12}$  improve the folding amplifier performance further. The folding amplifier has been designed to attain an effective resolution of more than 6 bits up to  $250 MHz$ .

The folding amplifier current sources are implemented with single long channel n-type MOS-FETs. There are several reasons for choosing this current source over an emitter degenerated bipolar transistor current source. Since the design uses a  $3.3 V$  power supply (with a worst case voltage of  $2.8 V$ ), the voltage headroom available for the folding amplifier current sources is lim-

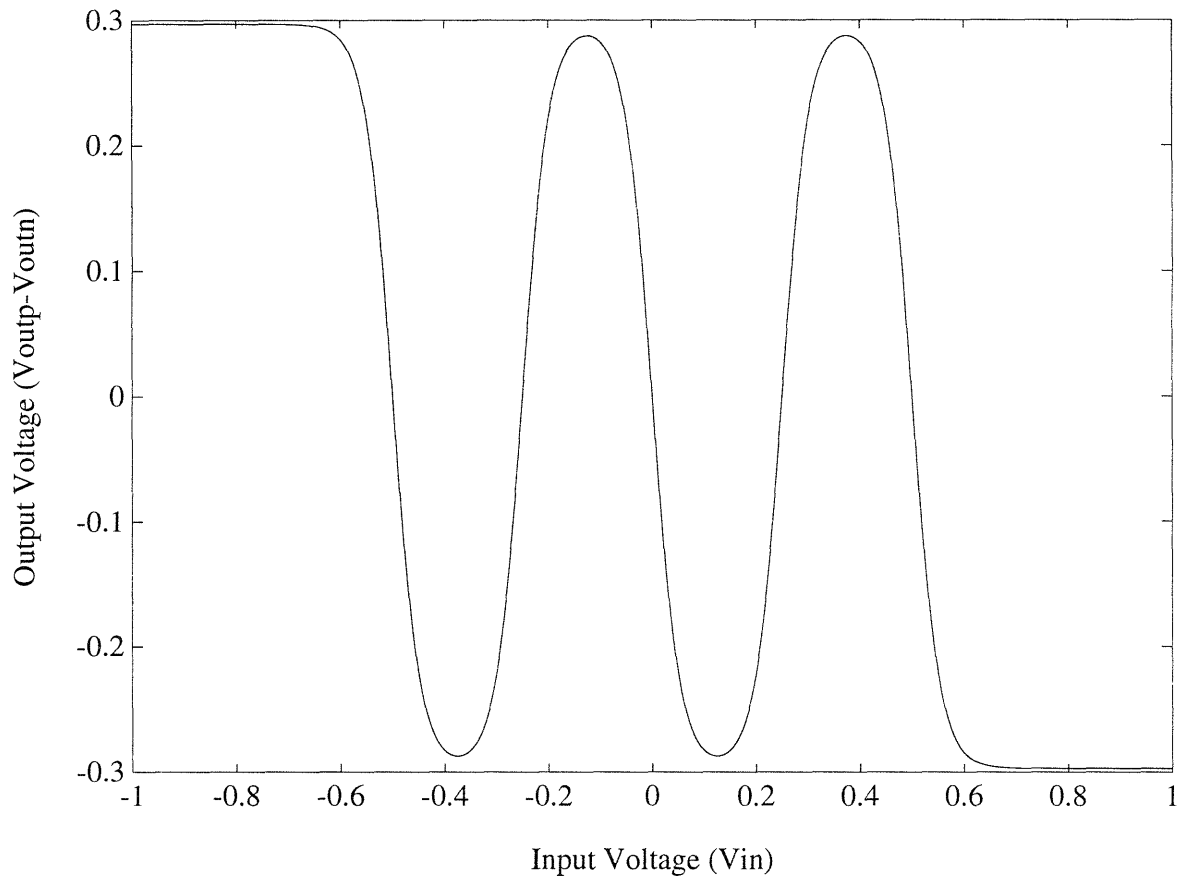


Figure 3-8: Ideal Folding Amplifier Transfer Characteristic

ited (about 0.7 V). This makes it very difficult to bias a bipolar transistor ( $V_{BE} = 0.8V$ ) with an emitter resistor in the constant current region. The biasing can be achieved by removing the emitter resistor. There is no longer any voltage headroom problem since the transistor acts as a constant current source with  $V_{CE}$  as low as 0.2 V. However, the output resistance of the single bipolar transistor current source is poor because of the low Early voltage associated with the process technology used for the design (worst case  $V_A = 20V$ ). This severely limits the folding amplifier's ability to reject common mode signals. This ability is crucial to ADC performance in the mixed-signal environment. The solution to this problem is an n-type MOSFET current source which has an output resistance scalable with the gate length.

As demonstrated in [13], the output resistance of a bipolar transistor and field effect transistor are as follows respectively:

$$r_{oBIPOLAR} = \frac{V_A}{I_C} \quad (3.11)$$

$$r_{oFET} = \frac{L_{eff}}{I_D} \left( \frac{dX_d}{dV_{DS}} \right)^{-1} \quad (3.12)$$

For the folding amplifier design,  $V_A = 20V$ ,  $I_C = I_D = 300\mu A$  and the channel length modulation parameter  $\left( \frac{dX_d}{dV_{DS}} \right) = 0.03$ . Thus

$$r_{oBIPOLAR} < r_{oFET} \quad (3.13)$$

when

$$0.6\mu < L \quad (3.14)$$

With  $L = 2\mu m$ , the CMRR of the folding amplifier is approximately 69 dB.

Besides providing better CMRR, the MOSFET current source easily meets the voltage headroom constraint of 0.7 V. The MOSFET current source will maintain a constant current with a drain-source voltage,  $V_{DS}$ , as low as the gate-source voltage minus a threshold voltage,  $V_{GS} - V_T$ .

The bias generator for the folding amplifier current sources consists of bias current  $I_{BIAS}$  and a diode connected MOSFET with a grounded source. This comprises the typical current mirror and is shown in the complete folding amplifier schematic in Fig. 3-9. From the large signal characteristics of n-type MOSFETs, we see that the current sources will operate correctly with  $V_{DS}$  as low as  $\sqrt{\frac{2I_{BIAS} L}{K' W}} = 0.45V$  with  $I_{BIAS} = 300\mu A$ ,  $W = 40\mu m$ ,  $L = 2\mu m$  and  $K' = 146\frac{\mu A}{V^2}$ . Although, the current matching of the MOSFET current sources is not as good as bipolar current sources with



emitter degeneration, 6-bit resolution is easily achievable using the bias current and geometries listed above.

The current sources for the emitter follower buffers of the folding amplifier are also implemented with n-type MOSFETs. They receive the same voltage bias as the emitter coupled pair current sources but are much wider ( $W = 120\mu m$ ) to sink more current. These buffers are biased with higher currents ( $I_{ee2} = 900\mu A$ ) because of slew rate considerations. This is needed since the folding amplifier actually increases the frequency of the input signal by a factor equal to the number of folds in the amplifier's transfer characteristic. A sinusoidal input signal with a frequency of  $90 MHz$  leaves the amplifier with an effective frequency of  $450 MHz$  ( $90 \times 5$  folds). The output stage is required to slew at  $2\pi fV_a$  (where  $V_a$  is the amplitude of the sinusoid and  $f$  is the maximum input frequency) to buffer the folded waveforms [14]. The maximum slew rate of the folding amplifier output is  $848\frac{V}{\mu s}$  since  $V_a = .3V$  and  $f_{max} = 450MHz$ . A good approximation for the maximum slew rate the emitter follower buffer can achieve is  $\frac{I}{C}$ , where  $I$  is the bias current and  $C$  is the capacitive load on the buffer. From the layout, the average load on the folding amplifiers is approximately  $600 fF$ . Biasing the buffer with  $900\mu A$  allows a maximum slew rate of  $\frac{900\mu A}{600fF} = 1500\frac{V}{\mu s}$ . Therefore, the buffers can handle frequencies of up to  $800 MHz$ .

The complete folding amplifier design is shown in Fig. 3-9. The bias current,  $I_{BIAS} = 300\mu A$ , is from an off chip reference. The total power dissipation of each folding amplifier is  $11 mW$ . The implementation of the input voltage and the DC reference voltages -  $V_1$  through  $V_5$  - will be discussed in the next section.

## 3.2 Input Buffer Design

The input buffer of the folding ADC is pictured in Fig. 3-10. This buffer receives a fully differential input voltage through off-chip coupling capacitors and distributes it across a resistor string reference ladder. The buffer is made up of two identical circuits - one for the positive input and one for the negative input. The benefit of using a differential input buffer of this type is that the base currents of the folding amplifier transistors flowing through the ladder resistance do not cause a bowing of the quantization levels [15].

The DC biasing of the buffers is established by the reference current source,  $I_{ref}$ . This current

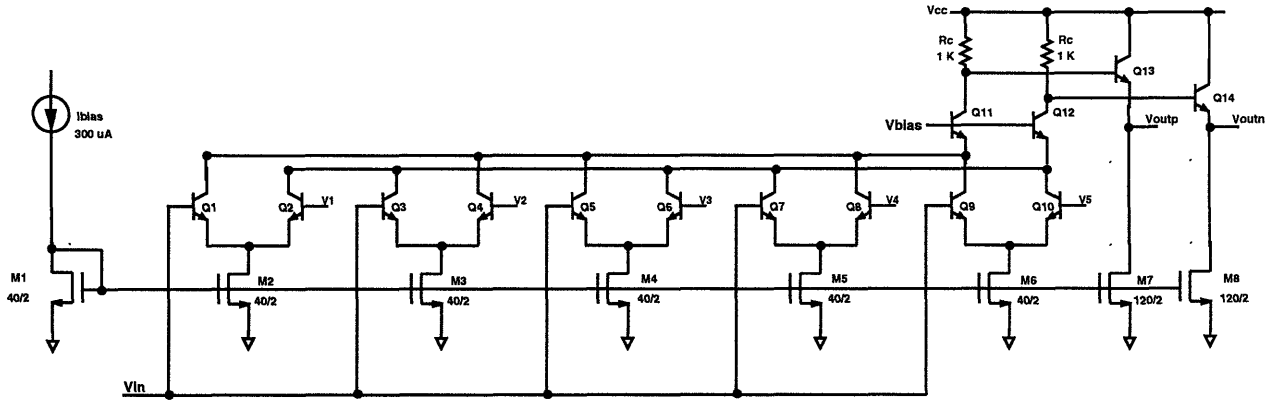


Figure 3-9: Complete Folding Amplifier Implementation

establishes a voltage drop across resistors  $R_1$  and  $R_2$ . From the circuit we can see that:

$$V_a = V_{CC} - R_1(I_{ref} + I_{B1} + I_{B3}) \quad (3.15)$$

$$V_b = V_a - R_2(I_{ref} + I_{B3}) \quad (3.16)$$

$$V_c = V_a - R_3 I_{B1} \quad (3.17)$$

The voltage that is buffered across each string of 9 equal-valued resistors is  $V_c - V_{BE1} - (V_b - V_{BE3})$ . Assuming  $I_1$  is chosen so that  $V_{BE1} = V_{BE3}$ , we see that the voltage across the resistor string is determined to be  $R_2(I_{ref} + I_{B3}) - R_3 I_{B1}$ . By choosing  $R_2 = R_3$ , the voltage across the resistor string is  $R_2 I_{ref}$  since the constraint put on  $I_1$  forces  $I_{B1} = I_{B3}$ . The voltage across each resistor of the strings,  $V_R$ , is  $\frac{R_2 I_{ref}}{9}$ .

The voltage  $R_2 I_{ref}$  needs to be greater than one-half of the full scale range in order to allow the folding amplifiers to properly encode the differential input signal. With the full scale range equal to 1V,  $R_2 I_{ref}$  is set at approximately .5625V. In this converter design,  $R_2 = R_3 = 1K\Omega$  and  $I_{ref}$  was implemented with a trimable emitter degenerated bipolar current source. Thus, the two reference current sources are well matched. The voltage across each resistor in the reference string  $V_R = 62.5mV$ .

For high frequency input signals, it is also necessary to discuss the AC performance of the

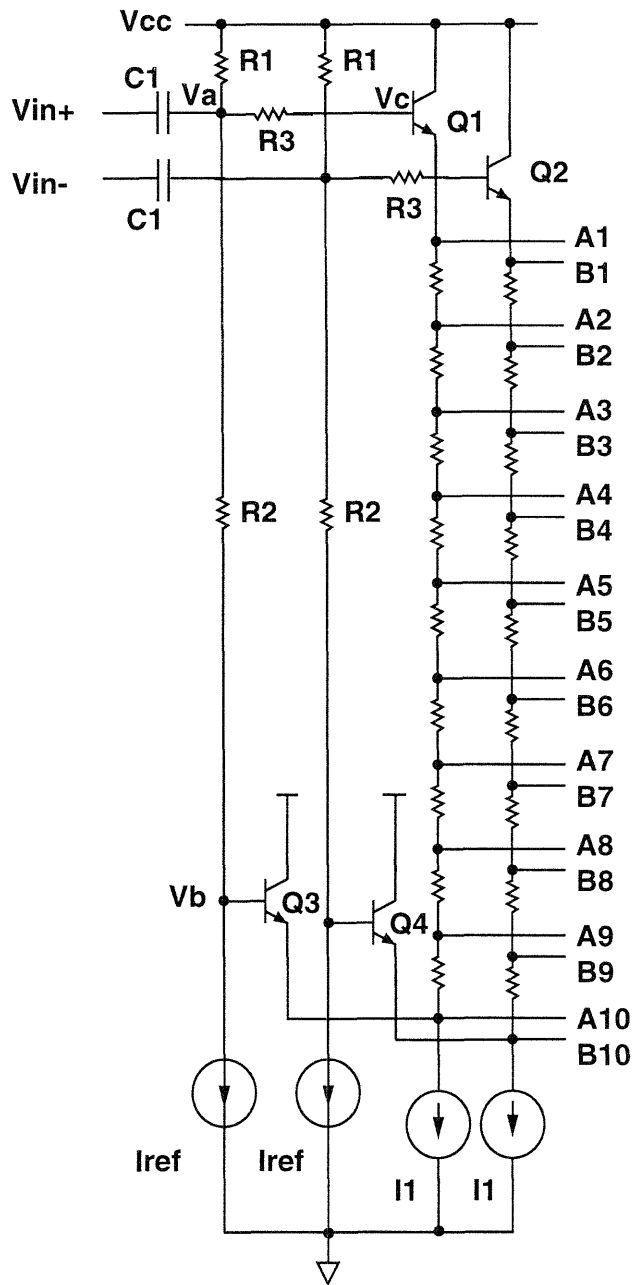


Figure 3-10: Input Buffer Stage

input buffer. From the buffer schematic, we see that any AC waveform coupled through the input capacitors ( $C_1$ ) will be buffered by the emitter follower stages driving the top and bottom of the resistor string. Because of this the complete AC input is available (at each tap) with a different DC offset voltage. Driving both the top and the bottom of the ladder insures there will be no scaling or voltage divider effect on the AC waveform.

In order to convert the analog input signal without significant errors, the signals driven at the emitters of  $Q_1$  and  $Q_3$  need to be in-phase. Insuring the signals are in phase is achieved by matching the delay between the node at  $V_a$  and the bases of  $Q_1$  and  $Q_3$ . Setting  $R_2 = R_3$  already (for DC considerations) is part of insuring a matched delay. The effective capacitive loads at the bases of  $Q_1$  and  $Q_3$  must also be matched. Since the majority of that capacitive load is due to the charge in the bases of the transistors, matching the capacitance can be performed by setting the collector currents equal.

The collector current of  $Q_1$  is set by the voltage drop across the 9 resistor string,  $\frac{.5625V}{9R}$ . Each resistor in the string is  $40\Omega$ . This is a result of the resistor dimensions required to insure 6-bit resolution with the underlying process technology tolerances. The collector current  $Q_1$  is then  $\frac{.5625V}{9(40\Omega)} = 1.5625mA$ . Setting  $I_1$  to double this value achieves considerable matching between the two delay paths. Statistical simulations show that the path delays differ by only  $3ps$ . This is largely due to the fact that the two path delays cannot be completely matched because of the capacitive load that the reference current source,  $I_{ref}$ , adds at the base of  $Q_3$ . This  $3ps$  maximum delay difference is tolerable for a 6-bit resolution. The timing accuracy that a converter must maintain to avoid making a LSB error is

$$dT < \frac{1}{2^n \pi f_{max}} \quad (3.18)$$

where  $dT$  is the converter path delay mismatch,  $n$  is the number of bits of resolution and  $f_{max}$  is the maximum input frequency [16]. For this design,  $n = 6$  and  $f_{max} = 90MHz$ , so  $dT$  has to be less than  $55 ps$ .

The folding amplifiers described in the previous section are driven by the resistor string taps of the input buffer. At taps  $A_1$  through  $A_{10}$ , the positive AC input voltage  $V_{in+}$  is available with different DC offset voltages. The DC voltage at tap  $A_1$  is  $V_c - V_{BE1}$ . The voltage at  $A_2$  is  $V_c - V_{BE1} - 62.5mV$ . The remaining taps each have a  $62.5 mV$  drop associated with them. The taps  $B_1$  through  $B_{10}$  have the same DC offset voltages as the  $A$  taps, but buffer the negative AC

input voltage,  $V_{in-}$ . Each emitter coupled pair of the folding amplifiers is driven by an  $A$  tap and a  $B$  tap. Therefore, the differential input voltage,  $V_{id}$ , of the typical emitter coupled pair amplifier (Fig. 3-2) will be the differential input voltage of the converter  $V_{in+} - V_{in-}$  plus some DC offset voltage determined by the relative distances between the two tap voltages. For example, if an emitter coupled pair is driven by taps  $A_1$  and  $B_{10}$ , then the input voltage is  $V_{A1} - V_{B10}$  which is equal to  $V_{in+} - V_{in-} + 9V_R$  or  $V_{in} + .5625$ . The two collector current waveforms for this emitter coupled pair crossover when the input voltage equals  $-.5625 V$ . Other combinations of taps allow different offset voltages to be created. This technique is used to create the five DC reference voltages required for the five-fold, folding amplifier used in this ADC design.

It should be noted that there are delay mismatches at the tap outputs. This mismatch is caused by the different output resistance at each tap. The output resistance at  $A_1$  is equal to the output resistance of emitter follower stage formed by  $Q_1$ . However, the output resistance at tap  $A_5$  is made up of this resistance and a parallel combination of the resistors above and below that tap - approximately 2.22 times a single string resistor. The delay between output taps is reduced by adding resistors in series between the output taps and the bases of the folding amplifier transistors. (These resistors are not shown in the buffer schematic.) This equalizes the output resistance at the different taps and improves the overall converter performance.

Folding amplifiers with tap connections are shown in Fig. 3-11. These amplifiers use fully-differential inputs. This is unlike the amplifiers discussed in Section 3.1 which use a single-ended input and have all of the left transistors of the differential pairs tied together. The advantage of using a folding amplifier with fully-differential inputs is the ability to reject common-mode input signals such as substrate noise.

The simulated transfer characteristics for these amplifiers is shown in Fig. 3-12. The two waveforms are referred to as  $I$  and  $Q$  or *in-phase* and *quadrature* respectively because the two sinusoidal waveforms are considered to be  $90^\circ$  *out of phase*. Each waveform provides 5 zero-crossings that are needed for the conversion. To increase the converter resolution, more zero-crossings are created using interpolation techniques. The process of interpolation is discussed in the next section.

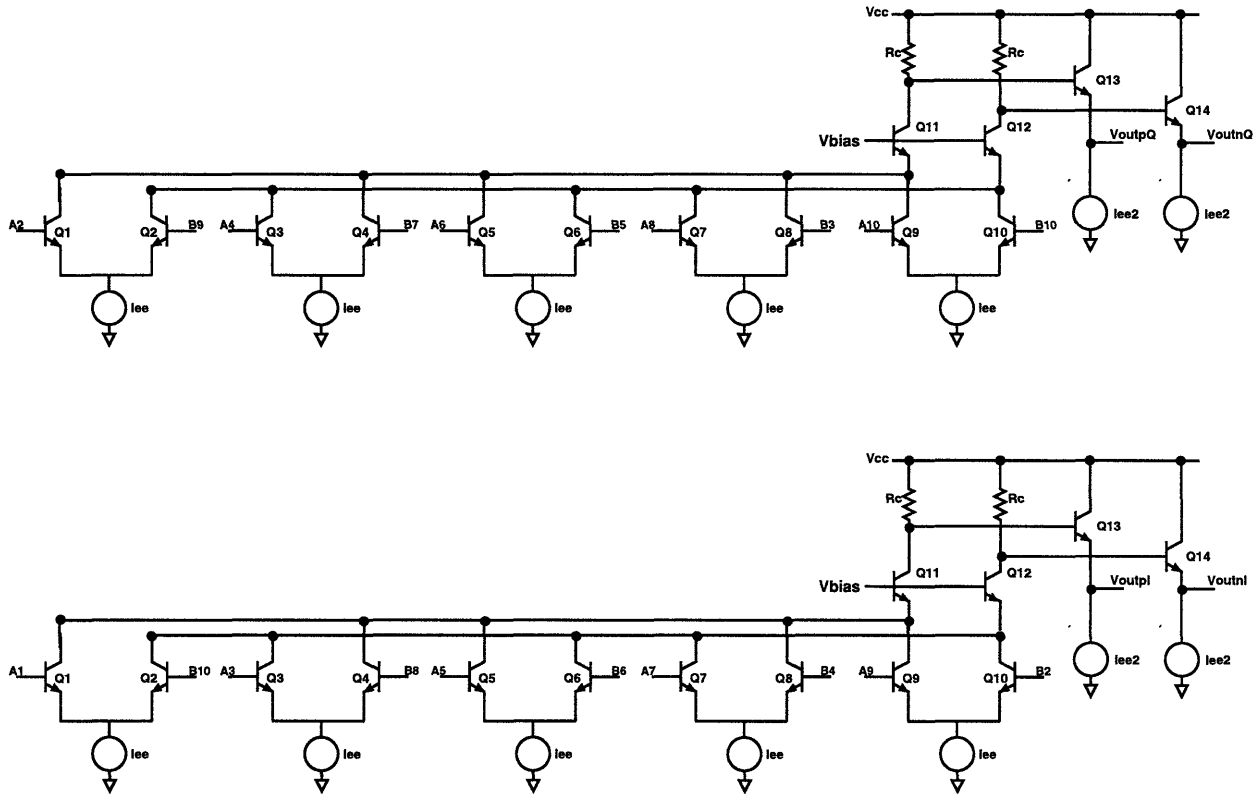


Figure 3-11: Folding Amplifiers with Input Buffer Tap Connections

### 3.3 Interpolation Ladder Design

The folding ADC uses interpolation to produce additional folded waveforms from existing folding amplifier outputs. These additional folded waveforms provide more zero-crossings (or quantization levels) that can be used in the conversion process without increasing the power dissipation of the converter. The interpolation is implemented with a resistor string driven by the outputs of two folding amplifiers. The locations of the zero-crossings of the interpolated waveforms can be determined with simple voltage divider calculations.

This folding ADC design requires 16 folded waveforms. Using the two folding amplifier outputs in Fig. 3-12, we see that 7 waveforms can be interpolated between  $V_{outpI} - V_{outnI}$  (or  $I$ ) and  $V_{outpQ} - V_{outnQ}$  (or  $Q$ ). The other 7 waveforms are interpolated between  $I$  and the inverse of the  $Q$  waveform,  $V_{outnQ} - V_{outpQ}$  (or  $\bar{Q}$ ). Thus, 14 interpolated waveforms and the 2 folding amplifier outputs provide the 16 waveforms necessary for the conversion.

Fig. 3-13 shows one method of interpolating 7 waveforms between  $I$  and  $Q$ . The  $I$  and  $Q$  folding amplifiers drive a string of 8 resistors of value  $R$ . The zero-crossings of the  $I$  and  $Q$  transfer

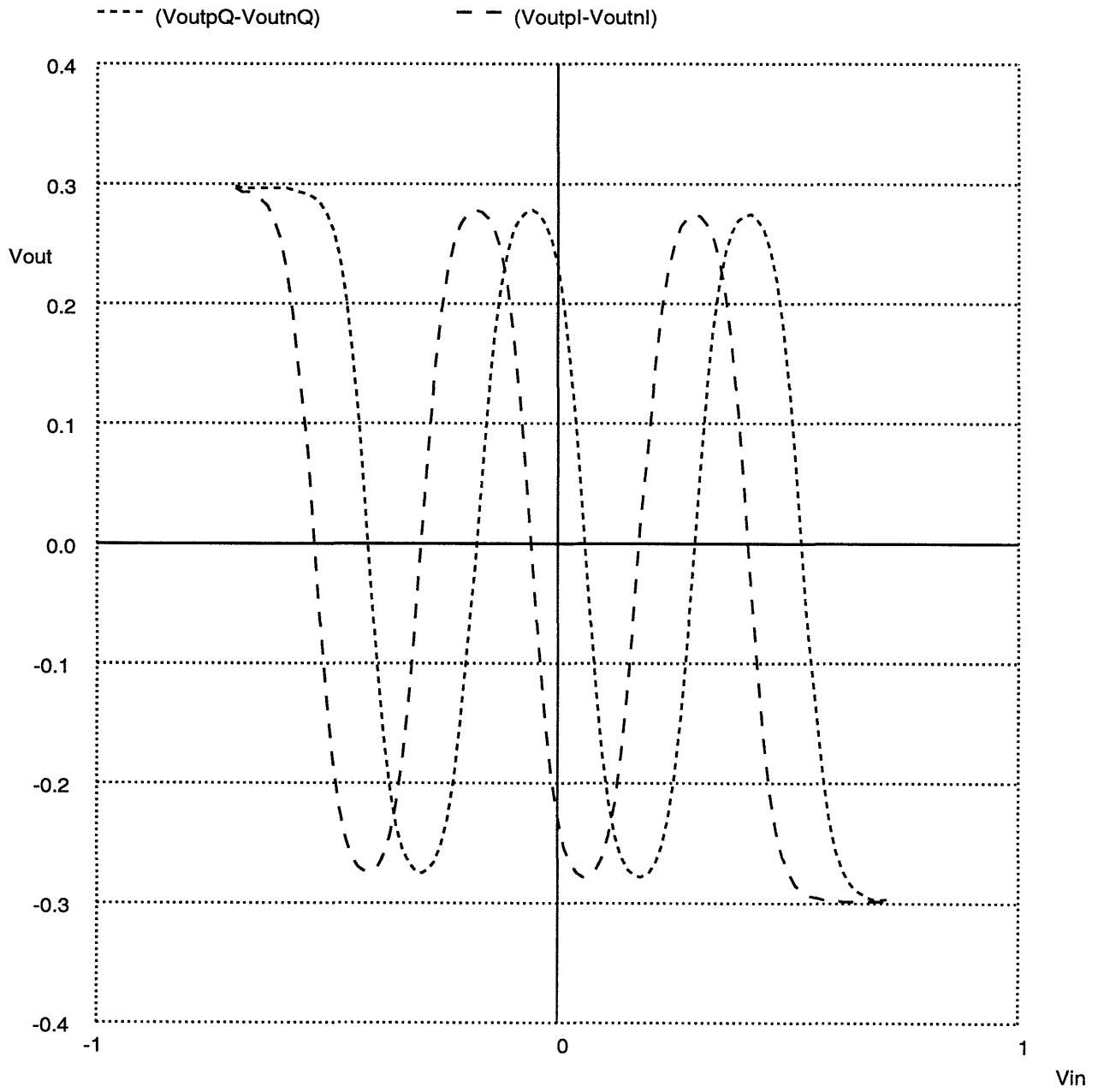


Figure 3-12: Folded Waveforms  $I$  and  $Q$

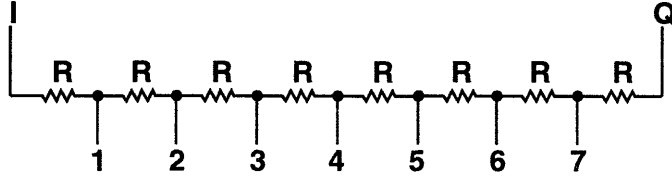


Figure 3-13: Resistive Interpolator

characteristics are separated by  $125\text{ mV}$ , so ideally the tap zero crossings should be separated by an eighth of that voltage or  $15.625\text{ mV} = 1\text{ LSB}$ . However, the nonlinear portions of the folding amplifier characteristics cause errors in the tap zero-crossing locations. These simulated DC errors are illustrated in Fig. 3-14. These DC errors are quite large (almost  $0.8\text{ LSB}$  in some cases). The equal-valued resistor interpolator is therefore unable to provide the 6 bits of resolution required. There are two approaches to correct this problem. The first is to tune the resistor values so that the DC errors are reduced to acceptable levels. The second approach is to drive the interpolator with another folding amplifier at tap 4. Using this technique, less of the nonlinear portions of the folding amplifier waveforms are used, allowing the interpolator to be implemented with equal-valued resistors.

The interpolator with tuned resistors is shown in Fig. 3-15. The structure is the same as the original interpolator with 4 different resistor values. By performing simple voltage divider calculations for each output tap, tuned resistor values can be found which will reduce DC errors. The resistors will have the following values (where  $R_U$  is a unit-valued resistor):

$$R_1 = 10R_U \quad (3.19)$$

$$R_2 = 6R_U \quad (3.20)$$

$$R_3 = 4R_U \quad (3.21)$$

$$R_4 = 3R_U \quad (3.22)$$

$$(3.23)$$



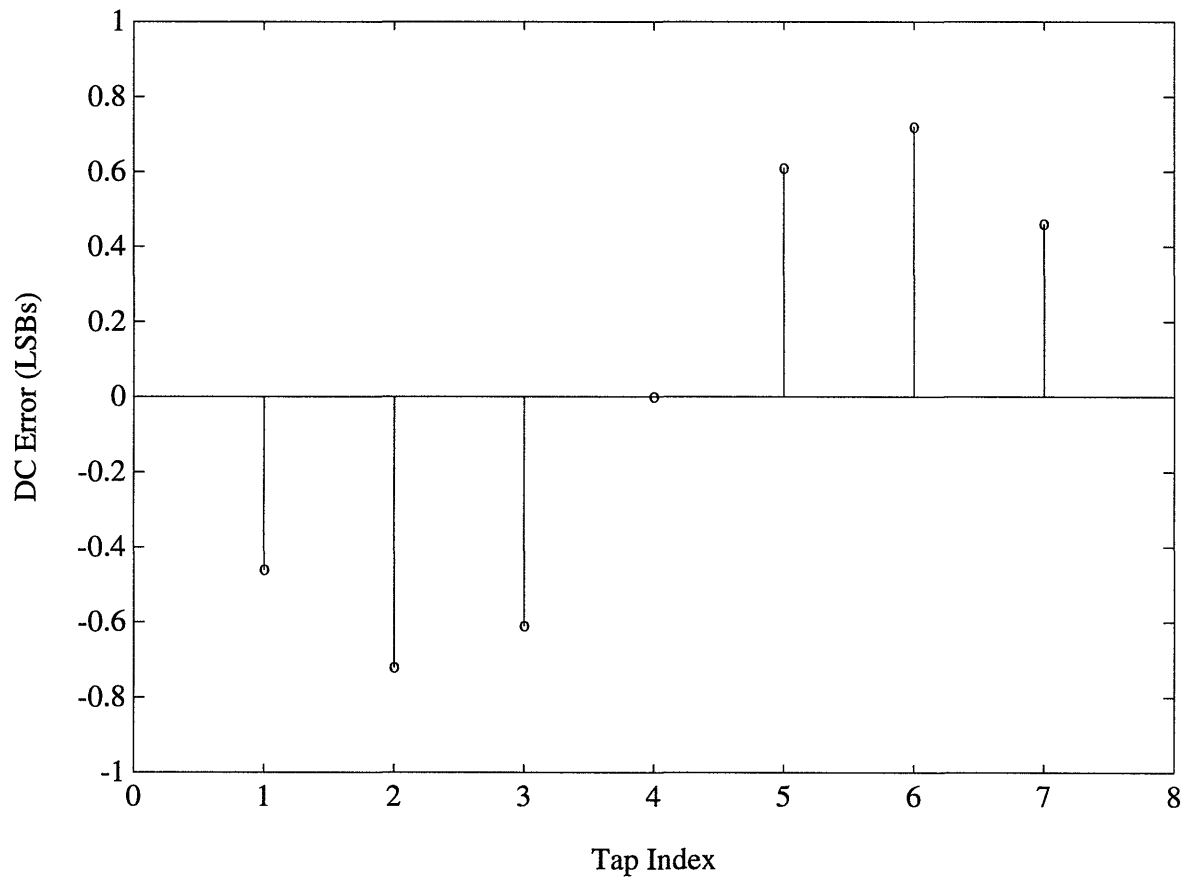


Figure 3-14: DC Errors of Resistive Interpolator

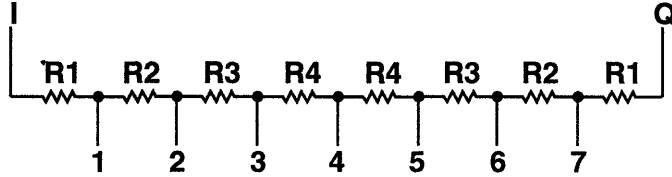


Figure 3-15: Tuned Resistive Interpolator

The DC errors for this interpolator are pictured in Fig. 3-16. The DC errors drop to less than 0.15 LSB with the tuned resistor approach. This amount of error is acceptable in this application. However, the tuned resistor approach has problems in compensating for timing mismatches associated with it. These problems will be discussed later in this section.

The second approach proposed to reduce the DC errors of the original interpolator is to add more folding amplifiers to the design. For example, a folding amplifier which has a waveform that crosses zero at points in between the  $I$  and  $Q$  zero-crossings can be used to drive tap 4 of the equal-valued resistor interpolator. With this architecture, only 3 waveforms are interpolated between 2 folding amplifier outputs. This method uses less of the nonlinear portions of the folding amplifier outputs, so the DC errors of the equal-valued resistor interpolator will be smaller. The DC errors for this approach are shown in Fig. 3-17. The errors are about two times smaller than those in the tuned resistor approach. This reduction required additional folding amplifiers which would increase the power dissipation of the converter. However, using this method allows the dynamic performance of the converter to be improved.

Because the interpolation network is driven from voltage-follower stages, the output impedance of the network which drives the comparators varies from tap to tap. The capacitive load of the comparator input stages on the interpolation network results in a variable signal delay which can easily vary more than what is allowed in this system (55 ps). Fig. 3-18 demonstrates how this problem is corrected. The interpolation network is driven by folding amplifiers at  $I$ ,  $J$  and  $Q$ . The zero-crossings of the  $J$  waveform lie halfway between those for  $I$  and  $Q$ . Additional resistors of  $R$  and  $\frac{R}{4}$  are added in series with the outputs to make all output impedances equal to  $R$ . All tap

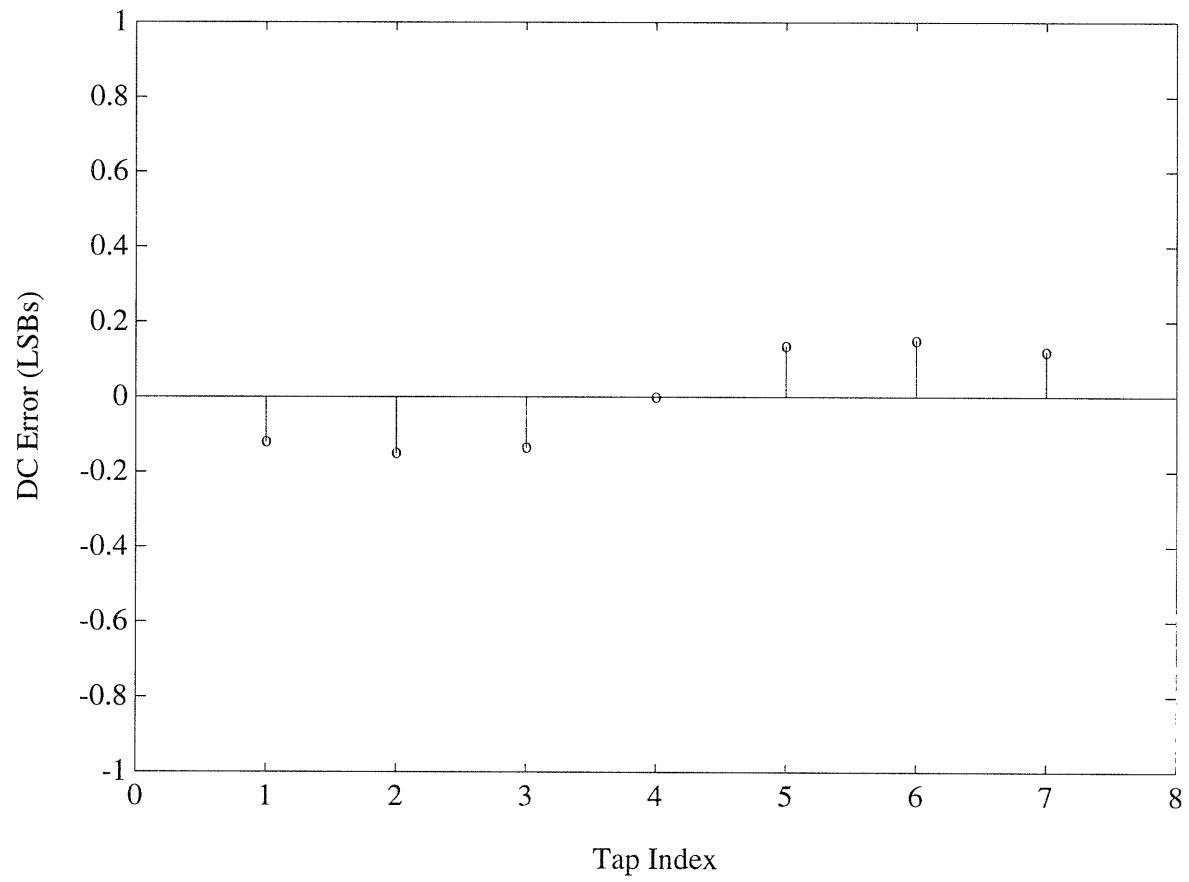


Figure 3-16: DC Errors of Tuned Resistive Interpolator

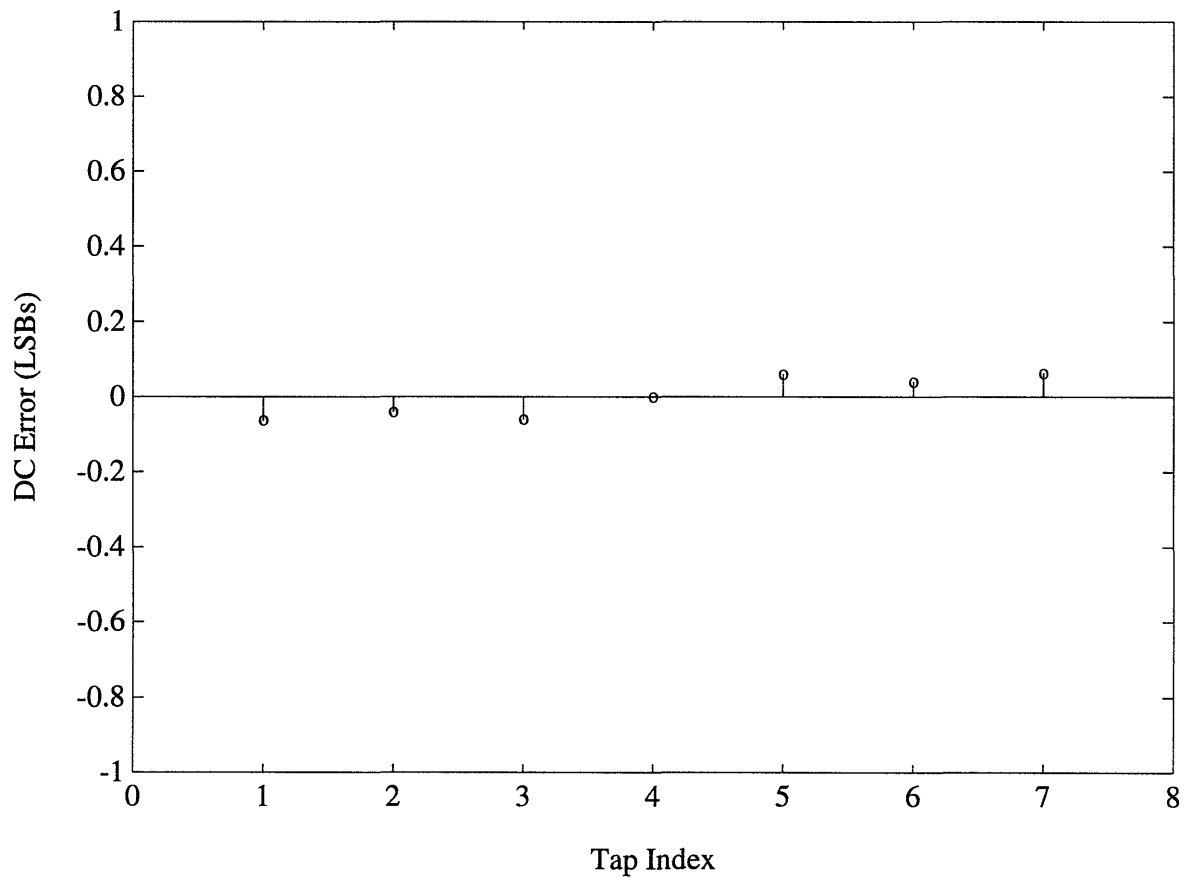


Figure 3-17: DC Errors of Interpolator 3 Folding Amplifiers

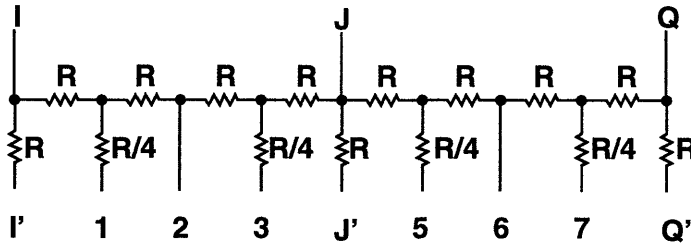


Figure 3-18: Resistive Interpolator with Delay Matching

outputs now have an equal delay [16].

This delay matching can also be performed with the tuned resistor interpolator. However, the ratios required for the series resistors are more difficult to implement with a single unit resistor cell. In addition to this, the tuned resistor interpolator has a larger resistance across the folding amplifier outputs than the interpolator that uses several folding amplifiers. This leads to other uncorrectable timing errors. For example, in the tuned resistor interpolator, the  $I$  signal will always reach tap 1 before the  $Q$  signal because it travels through a shorter network of interpolation resistors and parasitic capacitors than the  $Q$  signal. Such a mismatch in delays is tolerable when the period of the input signal is much longer than the delays. At high speeds, however, the delays are less tolerable and degrade converter performance. This will be demonstrated in the results. This error is less of an issue in the multiple folding amplifier interpolator because the resistance across the folding amplifier outputs is much smaller resulting in smaller delay mismatches.

### 3.4 Comparator Design

The high-speed comparator used in this design is shown in Fig. 3-19. The comparator consists of a pair of input emitter followers, a preamp, a second emitter follower stage and a latched comparator amplifier with emitter follower outputs. The latched comparator amplifier (transistors  $Q_7$  through  $Q_{12}$ ) is controlled by the LATCH and COMPARE signals. (The COMPARE signal is from the output of an inverter driven with the LATCH signal.) The comparator has two modes of operation - a compare mode and a latch mode. In the compare mode (LATCH is low), the comparator acts like an amplifier. In this mode, transistor  $M_2$  is cutoff, so the regenerative latch is disabled. When

the LATCH signal rises, COMPARE goes low and the comparator latches the analog signal. Note that the latched comparator amplifier uses two identical voltage controlled current sources ( $M_1$  and  $M_2$ ) that determine the mode of operation. Each current source draws a current of  $I_L$  when active.

The comparator uses bipolar transistors rather than MOSFETs in the signal path. Since the transconductance of a bipolar transistor is much larger than that of a MOSFET at the same bias current, a bipolar comparator can achieve high-speed operation at a lower power than a MOSFET comparator [17]. Another benefit of the bipolar comparator is that offset cancellation is unnecessary for a converter resolution of 6 bits. Through Monte Carlo simulations, the offset voltage of the comparator was found to be  $1.6\text{ mV}$ . This is a small fraction of a single LSB ( $15.625\text{ mV}$ ). A MOSFET comparator would have an offset voltage of at least  $10\text{ mV} = .64\text{ LSB}$ . Such a comparator would require offset cancellation.

The comparator input is buffered with emitter follower transistors,  $Q_1$  and  $Q_2$  to insure the input currents to the comparator remain constant. With constant input currents, the possibility of a DC offset error caused by unequal base currents flowing through the delay matching resistors of the interpolator is eliminated. Such an error can occur if the comparator input were an unbuffered differential pair. The buffer circuit is illustrated in Fig. 3-20. With emitter follower inputs, there will be an equal  $\frac{I}{\beta+1}R$  drop across the signal delay matching resistors of the interpolator. Thus, the differential input remains unchanged.

The comparator preamplifier is an emitter couple pair amplifier composed of transistors  $Q_3$  and  $Q_4$ . The preamplifier performs two functions. It isolates the interpolation stage from the comparator latch and improves the comparator recovery time. The isolation prevents any *kickback* noise from the clock line or latched signal line to travel back to the interpolation ladder and interfere with the input voltages of other comparators. The preamp also improves the recovery time by boosting the overdrive of the comparator stage at high frequencies [18]. The preamplifier is actually a key factor in reducing the comparator power dissipation [19]. A comparator with preamplification can achieve the same response time as a single stage latched comparator and dissipate less power. A study of the comparator response time was completed to demonstrate this.

The study results in Fig. 3-21 show how the comparator response time is related to the regenerative latch current,  $I_L$ . The experiment was repeated for several different preamplifier gains ( $A_P$ ). The results show that the response time improvement diminishes with a preamplifier gain greater

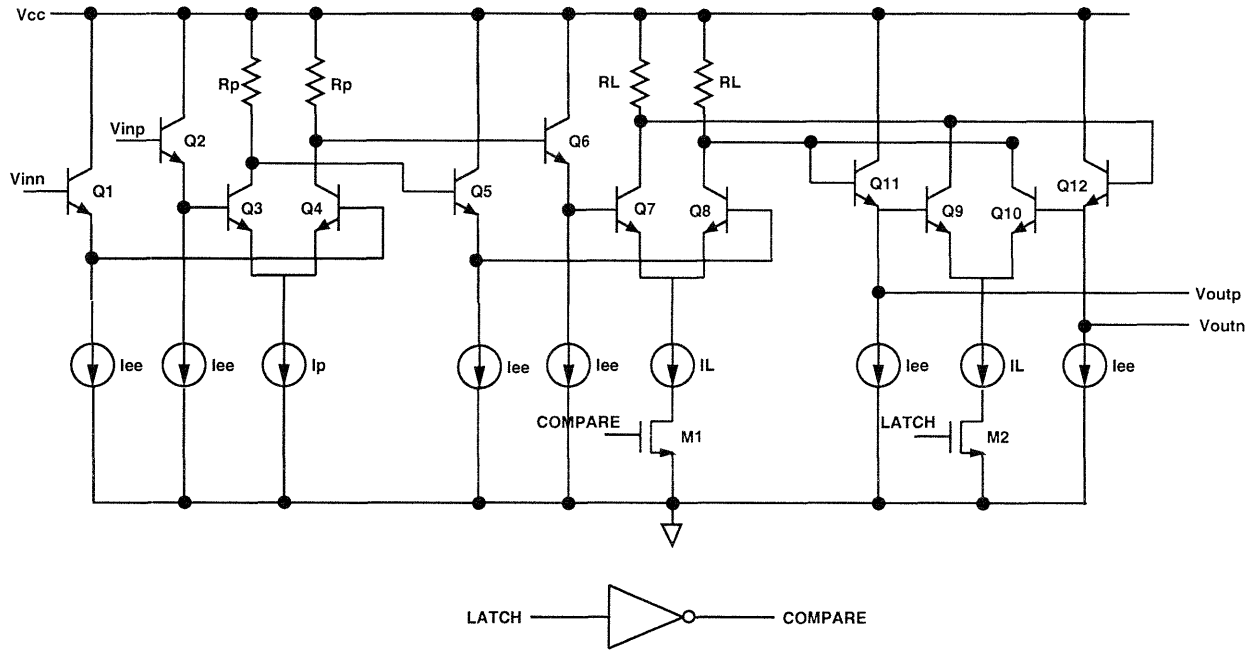


Figure 3-19: High Speed Comparator

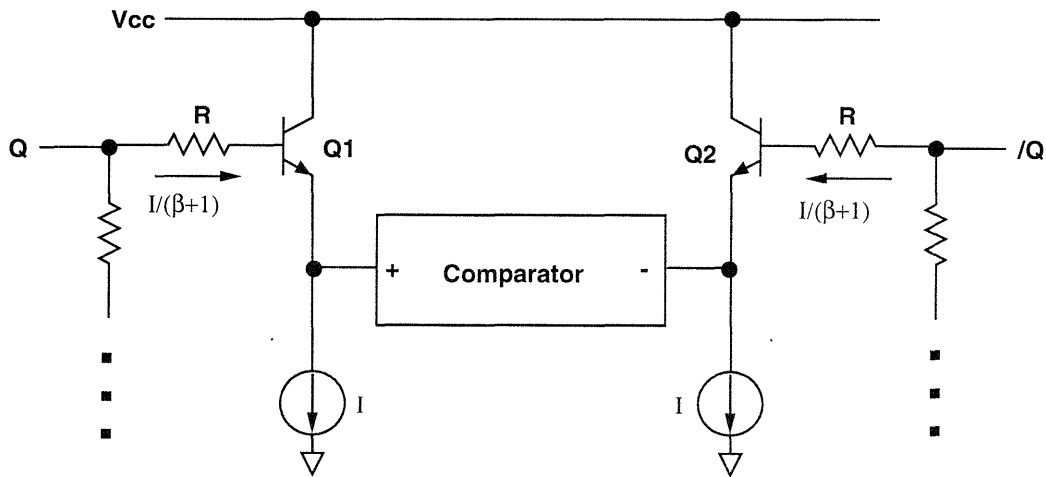


Figure 3-20: Emitter Follower Input Stage

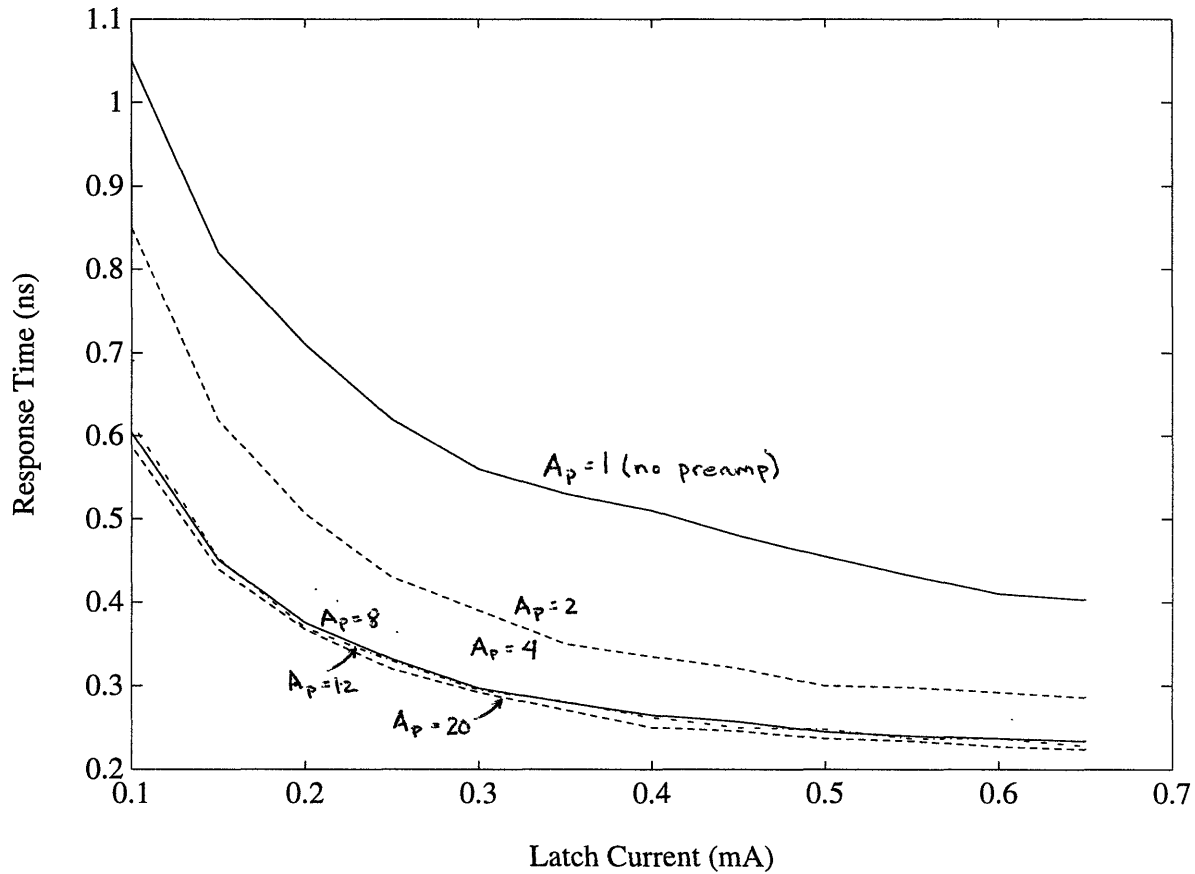


Figure 3-21: Comparator Response Times for Different Preamp Gains

than 8. For this reason, the preamplifier gain is set to 8. This provides a design point from which the comparator design can begin.

To achieve a conversion rate of 180 MHz, the comparator response time was chosen to be less than 300 ps. This would provide adequate time for the comparator outputs to settle and drive the digital encoding logic. With this constraint and  $A_P = 8$ , the latch current should be about .500 mA. With this information the required preamplifier current  $I_P$  can be found using the optimization equation from [19] which states:

$$I_P = \frac{2V_T I_L A_P}{nE_O} \quad (3.24)$$

where  $E_O$  is the comparator differential output signal level and  $n$  is the ratio of capacitive loads



on the preamp and latched comparator amplifier. A sufficient logic level for the comparator is  $E_O = 0.4V$ . The capacitor ratio is between 1.5 and 2. The preamp current is calculated to be  $.300\text{ mA}$  for  $n = 1.6$ . With differential logic levels equal to  $0.4\text{ V}$  for both the preamplifier and latched comparator amplifier, the load resistors values are  $R_P = \frac{0.4}{I_P} = 1.33K$  and  $R_L = \frac{0.4}{I_L} = 800\Omega$ . It should be noted that these current and resistor values insure that the bipolar transistors do not go into saturation. For example, consider  $Q_7$  when the comparator is in COMPARE mode. The highest voltage possible on its base is  $V_{CC} - V_{BE6}$ . Under these conditions all of the latch current is flowing through  $Q_7$  so that its collector voltage is at  $V_{CC} - 0.4V$ . The base-collector voltage of  $Q_7$  is  $-0.4\text{ V}$  for  $V_{BE6} = 0.8V$ . The comparator's performance is enhanced with this non-saturating by design concept.

When considering some second order effects, the optimal comparator design is met with the following component values -  $R_P = 1.6K$ ,  $R_L = 710\Omega$ ,  $I_P = .350\text{mA}$ ,  $I_L = .560\text{mA}$ . The emitter follower bias currents are all set to  $.100\text{ mA}$  due to slew rate considerations. For reasons similar to the folding amplifiers, the current sources are implemented with n-type MOSFETs. The comparator has a power dissipation of  $5\text{ mW}$  and a bandwidth of  $600\text{ MHz}$ . The simulated response of the comparator to a  $90\text{ MHz}$ ,  $10\text{ mV}$  peak-to-peak sine wave with a  $180\text{ MHz}$  clock rate is shown in Fig. 3-22.

A MOSFET sense amplifier (Fig. 3-23) is used to convert the comparator output signals to CMOS voltage levels. The amplifier is made up of two cross-couple inverters ( $M_4, M_5, M_6, M_7$ ), two precharge transistors ( $M_1, M_2$ ), an evaluate transistor ( $M_3$ ) and input transistors ( $M_8, M_9$ ). The precharge-evaluate control signal (P/E) is a delayed version of the LATCH signal. The operation of the sense amp is as follows. With the P/E signal low, nodes  $OUT$  and  $\overline{OUT}$  are precharged high through transistors  $M_1$  and  $M_2$ . During this time, the comparator is acting like an amplifier so the sense amplifier inputs vary. The output nodes are not affected due to the large drive on the precharge transistors. When LATCH goes high, the comparator outputs are latched and spread by  $0.4\text{ V}$ . After two inverter delays the evaluate transistor is activated. This enables the cross-coupled inverters to latch. The latched value is determined by the voltages on the gates of the input transistors. The input transistors force charge onto the nodes of the cross-coupled inverters. This causes an imbalance and forces the  $OUT$  node to go to  $V_{DD}$  or ground. No offset cancellation is required with this sense amplifier because by the time it evaluates, the input voltages differ by

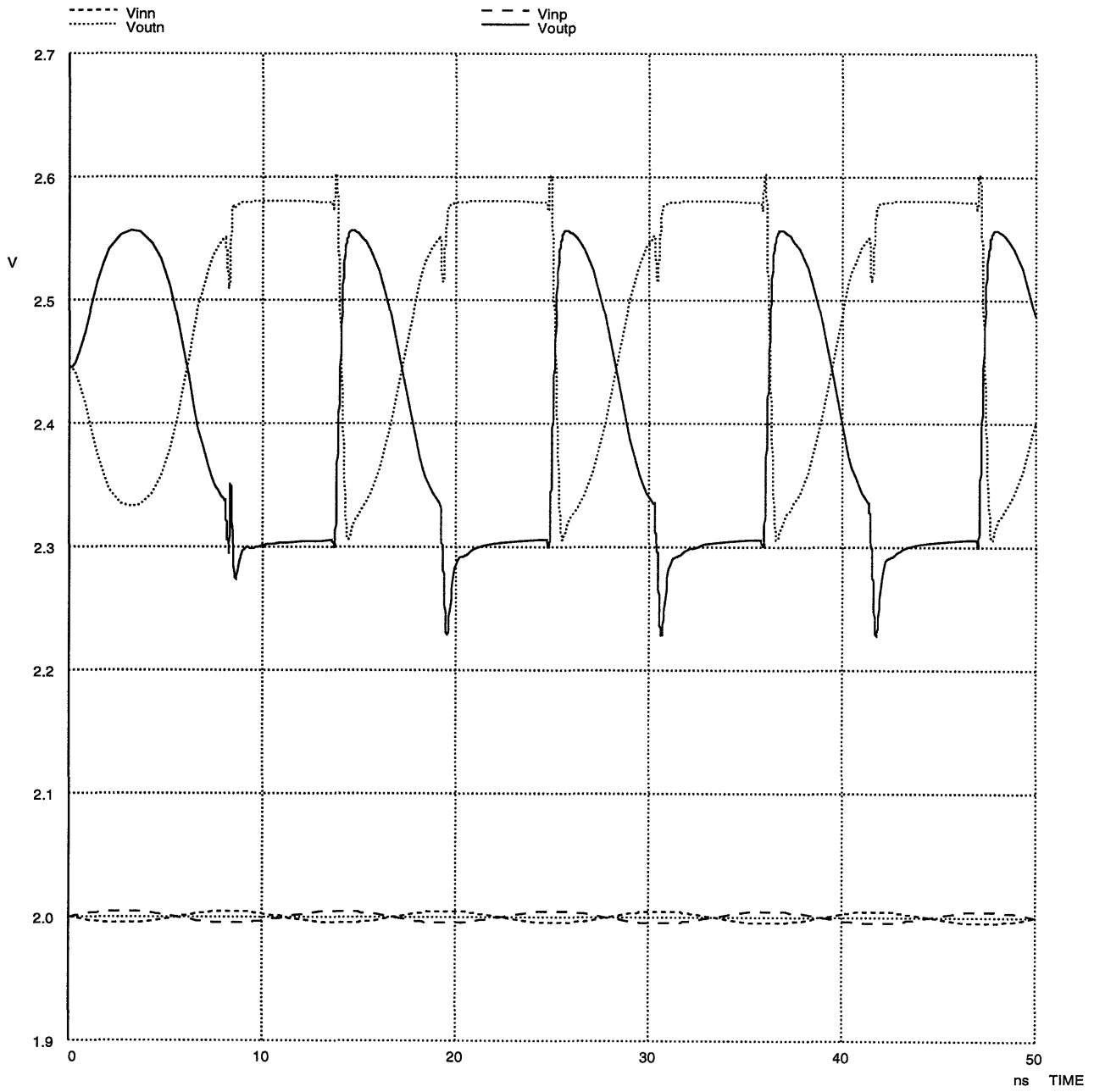


Figure 3-22: Simulated Comparator Response to 90 MHz Sinusoid

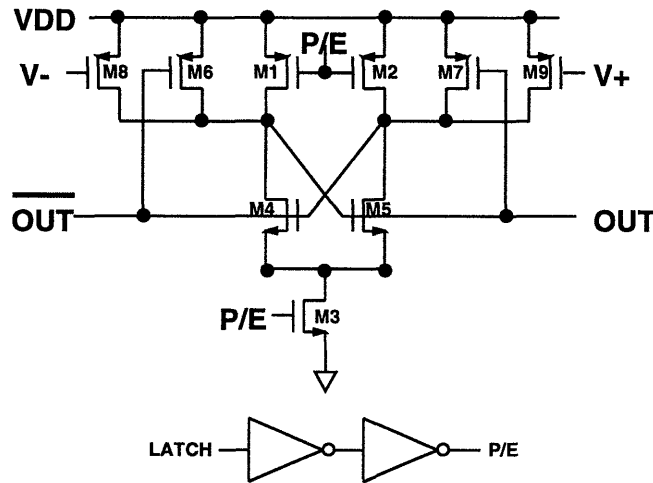


Figure 3-23: MOS Sense Amplifier

0.4 V. This large voltage difference also alleviates the need for any critical device ratios that would normally be required for operation. In fact, the sense amplifier will perform adequately in this ADC design with minimum-sized devices. Using larger device widths improves the comparator performance further.

The sense amplifier in-turn drives an RS flip-flop. This flip-flop acts as the slave to the sense amplifier latch (master). The RS flip-flop is implemented with two cross-coupled CMOS NAND gates. The comparator system is illustrated with block diagrams in Fig. 3-24. Simulated waveforms for the system are shown in Figs. 3-25 and 3-26. These simulations test the overdrive recovery of the comparator.  $V_{inn}$  was held at a constant 2.000 V while  $V_{inp}$  varied. In Fig. 3-25,  $V_{inp}$  switched from 2.100 V to 1.999 V. Therefore, the differential comparator input voltage ranged between 100 mV and -1 mV. The simulations show that it takes 1.5 ns to produce valid outputs from the RS-latch of the comparator after the LATCH signal goes high. For a 180 MHz conversion rate, there would still be an adequate time to perform digital processing on the signal. In Fig. 3-26, the differential input between 100 mV and 1 mV. As the simulations show, the RS latch output signal

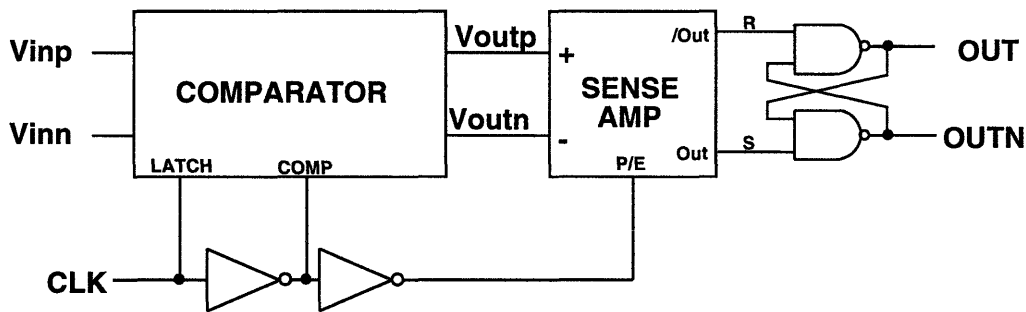


Figure 3-24: Complete Comparator System

is not affected.

### 3.5 Analog Design Summary

The complete analog system is summarized in Fig. 3-27. The figure shows the two separate paths used in the folding ADC. The LSB path consists of 4 (or 2 for a tuned resistor interpolator) folding amplifiers ( $A_1$  through  $A_4$ ), interpolation resistors and 16 high-speed comparators. The folding amplifiers are driven by 10 of the input buffer taps. In turn, the folding amplifiers drive the interpolation network which provides 32 inputs (16 fully differential inputs) to the 16 high-speed comparators. The MSB path is made up of 3 folding amplifiers ( $A_5$  through  $A_7$ ) with dummy inputs, delay matching resistors and 3 high-speed comparators. The delay matching resistors in the cycle encoder are included to avoid any delay mismatches between the LSB and MSB stages. The total power dissipation of the analog section of the folding ADC are summarized in Table 3.1. For this design, the total power dissipated in the analog section is 197.8 *mW*.

The outputs of the 19 comparators are processed by the digital logic to produce a 6-bit output. To achieve the 6-bit output, the digital logic has to detect and correct bubble errors, timing mismatch errors and overflow and underflow conditions. These operations are described in Chapter 4.

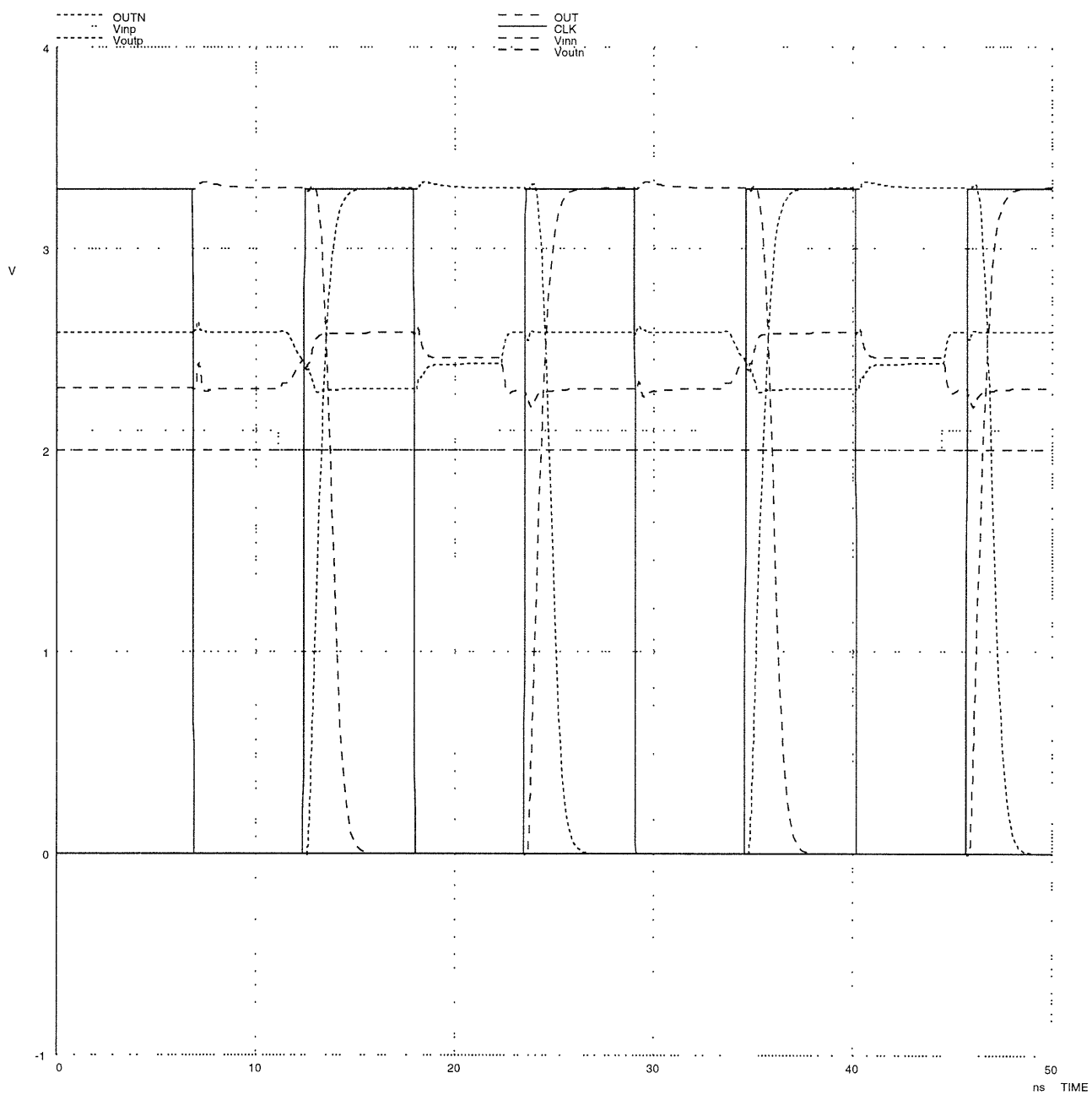


Figure 3-25: Input Overdrive Recovery Test - Diff. Input 100 mV to -1 mV

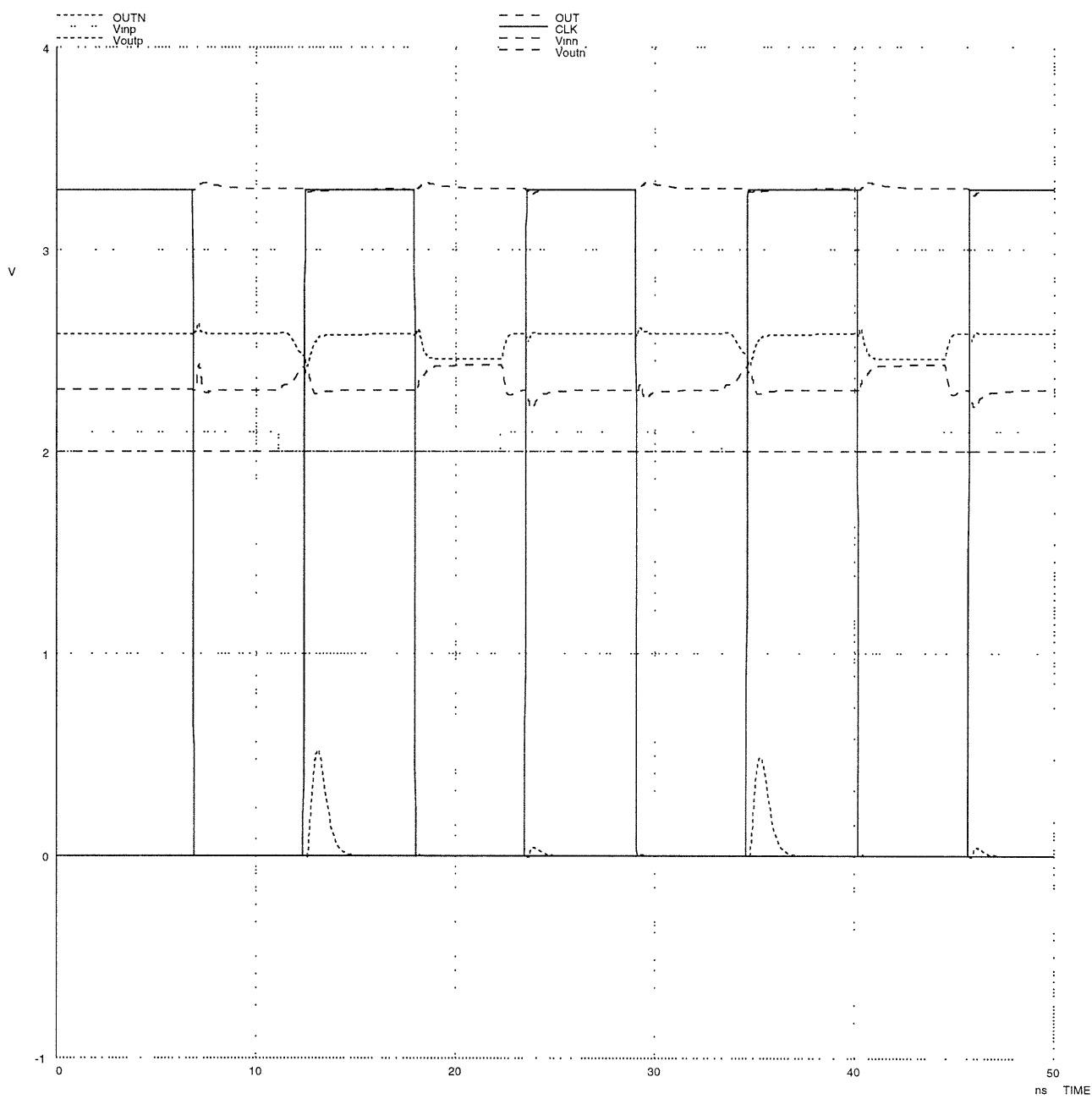


Figure 3-26: Input Overdrive Recovery Test - Diff. Input 100 mV to +1 mV

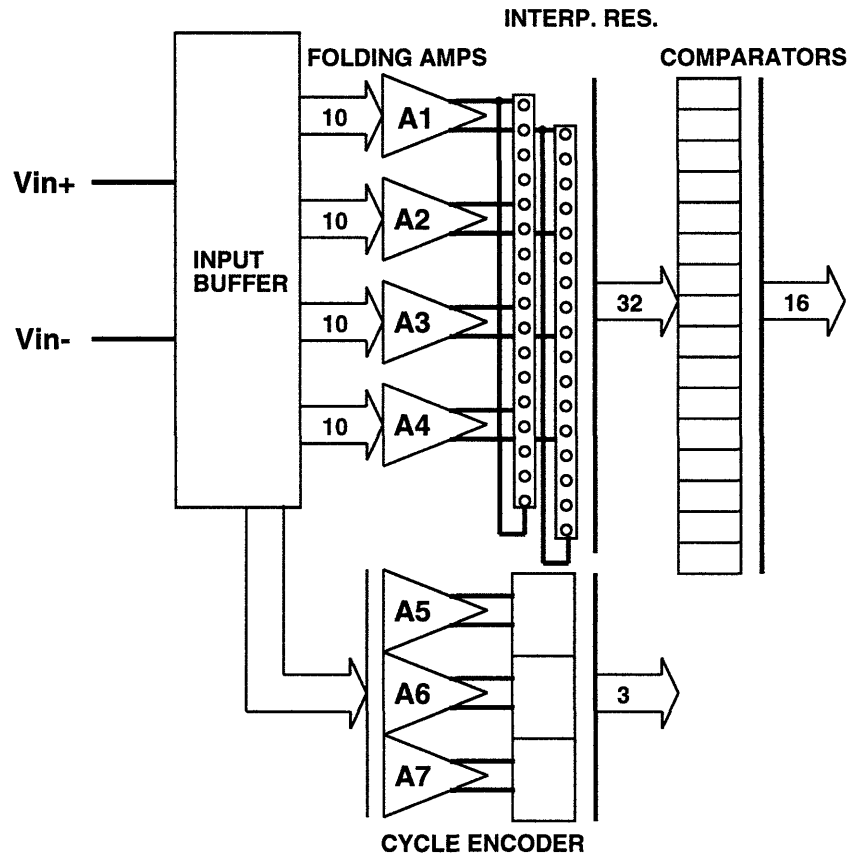


Figure 3-27: Overall Analog Circuit Summary

Table 3.1: Power Dissipation for Various Analog Circuits

Analog Circuit	No. Required	Unit Power	Total Power Dissipation
Input Buffer	1	6.8 <i>mW</i>	6.8 <i>mW</i>
Folding Amplifier	7	11.0 <i>mW</i>	77.0 <i>mW</i>
Comparator	19	6.0 <i>mW</i>	114.0 <i>mW</i>
<b>TOTAL</b>			197.8 <i>mW</i>

## Chapter 4

# Logic Design and Timing

### 4.1 Encode Logic

The encode logic is used to convert the values of the 19 comparator outputs into the binary-coded 6-bit output of the ADC. Fig. 4-1 shows the ideal latched comparator values and the corresponding binary output for voltages in the input range  $\pm 0.5V$ . The MSB of the digital output,  $D_5$  is determined by the outputs from the cycle encoder. The 5 LSBs of the digital output,  $D_4$  through  $D_0$ , are determined by comparator outputs  $Y_1$  through  $Y_{16}$ . There is some communication between the circuits determining the outputs to correct for timing errors. Also, bubble errors and overflow/underflow conditions must be detected and corrected to improve the converter accuracy.

#### 4.1.1 LSBs Encoding

To correct bubble errors, the encode logic employs the 3 input NAND gate circuits frequently used in flash ADCs. This circuit, however, needs to be modified slightly because the comparator values  $Y_1 - Y_{16}$  are not thermometer coded but circularly coded[16]. The circuit to perform the bubble correction errors is shown in Fig 4-2. The gates on the right (outputs  $W_{16}$  through  $W_{31}$ ) are exactly like those used in flash converters. If a bubble error occurred so that codes  $Y_1 - Y_{16}$  were (000000101111111) the 3 input NAND gates would suppress the bubble so that only one output ( $W_{25}$  in this case) would go low. The remaining outputs would stay high.



Vin		-0.5 V	-0.25 V	0.0 V	+0.25 V	+0.5 V
A	0000	0000000000000000	0000000000000000	1111111111111111	1111111111111111	1111
B	0000	0000000000000000	1111111111111111	1111111111111111	0000000000000000	0000
C	0000	1111111111111111	1111111111111111	1111111111111111	1111111111111111	0000
Y1	0000	0000000000001111	1111111111110000	0000000000001111	1111111111110000	0000
Y2	1000	0000000000001111	1111111111111000	0000000000001111	1111111111111000	0000
Y3	1100	0000000000000011	1111111111111100	0000000000000011	1111111111111100	0000
Y4	1110	0000000000000001	1111111111111110	0000000000000001	1111111111111110	0000
Y5	1111	0000000000000000	1111111111111111	0000000000000000	1111111111111111	0000
Y6	1111	1000000000000000	0111111111111111	1000000000000000	0111111111111111	1000
Y7	1111	1100000000000000	0011111111111111	1100000000000000	0011111111111111	1100
Y8	1111	1110000000000000	0001111111111111	1110000000000000	0001111111111111	1110
Y9	1111	1111000000000000	0000111111111111	1111000000000000	0000111111111111	1111
Y10	1111	1111100000000000	0000011111111111	1111100000000000	0000011111111111	1111
Y11	1111	1111110000000000	0000001111111111	1111110000000000	0000001111111111	1111
Y12	1111	1111111000000000	0000000111111111	1111111000000000	0000000111111111	1111
Y13	1111	1111111100000000	0000000011111111	1111111100000000	0000000011111111	1111
Y14	1111	1111111110000000	0000000001111111	1111111110000000	0000000001111111	1111
Y15	1111	1111111111000000	0000000000111111	1111111111000000	0000000000111111	1111
Y16	1111	1111111111100000	0000000000011111	1111111111100000	0000000000011111	1111
D5	0000	0000000000000000	0000000000000000	1111111111111111	1111111111111111	1111
D4	0000	0000000000000000	1111111111111111	0000000000000000	1111111111111111	1111
D3	0000	0000000011111111	0000000011111111	0000000011111111	0000000011111111	1111
D2	0000	0000111100001111	0000111100001111	0000111100001111	0000111100001111	1111
D1	0000	0011001100110011	0011001100110011	0011001100110011	0011001100110011	1111
D0	0000	0101010101010101	0101010101010101	0101010101010101	0101010101010101	1111

Figure 4-1: Latched Comparator Codes and 6-bit Output versus  $V_{in}$

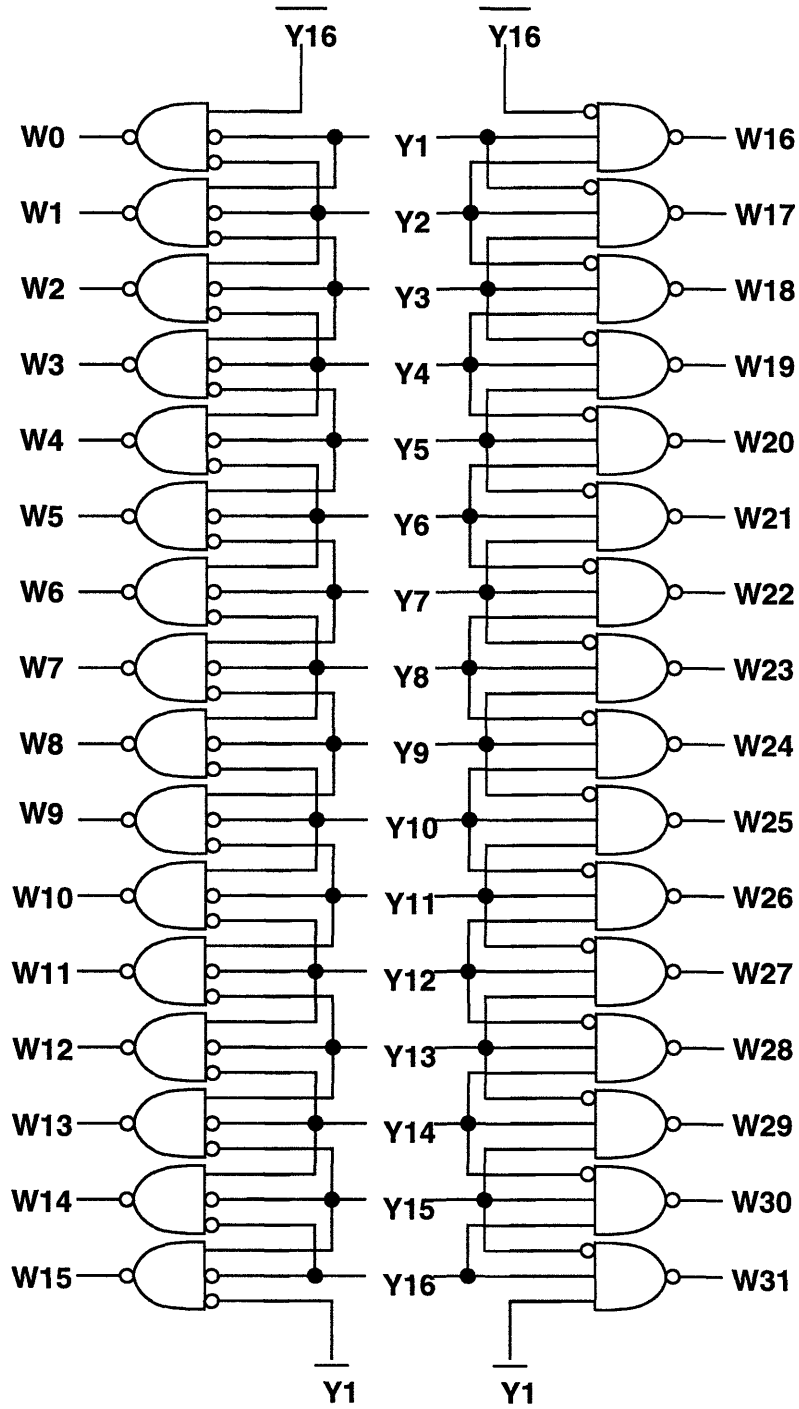


Figure 4-2: Bubble Error Correction Circuitry

The gates on the left are required to detect the remaining circular codes. The inputs to these gates are the inverse of their corresponding gates on the right. Bubble error correction is similar with these gates. For example, if codes  $Y_1 - Y_{16}$  were (1111010000000000) only  $W_6$  goes low. The other outputs stay high.

We see that only one output of the NAND gate array goes low at a time. Once this transition point is determined, it is fairly easy to encode the 5 LSBs of the 6-bit output with the AND plane of a PLA [20]. Fig. 4-3 shows how this is done. Initially, the  $CLK$  line is high so the comparator outputs are latched and  $W_0 - W_{31}$  are at stable values. During this time, the gate voltages of the p-type MOSFETs at the top of the PLA are driven low so lines  $X_0 - X_4$  are precharged to  $V_{DD}$ . The pull-down n-type MOSFETs are disabled with the clocked NOR gates. When  $CLK$  goes low the pull-down n-type MOSFETs are enabled. The clocked NOR gates now act as inverters, making the active low signals,  $W_0 - W_{31}$ , active high. Only one of the NOR gate outputs goes high, so a single row of the PLA determines the 5-bit output  $X_0 - X_4$ . The n-type MOSFET array in the PLA that corresponds to each  $W_i$  signal differs slightly from the standard flash ADC, but they can be derived from the ideal codes previously shown in Fig. 4-1.

Simulated waveforms for the PLA are shown in Fig. 4-4. For this simulation, all of the encoding gates are implemented with static CMOS. The simulation demonstrates how a single PLA output,  $X_i$ , (labelled  $PLAOUT$ ) responds to a  $W_i$  signal (labelled  $IN$ ) held low while the PLA is clocked at 180  $MHZ$ . The waveform  $NOROUT$  represents the behavior of the clocked NOR gates to the input signal describe above. We can see the PLA operates correctly at a 180  $MHz$  conversion rate.

#### 4.1.2 MSB Encoding

The MSB of the 6-bit digital output is determined by the 3 digit output ( $ABC$ ) of the cycle encoder. As seen in Fig. 4-1, there are 6 ideal values for  $ABC$  - 000, 001, 011, 111, 101 and 110. The MSB can be implemented from these codes rather simply. The MSB will equal 0 when  $ABC$  equals 000, 001 or 011 and 1 when  $ABC$  equals 111, 101 and 100. However, this encoding scheme provides no protection against any timing mismatch that could occur between the LSB section folding circuits and the cycle encoder. In order to protect against any possible mismatch errors, a more complex encoding scheme is required.

Such a scheme uses comparator outputs  $Y_5$  and  $Y_{13}$  along with  $ABC$  to generate the MSB and

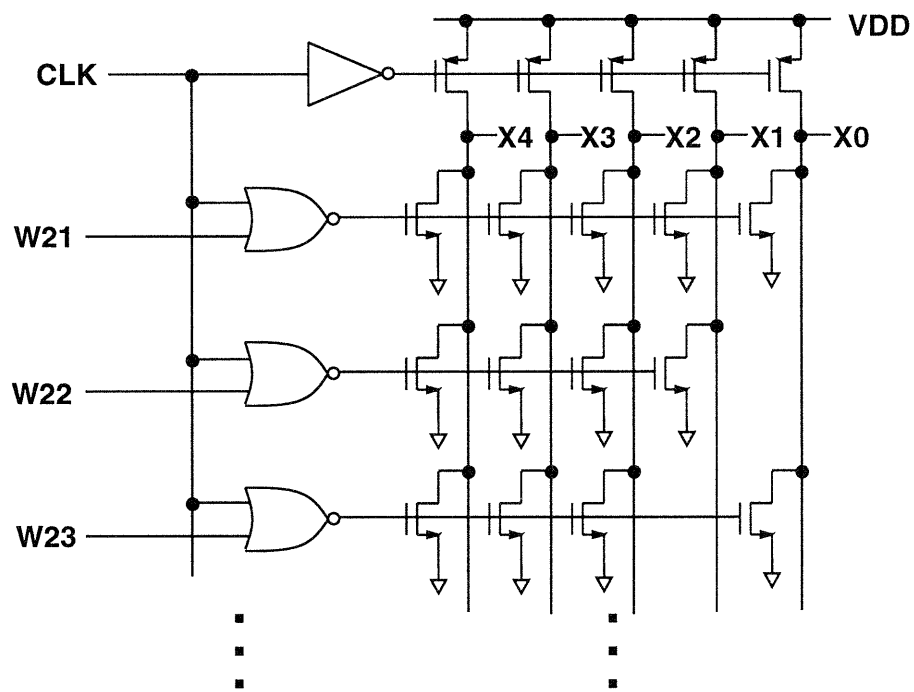


Figure 4-3: PLA to Encode 5 LSBs

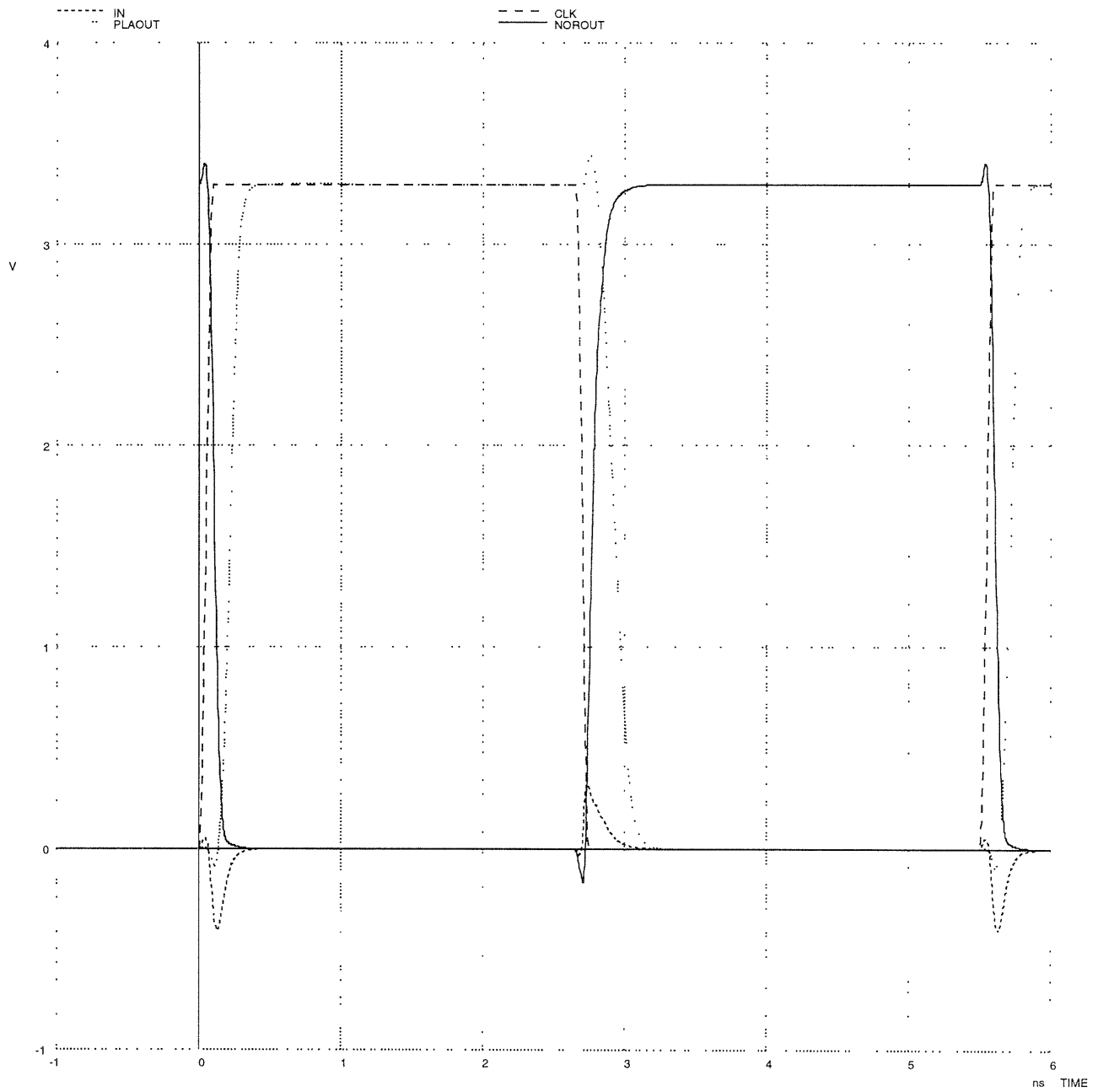


Figure 4-4: Simulated PLA Waveforms

the overflow ( $OF$ ) and underflow ( $UF$ ) signals. For example, let us assume that the latched values for  $ABC = 011$ ,  $Y_5 = 0$  and  $Y_{13} = 1$ . From the ideal codes of Fig. 4-1, we see that nowhere in the range of  $ABC = 011$  is  $Y_5 = 0$  and  $Y_{13} = 1$ . Therefore a timing error has occurred. It is assumed that the error has occurred in the MSB section since timing delays in the LSB section are well matched. This error must be corrected or else the 6-bit digital output will be off by half the digital range.

From the ideal codes in Fig. 4-1, we see that the  $ABC$  value closest to the place where  $ABC = 011$ ,  $Y_5 = 0$  and  $Y_{13} = 1$  is 111. Therefore the effective value of  $ABC$ ,  $ABC_{eff}$ , is 111. With  $ABC_{eff} = 111$ ,  $Y_5 = 0$  and  $Y_{13} = 1$ , we know that the analog input voltage was between 0.0 V and 0.25 V. The MSB will be 1 and the remaining LSBs can be determined normally. If the simple encoding scheme described above was used the MSB would be set to 0 and the LSBs would be encoded normally. The erroneous digital output would be off by 100000 (=0.5 V).

The encoding algorithm is summarized in Table 4.1.  $ABC_{eff}$  is listed for every possible combination of input values  $ABC$ ,  $Y_5$  and  $Y_{13}$ , including invalid  $ABC$  codes 010 and 110. The values of logic signals  $OF$ ,  $UF$  and  $MSB$  that correspond to each  $ABC_{eff}$  are listed in Table 4.2.

The algorithm can be implemented with the logic circuits shown in Fig. 4-5. For this design, these logic circuits were mapped into static CMOS. Simulation showed these circuits to have a critical path delay of 500 ps.

### 4.1.3 Binary Output Encoding

The output signals of the MSB algorithm logic circuits control a multiplexor which passes the final 6-bit binary output. The purpose of the multiplexor is to have the binary output appropriately respond to  $OF$  and  $UF$  signals. The  $OF$  signal goes high when the sampled analog input voltage is over +0.5 V. The corresponding binary output should be 111111. When  $UF$  goes high, the input voltage is below -0.5 V so the binary output should be 000000. When neither  $OF$  or  $UF$  is high ( $\overline{OF} + \overline{UF} = 1$ ) then the binary output should be obtained from the PLA( $X_0 - X_4$ ).

One block of the multiplexor circuit is show in Fig. 4-6. The multiplexor is implemented with pass gates. When  $OF$  is high the multiplexor output,  $D_i$ , is set high. With  $UF$  high, the multiplexor output is connected to ground. When the valid signal is high ( $V = \overline{OF} + \overline{UF}$ ), the output is driven by the PLA output  $X_i$ . With minimum sized devices, the simulated pass-gate multiplexor delay

$ABC$	$Y_5$	$Y_{13}$	$ABC_{eff}$
000	0	X	001
	1	X	000
001	0	0	001
	0	1	001
	1	0	011
	1	1	000
011	0	0	001
	0	1	111
	1	0	011
	1	1	011
111	0	0	111
	0	1	111
	1	0	101
	1	1	011
101	0	0	111
	0	1	100
	1	0	101
	1	1	101
100	0	X	100
	1	X	101
010	0	0	001
	0	1	001
	1	0	011
	1	1	000
110	0	0	111
	0	1	100
	1	0	101
	1	1	101

Table 4.1: MSB Algorithm Summary

$ABC_{eff}$	$OF$	$UF$	$MSB(D_5)$
000	0	1	0
001	0	0	0
011	0	0	0
111	0	0	1
101	0	0	1
100	1	0	1

Table 4.2: Corresponding Output Codes

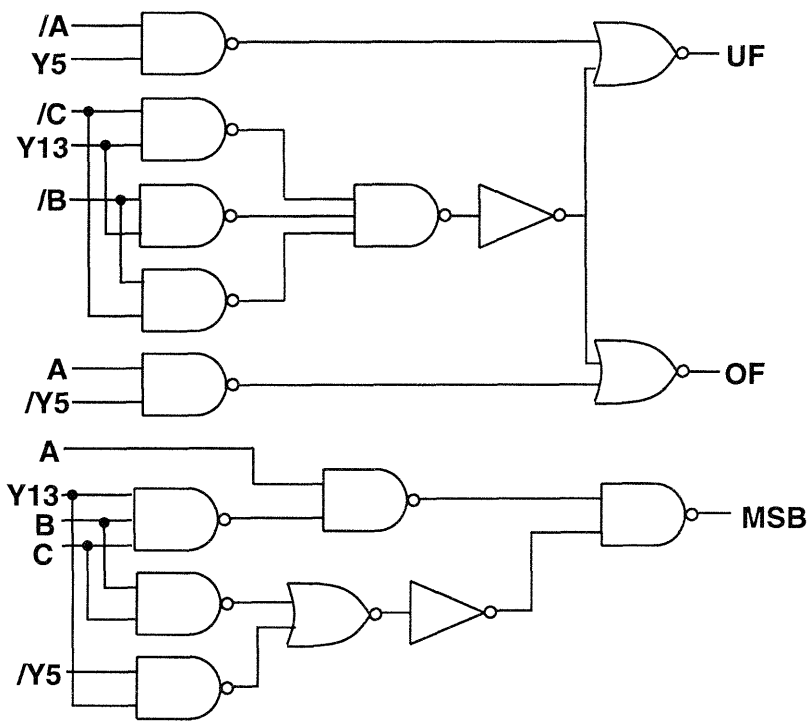


Figure 4-5: MSB Algorithm Logic Circuits



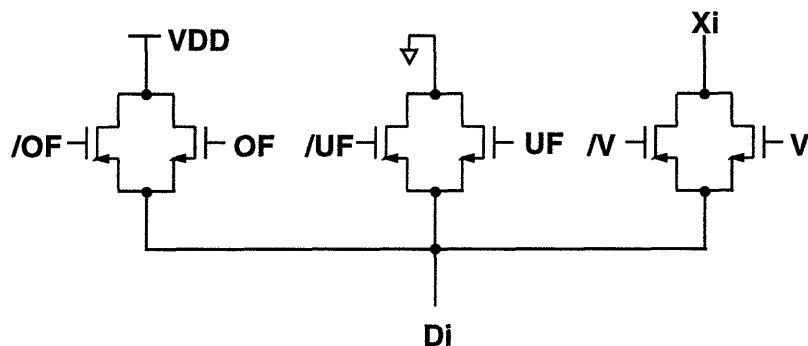


Figure 4-6: Multiplexor Block

was measured to be 200 ps. The full multiplexor is made up of 5 multiplexor blocks. One for each of the 5 PLA outputs. The MSB is not required to be gated by the multiplexor because it is determined in parallel with the  $UF$  and  $OF$  signals. When the gating function of the multiplexor is complete, the binary 6-bit output of the ADC is available.

## 4.2 Timing and Control

The three timing waveforms used in the folding ADC are pictured in Fig. 4-7. These control signals are mainly associated with the comparators, but it is convenient to discuss them in this section. The system clock,  $CLK$ , is routed around the entire circuit. It acts as the comparator  $LATCH$  signal. Signals  $COMPARE$  and  $P/E$  are generated locally at the comparators.

The  $CLK/LATCH$  signal controls several functions. When  $CLK/LATCH$  is high, the comparators are latched and the PLA is precharging. After a short delay, the  $P/E$  signal goes high. This enables the comparator sense amplifier to convert the comparator signal to CMOS levels. After half the clock period, the  $CLK/LATCH$  signal falls. The inputs to the digital logic remain valid because the comparators use a master-slave configuration. The PLA becomes active allowing digital output to be available. Simultaneously, the  $COMPARE$  signal goes high and the comparators begin to track the analog input voltage. The sense amplifier is also precharged for the next

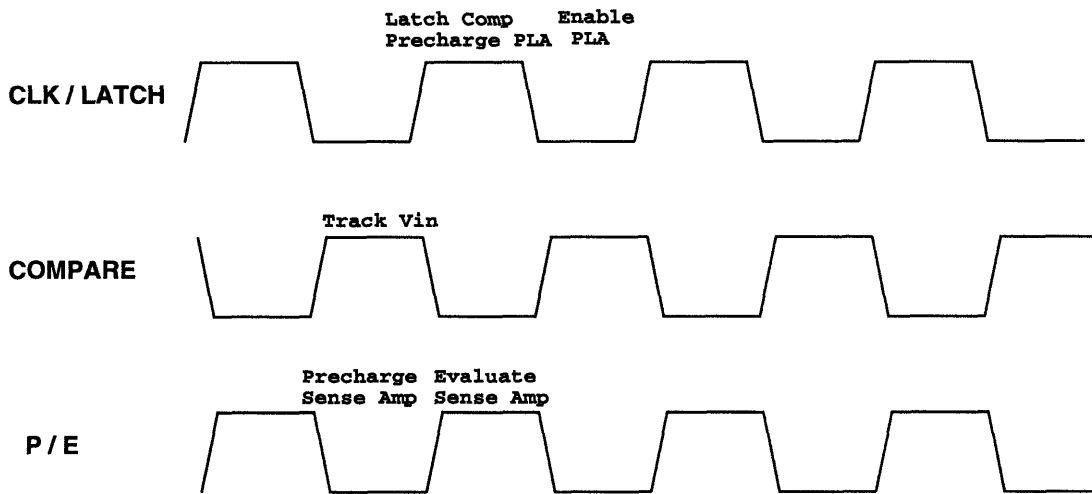


Figure 4-7: Timing Waveforms

sample at this time. The operations repeat themselves when the *CLK/LATCH* signal goes high again.

### 4.3 Digital Logic Summary

The complete digital logic system is summarized in Fig. 4-8. The 16 comparator outputs,  $Y_1 - Y_{16}$ , are encoded and bubble-error corrected with the NAND gates block. The NAND gate outputs drive the PLA through clocked NOR gates producing the LSBs,  $X_0 - X_4$ . In parallel with this process, the overflow/underflow signals and the MSB are determined. The overflow/underflow signals control the output multiplexor which provides the 5 LSBs. The MSB signal completes the 6-bit digital output.

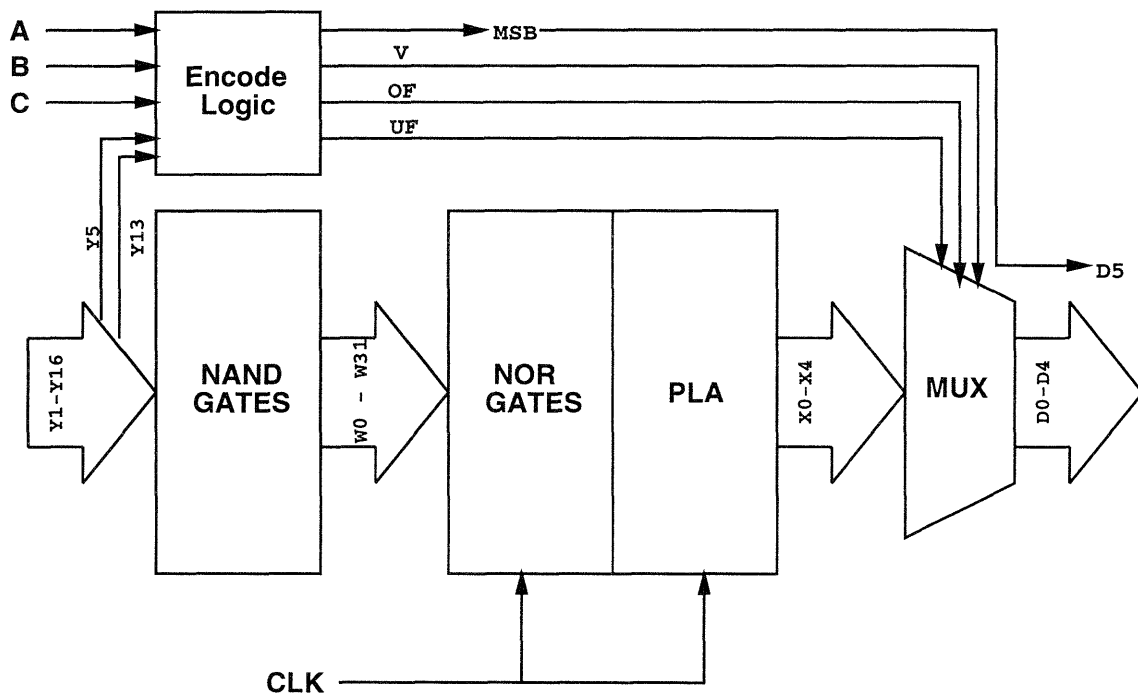


Figure 4-8: Digital Logic Summary

# Chapter 5

## Layout

The folding ADC design was laid out in the IBM BiCMOS4S technology. This technology combines high performance bipolar transistors ( $f_T = 12GHz$ ) with short-channel length MOSFETs ( $L_{eff} = 0.5\mu m$ ). The layout was completed and verified with Cadence Design Systems' Design Framework software running on IBM RS/6000s.

### 5.1 Inaccuracies from Layout

There are a number of issues in the layout of an ADC which can adversely affect converter accuracy. For example, the comparators of an ADC can exhibit a delay which is much larger than the allowable jitter in the sample moment. This will not affect proper operation of the ADC as long as every comparator delays the signal by the same amount of time. Some mismatch between delays is permissible, but if the delay difference becomes too large, performance will be affected. Unlike normal offsets, the delay matching is dependent on the absolute values of the parasitics in the comparator. The value of these parasitics spread over an integrated circuit due to doping gradients. The larger the die, the worse the delay matching becomes [9].

In a high-speed flash ADC, the comparators are spread all over the die. This results from *snaking* the comparator arrays and reference ladder around in order to avoid a very long, narrow die. The folding ADC has fewer comparators than a flash ADC, so the comparators can be more highly concentrated and experience minimal differences in signal delay. The absolute delay differences in the flash ADC comparators can be reduced by decreasing the signal delay time. Doing so implies

higher currents and more power dissipation. Thus, the folding ADC will yield better performance without the need for extra power.

A second source of inaccuracy is from the distribution of the analog signal and sample clock over the integrated circuit. When a signal has to be applied simultaneously to a number of circuits, a physical distance between their input terminals gives rise to inaccuracy. This inaccuracy becomes especially significant at higher input frequencies. In the folding ADC, the physical distance between the comparators farthest apart is reduced, so the clock-distribution problems are relieved.

## 5.2 Layout Floor Plan

As mentioned above, the typical high-speed flash ADC layout consists of comparators and digital logic being snaked all around the die. This can lead to problems in signal distribution and component matching. These problems are less significant in folding ADCs because the number of comparators is much smaller. Thus, the comparators are in closer proximity to each other. The layout floorplan of this design (Fig. 5-1) demonstrates this.

The layout measures 1 mm x 1 mm of die area. As the floorplan shows, the 19 comparators are stacked vertically in this design, making interconnection with other stages and signal distribution much simpler. The clock line, for example is simply routed from the right along the center of the die to a vertical bus connected to the comparators. With this floorplan, inaccuracies due to clock delays are reduced

Another benefit of the folding ADC layout is the symmetry of the analog circuitry. The folding amplifiers drive identical interpolation networks that are relatively close to one another. Close proximity keeps these interpolation networks well matched. Every output tap of the interpolation networks has the same effective output resistance. This keeps the mismatch of the delays to the comparator inputs very low.

A plot of the actual layout of the folding ADC is shown in Fig. 5-2. In this plot the pads, biasing circuits and busing have been removed for clarity. As we can see, the layout is quite sparse except for the comparator stage. Thus, the layout could be made significantly smaller if the area of the comparator could be decreased.

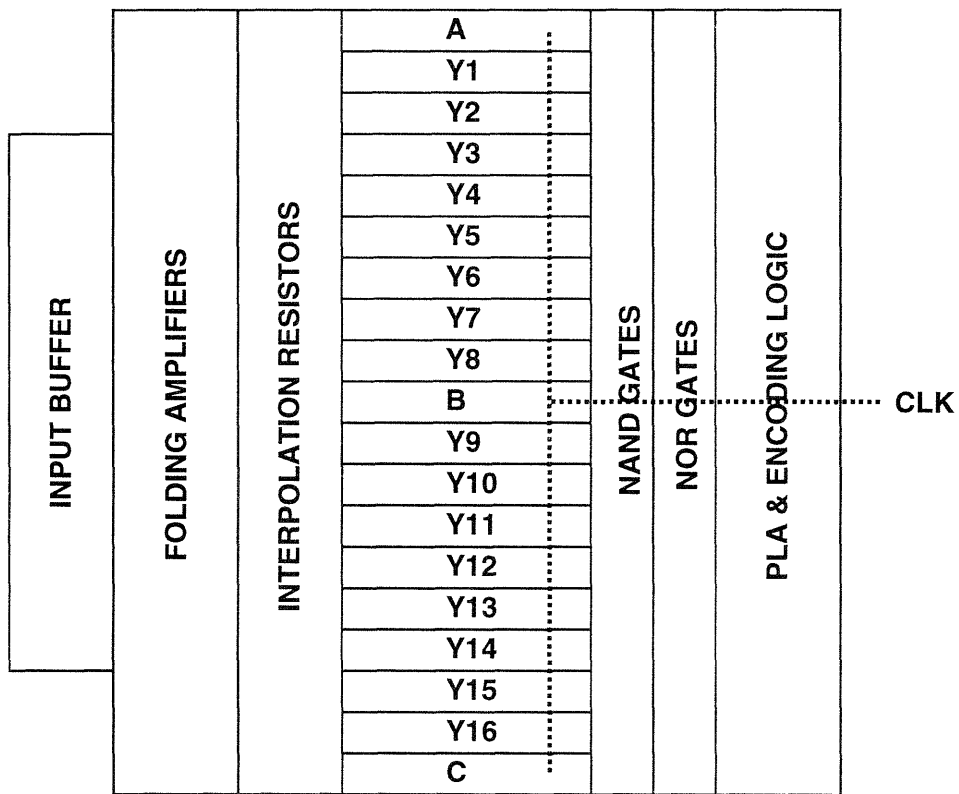


Figure 5-1: Folding ADC Floorplan

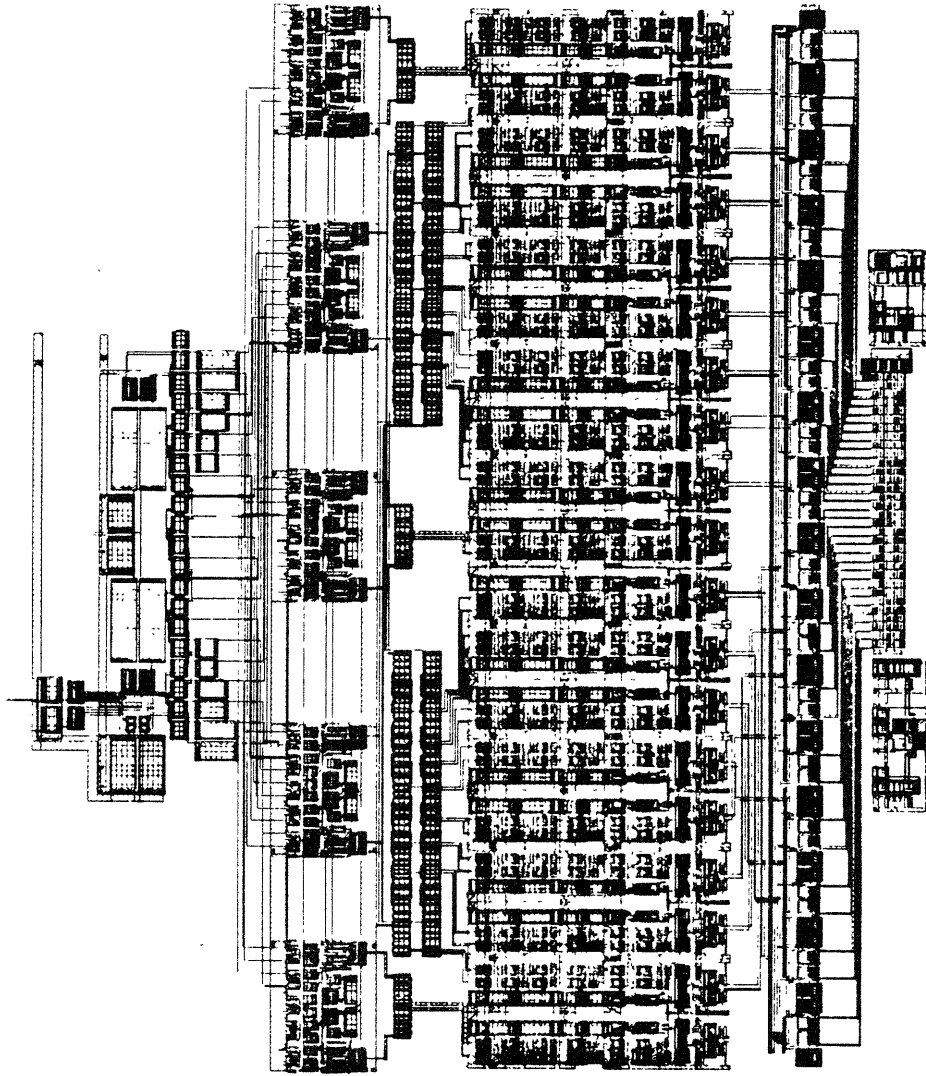


Figure 5-2: Folding ADC Layout

## Chapter 6

# Simulation Results and Conclusions

The full-speed, dynamic testing of analog-to-digital converters is performed using several techniques. The tests vary in complexity and in the amount of useful information they provide. The difficulty of implementing each test in a simulation environment also varies. The beat frequency test, the curve fitting test, the discrete fourier transform (DFT) test and the code density test are some of the most common tests used. The beat frequency test is very simple to implement using the real device models and demonstrates the functionality of the converter at high speeds. In the curve fitting test, a general measurement of the ADC transfer function is built by averaging the ADC errors. This test shows how nonlinearities affect the converter usefulness at given frequencies. A variation of this test can be easily implemented in the simulation environment. In the DFT test, a sine wave is applied at the input of the ADC and the DFT of the digitized waveform is taken. This test is more difficult to implement because it requires a larger number of samples. The code density test uses a statistical approach to determine the ADC differential nonlinearity. This test is extremely difficult to implement in the simulation environment. This is because the test requires a very large number of samples in order to be significant [21]. Generating these samples using real device models would take several days to complete and require an enormous amount computer memory. Using an analog hardware description language (AHDL) or simplistic device models would make the simulation bearable, but the results would be less significant.

The beat frequency and modified curve fitting tests are used to show the ADC performance at high input frequencies. Although, the DFT test could also be implemented, it is not useful with the frequencies associated with the PRML channel ( $f_{in}$  very close to  $\frac{f_{CLK}}{2}$ ) for which the folding



ADC was designed.

## 6.1 Curve Fitting Test

The modified curve fitting test is performed by driving the ADC with a high-speed ramp and sampling the converter at a time when the analog input is known. The digital output resulting from this experiment can be compared to the analog input voltage and the quantization error can be calculated. Performing this experiment for many analog input voltages over the full scale range produces an error plot for the converter at that particular input frequency. The error magnitude determines the converter performance.

For this experiment, the performance of the two folding ADC designs described in Chapter 3 is compared. Recall that the first folding ADC design used only 2 folding amplifiers and tuned interpolator resistors in the LSB section. The second ADC design uses 4 folding amplifiers and equal valued resistors in the LSB section.

The error for the two designs at a DC analog input voltage are shown in Figs. 6-1 and 6-2. We see that the 2 folding amplifier design has errors associated with it even at DC. These errors are mainly due to the limitations on the tuning resistors. The physical resistors that form the tuning network cannot be in every possible proportion. Therefore, the error due to nonlinear portions of the folded waveform cannot be completely tuned away. The error for the 4 folding amplifier design is smaller than that of the previous case ( $\pm 0.55$  LSBs). This shows that the addition of folding amplifiers improves converter accuracy at the cost of additional power.

The error for the 2 folding amplifier design gets much worse at high-speed (90 MHz). From Fig. 6-3, we see that the quantization error of the 2 folding amplifier design ranges from +1.3 LSB to -1 LSB. The source of the high speed error is the large resistance across folding amplifier outputs. This large resistance increases delay mismatches of the folded waveforms. These mismatches become more significant at high-speed. The error associated with the four folding amplifier converter at high-speed is less. From Fig. 6-4, we see that the error ranges from about +0.8 LSB to -0.6 LSB. The reasons for this better performance are less resistance across the folding amplifier outputs and more symmetry.

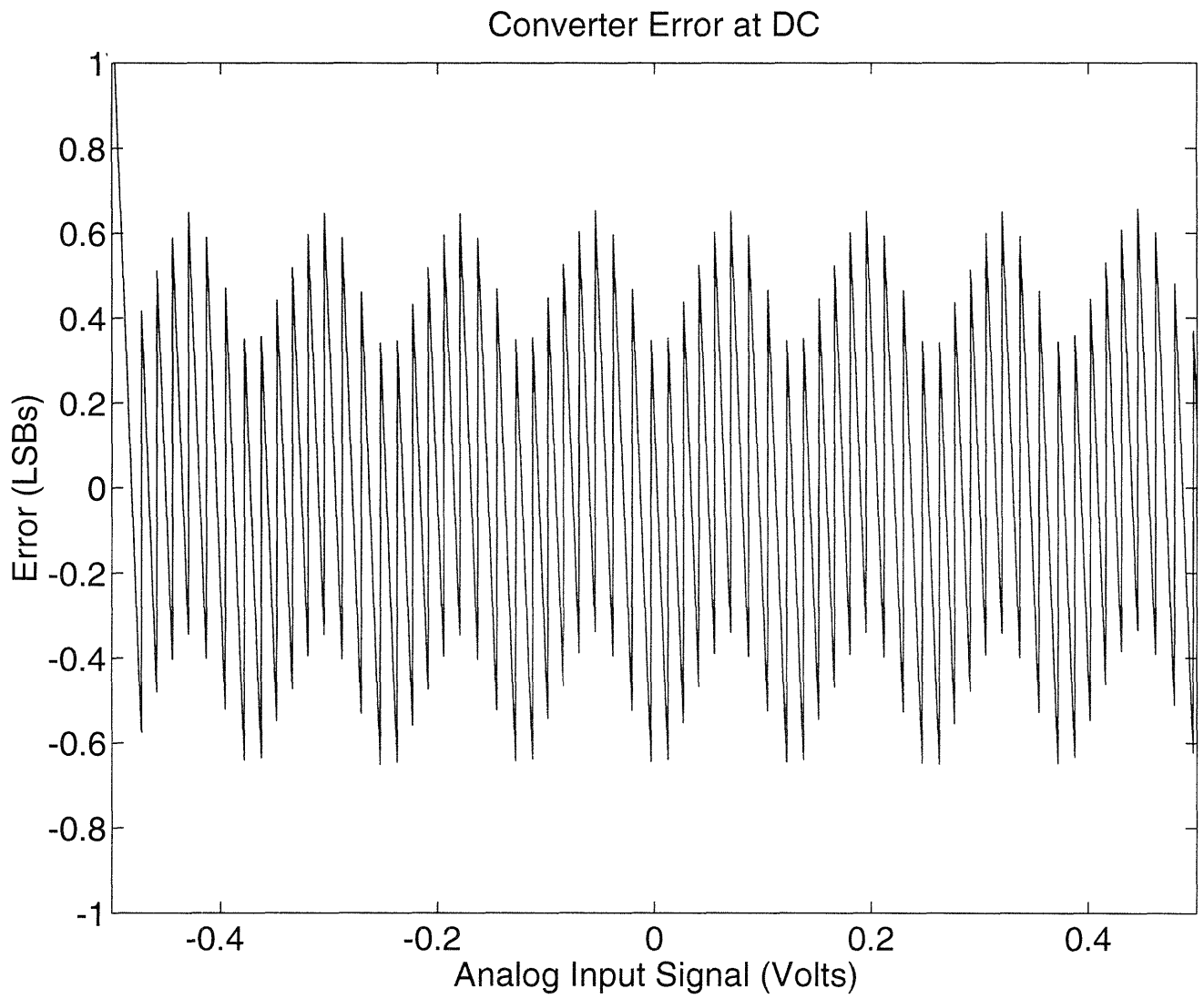


Figure 6-1: Error Plot of 2 Folding Amp ADC at DC

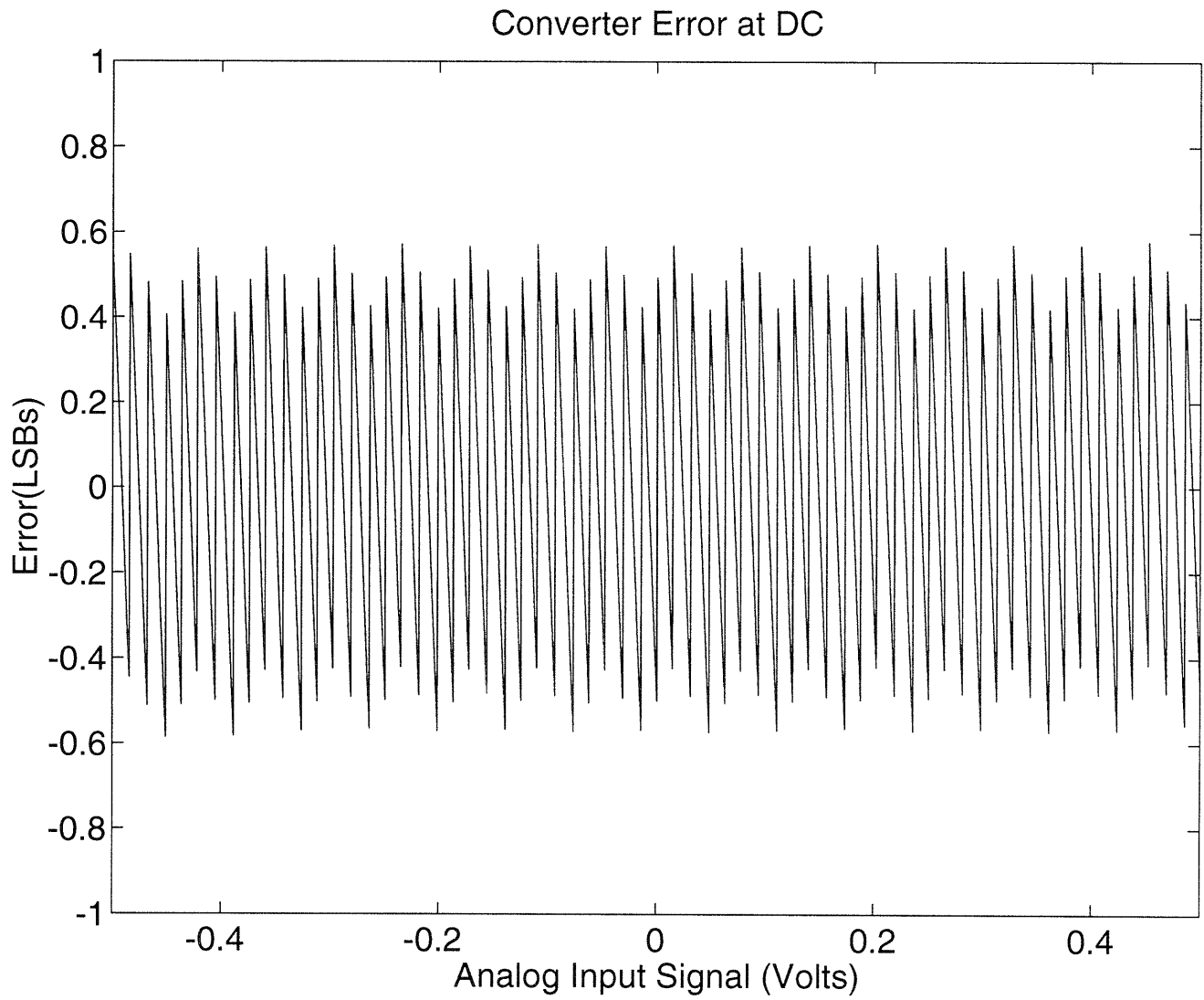


Figure 6-2: Error Plot of 4 Folding Amp ADC at DC

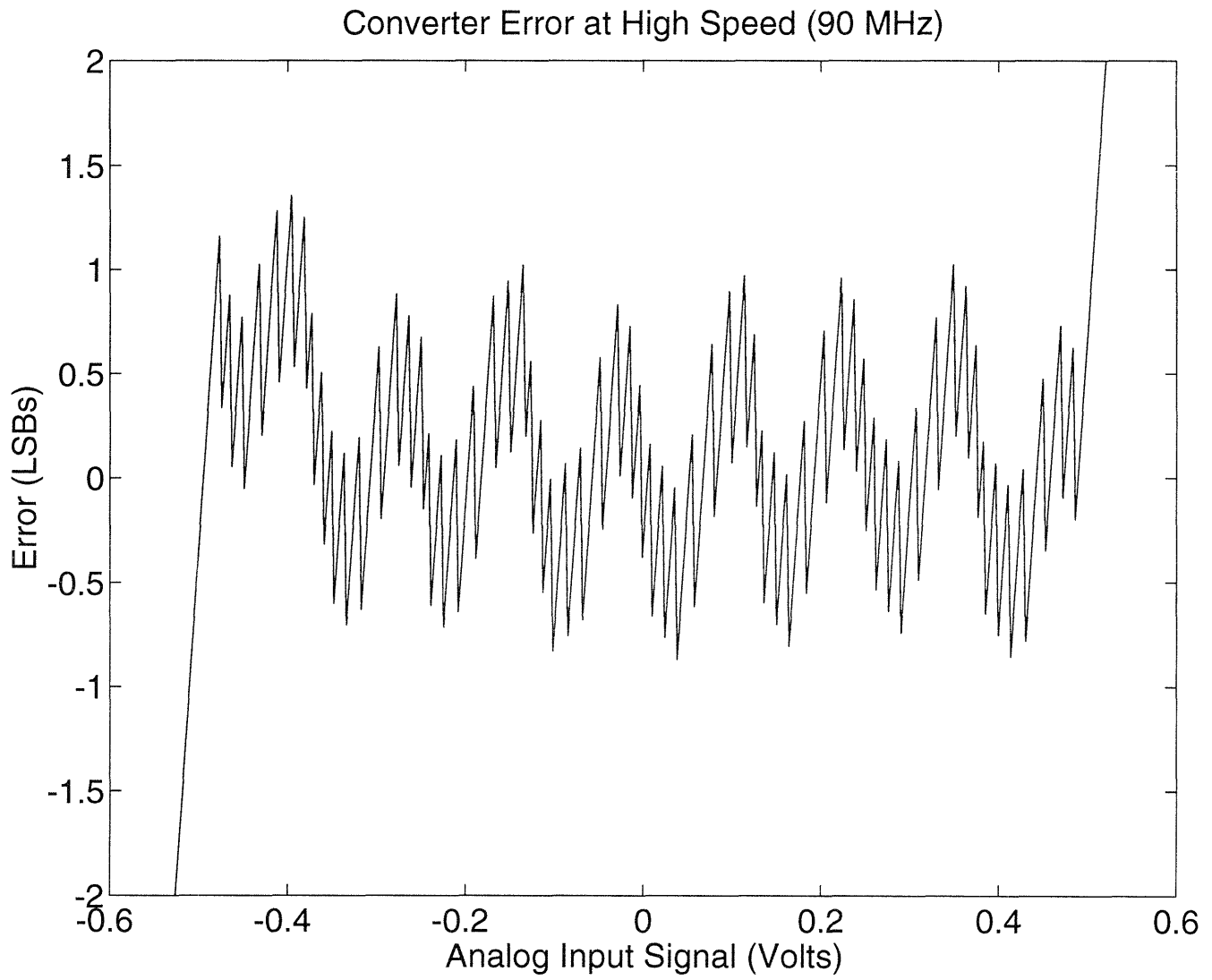


Figure 6-3: Error Plot of 2 Folding Amp ADC at 90 MHz

Converter Error at High Speed (90 MHz)

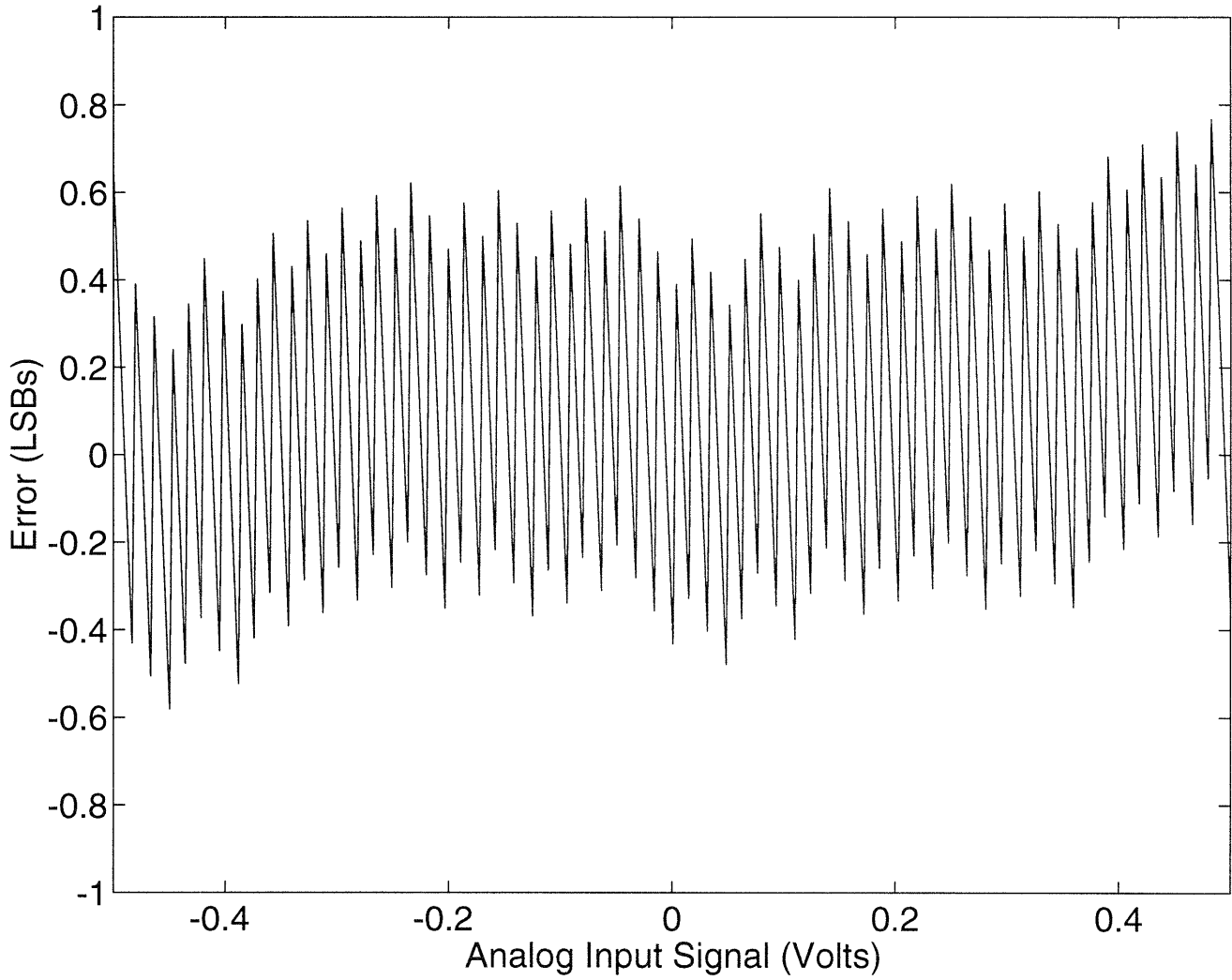


Figure 6-4: Error Plot of 4 Folding Amp ADC at 90 MHz

## 6.2 Beat Frequency Test

A beat frequency test exploits the aliasing phenomenon in order to test all of the possible output codes of an ADC to insure its operation at high-speed. During a beat frequency test, the ADC digitizes analog waveforms with frequencies that are multiples of the sampling rate. If you use an input sine wave just slightly higher in frequency than the sampling clock, the sampling point will change in relative phase at a rate equal to the difference in frequency between the two signals. By connecting the sampled data points in a continuous time record, the single tone beat frequency is traced [22].

In order to perform a beat frequency test, the input frequency should equal:

$$f_{IN} = \frac{f_{CLK}}{2^n} + f_{CLK} \quad (6.1)$$

where  $n$  equals the number of bits. For these experiments on the 4 folding amplifier ADC, the clock frequency is set to 45 *MHz* and 90 *MHz*. The required input frequency for each case is 45.22 *MHz* and 90.45 *MHz* respectively. The results of these tests are displayed in Figs. 6-5 and 6-6. By choosing the input waveform to have an amplitude greater than half the full scale range, the overflow and underflow circuitry can be tested during the beat frequency test. This shows up as clipping in the resulting waveforms. For each case, no output codes are missed. Thus, the converter operates well at these speeds.

## 6.3 Power Dissipation Comparison

During these high-speed tests, the power dissipation of the folding ADC is measured. The results of these measurements are summarized in Fig. 6-7. Folding ADC Design 1 uses 2 folding amplifiers and tuned resistors in the LSB section. Design 2 uses 4 folding amplifiers and equal valued resistors. The measured power dissipation for the two folding ADC designs is compared with the power dissipation of a similarly flash ADC designed in the same technology. In each comparison, the folding ADCs use less than half the power required for the flash ADC design.

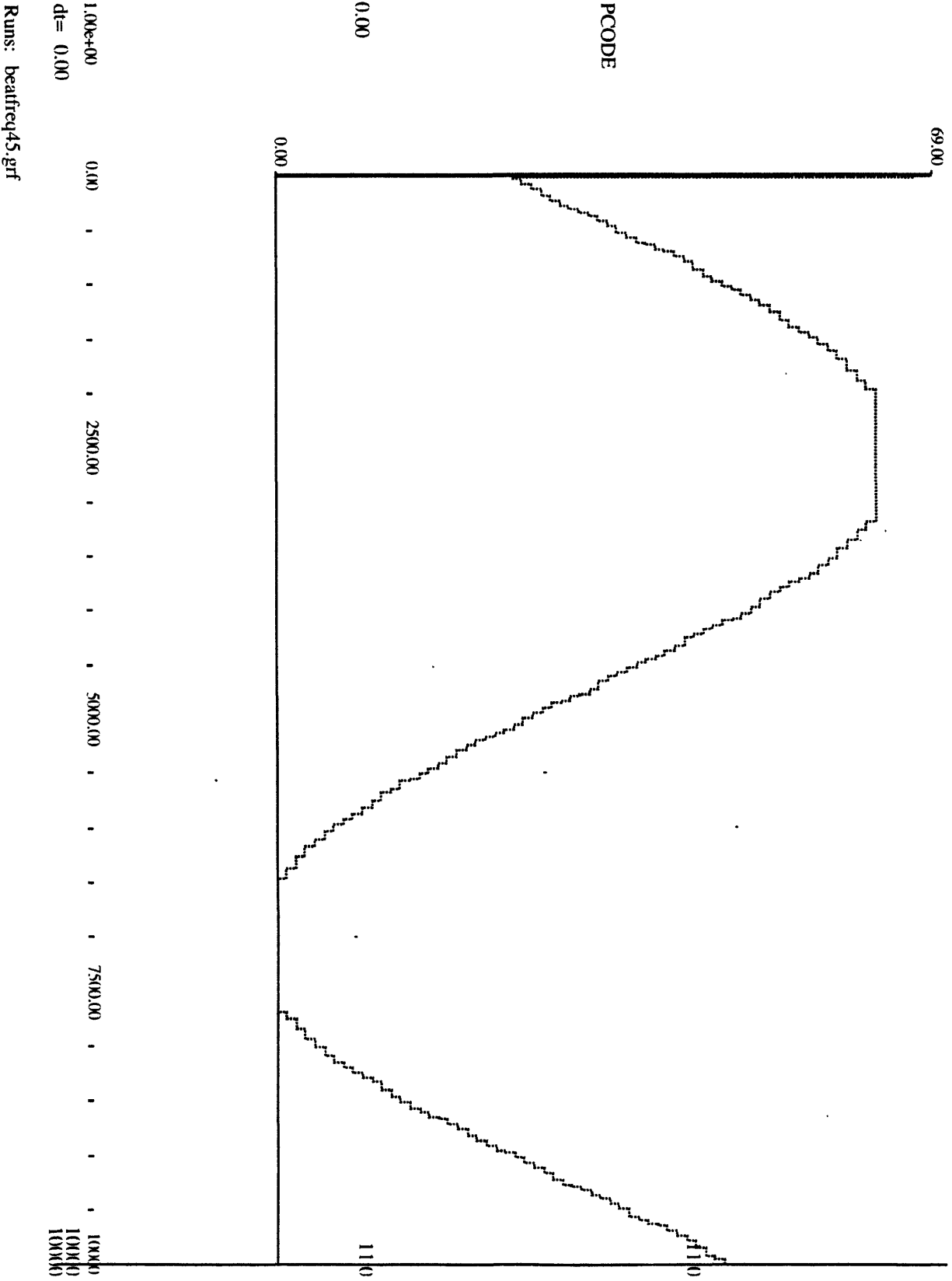


Figure 6-5: Beat Frequency Test at 45 MHz

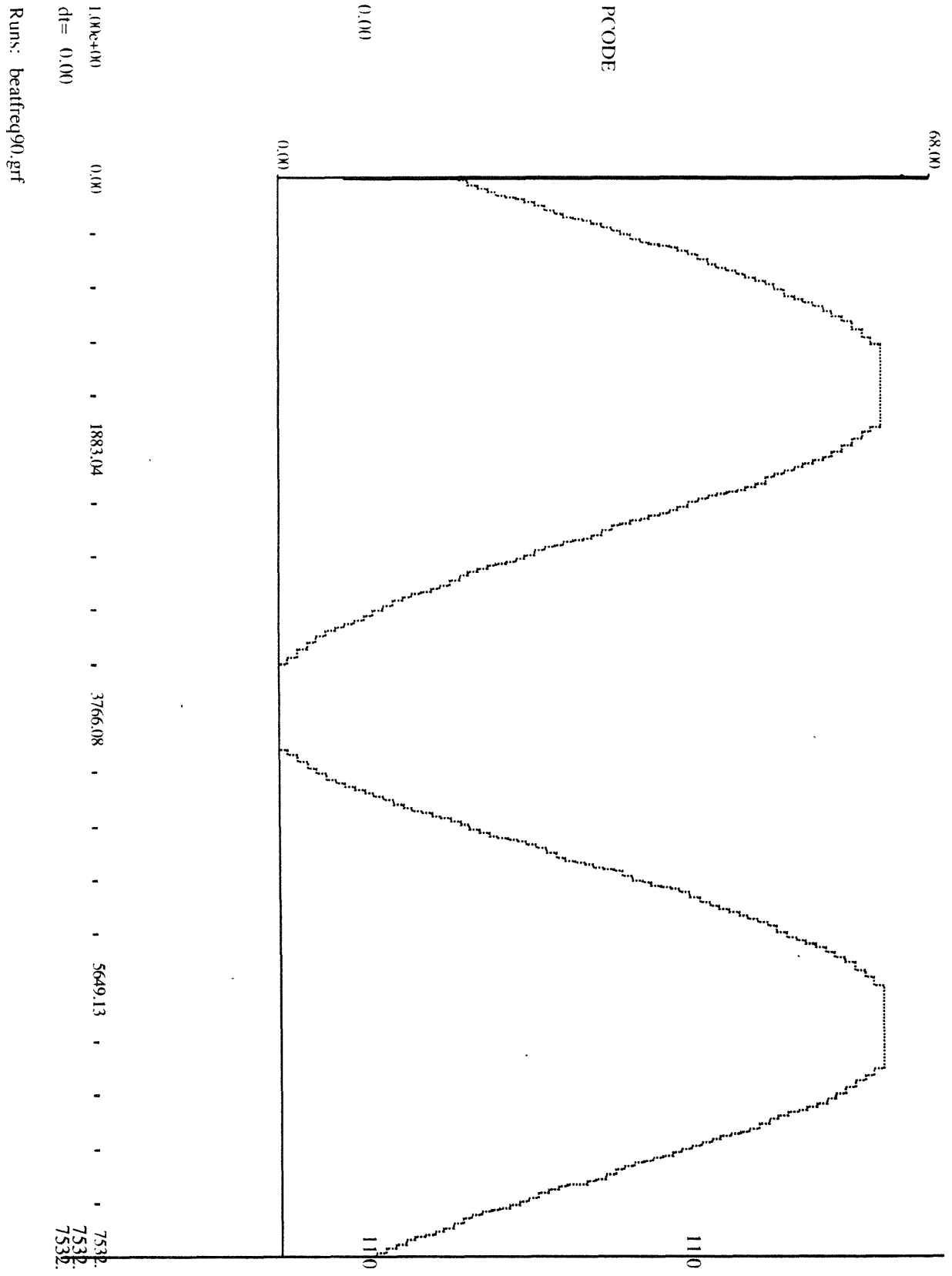


Figure 6-6: Beat Frequency Test at 90 MHz



	Flash ADC	Folding ADC	
		Design 1	Design 2
Comparators	(64) 384 mW	(19) 114 mW	(19) 114 mW
Folding Amps.		(5) 60 mW	(7) 84 mW
Input Buffer	30 mW	10 mW	10 mW
Clock	30 mW	11 mW	11 mW
Digital Logic	32 mW	17 mW	17 mW
Total	476 mW	212 mW	236 mW

Figure 6-7: Comparison of Power Dissipation in ADCs

## 6.4 Conclusions and Future Work

This study has demonstrated that folding ADCs are viable implementations of high-speed data converters using low power. Simulation shows that folding ADCs can operate at data conversion rates of up to 180 *MHz* with 6-bit resolution and use half the power required for a similarly performing flash ADC. Using the folding ADC architecture would also decrease the die area required for a data converter, making signal distribution easier.

Performance comparison between two folding ADC designs shows that using an equal-valued resistor interpolation ladder yields less error than an interpolation ladder using tuned resistors. However, the former design uses slightly more power due to two additional folding amplifiers.

The areas related to folding ADCs requiring further study are comparator design and full CMOS implementation. The size of the layout of a folding ADC is determined mainly by the size of a single comparator. Optimizing the comparators of this design for size would greatly reduce the total die area. A second area requiring study is the mapping of the BiCMOS folding ADC architecture into a less expensive CMOS technology. Folding ADCs use bipolar devices because of the high frequencies the folding amplifiers need to produce. Through circuit or technology innovations, full-CMOS folding amplifiers may be possible. This would create more opportunities for the folding ADC architecture to be used.

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