DESIGN AND IMPLEMENTATION OF A CAPACITIVE MEASUREMENT CIRCUIT WITH APPLICATION TO INTEGRATED MICROMOTOR POSITION SENSING

by

David G. Leip

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ABSTRACT

This thesis presents the design, analysis, and experimental results of a circuit to be used as a position sensor for microfabricated electric motors. The circuit is designed to measure the capacitance between the rotor blades and sensor electrodes implanted into the substrate beneath the rotor. This capacitance typically varies between five and fifteen femtofarads as the rotor turns. Analytic and experimental results show that the circuit is capable of measuring the required changes in capacitance in the presence of picofarad parasitic capacitances with a dynamic response approaching 1 MHz. However, successful implementation of the circuit as a position sensor for real micromotors requires the fabrication of buffer amplifiers in the micromotor substrate between the sensor electrodes and bonding pads.

Acknowledgments

I would like to take this opportunity to thank those who have helped to contribute to the successful completion of this thesis. I express my appreciation to the National Science Foundation for its support of micro-mechanical device research under project number 9109343-ECS. To my advisor, Professor Jeffrey H. Lang, I would like to thank you for all your help and guidance throughout the project. To Professor Stephen D. Senturia, your insight has been invaluable. I also express my gratitude to Professor James K. Roberge for his advice during a crucial juncture of the research. I am also very grateful for all the help from Eckart Jansen on the physics and operation of the micromotors.

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Chapter 1: Introduction

The objective of this thesis is to develop a method for accurate position sensing of a microfabricated electric motor, also known as a micromotor. To assist in this endeavor, a new micromotor design including buried capacitive sensors has been developed. A circuit designed to detect the change in capacitance between these new sensors and the rotor functions to pinpoint the position of the rotor. The two main obstacles to overcome in this design include the presence of relatively large parasitic capacitances inherent to integrated devices and the frequency constraint imposed by the speed of the motor. The problem is essentially to design and construct a circuit to detect femtofarad capacitance changes in the presence of picofarad capacitors at a frequency fast enough to maintain accurate positioning information. This thesis outlines the design and implementation of a capacitive sensing circuit to determine the position of the rotor of a microfabricated electric motor for use in closed-loop control.

1.1 Description and Modeling of an Integrated Micromotor:

A microfabricated electric motor, or micromotor, is a micron-scale mechanical device integrated on a silicon wafer. A sketch of a micromotor is shown below in Figure 1.1. The rotor of this device has a diameter of 80μm. Surrounding the rotor is a set of six stator poles. Stator poles having the same alignment to the rotor (opposite pairs) form a single phase. The excitation of a stator phase induces a charge of opposite polarity on the rotor poles nearest to the excited stator poles, creating tangential electrostatic forces. Since the rotor is charge neutral, the external sources driving the two stator poles of each phase must be of opposite polarity to ensure the accumulation of induced charge on opposite rotor poles. The tangential forces generate a torque which acts on the rotor so as to align its charged poles with the excited stator poles. The properly timed sequential excitation of the stator phases causes the rotor to turn in synchronism with the excitation [1].

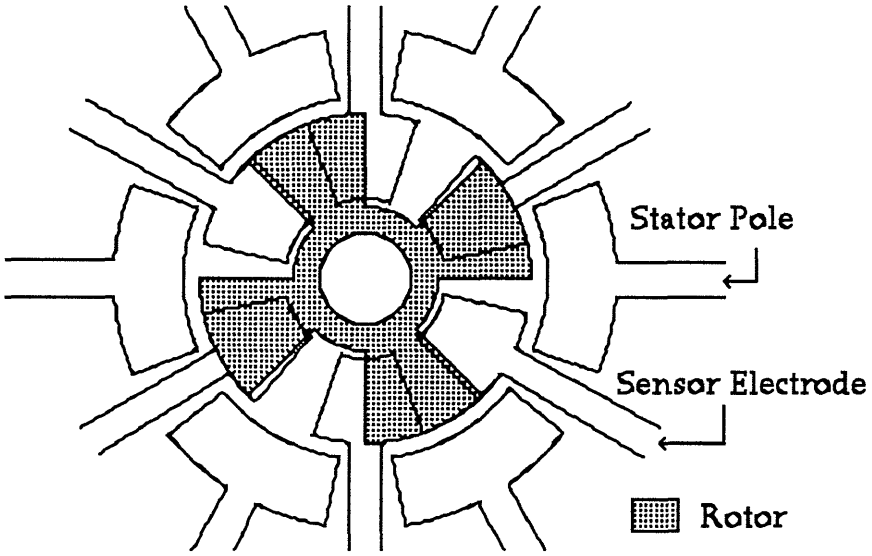

Figure 1.1: Top View of an Integrated Micromotor

To accurately control stator charging and discharging cycles, the position of the rotor must be known. To accomplish this task, six sensor electrodes are implanted into the substrate beneath the rotor. The capacitance between the rotor and these implanted sensors varies as the rotor turns. Hence, a measure of this capacitance reveals the position of the rotor.

Building a circuit to accurately sense the position of the micromotor requires a good understanding of the physics of the device. Translating the fundamental physics of the micromotor into an equivalent circuit model is the first part of the design process. The development of this model begins with a examination of its construction. A side view of the micromotor is shown below in Figure 1.2.

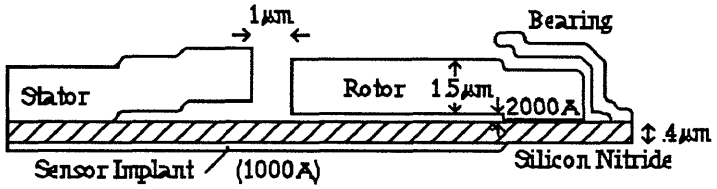

Figure 1.2: Side View of One-Half of an Integrated Micromotor

The stator and rotor are both fabricated using conducting material. The silicon-nitride layer insulates these regions from the substrate and sensor implant, both of which are conductive. The non-conductive bearing provides

the centerpoint around which the rotor turns. The bearing also prevents the rotor from making physical contact with the stator poles. With none of the major conductive components of the integrated micromotor resistively connected, the equivalent circuit model is entirely capacitive.

The various capacitances intrinsic to the integrated micromotor are shown below in Figure 1.3. The capacitance associated with the operation of the micromotor is the stator-rotor capacitance (C_{SR}). The rotor-implant capacitance (C_{RI}) is intentionally designed into the system and is used as a sensor to monitor the position of the rotor. The remaining capacitances are parasitics. The most important of these capacitance is C_{IS}, the implant-substrate capacitance. Since each implanted probe is connected to a large aluminum pad (required for wire-bonding), C_{IS} is very large compared to C_{RI}. The rotor-substrate capacitance (C_{RS}) is important because it forms a current divider with the rotor-implant capacitance. The presence of the stator-substrate capacitance (C_{SS}) does not affect the measurement (to first order) because one terminal is connected to a source and the other to ground. The stator-implant capacitance (C_{SI}) is quite small because the sensor implants and the stator poles do not overlap (see Figure 1.1). An equivalent circuit of the entire micromotor forms an array of capacitances and is shown below in Figure 1.4.

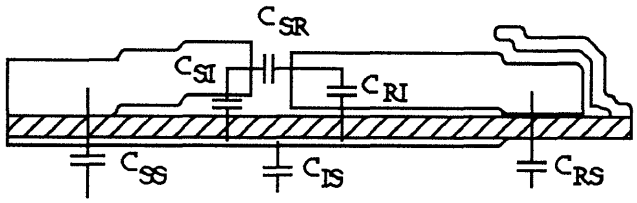

Figure 1.3: Intrinsic Micromotor Capacitances

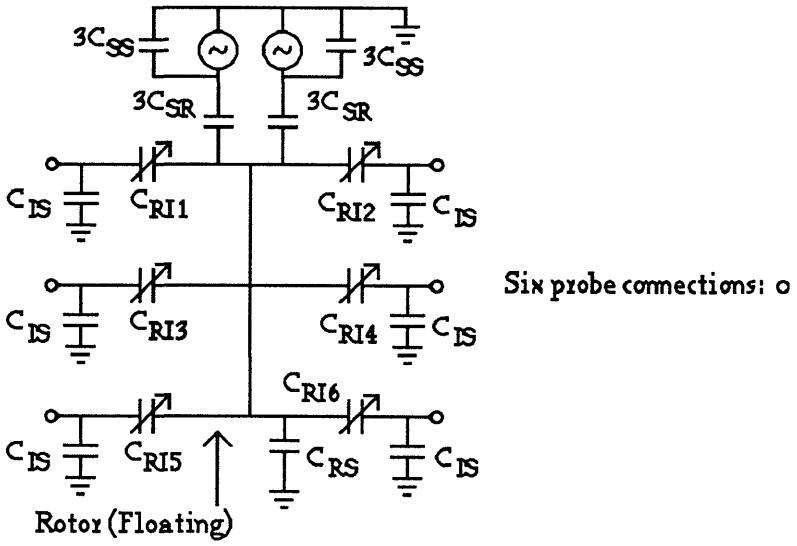

Figure 1.4: Micromotor Capacitance Array

The capacitance used to sense the rotor position (C_{RI}) can be estimated using the parallel-plate formulation.

$$C = \frac{\varepsilon A}{d} \qquad (1\text{-}1)$$

The calculation is slightly more complicated, however, because the implant layer and the rotor are separated by two dielectric layers. The first layer is a 0.2 μm air gap with a permittivity of $\varepsilon = 8.854 \times 10^{-14}$ F/cm. Beneath this layer is a 0.4 μm layer of silicon-nitride with a permittivity of $\varepsilon = 6.64 \times 10^{-13}$ F/cm. This two-dielectric capacitor (Maxwell Capacitor [2]) is equivalent to a series combination of two capacitors, C_{air} and C_{Si3N4}, each of which obeys Equation 1-1. Thus, $C_{RI} = C_{air}C_{Si3N4}/(C_{air} + C_{Si3N4}) = A\varepsilon_{Si3N4}\varepsilon_{air}/(\varepsilon_{Si3N4}d_{air} + \varepsilon_{air}d_{Si3N4}) = A \bullet 3.47 \times 10^{-9}$ F/cm^2. The area of this capacitance varies as the rotor turns and is maximized when the rotor blade and the implant probe align. Figure 1.5 shows approximate curves for the rotor-implant capacitances as a function of rotor angle. The rotor-implant capacitances are numbered sequentially around the rotor.

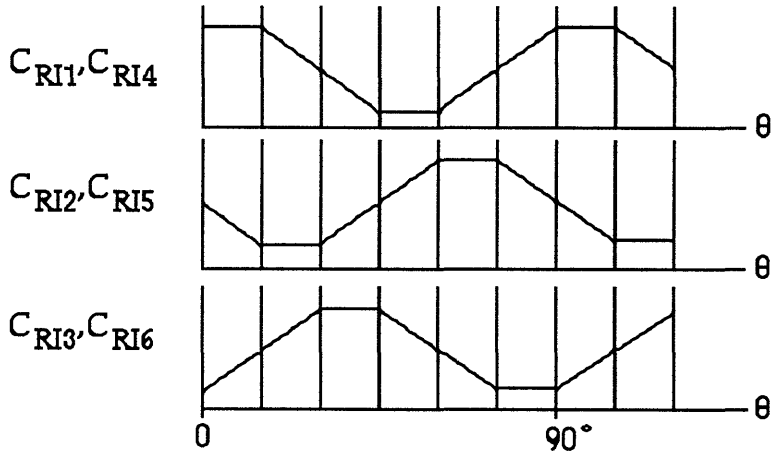

Figure 1.5: Sensor Capacitance as a Function of Time

With the six sensor geometry, adjacent rotor-implant capacitance functions differ by 60°. Furthermore, sensor implants located on opposite sides of the rotor have identical capacitance functions. Since there are four rotor blades, the C_{RI} function repeats for every 90 degree rotation of the rotor.

The maximum value of C_{RI} is limited by the area of the smaller plate. The implant probe is the smaller of the two plates with an area of 420 μm^2. Therefore, $C_{RImax} = 1.46 \times 10^{-14}$ F = 14.6 fF. The minimum capacitance is dominated by fringing fields and thus more difficult to calculate. However, the minimum value is at least a factor of 2 smaller than C_{RImax}.

The implant-substrate capacitance, C_{IS}, is a parallel combination of three capacitances. These include the implant depletion capacitance, the implant diffusion capacitance, and the metal-insulator-semiconductor parallel-plate capacitance present at the aluminum contact pad.

Approximating the implant-substrate junction as abrupt, the relationship describing the depletion capacitance [3] is

$$C_j = \frac{\varepsilon A}{\left[\frac{2\varepsilon}{q}(V_{bi} - V_A)\frac{(N_A + N_D)}{N_A N_D}\right]^{1/2}} \qquad (1\text{-}2)$$

No bias is applied to the junction (thus $V_A = 0$). The dopant concentration of the implant, N_D, is 1×10^{20} cm^{-3} and the dopant concentration of the substrate, N_A, is 1×10^{15} cm^{-3}. The permittivity of silicon, ε, is 1.045×10^{-12} F/cm, the electron charge, q, is 1.602×10^{-19} C, the area of the junction is

approximately 820 x 10^{-8} cm^2, and the built-in junction voltage, V_{bi}, is $kT/q(\ln(N_D N_A/n_i^2))$ = 0.89 V. Evaluating Equation 1-2 results in a junction depletion capacitance of C_j = 79 fF.

The diffusion capacitance [4] is described as

$$C_d = \frac{qQ_o e^{qV/kT}}{kT} \qquad (1\text{-}3)$$

Q_o represents the stored minority carrier charge. Since the implant-substrate diode has zero bias, the minority carrier charge is negligible, rendering the magnitude of the diffusion capacitance inconsequential.

The metal-insulator-semiconductor (MIS) capacitance is easily calculated from the standard parallel-plate capacitance formula presented as Equation 1-1. The permittivity of silicon-nitride is 6.64 x 10^{-13} F/cm, the area of the metal pad is designed as 200 μm x 200 μm = 4 x 10^{-4} cm^2, and the silicon-nitride thickness is 0.4 μm. This results in an MIS capacitance of 6.64 pF. Summing the three components of the implant-substrate capacitance results in C_{IS} = 6.72 pF - almost three orders of magnitude larger than the rotor-implant capacitance.

The stator-rotor capacitance, C_{SR}, also varies as the rotor turns. C_{SR} is maximized when the rotor blade and the stator align. This orientation forms 1/8 of a cylindrical capacitor and its value is estimated [5] as

$$C = \frac{1}{8} 2\pi\varepsilon_o \frac{L}{\ln(b/a)} \qquad (1\text{-}4)$$

The radius of the rotor, a, is 40 μm and the inner radius of the stator, b, is 41 μm. The length of the cylinder, L, is 1.5 μm. Utilizing Equation 1-4 results in a capacitance of (3.4 fF)/8 = 0.42 fF. The minimum capacitance is likely to be less than 0.1 fF, and is dominated by fringing fields.

Finally, the rotor-substrate capacitance is calculated using the parallel-plate formulation. The dielectric is pure silicon nitride with at thickness of 0.4 μm and an area of $\pi[(20\ \mu m)^2 - (10\ \mu m)^2]$ = 942 μm^2. Utilizing Equation 1-1 reveals C_{RS} = 156 fF. Table 1-1 summarizes the values of the micromotor capacitances.

Table 1-1: Micromotor Capacitance Values (fF)

Capacitance	Maximum Value	Minimum Value
C_{RI}	14.6	<5 (Fringing Fields)
C_{IS}	6,720	6,720
C_{RS}	156	156
C_{SR}	.42	<.1 (Fringing Fields)

The next goal is to configure the micromotor capacitance array into a useful arrangement for position measurement. The first step is to simplify the micromotor equivalent circuit shown in Figure 1.4. This is done below in Figure 1.6. The capacitive values listed in Table 1-1 are included in the figure. The stator-substrate capacitors, C_{SS}, are eliminated completely because they are driven by sources. The six stator-rotor capacitances, C_{SR}, are in parallel with the rotor-substrate capacitance, C_{RS}, and are therefore added together to form a single value equal to 160 fF. The impedance of each of the voltage sources driving the stator poles is assumed small compared with the impedance of C_{SR}. Additionally, it is assumed that the voltage sources driving the stator poles have equal and opposite amplitudes, resulting in a zero net contribution to the rotor voltage from these sources.

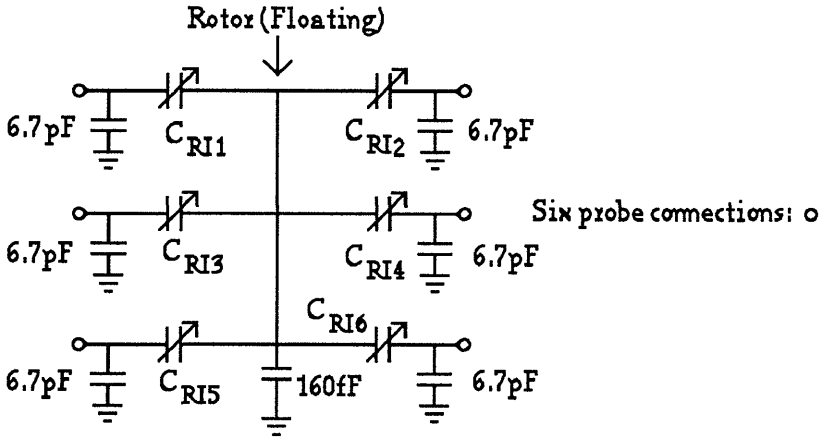

Figure 1.6: Simplified Micromotor Equivalent Circuit

To prepare the micromotor for position sensing, the wire-bonding pads of implant sensors C_{RI1}, C_{RI3}, and C_{RI5} are connected together. This forms a single input capacitance, C_T, equal to the sum of C_{RI1}, C_{RI3}, and C_{RI5}. The

value of C_T as a function of rotor angle is approximately constant and equal to 25 fF; see Figure 1.5. This step also places all three implant-substrate capacitances in parallel, forming a single parasitic capacitance equal to 20 pF. The resulting equivalent circuit is shown below in Figure 1.7.

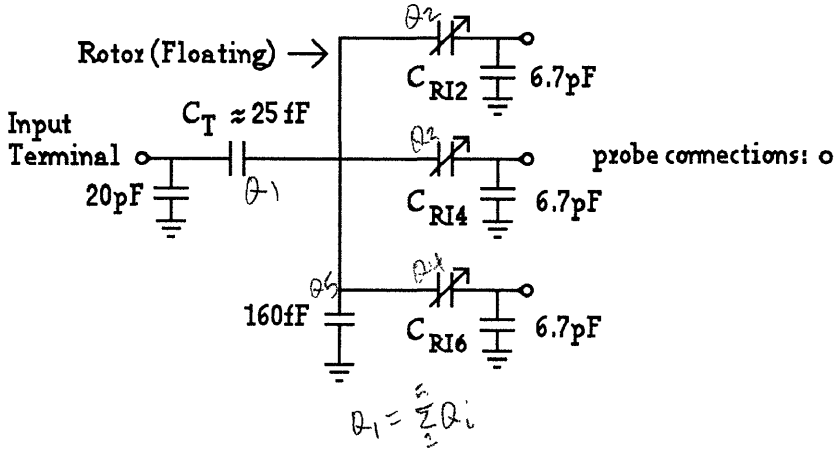

Figure 1.7: Equivalent Rotor Schematic for Measurement

Further simplification to the micromotor schematic shown in Figure 1.7 is possible by examining the effect of placing an ac signal at the input terminal to the capacitance array. The large 20 pF parasitic capacitor is now driven by a source and can henceforth be ignored. The rotor voltage is determined by a capacitor-divider relationship between C_T and the combination of the remaining capacitors to the right. From the rotor's point-of-view, the impedance of the series combination of a sensor capacitor and the 6.7 pF parasitic capacitor is dominated by the sensor capacitor. This statement assumes that the impedance of the load attached to the sensor capacitor is also small compared with the impedance of C_{RI}. Therefore, the voltage potential of the rotor is given by

$$V_{rotor} = V_{in} \frac{C_T}{C_T + C_{RI2} + C_{RI4} + C_{RI6} + 160\text{fF}} \qquad (1\text{-}5)$$

The sum of C_{RI2}, C_{RI4}, and C_{RI6} is identically equal to C_T; see Figure 1.5. The rotor potential is therefore independent of position and equal to $25\text{fF} \bullet V_{in}/(160\text{ fF} + 50\text{ fF}) = 0.12V_{in}$. With an ac source applied to the input terminal of the capacitance array, the equivalent rotor schematic shown in Figure 1.7 is simplified into the model shown in Figure 1.8. The micromotor

model for the measurement of an individual rotor-implant capacitive sensor is shown below in Figure 1.9.

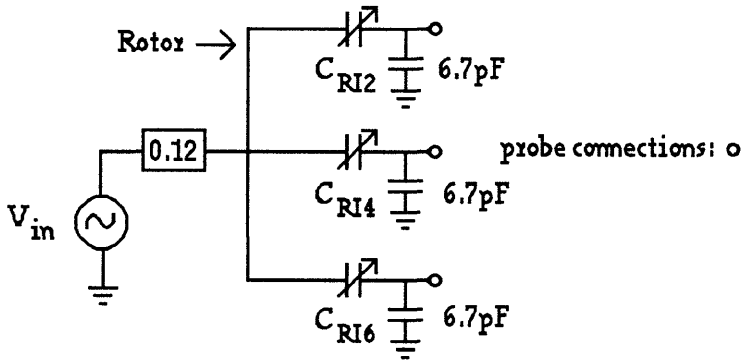

Figure 1.8: Simplified Micromotor Model for Measurement Purposes

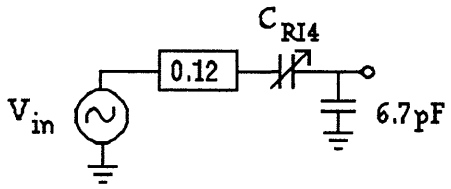

Figure 1.9: Micromotor Capacitance Model for a Single Capacitive Sensor

The single-sensor micromotor model given in Figure 1.9 presents a useful form from which the best method of measuring the value of C_{RI} is determined.

The constraints on the amplitude and frequency of the drive voltage, V_{in}, are determined by operational characteristics of the motor. The excitation frequency, f, required to permit an accurate output voltage proportional to the instantaneous rotor position is determined by how fast the micromotor can spin. The excitation frequency needs to be at least an order of magnitude larger than the inverse of the time required for one rotor blade to completely pass over one sensor. For the micromotor shown in Figure 1.1, this value is four times the rotor frequency. Additionally, this constraint insures that the current through the sensor capacitor due to changes in the drive voltage is much larger than the current through the sensor capacitor due to changes in the value of the sensor capacitor ($CdV/dt >> VdC/dt$). It is desirable to suppress the VdC/dt term as much as possible because the added voltage at the output due to changes in the sensor capacitance creates an error that is

proportional to the speed of the motor. The fastest micromotors to date have been run at 15,000 rpm. The electronics, however, have been the performance-limiting factor [6]. The maximum possible motor speed is likely much faster than this and can be estimated by measuring the rise-time of rotational start-up transients for the micromotor. Experiments performed by Stephen Bart and others [7] have shown rise-times as small as 40 μsec. To obtain 10 sample points during this risetime requires the excitation frequency of V_{in} to be 1/4μsec = 250kHz. To be conservative, the frequency for V_{in} is chosen to be four times this frequency, or 1 MHz.

The amplitude of the drive signal, V_{in}, is limited by electrostatic forces present between the rotor and the sensor electrodes. As the voltage on the sensor electrodes increases, the downward force exerted on the rotor increases, causing the friction between the rotor bushing and the silicon-nitride layer to become larger. The voltage eventually reaches a point when the friction is sufficiently large to prevent the rotor from turning. The maximum amplitude of V_{in} is estimated by comparing the motor drive torque (provided by the stators) with the torque due to friction between the rotor and the silicon-nitride layer. The pull-down force on the rotor is approximately equal to

$$F = \frac{\varepsilon V^2 A}{2x} \tag{1-6}$$

where V is the amplitude of the applied voltage, A is the area of the sensor electrode, ε is the permittivity of the material between the rotor and the sensor, and x is the distance between the sensors and rotor. The torque asserted on the rotor due to this pull-down force is equal to

$$\tau = F\mu r \tag{1-7}$$

where μ is the coefficient of friction between the rotor and the silicon-nitride layer and r is the radius of the contact point between the rotor and Si_3N_4. The value of the torque supplied to the rotor from the stators [7] is about 10 pN•m for stator drives of ±95 V. Therefore

$$\frac{\varepsilon V^2 A\mu r}{2x^2} = 10\text{pN} \bullet \text{m} \tag{1-8}$$

The term ε/x for the two-dielectric spacing is derived earlier in this chapter to be 3.47×10^{-9} F/cm^2. The separation between the rotor and the sensor pad, x, is 0.6 μm. Since three sensor probes are connected together, the area, A, is equal to three times the area of a single probe, which is derived earlier in this chapter to be 420 μm^2. Therefore, A = 1260 μm^2. The bushing radius for these micromotors is about 25 μm. A typical value for the friction coefficient, μ, is 0.35 [7]. Solving Equation 1-8 reveals V = 18 V. For stator drives of ±65 V, the critical voltage, V, drops to 10 V. The maximum drive voltage for the sensors must therefore be significantly lower than this value to prevent the motor from locking up. A the maximum amplitude for V_{in} is chosen to be 2 V.

1.2 Capacitance Measurement:

Four main techniques can be identified for measuring capacitance. These include the direct method, the bridge method, the open-loop method, and the closed-loop method [8].

The direct method of capacitance measurement uses a simple ac source and current detector, as shown in Figure 1.10. Since the current through a capacitor is equal to the product of the capacitor value and the time derivative of the voltage placed across the capacitor (I = CdV/dt), exciting the desired capacitor with an ac signal yields an output current with an amplitude proportional to the value of the capacitance.

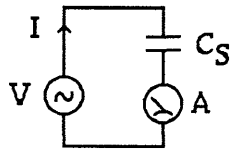

Figure 1.10: Direct Measurement Using an AC Current Detector

The circuit shown in Figure 1.10 benefits from its simplicity. Additionally, the large parasitic capacitances, C_{IS}, are rendered ineffectual because one side of C_S is tied to a source and the other to ground. However, the current output is not directly accessible. To obtain an output that can be used in a control loop, a current sensor (i.e. a resistor) is required in series with the capacitor. With a 1 V input, 1 MHz signal and a 1 fF capacitance, a resistor of 1 MΩ is required to obtain an output voltage on the order of mV. With the introduction of a resistor, the sensor capacitor is no longer directly connected

to ground. The sensor resistor is placed in parallel with the large parasitic capacitance, C_{IS}, as shown in Figure 1.11.

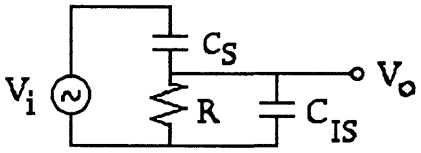

Figure 1.11: Direct Measurement with Sensor Resistor and Parasitic Cap.

The output voltage, V_o, is equal to $sRC_sV_i/(sR(C_s+C_{IS}) + 1)$. Since $C_{IS} >> C_s$, $V_o \approx s(C_s/C_{IS})V_i/(s+1/(RC_{IS}))$. For the values of R = 1 MΩ, $\omega = 2\pi$(1 MHz), and C_{IS} = 6.7pF, $s >> 1/(RC_{IS})$ and therefore, $V_o \approx V_i(C_s/C_{IS}) = V_i \bullet (1.5 \times 10^{-4})$. The large parasitic capacitance severely attenuates the drive signal, undermining the applicability of this method for capacitance measurement.

The second method of measuring capacitance utilizes the concept of the Wheatstone Bridge. The capacitor to be measured, sensor capacitor C_S, is placed in one arm of the bridge. The system is then balanced by adjusting one of the known capacitors. An AC signal excites the circuit and an AC detector monitors the bridge current resulting from changes in the sensor capacitor. The circuit diagram for this method is shown in Figure 1.11.

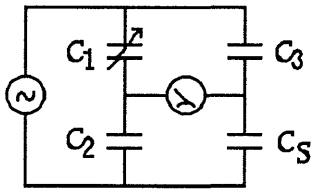

Figure 1.11: Capacitance Bridge

This circuit shown in Figure 1.11 also benefits from its simplicity. The advantage of this circuit over the previous circuit is improved sensitivity of the output due to changes in the sensor capacitance. However, since one side of the sensor capacitance is not tied to a source, the large parasitic capacitance, C_{IS}, is positioned in parallel with the sensor capacitance, C_{RI}. Since $C_{IS} \approx 650C_{RI}$, C_{IS} completely dominates the total value seen by the bridge. Any change in the rotor-implant capacitance is less than 0.2 percent of the implant-substrate capacitance, making accurate position sensing next to impossible.

A third method for measuring capacitance is the open-loop method, shown below in Figure 1.12.

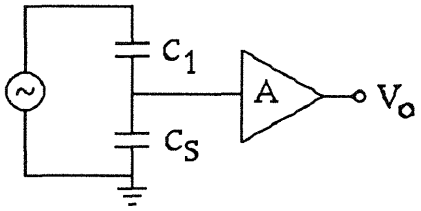

Figure 1.12: Open-Loop Capacitance Measurement

The circuit shown in Figure 1.12 has the advantage of very high sensitivity due to the large gain element. However, like the Wheatstone Bridge, the large parasitic capacitance, C_{IS}, all but obscures the sensor capacitance.

The fourth method for measuring values of unknown capacitors uses a closed-loop amplifier. The circuit is shown in Figure 1.13.

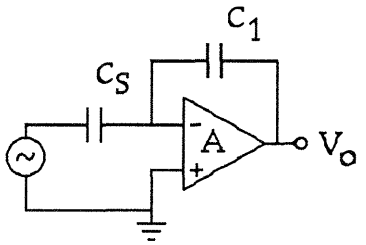

Figure 1.13: Closed-Loop Capacitance Measurement

The circuit shown in Figure 1.13 has a smaller gain (and hence lower sensitivity) than the open-loop method, but has greater stability in the presence of environmental stimuli. Most importantly, the negative feedback inherent to the design has the added advantage of forcing the negative input terminal to a potential which is equal to $-(V_+ + V_{out}/A)$, where A is the open-loop gain of the operational amplifier. With the positive terminal grounded and a large open-loop gain, the voltage at the negative terminal is very nearly equal to zero. This potential is referred to as a virtual ground. Therefore, the voltage across the large parasitic capacitance between the implant and the substrate, C_{IS}, is very small. With such a small voltage across C_{IS}, the current diverted through the capacitor is also very small. Thus, the presence of the virtual ground at the sensor capacitor terminal suppresses the shunting effect of the parasitic capacitor.

The huge advantage of the virtual ground in the closed-loop method make it the obvious choice to be used as the building block of a capacitance measurement circuit for micromotor position sensing.

1.3: Chapter Outline

The following chapters present a chronological progression of the design effort, beginning with an examination of a proposed design and culminating with a presentation of experimental data from the implementation of a more practical final design.

The initial circuit design for capacitance measurement is examined in Chapter 2 and is based on a topology first proposed by D. Marioli, E. Sardoni, and A. Taroni [9]. The design expands on the closed-loop measurement technique discussed in Section 1.2. The chapter begins with a mathematical analysis of the ideal circuit. An examination of the effect of error sources on the performance of the design is discussed. This is followed by a computer simulation of the circuit to confirm the analysis. The results from the analysis in addition to practical issues of circuit implementation lead to the conclusion that this circuit can not be used as the final design.

Chapter 3 takes a look at a modified version of this closed-loop capacitance measurement method. The circuit implementation of the new design is greatly simplified and the performance is improved. Once again, the analysis begins by solving for the circuit behavior mathematically. This is followed by an error analysis and computer simulation. This modified version still suffers from implementation difficulties of one of the circuit blocks. Therefore, further design modifications are made.

The final circuit design is examined in Chapter 4. A new point of view in examination of the entire circuit leads to modifications which simplify the design even more. Additionally, the feasibility of implementation is greatly improved. The chapter follows the pattern of its predecessors with mathematical and computer analysis. Following these sections is a presentation which includes the details of the final circuit construction, experimental results, and a discussion of the recorded data with emphasis on discrepancies with predictions. The experiments are conducted with small-valued macroscopic capacitors. Tests on actual micromotors are not performed as part of this thesis because there are presently no buffer

amplifiers on chip to suppress the effects of large variable parasitic capacitances between wires bonded to the pads.

The thesis concludes with a summary of the design and suggestions for future improvements. Included in this discussion are upgrades in micromotor fabrication which are necessary to successfully interlink the integrated micromotor and the discreet capacitive sensor circuit.

Chapter 2: Initial Design

An examination of the basic capacitive measuring techniques, given in Section 1.2, concludes that the best method for capacitive measurement with application of micromotor position sensing is based on the closed-loop amplifier. One idea which expands upon the closed-loop amplifier method for measuring capacitance [9] is proposed by D. Marioli, E. Sardoni, and A. Taroni. The circuit is shown below in Figure 2.1.

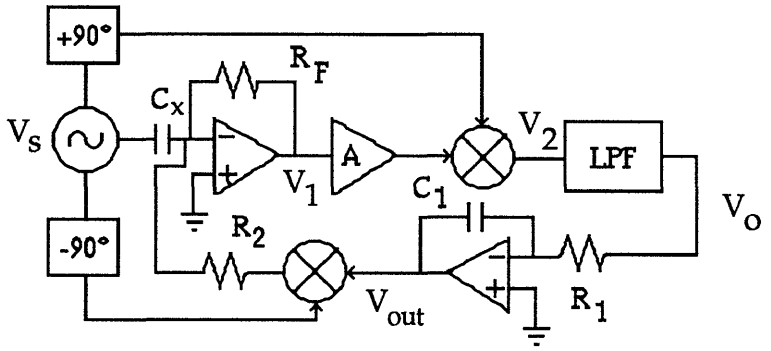

Figure 2.1: Capacitance Measurement Circuit

The circuit shown in Figure 2.1 is designed to produce an output voltage, V_{out}, which is proportional to the value of the capacitance to be measured, C_x. The block labeled "LPF" is a low-pass filter. The +90° and -90° blocks perform the function of shifting the phase of the input voltage the appropriate number of degrees.

2.1 Analysis:

An ac voltage source, $V_s = V\sin(\omega t)$, is connected to one terminal of the sensor capacitor, C_x. The current through this capacitor is equal to the product of its present value and the derivative of the voltage across the capacitor ($I_{Cx} = C_x dV_{Cx}/dt$). The other end of the sensor capacitor is attached to the negative terminal of the operational amplifier. With the amplifier in a negative feedback configuration, this node is held at virtual ground, assuming that the open-loop gain of the op-amp is large. The total voltage across C_x is therefore equal to V_s and the resulting capacitor current is

$$I_{Cx} = VC_x\omega\cos(\omega t) \tag{2-1}$$

This current is converted to a voltage by R_F such that

$$V_1 = -VR_FC_x\omega\cos(\omega t) \tag{2-1}$$

Following a non-inverting amplifier stage, the signal is multiplied by the input voltage shifted by 90°, resulting in a voltage at V_2 given by

$$V_2 = -AVR_FC_x\omega\cos^2(\omega t)/B_F \tag{2-2}$$

where B_F is the voltage scaling factor of the forward multiplier. The low-pass filter removes the ac component of V_2 resulting in a dc voltage at V_o equal to

$$V_o = -AVR_FC_x\omega(0.5/B_F) \tag{2-3}$$

The feedback loop first integrates V_o, $V_{out} = -(1/R_1C_1)\int V_o dt$. V_{out} is then multiplied by the input voltage shifted by -90° (-Vcos(ωt)). This value is converted to a current by R_2 which is added to the input current from the sensor capacitor. The -90° phase shift is necessary to insure that the two currents are 180° out-of-phase. With the loop closed, the total voltage at V_o is

$$V_o = \left(\frac{V_{out}}{B_1R_2} - C_x\omega\right)\frac{AVR_F}{2B_F} \tag{2-4}$$

B_1 is the denominator voltage setting of the feedback multiplier. If $V_{out}/B_1R_2 > C_x\omega$, then V_o is positive and the integrator capacitor accumulates more positive charge, reducing the value of V_{out}. If $V_{out}/BR_2 < C_x\omega$, the opposite occurs. A negative value at V_o charges the integrator capacitor more negative, thereby increasing the value of V_{out}. Consequently, the output voltage settles to a value such that the voltage at V_o is zero, assuming that the closed-loop system is stable. This fact dictates that in the steady-state, the magnitude of the current through R_2 is exactly equal and opposite to the magnitude of the current through the sensor capacitor ($V_{out}/BR_2 = C_x\omega$). Therefore, the final value of V_{out} is directly proportional to the sensor capacitance, C_x, according to

$$V_{out} = BR_2C_x\omega \tag{2-5}$$

A more rigorous mathematical analysis of the circuit begins with an examination of a block diagram shown below in Figure 2.2. The diagram is derived by arranging the input/output relations between the circuit nodes of the schematic pictured in Figure 2.1 into .

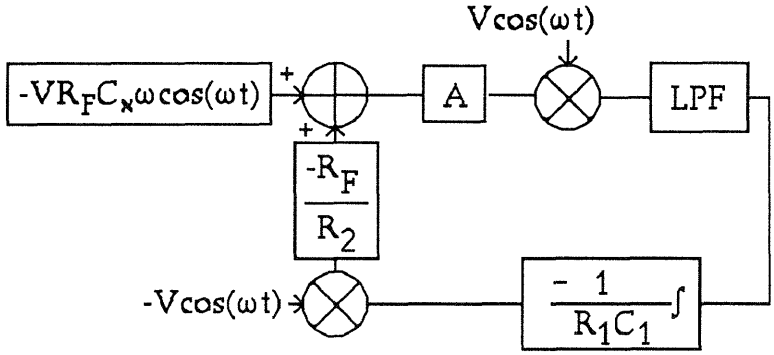

Figure 2.2: Block Diagram of the Capacitance Measurement Circuit

With some elementary block manipulation, the diagram shown in Figure 2.2 is simplified into the layout shown in Figure 2.3.

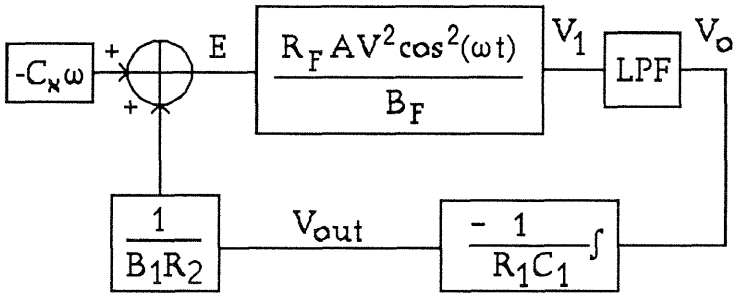

Figure 2.3: Simplified Block Diagram

V is the amplitude of the input sinusoid and B is the scaling factor in the denominator of the multiplier. The low-pass filter is a fourth-order Butterworth filter.

The static analysis of the circuit is straight-forward. With an integrator present in the loop, the steady-state error of the system, $E = -C_x\omega + V_{out}/BR_2$, must be zero. As previously mentioned, if the error is not zero, then charge is either added or removed from the integrator capacitor in such a manner as to return the error signal to zero. Therefore, in steady-state operation,

$$V_{out} = B_1R_2C_x\omega \qquad (2\text{-}6)$$

The result is the same as derived earlier in Equation 2-5.

The dynamic analysis of the circuit is a bit more involved. The three governing differential equations of the system are

$$V_1 = \left[-C_x\omega + \frac{V_{out}}{B_1R_2}\right]\frac{R_F A V^2}{B_F}\left(\frac{1}{2} + \frac{1}{2}\cos(2\omega t)\right) \tag{2-7}$$

$$\frac{dV_{out}}{dt} = -\frac{1}{R_1C_1}V_o \tag{2-8}$$

$$\frac{d^4V_o}{dt^4} = K_1\frac{d^3V_o}{dt^3} + K_2\frac{d^2V_o}{dt^2} + K_3\frac{dV_o}{dt} + K_4V_o + K_5V_1 \tag{2-9}$$

The first two equations are derived directly from the block diagram shown in Figure 2.1.2. Equation 2-9 is the input-output relationship for the fourth-order low-pass filter. The filter is implemented using two consecutive Sallen-Key circuits, as shown in Figure 2.1.3.

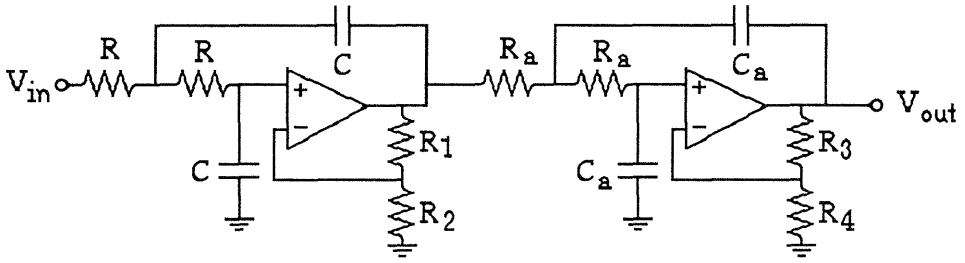

Figure 2.4: Fourth-Order Sallen Key Low-Pass Filter

For a Buttorworth filter, $R_a = R$ and $C_a = C$ so that the constants of Equation 2-9 [10] are defined as

$$K_1 = -(\frac{1}{RC})(6 - G_1 - G_2) \tag{2-10}$$

$$K_2 = -(\frac{1}{RC})^2(2 + (3 - G_1)(3 - G_2)) \tag{2-11}$$

$$K_3 = -(\frac{1}{RC})^3(6 - G_1 - G_2) \tag{2-12}$$

$$K_4 = -(\frac{1}{RC})^4 \tag{2-13}$$

$$K_5 = G_1 G_2 \left(\frac{1}{RC}\right)^4 \tag{2-14}$$

G_1 and G_2 are the values for the gain of the first and second stages of the Sallen-Key circuit respectively: $G_1 = (R_1+R_2)/R_2$ and $G_2 = (R_3+R_4)/R_4$. The RC time constant is set to the value of the 3 dB frequency of the filter, ω_o. Equations 2-7 through 2-14 can be simplified into the matrix form

$$\frac{d}{dt}\begin{bmatrix} V_{out} \\ V_o \\ \dot{V}_o \\ \ddot{V}_o \\ \dddot{V}_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{R_1C_1} & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ K_5\frac{R_F A V^2}{2B_1 B_F R_2} & K_4 & K_3 & K_2 & K_1 \end{bmatrix} \begin{bmatrix} V_{out} \\ V_o \\ \dot{V}_o \\ \ddot{V}_o \\ \dddot{V}_o \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ K_6 \end{bmatrix} \tag{2-15}$$

$$K_6 = -\frac{C_x \omega R_F A V^2}{2B_F (RC)^4} G_1 G_2 \tag{2-16}$$

The solution to the standard differential equation $\dot{x} = Ax + Bu$ [9] where A and B are matrices is

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + \int_{t_0}^{t_1} e^{A(t_1-t)}Bu(t)dt \tag{2-17}$$

The value of the definite integral is derived in Appendix 1 under the assumption that u(t) is constant. This allows the computation of step responses according to

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + A^{-1}\left[e^{A(t_1-t_0)} - I\right]Bu \tag{2-18}$$

where I is the identity matrix and has the same dimension as $e^{A(t1-t0)}$.

The dynamic performance of the circuit in response to a step change in sensor capacitance is ascertained by computing Equation 2-18 in incremental steps over the desired time interval. The computer application chosen to perform this task is MATLAB. From Equation 2-15, the values of matrices A and B are

$$A=\begin{bmatrix} 0 & -\frac{1}{R_1C_1} & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ K_5\frac{R_FAV^2}{2B^2R_2} & K_4 & K_3 & K_2 & K_1 \end{bmatrix} \qquad B=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ K_6 \end{bmatrix} \tag{2-19}$$

where the constants K_1 through K_5 are defined in Equations 2-10 through 2-14. Constant K_6 is repeated here as

$$K_6=-\frac{C_x\omega R_FAV^2}{2B_F(RC)^4}G_1G_2 \tag{2-20}$$

The initial condition vector, x(0), is set to the steady-state value of the system before the instance of the step. From Equation 2-1, the quiescent value of V_{out} is equal to $B_FR_2C_x\omega$. The quiescent values for V_o and its derivatives are zero. The resulting initial vector is

$$x(0)=\begin{bmatrix} BR_2C_x\omega \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{2-21}$$

To simulate the dynamic performance of V_{out} due to a step in capacitance from 10 fF to 5 fF, the MATLAB file is evaluated with the sensor capacitance, C_x, set to 10 fF in the initial condition vector (Equation 2-21) and C_x set to 5 fF in the input vector, B (Equation 2-19).

The next task is to assign values to all the circuit parameters. The requirements for drive frequency, f, and amplitude, V, are determined in Section 1.1 as 1 MHz and 2 V respectively. The global feedback resistor, R_2, is chosen such that V_{out} maintains a reasonable value in the steady-state for the range of the sensor capacitor, C_x. From Equation 2-6, $R_2 = V_{out}/(BC_x\omega)$. The default value for the multiplier denominator voltage, B_1, is 10V. The frequency, ω, is 2π(1 MHz) and the sensor capacitor ranges from zero to 10 fF. Therefore, $0 < V_{out} < 2\pi \times 10^{-7}R_2$. A value of R_2 = 1 MΩ keeps the output

voltage at a reasonable value without making the global feedback resistor overly large.

The feedback resistor of the differentiator, R_F, sets the gain of the differentiator; $H(s) = -R_F C_x s$. To make this gain equal to unity for the 1MHz input signal, $R_F = 1/(C_x\omega) = 16\ M\Omega$ for $C_x = 10$ fF. When the sensor capacitor is less than 10 fF, the gain of the amplifier is less.

The Sallen-Key filter parameters include the two gain stages, G_1 and G_2, and the resistor and capacitor values. For a four-pole Buttorworth low-pass filter, the values for G_1 and G_2 are 1.152 and 2.235 respectively [11]. The RC product determines the filter bandwidth, $RC = 1/\omega_{3dB}$. To remove the ac components of the squared sinusoid at V_2, the bandwidth of the filter must be significantly less than 1 MHz. However, the bandwidth must be large enough to be certain that the rise-time of the closed-loop circuit is faster than the 40 μsec rise time of the rotor dynamics. Two different bandwidths, 50kHz and 200kHz, are analyzed and compared.

The values of the feedback integrator capacitor, C_1, and resistor, R_1, only impact the gain of the overall loop. Equation 2-22 is derived from the block diagram in Figure 2.3. It shows the parameters which have an impact on the loop gain. This results in

$$G_{loop} = \frac{1}{2}\frac{R_F}{R_2}\frac{AV^2}{B_F B_1}\frac{G_1 G_2}{R_1 C_1} \qquad (2\text{-}22)$$

G_1 and G_2 are the gains of the two Sallen-Key filter stages. R_1 and C_1 are used in the analysis to vary the loop gain. Each of the two filter bandwidth cases is analyzed for three different values for the loop-gain. Table 2-1 summarizes the values of the circuit elements and parameters used in the numerical analysis.

The MATLAB file used to compute the solution to the dynamic behavior is shown in Appendix 2. The step response of the 50kHz case is graphed in Figure 2.5. The 200kHz case is plotted in Figure 2.6.

Table 2-1: Parameter Values

Component	50kHz	200kHz	Comments
A	1	1	Gain of Buffer Amp
B_F	10V	10V	Denominator of Forward Multiplier
B_1	10V	10V	Denominator of Feedback Multiplier
V	2V	2V	Amplitude of Input sine
G_1	1.152	1.152	Gain of Filter Stage 1
G_2	2.235	2.235	Gain of Filter Stage 2
C	.001μF	.001μF	Filter Capacitor
R	3200Ω	800Ω	Filter Resistor
C_x	10fF	10fF	Step down from 10fF
	5fF	5fF	to 5fF
C_1	.01μF	.01μF	Integrator Capacitor
R_1	1000Ω	250Ω	Integrator Resistor
	1500Ω	500Ω	Used to Vary the loop
	2000Ω	750Ω	Gain
R_2	1MΩ	1MΩ	Feedback R
R_F	16MΩ	16MΩ	differentiator feedback R
ω	2πMrps	2πMrps	Input frequency

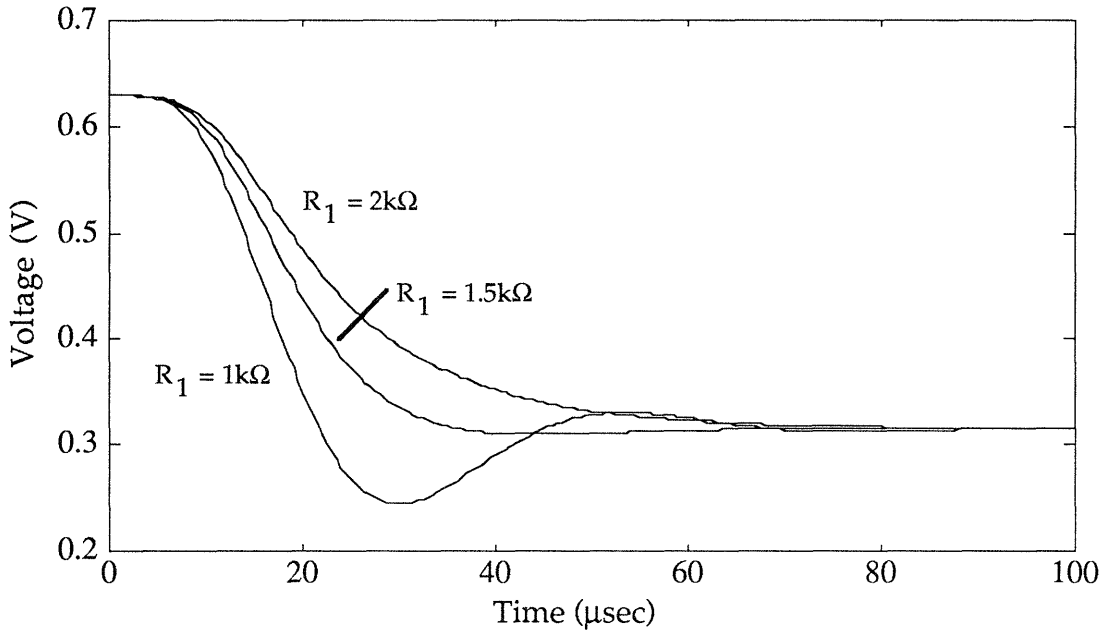

Figure 2.5: Results for 50kHz Bandwidth

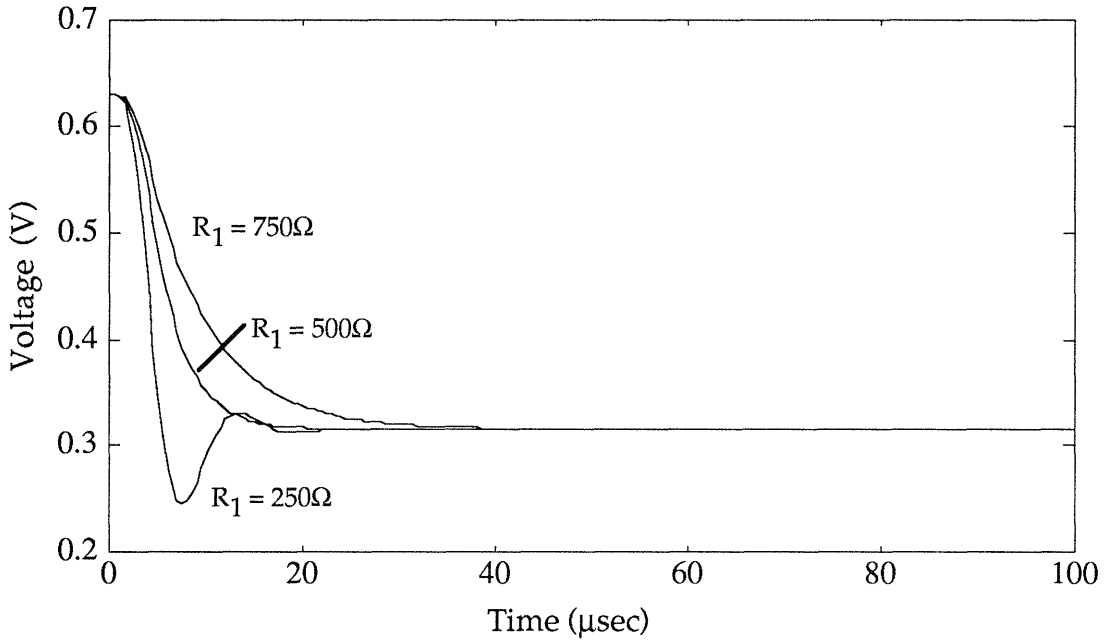

Figure 2.6: Responses for 200kHz Bandwidth

The responses shown in Figures 2.5 and 2.6 show a typical second-order dynamic response to a step change in input. The no-overshoot 50kHz settling

time to .1% is 73 μsec. The settling time for the 200 kHz bandwidth is 25 μsec. The rise-time of the two are cases are about 18 μsec and 50 μsec for the fastest no-overshoot responses in the 200 kHz and 50 kHz cases respectively. The steady-state value of the output voltage for C = 5 fF is 0.314 V. The analytical expression for the steady-state output voltage is given in Equation 2-1 as $BR_2C_x\omega = 10*1x10^6*5x10^{-15}*2\pi*1x10^6 = 0.314$ V.

The risetime of the no-overshoot transient response due to a step in sensor capacitance for the 50kHz bandwidth case, shown in Figure 2.5, is not fast enough to accurately measure the position of the micromotor. The speed-of-response of the circuit with the 200kHz filter is faster than the 40 μsec rise-time of the micromotor.

A more efficient method for finding the optimal loop gain for fast risetime without overshoot is the root-locus technique. For a system represented by the equation dx/dt + Ax = Bu, the closed-loop poles are equal to the eigenvalues of the matrix A [13]. Using MATLAB, the eigenvalues of A are calculated for many values of the loop gain using Equation 2-22. Resistor R_1 is the parameter used to vary the gain. The value of R_1 is stepped in increments of 20 Ω between 1 Ω and 2 kΩ. The root-locus plot for the case with the filter bandwidth equal to 200kHz is shown below in Figure 2.7.

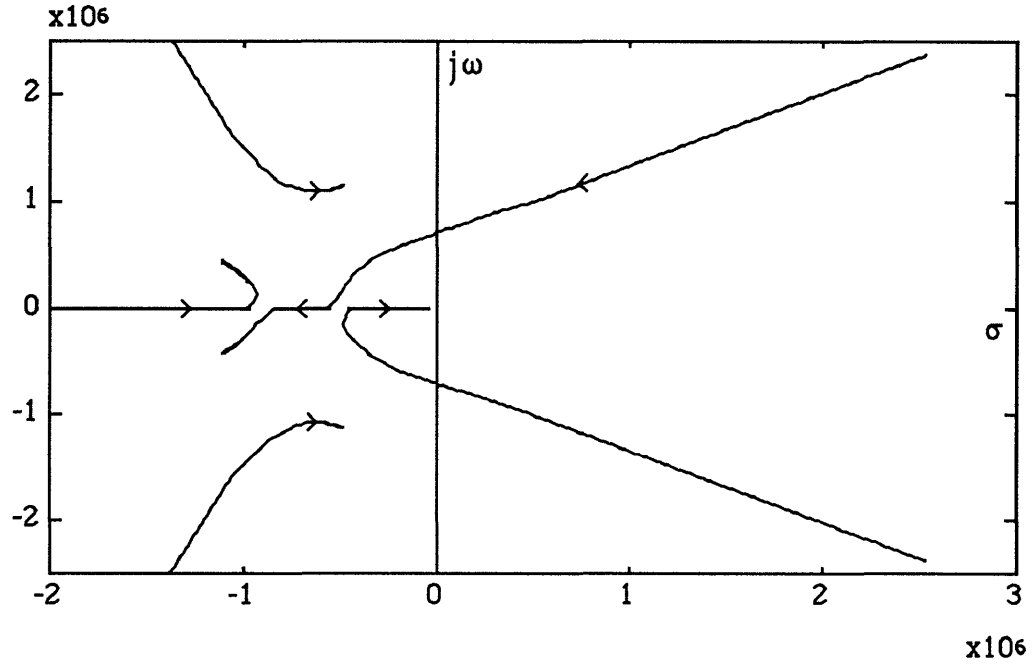

Figure 2.7: Root-Locus with a 200kHz Low-Pass Filter

The arrows labeled on the root-locus plot in Figure 2.7 indicate the direction of pole movement for increasing values of R_1 (decreasing loop-gain). The two poles which traverse the right-half plane dominate the circuit dynamics at higher gains. The system is unstable as long as these poles remain in the right-half plane. From the output data of the MATLAB file, the minimum value of R_1 required for the system to be stable is 120 Ω. The no-overshoot risetime of the step response is maximized when the loop gain is such that the two dominant poles meet on the σ axis. The value for R_1 to meet this condition is 480 Ω. The step response for R_1 = 500 Ω, which is shown in Figure 2.6, is close to the optimal behavior for the circuit.

So far, the entire analysis has assumed that all circuit components are ideal. The next step in this progressive analysis is to simulate the circuit with the non-idealities taken into account. The most important of these effects are native to the operational amplifiers, including the input buffers in the analog multipliers. The non-idealities include input bias currents, offset voltage, and the frequency dependence of the open-loop gain. Figure 2.8 shows a model of an op-amp with several of the non-ideal characteristics taken into account.

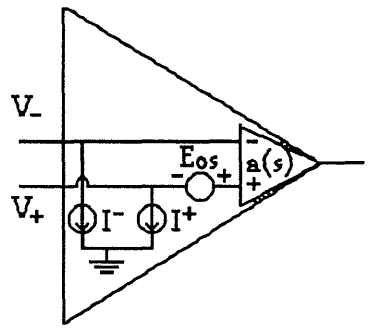

Figure 2.8: Model of "Real" Op-amp

The first variation from ideal is the dependence on frequency of the open-loop gain of the operational. Internally compensated op-amps are designed to exhibit a dominant pole around 100Hz to insure ample phase margin at unity gain cross-over. When this op-amp is implemented in a differentiator configuration as shown in Figure 2.1, two problems result. The RC feedback network adds an additional pole which contributes up to 90 degrees of phase shift to the loop. This reduces the phase margin and may result in instability. Second, the closed-loop gain of the circuit increases by

6dB per octave, allowing the amplifier to become susceptible to high frequency noise. Both of these problems are solved by the addition of a compensating lead network. The ideal differentiator and the "practical" differentiator are shown below in Figure 2.9.

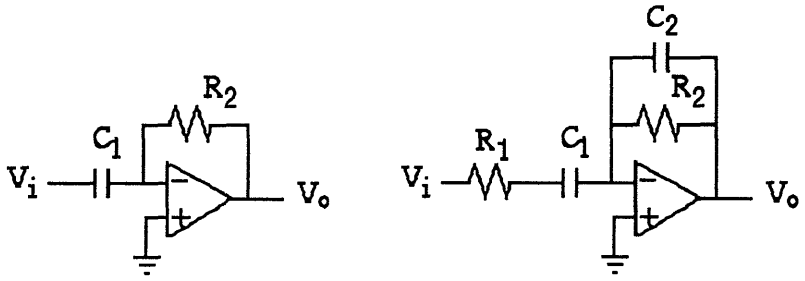

Figure 2.9: Ideal Differentiator Practical Differentiator

To better understand the frequency characteristics of the two differentiators, block diagrams of the above circuits are shown in Figures 2.10 and 2.11.

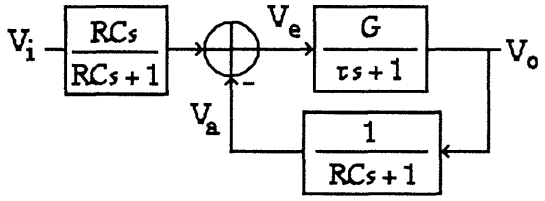

Figure 2.10: Block Diagram for the Ideal Differentiator

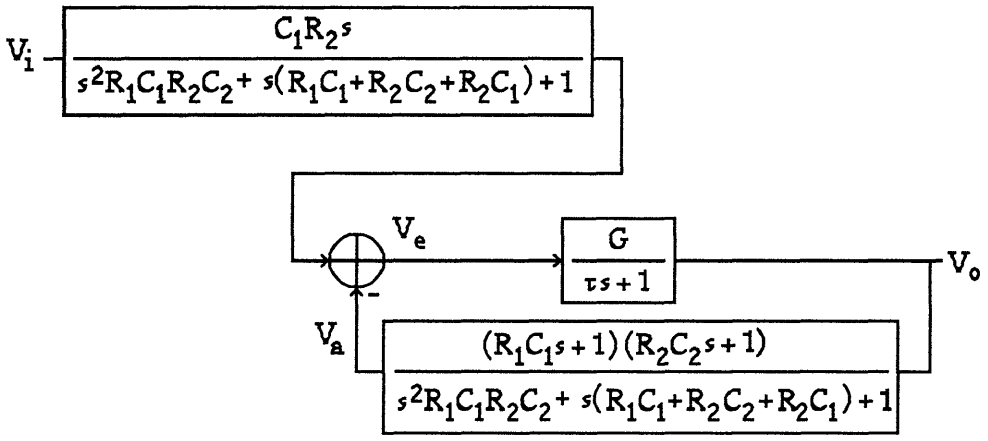

Figure 2.11: Block Diagram for the Practical Differentiator

The new components, R_1 and C_2, add a lead network to the loop which consists of two zeros and a pole. The zeros are located at $1/2\pi R_1C_1$ and $1/2\pi R_2C_2$. When the zeros are placed in the vicinity of unity-gain crossover, the added phase insures stability. When $R_2C_1 >> R_1C_1$ and R_2C_2, the poles of the feedback network are approximately located at $1/2\pi R_2C_1$ (the same pole as in the uncompensated version) and $1/2\pi R_1C_2$ (the lead-network pole).

The closed-loop response is altered with the addition of two poles. When the open-loop zeros are placed well below the unity-gain frequency of the op-amp, by a factor of 10 or so, the closed-loop poles are located approximately at the same location as the open-loop zeros. These poles then "roll-off" the transfer function above the frequency of interest and below the open-loop gain curve. This reduces high-frequency closed-loop noise. With $R_2C_1 >> R_1C_1$ and R_2C_2, the closed-loop unity-gain frequency of the compensated differentiator is still located at $1/2\pi R_2C_1$.

The next step is to choose a standard operational amplifier to be used in the differentiator. For good circuit performance, the specifications for the differentiator op-amp include unity-gain stability, a high degree of precision, and a wide bandwidth. The AD843K fits the first two criteria and has a gain-bandwidth product of 34 MHz. With an open-loop gain of 40,000, the dominant pole is located at 850 Hz. Capacitor C_1 (the sensor capacitance, C_x) has a maximum value of 10 fF. From Table 2-2, R_2=16MΩ. The compensating zeros are both placed at 10MHz, a factor of 3 below the unity-gain frequency of the op-amp and factor of 10 above the closed-loop unity-gain frequency. This sets the values of R_1 = 1.59MΩ and C_2 = 1fF. Using these values, Figure 2.12 presents the open-loop transfer functions of the two differentiators shown in Figure 2.1.7 (V_a/V_e). Figure 2.13 shows a bode plot for the closed-loop characteristics of two circuits (V_o/V_i).

The uncompensated differentiator has a second open-loop pole that is located at $1/2\pi R_2C_1$ = 6.2Mrps/2π = 1MHz, a lower frequency than the unity-gain crossover. This pole contributes a significant phase shift and may possibly compromise stability when additional phase shift due to higher-frequency poles is considered. The compensated differentiator adds two lead zeros to the open-loop transfer function followed by a pole. The zeros are both placed at 10MHz and the lead network pole is located at $1/2\pi R_1C_2$ = 100MHz, well beyond the frequencies of interest. The additional components

also have the side effect of moving the second pole (previously located at $1/R_2C_1$) to a slightly lower frequency.

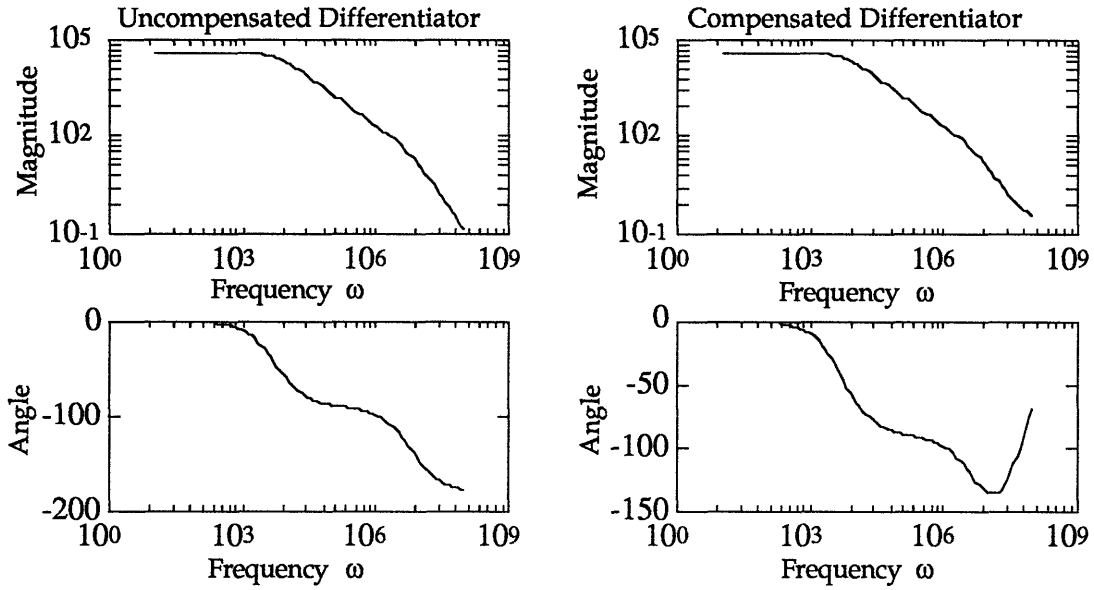

Figure 2.12: Bode Plots for Ideal and Practical Differentiator

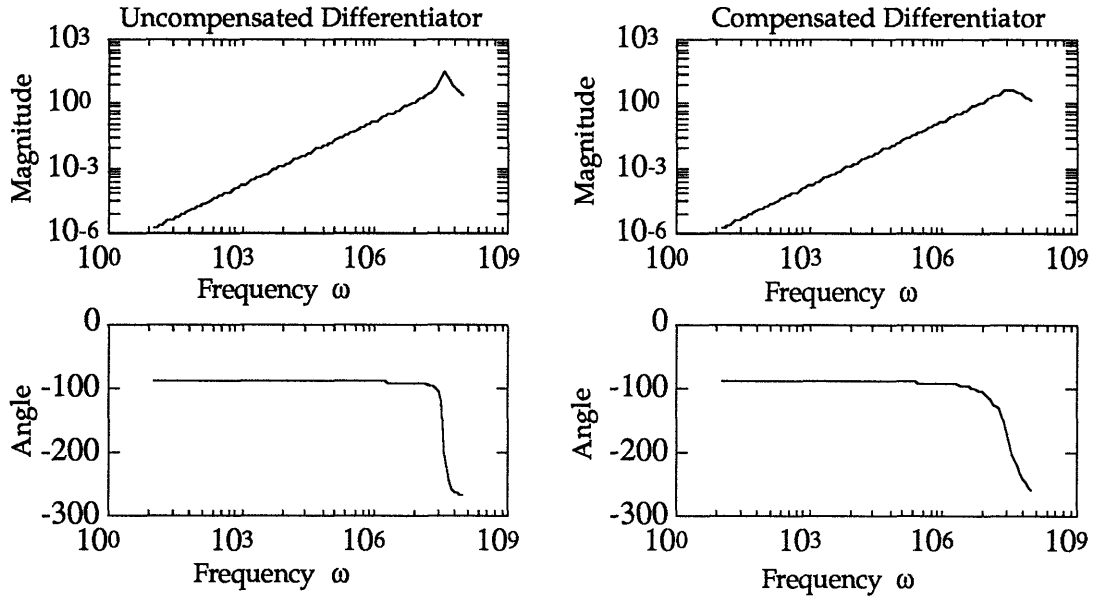

Figure 2.13: Frequency Response of the Closed-Loop Differentiators

The closed-loop transfer characteristic shows the double-pole rolling off the gain above 10MHz. The circuit functions as a differentiator for frequencies

below the double pole location and performs the integrating function for frequencies above this location.

The dominant pole present in the operational amplifier does not present the same problems in the integrator configuration as it does in the differentiator configuration because the RC feedback network adds an open-loop zero. Additionally, the closed-loop bode-plot is a decreasing function of frequency, thereby reducing contributions from high-frequency noise.

For the Sallen-Key filters, the frequency dependence of the gain is not a factor as long as the bandwidth of the filter is much less than the closed-loop bandwidth of the op-amp at the specified gain. The filters have a 200kHz bandwidth and a maximum gain of 2.2. The AD843K operational amplifiers have a bandwidth of 15MHz at a gain of 2.2.

Next, the effect on the output due to the parasitic sources inherent to operational amplifiers is addressed. The most important of these are the input bias current and input offset voltage. Errors in the output voltage due to a single parasitic source can be determined analytically. However, since the circuit is non-linear, superposition does not apply. On the other hand, the non-linearity is due to the presence of the multipliers. If their two inputs are $X + \Delta X$ and $Y + \Delta Y$, then their output is $(XY + X\Delta Y + Y\Delta X + \Delta X\Delta Y)/B$ where B is the divisor voltage of the multiplier. If it is assumed that the $\Delta X\Delta Y$ term is small, then superposition of the parasitic sources will still give an accurate estimate of the change in output voltage due to the parasitic elements. If the $\Delta X\Delta Y$ term is not small, then this component of the error is added in. Figure 2.14 repeats the circuit of Figure 2.1 with the important parasitic elements included.

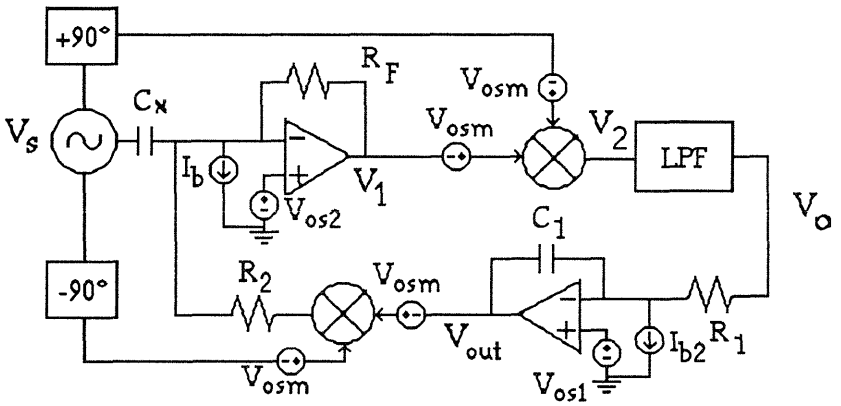

Figure 2.14: Capacitance Measurement Circuit with Parasitic Elements

The sine-wave drive inputs are assumed ideal. The input bias currents of the analog multiplier buffers have little effect on the system because the current is easily supplied by the operational amplifier sources driving the multipliers. The parasitics native to the low-pass filter are ignored for the present.

The three active devices chosen for this circuit include the AD843K op-amp, OP-07A op-amp, and AD734B multiplier. As previously discussed, the AD843K is a good choice for the differentiator operational amplifier because it is has a high degree of precision and very high bandwidth. The integrator op-amp is the OP-07A, an ultra-high precision amplifier. The high bandwidth is unnecessary to perform the integrating function in this circuit because only low-frequency signals are fed into the integrator. The analog multipliers are AD734B. These are high bandwidth multipliers. Table 2-2 shows some of the characteristics of these devices, including the parasitics labeled in Figure 2.13.

Table 2-2: Device Characteristics

Device	GB Product	Offset Voltage	Bias Current
AD843K	34 MHz	1.0 mV	1.0 nA
OP-07A	.4 MHz	25 μV	2.0 nA
AD734B	40 MHz 3dB Input 10 MHz 3dB Output	5 mV	150 nA

The presence of the parasitic sources contribute to an offset error at V_{out}. The first step in calculating the magnitude of this offset is to determine the effect of the parasitic sources on the value of V_o. The dc output voltage of the feedback analog multiplier is equal to $V_{out} \bullet V_{osm}/B$, where B is the denominator voltage. From Table 2-2, V_{osm} = 5mV. For an output voltage of 0.628 V (C_x = 10 fF) and a value of B set to 10 V, this dc error is equal to 0.314 mV. This results in a dc input current to the differentiator of $(0.314mV+V_{os2})/R_2$. The offset voltage of the AD843K op-amp is 1mV. For R_2 = 1 MΩ , this current equals 1.314 nA. The bias current of the AD843K is 1 nA. The sum of these two currents is forced through resistor R_F, creating an offset voltage at V_1 equal to V_{os2} + 2.314 nA$\bullet R_F$. With R_F = 16 MΩ, the voltage at V_1 due to the parasitics is 38 mV. Adding this value to the 5 mV input offset voltage of the analog multiplier results in a value of 43 mV. This voltage is then multiplied by a sine wave with a frequency of 1MHz. The resulting signal is attenuated by the low-pass filter (which has a 3dB point

below 1 MHz) and has little effect on the output voltage, V_o. Note that the 43mV offset is also multiplied by the 5mV offset at the sine-wave input to the multiplier, resulting in a dc output voltage of 215μV. This value is passed by the filter, creating an error at V_o.

Another source of offset at V_o originates from parasitic sources in the integrating op-amp. The bias current at the input to the integrating op-amp is forced through R_1 because the steady-state current through the integrating capacitor, C_1, is zero. This requires a non-zero steady-state voltage at V_o equal to I_bR_1. The bias current of the OP-07A is 2nA from Table 2-2. With a value of R1 = 750Ω, V_o must maintain a value of 1.5μV. The offset voltage of the OP-07A, which equals 25μV, also directly adds to the offset at V_o. Combining the three sources of error at V_o results in a voltage of 242μV not including contributions from the filter.

The offset error present at V_o is next translated to an offset at V_{out}. Since the steady-state voltage at V_o must be zero, the calculated dc voltage due to parasitic sources is negated by the superposition of an equal and opposite dc voltage which originates from the presence of an offset voltage at V_{out}. This is a characteristic of the global feedback. If the system is ideal and in the steady state and a positive quiescent offset voltage suddenly appears at V_o, then the integrator capacitor charges more negative, decreasing the value of V_{out}. This smaller value in turn forces the cosinusoidal current through resistor R_2 to be smaller. Since the input drive is constant, a small cosinusoidal current goes through resistor R_F, thereby creating a negative cosinusoidal voltage at V_1 (Before the offset voltage appeared, the currents through R_2 and C_x were equal and opposite). Multiplying this with the +90° phase-shifted sinusoid creates a negative voltage at V_o, reducing the offset. The system finally settles to a state where the offset at V_{out} corrects for the parasitic sources in the circuit.

Solving for the offset at V_{out} begins by working backwards from V_o. An average of 242 μV requires a steady-state sinusoidal voltage at V_1 of 2B/V where V is the amplitude of the multiplying sine wave. For B = 1 V and V = 2 V, the amplitude of the steady-state sinusoidal error at V_1 is 242 μV. Therefore, the steady-state sinusoidal current through R_F is 242 μV/16 MΩ = 15 pA. The additional voltage required at the output of the feedback multiplier to supply this sinusoidal current is 15 pA•1 MΩ = 15 μV. This value results in an error voltage at V_{out} of 15 μV•2B/V. For B = 10 V and V =

2 V, this value is 0.15 mV. Adding the 5 mV input offset voltage of the feedback analog multiplier results in an error at V_{out} of about 5.2 mV. Note that the input offset voltage of the multiplier dominates over the other errors. The magnitude of the errors in the filter are on the order of the other errors in that part of the circuit and their omission has little effect on the final result.

The total error of 5.2mV is not constant. Since the dc bias current into the differentiator from the output of the feedback multiplier is a function of the output voltage, a scale error is also present at V_{out}. Reworking the error analysis as a function of V_{out} results in

$$V_{outerr} = 5mV + 133\mu V + 25x10^{-6}V_{out} \tag{2-17}$$

The output voltage has an added offset plus a scale error.

An offset voltage at V_{out} of 5 mV translates via Equation 2-5 to a capacitance error of

$$\Delta C = \frac{5mV}{BR_2\omega} \tag{2-18}$$

For the values of B, R_2, and ω listed in Table 2-1, the capacitance error is 0.08 fF or 0.8% of a full-scale value of 10 fF. The scale error translates to 0.4 aF/V or .008%/V. The scale error is so small that its effect is negligible. The offset error is somewhat more significant, but its magnitude is still small. Additionally, a simple offset is fairly easy compensate for with calibration techniques.

Additional errors arise from the sinusoidal drives. Differences in the phase relations plus added offsets will likely contribute to the output error. These error sources are explored a bit more in the next section.

2.2 Computer Simulation

To confirm the previous analysis, the circuit was next simulated using SPICE. With the same set of components listed in Table 2-1, the circuit was simulated for 100μsec. The initial value of the output voltage is 0.628V, the steady-state value when C_x = 10fF. To simulate a step in capacitance, the sensor capacitance is set to 5fF. The results of this step transition with the bandwidth of the low-pass filter set to 50kHz is graphed in Figure 2.15. The 200kHz

bandwidth simulation is shown in Figure 2.16. An example of the SPICE file used to perform the analysis is given in Appendix 3.

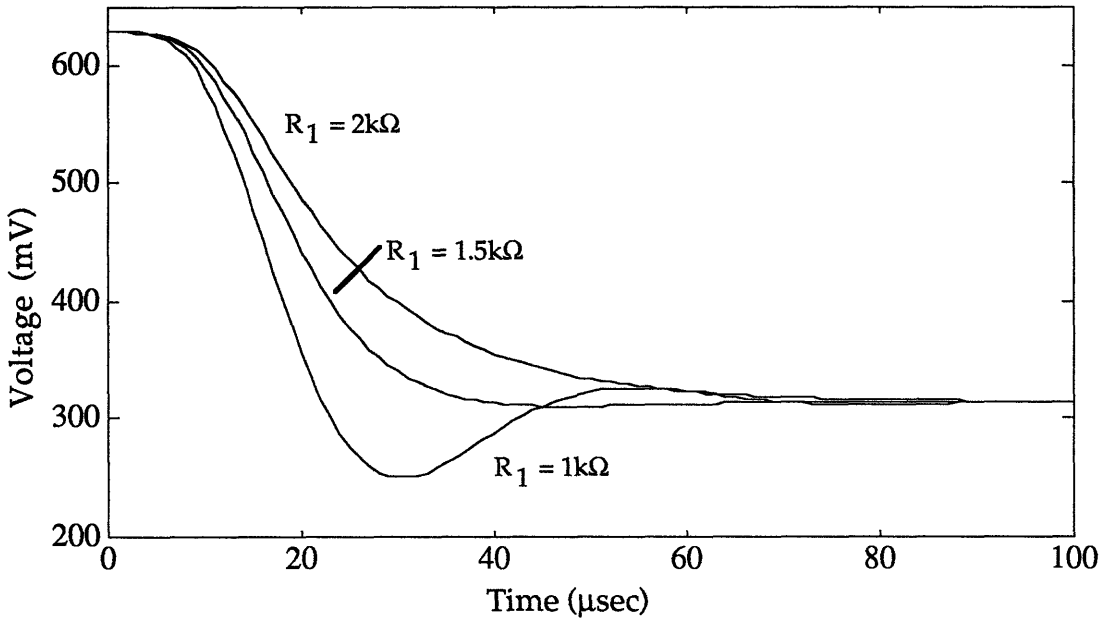

Figure 2.15: SPICE Simulation for 50kHz Bandwidth

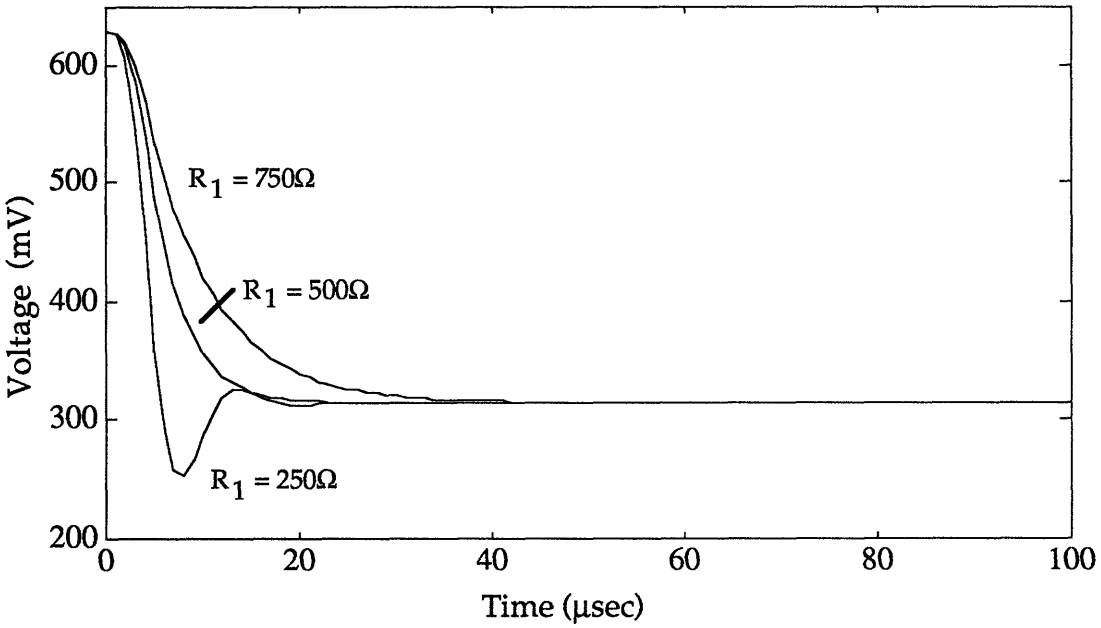

Figure 2.16: SPICE Simulation for 200kHz Bandwidth

The final value of V_{out} is 0.3142 V for both simulations. The settling time to 0.1% in the 50 kHz filter is about 70 μsec. The 200 kHz case has a settling time of 27 μsec. The results presented in Figures 2.15 and 2.16 confirm the results of the mathematical analysis shown in Figure 2.5 and 2.6.

Next, a simulation of the 200kHz bandwidth circuit with $R_1 = 500\Omega$ was performed with the parasitic bias currents and offset voltages modeled. The non-idealities of the filter and sine-wave sources were not included in the first simulation. The voltage, V_{out}, settled to a value of 0.3079V, 6.3mV less than the ideal result. The predicted result for the error is 5.2mV and was derived in Section 2.1.

When the parasitic elements inherent to the filters are included in the analysis, the output voltage settles to a value of 0.3019V. This is 6 mV less than the previous result with no non-ideal sources present in the filter. The previous assumption that the error sources in the filter contribute only a small fraction of the total offset is incorrect. However, the total 14 mV difference between the ideal output and the simulated output in the presence of parasitic sources translates to a capacitive error of only 0.22 fF; see Equation 2-18.

2.3 Summary

The circuit proposed by D. Marioli, E. Sardoni, and A. Taroni for capacitance measurement works adequately for the proposed application. The rise-time of the circuit for the case when the low-pass filter has a bandwidth of 200 kHz is about 18 μsec, sufficiently fast to track the motion of the micromotor. However, for cases when the low-pass filter has a lower bandwidth, the speed-of-response of the circuit becomes too slow for accurate position sensing. The parasitic sources inherent to the active devices in the circuit contribute a small offset at the output equivalent to a capacitance error of 0.08 fF, or about 0.8% of full scale. Additionally, there is a small scale error equal to 0.4 aF/V.

The main problem with this design is the difficulty of practical implementation. The sine-wave drive requires the presence of a function generator. The dependence of the output voltage on the value of R_2 also raises concern about the stability of large resistor values. Materials collecting on the surface, such as dust and finger grease, can significantly lower the value of large resistors. In addition, the performance of the circuit is only

adequate. With some modifications to the circuit, the output errors can be reduced, the speed of the dynamic response improved, and the implementation of the circuit greatly simplified. This modified design is discussed in Chapter 3.

Chapter 3: Modified Design

The circuit proposed by D. Marioli, E. Sardoni, and A. Taroni that was outlined in Chapter 2 adequately meets the performance specifications of the small capacitance measurement. With some modifications, however, the circuit performance is improved and the circuit implementation is simplified. Figure 3.1 shows a modified version of the capacitance measurement circuit.

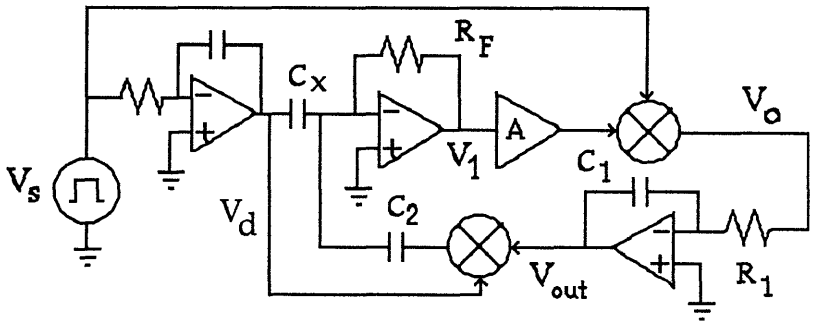

Figure 3.1: Modified Circuit Design

The circuit shown in Figure 3.1 has the same basic topology as the circuit shown in Figure 2.1 with some beneficial modifications. The input signal has been changed from a sine wave to a square wave, a signal which can be realized using far simpler circuitry than that required to produce a sine wave. With the desire for the final design to be self-contained, this is a marked improvement. The input into the summing differentiator is now a triangle wave (the integral of the square wave). The differentiator converts the triangle back into a square wave with an amplitude proportional to difference between the currents through the sensor capacitor and the reference capacitor. This waveform is then multiplied with the original square wave. Since the two inputs to the multiplier are in phase, the output is a positive dc voltage equal to the product of the amplitudes of the two inputs. Due to the constant nature of the voltage V_o, there is no longer a need for the multiple-pole low-pass filter to remove the ac components. The voltage is fed directly into the integrator, and the integrator acts as a filter to remove small variations in the value of V_o. Removing the filter from the signal path increases the bandwidth of the system, allowing a much faster

response time to changes in the input signal. Finally, the feedback reference resistor is changed to a capacitor, eliminating the need for the 90 degrees phase shift between the input signal and the feedback multiplier. This change also eliminates the concern over the susceptibility of large feedback resistor to changes in value due to dirt or dust settling on the resistor surface.

3.1 Analysis

As discussed in Chapter 2, the presence of the integrator in the feedback path drives the steady-state error voltage to zero. Therefore, from Figure 3.1, $V_dC_x = -V_{out}C_2V_d/B_1$ where B_1 is the divisor voltage inherent to the feedback multiplier. The output voltage in steady-state is

$$V_{out} = \frac{C_x}{C_2}B_1 \qquad (3\text{-}1)$$

A more detailed examination of the dynamics of the circuit begins with the block diagram shown in Figure 3.2.

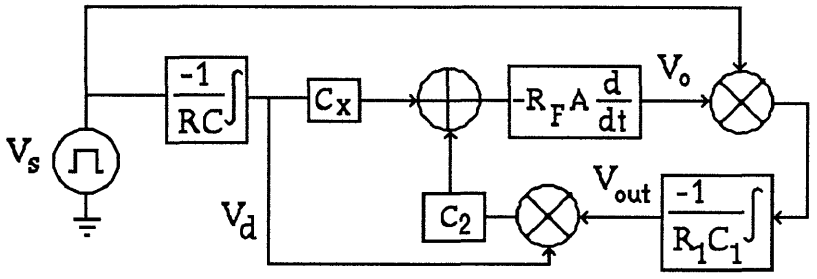

Figure 3.2: Block Diagram for the Revised Design

Beginning with Figure 3.2, it follows that

$$V_{out} = -\frac{1}{R_1C_1}\int\frac{V_oV_s}{B_F} \qquad (3\text{-}2)$$

$$V_o = -R_FA\frac{d}{dt}\left(\frac{V_{out}V_dC_2}{B_1} + V_dC_x\right) \qquad (3\text{-}3)$$

B_F is the denominator voltage in the forward multiplier. Taking the derivative of Equation 3-2 and substituting V_o from Equation 3-3 results in

$$\frac{dV_{out}}{dt} = \frac{R_F C_2 A V_s}{B_F R_1 C_1} \frac{d}{dt}\left(\frac{V_{out} V_d}{B_1} + \frac{V_d C_x}{C_2}\right) \tag{3-4}$$

Expanding the derivative on the right-hand side of Equation 3-4 results in

$$\frac{dV_{out}}{dt}\left(1 - \frac{R_F C_2 A V_s V_d}{B_1 B_F R_1 C_1}\right) + V_{out}\left(\frac{R_F C_2 A V_s}{B_1 B_F R_1 C_1}\frac{dV_d}{dt}\right) = \frac{R_F C_2 A V_s}{B_F R_1 C_1}\frac{d}{dt}\left(\frac{V_d C_x}{C_2}\right) \tag{3-5}$$

The relationship between the waveforms at V_s and V_d is shown below in Figure 3.3.

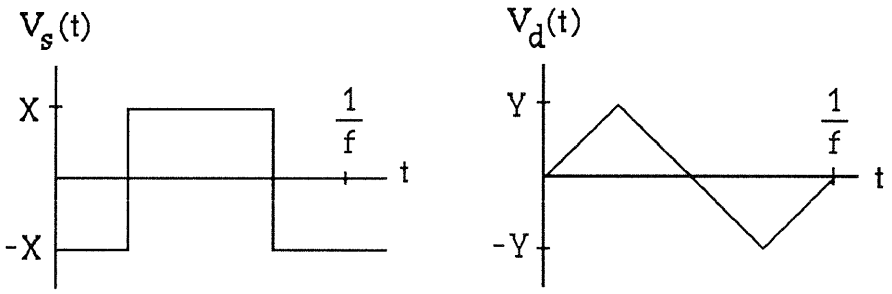

Figure 3.3: Waveforms at $V_s(t)$ and $V_d(t)$

From Figure 3.3, the product $V_s \bullet dV_d/dt$ is a constant equal to the product of the amplitude of V_s and the magnitude of the slope of V_d such that

$$V_s \frac{dV_d}{dt} = 4fXY \tag{3-6}$$

The product $V_s \bullet V_d$ is a periodic waveform shown below in Figure 3.1.3.

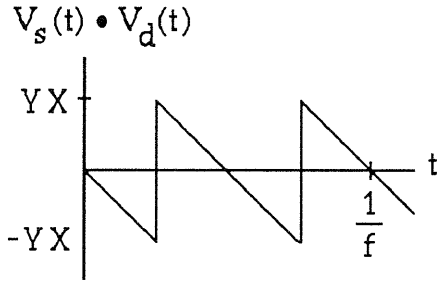

Figure 3.4: $V_s \bullet V_d$

For the interval $-1/4f < t < 1/4f$,

$$V_d V_s = -4XYft \tag{3-7}$$

Substituting Equations 3-6 and 3-7 into Equation 3-5 results in the following differential equation for the interval -1/4f < t < 1/4f:

$$\frac{dV_{out}}{dt}\left(1+\frac{R_F C_2 A4XYf}{B_1 B_F R_1 C_1}t\right)+V_{out}\left(\frac{R_F C_2 A4fXY}{B_1 B_F R_1 C_1}\right)=\frac{R_F C_2 A V_s}{B_F R_1 C_1}\frac{d}{dt}\left(\frac{V_d C_x}{C_2}\right) \tag{3-8}$$

Equation 3-8 is simplified into Equation 3-9 by applying the chain rule in reverse.

$$\frac{d}{dt}[(1+Wt)V_{out}(t)]=\frac{R_F C_2 A V_s}{B_F R_1 C_1}\frac{d}{dt}\left(\frac{V_d C_x}{C_2}\right) \qquad -1/4f < t < 1/4f \tag{3-9}$$

$$W=\frac{R_F C_2 A4fXY}{R_1 C_1 B_1 B_F} \tag{3-10}$$

Integrating both sides of Equation 3-9 from -1/4f to t results in

$$V_{out}(t)=\frac{\left(1-\frac{W}{4f}\right)}{(1+Wt)}V_{out}(-1/4f)+\frac{1}{(1+Wt)}\int_{-1/4f}^{t}\frac{R_F C_2}{R_1 C_1}\frac{AV_s}{B_F}\left[\frac{d}{dt}\left(V_d\frac{C_x}{C_2}\right)\right]dt \tag{3-11}$$

In steady-state, the value of C_x is constant so that the value of V_{out} as a function of time over the interval of -1/4f < t < 1/4f becomes

$$V_{out}(t)=\frac{\left(1-\frac{W}{4f}\right)}{(1+Wt)}V_{out}(-1/4f)-\frac{WB_1}{(1+Wt)}\frac{C_x}{C_2}(t+\frac{1}{4f}) \tag{3-12}$$

For the next-half of the period, 1/4f < t < 3/4f, the output voltage as a function of time becomes

$$V_{out}(t)=\frac{\left(1-\frac{W}{4f}\right)}{\left(1+W\left(t-\frac{1}{2f}\right)\right)}V_{out}(1/4f)-\frac{WB_1}{\left(1+W\left(t-\frac{1}{2f}\right)\right)}\frac{C_x}{C_2}\left(\left(t-\frac{1}{2f}\right)+\frac{1}{4f}\right) \tag{3-13}$$

The response is the same for both halves of the period of $V_s(t)$. In the steady state, the value of $V_{out}(t)$ at the end of each period (t+n3/4f) must be the same.

Therefore, the value of V_{out} must be constant over the entire interval ($-1/4f < t < 3/4f$). Substituting $t=1/4f$ into Equation 3-12 results in

$$V_{out}\left(\frac{1}{4f}\right) - V_{out}\left(\frac{-1}{4f}\right) + \left[V_{out}\left(\frac{1}{4f}\right) + V_{out}\left(\frac{-1}{4f}\right)\right]\frac{W}{4f} = -\frac{B_1 C_x}{C_2}\frac{2W}{4f} \qquad (3\text{-}14)$$

Since $V_{out}(1/4f) = V_{out}(-1/4f)$, the steady-state value of V_{out} is

$$V_{out} = -\frac{B_1 C_x}{C_2} \qquad (3\text{-}15)$$

Equation 3-14 is the same result as was derived by setting the steady-state error to zero.

Next, the dynamics of V_{out} due to a step change in the sensor capacitance, C_x, from 10 fF to 5 fF is accomplished by evaluating Equation 3-12 numerically in MATLAB. The procedure begins by setting the initial condition, $V_{out}(-1/4f)$, to the appropriate value when C_x = 10 fF. From Equation 3-15, $V_{out}(C_x = 10\text{ fF}) = -5$ V when $B_1 = 10$ V and $C_2 = 20$ fF. Next, the value of C_x in Equation 3-12 is set to 5 fF. Table 3-1 lists the values of the circuit parameters and Figure 3.5 shows a graph of step responses for various levels of loop gain.

Table 3-1: Circuit Parameters

Element	Value	Comments
C_2	20fF	Reference Capacitance
R_F	16MΩ	Differentiator Resistor
f	1MHz	Drive Frequency
X	2V	Amplitude of V_s
Y	2V	Amplitude of V_d
A	1	Gain Stage Value
B_1	10V	Feedback Multiplier Devisor Voltage
B_F	1V	Forward Multiplier Devisor Voltage
C_1	1nF	Integrator Capacitor
R_1	100Ω	Integrator Resistor
	1000Ω	Varied to change the loop gain
	5000Ω	

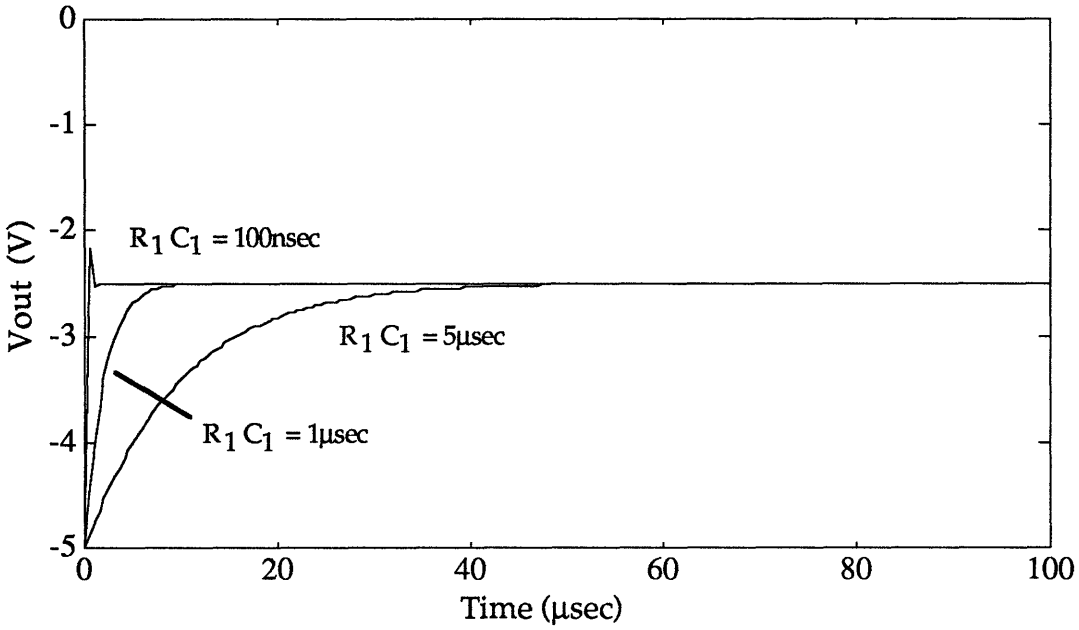

Figure 3.5: Response of V_{out} due to a Step Change in C_x

As shown in Figure 3.5, the step response of the circuit for small values of the loop-gain, integrator time constants of 5μsec and 1μsec, is that of an overdamped system. The speed of response becomes faster as the loop gain increases. For very high gains, the system becomes underdamped as shown by the presence of a small overshoot in the step response of the 100nsec example. Each of the three step-transients shown in Figure 3.5 settle to a final value of -2.500V. The predicted value of the output voltage for C_x = 5 fF is calculated using Equation 3-15 is -2.500 V.

The rise-time of the R_1C_1 = 1 μsec transient response shown in Figure 3.5 is about 8 μsec. This is significantly faster than rise-time of the transient responses for the circuit examined in Chapter 2 where the best rise-time is about 20 μsec for the case when the low-pass filter bandwidth is 200 kHz.

Next, the influence of the parasitic elements is examined. Figure 3.6 shows the circuit of Figure 3.1 with the offset voltages and bias currents present.

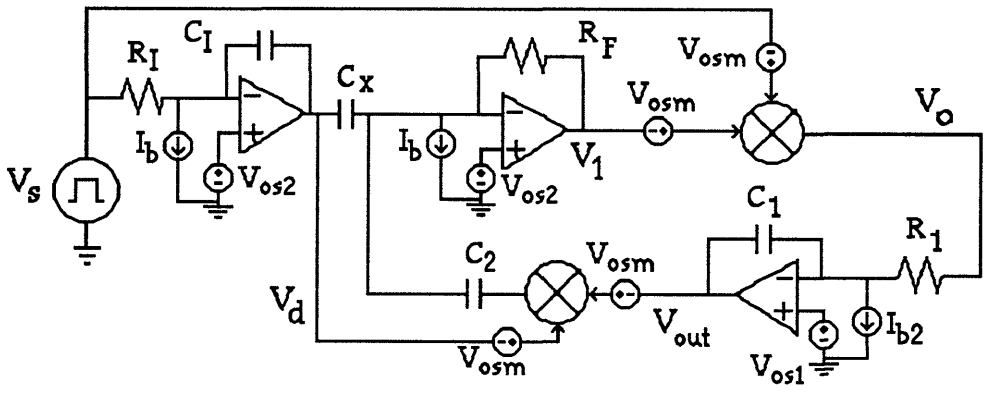

Figure 3.6: Modified Circuit Design with Parasitic Elements

The parasitic sources shown in Figure 3.6 are arranged with a polarity such that the total error is worst-case (constructive superposition of errors). The input integrator op-amp is chosen to be the AD843K because of its large bandwidth and good precision. The other active devices are the same as were chosen for the initial design presented in Chapter 2. Table 2-2 summarizes the values of the parasitic elements shown in Figure 3.6.

The bias current present in the triangle-wave integrator has serious consequences on its performance. Since the left side of resistor R_I is held at V_s, the bias current is forced through the capacitor, C_I. The voltage, V_d, increases as a function of time: $V_d = I_b t/C$. The output of the amplifier eventually saturates, terminating any useful operation of the integrator. The solution to this problem is relatively simple. A resistor, R_N, is placed in parallel with C_I to give the bias current a low-impedance outlet. The transfer function of the modified integrator is

$$H(s) = -\frac{R_N}{R_I}\frac{1}{R_N C_I s + 1} \tag{3-16}$$

At the frequencies of interest, f > 1 MHz, H(s) must approximate the original integration given by

$$H(s) = -\frac{1}{R_I C_I s} \tag{3-17}$$

The values of R_I and C_I are chosen to set the peak-peak value for the triangular waveform. As discussed in Chapter 1, the maximum value for the amplitude of the input drive is 2 V. For a 1 MHz square wave with an

amplitude of 2 V, the output has a peak-to-peak value is 2 V(.5 μsec)/R_IC_I. Setting this equal to 4 V requires $R_IC_I = 2.5x10^{-7}$sec. For C_I = 1 nF, the value of R_I is 250 Ω .

For Equation 3-16 to approximate Equation 3-17, $R_NC_Is >> 1$. For frequencies larger than 1 MHz, $s > 2\pi$(1 MHz), $R_N >> 1.59x10^{-7}/C_I$. Therefore, $R_N >>$ 159 Ω. It is also desirable not to make R_N too large because the offset voltage at V_d is equal to $I_b \bullet R_N + V_{os2}$. To make the offset due to the bias current about one-tenth that of the input offset voltage means that R_N must be less than $0.1V_{os2}/I_b$. For a 1nA bias current and a 1 mV offset voltage, $R_N <$ 100 kΩ. Setting the value of R_N to 100 kΩ keeps the offset voltage low and makes the circuit behave like an integrator at the frequencies of interest.

The first step required to ascertain the effect of the parasitic sources on the output voltage, V_{out}, is to translate all the offsets to V_o. The dc voltage at the output of the feedback multiplier is $(1.1V_{os2} + V_{osm}) \bullet (V_{out}+V_{osm})$. However, now that the feedback element has been changed to a capacitor, this voltage is blocked, resulting in no dc input current from the feedback multiplier into the summing node of the differentiator. The offset voltage at V_1 is now equal to 1 nA•16 MΩ + 1 mV = 17 mV. Adding this value to the input offset voltage of the multiplier totals 22mV. Multiplying this by the input square wave plus 5mV offset voltage results in an output at V_o of 100 μV dc plus a 44 mV amplitude square wave. The feedback integrator adds an additional 25 μV to the dc value at V_o. The bias current adds 2 nA•R_1 to the error at V_o. For values of $R_1 <$ 1 kΩ, this error is small compared to the other offsets and is ignored. The total error at V_o is the sum of a 125 μV dc voltage and a 44mV amplitude square-wave.

Since the total dc value at V_o must be zero, a constant voltage equal and opposite to the offset must be superimposed at V_o to compensate for the non-idealities. As discussed in Section 2.1, the dc value at V_o projects to an offset voltage at V_{out}. To cancel a constant value at V_o of 125 μV, a square-wave at V_1 of $V_{odc}B_F/V$, where V is the amplitude of the input square wave, must be present. For V=2 V and B_F equal to 1 V, the amplitude of the square wave at V_1 is 63 μV. The current through R_2 needs to be a 3.9pA square wave. To translate this to an offset voltage at V_{out}, a relationship between V_{out} and I_{R2} is needed. I_{R2} = 3.9 pA = C_2 dV/dt, where V is the output voltage of the feedback multiplier. With $V = V_{out} \bullet V_d$, dV/dt = V_{out}•4 V/.5 μsec = $V_{out} \bullet 8x10^6$ V/sec. Therefore, V_{out} = 3.9 pA/($C_2 \bullet 8x10^6$ V/sec) = 25 μV for C_2 =

20fF. The total dc offset at V_{out} is the sum of 25 μV and the input offset voltage of the feedback multiplier, V_{osm}. Since V_{osm} = 5 mV, it completely dominates the error.

The 25 μV error is lower in this circuit than the 130μV calculated for the error in Chapter 2. This is true for a couple of reasons. First, the global feedback element has been changed to a capacitor, thereby blocking the dc error at the output of the feedback multiplier. This modification also makes the offset error at V_{out} independent of the value of V_{out}. Second, the sine-wave drive, when squared has an average value of 1/2 where a square wave squared has an average value of 1. This fact means that for the same dc value at V_o, the offset voltage at V_{out} needs to be only half as big in the square wave case to negate the error.

A 5 mV offset at the output is translated to a capacitance error of

$$\Delta C = \frac{5mV}{B_1} C_2 \tag{3-18}$$

For B_1 = 10 V and C_2 = 20 fF, the capacitance error is equal to 0.01 fF, or 0.1% of full-scale of 10 fF. The error is quite small and not of serious consequence.

The other part of the error at V_o is a 44 mV amplitude square wave. This signal creates a ripple voltage at the output. This ripple is a triangle wave (to first order) with a slope of $dV/dt = 44\ mV/(R_1C_1) = 4.4x10^6 V/sec$ for R_1C_1 = 100 nsec. Over one-half period, 0.5 μsec, the peak-peak ripple is 0.22 V. This value is unacceptably large. It can be reduced by lowering the gain of the feedback integrator or increasing the denominator voltage of the analog multiplier, B_F. For the case when R_1C_1 = 1 μsec, the ripple voltage is 1/10 of the previous case or 22 mV. However, reducing the voltage ripple at V_{out} also hurts the dynamic response of the system. Another possible method of removing the ripple is to filter the output voltage, V_{out}. A low-pass filter with a wide-enough bandwidth such that the dynamics of the system is not compromised reduces this error.

Other sources of possible error include phase differences between the input square wave and the triangle wave, non-zero rise times in the square wave, and offset voltages in the square waves. The first error will likely be small because the triangle wave is derived directly through from the input square wave and only a small propagation delay is present. The quality of the square wave is a controllable factor and the technology exists for a reasonably

good waveform. An offset in the square wave adds directly to the input offset voltage of each of the multipliers. Such an error increases the offset voltage at V_{out} and is calculated in the same manner as was previously done.. With the ability to control the square wave, this additional source of error is mitigated by making the duty cycle 50% and then ac coupling the waveform with a large capacitor.

3.2 Computer Simulation:

The modified circuit design, pictured in Figure 3.1, is next simulated using SPICE. The values of the circuit parameters are given in Table 3-1. The integrator time constant, R_1C_1, is once again used to vary the loop gain. Figure 3.7 shows a combined graph of the SPICE outputs for step changes in C_x from 10 fF to 5 fF at three different values for the loop gain.

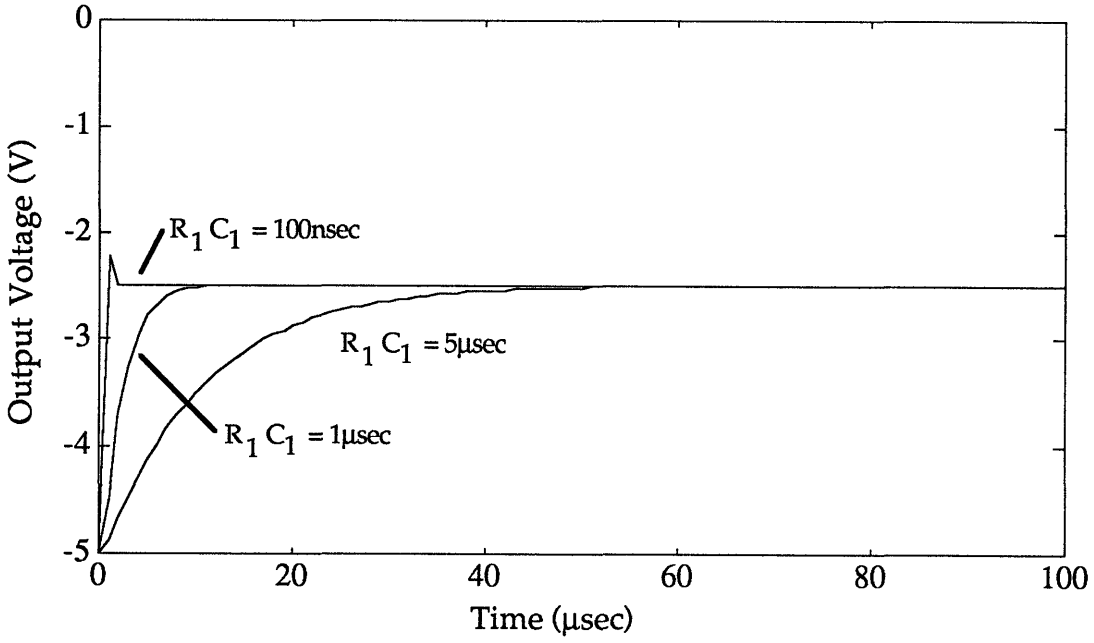

Figure 3.7: SPICE Output Response for Step Change in C_x

The three step responses graphed in Figure 3.7 appear identical to the results of the mathematical analysis shown in Figure 3.5.

A second simulation to determine the effects of parasitic sources is performed. In order to examine the characteristics of the voltage ripple, the simulation is run with a much smaller timestep. Figure 3.8 shows the results

of a steady-state simulation of the modified circuit design. The R_1C_1 time constant is 1μsec and the time step is 0.01 μsec.

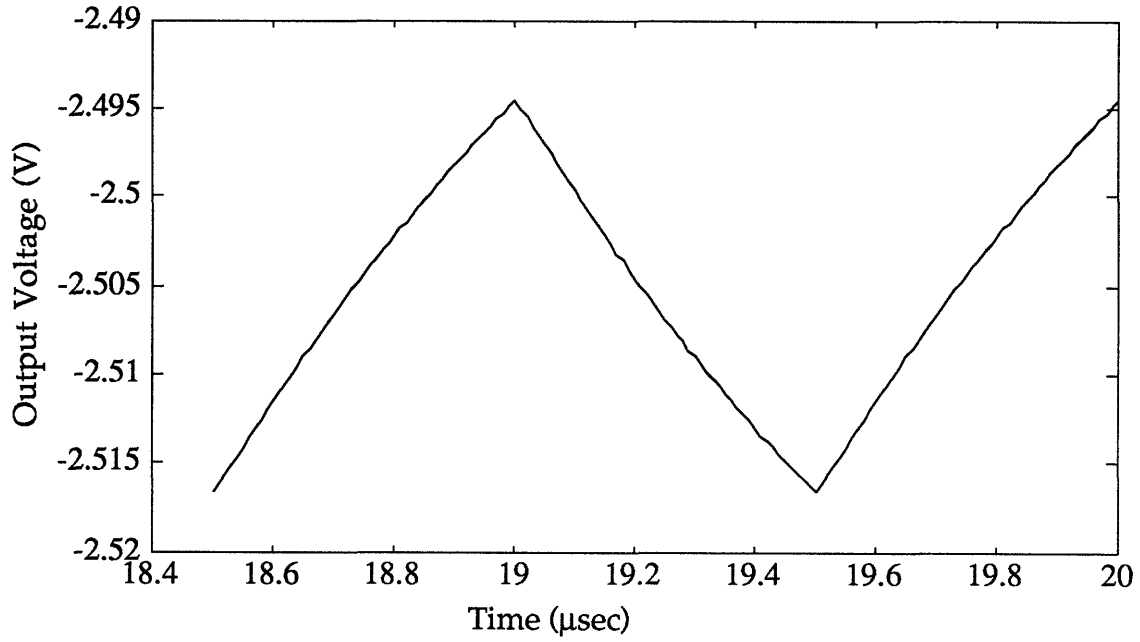

Figure 3.8: Effect of Parasitic Sources on the Steady-State Output Voltage

The output waveform shown in Figure 3.8 shows a voltage ripple with a peak-peak value of 22mV and an average value of -2.5056V. The error analysis performed in Section 3.2 predicted an offset voltage of 5mV and a peak-peak voltage ripple of 22 mV. The offset voltage of the computer-simulation is -2.5056 V+2.5000 V = 5.6 mV. This is extremely close to the value calculated through the analysis. The ripple voltage of the simulation also matches the predicted value of 22 mV. However, the shape of the output is not quite triangular. The reason for this originates with the first-order approximation that the voltage at V_o remains constant during each half-cycle of V_s. This assumption requires the voltage ripple to be triangular. Ignored was the fact that a changing voltage at V_{out} influences the value at V_o. A single half-cycle of the square-wave at V_o appears as a dc offset. If this offset is allowed to persist indefinitely, the output voltage, V_{out}, approaches a new final value which compensates for this offset by driving the value of V_o to zero; this is the same mechanism that corrects the dc offset at V_o. For slow loop-gains, the 0.5 μsec duration of the square-wave offset is short enough to

prevent the output voltage from approaching its new final value. Therefore, the voltage at V_o remains fairly constant and the ripple looks triangular. However, for larger loop-gains, the voltage at V_{out} approaches its final value much faster. The quick increase in V_{out} causes the value of V_o to decrease which in turn slows down the rate at which V_{out} increases. In short, each edge of the square wave at V_o causes the system to have the same dynamic response at V_{out} as a step change in C_x. The result is an exponential ripple. For even higher values of loop-gain, the voltage at V_{out} may actually reach its final value before the next edge of V_s, resulting in a square-wave ripple. Thus, the relatively fast loop gain of the example graphed in Figure 3.8 causes the ripple voltage to appear exponential. For comparison, an example of the voltage ripple for a larger loop-gain (R_1C_1 = 100 μsec) is shown in Figure 3.9.

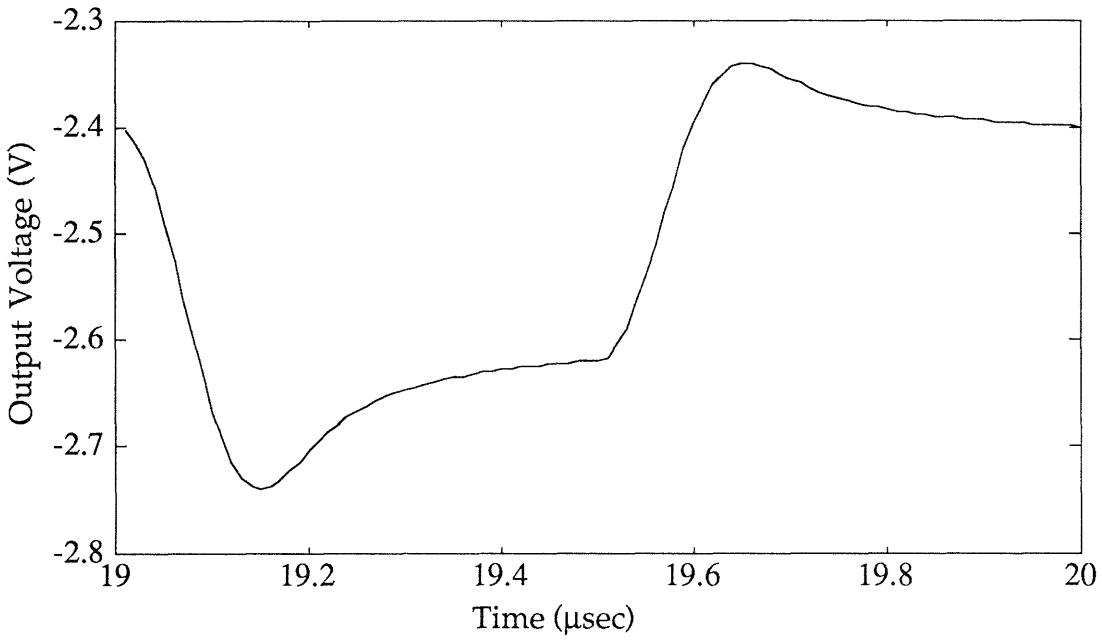

Figure 3.9: Ripple Voltage at High Loop Gain

The ripple voltage shown in Figure 3.9 shows an underdamped squarewave which comes close to reaching a steady-state. The larger loop-gain of this example allows V_{out} to adjust fast enough to correct for the presence of an instantaneous dc offset at V_o. The underdamped behavior is consistent with the dynamic result of the 100 nsec case shown in Figure 3.7.

The computer simulation of the circuit is consistent with the theory and predictions of the numerical analysis presented in Section 3.2.

3.3 Experimental Results:

To test the feasibility of implementing the modified design, the circuit shown in Figure 3.10 was constructed on a perfboard. A macroscopic scale model of the micromotor was built for testing purposes. The variable capacitance for this model is on the order of 1 pF. The reference capacitor constructed for use with the model has a value of 6.7 pF. The practical differentiator discussed in Section 2.1 is used in the design. The values of the added components are chosen such that the closed-loop differentiator has a unity-gain frequency of 1MHz and a double-pole rolloff at 10 MHz.

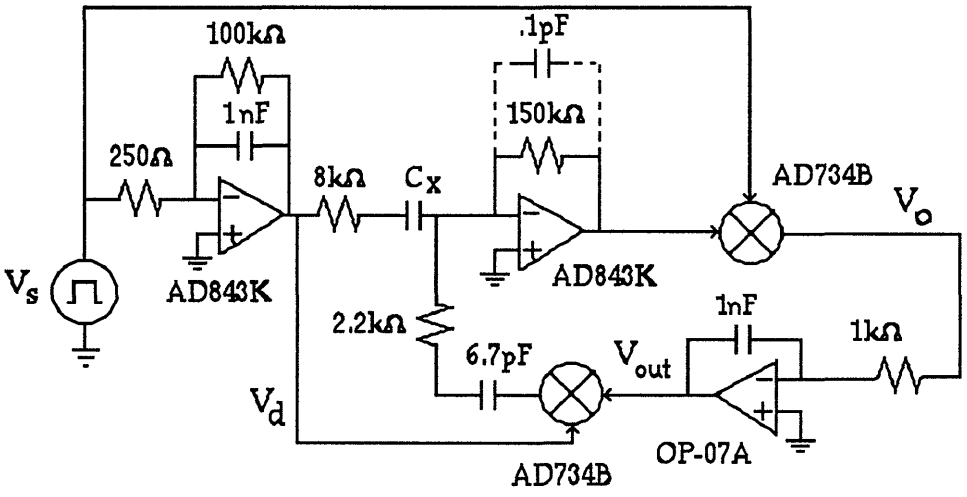

Figure 3.10: Implemented Circuit Schematic

The differentiator feedback capacitor is not an actual component because discreet capacitors do not exist in sizes that small. Additionally, it is likely that sufficient parasitic capacitance exists between those two nodes to produce the desired result and so is shown as a dashed connection in Figure 3.10. The forward multiplier has a denominator value of 1 V and the feedback multiplier has a denominator value of 10 V. The details of the analog multiplier connections have been omitted.

For the main test, the circuit is connected to the micromotor model, the rotor is spun, and the output voltage, V_{out}, is monitored on an oscilloscope. For square-wave frequencies less than 200 kHz, the circuit

performs as expected with the resistor and capacitor values of the triangle-wave integrator adjusted to maintain a 4 Vp-p triangle. The output voltage, V_{out}, is lowest (most negative) when the rotor blades are directly over the probes and highest (least negative) when the blades and probes are not coincident. When the motor is spun, a sinusoidal output voltage is observed. A closer look at V_{out} also reveals a ripple voltage on the same order as the predicted value calculated in Section 3.2.

When the frequency of the square wave is increased beyond 200 kHz, the circuit no longer functions as designed. An examination of the voltage at V_1 with the feedback loop disconnected reveals that the waveform is no longer square. As the source drive, V_s, increases, V_1 changes from a square wave to a negative triangle wave. Further increases in frequency create some peaking and then a smoother wave which decreases in amplitude. This order of events suggests the presence of parasitic inductance and a pole at a lower frequency than 10 MHz.

One possible explanation for the change in waveform of V_1 from a square wave to an inverted triangle wave is the presence of a closed-loop pole at a frequency less than 1 MHz. The practical differentiator is designed with a compensating network to improve stability and reduce high-frequency noise; see Section 2.1. For the roll-off pole of this compensator to be at 10 MHz, the feedback capacitance around the differentiator needs to be 0.1 pF. However, if sufficient parasitic capacitance exists between the input and output terminals, then this pole is shifted to a lower frequency. One possible source of such capacitance is within the large feedback resistor, R_F.

The observed peaking of the voltage at V_1 is likely caused by the presence of parasitic inductance. The wires used to connect components of the circuit have an inductance of about 1 nH per inch. Additionally, the use of copper tape in the construction of the micromotor may have added additional inductance which is responsible for the brief resonant peak.

Regardless of the problems present in the scale model, the practical implementation of the differentiator for real micromotors is unachievable. The feedback resistor required for unity gain at 1 MHz was derived in Section 3.2 as 16 MΩ. To place the closed-loop roll-off pole of the differentiator at 10MHz, the feedback capacitance must be 1 fF. The parasitic capacitance of the resistor is likely equal to a hundred times this value. The effect of this parasitic element is to move one of the closed-loop poles to a lower frequency

and possibly even lower than the frequency of the square wave. In this case, the circuit no longer behaves like a differentiator at 1 MHz. Instead, the circuit behaves like a gain element and the differentiator output is a negative triangle. The circuit no longer functions properly.

One possible correction for this error is to place a known capacitor in the feedback of the differentiator and replace the triangle wave drive with a square wave. This changes the function of the minor-loop op-amp circuit from a differentiator to a simple gain. The large feedback resistor is maintained to give the bias current of the operational amplifier an outlet. The output at V_1 is once again a square wave error voltage and the circuit functions as before. However, to avoid attenuating the error signal into the noise level, the feedback capacitor needs to be on the order of the sensor capacitor. No reliable discreet components are even within two orders of magnitude of C_x. Therefore, the practicality of this approach is questionable.

3.4 Summary

The analysis of the modified circuit design shows an improvement in performance over the original design proposed by D. Marioli, E. Sardoni, and A. Taroni. The speed of response has improved by more than a factor of two over the initial circuit, giving a rise time of less than 8 μsec. The offset voltage present at the output has been reduced to an equivalent capacitance error of only 0.01 fF or about 0.1% of full scale. The scale error has been removed completely. However, the elimination of the low-pass filter from the design now permits a ripple voltage to exist at the output. The magnitude of this voltage increases with increasing gain. For the case with the 8 μsec rise-time, the ripple is about 22mV or 0.22% of full scale.

The modified design greatly simplify the implementation. However, the practical issues of realizing the differentiator for use in measuring the position of a real micromotor suggests that additional modifications are still necessary.

Chapter 4: Final Design

The modified circuit examined in Chapter 3 is an improvement over the original circuit in both performance and simplicity of implementation. However, the frequency requirements necessary for accurate tracking of the micromotor make the implementation of the practical differentiator unachievable. This shortcoming is alleviated with the final circuit, shown below in Figure 4.1. This design replaces the differentiator with a follower, simplifying the layout and improving the performance.

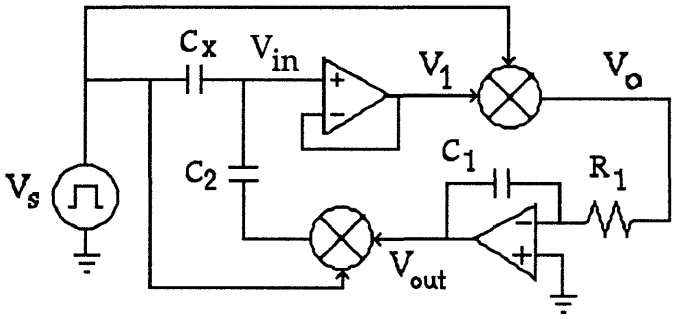

Figure 4.1: Final Circuit Design

As discussed in Chapter 1, the closed-loop amplifier is the desired choice for capacitance measurement because the virtual ground node suppresses the large parasitic capacitance present in the micromotor. The unity-gain buffer in this circuit does not provide a virtual ground node at V_{in}. However, the presence of the integrator in the global feedback forces the steady-state voltage at V_{in} to zero. Therefore, in a quiescent state, the parasitic capacitance has no effect on the output voltage V_{out}. Dynamically the parasitic capacitance from C_x to ground is very influential. It acts as an attenuator for the error signal by diverting charge away from the reference and sensor capacitors. The presence of the parasitic capacitor therefore reduces the loop-gain of the system. This problem is easily compensated by increasing the gain in other elements of the feedback loop, primarily the integrator.

The second major modification in the final design is the change in drive signal into the reference and sensor capacitors. Previously, these capacitors were driven by a triangle wave. The currents through the sensor and reference capacitors, which are proportional to the integral of the voltage

drive, were added at the negative terminal of the differentiator op-amp, which is driven to virtual ground by the negative feedback around the op-amp, and then converted to the error voltage, V_1, by a large feedback resistor. The desire for the error voltage to be a square wave, which is multiplied by another square wave to give a constant, required the drive to be triangular. In the steady-state, the current into the sensor capacitor is forced by the feedback integrator to match the current out of the reference capacitor, resulting in zero error voltage. In the final design, the current into the sensor capacitor is always equal to the current out of the reference capacitor. The voltage at the summing node, the positive input terminal of the follower op-amp, V_{in} , is now equal to the superposition of two capacitive voltage dividers. With the operational amplifier connected in a follower configuration, the error voltage, V_1, it is equal to V_{in}. Therefore, driving C_x and C_2 directly with a square wave results in an the error voltage that is also a square. In the steady-state, the feedback integrator forces the voltage at V_{out} to a value such that the voltage at V_{in} goes to zero.

4.1 Analysis

The presence of the parasitic capacitance, C_{IS}, is important to the dynamic analysis of this circuit. Figure 4.2 repeats the circuit shown in Figure 4.1 with C_{IS} included.

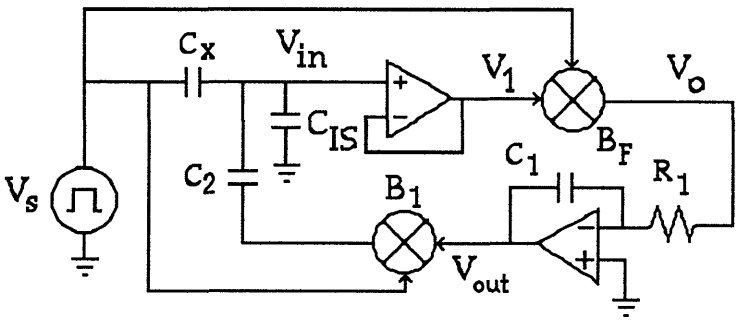

Figure 4.2: Final Circuit Design with C_{IS}

The circuit operation of the final circuit shown in Figure 4.2 is similar to the previous designs discussed in Chapters 2 and 3. This time, capacitors C_x and C_2 form a voltage divider. The value of V_{in} is determined by the superposition of V_s and $V_{out} \bullet V_s / B_1$, each multiplied by the appropriate

capacitive divider relationship. The square-wave error voltage, V_1, is equal to the value at V_{in} and is multiplied by the input square wave, V_s, to form a dc input voltage to the integrator. Any voltage at V_o charges capacitor C_1 until the voltage at V_{out} is adjusted such that the error voltage at V_1 is zero.

The numerical analysis begins with a current summation at V_{in} which yields

$$(V_s - V_{in})C_x s = (V_{in} - \frac{V_{out}V_s}{B_F})C_2 s + V_{in}C_{is}s \tag{4-1}$$

Solving for V_{in} gives

$$V_{in} = \frac{V_s}{C_x + C_2 + C_{is}}(\frac{V_{out}}{B_F}C_2 + C_x) \tag{4-2}$$

V_o and V_{out} are related through the integrator equation according to

$$V_o = -R_1C_1\frac{dV_{out}}{dt} \tag{4-3}$$

V_o and V_{in} are related through the analog multiplier and input buffer according to

$$V_o = \frac{V_sV_{in}}{B_1} \tag{4-4}$$

Combining Equations 4-2, 4-3, and 4-4 results in

$$\frac{dV_{out}}{dt} + \frac{C_2V_s^2}{R_1C_1(C_2 + C_x + C_{is})B_1B_F}V_{out} = -\frac{1}{R_1C_1B_1}\frac{V_s^2C_x}{(C_2 + C_x + C_{is})} \tag{4-5}$$

The steady-state value for V_{out} is determined by solving Equation 4-5 for V_{out} with dV_{out}/dt set to zero. This yields

$$V_{out} = -B_1\frac{C_x}{C_2} \tag{4-6}$$

Equation 4-6 is exactly the same result as derived for the circuit examined in Chapter 3; see Equation 3-1. Since the fundamental operation of the circuit has not been changed by the modifications, this result is not a surprise.

Next, the dynamic response to a step change in capacitance is determined. Equation 4-5 is a linear constant-coefficient first-order differential equation for a fixed value of C_x. A step change in the drive term results in an exponential transient to the new steady-state output value. Equation 4-7 shows the exponential output behavior to the first-order differential equation $dV_{out}/dt + V_{out}/\tau = V_{x\infty}/\tau$. The form of the equation is zero-input response plus zero-state response, namely

$$V_{out} = \left[V_{xo}e^{-t/\tau} + V_{x\infty}(1-e^{-t/\tau})\right] \tag{4-7}$$

where V_{xo} is the initial condition of the output voltage, $V_{x\infty}$ is the final value of V_{out}, and τ is the time constant of the exponential. Using Equation 4-6, the constants are $V_{xo} = B_1C_{xo}/C_2$ and $V_{x\infty}=B_1C_{x1}/C_2$ where C_{xo} is the initial value of the sensor capacitor and C_{x1} is the final value. Therefore, Equation 4-7 becomes

$$V_{out} = -\frac{B_1}{C_2}\left[C_{xo}e^{-t/\tau} + C_{xn}(1-e^{-t/\tau})\right] \tag{4-8}$$

The time constant, τ, is found directly from Equation 4-5 and is expressed as

$$\tau = \frac{C_2 + C_x + C_{is}}{C_2}\frac{B_1B_F}{V_s^2}R_1C_1 \tag{4-9}$$

The values of the circuit parameters are the same as those used in the modified design of Chapter 3. The values are repeated here in Table 4-1.

Once again, MATLAB is used to determine the step response of the sensor capacitor from 10fF to 5fF. Equation 4-8 was evaluated for several values of the loop gain. The R_1C_1 product was again used to vary the gain. Figure 4.3 shows the response with the parasitic capacitor, C_{is}, set to zero. Figure 4.4 graphs the step response with the parasitic capacitor included.

Table 4-1: Circuit Parameters

Component	Value	Comments
C_2	20fF	Feedback Capacitor
C_{is}	6.7pF	Implant-Substrate Parasitic Capacitance: From Table 1-1
C_x	10fF 5fF	Step Change from 10fF to 5fF
B_1	10V	Denominator Voltage of the Analog Multipliers.
B_F	1V	Set to 10 for the feedback multiplier and 1 for forward multiplier
V_s	2V	Amplitude of the input square wave
R_1	5kΩ, 1kΩ, 100Ω 10Ω, 1Ω	Integrator feedback resistor R_1C_1 time constant is used to vary the gain of the system
C_1	1nF	Integrator capacitor

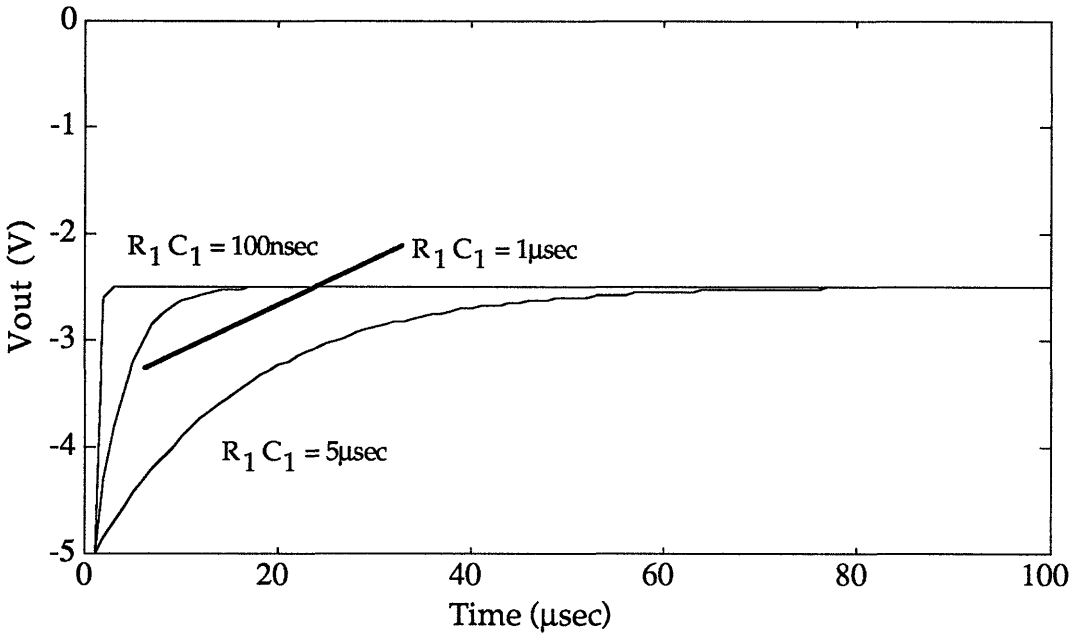

Figure 4.3: Step Response of Final Circuit without Parasitic Capacitance

The dynamic response of the final circuit design is also very similar to that of the modified design presented in Chapter 3; see Figure 3.5.

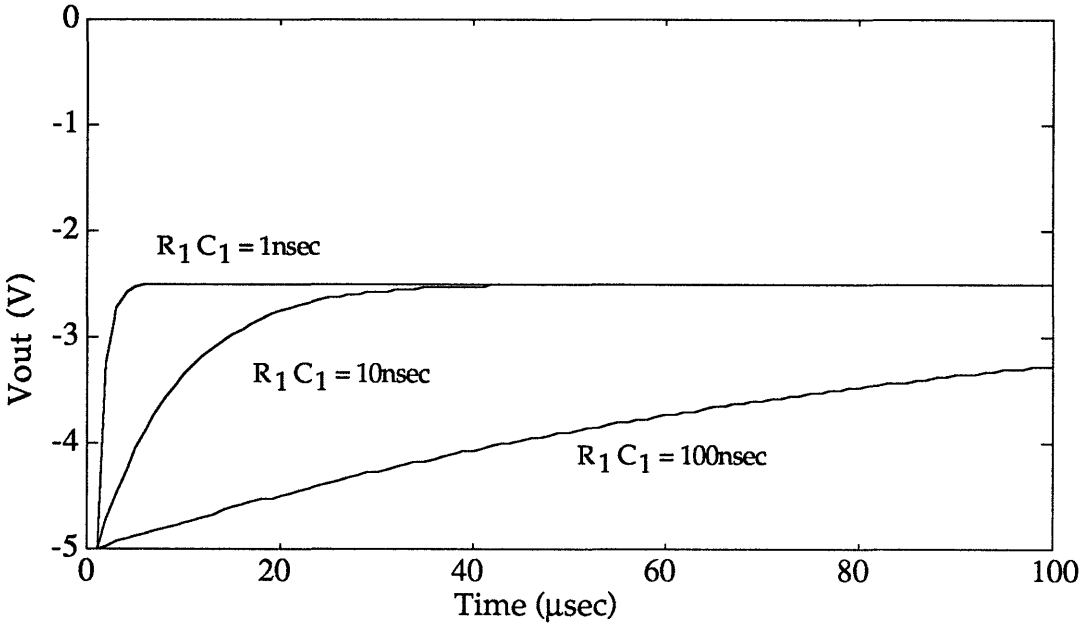

Figure 4.4: Step Response of Final Circuit with 6.7pF Parasitic Capacitance

From Figures 4.3 and 4.4, the response time of the output voltage to a step change in sensor capacitance is more than 100 times slower when C_{IS} is included in the analysis than when it is ignored. This is not a surprise because the voltage divider formed by the parasitic capacitor and the sensor/reference capacitors reduces the loop gain by slightly more than a factor of 100 as seen in Equation 4-2. The effect is compensated by increasing the gain of the integrator (reducing the value of R_1C_1) as shown in Figure 4.4.

The rise-time of the transient response for both the ideal circuit and the circuit with C_{IS} can be made very fast by increasing the loop gain. None of the transients graphed in Figure 4.3 and 4.4 become underdamped. However, non-idealities within the active components eventually limit the response-time.

The next consideration is to examine the effects of parasitic sources on the performance of the circuit. The circuit as drawn in Figure 4.1 has a very high impedance node at V_{in}, the positive input terminal to the follower amplifier. Even the smallest of input bias current present at that node causes the voltage at V_{in} to ramp off until the operational amplifier saturates. To alleviate this predicament, a large resistor is placed between the V_{in} node and ground. The size of the resistor is determined by the relative impedance of

the parasitic capacitor and the size of the bias current. To keep the offset voltage created by the bias current ($I_b \bullet R_b$) on the same order of magnitude as the input offset voltage of the amplifier (V_{os}), the resistor, R_b, should be less than V_{os}/I_b. The amplifier chosen for the follower is the AD843K because of its good frequency response and low bias current. It has an offset voltage of 1mV and a bias current of 1nA (Table 4-2). Therefore, $R_b < 1$ MΩ.

To avoid further degradation in the dynamic response of the circuit, the impedance of R_b must be large compared with the impedance of C_{IS}. Therefore, $R_b > 10 \bullet (C_{IS} \bullet \omega)^{-1}$. From Table 4-1, $C_{IS} = 6.7$ pF. The primary frequency component of the square wave is at 2π(1 MHz). Thus, $R_b > 238$ kΩ. The value of R_b is chosen to be 1 MΩ.

A more detailed analysis of the contributions of the parasitic elements begins with a look at the complete circuit. Figure 4.5 is a diagram of the circuit shown in Figure 4.2 with R_b and the parasitic sources included.

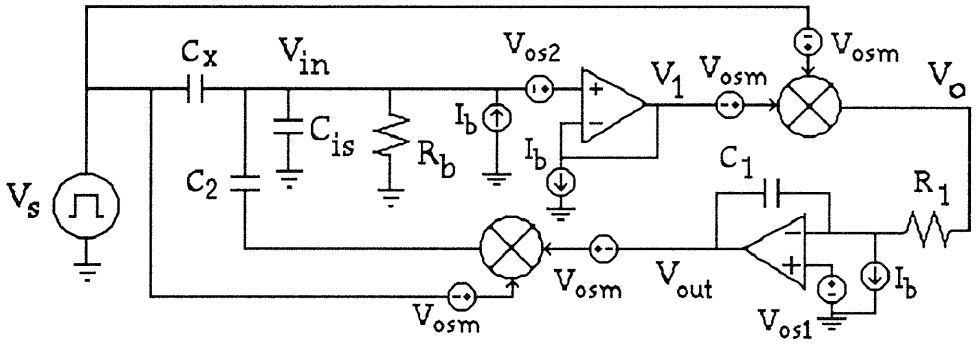

Figure 4.5: Final Design with Parasitic Elements and R_b

The polarity of the parasitic sources shown in Figure 4.5 are labeled such that their contributions to the offset at V_{out} are constructive (worst-case scenario). The active devices in the circuit are the same as were used in the previous designs examined in Chapters 2 and 3. The analog multipliers are AD734B. The follower op-amp is an AD843K and the integrator op-amp is an OP-07A. Table 4-2 repeats the characteristics of the aforementioned devices.

Table 4-2: Device Characteristics

Device	GB Product	Offset Voltage	Bias Current
AD843K	34MHz	1.0mV	1.0nA
OP-07A	.4MHz	25μV	2.0nA
AD734B	40MHz 3dB Input 10MHz 3dB Output	5mV	150nA

The total offset voltage at the positive terminal of the follower amplifier, V_{in}, is $V_{os2} + I_b \bullet R_b = 2$ mV. The bias current present at the negative terminal of the AD843K has no effect on the circuit because it can easily be supplied by the output of the amplifier. The total offset voltage present at the input to the multiplier is 7 mV. The contribution of the offset at V_o from the multiplier is 7 mV$\bullet V_s$ + 35 μV. The offset voltage, V_{os1}, and the bias current, I_b, add an additional constant voltage to V_o of 25 μV. The total voltage at V_o due to parasitic sources is 60 μV + 7 mV$\bullet V_s$. Since the dc value at V_o must be zero, the constant 60 μV must be nulled via the superposition of another dc voltage with equal magnitude and opposite sign. As discussed in Section 2.1, the source of this opposite dc voltage is an offset at V_{out}.

The signal at V_1 required to maintain a constant 60 μV at V_o is a square wave with an amplitude of 60 μV/V_s = 30 μV for V_s = 2 V. The relationship between the voltage at $V_1 = V_{in}$ and the drive voltages is given by Equation 4-2, repeated here as

$$V_{in} = \frac{V_s}{C_x + C_2 + C_{is}} \left(\frac{V_{out}}{B} C_2 + C_x \right) \tag{4-10}$$

Since the voltage source, V_s, is a constant, the variation in V_{in} must be supplied by a variation in the output voltage, V_{out}. The relationship between V_{in} and V_{out} for variations away from their nominal values is expressed as

$$V_{in} + \Delta V_{in} = \frac{V_s}{C_x + C_2 + C_{is}} \left(\frac{V_{out} + \Delta V_{out}}{B} C_2 + C_x \right) \tag{4-11}$$

In the steady-state, both sides of Equation 4-10 are equal to zero and Equation 4-11 reduces to

$$\Delta V_{in} = \frac{V_s}{C_x + C_2 + C_{is}} \frac{\Delta V_{out}}{B} C_2 \qquad (4\text{-}12)$$

Equation 4-12 presents a relationship between the deviation in the output voltage from its ideal value and the error signal required at V_{in} to compensate for the parasitic sources. The offset voltage, ΔV_{in}, was previously derived as a 30 μV square wave. Inserting the values listed in Table 4-1 into Equation 4-12 reveals ΔV_{out} = 50 mV. Adding this value to the offset voltage, V_{osm}, results in a total offset at V_{out} of 55 mV. The equivalent capacitance error of this offset is equal to 0.11 fF or about 1.1% of 10 fF full scale; see Equation 4-6. For C_{IS} = 0, the offset is only 0.19 mV+5 mV = 5.2 mV and the capacitance error is only 0.01 fF or 0.1%. The error of the final circuit with the presence of C_{IS} is much larger than the offset without C_{IS}. The reason lies with the attenuation of the gain between V_{out} and V_o due to the presence the large parasitic capacitance, C_{IS}. The offset at V_{out} required to negate the constant error at V_o is now several hundred times larger than before; 50 mV vs. 0.19 mV. Therefore, the total offset at V_{out} is no longer dominated by the input offset voltage of the feedback analog multiplier. In fact, the value of the parasitic capacitance, C_{IS}, has a large impact on the error at V_{out}. Although the value of C_{IS} may vary between sensor probes, the values of C_{IS} at each individual probe are fairly stable with temperature and voltage. Overall, however, the error is not very significant and with a small calibration effort, this offset is easily corrected.

The second part of the offset voltage at V_o is a square wave equal to 7 mV•V_s. This signal produces a triangular ripple on the output voltage, V_{out}. Derived from the integrator equation, Equation 4-3, the peak-peak value of this ripple is equal to

$$\Delta V_{outp-p} = \frac{7mV}{R_1 C_1} V_s \Delta t \qquad (4\text{-}13)$$

The time Δt is equal to one-half of a period, or 0.5 μsec. For V_s = 2 V amplitude square wave and a time constant of R_1C_1 = 10 nsec, $\Delta V_{outp\text{-}p}$ = 0.7 V. As discussed in Section 2.2, the triangular approximation of the output voltage ripple is only valid if the loop-gain of the circuit is small enough such that V_{out} does not approach the final value required to nullify the amplitude of the square wave present at V_o in one-half of the period of V_s. The final

offset value of V_{out} is determined by using Equation 4-12. The value of ΔVin is equal to V_o/V_s = 7 mV•V_s/V_s = 7 mV. Using the values listed in Table 4-1, the calculated offset voltage at V_{out} is 11.7 V. The peak-peak value of the final values is twice this, or 23.4 V. Since the 0.7 V approximation is less than 5% of this value, the ripple will approximate a triangle wave.

The large value of the output ripple is a direct result of the large value for the $1/R_1C_1$ integrator gain. The loop-gain attenuation due to the presence of the large parasitic capacitor, C_{IS}, required raising this gain to maintain the necessary dynamic characteristics. Thus, the magnitude of the ripple is indirectly attributed to the size of C_{IS}. For C_{IS} = 0 and R_1C_1 reduced to 1 μsec, the value of the ripple is only 7 mV.

The problems with the ripple and offset voltage at V_{out} are both a result of the presence of the large parasitic capacitor, C_{IS}. The effects of this capacitor can be significantly reduced by fabricating buffer transistors on the micromotor substrate between the sensor probes and the large bonding pads. This modification is discussed in more detail in Chapter 5. For testing purposes, the parasitic capacitor is not included and the component values are chosen such that the loop gain is large enough for good dynamic response, but small enough to keep the ripple at V_{out} small (R_1C_1=1 μsec). Testing results are presented in Section 4.3.

4.2 Computer Simulation

The modified circuit design, shown in Figure 4.1, is next simulated using SPICE. The component values are identical to those used in the hand analysis and are listed in Table 4-1. The simulator's dislike for high-impedance nodes requires the addition of a large resistor between the positive input node of the follower amplifier and ground. A value of 10 MΩ was used. The SPICE input file is similar to the one listed in Appendix 3. Figure 4.6 shows a combined plot of the ideal circuit output voltage as a function of time for a step in sensor capacitance from 10 fF to 5 fF. The graph shows responses for three different values of loop-gain. A second SPICE simulation, shown in Figure 4.7, analyzes the output transient for the same step with the parasitic capacitor, C_{IS}, present. The 10 MΩ resistor placed between V_{in} and ground is replaced by a 1 MΩ resistor; the value calculated in Section 4.1. Once again, the response for three separate values of loop-gain are shown. The

integrator time constant, R_1C_1, is used as a parameter to vary the loop gain in both cases.

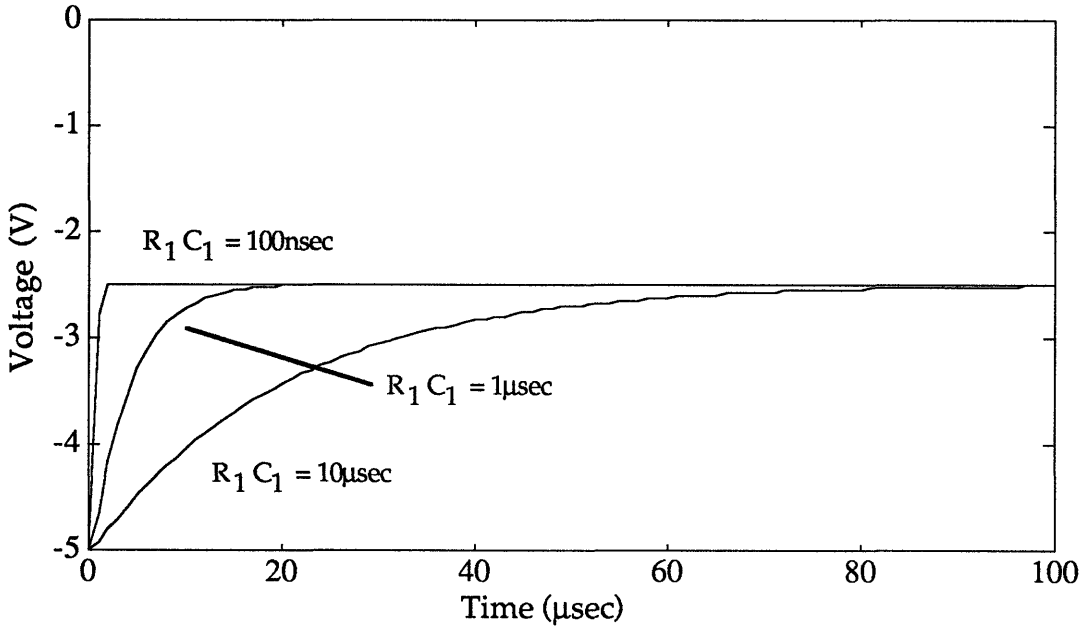

Figure 4.6: SPICE Simulation of a Step without Parasitic Capacitance

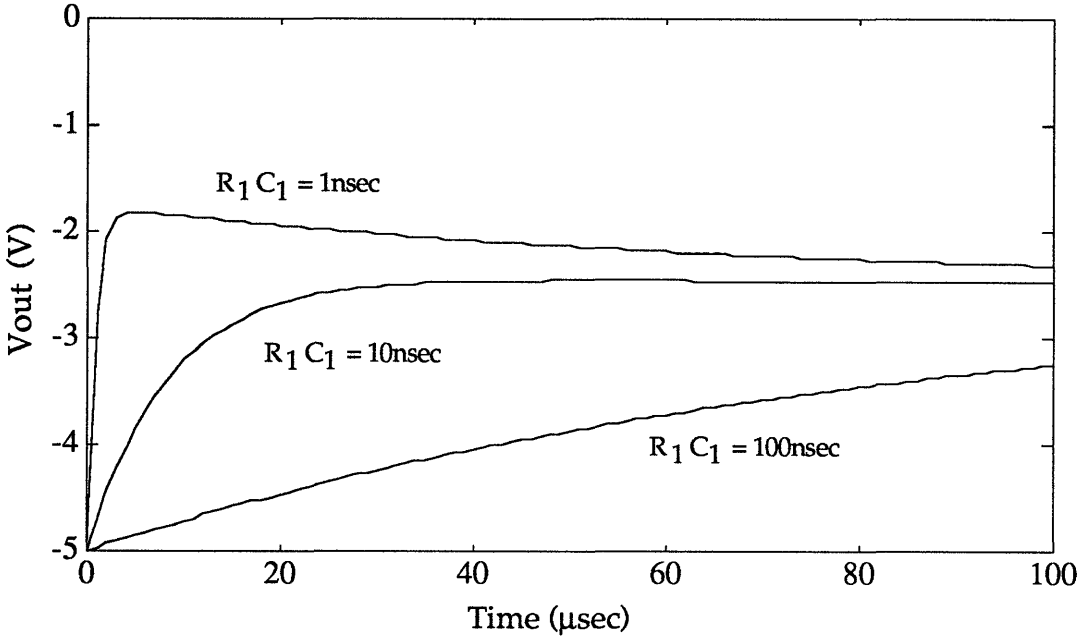

Figure 4.7: SPICE Simulation of a Step with Parasitic Capacitance

The simulated dynamic response graphed in Figure 4.6 is almost identical to the hand-analyzed result plotted in Figure 4.3. The computer simulation of the ideal circuit confirms the analysis of Section 4.1.

The 10 nsec and 100 nsec curves shown in Figure 4.7 closely resemble the hand analysis graphs of Figure 4.4. However, the 1 nsec curve has a significant overshoot which decays with a time constant of about $1/RC_{IS}$ = 67 μsec, where R is the large resistor placed between V_{in} and ground. The mathematical analysis presented in Section 4.1 did not include the resistor, R. The presence of this overshoot is a significant problem because the rise-time of the fastest transient shown in Figure 4.7 looks to be on order of 35 μsec. This slow time is pushing the lower limit of the ability to accurately sense the position of the micromotor. This adds further evidence for the need to suppress the effects of C_{IS} by fabricating buffer transistors between the sensors and bonding pads.

Next, a simulation is run to determine the effects of the parasitic sources on the output. Figure 4.8 shows the steady-state output voltage for C_{IS} = 6.7 pF and the integrator time constant, R_1C_1, equal to 10 nsec.

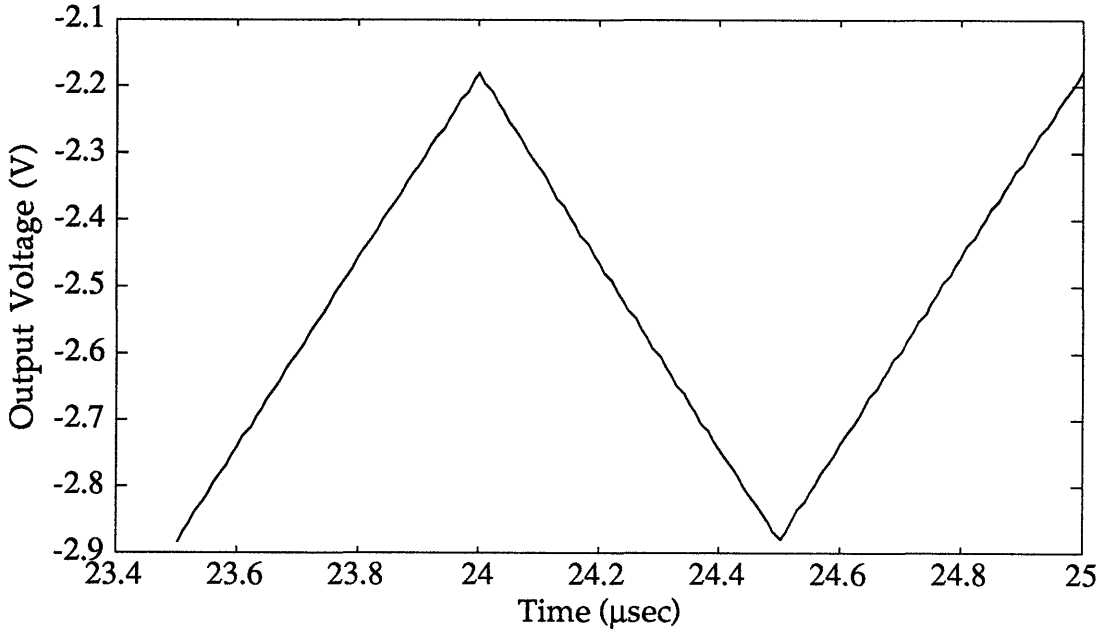

Figure 4.8: Output Voltage Ripple, C_{IS} = 6.7 pF; R_1C_1 = 10 nsec

The output ripple voltage shown in Figure 4.2.3 has an average voltage of -2.5317 V and a peak-peak ripple of 0.7 V. The output voltage offset and ripple values predicted by the analysis presented in Section 4.1 are 55 mV and 0.7 V respectively. The predicted and calculated values for the ripple voltage match exactly. The offset voltage, however, is somewhat smaller than expected.

Figure 4.9 shows the steady-state output voltage for the case when C_{IS} = 0, R_b = 1 MΩ, and the integrator time constant, R_1C_1, is equal to 1 μsec.

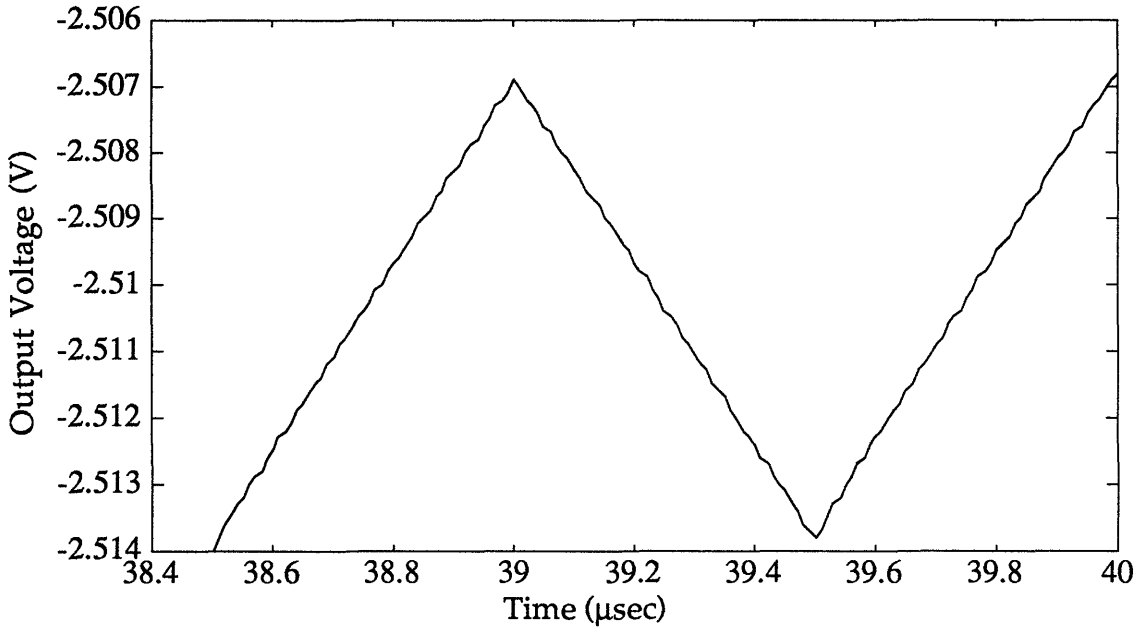

Figure 4.9: Output Voltage Ripple, C_{IS} = 0; R_1C_1 = 1 μsec

The ripple voltage shown in Figure 4.9 has an average value of -2.5104 V and a ripple voltage of 7 mV. The predicted values for the offset and ripple at V_{out} are 5.2 mV and 7 mV respectively. As in the previous case, the predicted and simulated ripple voltages match exactly. However, the offset voltage is larger than predicted. This is likely due to the presence of the 1 MΩ resistor placed between V_{in} and ground to give the bias current an outlet. With the parasitic capacitor, C_{IS}, removed, the 1 MΩ resistor no longer has a large impedance compared with the capacitive elements in parallel with R. The impedance of the feedback and sensor capacitors are 8 MΩ and 32 MΩ respectively at a frequency of 1 MHz. These values predict a voltage division

at V_{in} of 1 MΩ/(1 MΩ + 8 MΩ) = 0.11. Thus, the offset at V_{out} due to the dc value at V_o should be a factor of nine larger. From Section 4.1, this value is 0.19 mV•9 = 1.7 mV. Adding this value to the offset voltage at the input to the feedback multiplier still does not explain the entire discrepancy.

The voltage division at V_{in} due to the small value of R_b has the same effect on the dynamic response as does the presence of C_{IS}. As expected, a simulation of the circuit with C_{IS} = 0 and R_b = 1 MΩ reveals a slower step response. In the case when C_{IS} = 0, the offset voltage at V_{out} due to the flow of bias current through R_b is small. Therefore, it is advantageous to increase the value of this resistor to improve the dynamic performance.

The computer simulations of the final circuit design confirms the accuracy of the analyzed results presented in Section 4.1.

4.3 Experimental Design

To test the final design of the capacitance measurement circuit, the schematic shown in Figure 4.1 was soldered together on a perfboard. To help mitigate effects due to stray capacitance, circuit topography was carefully considered. The final layout is shown below in Figure 4.10. The schematic presents the details of the design and shows the approximate relative positions of the components.

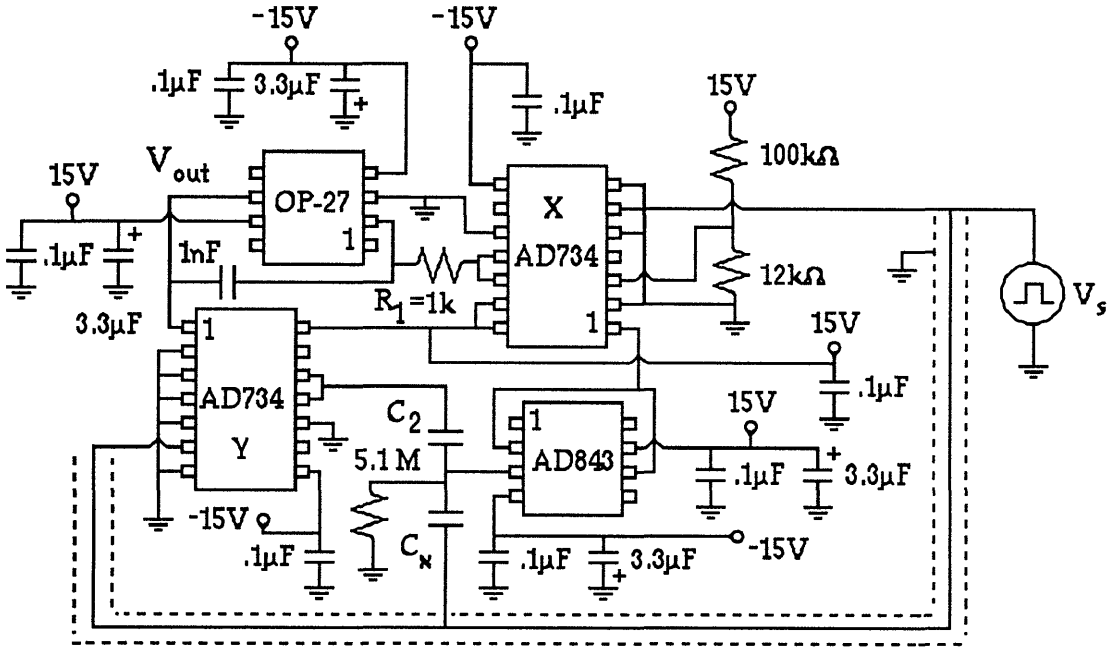

Figure 4.10: Detailed Layout of Capacitance Measurement Circuit

The AD734 labeled "X" is the forward multiplier and is configured for a denominator value of 1 V. The AD734 labeled "Y" is the feedback multiplier with a denominator equal to the default, 10 V. An OP-27 operational amplifier was used for the integrating op-amp. The OP-27 has specifications similar to the OP-07 for parasitic sources and better performance in the areas of noise voltage and slew rate. The shielded wire from the drive voltage, V_s, to the feedback multiplier is a length of coaxial cable. An external power supply provides the +15 V and -15 V potentials. As shown, these supply voltages are bypassed with decoupling capacitors. The 3.3 μF tantalum electolytic and 0.1 μF ceramic capacitors are soldered very near to the individual microchips. The reference capacitor, C_2, is chosen to be as small as practical for a discreet component, about 150 fF; real micromotors will have a reference capacitor integrated on the chip. Since standard capacitor values less than 1 pF are not available, C_2 was hand-made by gluing two small copper squares to a piece of plexiglass and soldering leads to each side.

To improve the practicality of the measurement circuit, it is desirable to implement the square wave drive, V_s, on the same perfboard. Doing this allows the circuit to perform its measurement function without the presence of a function generator. Additionally, the close proximity of the square wave helps to eliminate stray capacitance problems caused by long wire leads.

The most common methods of implementing a square wave include a crystal oscillator, 555 timer, and Schmitt Trigger. The main attribute of a crystal oscillator is to provide a very accurate and stable frequency. The capacitive measurement circuit design does not require a precise frequency of a crystal to operate correctly. The 555 timer provides a good square wave, but the bandwidth of the device is much to low to accommodate a 1MHz signal. The third and best choice is to build a square wave from a Schmitt Trigger.

The 74LS14 is a TTL Schmitt Trigger with a rise-time of 20 nsec. The proper configuration of an external resistor and capacitor causes the 74LS14 to oscillate between zero and 2.4 V at a frequency approximately equal to 1/RC. Unfortunately, the hysteresis curve of the 74LS14 is non-symmetrical. This shortcoming results in a waveform with a duty cycle significantly different from 50%. The symmetry of the square wave is important because it must be capacitively coupled to provide the measurement circuit with a waveform which has no dc offset. If the duty cycle is not 50%, then the positive and negative amplitudes of the coupled waveform are not equal. Multiplying two

signals of this type together results in a square wave superimposed upon a dc value. The presence of the square wave causes a voltage ripple at V_{out}.

To correct for the asymmetry of the Schmitt Trigger, a counter is used. The output frequency of the 74LS14 is designed to be twice the desired frequency of V_s. This signal is sent to the input of the 74LS161 counter. The output is taken from the first bit of the counter which increments for each rising edge of the square wave. Since the rising edges of the input signal occurs at equal intervals, the output of the counter is a symmetric square wave with a frequency equal to one-half that of the input. The counter output is buffered with a high-speed operational amplifier in order to drive the multipliers and sensor capacitor. The square-wave generator is shown below in Figure 4.11

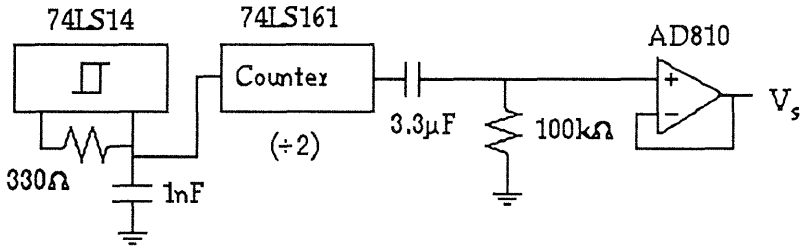

Figure 4.11: Square-Wave Generator

To accurately characterize the steady-state output voltage of the circuit as a function of the sensor capacitance, a precise method of controlling the value of C_x is required. One way to do this is to build a variable parallel-plate capacitor. The device constructed to perform this task is shown below in Figure 4.12.

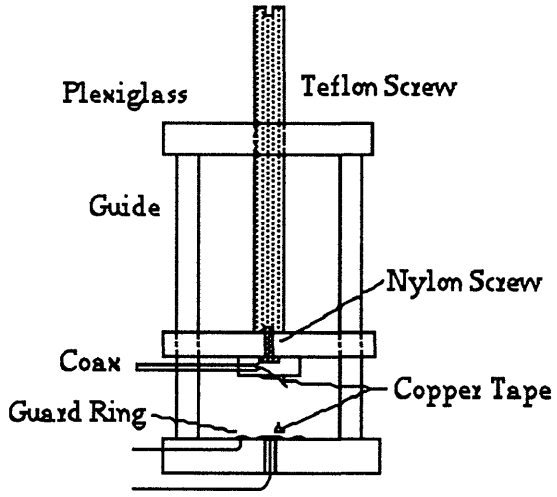

Figure 4.12: Variable Capacitor Device

The device pictured in Figure 4.12 is similar in concept to a test capacitance built by Reinoud F. Wolffenbuttel for a capacitance-to-phase angle measurement circuit [14]. The support structure of the device consists of two plexiglass rectangles about 5 cm x 4 cm x 0.5 cm separated by two 8 cm plexiglass dowels. A third rectangle is placed between the top and bottom plates and is free to move up and down along the dowel guides. A threaded teflon screw is guided by the top piece of plexiglass and attached to moveable platform with a nylon screw. A small copper square which forms one plate of the capacitor is glued to a small piece of plexiglass (1 cm x 1 cm) and is attached to a length of coaxial cable through a drilled access hole. A relief hole for the head of the nylon screw is machined into this small piece of plexiglass and then this assembly is glued to the platform. The second plate of the capacitor is soldered to a length of wire and glued to the base of the structure. A small hole is drilled in the base to give the wire an outlet. A grounded guard ring surrounds this plate to help mitigate effects of stray capacitance. The capacitance between the two plates is varied by rotating the teflon screw.

To test the dynamic behavior of the circuit, a method of applying a step input is needed. However, creating a step in capacitance is a difficult task. A much easier approach to this problem is to produce a step in the amplitude of the voltage driving the sensor capacitor, C_x. This alternative is more easily seen by examining the equation for the error voltage, V_{in}, given earlier as

Equation 4-10 and modified here for the case when $C_{IS} = 0$. This equation states that

$$V_{in} = \frac{\frac{V_{out} V_s}{B_1} C_2 + V_s' C_x}{C_2 + C_x} \tag{4-14}$$

where V_s' is the voltage input to the sensor capacitor. In the steady-state, $V_{in} = 0$. From Equation 4-14, a step in C_x produces a step in V_{in}. A similar result is achieved by producing a step in V_s'. Therefore, step-modulating the amplitude of the square-wave driving C_x has the same dynamic effect on the system as a step change in C_x. The test setup including the amplitude modulation is shown below in Figure 4.13.

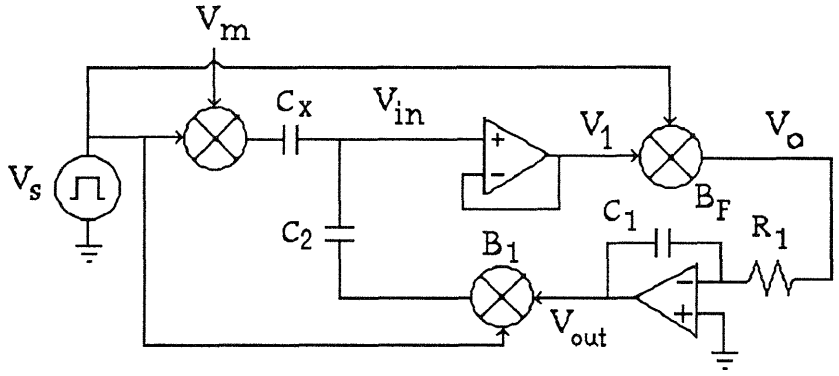

Figure 4.13: Test for Dynamic Response

The multiplier used in Figure 4.13 to modulate the input signal to the sensor capacitance is the AD734B, configured for a denominator voltage of 1 V. V_m is supplied by a function generator. The results of these experiments is presented in the following section.

4.4 Experimental Data

The first experiment to be performed on the experimental version of the final design is to measure of the steady-state output voltage as a function of sensor capacitance. The variable-capacitance device pictured in Figure 4.12 is used as C_x. The device is adjusted until the output voltage of this circuit reads 10 V full scale. The value of C_x for that point is then determined by removing the variable capacitor from the circuit and measuring it on a Hewlett-Packard (HP) capacitance meter. Twelve additional data points are then recorded for

steps down in C_x of 5 fF each. Each data point is obtained by first connecting C_x to the HP capacitance meter and rotating the teflon screw until the desired value appears on the readout. Next, C_x is reinserted into the circuit and the output voltage is measured. Four more measurements of V_{out} are recorded by removing C_x and then reinserting it into the circuit. Once complete, the variable capacitor is returned to the HP capacitance meter and its value is measured again. The final recorded value for C_x is the average of the two HP measurements. The variable capacitor is then adjusted to the next desired value and the process is repeated. The recorded data is presented in Table 4-3.

The average measured value for C_x shown in Table 4-3 is the absolute reading recorded on the HP capacitance meter. With nothing connected to the meter, its readout gives an average value of approximately 52 fF. Column 2 in Table 4-3 gives a listing of the adjusted value for C_x equal to the difference between absolute reading of the meter and the 52 fF offset. The average V_{out} vs. the adjusted value for C_x is plotted in Figure 4.14.

Table 4-3: Static Measurement Data

Average Measured C_x	Adjusted Value for C_x	Average Value of V_{out} (V)	Twice Standard Deviation (V)
121 fF	69 fF	-10.18	0.29
115 fF	63 fF	-9.55	0.34
110 fF	58 fF	-8.60	0.13
104.5 fF	52.5 fF	-7.31	0.31
100 fF	48 fF	-6.94	0.04
95 fF	43 fF	-6.40	0.06
90 fF	38 fF	-6.25	0.10
85 fF	33 fF	-5.64	0.09
80.5 fF	28.5 fF	-4.50	0.07
75 fF	23 fF	-3.81	0.08
70 fF	18 fF	-3.22	0.13
65 fF	13 fF	-2.29	0.09
60 fF	8 fF	-2.00	0.11

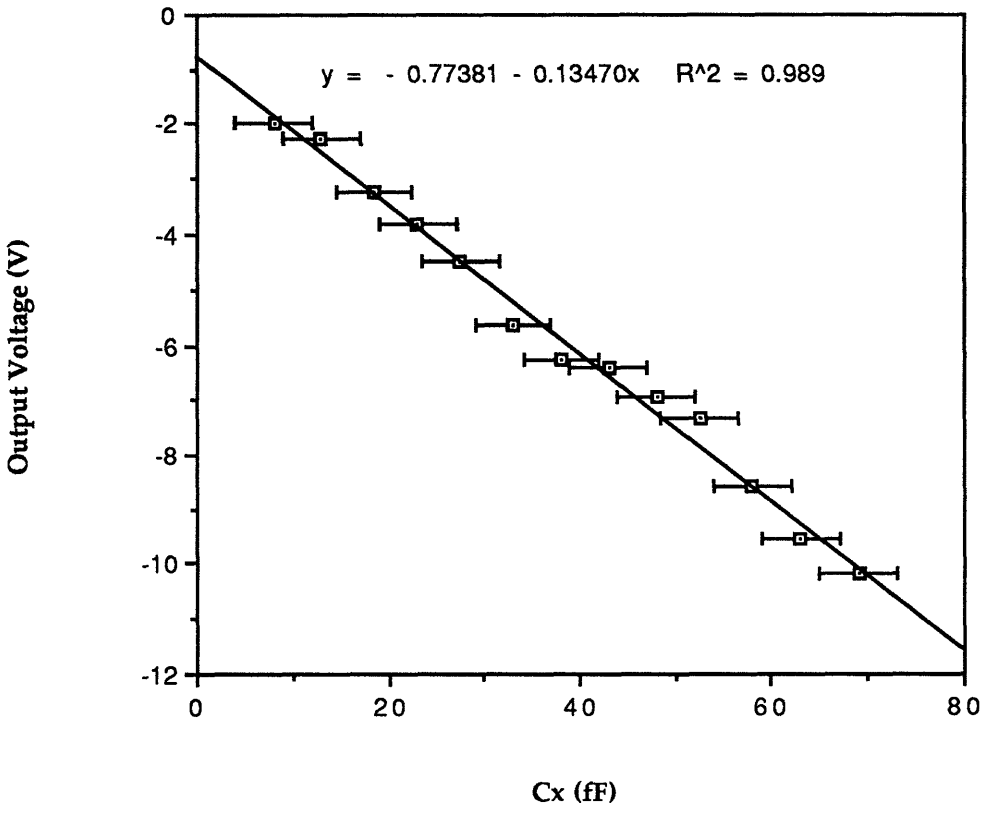

Figure 4.14: Graph of Output Voltage vs. Sensor Capacitance

The error-bars presented on the graph shown in Figure 4.14 reflect the uncertainty of the true value of C_x from the measured value. The two causes of uncertainty accounted for in the graph include the readout resolution and the drift of the offset. The meter readout has a resolution of 1 fF. The drift observed in the zero-capacitance offset reading is 3 fF. Therefore, the error bars shown in Figure 4.14 have a value of ±2 fF.

The ripple voltage is examined using a Tektronix digital oscilloscope. Figure 4.15 shows the ripple when the integrator resistor, R_1, is equal to 1 kΩ The ripple shown in Figure 4.16 is for the case when R_1 = 100 Ω.

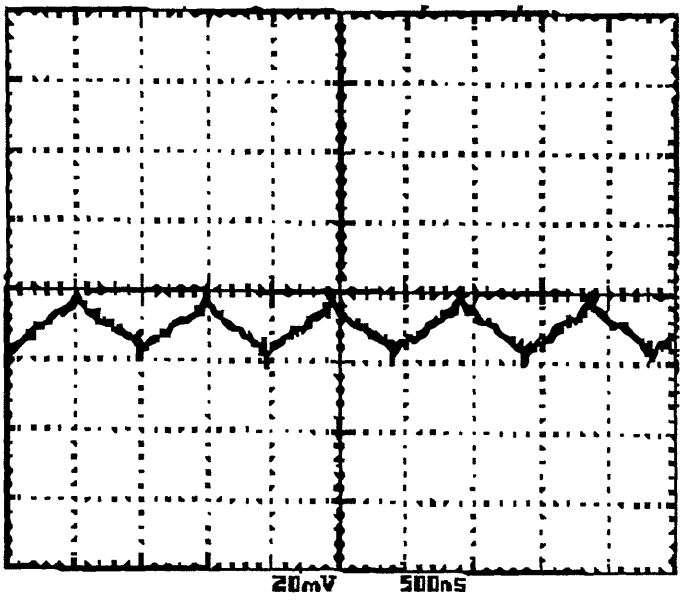

Figure 4.15: Output Voltage Ripple R_1 = 1 kΩ

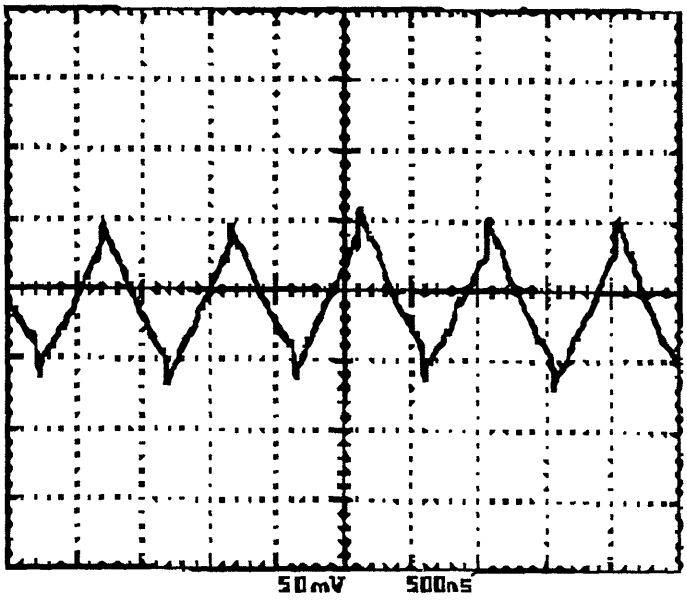

Figure 4.16: Output Voltage Ripple R_1 = 100 Ω

The dynamic response of the circuit is tested using a modulated square wave drive for C_x as shown in Figure 4.13. An oscilloscope snapshot of this signal is given below in Figure 4.17. Figures 4.18 and 4.19 show typical step responses for R_1 = 1 kΩ and 100Ω respectively.

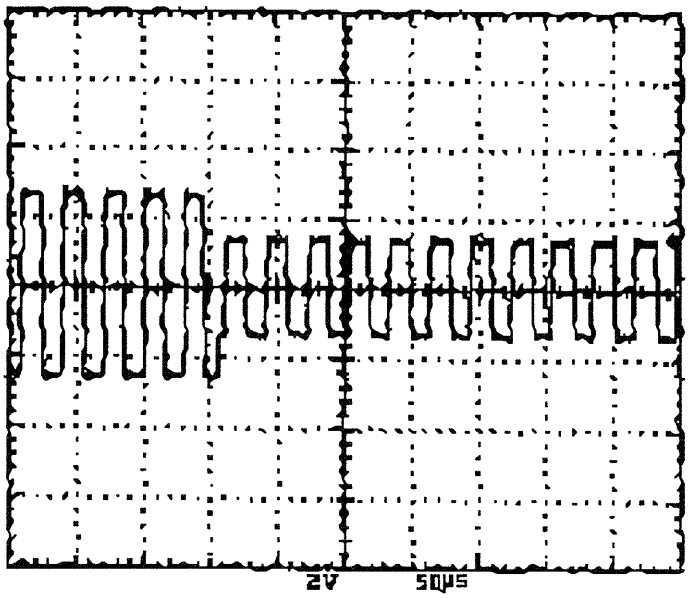

Figure 4.17: C_x Drive Signal for Dynamic Testing

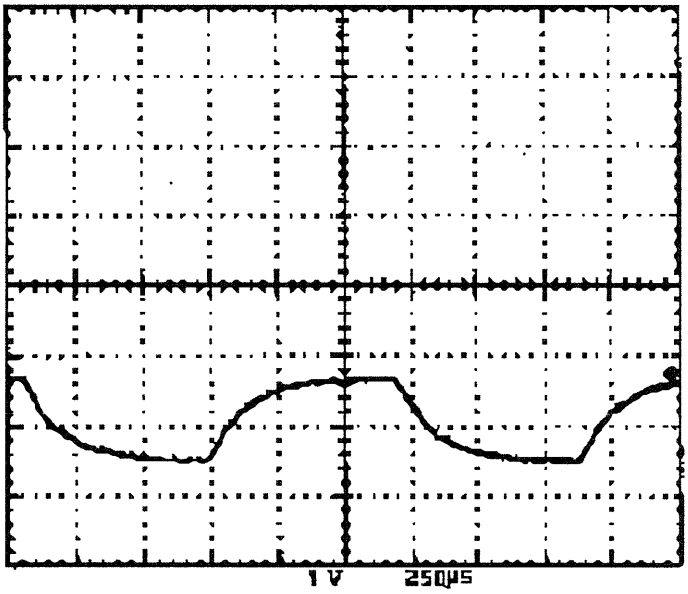

Figure 4.18: Dynamic Response for R_1 = 1 kΩ

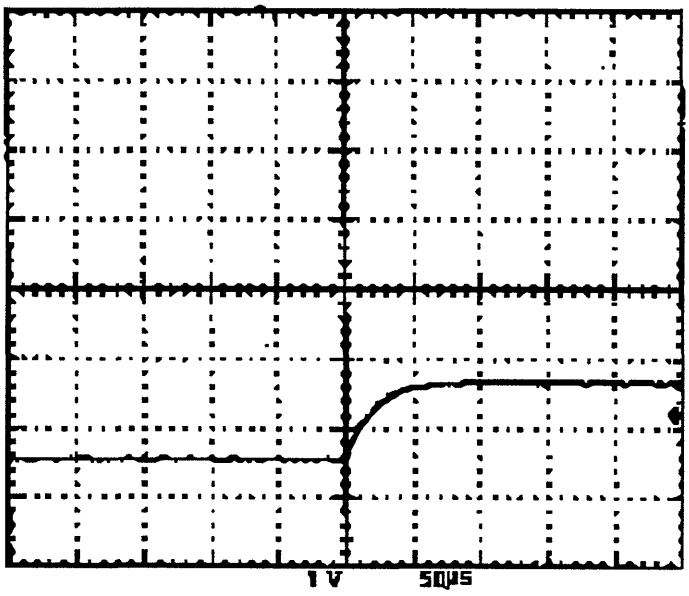

Figure 4.19: Dynamic Response fore $R_1 = 100\ \Omega$

4.5 Discussion of Experimental Results

The results of the static analysis are graphed in Figure 4.14. The linear approximation to the data has a slope of -0.135 V/fF and an offset value of -0.774 V. Equation 4-6 gives the steady-state relationship between the output voltage and the value of C_x as

$$V_{out} = -B_1 \frac{C_x}{C_2} \tag{4-15}$$

The multiplier divisor voltage, B_1, is set to its default of 10 V. Setting the slope of Equation 4-15 equal to the slope of the best-fit line from Figure 4.14 gives a measure of the reference capacitance equal to 74 fF. The offset voltage therefore corresponds to a capacitance value in parallel with C_x equal to 5.7 fF. A parasitic capacitance of 6 fF in parallel with C_x is not an unreasonable value. In fact, it seems a bit small. The calculated value for C_2 is smaller than the measured value of 150 fF. A somewhat smaller value for C_2 is expected because the leads are shortened when soldered in place. However, some additional capacitance due to proximity of the leads makes up for some of this loss. The 4 fF error bars shown in the graph imply that measurement uncertainly sufficiently explains the non-alignment of the points. However, additional sources of error influence the results. Measuring the capacitance

on the meter requires keeping human hands in the vicinity of the measurement probes. Stray capacitance due to motion and the unrepeatability of the physical arrangement are sources of additional errors. Small errors are also caused by differences in physical placement of C_x when it is connected to the circuit. Nonetheless, the ability to measure femtofarad changes in C_x is successfully demonstrated. A much better test of the linearity of the steady-state output voltage is to perform an experiment which does not require the removal of the variable capacitor from the circuit. This requires the ability to know the value of C_x as it is varied.

The output voltage ripple for the case when $R_1 = 1\ k\Omega$ is measured from the oscilloscope plot in Figure 4.15 as 12 mV. The worst-case ripple calculated in Section 4.1 for the case when $C_{IS} = 0$ and $R_1 = 1\ k\Omega$ is 7 mV. The measured ripple is not significantly different from the calculated one. However, the measured ripple is larger than the calculated worst-case. This is likely explained by non-idealities in the square wave drive. A quick look at Figure 4.16 shows that the actual square wave does not have a zero rise time nor is it perfectly clean. When these irregularities are squared, a small ac wave pattern is superimposed on the dc value at V_o, adding to the output ripple. When the value of R_1 is reduced to 100 Ω, the gain of the feedback integrator is increased by a factor of 10. Figure 4.16 shows that the ripple also increases by a factor of 10, to 120 mV. This result completely agrees with the analysis performed in Section 3.1.

The response of the output voltage to a step in input with the integrator resistor equal to 1 $k\Omega$ is shown in Figure 4.17 to have a risetime of 200 μsec. When R_1 is reduced to 100 Ω, the risetime is about 30 μsec. Both of these values are significantly lower than the 10 μsec and 1 μsec risetimes predicted in Section 4.1. Some of the discrepancy is explained by attenuation in the loop gain caused by the presence of the 5.1 $M\Omega$ resistor placed between V_{in} and ground. At a frequency of 1 MHz, the impedance of the 150 fF reference capacitor is 1 $M\Omega$. Therefore, the attenuation between the output and V_{in} is 0.84. This alone explains a factor of 1.2 out of 20 in the bandwidth. Parasitic capacitance between the summing node and ground attenuates the loop gain even more. A third reason for a slower step-response originates with the frequency characteristics of the active circuit elements. The analysis performed in Section 4.1 assumes that the multipliers and op-amps have infinite bandwidths. This is, of course, a false assumption. For instance, the

output buffers of the AD734B analog multipliers have a bandwidth of only 8 MHz. Therefore, the active devices in the circuit also contribute to a slower ristetime.

4.6 Summary

The final design solves the implementation problem by replacing the differentiator with a simple follower. This modification removes the virtual ground node at V_{in}, causing the large parasitic capacitor, C_{IS}, to have a profound negative impact on the dynamic response. However, modifying the micromotor by integrating a buffer amplifier between the sensor electrodes and the bonding pads suppresses this capacitor and makes the final design very practical. For the case when $C_{IS} = 0$, the offset and ripple at the output due to parasitic sources are on the same order as the modified design; the equivalent offset capacitance is 0.01 fF and the ripple error is 0.07% of full scale. The experimental results performed on an implemented version of the final design show a linear relationship between the output voltage and C_x. The rise-time of this circuit is slower than the analysis predicts. This is explained by the presence of R_b between V_{in} and ground as well as the additional poles inherent to the active devices. The ripple voltage at V_{out} is slightly larger than expected, but is explained by the non-idealities present in the squarewave.

Chapter 5

Summary, Conclusions, and Suggestions for Future Work

5.1 Summary

This thesis presents a circuit to be used as a position sensor for a microfabricated electric motor. The circuit accomplishes this task by measuring the capacitance between the blades of the rotor and sensor pads implanted into the substrate beneath the rotor. This capacitance typically varies between five and fifteen femtofarads as the rotor turns. The upper limit of the motor dynamics requires the circuit to have a risetime of less than 40 μsec. Additionally, the maximum amplitude of the drive signal applied to the sensors is limited to 2 V so as to prevent the pull-down force exerted on the rotor by the voltage applied to the sensors from becoming large enough to stop the rotor from turning. The main design obstacle is the large parasitic capacitors located between the bonding pads and ground. The closed-loop technique for capacitive measurement is chosen to because the virtual ground node inherent to the design suppresses the shunting effect of these large capacitors. This measurement technique is found to be successful.

The initial circuit design examined in Chapter 3 is based on the closed-loop technique for capacitive measurement and was first proposed by D. Marioli, E. Sardoni, and A. Taroni. A full mathematical analysis of the circuit is performed followed by a SPICE simulation to confirm the results. The circuit adequately meets the specifications with a risetime of 18 μsec. Additionally, the offset error due to the presence of parasitic sources is small. A negligible scale error is also present. The major problem with the circuit is that it is difficult to implement.

The modified design presented in Chapter 2 is an improvement over the initial design in both simplicity and performance. Once again, the circuit is analyzed both mathematically and with the aid of SPICE. The speed of the modified circuit is improved by more than a factor of two, the offset error is reduced by a factor of eight, and the scale error is eliminated. However, the removal of the low-pass filter from the design allows a triangular ripple

voltage to appear at the output. The peak-peak value of the ripple increases with increasing loop-gain. For moderately fast risetimes, the magnitude of the ripple is only about 0.22% of full scale. The only problem with the modified circuit is the difficulty of implementing a practical differentiator within the frequency and gain constraints.

The final design examined in Chapter 4 solves the implementation difficulties of the modified design by replacing the differentiator with a follower amplifier. The steady-state characteristics of the circuit are unchanged by this modification. However, because the voltage across the parasitic capacitor is no longer forced to a virtual ground potential, the large parasitic capacitor, C_{IS}, is no longer suppressed during the dynamic response. This capacitance attenuates the loop gain by more than a factor of 100 and therefore reduces the response time by the same two orders of magnitude. The attractiveness of this circuit design leads to another solution for suppressing C_{IS}, the integration of a buffer amplifier between the sensor pads and the bonding pads. This modification to the micromotor fabrication makes the final circuit design practical. Mathematical and computer analysis compare the dynamic performance of the final design for the cases with and without C_{IS}. The effect of the parasitic sources on the final design in the presence of C_{IS} is magnified. In order to meet the risetime constraint, the loop-gain of the must be dramatically increased. The larger loop gain magnifies the ripple voltage by an amount proportional to the increase in gain. The offset voltage at V_{out} increases to an equivalent capacitance error of 0.11 fF because of the signal attenuation between the output voltage and the error signal. When C_{IS} is removed, the same analysis reveals errors on the same order as those calculated in the modified design.

The experiments performed on the implemented version of the final design shown in Figure 4.10 produce results which are either consistent with the analysis or explained by circuit non-idealities. The steady-state output voltage is a linear function of the sensor capacitor. The risetime of the circuit is slower than expected, but this is explained by attenuation at the buffer input due to bias resistance and the additional frequency characteristics of the active devices. The ripple voltage is slightly larger than expected and is likely caused by non-ideal components present in the squarewave. Table 5-1 summarizes the performance characteristics of the designs examined in Chapters 2 through 4. The ripple error is expressed as a percentage of full scale.

Table 5-1: Comparison of Circuit Performance

Design	Risetime	Offset Error	Scale Error	Ripple Error
Initial	18 μsec	0.08 fF	0.4 aF/V	0
Modified	8 μsec	0.01 fF	0	0.22%
Final with C_{IS}	31 μsec	0.11 fF	0	7%
Final without C_{IS}	8 μsec	0.01 fF	0	0.07%
Experimental No C_{IS}	30 μsec		0	1.2%

5.2 Conclusions

A discrete circuit capable of detecting femtofarad changes in capacitance in the presence of picofarad parasitic capacitances for application to microfabricated electric motor position sensing is achievable. The implementation of the final circuit design demonstrates that sensitivities of this level are realizable. However, some additional work is needed to successfully implement the circuit as a position sensor for a micromotor. In particular, buffer amplifiers are needed between the sensor electrodes and bonding pads to suppress the large parasitic capacitances which otherwise will completely obscure the capacitors of interest.

5.3 Suggestions for Future Improvements

There are several improvements to the circuit which have the potential to enhance the performance. First, when the micromotor is rotating, the sensor capacitance, C_x, as a function of time is a ramp; see Figure 1.5. For the circuit to track a ramp input and have no steady-state error, two integrators are required in the feedback path. Of course, the addition of an integrator compromises loop stability because the phase shift is greater than 180 degrees. Therefore, a compensating zero must also be added in addition to a second integrator.

As discussed in Chapter 4, the dynamic response of the final design is severely compromised by the presence of the large parasitic capacitor, C_{IS}. An additional problem presents itself when the discrete capacitive measurement circuit is directly connected to an integrated micromotor. When the lead wires are bonded to the pads, a significant capacitance exists between these wires. A schematic of this is shown below in Figure 5.1.

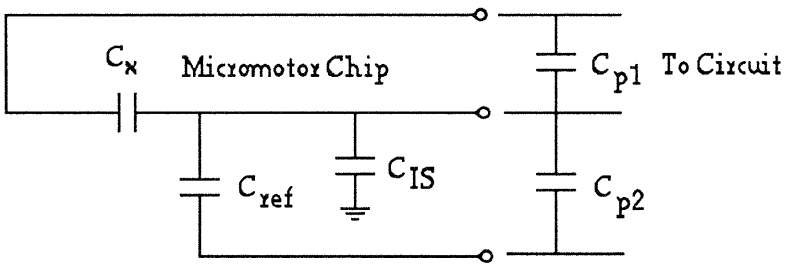

Figure 5.1: Interconnect Between the Discreet Circuit and a Real Motor

The magnitudes of capacitors C_{p1} and C_{p2} are on the order of 1 pF. Additionally, these capacitors are in parallel with the reference capacitor and the sensor capacitor. The small sizes of C_x and C_{ref} will cause their effects to be minimal. Fabricating a buffer transistor between the junction of C_x and C_{ref} and the bonding pad for these elements alleviates both problems. The modified micromotor schematic is shown in Figure 5.2.

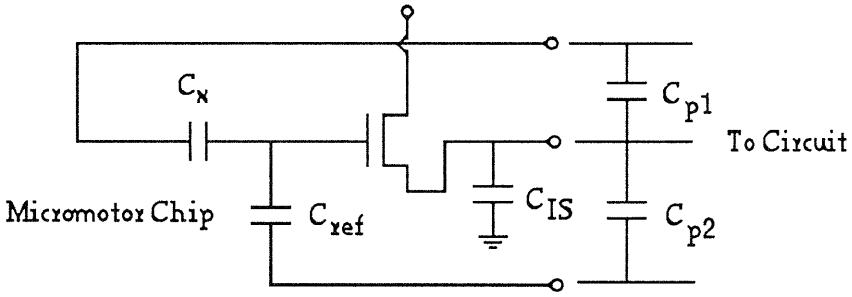

Figure 5.2: FET Buffer Implementation

Now, with the modified design shown in Figure 5.2, the charge from C_x and C_{ref} only divides with the input capacitance of the FET. The buffer transistor is driving the parasitic capacitors, improving circuit performance dramatically.

Appendix 1

Derivation of Discreet Numerical Solution to: $\dot{x} = Ax+Bu$

Equation 2-11 is repeated here as

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + \int_{t_0}^{t_1} e^{A(t_1-t)}Bu(t)dt \qquad \text{(A1-1)}$$

The vector $x(t_o)$ describes the initial conditions and is independent of time. Further, we assume that u(t) is constant over the interval t_o to t_1. Then, selecting a substitutional variable, $\eta = t_1 - t$ so that $d\eta = -dt$, Equation A1-1 becomes

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) - \left[\int_{t_1-t_0}^{0} e^{A\eta}d\eta\right]Bu(t_o) \qquad \text{(A1-2)}$$

Reversing the limits of integration, Equation A1-2 becomes

$$x(t_1) = e^{A(t_1-t_0)}x(t_0) + \left[\int_{0}^{t_1-t_0} e^{A\eta}d\eta\right]Bu(t_0) \qquad \text{(A1-3)}$$

Inserting Equation A1-3 into the original differential equation $\dot{x} = Ax + Bu$ results in

$$Ae^{A(t_1-t_0)}x(t_0) + e^{A(t_1-t_0)}Bu = Ae^{A(t_1-t_0)}x(t_0) + A\left[\int_{0}^{t_1-t_0} e^{A\eta}d\eta\right]Bu + Bu \qquad \text{(A1-4)}$$

Solving for the definate integral reveals

$$\left[\int_{0}^{t_1-t_0} e^{A\eta}d\eta\right] = A^{-1}\left[e^{A(t_1-t_0)} - I\right] \qquad \text{(A1-5)}$$

provided that A^{-1} exists, where I is the identity matrix. Combining Equations A1-3 and A1-5 yields

$$x(t_1) = e^{A(t_1 - t_0)}x(t_0) + A^{-1}\left[e^{A(t_1 - t_0)} - I\right]Bu \qquad \text{(A1-6)}$$

which is a computable solution to the equation $\dot{x} = Ax + Bu$ for a constant u.

Appendix 2

Matlab Input File for Calculating the Transient Response from an Initial Condition

```
% Low pass filter resistor and capacitor values - ωo2=(1/RC)
R = 800;
C = .000000001;
% Integrator resistor and capacitor values - control loop-gain
R2 = 750;
C2 = .00000001;
Rf = 16e6;                          % Input differentiator resistance
w = 2*3.14159*1e6;                  % input waveform frequency
Cx = 5e-15;                         % Sensor capacitance
A = 1;                              % Gain stage
g1 = (1.848 * (1/(R*C)));
g2 = (.765 * (1/(R*C)));
d = (1/(R*C))*(1/(R*C));
b = -(1/(R2*C2))/1e6;
h = (d*d*1.152*2.235*A*Rf*2/(1e6*10*10*1e24));
i = - d * d/1e24;                   % K4
j = - (d * (g1 + g2))/1e18;         % K3
k = - (2 * d + g1*g2)/1e12;         % K2
l = - (g1 + g2)/1e6;                % K1
% Full Matrix
W = [0 b 0 0 0;0 0 1 0 0;0 0 0 1 0;0 0 0 0 1;h i j k l];
B = [0;0;0;0;-Cx*w*A*Rf*d*d*1.152*2.235/(5*1e24)];   % Bu
Q = inv(W);
dt = .5;
tf = 100;
t=0:dt:tf;
Y = Q*(expm(W*dt)-eye(5))*B;
m=zeros(5,length(t));               % Create solution matrix
m(1,1)=.628;                        % Initial condition
for p = 1:length(t)-1, m(:,(p+1))=expm(W*dt)*m(:,p)+Y;
end
```

Appendix 3: SPICE Input File

```
*David Leip
*Micromotor Capacitive Sensing Circuit

* Variable capacitor subcircuit
.subckt varcap 1 2 3 0
cdf 4 5  1
rdf 5 6  1
e1 4 0 poly(2) 1 2 3 0  0 0 0 0 1
e2 6 0 0 5 1e8
gcap 2 1 6 0 1
.ends varcap

*AC excitation
vac 1 0 sin(0 2 1meg 0 0)
vneg 13 0 sin(0 2 1meg .25u 0)
*eneg 13 0 0 91 1meg        *negative 90 phase shift
*rneg 91 13 159.15
*cneg 1 91 .001u

epos 3 0 0 2 100meg         *positive 90 phase shift*
rp 1 2 159.15
cp 2 3 .001u
*rr 2 3 10k                 *integrator low-pass resistor*

*Capacitance step function
*xcx 1 4 90 0 varcap
*vcd 90 0 pwl(0 10f 198u 10f 200u 5f)

*differentiator op-amp
ediff 5 0 0 4 1meg
rf 4 5 16meg
cx 1 4 5f
*ip 4 0 1n                  *parasitic current*
*vosdiff 52 0 1m            *offset voltage*
```

```
*filter
efilter1 9 0 11 10 100meg
rf11 14 8 800
rf12 8 11 800
cf11 8 9 .001u
cf12 11 0 .001u
rf1g1 9 10 1.52k
rf1g2 10 0 10k
*ipf1 11 0 1n              *parasitic  current*
*ifp2 10 0 1n              *parasitic  current*
*vosf1 96 11 1m                 *offset  voltage*

*second  filter
efilter2 24 0 22 23 100meg
*ipf 22 0 1n               *parasitic  cur*
*ipf2 23 0 1n              *parasitic  cur*
rf21 9 21 800
rf22 21 22 800
cf21 21 24 .001u
cf22 22 0 .001u
rf2g1 24 23 12.35k
rf2g2 23 0 10k
*vosf2 95 22 1m                 *offset  voltage*

*integrator
eint 12 0 0 19 100meg
*ibint 19 0 2n             *parasitic  current*
*vosint 51 0 25u           *offset  voltage*
rint1 19 24 500
cint1 12 19 .01u
r2 4 15 1meg

*multipliers
emult1 14 0 poly(2) 5 0 3 0 0 0 0 0 .1
*vosm1a 53 5 5m            *offset  voltage*
*vosm1b 54 3 5m            *offset  voltage*
```

```
emult2 15 0 poly(2) 12 0 13 0 0 0 0 0 .1
*vosm2a 55 12 5m     *offset  voltage*
*vosm2b 56 13 5m     *offset  voltage*

.ic v(3) = 2 v(12) = .628
.tran 1u 100u uic
.print tran v(12)
.end
```

References

1. J. H. Lang,"Initial Thoughts on the Dynamics and Control of Electric Micromotors," *Integrated Micro-Motion Systems - Micromachining, Control and Applications,* Elsevier Science Publishers B. V., 1990, p 167.

2. H. A. Haus and J. R. Melcher, *Electromagnetic Fields and Energy,* Prentice Hall, 1989, p 290.

3. Neudeck, Gerold W., *Modular Series on Solid State Devices,* Second Edition, Vol II, 1989, p 95.

4. R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits,* Second Edition, Wiley, 1986,p 252.

5. David Halliday and Robert Resnik, *Fundamentals of Physics,* Third Edition Extended, Wiley, 1988, p 621.

6. J. H. Lang, "Electric Micromotrs - A Status Report," *Selected Publications on Microfabricated Electric Motors,* p 111.

7. Stephen F. Bart, Mehran Mehregany, Lee Tavrow, and others, "Electric Micromotor Dynamics," *IEEE Transactions on Electron Devices,* Vol 39, No. 3, March 1992, p 568.

8. Bing J. Sheu and Ping-Keung Ko, "Measurement and Modeling of Short-Channel MOS Transistor Gate Capacitances," *IEEE Journal of Solid-State Circuits,* Vol. SC-22, NO. 3, June 1987.

9. D. Marioli, E. Sardini, and A. TAroni, "Measurement of Small Capacitance Variations," *CPEM '90 Digest,* 1990, pp 22-23.

10. William Siebert, *Circuits, Signals, and Systems,* The MIT Press, 1986, p 133.

11. J. H. Lang, "6.142 Course Notes on Computer-Based Control Systems", Jan 1984, pp 5-7.

12. P. Horowitz and W. Hill, *The Art of Electronics*, Cambridge University Press, p 274.

13. J. H. Lang, "6.142 Course Notes on Computer-Based Control Systems", Jan 1984, p 29.

14. R. F. Wolffenbuttel and Paul P. L. Regtien, "Capacitance-to-Phase Angle Conversion for the Detection of Extremely Small Capacities," *IEEE Transactions on Instrumentation and Measurement*, Vol IM-36, No 4, Dec 1987.