A DC Stabilized Fully Differential Amplifier

by

Nancy Y. Sun

Submitted to the Department of Electrical Engineering and Computer Science

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Abstract

The conventional method of constructing a gain amplifier is to use resistor feedback networks. However, present CMOS technology provides capacitors that offer substantially better tracking and linearity performance over variations in temperature. Draper Laboratory's High Performance Gyroscope currently employs two single-ended amplifiers configured to work fully differentially. Gain is provided with capacitive feedback, but DC stabilization of the amplifiers, necessary to provide bias to the amplifier and prevent output saturation, is achieved with large, external resistors. In this thesis, a fully-differential gain amplifier using capacitive feedback is proposed. An integratable, on-chip DC stabilization network is also presented.

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Nancy Y. Sun

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Chapter 1

Overview

Micromechanical tuning fork gyroscopes are attractive as inertial devices because they offer system miniaturization and can be produced at low cost [2]. Advances in microfabrication of both sensor and accompanying electronics have led to low cost solutions for both military and commercial applications. However, in order to compete with conventional inertial systems, MEMS-scale systems must also offer high resolution and performance stability over environment variations.

Because of the miniaturization trends of inertial Micro-Electro-Mechanical Systems (MEMS), reduced signal levels present great challenges for the readout electronics. In digital circuits, CMOS technology has allowed for tremendous gains in chip density, power, and cost, without sacrificing performance. However, the same cannot be said for analog circuitry. One reason for this is the poor quality of the passive components available in most CMOS processes. These components, particularly resistors, tend to have poor tolerances and poor stability over temperature and operating voltages.

Resistor ratios are used extensively in analog circuit design. However most CMOS processes do not offer the resistor matching required to maintain precise ratios. Fortunately, CMOS technology provides capacitors with more attractive performance characteristics. This thesis explores the substitution of capacitors for resistors in an AC gain amplifier for a Draper Laboratory MEMS gyroscope.

1.1 Gyroscope System Overview

Draper's tuning fork gyroscope takes advantage of the Coriolis Effect to sense rate of rotation. Its construction is shown in Figure 1-1. The proof masses are supported by flexure beams that allow motion in the x- and y-directions at a resonant frequency ranging from 8kHz to 25kHz. The masses are suspended above stationary sense electrodes. Application from a motor of an oscillatory electrostatic force between the combs of the proof masses and those of the left and right motor electrodes cause the proof masses to vibrate in opposite directions along the x-axis (which is often referred to as in-plane motion). The Coriolis acceleration, then, is the cross product between a mass's velocity in the x-direction and the input rate of rotation about the z-axis.

1.1.1 Sense Channel

In the presence of rotation about the z-axis, the Coriolis Effect causes the proof masses to deflect in the y-direction. This deflection or displacement is referred to as an out-of-plane motion and occurs at the same frequency as the in-plane oscillatory motion. The change in the gap between the proof masses and the sense electrodes beneath them causes a change in capacitance that is directly proportional to the magnitude of the rate of rotation. The change in capacitance induces a current that is output along the sense channel. This current is integrated by the charge amplifier circuit to produce a voltage proportional to the rate of rotation.

1.1.2 Motor Position Channel

The positions of the proof masses are sensed by the left and right center electrodes in a manner similar to how the sense electrodes beneath the proof masses sense rotation. In this case, the charge amplifier integrates a charge induced by the change in capacitance of the capacitors formed between the tines on the left and right center electrodes and the inner tines on the proof masses. The charge amplifier produces a voltage proportional to the position of the proof masses.

The motor position signal will be used throughout the system as a reference clock

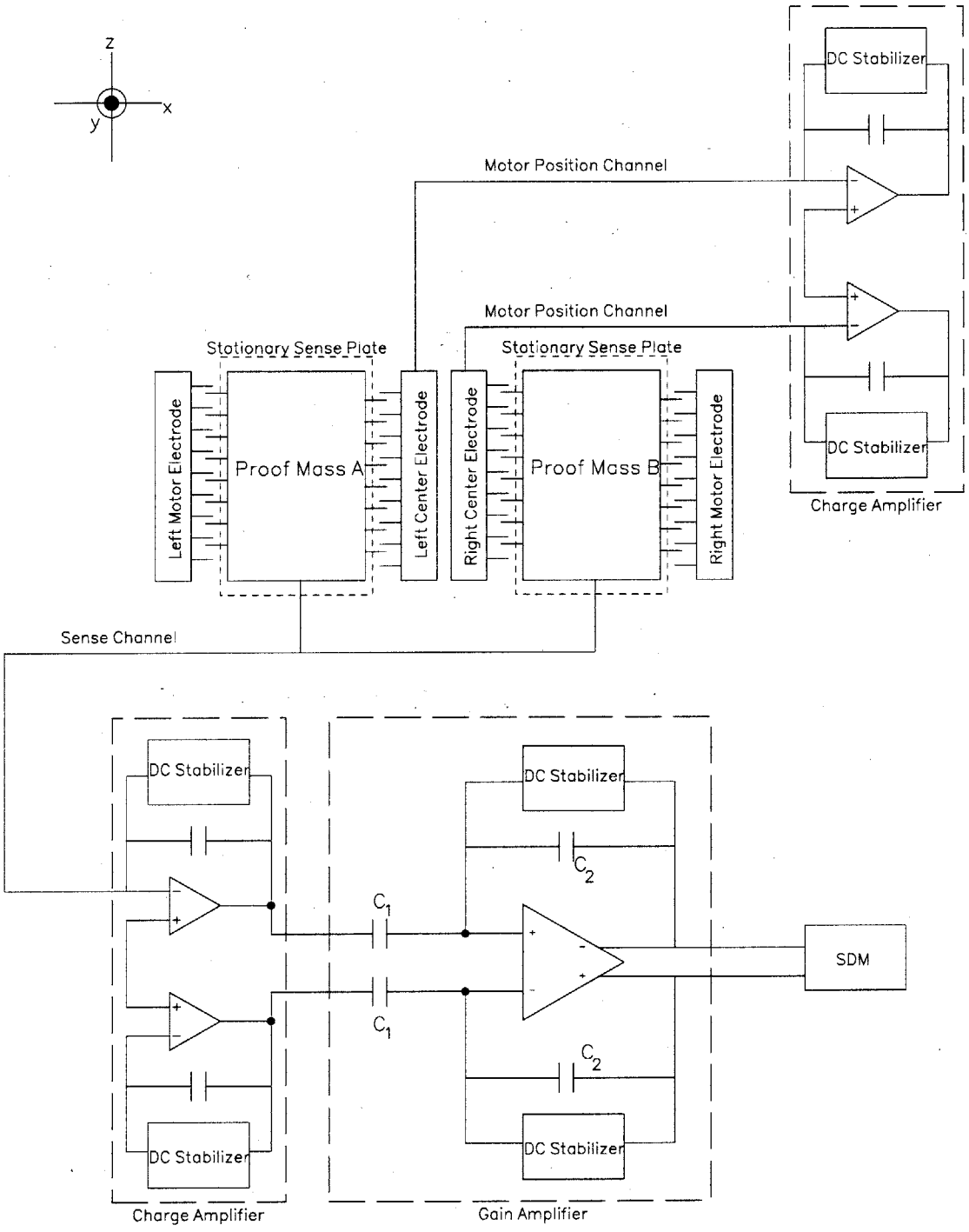


Figure 1-1: Gyroscope Block diagram.

since this signal is always available once the gyroscope's motor is started. The clock generated from the position signal will be used to demodulate the input rate information to baseband. For this reason, both the motor position and the sense channels must be designed to achieve a high level of phase matching.

1.2 Thesis Scope

There are electronics needed to operate the gyroscope that are not shown in Figure 1-1, but this thesis will only focus on a portion of the readout electronics in the sense channel. The focus of the thesis is on designing the fully differential AC gain amplifier block in Figure 1-1. The fact that the signal of interest is modulated to a frequency ranging from 8kHz to 25kHz allows us to consider substituting the typical resistive feedback network with other types of feedback networks. The following sections will discuss some of the design motivations, considerations, and requirements of the gain amplifier.

1.2.1 Temperature Sensitivity of Gain Amplifier Closed-Loop Topologies

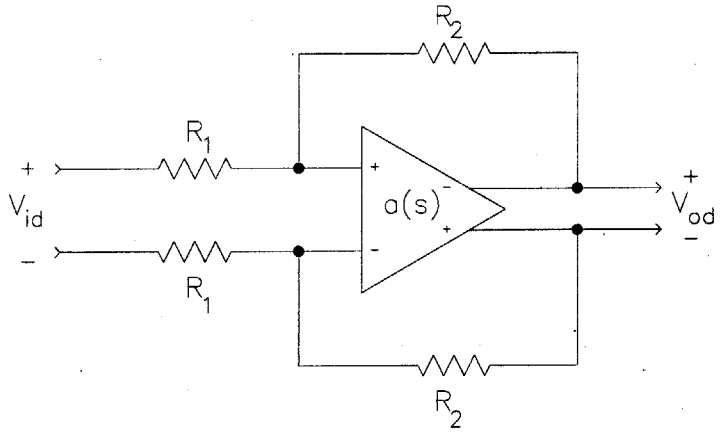


Figure 1-2: Gain amplifier with resistive feedback.

Draper Laboratory's gyroscope is designed for use in space and military applica-

tions so it must be able to operate with high precision in a wide range of temperatures. However, recent studies at Draper have shown that a gain amplifier using resistive feedback, like that shown in Figure 1-2, has an unacceptable drift in gain over temperature. Draper has shown that the on-chip resistor ratios (which are conventionally used to set gains) offer inadequate tracking over temperature, making it difficult to achieve precision gain. This issue is primarily due to the poor matching tolerance of the chosen polysilicon resistors. Furthermore, their high voltage coefficients lead to harmonic distortion. However, on-chip capacitors offer superior temperature and voltage coefficients, making them attractive feedback elements.

Tables 1.1 and 1.2 lists typical values for the most common integrated circuit resistors and capacitors. Temperature and voltage coefficients (TC and VC, respectively) are usually expressed in parts per million per degree Celcius ($\frac{ppm}{C}$). For example, a temperature coefficient of resistance of $1000\frac{ppm}{C}$ means that a 100Ω resistance will not change more than 0.01 Ω per degree Celcius change in temperature.

Unfortunately, typical CMOS processes do not offer thin-film resistors. Diffusion and N-well resistors have voltage coefficients that are too high to meet our linearity specifications. Polysilicon is a good compromise, but even with careful layout, good resistor matching is difficult to achieve.

Resistor material	TC ($\frac{ppm}{C}$)	VC ($\frac{ppm}{C}$)	Expected matching
Thin-film	<50	<30	0.5-2%
Polysilicon	50-2000	30-150	0.5-2%
N-Well	1000-50000	50000	1-2%
Diffusion	1000	1000-10000	1-2%

Table 1.1: Performance of typical resistors in today's semiconductor processes.

Capacitor material	TC ($\frac{ppm}{C}$)	VC ($\frac{ppm}{C}$)	Expected matching
Poly-diffusion	–	–	–
Metal-poly	–	–	–
Poly-poly [7]	20-30	10-200	0.2-0.5%

Table 1.2: Performance of typical capacitors in today's semiconductor processes.

1.2.2 Motivation

Because gain amplifier performance is determined by the amplifiers feedback network(s), the temperature coefficients and voltage coefficients of the components that comprise the feedback network are important metrics of amplifier performance. Tables 1.1 and 1.2 indicate that capacitor temperature and voltage coefficients are significantly better than those of resistors. This allows capacitors to track each other more accurately over temperature and voltage changes, thus minimizing harmonic distortion. Therefore, when component value and ratio matching is of great importance, capacitors are a more attractive option than resistors. Motivated by the insufficiencies of on-chip resistors, this thesis will investigate the implementation of an amplifier using capacitive feedback.

1.2.3 Performance Requirements

Some of the more notable performance requirements of the gain amplifier are described in this section.

Fully Differential Topology

Fully differential circuits are desirable in analog circuit design primarily because they are useful in rejecting common-mode noise, particularly in mixed-mode design. Since a fully differential circuit is built symmetrically, noise should affect both signal paths equally. In a fully differential amplifier, the signals at the two output terminals are subtracted from each other, so any common-mode disturbances, such as power supply noise, are rejected.

Phase Shift

Phase shift is a Draper Laboratory system requirement of all components in the gyroscope system. Once the gyroscope motor is started, the motor position signal is used as a reference signal for demodulating the rate input information to baseband. In order to minimize demodulation errors (which would result in offset and gain errors),

the sense and motor position channels must posses similar phase shift characteristics. As much as possible, identical designs are used in both channels to achieve phase shift matching.

There are two primary types of phase shift:

- **Static phase shift** - Static phase shift is how much the closed-loop output phase varies across the desired signal frequency range. The requirement is that static phase shift must be $< 1°$ from 8kHz to 25kHz.

- **Dynamic phase shift** - Dynamic phase shift is how much the closed-loop output phase across the desired signal frequency range varies across temperature. The dynamic phase must vary by $< 0.5°$ for signals from 8kHz to 25kHz within a temperature range of -55°C to 105°C. Errors due to dynamic phase shift are more problematic because dynamic phase shifts of the two channels are less likely to match.

Unity-Gain Frequency

The desired unity-gain frequency can be derived from the static phase shift requirement. The phase of a system with a single pole roll-off is given by $-\arctan\frac{signal frequency}{system-3dB bandwidth}$. For a unity-gain configuration, this means that in order for the system to have less than 1° of static phase shift at a signal frequency of 25kHz (the maximum resonant frequency of the proof masses), the -3dB bandwidth of the unity-gain system (which is also the crossover frequency of an open-loop system with 90° of phase margin) needs to be greater than 1.5MHz. As the closed-loop gain increases, however, the system open-loop crossover frequency also needs to increase to maintain the phase shift.

To see how much the open-loop crossover frequency needs to increase, refer to the block diagram of a typical op-amp shown in Figure 1-3. We model the op-amp as a system with a single pole roll-off having a transfer function of $a(s) = \frac{a_o}{\frac{s}{p_1}+1}$, where a_o is the open-loop DC gain, and p_1 is the single pole location. f is the feedback factor of the closed-loop configuration. For the closed-loop configuration in Figure 1-4, $f = \frac{R_1}{R_1+R_2}$.

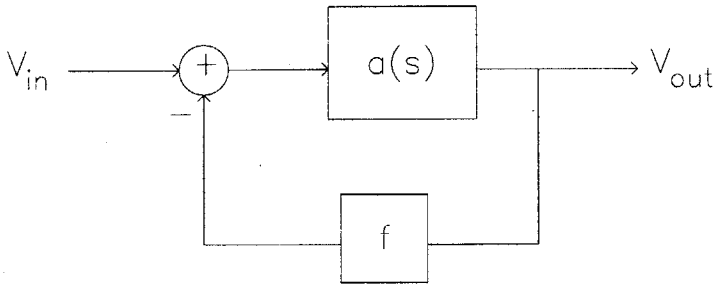


Figure 1-3: Block diagram of a typical op-amp.

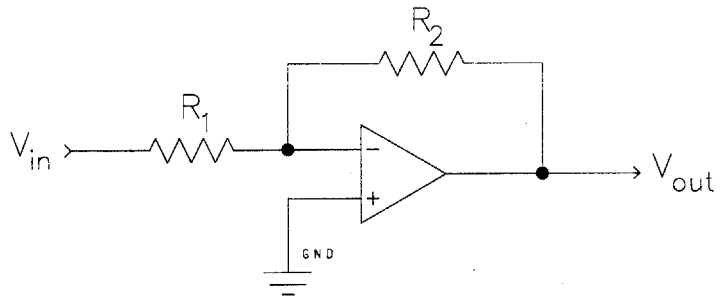
The gyroscope system requires that the op-amp be configured for differential closed-loop gains from 2 to 20. With a closed-loop gain of 20 ($R_2 = 20k$ and $R_1 = 1k$, equivalently a feedback factor of $\frac{1}{21}$), the crossover frequency of the open-loop gain needs to be increased by a factor of 21 (one over the feedback factor) in order to have less then 1° of static phase shift at a signal frequency of 25kHz. Therefore, the crossover frequency of the op-amp must be increased from the previous figure of 1.5MHz to 31.5MHz. This is illustrated in Figure 1-5. To maintain good stability of the gain amplifier, we require that the loop gain phase margin (phase at the open-loop unity-gain frequency) be greater than 45°.

Output Swing and Load Capacitance

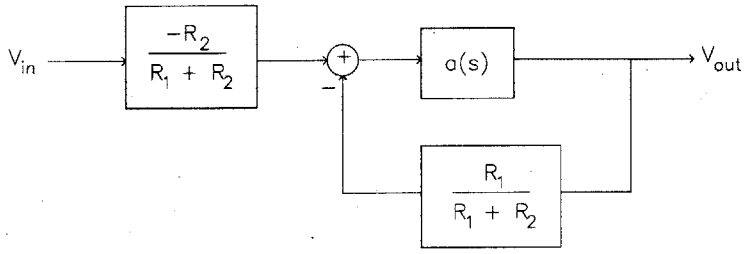
The output of the gain amplifier is AC coupled to drive a $\Sigma - \Delta$ converter, which digitizes all the sense channel signals. The input range of the $\Sigma - \Delta$ converter (5Vpp differential) sets the output swing requirement of the gain amplifier. Similarly, the input capacitance of the $\Sigma - \Delta$ converter ($\leq$ 10pF) sets the maximum load capacitance that the gain amplifier must drive.

Noise

The total input referred noise of the gain amplifier must be $< 35\text{nV}/\sqrt{(Hz)}$ at 8kHz so that the noise of the amplifier does not limit the minimum resolution of the gyroscope input signal.



(a) Single ended op-amp with resistive feedback.



(b) Block diagram of the single ended op-amp with resistive feedback.

Figure 1-4: Block diagram of an inverting amplifier.

Performance Requirements Summary

Table 1.3 lists the performance requirements of the gain amplifier system.

1.2.4 Thesis Outline

The remainder of the thesis is organized as follows:

Chapter 2 describes the design of the op-amp and the motivations for the design decisions made. Chapter 3 describes the capacitive feedback network and explains why a DC stabilization network is necessary. Chapter 4 describes the design of the DC stabilization network. Chapter 5 gives the simulation results of the gain amplifier system. Chapter 6 summarizes the thesis and discusses possible future improvements. The appendix shows final circuit schematics and the configurations used to run simulations.

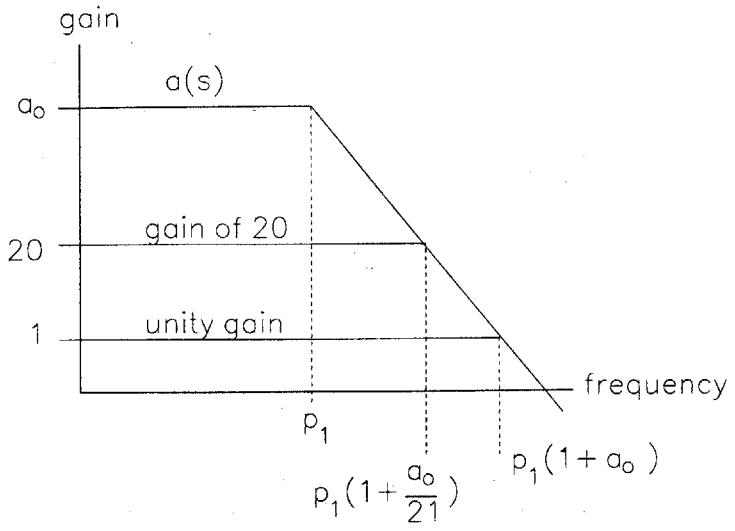


Figure 1-5: Magnitude plot of various closed-loop gains.

Power supply	5V
Load	10pF
Signal static phase shift	$< 1°$
Signal dynamic phase shift	$< 0.5°$
Total Harmonic Distortion (THD)	60dB for 4Vpp differential output swing at 25kHz
Input Referred Noise	$< 35\text{nV}/\sqrt{(Hz)}$ at 8kHz
PSRR	> 60dB at 25kHz
CMRR	> 60dB at 25kHz
Loop gain phase margin	45°

Table 1.3: Performance requirements of the gain amplifier system

Chapter 2

Op-Amp Topology

A single stage fully differential folded-cascode op-amp is proposed in this chapter to be used in place of the two single-ended gain amplifiers seen in Figure 1-1. Refer to Section 1.2.3 for why a fully differential topology was chosen. Since the op-amp only has to drive a capacitive load, a single stage design is proposed primarily for simplicity and ease of compensation. The main limitation of the single stage design is its small output swing. However, the output swing requirement (refer to Section 1.2.3) is within the capability of some single stage topologies.

A folded-cascode is chosen over its telescopic counterpart primarily because the folded-cascode has increased output swing. It can swing within two $V_{DS,SAT}$ of both rails, while the telescopic can swing within two $V_{DS,SAT}$ of one rail, but only three $V_{DS,SAT}$ of the other rail. An added advantage of the folded-cascode is increased common mode input range. By folding the input differential pair, this architecture has decoupled input swing from output swing.

2.1 Folded-Cascode Architecture

The basic fully differential folded-cascode op-amp is shown in Figure 2-1. Transistors M_1 and M_2 form the input differential pair. M_{12} forms a tail current source to set the current through the differential pair. M_5 and M_6 form a common-gate stage to cascode the differential pair. Current through M_5 and M_6 is set by M_7-M_{10}. M_3

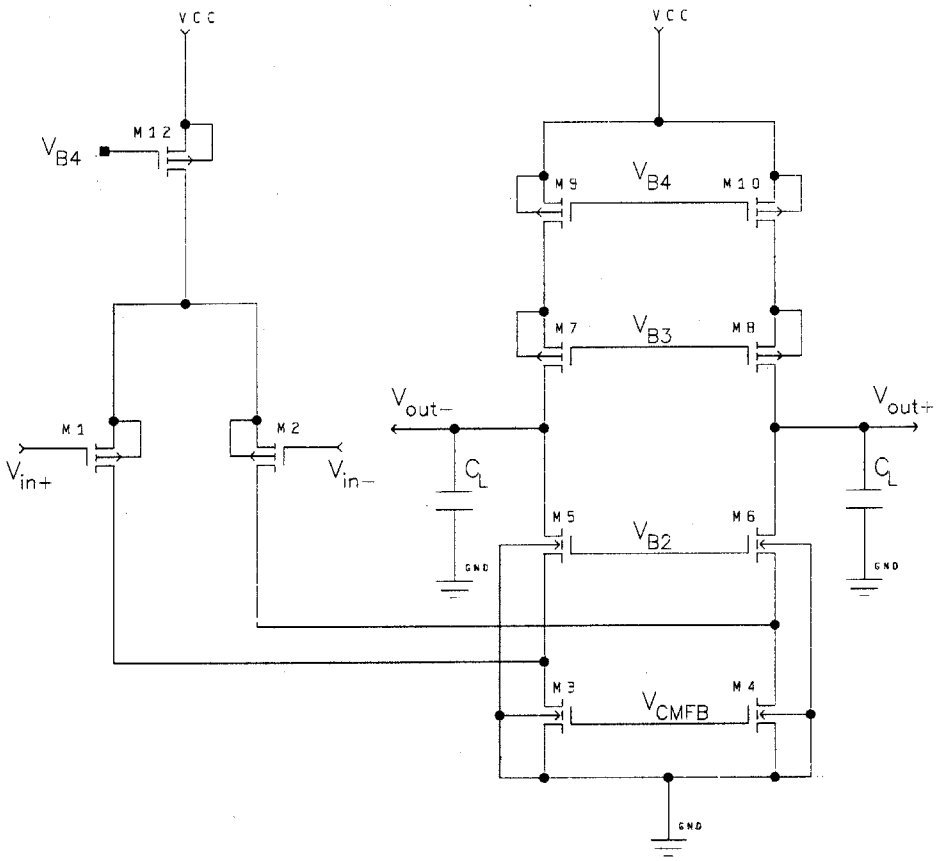


Figure 2-1: A fully-differential folded-cascode op-amp

and M_4 are the current source loads; the drain currents of these transistors are split between the input differential pair and cascode stages.

2.1.1 DC Small Signal Gain

A two-port model of the amplifier is shown in Figure 2-2. The DC gain of this system is $a_{vd} = G_M R_o$.

G_M is the short-circuit transconductance, given by $\frac{i_{sc}}{v_{id}}$, where i_{sc} is the output current when the output is shorted to ground. With the output shorted to ground, there is no current gain across M_5, and $i_{sc} = g_{m1} v_{id}$, so $G_M = g_{m1}$.

R_o is the output impedance of the folded-cascode op-amp and is a parallel combination of the impedances looking into the drains of M_5 and M_7 (where $\beta_x = g_{mx} r_{ox}$ in this and all subsequent equations):

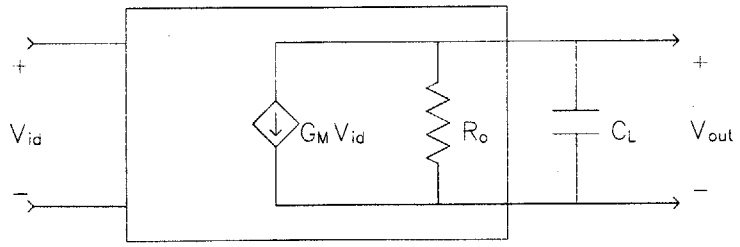


Figure 2-2: A two-port model of the fully-differential folded-cascode.

$$R_o = R_{o,up}//R_{o,down} = (\beta_7 r_{o9})//(\beta_5(r_{o1}//r_{o3})) \tag{2.1}$$

Therefore, the DC small signal gain of the system is:

$$a_{vd} = G_M R_o = g_{m1}((\beta_7 r_{o9})//(\beta_5(r_{o1}//r_{o3}))) \tag{2.2}$$

2.1.2 Frequency Response

Nodes of high resistance connected to a capacitive or inductive load have the most significant impact on a system's frequency response. In the circuit of Figure 2-1, the node with the largest impedance appears at the output and gives the dominant pole p_1 of the system. At the output, we have the parallel combination of the output resistance R_o and the load capacitance C_L seen in Figure 2-2.

$$a_{vd} = \frac{g_{m1} R_o}{sR_oC_L + 1} \tag{2.3}$$

$$p_1 = -\frac{1}{R_oC_L} = -\frac{1}{s((\beta_7 r_{o9})//(\beta_5(r_{o1}//r_{o3})))C_L} \tag{2.4}$$

The lowest frequency non-dominant pole is due to parasitic capacitances (the sum of the parasitics will be given by C_p) at the sources of M_5 and M_6 [8]. C_p is large (typically on the order of .1pF) because of the following reasons [8]:

- There are a large number of devices connected at the sources of M_5 and M_6.

- M_1 and M_2 are sized to have a large $\frac{W}{L}$ ratio for high g_m and low noise.
- M_3 and M_4 are sized to have a large $\frac{W}{L}$ ratio for a low $V_{DS,SAT}$ drop.

These parasitics create a non-dominant pole located at:

$$p_2 = -\frac{g_{m3}}{C_p} \tag{2.5}$$

where g_{m3} is the transconductance of M_3.

Assuming that the two poles are real and widely separated (which is a valid assumption because $C_L > C_p$ and $R_o >> \frac{1}{g_{m3}}$), then at the unity gain frequency, the gain of the op-amp can be approximated by a single pole roll-off:

$$a_{vd} = \frac{g_{m1}R_{out}}{sR_{out}C_L + 1} \approx \frac{g_{m1}}{sC_L} \tag{2.6}$$

This results in a unity gain frequency at $w_t = \frac{g_{m1}}{C_L}$.

2.1.3 Alternative calculations

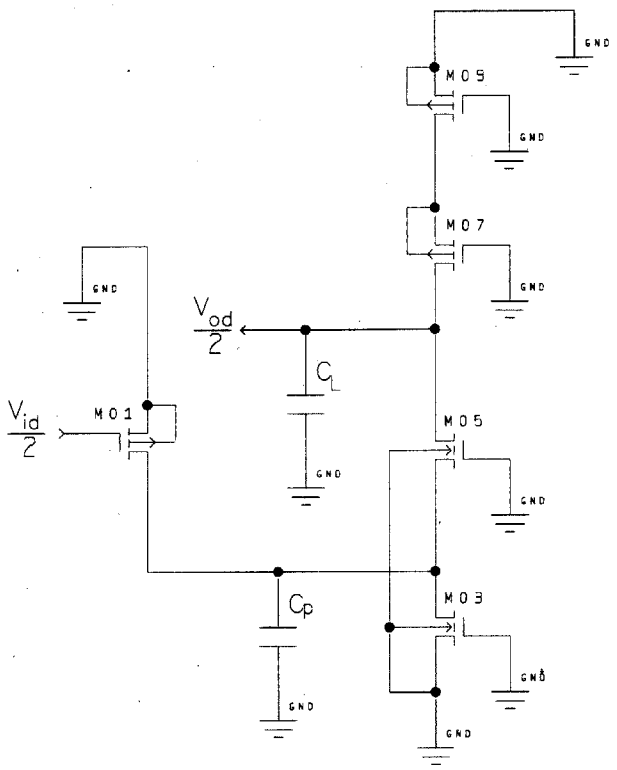
The results of Section 2.1.2 can also be derived algebraically, without the aid of conceptual insight by analyzing the differential half circuit in Figure 2-3(a) and the corresponding small signal model in Figure 2-3(b). If we assume that $g_m r_o >> 1$ and that the output impedance looking up into the drain of M_7 is very large, then:

$$a_{vd} = \frac{-g_{m1}r_{o3}\beta_5}{1 + sr_{o3}\beta_5 C_L + s^2 r_{o3}r_{o5}C_p C_L} \tag{2.7}$$

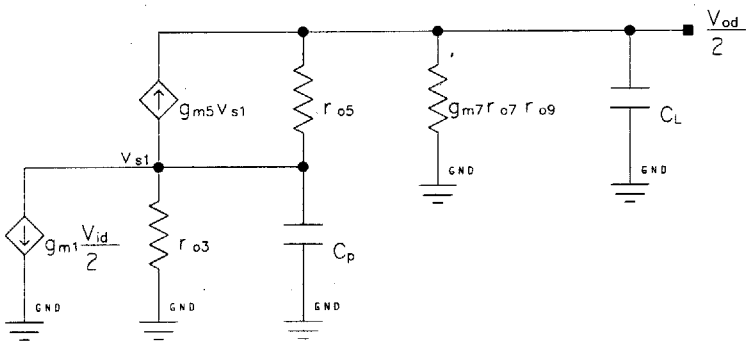
For this two pole transfer function, if we assume that the poles are real and widely separated, the polynomial can be approximated as:

$$P(s) = (1 - \frac{s}{p_1})(1 - \frac{s}{p_2}) = 1 - s(\frac{1}{p_1} + \frac{1}{p_2}) + \frac{s^2}{p_1 p_2} \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \tag{2.8}$$

By matching coefficients, $p_1 = -\frac{1}{R_o C_L}$ and $p_2 = -\frac{g_{m3}}{C_p}$, which are the same results as we found in Section 2.1.2.



(a) Differential half circuit.



(b) Small signal model of the differential half circuit.

Figure 2-3: The op-amp half circuit and its small signal model equivalent.

2.1.4 Noise [9, 4, 6]

Because the gain amplifier is near the front end of the readout electronics, we must deal with noise fundamental to the circuit that is due to the discrete nature of charged particles. This noise level can be reduced through proper circuit design. There are three primary types of noise: (1) shot, (2) thermal, and (3) flicker. Since noise is random by nature, it is often expressed in root mean squared (RMS) values to indicate normalized noise power. We will begin by reviewing the three primary types of noise, and see how they are manifested in the folded-cascode op-amp.

Shot Noise

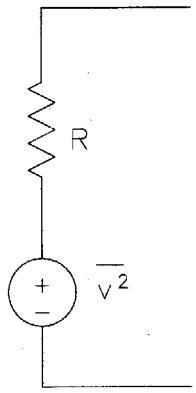
Shot noise is present wherever there is direct current flow. Current, which appears to be continuous and constant, is in reality composed of many discrete and random events. Shot noise is caused by these events. An example of shot noise is a carrier jumping the potential barrier between the p-type and n-type regions of a p-n junction. If the current is composed of a series of discrete and random events, we denote the average DC current by I_D, the bandwidth of the circuit by Δf, and the RMS current noise as [4]:

$$\overline{i^2} = 2qI_D\Delta f \tag{2.9}$$

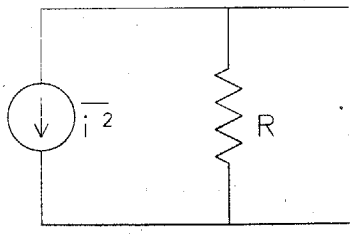
From this equation, we can see that the spectral density of shot noise, $\frac{\overline{i^2}}{\Delta f}$, is constant. Noise with a spectral density independent of frequency is also known as white noise.

Thermal Noise

Thermal noise is due to the random thermal motion of electrons in any conductor. Since electron thermal velocities are higher than electron drift velocities (the mechanism by which current is produced), thermal noise is independent of current. As its name indicates, thermal noise is proportional to temperature T ($^\circ K$).



(a) Voltage source equivalent of thermal noise.



(b) Current source equivalent of thermal noise.

Figure 2-4: Circuit Models for Thermal Noise

The voltage source and current source equivalent of thermal noise through a resistor is shown in Figures 2-4(a) and 2-4(b), respectively.

$$\overline{v^2} = 4kTR\Delta f \tag{2.10}$$

$$\overline{i^2} = \frac{4kT\Delta f}{R} \tag{2.11}$$

The spectral density of thermal noise is also white.

Flicker Noise

Flicker noise is found in all active devices and is always associated with a flow of direct current. It is generally caused by traps in a material which capture and emit carriers in a random fashion. Because MOSFETs conduct current right below the gate where the gate oxide contains many traps, flicker noise in CMOS devices can be very large. From empirical data, flicker noise can be modeled by:

$$\overline{i^2} = \frac{K_1 I^a \Delta f}{f^b} \tag{2.12}$$

Where I is the DC current, K_1 is a device-dependent constant, a is a constant from 0.5 to 2, and b is a constant with a value of approximately 1.

Flicker noise is also known as $\frac{1}{f}$ noise because the spectral density curve is approximated by the function $\frac{1}{f}$.

Noise Model for a MOSFET[9]

Now that we have identified all the intrinsic noise types in circuit components, we will calculate the equivalent voltage noise for a MOSFET so that we can find the noise of the folded-cascode op-amp.

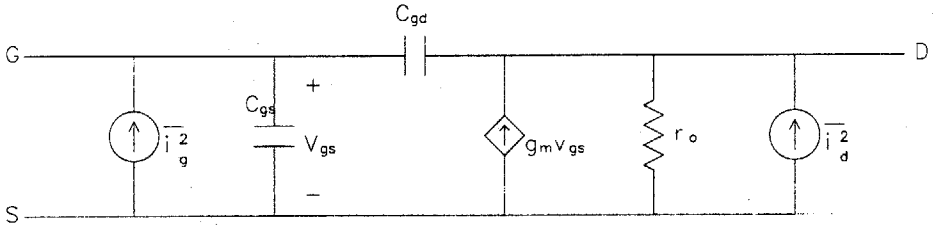


Figure 2-5: Small signal noise model for a MOSFET.

Figure 2-5 shows the small signal noise model for a MOSFET. In strong inversion, the channel is resistive, so a MOSFET exhibits thermal noise. The effective channel resistance for the thermal noise calculation is:

$$R_{channel} = \frac{L}{\frac{2}{3}\mu C_{ox}(V_{GS} - V_T)} = \frac{3g_m}{2} \tag{2.13}$$

In a MOSFET, shot noise is due to gate leakage current (in Equation 2.9, I_D is the gate current), which is typically negligible for non-high-frequency circuits (typically less than $10^{-15}A$[4, p.759]). Neglecting shot noise, the total current noise in a MOSFET is given by the sum of its thermal and flicker noise:

$$\overline{i_d^2} = 4kT\frac{2}{3}g_m\Delta f + \frac{KI_D^a\Delta f}{f} \tag{2.14}$$

An asymptotic approximation to the MOSFET noise spectral density is shown in

Figure 2-6. f_{knee} is the knee frequency up to which flicker noise is dominant, and above which thermal noise is dominant. By comparing Equations 2.11 and 2.12, we can solve for f_{knee}:

$$f_{knee} = \frac{K_1 I^a R}{2kT} \tag{2.15}$$

where R represents the channel resistance.

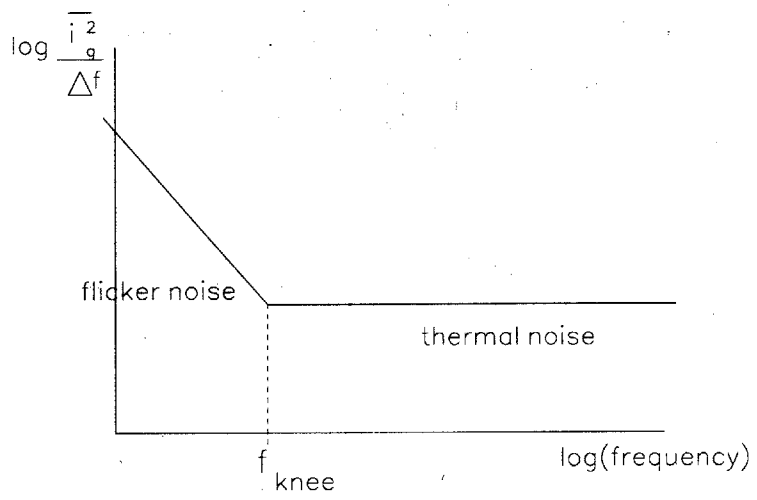


Figure 2-6: Noise spectral density for a MOSFET.

The equivalent voltage noise for a MOSFET can be found by dividing the current noise in Equation 2.14 by g_m^2.

$$\overline{v_{eq}^2} = \frac{\overline{i_d^2}}{g_m^2} = \frac{8kT}{3g_m}\Delta f + K\frac{I_D^a}{g_m^2 f}\Delta f = \frac{8kT}{3g_m}\Delta f + \frac{K_f \Delta f}{WLC_{ox}^2 f} \tag{2.16}$$

The third equality arises from empirical data [9] that shows that $K\frac{I_D^a}{g_m^2} = \frac{K_f}{WLC_{ox}^2}$ in both strong and weak inversion. In Equations 2.14 and 2.16, the first term is the thermal noise component, and the second term is the flicker noise component.

2.1.5 Noise in the Folded-Cascode Op-Amp

The first step in calculating the noise of the folded-cascode topology is to sum the noise currents at the output. Assume that the noise from M_{12} is canceled by circuit

symmetry and input device matching. We also know that cascode transistors contribute negligible noise because they are source degenerated and have a small effective transconductance (see Section 2.3.1). By symmetry, the output noise current is:

$$i_o^2 = 2(g_{m1}^2 v_{n1}^2 + g_{m3}^2 v_{n3}^2 + g_{m9}^2 v_{n9}^2) \tag{2.17}$$

Referring this back to the input gives an input referred noise of:

$$v_{ni}^2 = 2(v_{n1}^2 + \frac{g_{m3}^2}{g_{m1}^2} v_{n3}^2 + \frac{g_{m9}^2}{g_{m1}^2} v_{n9}^2) \tag{2.18}$$

Where $g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$.

Thermal Noise

Plugging in the thermal noise of a MOSFET from Equation 2.16 into Equation 2.18 gives the thermal noise of the folded-cascode op-amp:

$$\frac{v_{I,TH}^2}{\Delta f} = \frac{16kT}{3\sqrt{2\mu_p C_{ox} \frac{W_1}{L_1} I_{D1}}}(1 + \sqrt{\frac{\mu_n \frac{W_3}{L_3}}{\mu_p \frac{W_1}{L_1}}} + \sqrt{\frac{\frac{W_9}{L_9}}{\frac{W_1}{L_1}}}) \tag{2.19}$$

Flicker Noise

Likewise, plugging in the flicker noise component from 2.16 into Equation 2.18 gives the flicker noise of the folded-cascode op-amp:

$$\frac{v_{I,\frac{1}{F}}^2}{\Delta f} = \frac{2K_p}{W_1 L_1 C_{ox}^2 f} + \frac{\mu_p}{\mu_n \frac{W_1}{L_1}} \frac{4K_n}{L_3^2 C_{ox}^2 f} + \frac{1}{\frac{W_1}{L_1}} \frac{2K_p}{L_9^2 C_{ox}^2 f} \tag{2.20}$$

Folded-cascode Noise Summary

All MOSFET widths, lengths, and currents are parameters that can be set to optimize the circuit noise performance. Since our signals of interest span a frequency range of 8kHz to 25kHz, we are most interested in the noise at 8kHz because at higher frequencies, the effects of flicker noise are reduced. Minimizing thermal noise and flicker noise are not exclusive goals. Both can be accomplished by sizing MOSFET

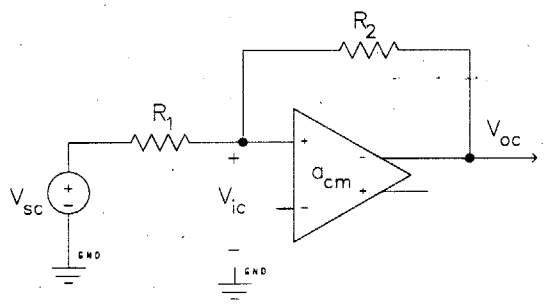
parameters appropriately, but because thermal noise dominates here, we focus on reducing it first. To minimize thermal noise, we desire:

- Large current through the input differential pair
- Large $\frac{W}{L}$ ratio for the input differential pair
- Small $\frac{W}{L}$ ratio for current sources M_3, M_4, M_9, and M_{10}.

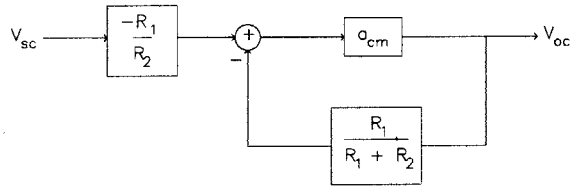
2.2 Common Mode Feedback

One downside to using a fully differential topology is the need for a common mode feedback (CMFB) circuit. This section will discuss why CMFB is needed and analyze the particular topology chosen for use in our application.

2.2.1 Why is Common Mode Feedback Necessary?



(a) Common mode half circuit.



(b) Block diagram of the common mode half circuit.

Figure 2-7: half circuit model of the CMFB circuit.

Let us look at the common mode half circuit and corresponding block diagram shown in Figures 2-7(a) and 2-7(b), respectively. Ideally, we want the common mode

gain a_{cm} to be zero so that our fully differential amplifier rejects all common mode signals. Recall that the loop gain of a block diagram is the product of all the blocks through the feed-forward path and around the feedback path. In this example, the loop gain of the system is $\frac{R_1}{R_1+R_2}a_{cm}$. A small common mode gain causes the loop gain of the common mode half circuit to be small so that the inputs of the op-amp do not have much control over the common mode output. This allows the common mode output voltage to swing uncontrolled and may decrease output swing and/or cause transistors to operate outside of the desired operating regions. Common mode feedback is necessary to keep the output common mode tightly controlled.

A more concrete way to see the need for CMFB is to take a look at Figure 2-1. The current through the tail current source M_{12} needs to be equal to the sum of the currents through M_1 and M_2. This condition is met automatically by KCL. Since the gain from the gates of M_3 and M_4 to the output is high (see Equation 2.24), we can use the gates to adjust the currents through M_3 and M_4 in order to control the common mode output voltage.

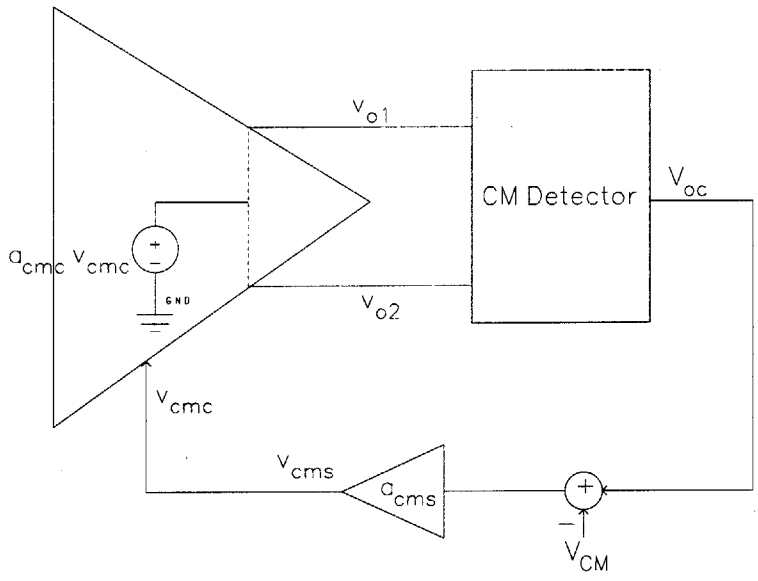


Figure 2-8: Block diagram of a typical CMFB network ([4], 818).

The typical CMFB network is shown in block diagram form in Figure 2-8. Connected to the outputs of the op-amp is a common mode detector block that detects

the CM output by averaging the output voltages. The difference between the detected CM and the desired CM is amplified, and then fed back to the op-amp.

The figure of merit that we want to look at with the CMFB loop is its gain, $a_{cmfb} = \frac{v_{cms}}{v_{cmc}}$. This gain can be further broken up into a common mode control component, $a_{cmc} = \frac{v_{oc}}{v_{cmc}}$, which is calculated with a zero common mode input, and a common mode sense component, $a_{cms} = \frac{v_{vms}}{v_{oc}}$, which is calculated with the CMFB loop disconnected from the op-amp. As explained earlier, we would like a large gain in the CMFB loop to keep the output tightly regulated.

2.2.2 Continuous-Time common mode Feedback

Switched CMFB topologies have the advantages of being area efficient and not needing an additional amplifier. However, switched topologies also introduce switching transients, and the noise levels associated with switching are often not compatible with high performance applications. This project is designed with a continuous-time application in mind, so a continuous-time CMFB is employed.

CMFB using a Resistive Divider for CM Detection

A popular approach for realizing a continuous-time CMFB circuit is shown in Figure 2-9 [4, p.824]. Here, resistors R_s form the CM detector. The average of the op-amp outputs appears at node V_a. Source followers MD_1 and MD_4 are needed to buffer the output of the op-amp so that the R_s resistors do not load the op-amp outputs (remember the op-amp is designed to drive a capacitive load). Similarly, MCM_7 is used to level shift the desired common mode by the same amount that MD_1 and MD_4 level shift the output voltages. The main disadvantage of this topology is that it is difficult to stabilize because of the many nodes in the circuit. To achieve stability, capacitors are often placed across the sensing resistors, which increases chip area. Another problem is that the output swing of the op-amp is limited to levels that keep the source followers operating in the active region. These problems led us to choose another CMFB topology, described in the next section.

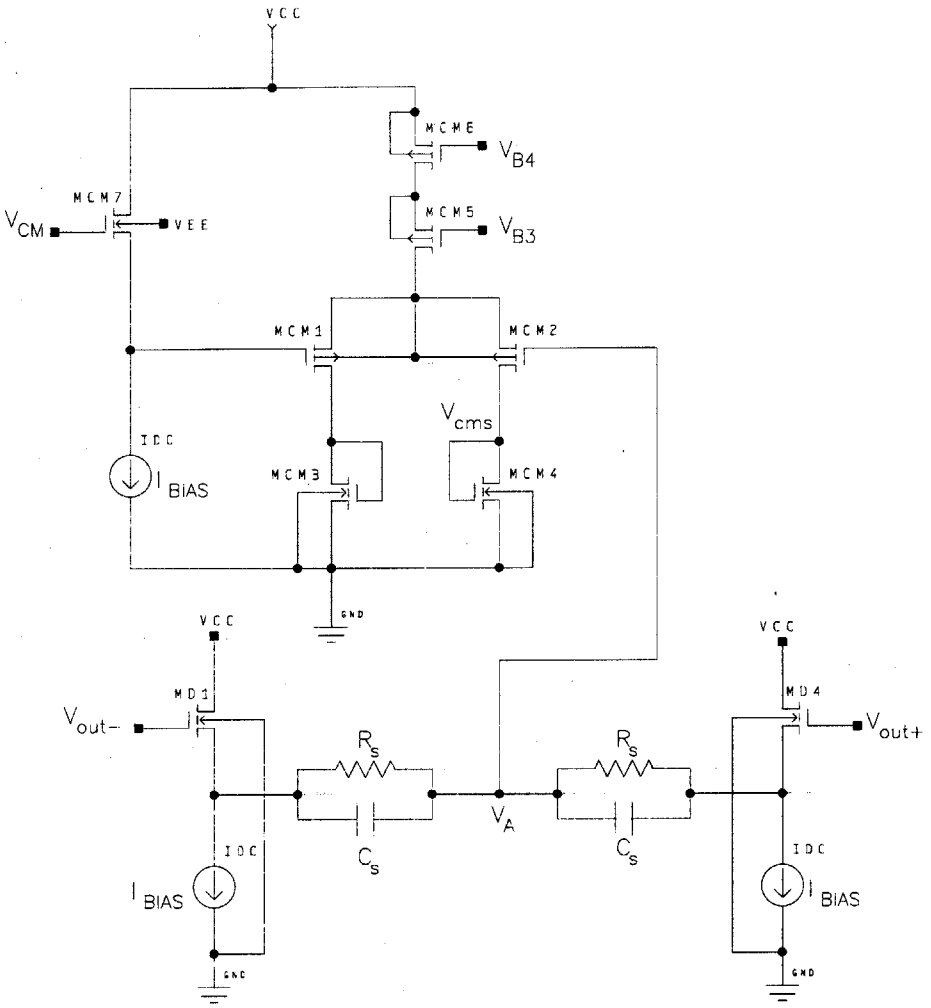


Figure 2-9: CMFB using a resistive divider and amplifier.

CMFB using Two Differential Pairs for CM Detection

Another possible continuous-time CMFB circuit is shown in figure 2-10 [4, p.828]. Here, transistors MCM_1 through MCM_4 form two differential pairs that function as the common mode detection network.

Figure 2-10 shows the CMFB amplifier. The folded-cascode op-amp is reproduced in Figure 2-11 as a reference to show the connections between the CMFB and the op-amp. The v_{cmc} and v_{cms} nodes are tied together. The CMFB circuit consists of two differential pairs. The CMFB loop includes the differential pairs in the CMFB circuit as well as a portion of the main op-amp (the CMFB signal path goes through

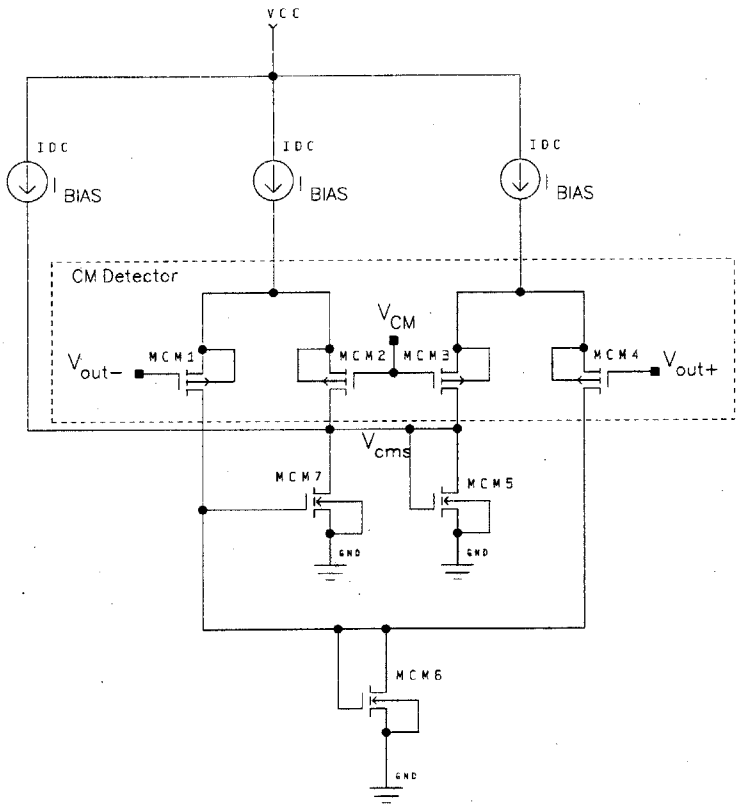


Figure 2-10: CMFB schematic.

transistors $M_3 - M_6$ in the main op-amp). Ignoring MCM_7 and its current source for now, each differential pair senses how far the positive or negative output has deviated from the desired common mode voltage and outputs a current proportional to this difference. The small-signal analysis below shows that the current fed back to the folded-cascode amplifier is a fraction of the difference between the average of the outputs and the desired common mode voltage. Note that I_{dx} corresponds to the current through device M_x.

$$I_{dCM2} = -\frac{I_{bias}}{2} - \frac{g_{mcm2}}{2}(V_{op} + V_{CM}) \tag{2.21}$$

$$I_{dCM3} = -\frac{I_{bias}}{2} - \frac{g_{mcm3}}{2}(V_{op} + V_{CM}) \tag{2.22}$$

(The factor of $\frac{1}{2}$ appears in the g_{mcm} term because the effective transconductance

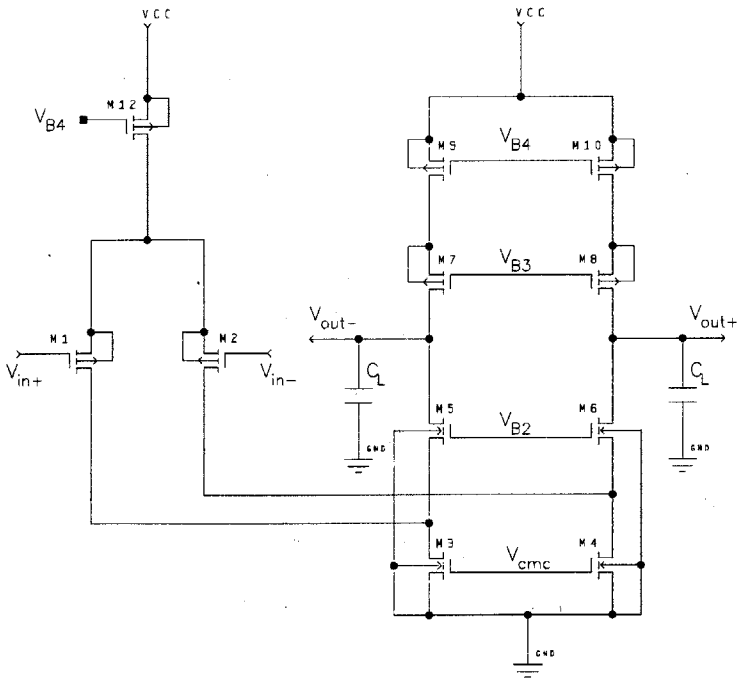


Figure 2-11: Folded-cascode schematic.

of a differential pair is $\frac{g_m}{2}$.)

$$I_{dCM5} = I_{dCM2} + I_{dCM3} = -I_{bias} - g_{mcm}(\frac{V_{op} + V_{on}}{2} - V_{CM}) \tag{2.23}$$

With devices MCM_1 through MCM_4 sized equally, $g_{mcm2} = g_{mcm3} = g_{mcm}$.

Analyzing the folded-cascode in Figure 2-11, the gain of the common mode-control (from the gate of M_3 to the output of the op-amp) is:

$$a_{cmc} = g_{m3}((\beta_7 r_{o9})//(\beta_5 r_{o3})) \tag{2.24}$$

Because this gain is derived from devices in the main op-amp, it remains the same regardless of the chosen CMFB topology. This gain is large enough so that the common mode sense gain from the gate of $MCM_{2,3}$ to the gate/drain of MCM_5 (a_{cms}) can be made to be small, which affords a larger bandwidth design. Without MCM_7 included, $a_{cms} = \frac{2g_{mcm}}{g_{mcm5}}$. In contrast, with MCM_7 included [6, p.289], a_{cms} becomes

$a_{cms} = \frac{2g_{mcm}(g_{mcm6}+g_{mcm7})}{g_{mcm5}g_{mcm6}}$, which is approximately a factor of 2 in gain improvement. Therefore the addition of MCM_7 will give better control of the common mode output with little added complexity. In both equations, g_{mcm} is defined as the transconductance of MCM_1, MCM_2, MCM_3, or MCM_4 (which are all designed to match by equal biasing and sizing).

The disadvantage of CMFB with two differential pairs is that the output swing of the op-amp is limited to the common mode differential input voltages that keep the differential pairs of the CMFB in the active region of operation. Writing KVL from the gate of MCM_1 to the gate of MCM_2, and defining the common mode input as $v_{id} = V_{out-} - V_{CM}$, we can calculate how much the output swing is limited by the CMFB circuit:

$$|v_{id}| \leq \sqrt{\frac{2I_{BIAS}}{\mu_p C_{ox}\frac{W}{L}}} \tag{2.25}$$

To minimize the limitation that the CMFB circuit has on the output swing, we can increase the bias current of the CMFB circuit, or decrease the $\frac{W}{L}$ ratio of MCM_1 through MCM_4. For our application, $I_{bias} = 200\mu A$, $\mu_p C_{ox} \approx 38\frac{\mu A}{V^2}$, and $\frac{W}{L} = \frac{52}{7}$, so we expect the input common mode range of the CMFB circuit to be: $|v_{id}| \leq 1.19V$.

Determining the Optimal common mode Voltage

The output swing of the op-amp is effected by both the op-amp output stage and the CMFB input stage. Referring to Figure 2-1 for device names, one output reaches its lowest limit ($V_{out,min}$) when transistors M_3 and M_5 or M_4 and M_6 exit saturation. So $V_{out,min} = 2V_{DS,SAT} = 500\text{mV}$, where $V_{DS,SAT}$ has been approximated as 250mV. The upper limit of one output ($V_{out,max}$) is reached when the input transistors of the CMFB exit saturation. MCM_{1-4} are operating in the active region when their source-to-gate voltage $V_{SG} > V_{tp}$. Plugging in $V_{SG} = VCC - V_{SD,SAT_{10}} - V_{out}$ (where $VCC = 5V$, $V_{SD,SAT}$=250mV, and $V_{tp} = 0.95V$) we find that $V_{out,max} = 3.8V$. To maximize the output swing, the common mode voltage should be halfway between $V_{out,max}$ and $V_{out,min}$, or at 2.15V. Because we estimated $V_{DS,SAT}$ for this calculation,

we can only expect for it to give us an approximate answer. In simulation, the actual optimal common mode voltage was found to be 2.25V.

Since $V_{out,max} = 3.8V$, and from Equation 2.25, we know that $|v_{id}| \leq 1.19V$, the CMFB circuit forces $V_{in,max}$ equal to $V_{out,max} - 2v_{id,max} = 1.06V$. Therefore, the actual predicted single-sided swing of the op-amp is $V_{out,max} - V_{in,max} = 2.74V$. The plot in Figure 2-23 shows the actual achieved output single-sided swing, which is $\pm 1.43V$ from the common mode. The total differential swing is $\pm 2.86V$, which meets our goal.

2.3 Gain-Enhancement through Active Cascoding

High open-loop gain is desirable in an op-amp because it affects the accuracy of the closed-loop network. Since our signal is important at frequencies between 8kHz and 25kHz, we want high open-loop gain at those frequencies. While a single stage folded-cascode amplifier is easily compensated (compensation is achieved by the output capacitance) and can have less noise and lower power than a multi-stage alternative, the DC open-loop gain is limited to $\approx$50dB. Depending on the placement of the dominant pole, the gain at 20kHz can be equal to or less than 50dB. A technique called active cascoding can be used to increase the open-loop gain of the op-amp without adding extra stages.

2.3.1 Regular Cascode

This section will begin by reminding the reader of the regular cascode topology, and expand upon it by analyzing the active cascode and applying it to the folded-cascode op-amp analyzed in Section 2.1.

Small-Signal Analysis of a Standard Cascode

A typical two-transistor cascode structure is shown in Figure 2-12. Assuming the output resistance of the current source I_{bias} is very large, the small-signal DC gain of the cascode is:

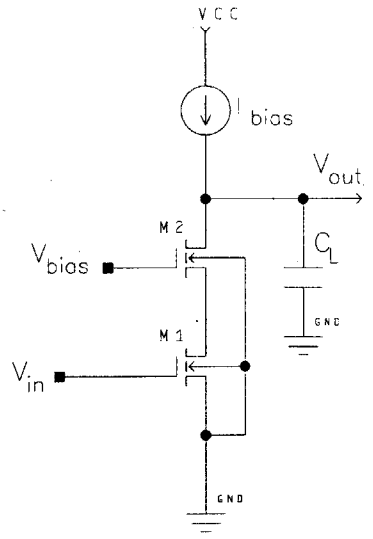


Figure 2-12: Cascode topology.

$$a_{vd} = \frac{v_{out}}{v_{in}} = g_{m1}R_{out} = g_{m1}g_{m2}r_{o1}r_{o2} = \beta_1\beta_2 \tag{2.26}$$

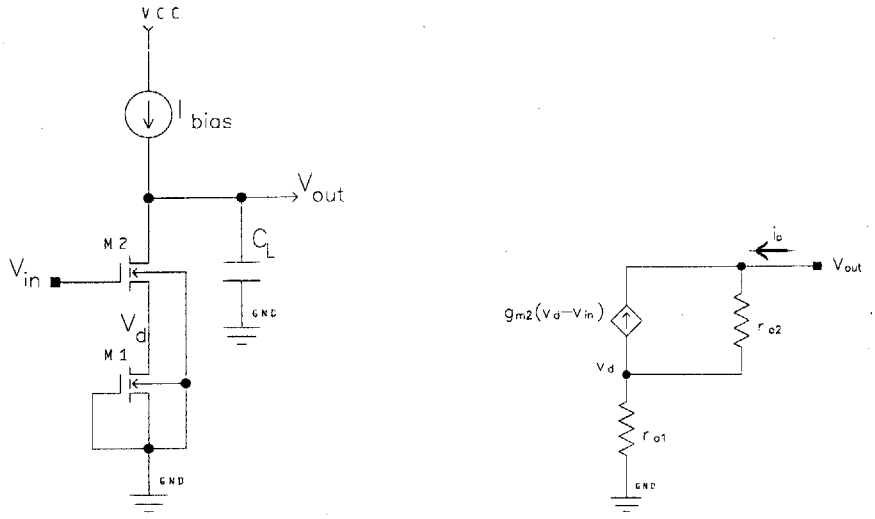
Note that cascoding increases the output impedance by the $g_m r_o$ of the cascoding transistor.

Noise of a Standard Cascode

Noise of the cascode circuit shown in Figure 2-12 is dominated by M_1. M_2 contributes negligible noise because the current noise from M_2 is proportional to its effective transconductance, G_{M2}, and its effective transconductance is small. Figure 2-13 shows the models that we use to find the effective transconductance of M_2. Intuitively, we can look at M_2 as being source degenerated by M_1. From analysis on the small-signal model in Figure 2-13(b):

$$G_{M2} = \frac{g_{m2}}{g_{m2}r_{o1} + 1} \tag{2.27}$$

Therefore, the only important contributer of noise in the cascode circuit comes from the noise of M_1, modeled as a noise source on its gate.



(a) M_2 Source degenerated by M_1.

(b) Small signal model.

Figure 2-13: Source degeneration

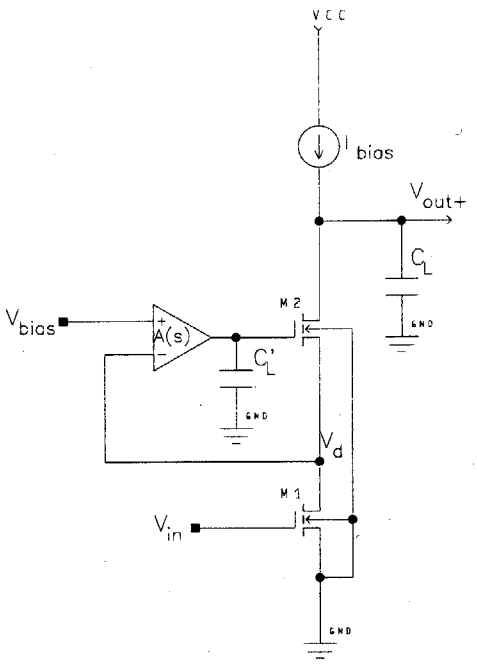
2.3.2 Basic Active Cascode Architecture

Active Cascode using an Op-Amp

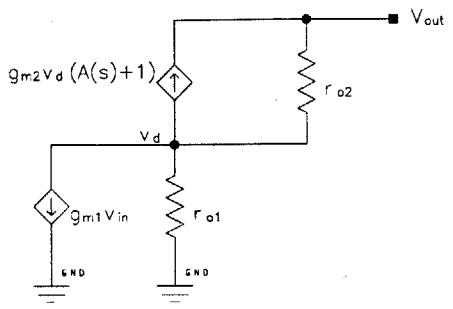
Without adding extra stages, the easiest way to increase the gain of a folded-cascode amplifier is to add another level of cascoding. However, this cuts into an already limited signal swing. To increase the op-amp gain without reducing output swing, we can use the active cascode technique (also known as a regulated cascode) shown in Figure 2-14(a).

The amplifier with an open-loop gain of A(s) is called a gain enhancement amplifier and increases the gain of the cascode circuit by increasing its output impedance. The gain enhancement amplifier sets the gate voltage of M_2 such that the drain-to-source voltage across M_1 is held relatively constant despite changes in drain current, resulting in a large output impedance. An analysis of the small signal model of the active cascode circuit, shown in Figure 2-14(b), shows that the active cascode increases the output impedance of the regular cascode by a factor of 1+A(s), where A(s) is defined in Equation 2.29:

$$R_{out} = \beta_2 r_{o1}(1 + A(s)) = \frac{\beta_2 r_{o1}(s\tau_1 + A_o + 1)}{s\tau_1 + 1} \tag{2.28}$$



(a) Active cascode topology.



(b) Small signal model of the active cascode.

Figure 2-14: Active cascode and its equivalent small signal model.

The open-loop gain of the gain enhancement amplifier A(s) is defined as:

$$A(s) = \frac{A_o}{s\tau_1 + 1} \tag{2.29}$$

In Equation 2.29, A_o is the open-loop DC gain of the active cascode amplifier, and $\frac{1}{\tau_1}$ is the location of the dominant pole. The increased output impedance can be used to calculate the gain of the circuit:

$$a_{vd} = \frac{v_{out}}{v_{in}} = -g_{m1}(R_{out}//\frac{1}{sC_L}) \approx -\frac{\beta_1\beta_2(A_o+1)(s\frac{\tau_1}{A_o+1}+1)}{1+s\beta_2 r_{o1}C_L(A_o+1)+s^2\beta_2 r_{o1}C_L\tau_1} \tag{2.30}$$

The second equality in Equation 2.30 arises from plugging in the result from Equation 2.28 and assuming that $\tau_1 << \beta_2 r_{o1} C_L(A_o+1)$.

The transfer function for the active cascode circuit in Equation 2.30 shows that there is a zero at $z_1 = -\frac{A_o+1}{\tau_1}$, which is also the unity gain frequency of amplifier A. Using the approximations from Equation 2.8, we have a dominant pole at $p_1 = -\frac{1}{\beta_2 r_{o1} C_L A_o}$ and a second pole at $p_2 = -\frac{A_o+1}{\tau_1}$. Notice that zero z_1 and pole p_2 appear

to cancel. However, remember this is only true if the approximation that we made earlier holds: $\tau_1 << \beta_2 r_{o1} C_L (A_o + 1)$. τ_1 is typically given by $R'_{out} C'_L$ where R'_{out} is the output resistance of the gain enhancement amplifier and C'_L is its load capacitance. Experimentation shows that sufficient cancellation is achieved for $C'_L = C_L = 10pF$. An added benefit of a load capacitance placed at the output of the gain enhancement amplifier is that this capacitor also serves to compensate the active cascode feedback loop.

The active cascode technique is limited by the bandwidth of the gain enhancement amplifier. This limitation reduces the usefulness of the technique for high-frequency applications. Fortunately, at our 8kHz to 25kHz frequency of interest, the active cascode technique does provide more gain boost than a standard cascode. At DC, the active cascode provides a much more substantial gain boost.

Single Transistor Gain Enhancement

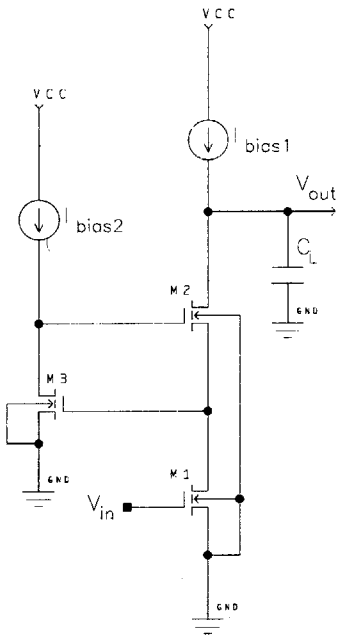


Figure 2-15: Single transistor active cascoding.

The gain enhancement amplifier can be as simple as just a single transistor, as

illustrated in Figure 2-15. Although this configuration is more simple than a multi-transistor gain enhancement amplifier, its major limitation is that it significantly reduces signal swing. The reason is because M_3 forces the drain-to-source voltage across M_1 to be much larger (by one threshold voltage drop) than the minimum necessary to keep it in saturation. More specifically, $V_{DS1} = V_{GS3} = V_{DS,SAT} + V_{tn}$, when M_3 is used as shown in Figure 2-15. In contrast, the minimum V_{DS} to keep M_1 saturated is $V_{DS,SAT}$.

Noise Contribution of the Active Cascode

From the active cascode circuit in Figure 2-14(a), we see that the output noise of the gain enhancement amplifier feeds into the gate of cascode transistor M_2. However, cascode transistors contribute negligible noise to the overall circuit because of their small effective transconductances. (Refer to Section 2.3.1 for this calculation.) As a result, the gain enhancement amplifier of the active cascode also contributes minimal noise to the overall circuit.

2.3.3 Implementation of the Active Cascode Technique

As shown in the previous section, active cascoding can be used to increase the gain of an overall system by a factor equal to the open-loop gain of the added amplifier. (The added amplifier is also known as a gain enhancement amplifier). Figure 2-16 gives an example of a fully differential folded-cascode circuit to which this technique is applied. Amplifiers are needed on both the NMOS and PMOS cascodes so that effort of increasing the gain of one side is not wasted by the lower impedance of the non-gain boosting side.

One disadvantage of active cascoding is that it requires four additional amplifiers. This adds complexity as well as increases power and area usage. Two fully differential gain enhancement amplifiers are proposed in [10] to replace the four single ended gain enhancement amplifiers. Shown in Figure 2-17, this method takes advantage of the unity gain feedback configuration of the gain enhancement amplifiers in the active

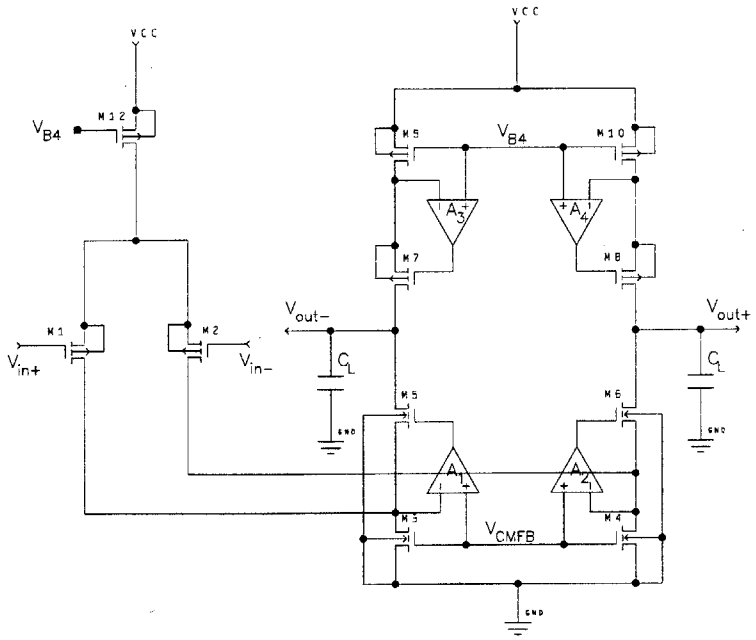


Figure 2-16: Four single-ended amplifiers used for Active cascoding in a fully-differential folded-cascode.

cascodes to achieve common mode feedback of the gain enhancement amplifier with a single transistor. The unity gain feedback configuration allows us to set the output common mode level simply by setting the input common mode level. Figure 2-18 shows schematics for amplifiers A_1 and A_2. In each amplifier, transistor M_{CM} accomplishes the common mode feedback by setting the input common mode level. This implementation of a fully differential gain enhancement amplifier is not much more complex than its single ended counterpart, and also represents a savings in power and area.

The A_1 amplifier has a PMOS input stage (as shown in Figure 2-18(a)) to maximize the output swing of the folded-cascode. For high output swing, we choose $V_{DS3,4}$ to be a little larger than $V_{DS,SAT}$. Therefore, A_1 must operate with a low common mode input range. From Figure 2-17, the voltage from ground to the output of A_1 is $V_{DS3,4} + V_{DS5,6} + V_{tn}$. In order to keep $V_{DS3,4}$ around $V_{DS,SAT}$, the gate-to-drain voltage of the PMOS input transistors of A_1 is $V_{DS5,6} + V_{tn}$ and these input transistors operate in saturation only when $V_{tp} > V_{DS5,6} + V_{tn}$. A similar argument can be made

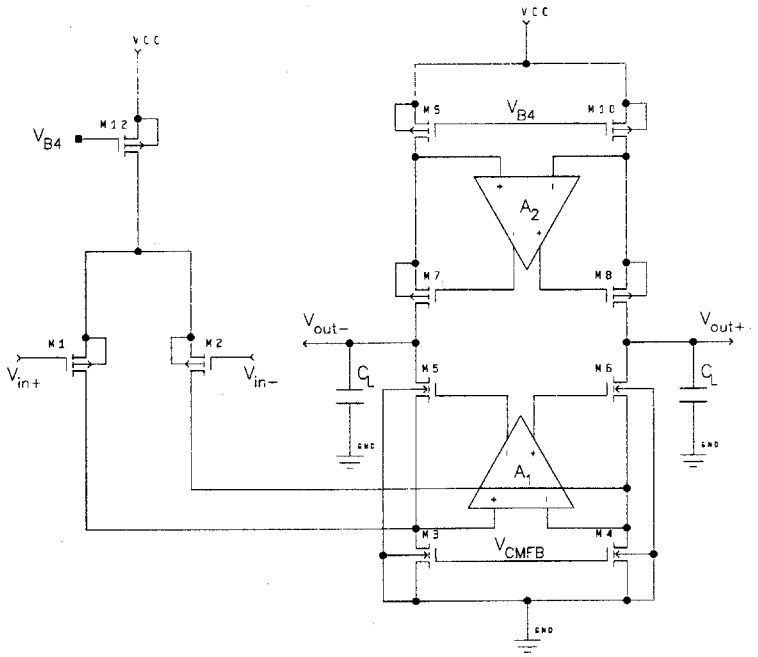
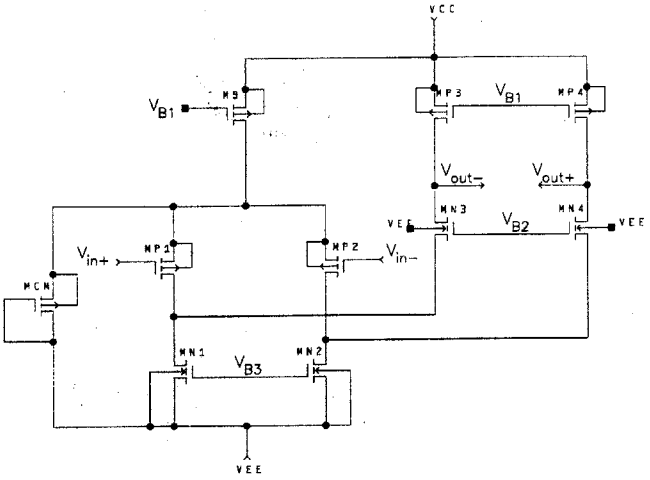


Figure 2-17: Two fully-differential amplifiers used for active cascoding in a fully-differential folded-cascode.

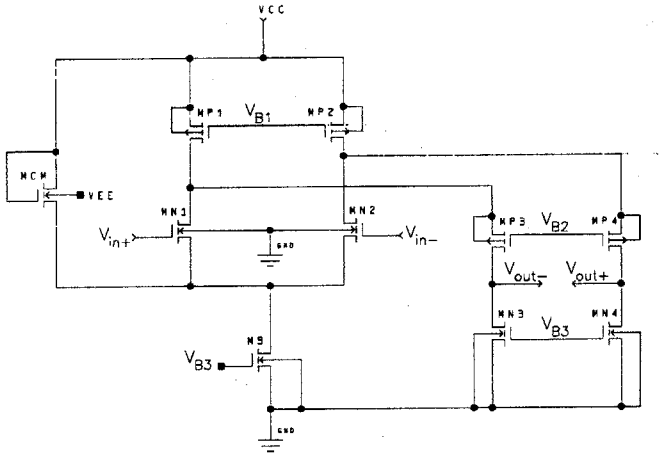
for why A_2 has an NMOS input stage.

2.4 Folded-Cascode Op-Amp Simulation Results

Important simulation results are summarized in table 2.4. All results are given fully differentially, except for results marked with an asterisk (*), which are for a single-ended readout. See Appendix A for output plots and the setup used to perform each simulation.



(a) Gain Enhancement Amplifier with PMOS input stage.



(b) Gain Enhancement Amplifier with NMOS input stage.

Figure 2-18: Fully Differential Gain Enhancement Amplifiers.

	Requirement	Achieved
Gain at 8kHz		75dB
Gain at 25kHz		65dB
Phase margin	$> 45°$	70°
Unity gain frequency	31.5MHz	42MHz
Output swing	5Vpp	5.72Vpp
Noise	$35\frac{nV}{\sqrt{Hz}}$	$19\frac{nV}{\sqrt{Hz}}$
PSRR+*	> 60dB at 25kHz	117dB at 25kHz
PSRR-*	> 60dB at 25kHz	103dB at 25kHz
CMRR*	> 60dB at 25kHz	107dB at 25kHz
CMFB Phase margin		70°

Table 2.1: Op-amp simulation results. Results are given fully differentially except for those marked with an asterisk (*), which are given as a single-ended readout.

2.4.1 AC Simulations

Open-Loop Response

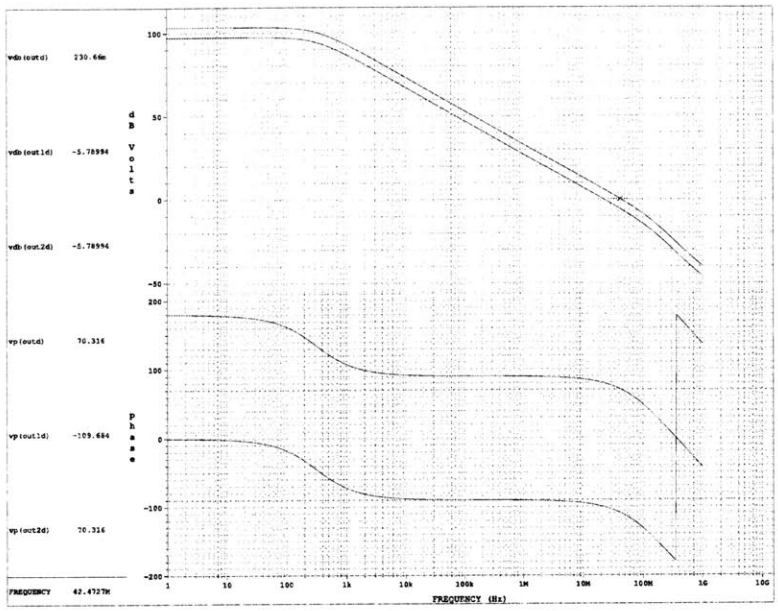


Figure 2-19: Bode plot of the op-amp in an open-loop configuration. The unity gain frequency is labeled on the plot.

Input Referred Noise

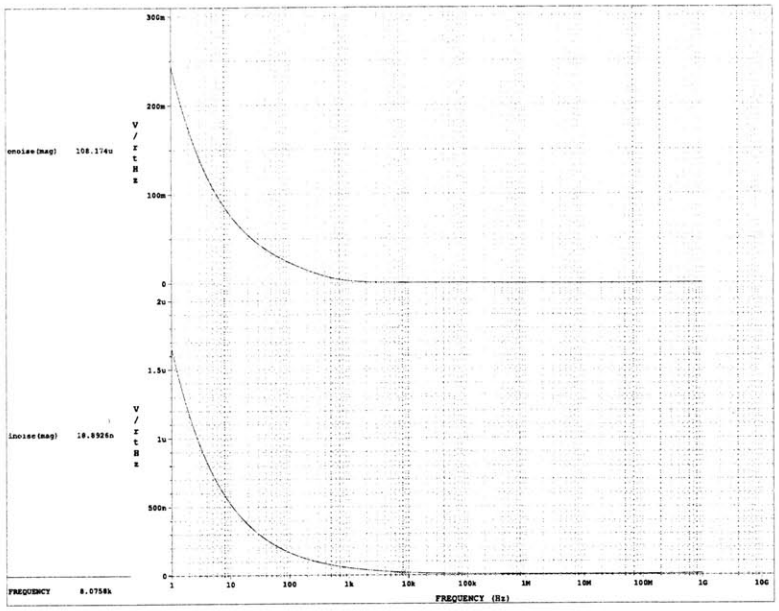


Figure 2-20: Output and input referred noise of the op-amp. The noise at 8kHz is labeled on the plot.

common mode Rejection Ratio

The common mode rejection ratio (CMRR) is a useful figure of merit for fully differential amplifiers because it gives the ratio between the differential gain and common mode gain of the amplifier. A large CMRR is desired so that common mode signals are suppressed.

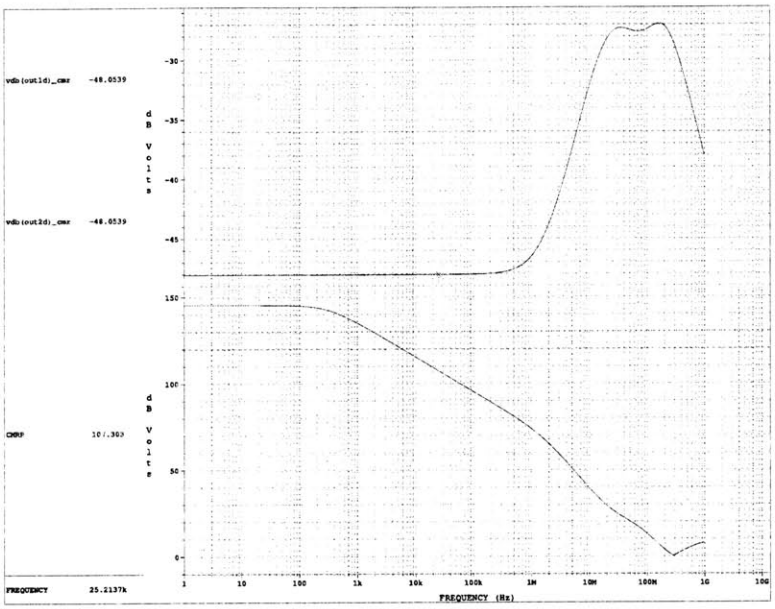
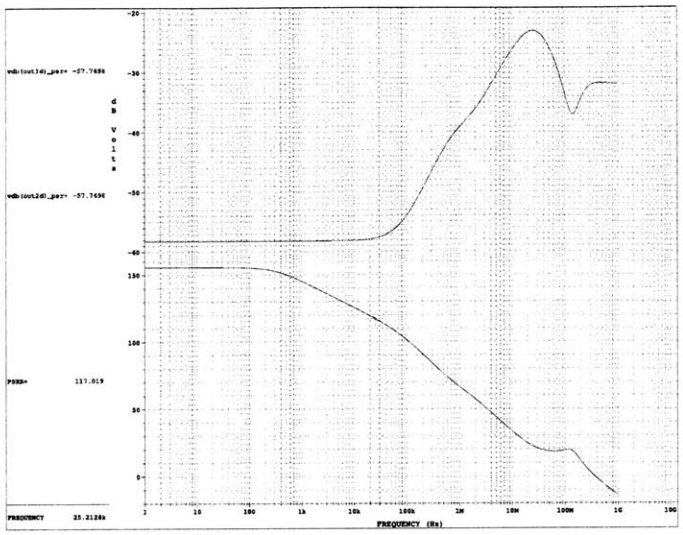


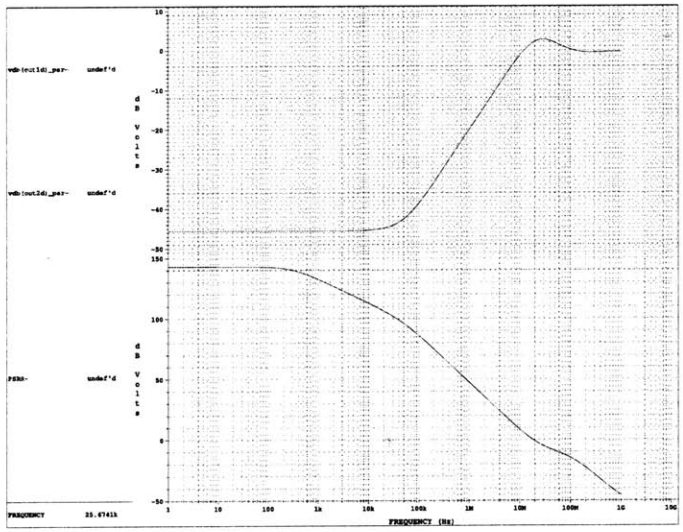
Figure 2-21: The upper plot shows the common mode gain of the op-amp. The lower plot shows the common mode rejection ratio.

Power-Supply Rejection Ratio

The power supply rejection ratio (PSRR) is another useful figure of merit for amplifiers. It gives the ratio between the differential gain and gain from the power supply. A large PSRR is desired so that any noise coupled from the power supply is suppressed.



(a) PSRR+.



(b) PSRR-.

Figure 2-22: Upper plots show the power supply gain. Lower plots show the power supply rejection ratio.

2.4.2 Output Swing

Refer to Section 2.2.2 for an explanation on what limits the output swing of the op-amp.

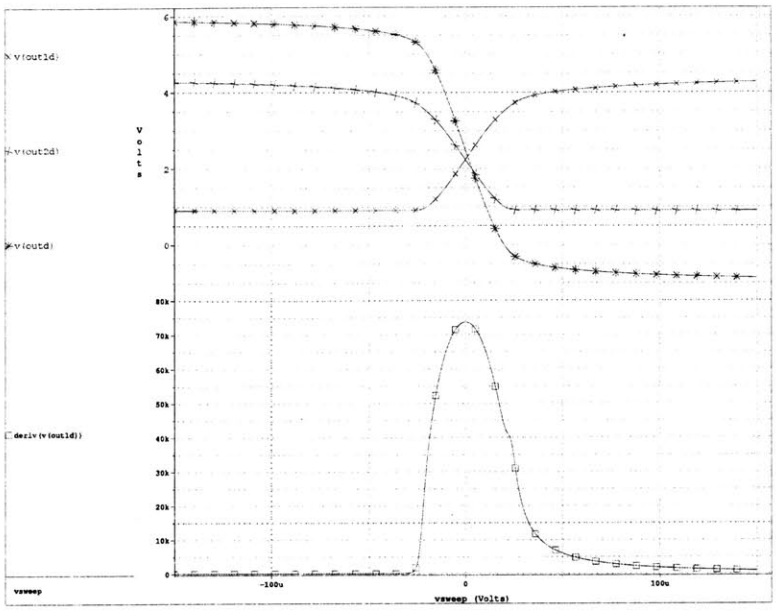
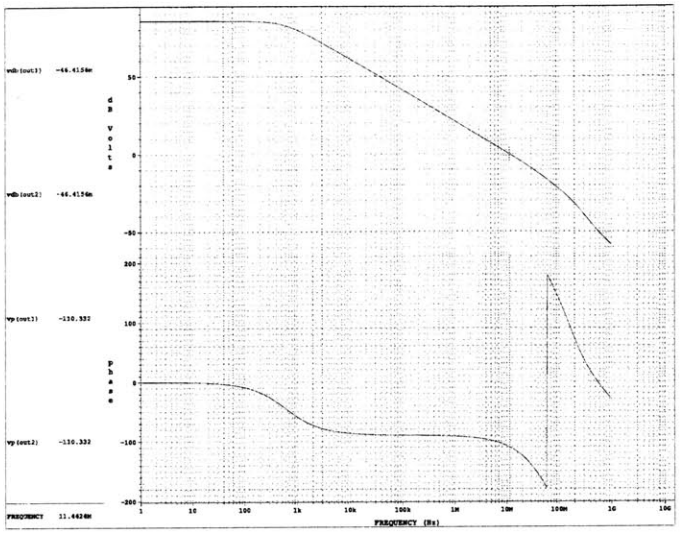


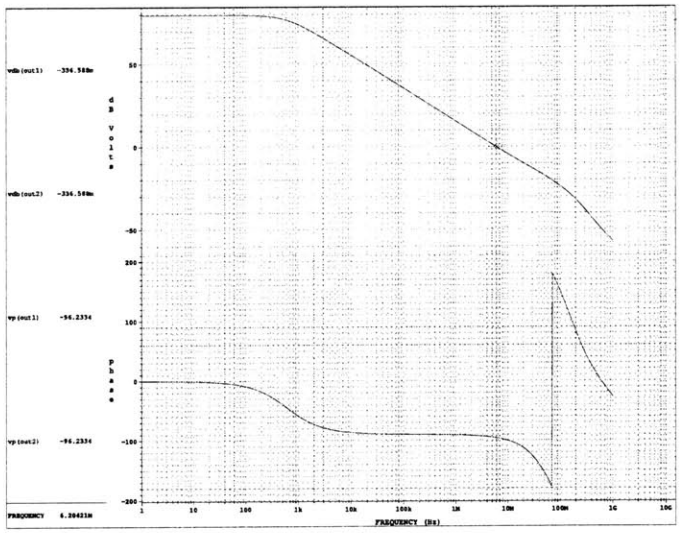
Figure 2-23: Output swing of the op-amp. The upper plot shows the output voltage as the input voltage is swept, and the lower plot shows the derivative of one of the outputs.

2.4.3 CMFB Loop

Section 2.2.2 covered a small-signal analysis on the the CMFB loop. Figures 2-24(a) and 2-24(b) compare the open-loop gain of the CMFB loop with and without MCM_7. The simulation results confirm the calculations in Section 2.2.2 that shows the open-loop gain of the circuit with MCM_7 to be twice that of the circuit without MCM_7.



(a) With transistor MCM_7.



(b) Without transistor MCM_7.

Figure 2-24: Bode plot of the open-loop configuration of the op-amp CMFB network

Chapter 3

Capacitive Feedback

In Sections 1.2.1 and 1.2.2 we discussed why we are choosing to use a capacitive feedback topology to close the loop around the gain amplifier. Recall that on-chip resistors perform poorly over temperature. In contrast, on-chip capacitors offer better ratio tracking, and superior voltage and temperature coefficients. This chapter will discuss the issues with capacitive feedback, and will introduce the topology that was chosen to deal with the problems.

It is important to note that all figures in this chapter display single ended op-amps to simplify the discussion. In implementation, the op-amps will be the fully differential gain amplifier analyzed in Chapter 2.

3.1 The Basic Capacitive Feedback Gain Topology

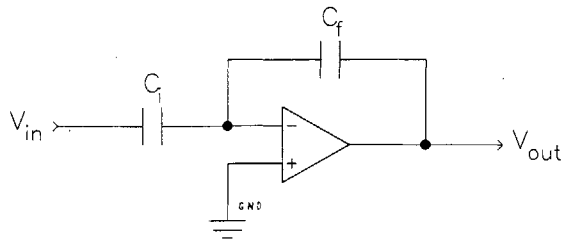


Figure 3-1: Capacitors as elements in a feedback path to provide gain.

As discussed in Section 1.2.1, one reason for choosing capacitors over resistors as passive feedback elements in an amplifier is that capacitors can be expected to match each other more closely. Figure 3-1 shows an inverting amplifier with capacitors, instead of resistors, used to provide gain. The transfer function of this amplifier is given by Equation 3.1.

$$\frac{V_{out}}{V_{in}} = -\frac{C_i}{C_f} \tag{3.1}$$

3.2 Adding a Feedback Resistor

The immediate problem with the configuration shown in Figure 3-1 is that capacitors have infinite impedance at DC, so no DC feedback voltage will be present at the inverting terminal of the op-amp. DC leakage currents (such as those coupled via the substrate) that enter the inverting node will have no alternative but to flow through the feedback capacitor. When sufficient charge is developed across the feedback capacitor, the output will saturate - rendering the amplifier inoperative.

One solution is to place a high valued resistor across the feedback capacitor. This is often seen in a charge amplifier and is shown in Figure 3-2. The transfer function of this amplifier is given by Equation 3.2. Resistor R_f provides a DC path (than the feedback capacitor) for current to flow to the output and, therefore, prevents output saturation.

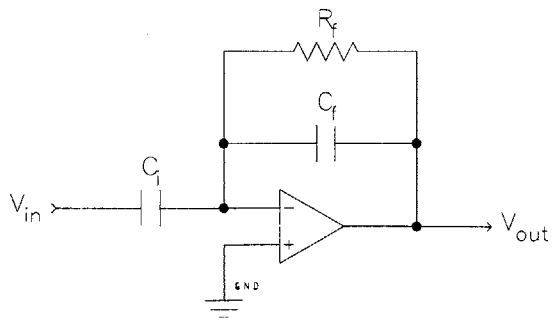


Figure 3-2: Using a feedback resistor to provide DC stabilization of the op-amp.

$$\frac{V_{out}}{V_{in}} = -\frac{sC_iR_f}{sC_fR_f + 1} \tag{3.2}$$

When $sC_fR_f >> 1$, the transfer function of the circuit approximates that of the circuit in Figure 3-1. For lower frequency input signals, in particular at the 8kHz-25kHz frequency band of interest (the resonant frequency of the proof mass flexures), the feedback resistance R_f needs to be very large (in the MΩ to GΩ range) in order for the two circuits in Figures 3-1 and 3-2 to have substantially equal transfer functions.

In the configuration in Figure 3-2, a higher R_f actually decreases its overall noise contribution. Voltage noise increases as the $\sqrt{R}$, but the low pass filter formed by the parallel combination of R_f and C_f causes noise to decrease as R. We can set R_f to be large enough so that the filter pole moves to a frequency well below our frequency range of interest so that the noise at that frequency band is attenuated by the filter. Of course, the R_f value must be appropriately sized for the expected DC leakage of the particular design so that a respectable dynamic range is preserved.

The major problem of the large feedback resistor solution to DC leakage is the difficulty of integrating it onto a chip. In a modern day CMOS manufacturing process, the resistor would require a silicon area that is orders of magnitude larger than the circuit itself. As a result, the resistor must be external to the IC, but it still exacts a small cost to board area.

3.3 Using an OTA as a DC Stabilizer

A continuous time, fully-integratable on-chip solution is shown as a simplified schematic in Figure 3-3. An operational transconductance amplifier (OTA) senses the voltage difference at its input terminals and outputs a current proportional to this difference. The OTA provides DC stabilization by sensing a rise or fall in the voltage at the output and sourcing or sinking, respectively, current from the summing node to compensate for the changing output.

This design has several drawbacks. First, the bias current of the OTA is dependent on the maximum leakage current, which is often not known beforehand. Second, this

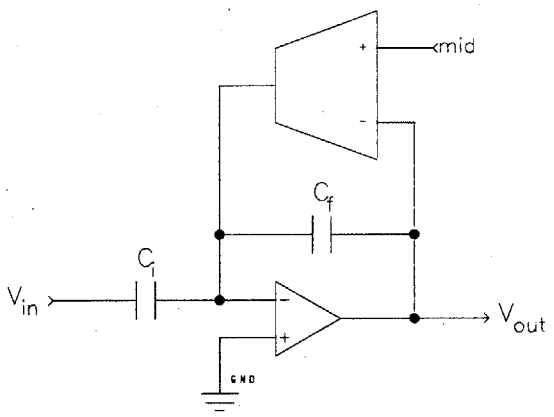


Figure 3-3: Using an OTA for DC stabilization.

topology can be very noisy because of the active element in the feedback path. Finally, such a complex feedback loop may be difficult to stabilize.

The next chapter will address each of these drawbacks as the design of a DC stabilizer is discussed.

Chapter 4

DC Stabilization Network

Section 3.2 discussed why a DC stabilizer is needed when capacitive feedback around an op-amp is used. Since capacitors have infinite impedance at DC, a DC bias must be provided for the summing node of the op-amp, or else any leakage current onto that node will saturate the amplifier. Typically, a very high valued resistor is used to stabilize the feedback capacitor, but that takes up more board area. Furthermore, bringing out nodes to connect the external resistor makes the amplifier gain sensitive to package pin parasitics. Instead, based upon an earlier design at Draper Laboratory[5], we propose the DC stabilizer shown in Figure 4-1. In addition to the operational transconductance amplifier (OTA) discussed in Section 3.3, a noise shunting capacitor and a high impedance path formed by two parallel transistors are added.

Table 4.1 gives a short description of each component found in Figure 4-1 and a typical value(s). Each component and how its value was chosen will be discussed in this chapter.

Note that references to leakage current in this chapter refer to the leakage current onto the input nodes of the op-amp.

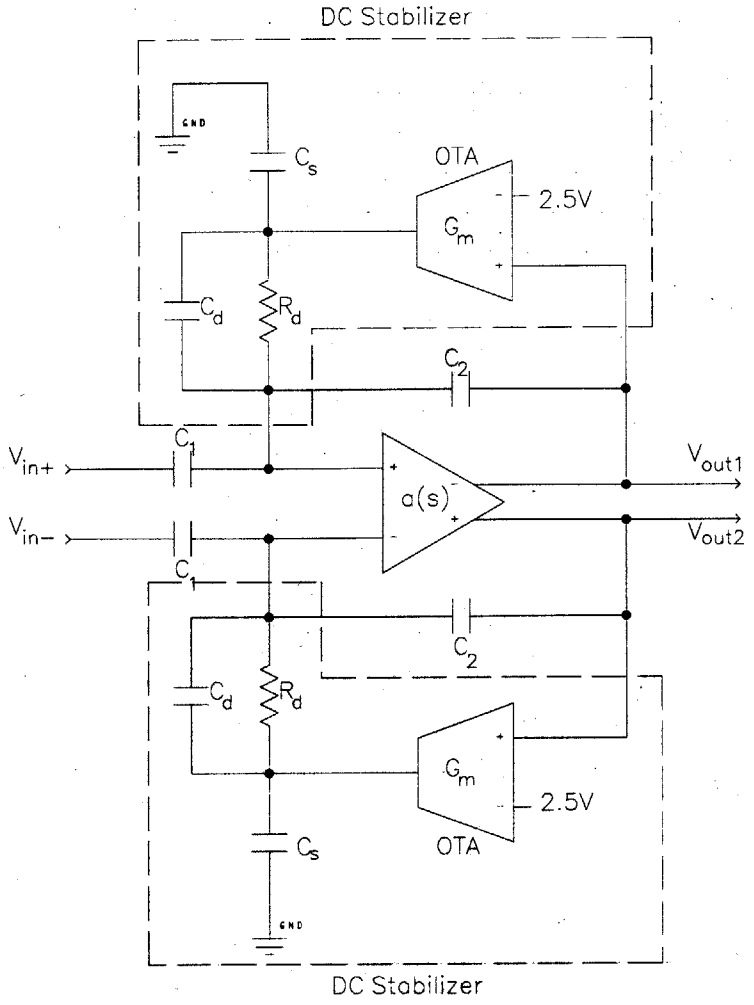


Figure 4-1: Simplified schematic of the op-amp and DC stabilizer loop.

4.1 Review of Second Order Systems [3, Sec 2.6]

The design of the DC stabilizer is tackled from a control theory perspective. To help the reader best understand the rest of this chapter, this section provides a quick review of second order systems.

A second order closed-loop transfer function can be written as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.1}$$

Here, ζ is the damping ratio of the system and ω_n is the undamped natural frequency.

C_1	Input capacitor	2-20pF
C_2	Feedback capacitor	2pF
G_m	OTA Transconductance	$25n\Omega^{-1}$
R_o	OTA output impedance	$10G\Omega$
C_s	OTA Load capacitance	5pF
R_d	High impedance path	$500M\Omega$-$500G\Omega$
C_d	Shaping capacitance across $_d$	.3pF

Table 4.1: Typical values of components in Figure 4-1.

When the damping ratio ζ is zero, ω_n is the frequency of oscillation of the system. Values for ζ fall into three categories:

1. *Underdamped,* $0 \leq \zeta < 1$ - The closed-loop poles are complex conjugate and lie in the left-half of the s-plane and the transient response oscillates. The system will oscillate indefinitely for ζ equal to zero.

2. *Critically damped,* $\zeta = 1$ - The closed-loop poles are nearly equal. The transient response does not oscillate.

3. *Overdamped,* $\zeta \geq 1$ - The closed-loop poles are unequal and located on the negative real axis. The transient response does not oscillate.

With respect to the DC stabilizer, the most relevant of these three cases is the underdamped case. An underdamped system will exhibit peaking in the frequency response. Peaking in the system can be viewed as a decrease in stability because it corresponds to the system poles being closer to the right-half plane. This is best illustrated by the complex conjugate pole pair seen in Figure 4-2. $\theta = cos^{-1}\zeta$ is defined as the angle that the poles make with the imaginary axis. The larger ζ is, the farther away the poles are from the imaginary axis and the more stable the system. The magnitude of the peaking, M_p, is related to the damping ratio through Equation 4.2.

$$M_p = \frac{1}{2\zeta\sqrt{1-\zeta^2}} \tag{4.2}$$

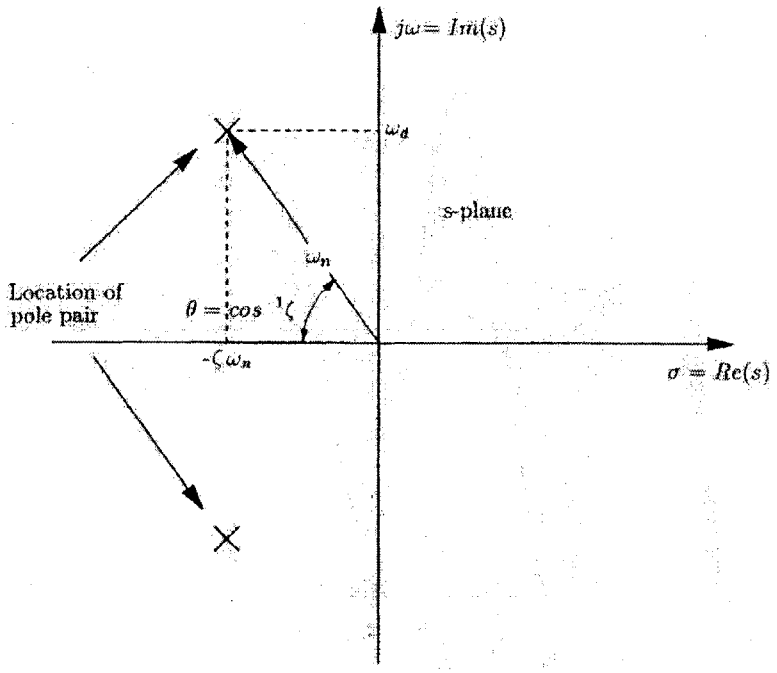


Figure 4-2: Complex conjugate poles in the s-plane. System is underdamped. [3, p.43].

For maximum stability, and minimal peaking, we want to increase ζ, or equivalently, we want to move the poles away from the imaginary axis.

4.2 DC Stabilizer Loop Analysis

4.2.1 Closed-Loop Transfer Function and AC Response

The frequency response of the op-amp was calculated in Section 2.1.2. The open-loop gain of the op-amp is:

$$a(s) = \frac{-g_{m1}r_{o3}\beta_5}{1 + s\beta_5 r_{o3}C_L + s^2 r_{o3}r_{o5}C_p C_L} \tag{4.3}$$

From Figure 4-1, we define the feedback factor $f(s)$ to be the gain from the output

node of the op-amp to the input node with the op-amp disconnected.

$$f(s) = \frac{V_{op}(s)}{V_{im}(s)} = \frac{s^2 N_2 + sN_1 + N_0}{s^2 D_2 + sD_1 + D_0} \tag{4.4}$$

Where:

$$N_2 = R_d R_o (C_2 C_d + C_2 C_s); \tag{4.5}$$

$$N_1 = R_d C_2 + R_o C_2 + R_d R_o C_d G_m \tag{4.6}$$

$$N_0 = G_m R_o \tag{4.7}$$

$$D_2 = R_d R_o ((C_1 + C_2)(C_d + C_s) + C_s C_d) \tag{4.8}$$

$$D_1 = R_o (C_1 + C_2) + R_d C_d + R_o C_s + R_d (C_1 + C_2) \tag{4.9}$$

$$D_0 = 1 \tag{4.10}$$

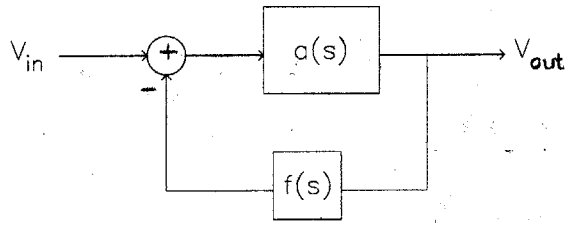


Figure 4-3: Op-amp block diagram.

Figure 4-3 shows the block diagram that can be used to model the closed-loop formed by one side of the op-amp. $a(s)$ is the open-loop gain of the op-amp given by Equation 4.3, and $f(s)$ is the feedback factor given by Equation 4.4.

The closed-loop gain of the op-amp is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a(s)}{1 + a(s)f(s)} \tag{4.11}$$

When $a(s)f(s) >> 1$, $\frac{V_{out}(s)}{V_{in}(s)}$ can be approximated as $\frac{1}{f(s)}$, or one over the feedback factor. By looking at the bode plot of the loop gain $a(s)f(s)$, we can conclude that this approximation is valid for frequencies up until 1MHz. This approximation also

allows us to approximate the poles of the closed-loop gain as the zeroes of the feedback factor.

We can use Equations 4.4 through 4.10 to calculate the closed-loop pole locations:

$$p = -\frac{N_1}{2N_2} \pm \frac{1}{2}\sqrt{(\frac{N_2}{N_1})^2 - 4\frac{N_0}{N_2}} \tag{4.12}$$

By matching the coefficients between the denominators of Equations 4.1 and 4.4, the damping factor ζ is:

$$\zeta = \frac{1}{2}\frac{N_1}{\sqrt{N_0 N_2}} \tag{4.13}$$

After we make the approximations that $N_1 \approx R_d R_o C_d G_m$ and $C_s >> C_d$ (reasonable approximations to make, given the values in Table 4.1), the approximate closed loop pole locations and damping factor are given by Equations 4.14 and 4.15, respectively.

$$p \approx -\frac{G_m C_d}{2C_s C_2} \pm \frac{1}{2}\sqrt{(\frac{G_m C_d}{C_s C_2})^2 - \frac{4G_m}{R_d C_2 C_s}} \tag{4.14}$$

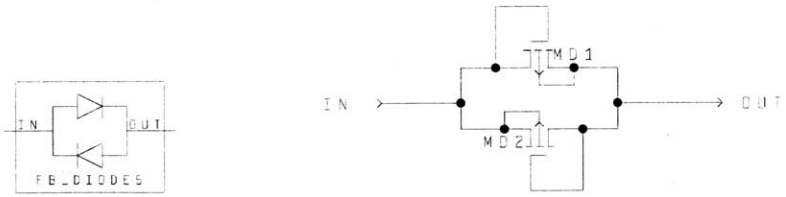
$$\zeta = \frac{1}{2}\frac{\sqrt{R_d G_m} C_d}{\sqrt{C_2(C_d + C_s)}} \tag{4.15}$$

Equations 4.14 and 4.15 will be referred to often in the sections to follow as we analyze how choices in component values affect the stability of the loop.

4.3 Component Description

4.3.1 Back-to-Back Diodes

The high-impedance path represented by resistor R_d is comprised of two parallel transistors with their gate and drain terminals connected. A schematic is shown in Figure 4-4(b). When a transistor has its gate and drain terminals tied together, it is often referred to as being diode connected. Therefore, the topology shown in



(a) Symbol (b) Schematic.

Figure 4-4: Back-to-back diodes

Figure 4-4(b) is called a back-to-back diode block.

The transistors are connected in opposite directions to allow for current flow in either direction. This block has extremely high impedance if the current through it is very small. Figure 4-5 shows the impedance of the back-to-back diodes as a function of leakage current. Sample impedances at various leakage values are given in Table 4.2.

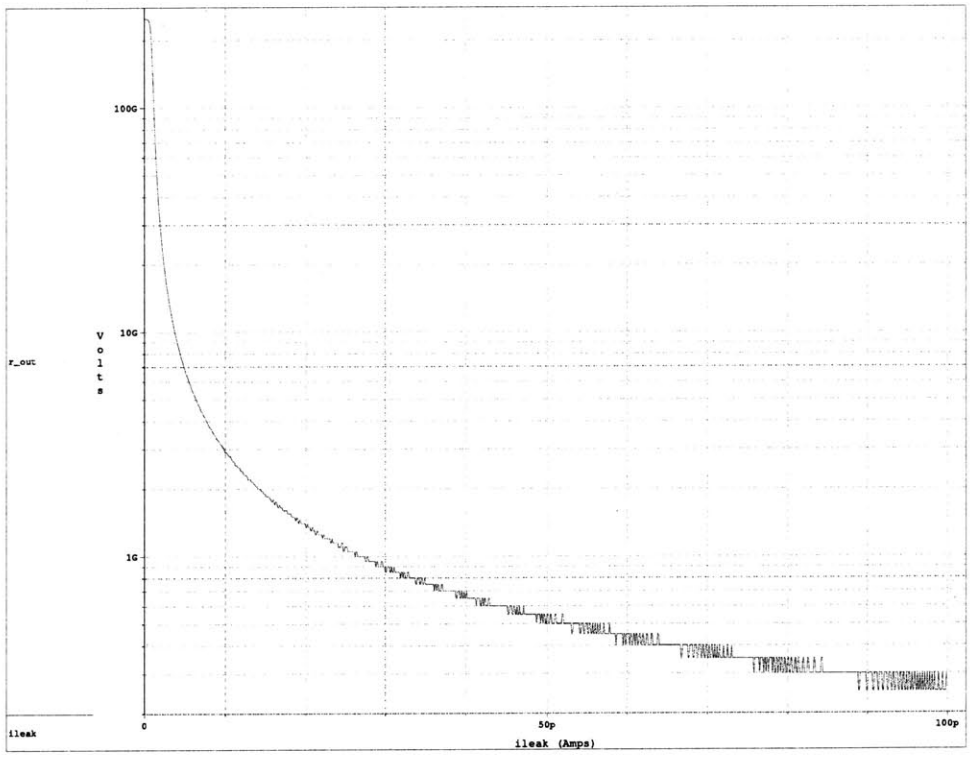


Figure 4-5: Impedance of the back-to-back diodes as a function of leakage current.

Figure 4-5 shows that the impedance of the diodes is an exponential function. This is because transistors M_{d1} and M_{d2} operate in the linear region of weak inversion

I_{leak}	R_o
1pA	150GΩ
2pA	28.3GΩ
3pA	14GΩ
4pA	9.33GΩ
5pA	6.5GΩ
10pA	3GΩ
15pA	2GΩ
20pA	1.25GΩ
30pA	850MΩ
50pA	550MΩ
100pA	250MΩ

Table 4.2: Impedances of the back-to-back diodes for various values of leakage current.

(weak inversion is when $V_{GS} < V_T$ and the linear region of operation is when $V_{DS} <$ 100mV). The effective impedance of a transistor with its gate and drain connected is equal to $\frac{1}{g_m}$, where g_m is the transconductance of the transistor. In weak inversion, $g_m = \frac{qI_{ds}}{nkT}$, where I_{ds} is the drain to source current of the transistor, $\frac{kT}{q}$ is the thermal voltage $\approx$ 26mV, and n is the transistor slope factor $\approx$ 1.5-1.6.

The drain-to-source current of transistors in weak inversion is an exponential function of the gate-to-source voltage (or more indirectly, the surface potential of the channel):

$$I_{ds} = I_o e^{\frac{qV_{gs}}{nkT}}(1 - e^{\frac{-qV_{gs}}{kT}}) \tag{4.16}$$

Where I_o is the specific current of the transistor.

Therefore, the impedance of one diode connected transistor is inversely related to the drain-to-source current given in Equation 4.16. This gives the back-to-back diodes the exponential impedance response seen in Figure 4-5.

The purpose of capacitor C_d, placed across the back-to-back diodes, will be explained in Section 4.3.4.

4.3.2 Noise Shunting Capacitor

One of the main problems with using an OTA for DC stabilization is that its bandwidth may not be low enough, which means it can feed signals at the frequency band of interest from the output of the op-amp back to the input. The excess bandwidth leads to poor noise performance. Therefore, we desire for the DC stabilizer to have a low enough bandwidth so that it will only respond to DC level changes at the output of the op-amp.

Mathematically, the ratio $\frac{G_m}{C_s}$ can be sized to help determine the bandwidth of the feedback loop. This is discussed in Section 4.3.3. What follows below is more of an qualitative explanation for the function of C_s.

Capacitor C_s provides a low impedance path to shunt the undesired high frequency feedback signals to ground. C_s presents an impedance of $\frac{1}{2\pi f C_s}$ to the signal, where f is the signal frequency. The value of C_s is chosen to ensure that the impedance of the shunting capacitor is much lower than the impedance of the back-to-back diodes for signal frequencies between 8kHz and 25kHz (the resonant frequency range of the proof masses).

In order to guarantee that the impedance of $\frac{1}{sC_s} << R_d$, we want to make C_s as large as possible, e.g. the largest capacitor able to be manufactured on-chip. However, as shown in Figure 4-6, increasing C_s also destabilizes the system, as evidenced by the increasing peaking by the closed-loop response.

The lower bound on the value of C_s can be found by knowing the expected leakage current into the summing node. From experimentation, the maximum expected leakage is 20pA. From Table 4.2, the minimum impedance of the back-to-back diodes for 20pA of current is 1.25GΩ. Therefore, the minimum C_s is chosen to be 5pF so that its impedance from 8kHz to 25kHz is much less than 1.25GΩ. For signal frequencies at 8kHz and 25kHz, C_s has an impedance of 3.98MΩ and 1.27MΩ, respectively.

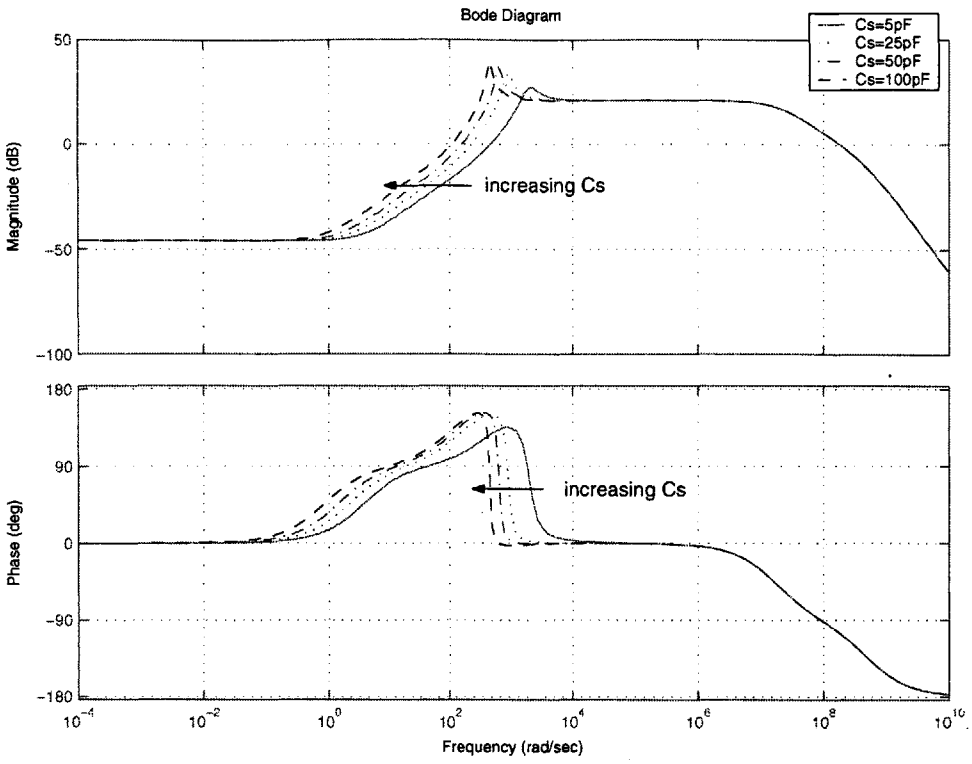


Figure 4-6: Bode plot of the system closed-loop response with varying C_s.

4.3.3 Operational Transconductance Amplifier (OTA)

An OTA is a transconductance amplifier; it outputs a current proportional to the voltage difference at its inputs. Two important figures of merit for an OTA are its linear range V_L and its transconductance G_M. The linear range is defined as the range of differential input voltage that produces an approximately linear output current. The transconductance is the slope of the output current to the input voltage. Typically, the value cited is for zero differential input. However, often the transconductance changes with the differential input (the slope of the voltage-to-current curve is not necessarily constant). Given an input voltage, the transconductance allows us to calculate the output current: $I_{out} = G_m V_{in}$.

Transconductance

From Equation 4.14, the closed-loop pole locations are proportional to the ratio of transconductance and output capacitance: $\frac{G_m}{C_s}$. The closed-loop pole locations are

calculated in Section 4.2.1.

Figure 4-6 shows how the low frequency breakpoint of the OTA changes as a function of varying the $\frac{G_m}{C_s}$ ratio (In this plot, G_m is fixed at $20n\Omega^{-1}$, while C_s changes). Notice the peaking that occurs at low frequency (more detail on the peaking is found in Section 4.3.4). The system will behave properly only when the signal frequency range is contained within the flatband of the closed-loop AC response curve. A maximum $\frac{G_m}{C_s}$ ratio of approximately 4000 will ensure that the low frequency peaking occurs at frequencies below 1kHz.

The freedom in choosing G_m will be limited by the value of the shunting capacitor C_s. Section 4.3.2 explains why we chose the minimum value of C_s to be 5pF. Given a minimum C_s of 5pF, and a maximum $\frac{G_m}{C_s}$ ratio of 4000, the minimum G_m is $20n\Omega^{-1}$.

Linear Range

The relationship between linear range and transconductance is given by $V_L = \frac{I_{bias}}{G_m}$, where I_{bias} is current for when the output of the OTA saturates. The value for I_{bias} should be chosen such that it is greater than the maximum expected leakage current. This will guarantee that the OTA will operate in its linear range for all possible leakage currents and the DC stabilizer loop will be able to respond properly. The maximum measured leakage current on the summing node is 20pA. However, Draper Laboratory expects that the leakage could be as high as 20nA, so I_{bias} has been set at at least 20nA.

The input to the OTA in the DC stabilizer is connected directly to the output of the op-amp. Even though the output of the op-amp may swing up to 2Vpp (on either side), the limited bandwidth of the DC stabilizer loop allows it to only respond to the smaller changes in the DC value of the output. This means that the OTA does not have to have a wide linear range. However, a smaller linear range for a given I_{bias} means that the transconductance G_m must be larger. Subsequently, the shunting capacitor C_s must also be increased to maintain a low loop bandwidth. A wide linear range OTA is typically more difficult to design, but a smaller linear range OTA requires a larger chip area for C_s. Therefore, a tradeoff exists when choosing

the proper G_m and V_L.

OTA100MB

Draper Laboratory has previously designed and tested a low-g_m OTA called the OTA100MB. The advantage of the OTA100MB over some standard OTAs is its high linearity and provision for temperature compensation. A circuit level discussion is beyond the scope of this thesis, but a brief summary of its characteristics is presented in this section.

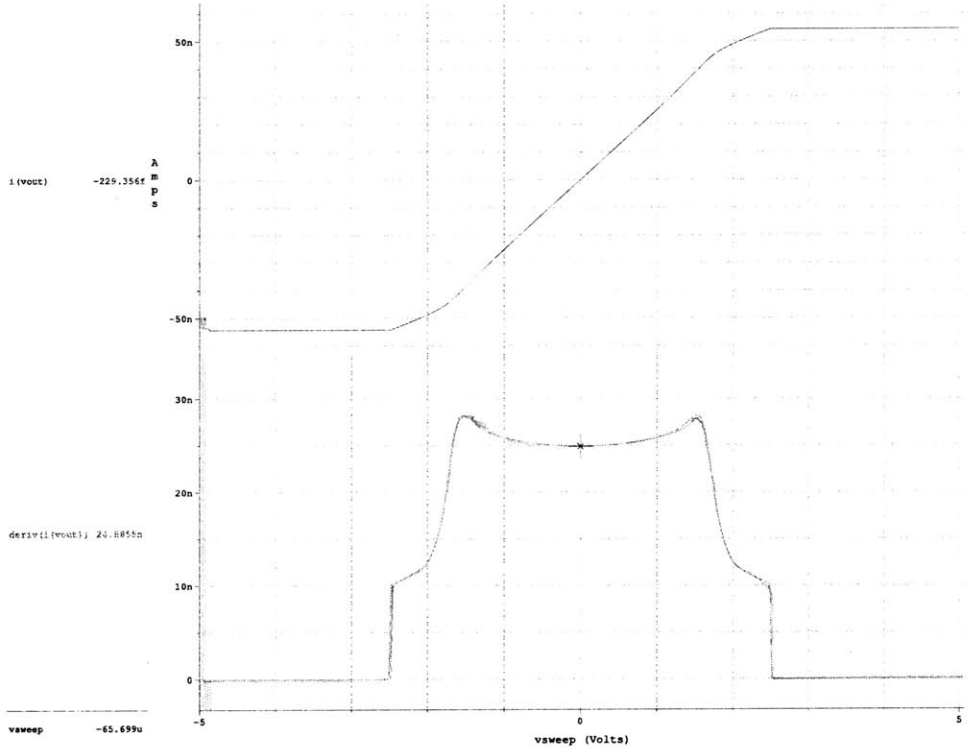


Figure 4-7: DC sweep showing the linear range and transconductance of the OTA100MB.

From Figure 4-7, we see that the transconductance G_m of the OTA100MB is 24.8855nΩ^{-1} and the linear range V_L is $\pm$2.184V. The saturation current level I_{bias} is set at 54.349nA. By setting the transconductance to be 24.8855nΩ^{-1}, we are able to use the minimum possible value for shunt capacitance, C_s =5pF, to minimize chip area.

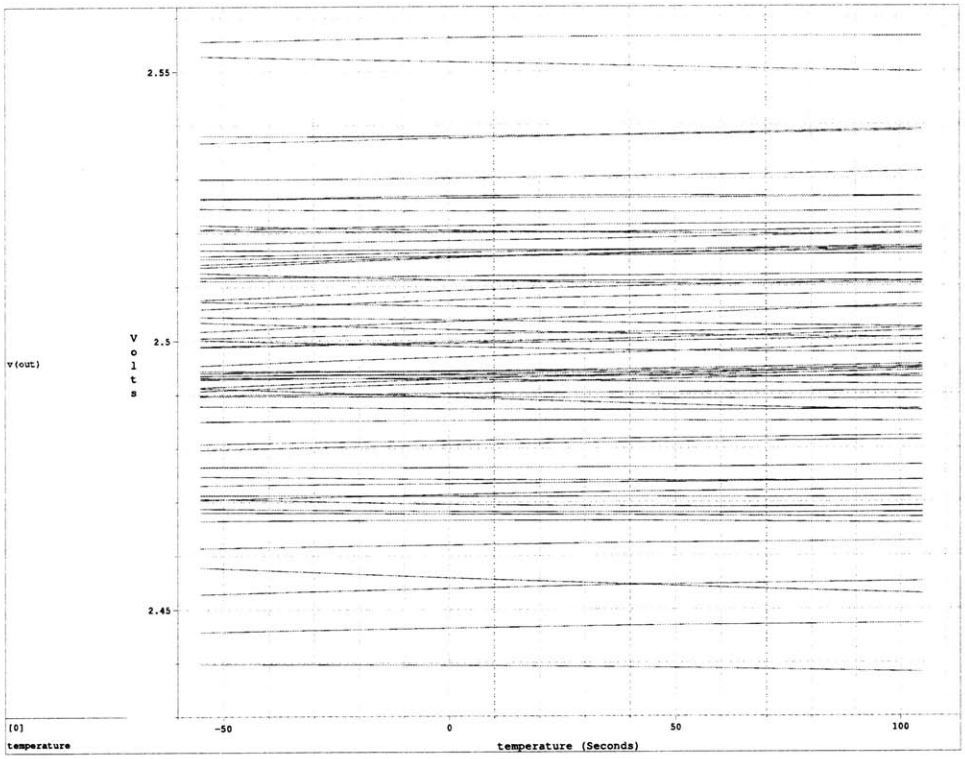


Figure 4-8: Monte carlo simulation with a temperature sweep showing OTA offset.

The one disadvantage of the OTA100MB is its high offset levels. The offset is defined as the differential input voltage that produces zero output current. Offset of the OTA100MB is illustrated in Figure 4-8. This offset is typical low-g_m transconductance amplifiers. To achieve the low-g_m, transistors of the OTA are driven into sub-threshold where voltage offset becomes more sensitive to device mismatches. The output of the Monte Carlo simulation in Figure 4-8 shows that there is approximately a $\pm$50mV offset in the OTA. In the DC stabilizer, the negative terminal of the OTA is connected to MID. Therefore, the OTA offset appears as voltage source on the positive terminal of the OTA. However, the positive terminal of the OTA is connected directly to the output of the op-amp. This OTA offset causes the output voltage of the amplifier to be offset by 2.5$\pm$.05V.

Fortunately, the offset of the OTA does not present an issue because the output of the amplifier is AC coupled to the following stage.

4.3.4 Diode Capacitance

In order to understand why C_d was added to the system, consider first the DC stabilizer without C_d. The OTA senses a rise or fall in output voltage due to the charging of capacitor C_2 and outputs a current proportional to the difference between the output voltage and desired common-mode level. High frequency components are shunted to ground by C_s so that very little signal noise is fed back to the input.

The plots in Figure 4-9 show the pole-zero locations of the closed-loop system without C_d for various values of R_d (representing various values of leakage current). The closed-loop response has been approximated as $\frac{1}{f(s)}$ so that we can look most closely at the poles and zeroes due to the DC stabilizer. Figure 4-10 shows the corresponding frequency responses (no approximations have been made on the closed-loop response here).

The low frequency peaking seen in Figure 4-10 is caused by the complex conjugate poles of the second order response of the closed-loop system. Section 4.1 explained how the damping ratio ζ affected the peaking in the system and the stability of the system. C_d increases the stability of the system by increasing the damping ratio ζ.

The plots in Figure 4-11 show the pole-zero locations of the closed-loop system with C_d included for various values of R_d (representing various values of leakage current). Again, the closed-loop response has been approximated as $\frac{1}{f(s)}$. Figure 4-12 shows the corresponding frequency responses (no approximations have been made on the closed-loop response here).

With the addition of C_d, the low frequency peaking has been reduced. The root-locus plots support the lower peaking by showing that for high levels of leakage current, the complex conjugate poles move farther away from the imaginary axis. For lower levels of leakage, the addition of C_d causes the poles to move to the real axis and eliminates peaking entirely.

A less intuitive, but equally reasonable way of seeing the affect of C_d is to analyze the damping ratio ζ mathematically. From Equation 4.15, we see that ζ is approximately proportional to $\sqrt{C_d}$. So by increasing C_d, we increase the damping ratio ζ,

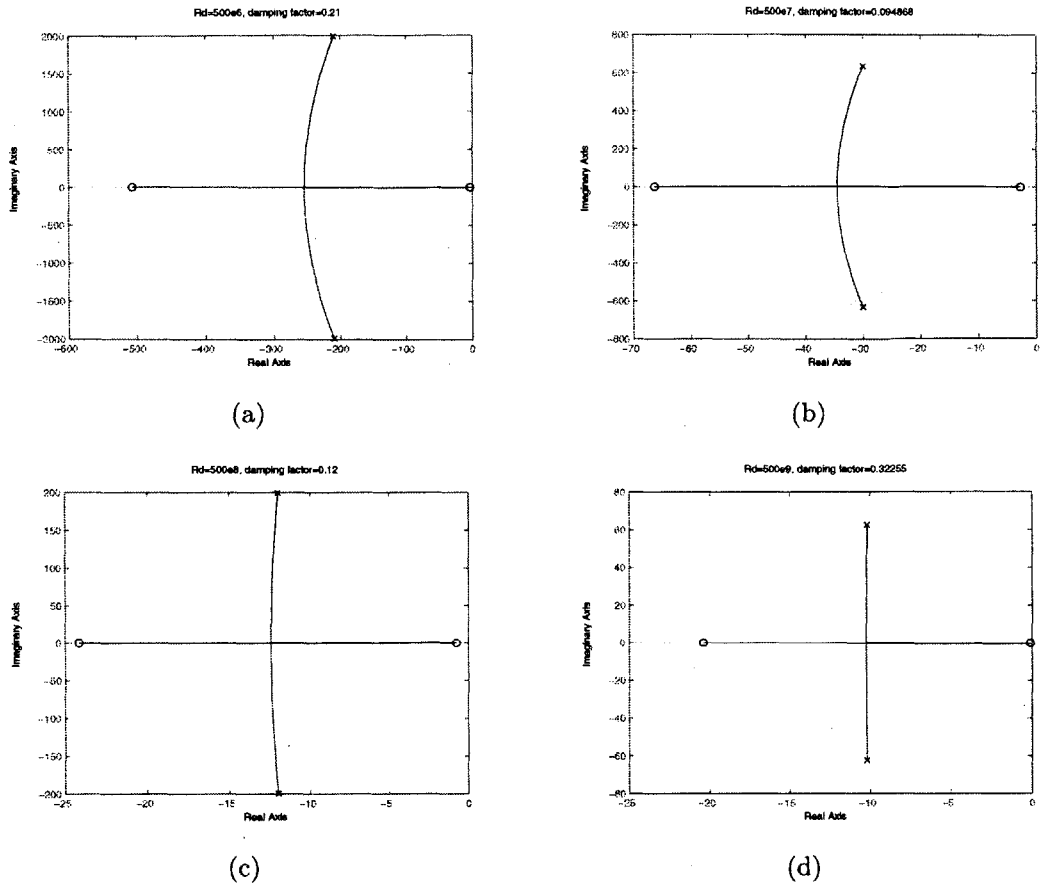


Figure 4-9: Root locus plots of the system closed-loop response with varying leakage current. Plots created with $C_d = 0pF$.

which decreases peaking.

Clearly, increasing C_d improves the stability of the closed-loop system. However, C_d cannot be increased without limit because of the penalty in noise performance. The impedance presented by C_d should be large enough that within the 8kHz to 25kHz frequency band of interest, signal noise still prefers to travel through C_s. A value of .5pF for C_d is a good compromise between reducing the low frequency peaking and not letting too much signal noise through to the input of the op-amp.

4.4 Summary

The values of the final design of the system are summarized in Table 4.1 at the beginning of the chapter.

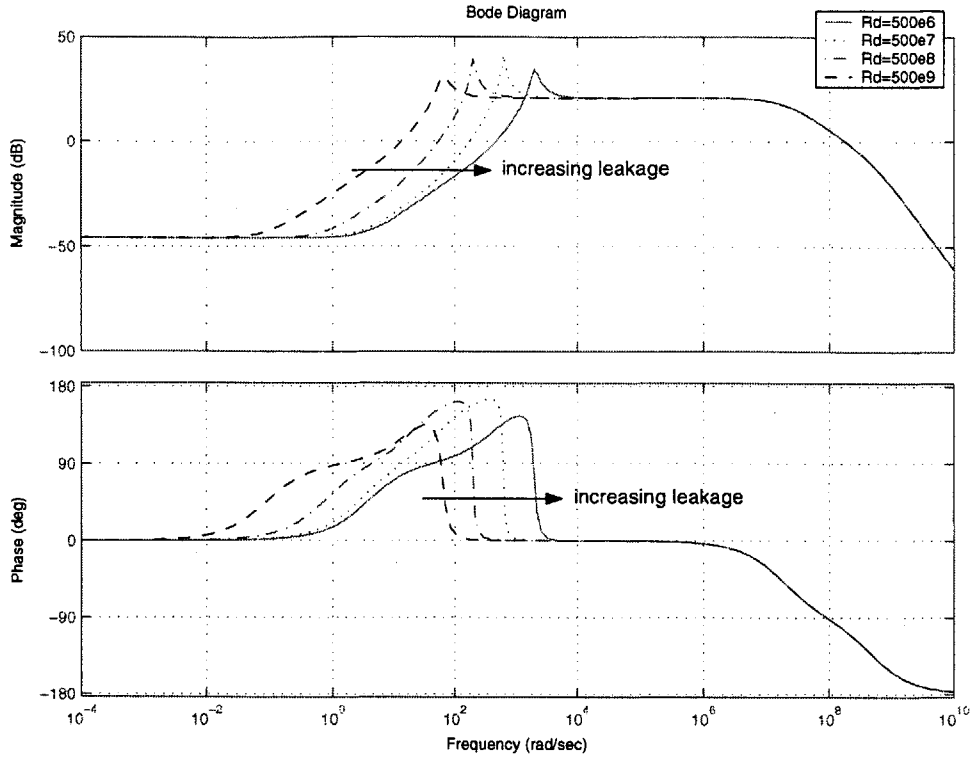


Figure 4-10: Bode plot of the system closed-loop response with varying leakage current. Plot created with $C_d = 0pF$.

In Section 3.3, three drawbacks of using an OTA as a DC Stabilizer were mentioned. These drawbacks, as well as the methods proposed here to deal with them are summarized below.

1. *Bias current of the OTA is dependent on the maximum leakage, which is not often known beforehand.* Draper Laboratory has tested its chips and has been able to accurately predict maximum levels of leakage current.

2. *The OTA in the feedback path degrades noise performance.* The addition of capacitor C_s allows the system to shunt noise at the signal frequencies to ground.

3. *OTA feedback loop can be difficult to stabilize and achieve good frequency performance.* The low frequency peaking caused by the complex conjugate poles in the second order system of the DC stabilizer can be minimized by the addition of capacitor C_d across the back-to-back diodes.

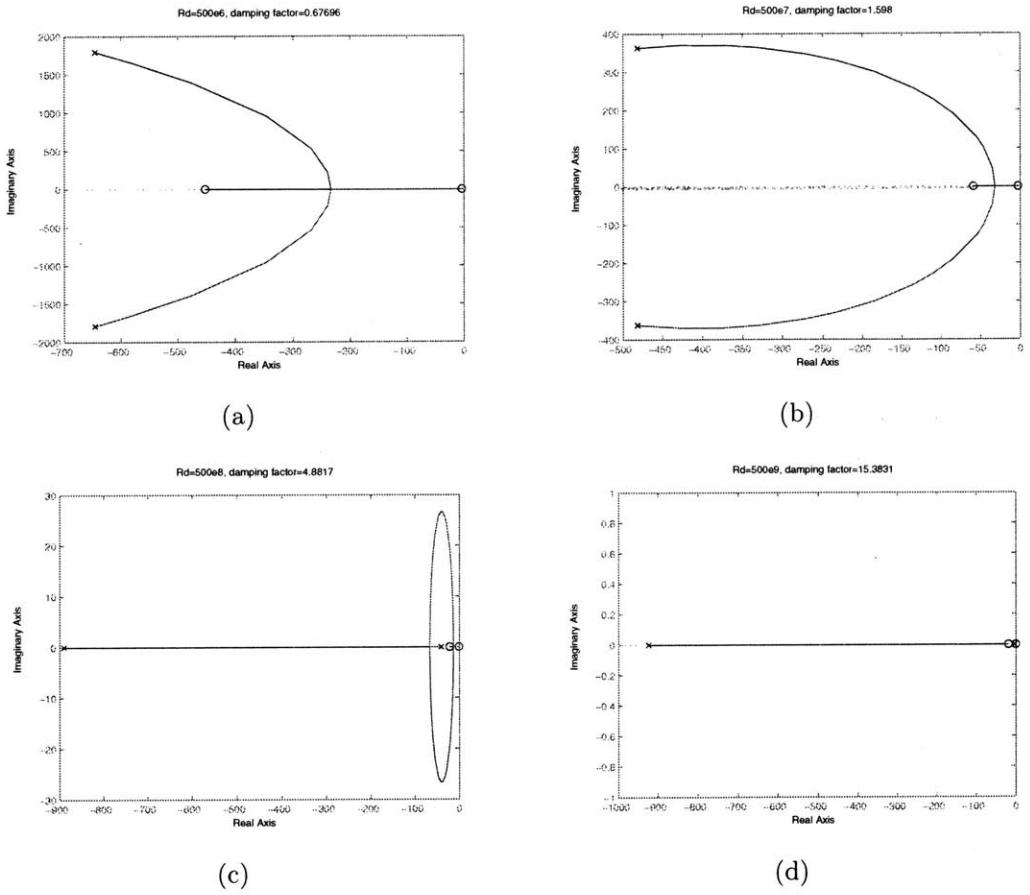


Figure 4-11: Pole-zero plots of the system closed-loop response with varying leakage current. Plots created with $C_d = 0.5pF$.

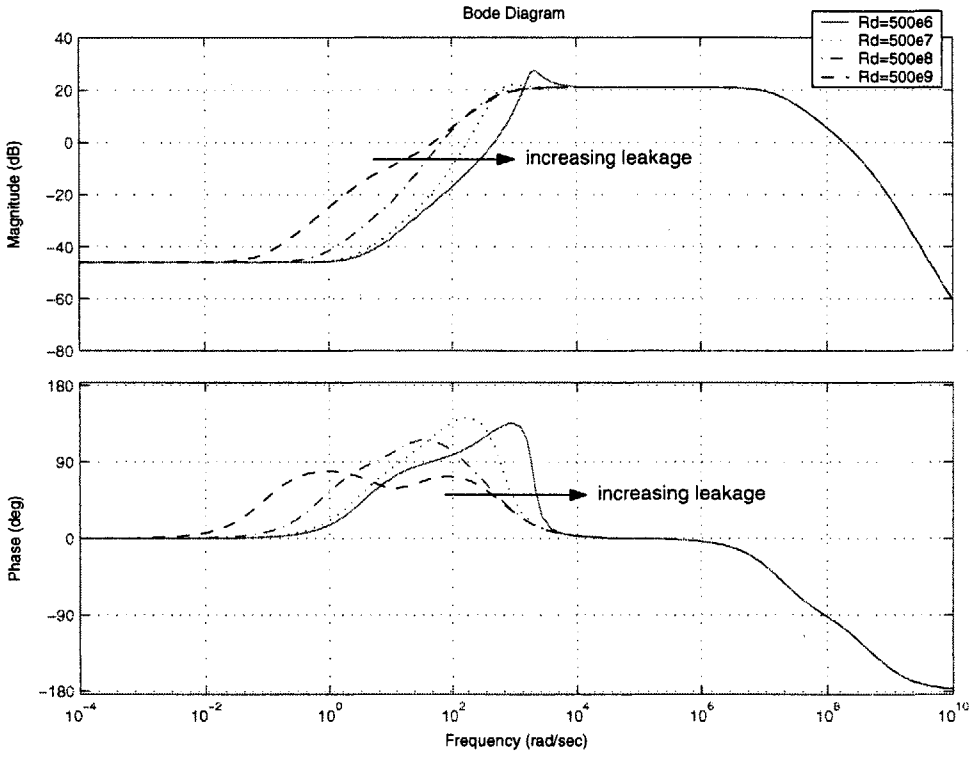


Figure 4-12: Bode plot of the system closed-loop response with varying leakage current. Plot created with $C_d = 0.5pF$.

Chapter 5

Gain Amplifier System Simulation Results

Important simulation results are summarized in Table 5. See Appendix A for output plots and the setup used to perform each simulation.

	Requirement	Achieved
Total Harmonic Distortion (THD)	-60dB for 4Vpp output swing at 25kHz	-100dB
Input referred noise	$< 35\frac{nV}{\sqrt{Hz}}$	$30\frac{nV}{\sqrt{Hz}}$
Gain Stability	< 0.1% from -55°C to 105°C	< 0.025% from -55°C to 105°C
Static phase shift	< 1°	< 1°
Dynamic phase shift	< 0.5°	< 0.5°
Loop gain phase margin	45°	89°

Table 5.1: System simulation results.

5.1 AC Simulations

5.1.1 Gain and Magnitude

Figure 5-1 shows the AC closed-loop response of the AC gain amplifier for a leakage current range of 0pA to 100pA. To see why we needed to add the capacitance across

the back-to-back diodes, compare the low frequency peaking in Figure 5-1 to that in Figure 5-2 and notice the increased peaking when the capacitance is removed.

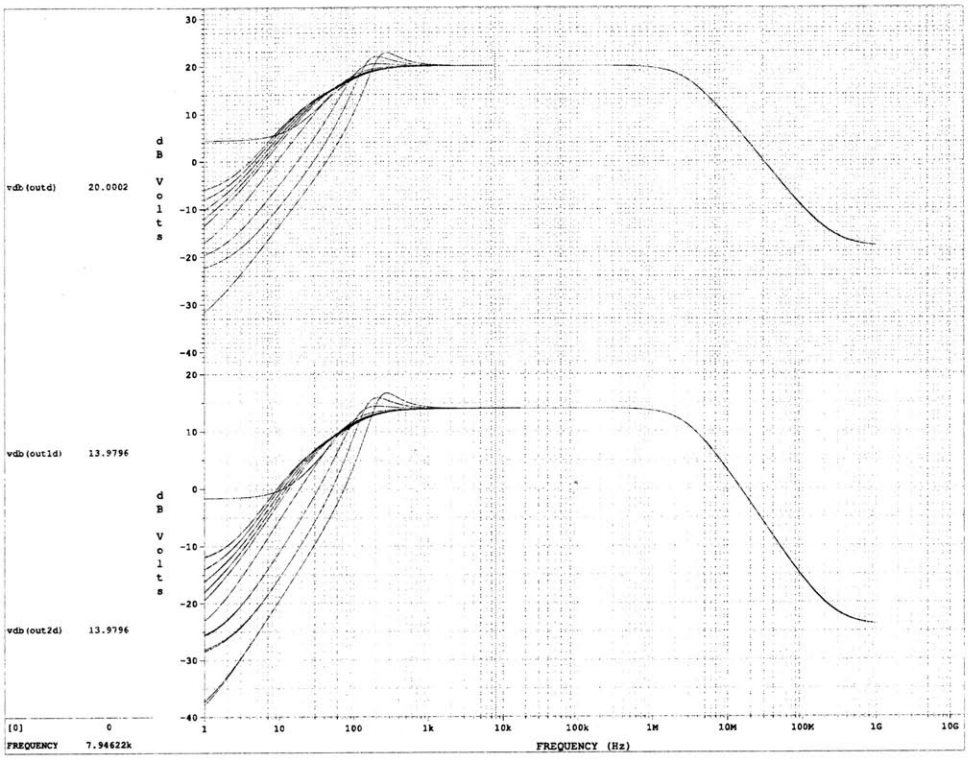


Figure 5-1: Bode plot of the closed-loop system with C_d included.

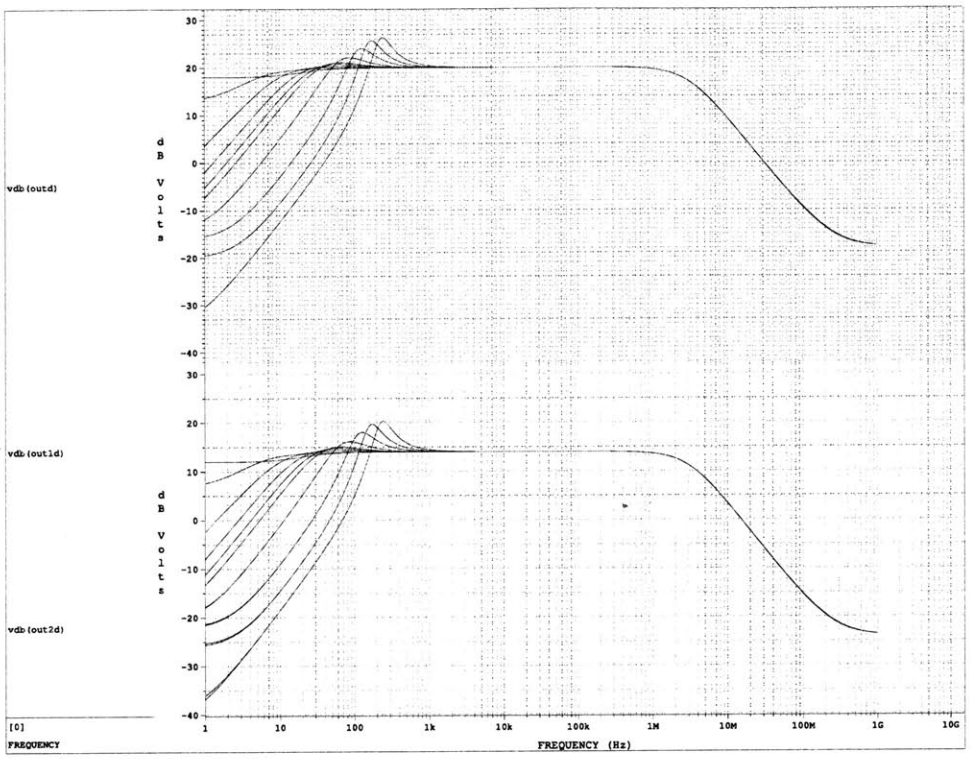


Figure 5-2: Bode plot of the closed-loop system with C_d removed. Notice the increased peaking.

5.1.2 Noise

Recall from Section 2.4 that the input referred noise of the op-amp was $19\frac{nV}{\sqrt{Hz}}$. From figure 5-3, we can see that the addition of the DC stabilizer contributes only $23\frac{nV}{\sqrt{Hz}}$, increasing the total input amplifier noise by only $11\frac{nV}{\sqrt{Hz}}$. There are two ways to decrease the noise contribution of the DC stabilizer. First, we could increase the shunt capacitance, C_s, so that more noise at the frequency range of interest is shunted to ground and less is fed back to the input. Second, we could decrease the capacitance across the back-to-back diodes, C_d (recall from Section 4.3.4 that this capacitance acts to feed-through signal back to the input). However, both of these solutions would also increase the low frequency peaking of the system. The values of C_d and C_s were chosen to maximize system stability while maintaining the noise level of the system to be under the maximum value of $35\frac{nV}{\sqrt{Hz}}$.

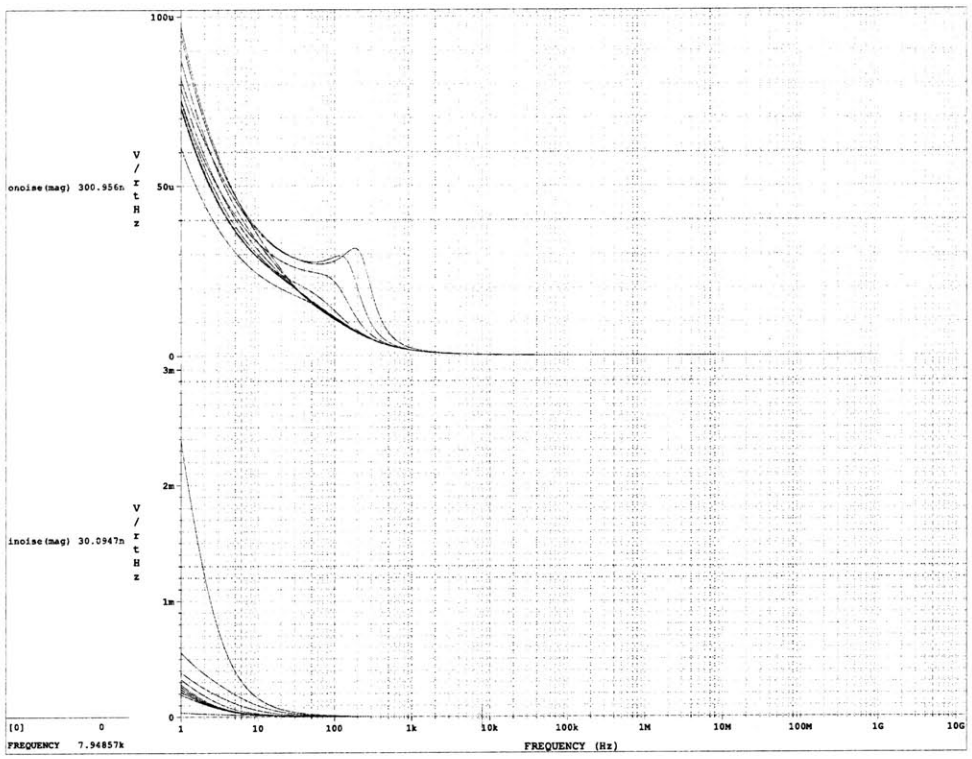


Figure 5-3: Output and input referred noise of the system.

5.1.3 Phase Shift and Gain Stability

The system gain stability and dynamic phase shift are both functions of temperature. From -55°C to 105°C, the gain should not vary more then 0.1% and the phase should not vary more then 0.5°. Gain stability and phase shift are described in more detail in Section 1.2.3.

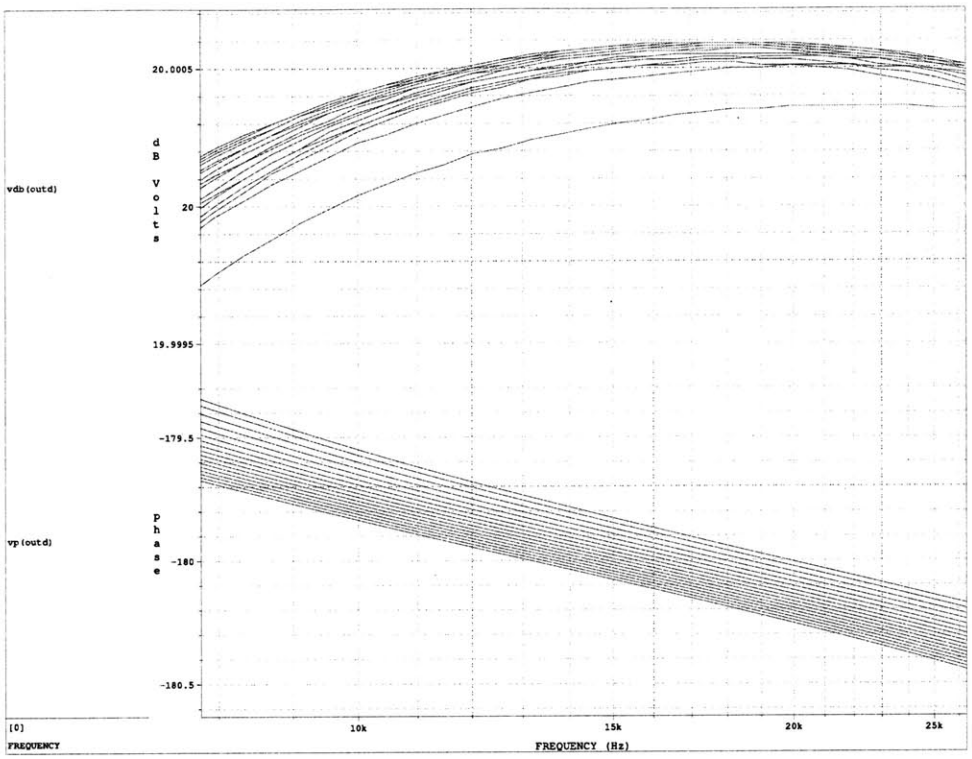


Figure 5-4: Upper plot demonstrates gain stability, and the lower plot shows the dynamic phase shift of the system.

Figure 5-4 is a plot of the gain and phase of the system. We have zoomed into the frequency range of interest, from 8kHz to 25kHz. The temperature has been swept from -55°C to 105°C in increments of 10°C and each line represents the gain/phase at a particular temperature. The upper plot shows that the gain varies between 19.9998dB and 20.0006dB. This is equivalent to a maximum of .004% of variation in gain. The lower plot shows that the phase at each frequency stays within 0.5° over temperature.

5.1.4 Static Phase Shift

The system's static phase shift as leakage current is varied is shown in Figure 5-5. Even with varying leakage current, the phase varies less than 1° for signals in the frequency band from 8kHz to 25kHz.

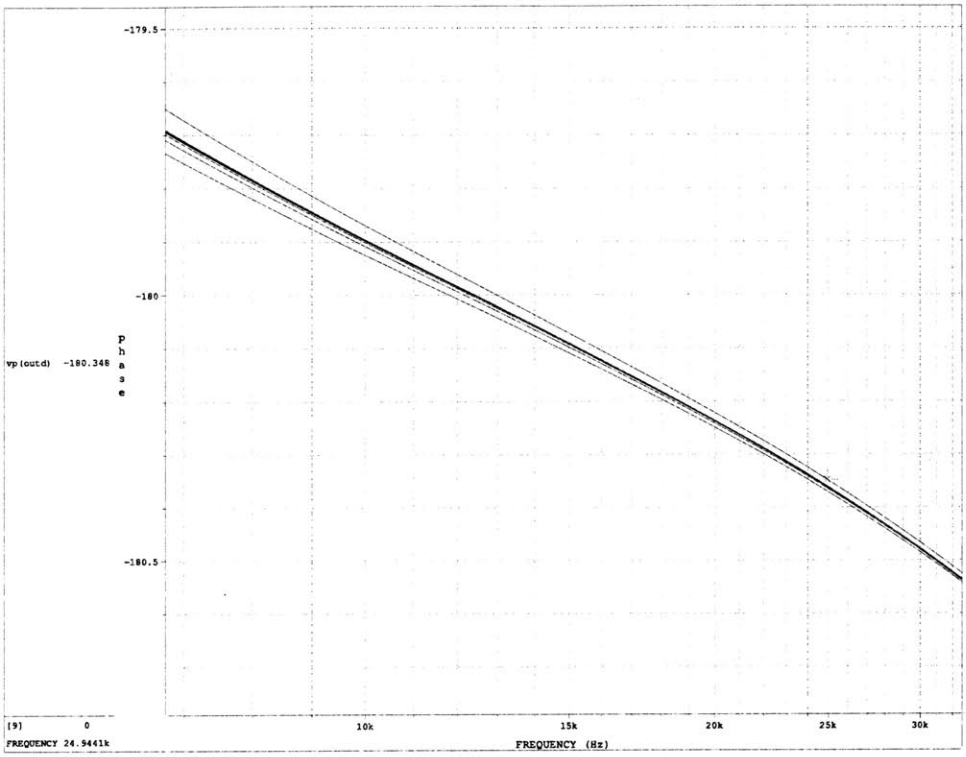


Figure 5-5: Static phase shift.

5.1.5 Loop Gain

Figure 5-6 verifies the stability of the system; there is sufficient loop gain phase margin.

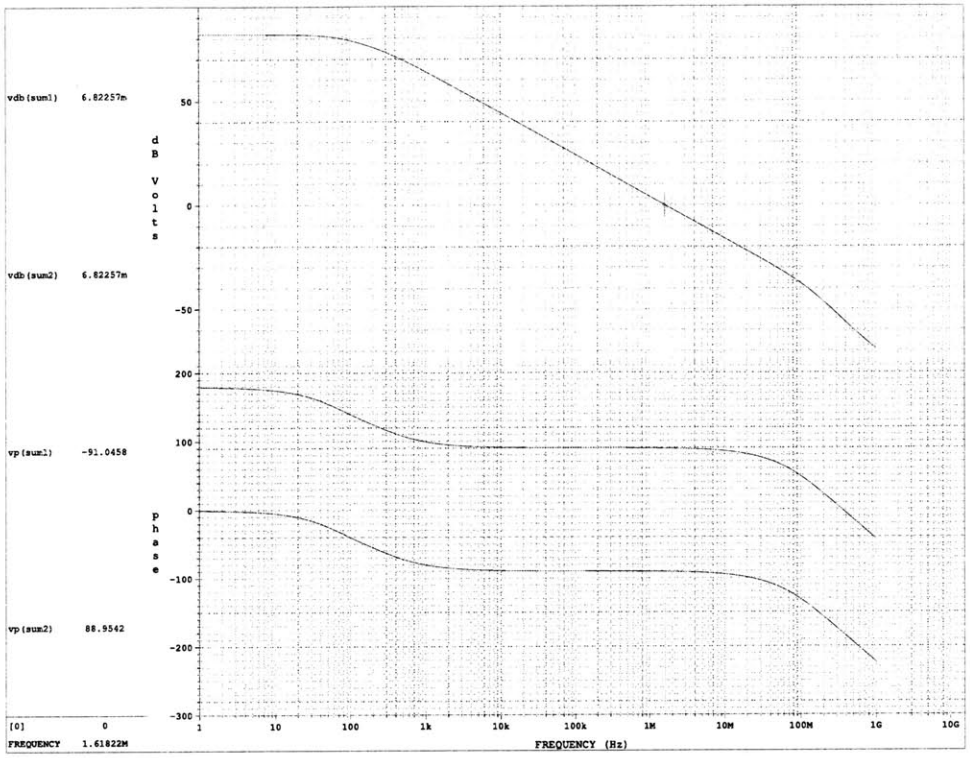


Figure 5-6: Loop gain.

5.2 Transient Simulations

5.2.1 Total Harmonic Distortion

Total Harmonic Distortion (THD) is mathematically defined as the square root of the sum of the squares of the second through ninth normalized harmonic expressed as a percent [1, p.467]:

$$THD = \frac{1}{R_1}\sqrt{\sum_{m=2}^{9} R_m^2}100 \tag{5.1}$$

Intuitively, THD is a measure of the linearity of the system. It tells us what undesired harmonics are appearing at the system output. In our case, the output should be a scaled version of the input so THD gives a way to measure how distorted or undistorted the output may be. The lower the THD, the more linear the system is and the closer the output appears to the scaled input.

Figure 5-7 shows a sample output plot of the system. It was produced using the simulation setup found in Figure A-12. A 100mVpp sine wave at 25kHz is applied to each input. We see that each output is a 2Vpp sine wave at 25kHz.

Table 5.2.1 gives THD values for various values of leakage current injected onto the summing nodes of the op-amp. The job of the DC stabilizer is to correct for these leakage currents to ensure that the op-amp does not saturate. We observe that the THD increases with leakage current. Even at levels of leakage well beyond the measured maximum of 20pA, the system still exhibits excellent linearity. OUTD is the differential output node of the amplifier, INM is the negative input terminal of the op-amp, and INP is the positive input terminal of the op-amp.

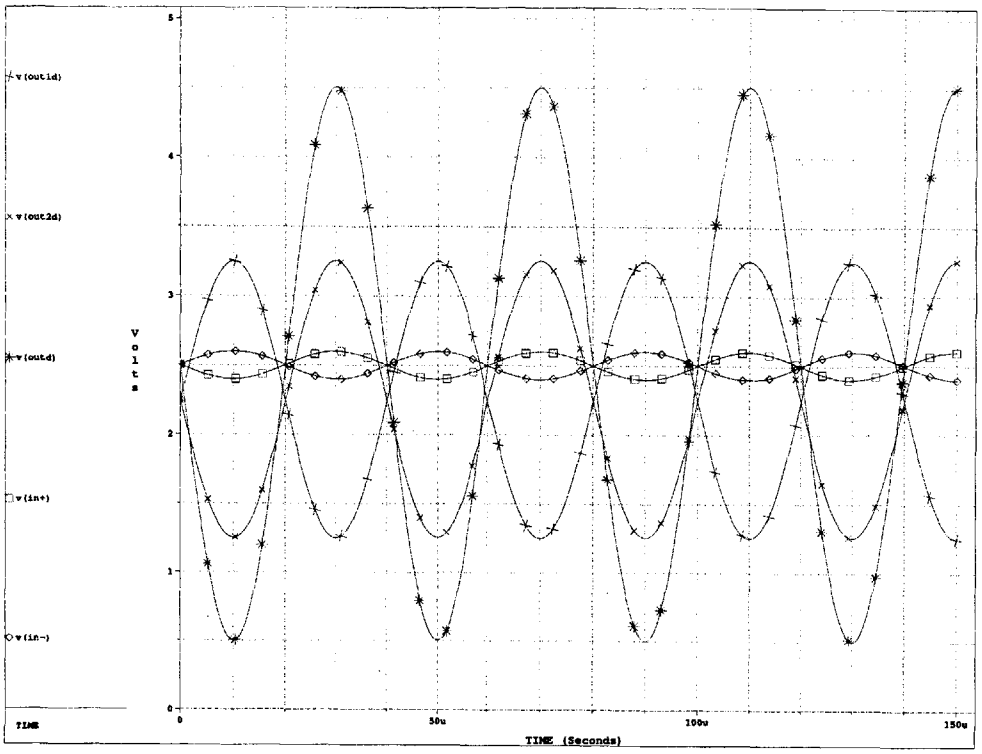


Figure 5-7: Results of a transient simulation.

Leakage	THD at output (pin OUTD)
0pA	-95dB
10pA on INM	-98dB
10pA on INP	-97dB
10pA on INM and INP	-111dB
20pA on INM	-100dB
20pA on INP	-100dB
20pA on INM and INP	-93dB
50pA on INM	-98dB
50pA on INP	-85dB
50pA on INM and INP	-85dB
100pA on INM	-101dB
100pA on INP	-79dB
100pA on INM and INP	-77dB
1nA on INM	-66dB
1nA on INP	-78dB
1nA on INM and INP	-66dB

Table 5.2: THD for various amounts of leakage current.

Chapter 6

Conclusion

Thermal insensitivity is critical for maintaining high precision performance in Draper Laboratory's High Performance Gyroscope. Recent studies at Draper Laboratory have shown that on-chip resistor ratios (which are conventionally used to set gains) offer inadequate tracking over temperature, making it difficult to achieve precision gain. Moreover, their high voltage coefficients lead to harmonic distortion.

In this thesis, a fully-differential amplifier with capacitive feedback is proposed. The superior ratio tracking and temperature and voltage coefficients of capacitors make them a more desirable device to use in the feedback path of an op-amp. However, using capacitors in the feedback path also requires additional circuitry to set the DC operating point of the op-amp input nodes so that the op-amp does not saturate.

The amplifier was designed for a low noise application. It uses the regulated cascode technique to provide increased gain without adding additional noise or cutting into the output swing. A continuous time common mode feedback network is implemented. The DC stabilizer was optimized for performance over the 8kHZ to 25kHz signal frequency range of Draper's gyroscope. Methods are discussed to decrease the noise contribution of the stabilizer and to increase its stability.

6.1 Future Recommendations

There are several areas of this thesis which can be pursued further.

- Op-Amp - Currently, the output signal swing just barely exceeds the 2.5Vpp on each output requirement. It is limited in part by the output stage of the op-amp, and in part by the input stage of the common mode feedback (CMFB) network. A class-AB output stage would allow the use of the resistive divider CMFB network without the level shifting source follower transistors. Furthermore, it would allow the output to be centered halfway between the rails. This method could be explored to increase the output swing.

- Operational Transconductance Amplifier (OTA) offset - The low g_m requirement of the OTA typically causes a substantial amount of offset to be present. Fortunately, offset is not very important in the gain amplifier because it is AC coupled to the following stage. However, if the DC stabilizer were to be used as a more general purpose device, a low offset OTA would be highly desirable.

- Using the DC stabilizer as a CMFB loop - Currently, the DC stabilizer and CMFB seem to serve similar purposes - namely to regulate the DC operating point of the output. The difference is one CMFB loop regulates both outputs at once while two separate DC stabilizers act on the outputs individually. It would be interesting to explore if the functionality of these separate loops could be combined.

Appendix A

Circuit Configurations

A.1 Final schematics

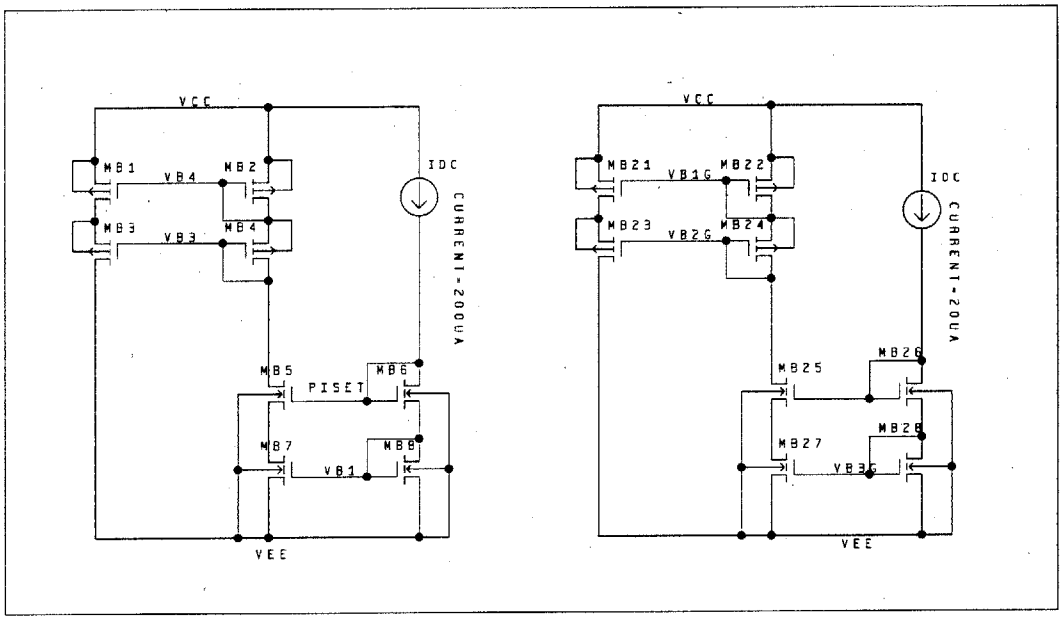


Figure A-1: Schematic for the biasing circuit.

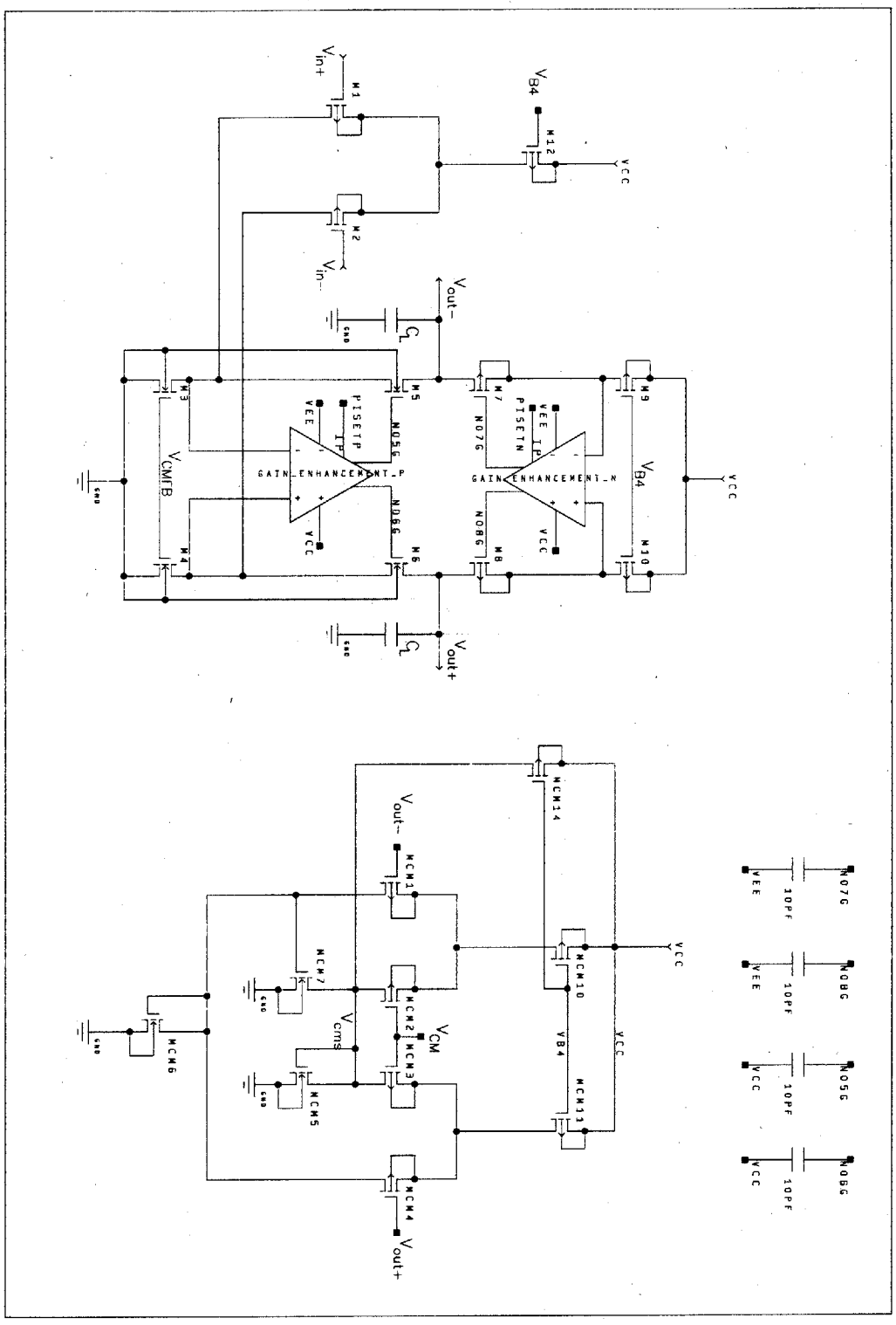


Figure A-2: Schematic for the fully-differential folded cascode op-amp.

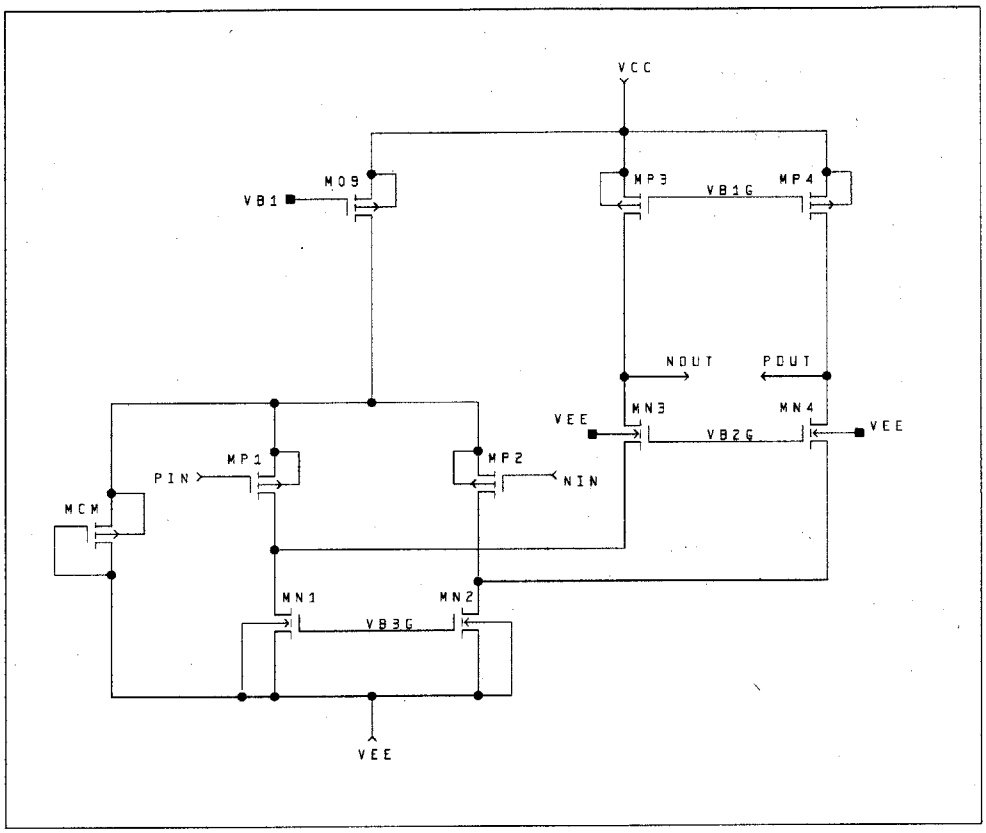


Figure A-3: Schematic for the PMOS input stage gain enhancement op-amp.

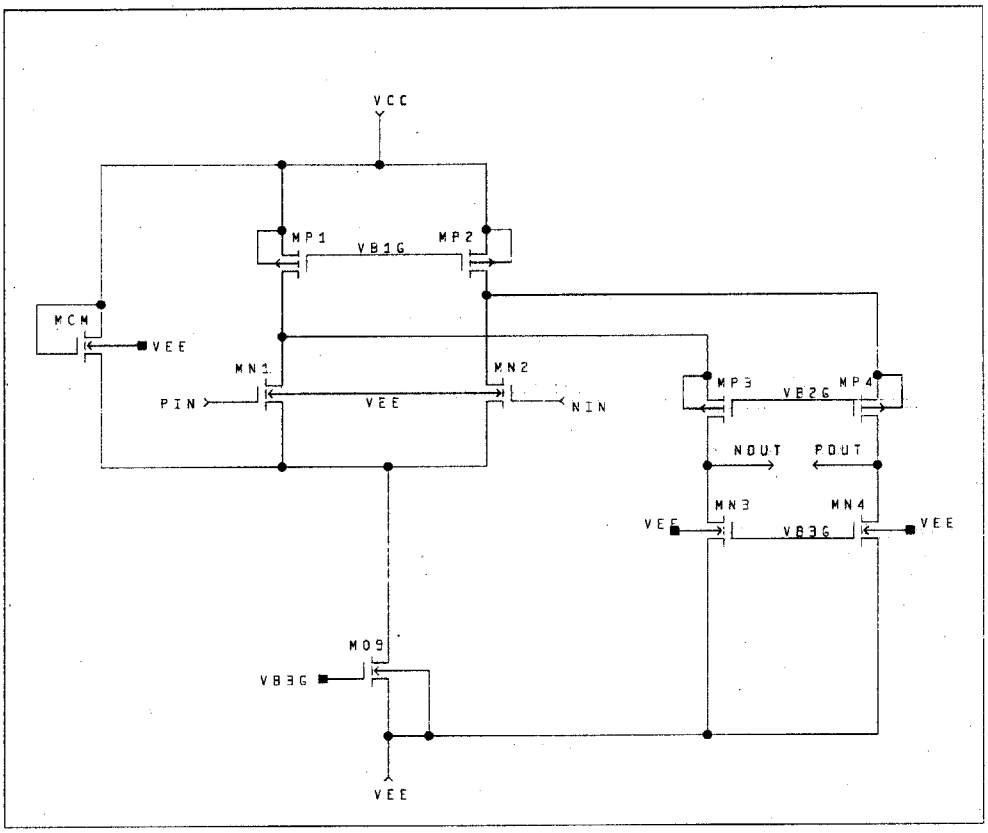


Figure A-4: Schematic for the NMOS input stage gain enhancement op-amp.

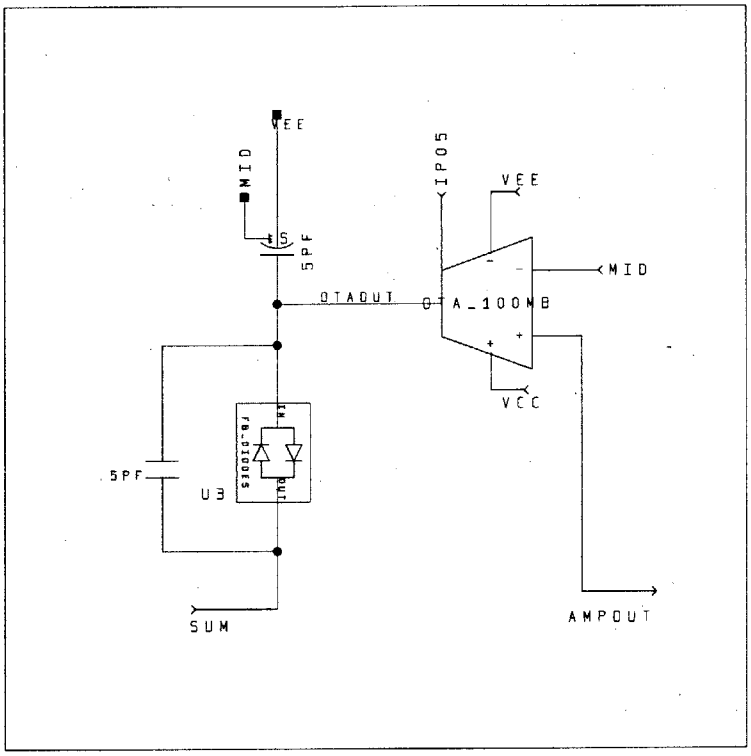


Figure A-5: Schematic for the DC stabilizer block.

A.1.1 Summary of Device Sizes

device	W (um)	L (um)
MB_1	300	3.6
MB_2	300	3.6
MB_3	300	3.6
MB_4	300	3.6
MB_5	200	1.8
MB_6	200	1.8
MB_7	200	1.8
MB_8	200	1.8
MB_{21}	50	0.6
MB_{22}	50	0.6
MB_{23}	50	0.6
MB_{24}	50	0.6
MB_{25}	36	0.6
MB_{26}	36	0.6
MB_{27}	36	0.6
MB_{28}	36	0.6

Table A.1: Devices sizes for the biasing networks

device	W (um)	L (um)
M_1	750	0.9
M_2	750	0.9
M_3	400	1.8
M_4	400	1.8
M_5	30	0.6
M_6	30	0.6
M_7	7	0.6
M_8	7	0.6
M_9	300	3.6
M_{10}	300	3.6

Table A.2: Devices sizes for the folded cascode op-amp

device	W (um)	L (um)
MCM_1	52	7
MCM_2	52	7
MCM_3	52	7
MCM_4	52	7
MCM_5	200	1.8
MCM_6	200	1.8
MCM_7	200	1.8
MCM_{10}	300	3.6
MCM_{11}	300	3.6
MCM_{14}	300	3.6

Table A.3: Devices sizes for the CMFB circuit

device	W (um)	L (um)
MN_1	18	0.6
MN_2	18	0.6
MP_1	50	0.6
MP_2	50	0.6
MP_3	10	0.6
MP_4	10	0.6
MN_3	36	0.6
MN_4	36	0.6
MCM	25	2.4

Table A.4: Devices sizes for the NMOS input gain enhancement op-amp

device	W (um)	L (um)
MP_1	50	0.6
MP_2	50	0.6
MN_1	36	0.6
MN_2	36	0.6
MN_3	9	0.6
MN_4	9	0.6
MP_3	16	0.6
MP_4	16	0.6
MCM	16	1.2

Table A.5: Devices sizes for the PMOS input gain enhancement op-amp

A.2 Circuit Configurations for Simulations

A.2.1 Folded Cascode Op-Amp

Open-Loop AC Simulation

In the real world, you cannot use the method in figure A-6 to measure the open-loop response of the op-amp. However, the method works very well in simulation. For frequencies less than $\frac{1}{2\pi\sqrt{LC}}$, the capacitor is an open and the inductor is a short, so we have the op-amp configured in a unity gain configuration. This allows the simulation to be able to converge to a DC operating point. At frequencies greater than $\frac{1}{2\pi\sqrt{LC}}$, the capacitor is a short and the inductor is open and the op-amp is running open-loop. The capacitor and inductor values are chosen to be very large such that $\frac{1}{2\pi\sqrt{LC}}$ is very small so that we can primarily look at the open-loop response of the op-amp.

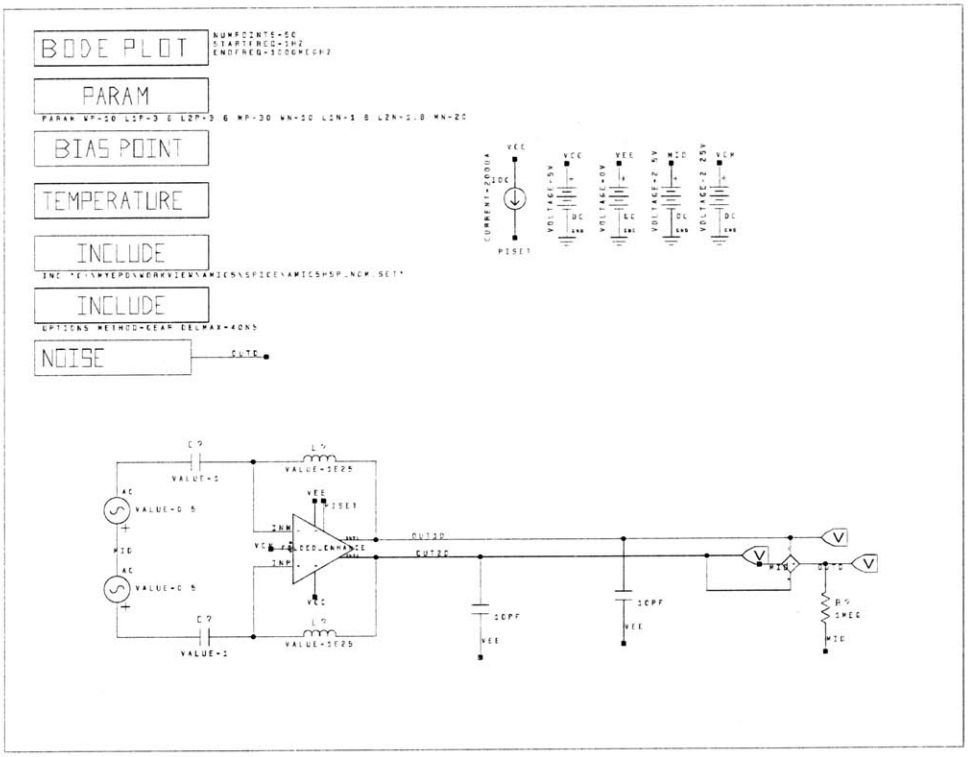


Figure A-6: Schematic file used to perform an open-loop AC simulation on the op-amp.

Common-Mode Rejection

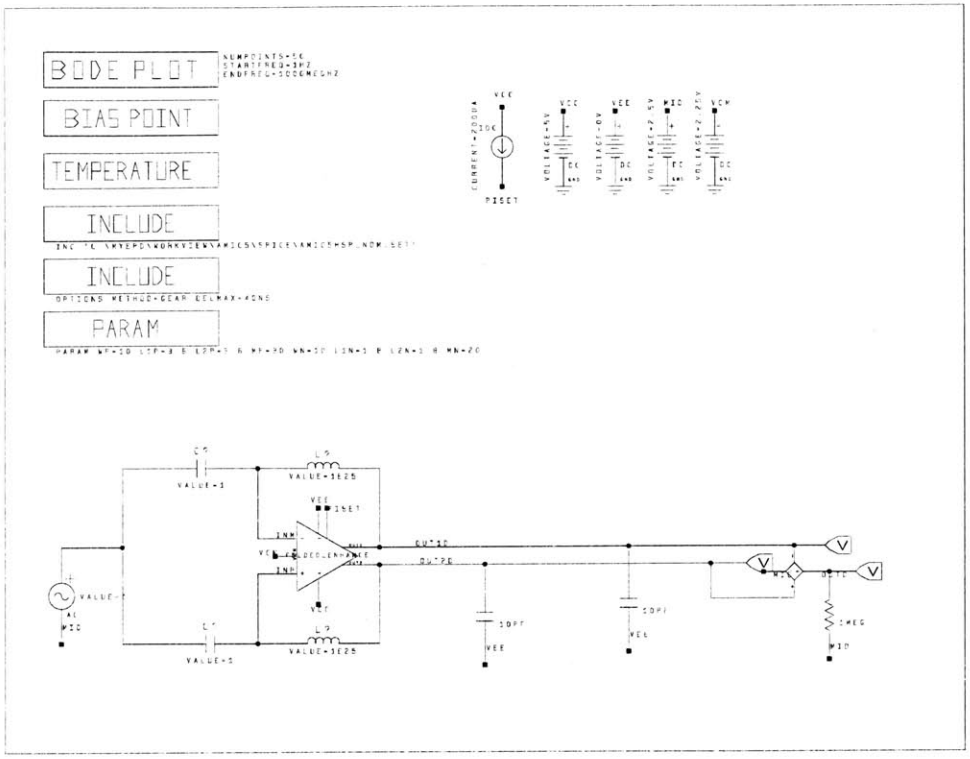
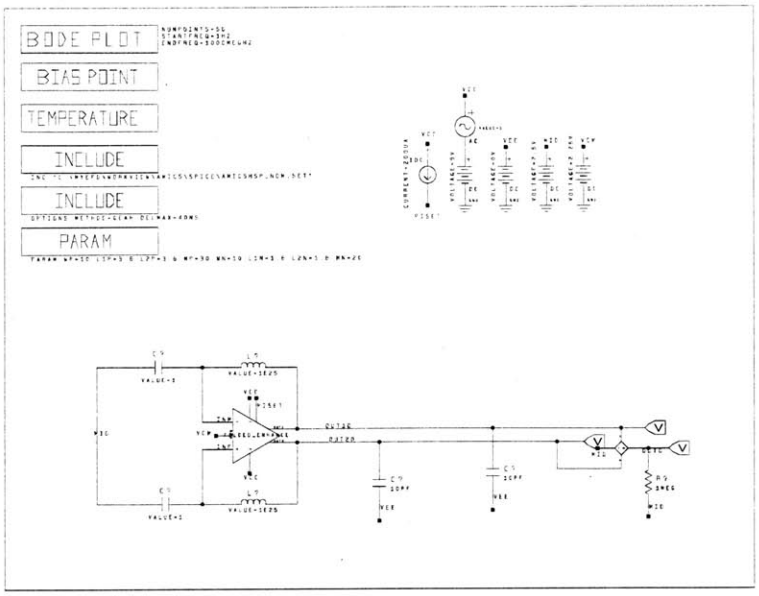
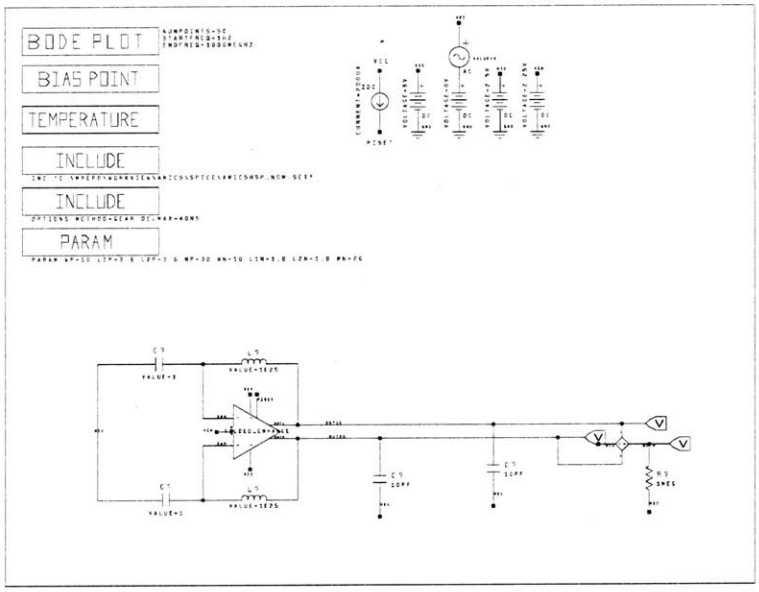


Figure A-7: Schematic file used to simulate the op-amp's common-mode rejection ratio.

Power-Supply Rejection



(a) PSRR+.



(b) PSRR-.

Figure A-8: Schematic used to simulate the op-amp's power-supply rejection ratio.

Output Swing

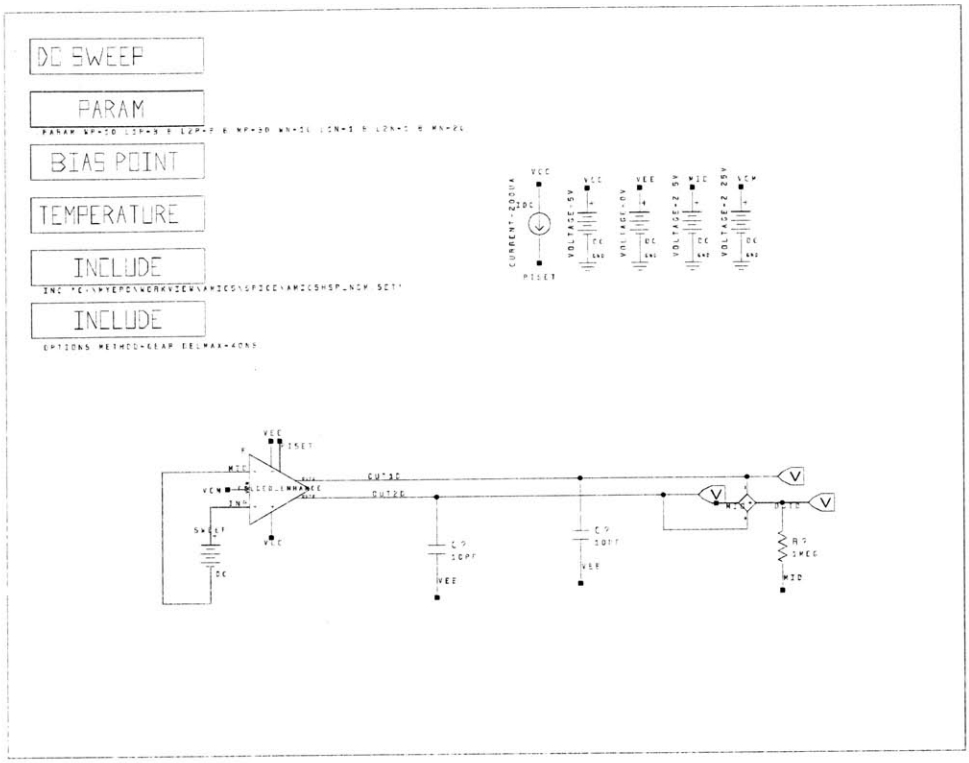


Figure A-9: Schematic file used to simulate the op-amp's output swing.

CMFB Open-Loop AC Simulation

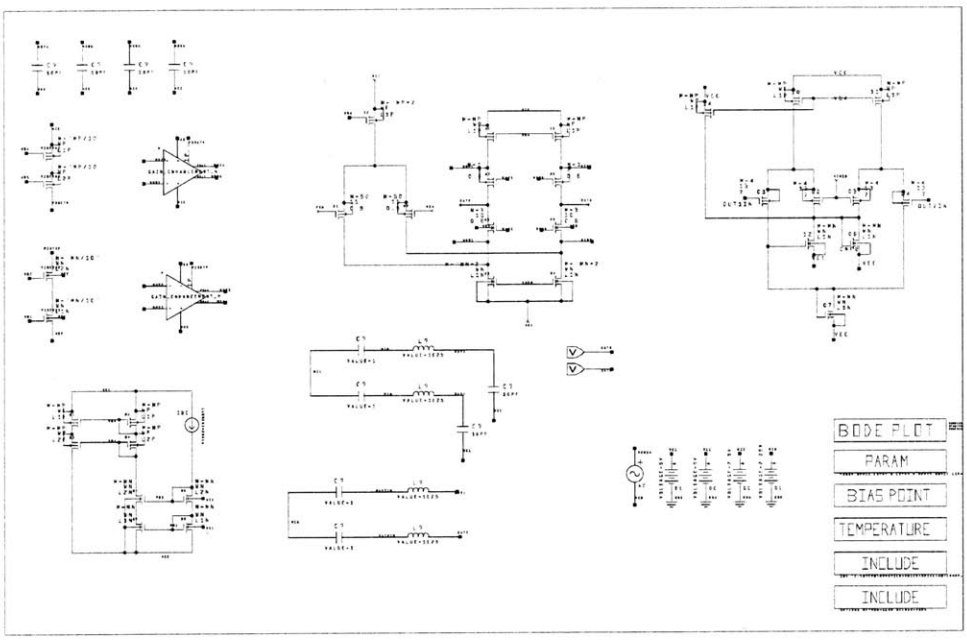


Figure A-10: Schematic file used to simulate the op-amp's CMFB loop

A.2.2 Gain Amplifier System

Convergence

It was often difficult to get spice to converge for the simulations performed on this circuit. Specifically, the simulator has trouble calculating the operating point for the input and output nodes of the op-amp. This is especially troublesome when current is injected into the input nodes, which causes the voltage on those nodes to rise. In order to achieve convergence, an initial condition file was created with the setup shown in figure A-11. The power supply is stepped from 0V to 5V, and the system DC operating points are saved after nodes have been allowed to settle. This simulation was performed for different values of leakage current and saved as .ic files to be loaded into subsequent simulations.

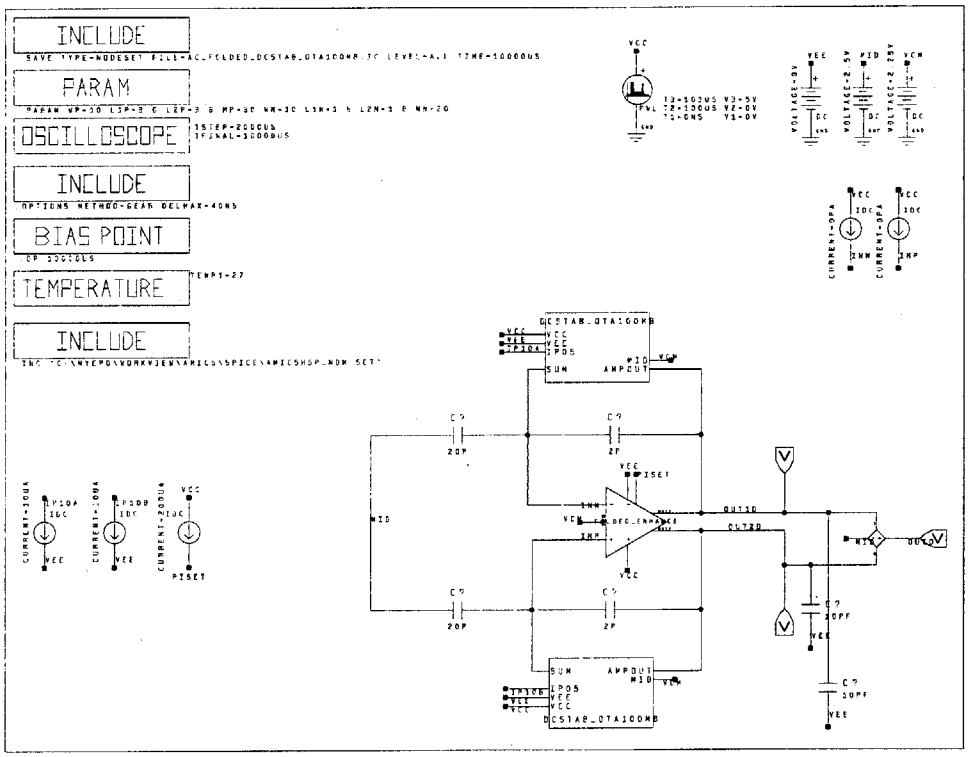


Figure A-11: Schematic file used to capture the operating points of the system at startup.

Total Harmonic Distortion

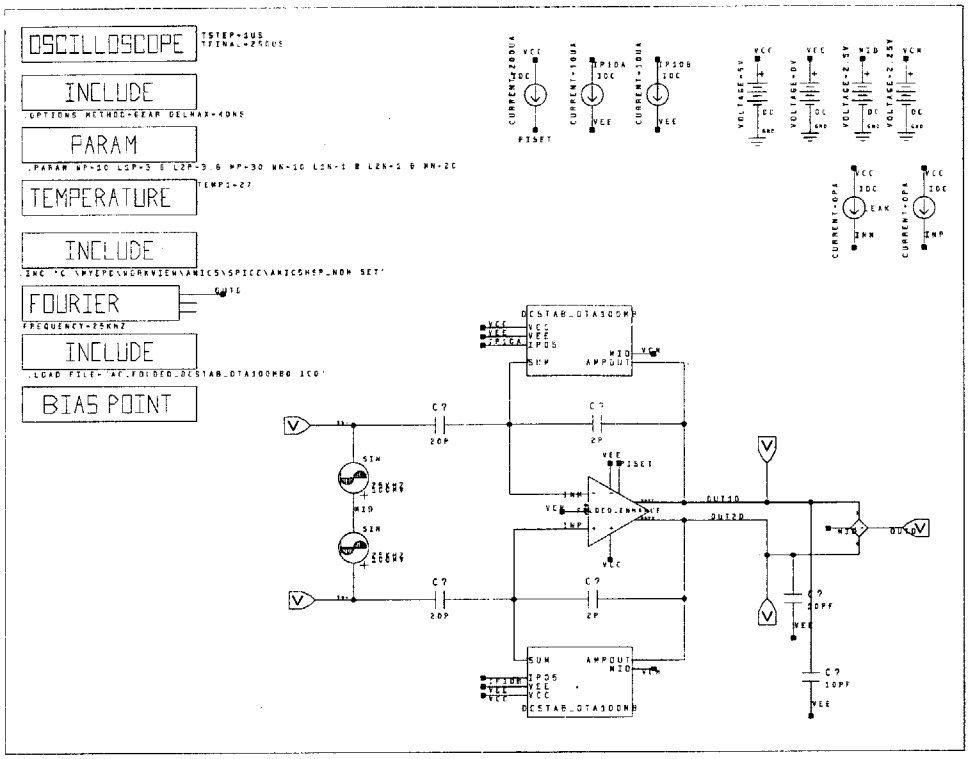


Figure A-12: Schematic file used to simulate the system's Total Harmonic Distortion (THD)

A.2.3 AC Response

The configuration shown in Figure A-13 was used to acquire the system's closed loop magnitude and phase, noise, and static phase shift for various values of leakage current injected into one of the summing nodes.

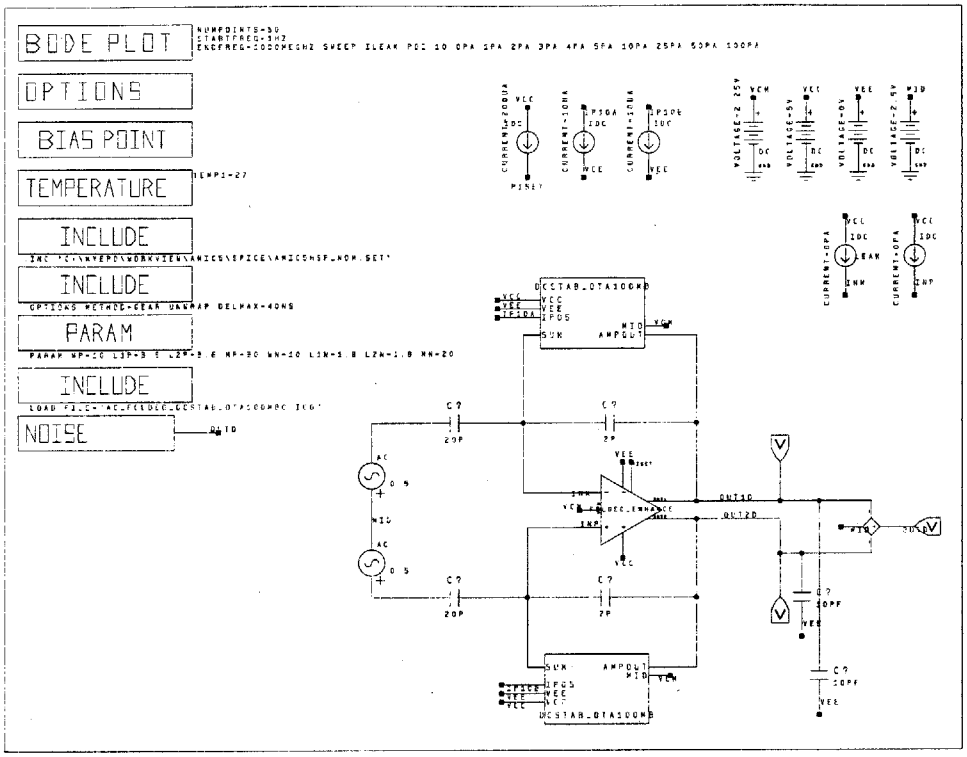


Figure A-13: Schematic file used to simulate the system's AC response.

A similar setup was used to simulate the system's dynamic phase shift and gain stability. Instead of sweeping leakage current, we swept temperature from -55°C to 105°C.

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