Abstract—A research synopsis is presented summarizing work with integration of Ge and III-V semiconductors and optical devices with Si. III-V GaAs/AlGaAs quantum well lasers and GaAs/AlGaAs optical circuit structures have been fabricated on Si using Ge/GeSi/Si virtual substrates. The lasers fabricated on bulk GaAs showed similar output characteristics as those on Si. The GaAs/AlGaAs lasers fabricated on Si emitted at 858nm and had room temperature cw lifetimes of ~4hours. Straight optical links integrating an LED emitter, waveguide and detector exhibited losses of approximately 144dB/cm. A process for fabrication of a novel CMOS-compatible platform that integrates III-V or Ge layers with Si is demonstrated. Thin Ge layers have been transferred from Ge/GeSi/Si virtual substrates to bulk Si utilizing wafer bonding and an epitaxial Si CMP layer to facilitate virtual substrate planarization. A unique CMP-less method for removal of Ge exfoliation damage induced by the Smart Cut™ process is also presented.

Index Terms—Chemo-mechanical planarization, GaAs/AlGaAs lasers, GeSi virtual substrates, optical circuit, wafer bonding

I. INTRODUCTION

The current challenge in monolithic integration of lattice-mismatched semiconductors with CMOS is fabrication of high-quality device layers on a Si substrate. Ge or GaAs films grown directly on Si have threading dislocation densities (TDD) as high as $10^6$ cm$^{-2}$ rendering the material useless for minority carrier device applications. However, using SiGe compositional grading [1] to pure Ge, we have realized high-quality (TDD=$10^6$ cm$^{-2}$) Ge and GaAs on a Si wafer. These virtual substrates have enabled us to fabricate the first compound semiconductor laser and the first optical circuit with a LED emitter, waveguide and detector monolithically integrated on a Si substrate. [2],[3],[4] However, more practical hetero-integration with CMOS requires removal of the thick (~10µm) underlying graded buffer. One solution is film transfer via wafer bonding. Traditional wafer bonding allows transfer of monocrystalline films of arbitrary composition, orientation, crystal structure and lattice constant to Si [5]. However, the differing coefficient of thermal expansion of Si relative to GaAs and Ge restricts the annealing temperature of the bonded pairs. In addition, the issue of wafer size mismatch limits their use to non-leading edge CMOS fabrication facilities. Using SiGe/Ge graded buffers, Ge or GaAs films can be transferred to Si from large diameter wafers while eliminating the large thermal strain energy that arises during bulk wafer bonding. Using virtual substrate wafer bonding, we have successfully demonstrated transfer of monocrystalline Ge films from Ge/GeSi/Si virtual substrates to Si with the aid of an epitaxial Si CMP layer and the Smart Cut™ process. Our current goal is to bring III-V/Ge integration with Si CMOS closer to reality by engineering a new platform to integrate III-V/Ge semiconductors with Si via wafer bonding SiGe/Ge virtual substrates. To date, we have successfully transferred monocrystalline Ge layers to Si from Ge virtual substrates using an epitaxial Si CMP layer and the Smart Cut™ process. [6] These engineered substrates will allow future fabrication of laser and optical circuit structures on a new, CMOS-friendly platform.

II. III-V OPTOELECTRONICS INTEGRATION USING GE/GESi/SI VIRTUAL SUBSTRATES

A. III-V on Si with Ge/GeSi/Si Virtual Substrates

Work in our group has demonstrated an effective approach to successful monolithic GaAs on Si integration making use of relaxed graded Ge/GeSi buffer layers. These GeSi virtual substrates are grown by hot-walled ultra-high vacuum chemical vapor deposition (UHVCVD) utilizing SiH$_4$ and GeH$_4$ as precursor gases. Surface threading dislocation densities in these samples have been measured at $1 \times 10^6$ cm$^{-2}$ using defect selective etching and plan-view transmission electron microscopy (TEM). Minority carrier lifetime measurements for GaAs films grown on GeSi buffers [7] have shown lifetimes comparable to bulk GaAs, indicating that the mean dislocation spacing has approached the minority carrier diffusion length in this optimized material.

Our GaAs films are grown via metalorganic chemical vapor deposition (MOCVD) utilizing a cold-walled reactor and TMGa and AsH$_3$ as precursors. TMIn, TMAl and PH$_3$ are also available for III-V growth. SiH$_4$ and DMZn are used as dopant sources.

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Semiconductor lasers remain a primary goal for GaAs on Si integration due to their proven usefulness in a wide variety of optoelectronic applications, but they also remain the most difficult devices to demonstrate successfully. As high-power minority carrier devices, semiconductor lasers are very sensitive to epitaxial material quality and crystal defect density. Early attempts to grow reliable GaAs lasers directly on Si using a wide variety of epitaxial techniques were unsuccessful [8]. More recently, alternative techniques involving hybrid wafer bonding [9], epitaxial lateral overgrowth [10] and migration-enhanced epitaxy [11] have been investigated for integration applications. To date, none of these techniques has demonstrated successful laser operation on an economical monolithically integrated platform. To contrast, the virtual substrate approach enjoys the benefits of economics of scalability to large diameter wafers while providing an effective technique for fabricating high-quality semiconductors on a lattice-mismatched substrate.

The laser structures we chose for these experiments were AlGaAs/GaAs graded index separate confinement heterostructure (GRINSCH) quantum-well devices. We also investigated the suitability of InGaAs/AlGaAs strained quantum well structures for integration but determined empirically that the mismatch in thermal expansion behavior between the Si substrate and the AlGaAs/InGaAs laser structure will lead to unwanted relaxation in the strained InGaAs layers.

Secondary ion mass spectroscopy (SIMS) measurements of the initial growths on Ge/GeSi/Si in Figure 1 shows uniform Ge contamination in all layers of the GaAs device at concentrations of $1 \times 10^{18}$ cm$^{-3}$ or higher. Ge is an amphoteric dopant in GaAs which compensates intentional doping and increases free-carrier absorption. To reduce the high Ge autodoping in our device layers, we completed a series of experiments to remove the chief sources of Ge in the growth sequence. With proper sample passivation and reactor cleaning via a two-step GaAs initiation sequence, we reduced Ge autodoping in the GaAs/AlGaAs device layers to undetectable limits ($<10^{16}$ cm$^{-3}$) and demonstrated high-quality films above the regrowth interface.

Cleaving smooth facet mirrors to form a laser cavity initially proved difficult on our offcut Ge/GeSi/Si substrates. Simulations and experiments showed a large dependence of laser threshold on facet roughness. After many experiments we determined that precise thinning of the substrate after laser growth and cleaving bars along the offcut direction allows acceptably smooth facet mirrors to be generated on a Ge/GeSi/Si substrate.

With optimized growth and fabrication steps, we demonstrated GaAs/AlGaAs lasers on Ge/GeSi/Si substrates for the first time. These devices operated cw at room temperature, with a threshold current density of 577 A/cm$^2$ and a differential quantum efficiency of 0.13 at a wavelength of 858 nm. Identical devices grown on bulk GaAs substrates showed equivalent thresholds and efficiencies. Side-by-side comparisons of lasers on Si to GaAs control devices have not been reported before to our knowledge. The light vs. current and current vs. voltage data for the devices on Ge/GeSi/Si and GaAs are shown in Figure 2.
Figure 2: Side-by-side light vs. current (a.) and current vs. voltage (b.) characteristics for identical GaAs/AlGaAs lasers grown on Ge/GeSi/Si and GaAs substrates.

The temperature sensitivity of both devices was also measured; the laser on Ge/GeSi/Si had a characteristic temperature $T_0$ of 61 K, while the device on GaAs had a measured $T_0$ of 128 K. The current-voltage characteristics of the device on Ge/GeSi/Si showed higher turn-on voltages and slightly larger series resistance at high current levels than the device on GaAs.

Reliability measurements were made at constant currents for both devices. The lasers on Ge/GeSi/Si showed gradual degradation, and fell below threshold after a ~4 hours. The device on GaAs showed no obvious degradation.

The higher series resistance and lower characteristic temperature (and thus lower lifetimes) for the laser on Ge/GeSi/Si indicates that this device will require further optimization. Improved contact geometries (to avoid contacting through the double junction at the GaAs/Ge interface) and facet coating may be useful in reducing turn-on and threshold current densities.

C. Monolithic Integration of III-V Optical Interconnects on Si Using GeSi Virtual Substrates

With the advances in VLSI technology through device processing and scaling, silicon integrated circuit performance has improved drastically in the past decade. However, in the future gains in performance through simple scaling will decrease as fundamental physical and economic limits are reached. Further improvements will most likely come from new architectures, better circuit designs, and the introduction of new technologies such as photonics, which includes the use of optical waveguides [12]. Additionally, electrical interconnection delay has already become a dominant factor in circuit performance [13]. If these electrical interconnections can be replaced by optical interconnections, power consumption will decrease and data transmission rates will increase [14, 15]. These advantages arise from the intrinsic properties of optics when compared to electronics. For example, optics is immune to electromagnetic interference, such as cross-talk, and provides voltage isolation between different parts of the chip [13]. Furthermore, electrical interconnects suffer from bandwidth penalties over distance that relate to the skin effect at high data rates [16].

Figure 3: Schematic diagram of the optical link structure on a GeSi substrate. The LED and detector (DET) have the same structure, making this a bi-directional link. The $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ layer acts as the waveguide and underneath it, the $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ layer acts as the waveguide cladding. On top of the waveguide is the $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ p+ electrode and the diodes.

The design of our optical link structure is shown in Figure 3. A GaAs PIN-LED acts as the light source and an identical PIN diode acts as the detector. These devices are then vertically coupled to an $\text{Al}_{0.15}\text{Ga}_{0.85}\text{As}$ waveguide that is clad with SiO$_2$ and $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$. The advantages of having a light source and detector of the exact structure include the ease of fabrication and the formation of a bi-directional link structure. We have chosen a vertical coupling scheme between the waveguide and both the emitter and detector in which both the emitter and the detector sit directly on top of the waveguide. Vertical coupled devices require no regrowth and no vertical guide-detector alignment. With this configuration, additional regrowth steps can be avoided, simplifying fabrication and processing. However, because of the weak guide-to-absorber coupling, the detector length needs to be increased in order to absorb all the waveguide light.

The various waveguide geometries examined are shown in Figure 4. Figure 4a) shows an optical link with a straight 10
μm waveguide, 4b) shows a link with a 5° Y-junction, and 4c) shows a link with a 30° bend in the waveguide. A straight 100μm waveguide (not shown) was also fabricated. The optical links were characterized using a HP 5145b semiconductor parameter analyzer, and a typical optical link diode I-V behavior is shown in Figure 5. The I-V curve shows good leakage current of 8x10⁻³ A/cm². However, these diodes have very high series resistance, likely resulting from the thin 7000Å p+ electrode. The p+ electrode was purposely kept thin to minimize the propagation distance of the light signals.

Figure 4: Fabricated optical lines of various geometries. a) 10μm waveguide link, b) waveguide with a 5° Y-junction, c) waveguide with bends.

Figure 5: I-V characteristics of a 100μm waveguide link. a) Plot of LED I-V curve with the detector response to LED emission. I-V plot shows good leakage current but very high series resistance. b) LED I-V curve.

III. TRANSFER OF LATTICE-MISMATCHED SEMICONDUCTORS FROM GE/GE/SI/SI VIRTUAL SUBSTRATES

The next task in bringing III-V integration with Si closer to reality is fabrication of a CMOS-compatible substrate. A major limitation of the virtual substrate is the thick graded buffer that separates the integrated semiconductor with the underlying Si wafer. The thermal stress induced by these layers causes extreme wafer bow making wafer handling and fine line lithography in state-of-the-art CMOS difficult. Furthermore, the large dimensional step between the Ge/III-V and Si layers further complicates lithography between the device layers.

Our method for fabricating a new platform for III-V integration with Si involves wafer bonding virtual substrates. This process involves transfer of a thin Ge or GaAs layer from a virtual substrate seed wafer to a Si handle wafer, thus eliminating the thick graded buffer in the final structure. Unlike hybrid wafer bonding where completed III-V devices are bonded to Si one device at a time, our approach enjoys the benefits of a scalable technology where lattice-mismatched materials are integrated monolithically on the wafer scale. Furthermore, since our films are transferred from virtual substrates fabricated on bulk Si, we are not limited to the small diameter when bonding bulk Ge or GaAs wafers.
A. Planarization of GeSi Virtual Substrates

As-grown virtual substrates have a crosshatch pattern characteristic to graded buffer growth. GeSi virtual substrates graded to Ge have a roughness of 10-15nm RMS (on a 25×25µm scale) as measured by atomic force microscopy. This roughness must be reduced by chemo-mechanical planarization (CMP) to less than 0.5nm prior to wafer bonding for efficient mating of the two surfaces.

SiGe films suffer reduced material removal rates (MRR) as the Ge fraction is increased. Figure 6 shows the dramatic decrease in MRR as the Ge fraction is increased past ~20%. Nonetheless, virtual substrates with a Ge fraction of up to x~0.6 can be readily planarized using a standard Si CMP process consisting of a KOH-stabilized colloidal silica slurry.

With pure Ge however, the MRR decreases to less than 0.5Å/sec, rendering planarization of Ge virtual substrates highly inefficient. Furthermore, the H2O component of the polishing slurry causes preferential etching around dislocations threading to the Ge surface. Figure 7 shows the combined effect of a slow polishing rate with anisotropic etching, resulting in surface pitting before complete removal of the crosshatch roughness.

![Figure 6](image)

Figure 6: Material removal rate for SiGe films CMPed with a KOH-stabilized slurry (Cabot Semisperse-25 (1:1), IC1000 pad).

![Figure 7](image)

Figure 7: AFM scan of a Ge virtual substrate after CMP using a KOH-stabilized slurry. Surface pits occur as a result of anisotropic etching of threading dislocations before crosshatch is completely removed.

B. Wafer Bonding and Film-transfer

A schematic of our film-transfer process is shown in Figure 9. After CMP, the virtual substrates were implanted with H2+ at 200keV to a dose of 4×10¹⁶ cm⁻² for the purpose of layer exfoliation. After chemical and O₂ plasma surface activation, the virtual substrate and Si handle wafers were bonded and annealed. Upon thermal activation, the H2+ implant induced fracture within the buried Ge resulting in the transferred structure shown in cross-section TEM in Figure 10. The extensive implant damage observed in the transferred Ge can

![Figure 8](image)

Figure 8: Cross-sectional TEM micrograph of an epitaxial Si planarization grown on a Ge virtual substrate.
be reduced by lowering the implant energy.

IV. NOVEL APPROACH FOR REMOVING EXFOLIATION DAMAGE FROM TRANSFERRED GE FILMS

A. Chemical Removal of Exfoliation Damage using Strained GeSi Etch-stop layers

The damaged layer induced by Si layer splitting is typically removed with a CMP step during fabrication of SOI wafers via the Smart Cut\textsuperscript{TM} process. However, traditional CMP is difficult to implement with Ge. Therefore, we have devised a novel technique for removal of layer exfoliation damage in Ge using chemical etching and a strained GeSi etch-stop layer.

This approach, illustrated in Figure 11, utilizes a thin, strained GeSi etch-stop layer grown into the Ge cap. The strained layer may be incorporated in-situ, during growth of the Ge virtual substrate or grown on bulk Ge wafers or previously fabricated virtual substrates. Using this modified seed wafer, the implant depth is tailored to penetrate the etch-stop layer (Fig. 11a) grown in the cap of the Ge virtual substrate. After wafer bonding (Fig. 11b) and layer exfoliation, the etch-stop layer is incorporated with the transferred film (Fig. 11c) allowing chemical removal of the damaged Ge surface (Fig. 11d). Use of an etch-stop layer also benefits from extremely precise dimensional control of the transferred Ge layer as the final thickness is controlled by epitaxy rather than hydrogen implant depth and subsequent CMP.

We have shown that Ge exhibits excellent etch selectivity relative to Ge\textsubscript{x}Si\textsubscript{1-x} for x<0.7 in I\textsubscript{2} and H\textsubscript{2}O\textsubscript{2}-based wet etch chemistries. Figure 12 shows the dramatic increase in Ge\textsubscript{x}Si\textsubscript{1-x} etch rate in mixtures of 1.7g KI:60mg I\textsubscript{2}:100mL H\textsubscript{2}O and undiluted H\textsubscript{2}O\textsubscript{2} with increasing Ge content. Although the I\textsubscript{2} etch shows better overall Ge:GeSi selectivity, we have chosen to use the H\textsubscript{2}O\textsubscript{2} etch because it does not contain alkali metals and is therefore more compatible with CMOS processing.
Figure 12: Etch rate for relaxed Ge<sub>x</sub>Si<sub>1-x</sub> films in I<sub>2</sub> (1.7g KI:60mg I<sub>2</sub>:100mL H<sub>2</sub>O) and undiluted H<sub>2</sub>O.

B. Growth and Characterization of Strained GeSi/Ge Etch-stop Test Structures

Etch test structures were grown on bulk Ge wafers to test the etch-stop behavior of strained Ge layers. The test structure consisted of a strained Ge<sub>x</sub>Si<sub>1-x</sub> (x=0.5,0.6) layer capped with relaxed Ge grown by hot-walled UHVCVD using SiH<sub>4</sub> and GeH<sub>4</sub> as precursor gases. Some structures were also capped with a thin layer of Si. The purpose of the Si cap is to protect the Ge surface from chemical cleaning prior to deposition of the CMP layer in the subsequent layer-transfer process. Figure 13 is a cross-sectional TEM micrograph showing a 110Å strained Ge<sub>0.6</sub>Si<sub>0.4</sub> layer buried under an 850Å relaxed Ge transfer layer and capped with 130 Å of Si.

Figure 13: XTEM of a strained Ge<sub>0.6</sub>Si<sub>0.4</sub> etch-stop layer on bulk Ge for etch-stop characterization. The Si cap protects the underlying Ge during chemical cleaning prior to CMP layer deposition.

The thickness of the strained etch-stop was kept below the critical thickness of a buried layer to prevent possible nucleation of threading dislocations during subsequent thermal processing. Since the critical thickness of a buried layer is twice that of surface layer, the growth temperature was reduced to 450°C in order to keep the film under metastable strain and prevent relaxation during growth.

Prior to etch selectivity experiments, the Si cap was stripped with a quick dip (~5sec) in 3:1KOH at 80°C. Figure 14 shows the excellent selectivity of a strained Ge<sub>0.6</sub>Si<sub>0.4</sub> layer to Ge. Such a layer can be used as a hard etch-stop for precise thickness control of the transferred Ge layer. The etch-stop layer remains intact after 30min of etching, or removal of nearly 1μm of Ge.

![Etch Rate Graph](image)

Figure 14: Etch selectivity characterization of Ge/Ge<sub>0.6</sub>Si<sub>0.4</sub> etch-stop on Ge. Etch-stop layer remains intact after 30min of etching.

V. CONCLUSIONS

Using Ge/Ge/Si virtual substrates we have demonstrated the first operating GaAs/AlGaAs lasers and optical circuit structures on a Si substrate. Motivated by the need to integrate these devices with Si CMOS, we have successfully demonstrated a general process for transferring lattice-mismatch semiconductors to large Si wafers using wafer bonding. Bonding virtual substrates is not limited to the comparatively small Ge and III-V wafers and is free of thermal stress issues that arise when bonding thermally mismatched bulk wafers. Fabricating thin semiconductor layers on Si is a more practical approach for integration of lattice mismatched semiconductors with CMOS.

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