Formation of Nanocrystalline Germanium via Oxidation of $Si_{0.54}Ge_{0.46}$ for Memory Device Applications

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Abstract—**In this work, we studied the possibility of synthesizing nanocrystalline germanium (Ge) via dry and wet oxidation of both amorphous and polycrystalline $Si_{0.54}Ge_{0.46}$ films. In dry oxidation, Ge was rejected from the growing SiO_2 forming a Ge-rich polycrystalline layer. As for wet oxidation, Ge was incorporated into the oxide, forming a layer of mixed oxide, $Si_xGe_{1-x}O_y$. Formation of nanocrystalline Ge was observed when the layer of $Si_xGe_{1-x}O_y$ was annealed in a N_2 ambient. We have fabricated a metal-insulator-semiconductor structure with nanocrystalline Ge embedded within the insulator layer to study its feasibility as a memory device.**

Index Terms—**Germanium nanocrystal, Silicon-Germanium, Oxidation.**

I. Introduction

Silicon-Germanium ($Si_{1-x}Ge_x$ or SiGe) alloy is an important material for future Si based devices as its preparation technique is completely compatible with existing CMOS logic technology. Devices using SiGe technology, such as heterojunction bipolar transistors, modulation-doped field-effect transistors, resonant tunnelling diodes and photodetectors, have been reported [1],[2]. With regards to the fabrication of these devices, there are quite a number of publications on the oxidation of $Si_{1-x}Ge_x$ films [3]-[11]. Among these studies, it is generally agreed that when the $Si_{1-x}Ge_x$ films were oxidized in a pure O_2 ambient (i.e., dry oxidation), a layer of Ge is formed due to the fact that Ge is being rejected from the growing oxide. Such an accumulation of Ge at the oxide interface usually results in a very high interface state density [10],[11]. On the other hand, when the $Si_{1-x}Ge_x$ ($x<0.5$) films were wet oxidized at lower temperatures (600-700˚C), the oxide layer contained a mixture of Si-O and Ge-O bonds. The Ge-O bonds can be broken when the oxide films were annealed in hydrogen, resulting in nanocrystalline Ge being embedded in the SiO_2 matrix [12],[13].

To date, there are very few reports on synthesizing nanocrystalline Ge by oxidizing and/or annealing $Si_{1-x}Ge_x$ films [12],[14] for practical applications. In all these reports, it was proposed that GeO_2, due to its large negative free energy, tends to decompose to Ge in the presence of a reducing agent; the O_2 being transferred to the reducing agent. Also due to the effect of the reducing agent, nanocrystalline Ge were formed in the SiO_2 matrix. So far, only King *et al.* [15] have fabricated non-volatile memory devices from a series of wet and dry oxidation of an epitaxial $Si_{1-x}Ge_x$ layer. The memory devices have exhibited very attractive write/erase and charge retention characteristics. It should be noted that the method of fabricating such memory devices required several rounds of oxidation processes.

In this work, our first aim is to carry out a systematic study on the possibility of obtaining nanocrystalline Ge by wet and dry oxidation of polycrystalline and amorphous $Si_{0.54}Ge_{0.46}$ films. We have recently reported memory effects in a metal-insulator-silicon (MIS) structure [16],[17]. The insulator layer consists of a rapid thermally grown tunnel oxide (RTO)/Ge nanocrystals+SiO_2/capping SiO_2 trilayer structure. The Ge nanocrystals were embedded in the SiO_2 network by rapid thermal annealing the co-sputtered Ge+SiO_2 films. The second objective of this work is to explore the possibility of obtaining memory devices by oxidizing the polycrystalline or amorphous $Si_{1-x}Ge_x$ films sandwiched between the RTO and capping SiO_2 layer.

II. Experiment

The substrates used for the deposition of $Si_{0.54}Ge_{0.46}$ films were p-type silicon wafers with (100) orientation and resistivity of 4-8 Ω cm. Prior to the deposition of the $Si_{0.54}Ge_{0.46}$ films, the wafers were cleaned in RCA I and II

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solutions and etched in 10% hydrofluoric acid. A thin (5nm) RTO layer was grown on the Si surface by rapid thermal oxidation. A layer of amorphous $Si_{0.54}Ge_{0.46}$ film of ~10nm was then sputtered in Ar on the RTO-Si substrate sample using an Anelva (SPH-210H) sputtering system. The sputtering was done at room temperature at 1 mTorr and rf power of 300 W. The sputtering target consisted of intrinsic (111) Ge pieces attached to a 4 inch n-doped Si wafer. The Ge pieces were evenly distributed across the wafer surface to ensure uniform distribution of Ge in the sputtered film. The Ge content was measured using the Rutherford backscattering technique. To prepare the polycrystalline $Si_{0.54}Ge_{0.46}$ films, the as-prepared amorphous films were annealed in a pure N_2 ambient at 800˚C for 6 hours [18]. The oxidation of the polycrystalline and amorphous films were carried out in a Tempress furnace. After the oxidation was completed, a layer of sputtered silicon oxide of ~50nm was deposited as the capping oxide layer.

We used the Raman spectra to monitor the progress of oxidation of our samples. The Raman experiments were performed with a Renishaw Raman spectrometer using the 514 nm line of an Ar ion laser operated at 10 mW. The Raman signal was detected in the backscattering configuration with a spectral resolution of 1.5 cm^{-1}. The transmission electron microscopy (TEM) experiments were carried out using a Philips CM300 field emission system with an operating voltage of 300 kV. The electrical characterization of the memory devices, i.e. the capacitance versus voltage (C-V) measurements, was performed using a HP4284A LCR analyzer.

III. Results and Discussion

A. Dry Oxidation

Figure 1 shows the Raman spectra of the as-prepared and oxidized films for different oxidation time. All the films were oxidized at 900˚C. As the as-prepared film was amorphous, its spectrum was featureless. It is interesting to note that when the film was oxidized for 2 to 4 minutes, two broad peaks at ~295 and 400 cm^{-1} that correspond to the Ge-Ge and Si-Ge bonds, respectively, are observed. The Si-Ge peak disappears and the Ge-Ge peak becomes sharper with further increase in the oxidation duration. Note that the Ge-Ge peak also shifts from 288 to 300 cm^{-1} when the oxidation duration was increased from 2 to 11 minutes.

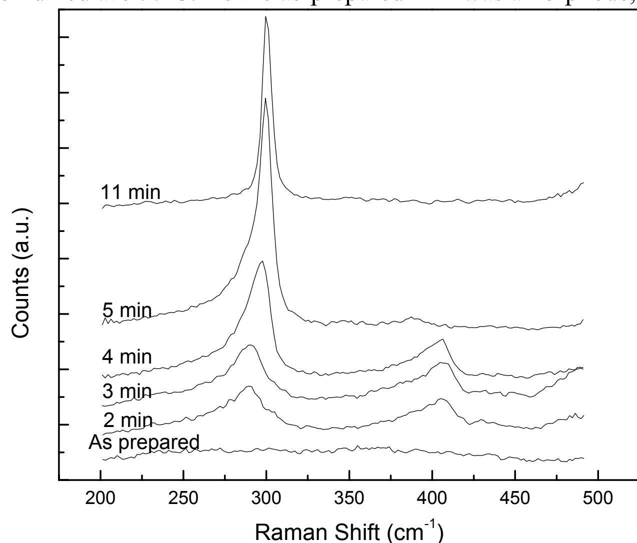


Fig. 1. Raman spectra taken from dry oxidation (900ºC) of amorphous $Si_{0.54}Ge_{0.46}$ for different durations.

We suggest that when the films were oxidized for 2 to 4 minutes, polycrystallization of the remaining un-oxidized $Si_{0.54}Ge_{0.46}$ film takes place due to the high oxidation temperature and this accounts for the appearance of the Si-Ge peak. Such a polycrystallization process was overtaken by the oxidation process with further increase in oxidation time. The reduction in the full-width-at-half maximum (FWHM) from 21.2 to 7.7 cm^{-1} and the shift to higher wavenumber from 288 to 300 cm^{-1} of the Ge-Ge peak means an improved crystallinity as oxidation time increased.

Figure 2 shows a TEM micrograph of a $Si_{0.54}Ge_{0.46}$ film oxidized at 900˚C for 11 minutes. A Ge layer with clear lattice fringes can be clearly seen between the RTO and the SiO_2 layer. This means that a Ge layer of good crystalline quality was formed after being oxidized in a pure O_2 ambient. No nanocrystalline Ge was observed via the dry oxidation of $Si_{0.54}Ge_{0.46}$ films. This is expected as Ge segregates out of the growing SiO_2 and due to the high concentration of Ge in the film, a layer of polycrystalline Ge is formed. However, a similar attempt by using lower Ge concentration ($Si_{0.7}Ge_{0.3}$) has shown formation of Ge-rich clusters [19].

We are currently studying the possibility of synthesizing nanocrystalline Ge from the layer of polycrystalline Ge by further oxidizing the layer and followed by a high temperature annealing process.

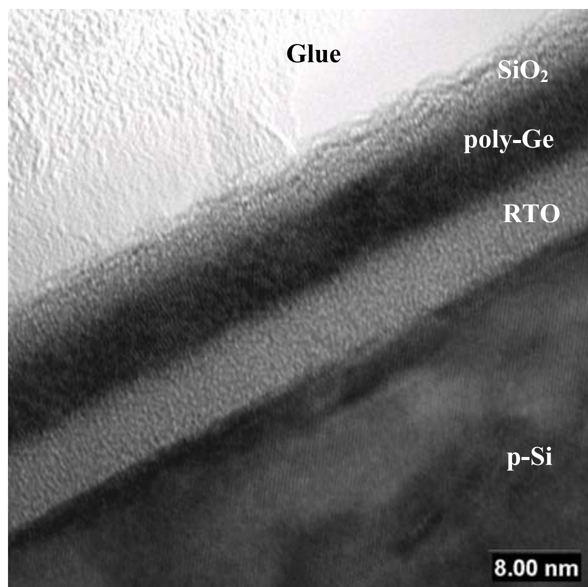


Fig. 2. Bright field cross-section TEM image of $Si_{0.54}Ge0_{.46}$ film oxidized at 900˚C for 11 minutes.

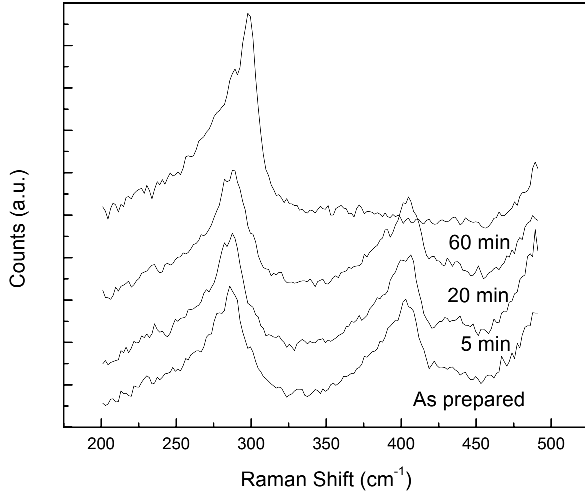


Fig. 3. Raman spectra taken from wet oxidized (600°C) polycrystalline $Si_{0.54}Ge_{0.46}$ for different oxidation durations.

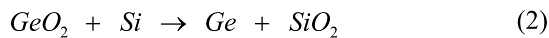
B. *Wet Oxidation*

Figure 3 shows the Raman spectra of the as-prepared polycrystalline films oxidized at 600˚C in a wet oxidation ambient for different durations. As the as-prepared film was polycrystalline, the peaks at ~288 and 400 cm^{-1} correspond to the Ge-Ge and Si-Ge bonds. These two peaks remain distinguishable when the film was oxidized up to 30 minutes. The Si-Ge peak, however, completely disappears when the film was oxidized for 60 minutes. This means that the polycrystalline films were completely oxidized in 60 minutes.

It is interesting to note that the Ge-Ge peak shifts from ~288 to 300 cm^{-1} as the oxidation duration increases from 0 to 60 minutes. There is also a sharpening of this peak as the oxidation duration increases as the FWHM of the peak reduces from 27.0 to 21.1 cm^{-1}. For films oxidized for 60 minutes, there exists a sharp peak at 300 cm^{-1} but with a pronounced shoulder at the lower wavenumber side. It should be noted that we have also observed the shift towards higher wavenumber and the sharpening of Ge-Ge peak with a pronounced left shoulder as annealing duration increased in our polycrystallization study of $Si_{1-x}Ge_x$ films [18].

Figure 4 shows a TEM micrograph of the polycrystalline $Si_{0.54}Ge_{0.46}$ films oxidized at 600˚C for 60 minutes. It is observed that an amorphous layer of $Si_xGe_{1-x}O_y$ is formed and the thickness of the layer (~10nm) corresponds to the initial thickness of the polycrystalline $Si_{0.54}Ge_{0.46}$ film. However, in Fig. 3, there still exists a Ge-Ge peak at ~300 cm^{-1}. This could be due the concurrent reduction of Ge-O bonds to elemental Ge through the following reactions:

$$GeO_2 + 2H_2 \rightarrow Ge + 2H_2O \qquad (1)$$



$$GeO_2 + Si \rightarrow Ge + SiO_2 \qquad (2)$$

C. *Formation of Nanocrystalline Ge*

Figure 5(a) shows the cross-section TEM micrograph of a polycrystalline sample that has been wet oxidized at 600°C for 60 minutes followed by a rapid thermal annealing at 1000°C for 300 seconds in a N_2 ambient. Nanocrystalline Ge was observed to have formed from the initial $Si_xGe_{1-x}O_y$ layer as shown in Fig. 4. The largest Ge nanocrystal is 20nm in diameter as shown in Fig. 5(b).

Taraschi *et al.* [14] have reported Ge nanocrystals in SiO_2 matrix after annealing in 100% or 6% H_2 ambient at 700 and 800˚C. The oxide was obtained from wet oxidation of epitaxial $Si_{0.75}Ge_{0.25}$ films. It was concluded that the process

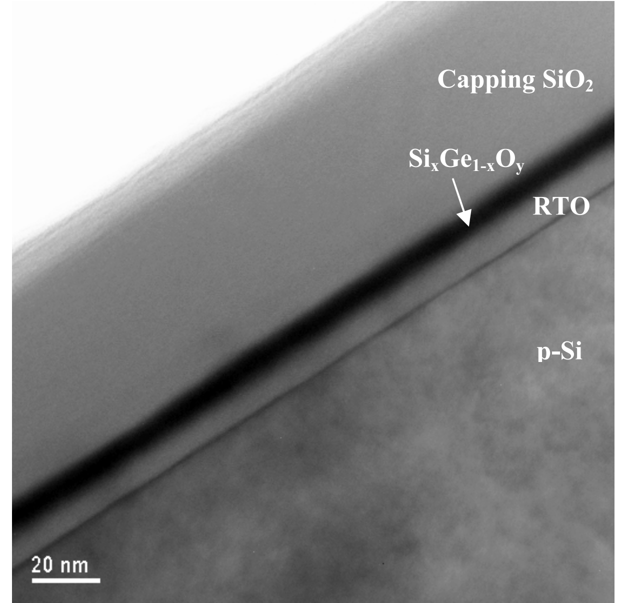


Fig. 4. Bright field cross-section TEM image of $Si_{0.54}Ge_{0.46}$ film wet oxidized at 600˚C for 60 minutes.

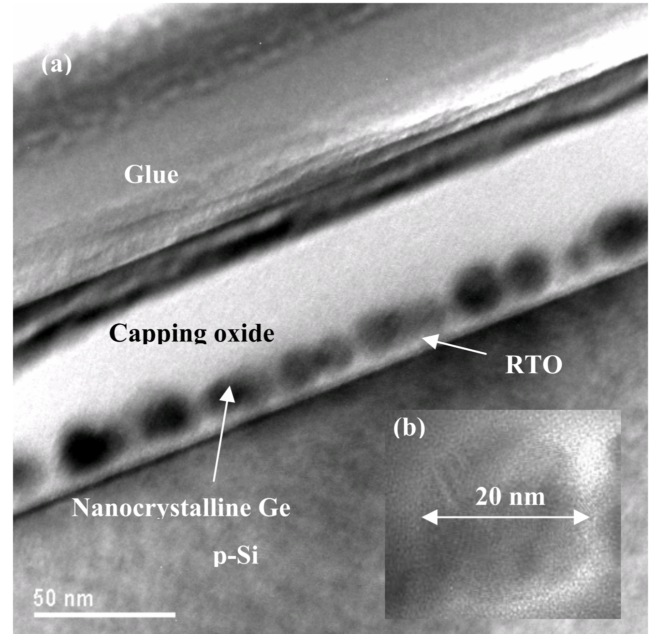


Fig. 5 (a). Bright field cross-section TEM micrograph of nanocrystalline Ge. (b) High resolution cross-section TEM micrograph of a nanocrystalline Ge.

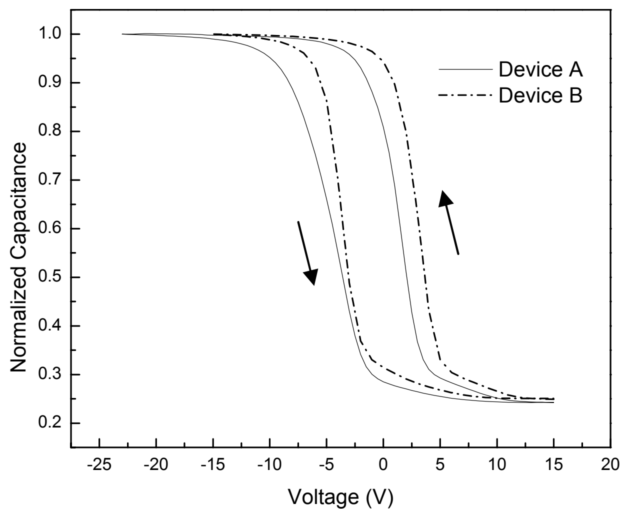


Fig. 6. Normalized Capacitance vs Voltage for devices fabricated via wet oxidation and annealing of polycrystalline and amorphous $Si_{0.54}Ge_{0.46}$.

kinetics for Ge nanocrystal formation comprise of the following steps: (i) GeO_2 reduction leading to formation of Ge, (ii) diffusion of Ge in the oxide matrix, (iii) formation of Ge clusters due to Ge-Ge collisions (nucleation) and (iv) ripening of nanocrystals. It is possible that these four steps can happen during annealing of our wet oxidized samples. Although we did not introduce any reducing agent (i.e. H_2) in our annealing process, there could have been trapped H_2 during the wet oxidation process. Furthermore, our annealing temperature of 1000°C is adequately high to break the Ge-O bonds without any reducing agent.

D. Charge Storage Capability

As we have succeeded in synthesizing nanocrystalline Ge in SiO_2 via the wet oxidation and subsequent annealing of polycrystalline $Si_{0.54}Ge_{0.46}$ films, we have fabricated devices with the same structure to investigate their memory characteristics. The thicknesses of the RTO layer, the as-deposited $Si_{0.54}Ge_{0.46}$ layer and the SiO_2 capping layer were 5 nm, 10 nm and 50 nm, respectively.

Figure 6 shows the normalized capacitance versus voltage (C-V) characteristics of MIS devices obtained from the wet oxidation and annealing of polycrystalline (Device A) and amorphous (Device B) $Si_{0.54}Ge_{0.46}$ films. A counter-clockwise C-V hysteresis was observed for both devices. The charge stored was estimated to be 1.5×10^{12} cm^{-2}.

We are currently examining differences in the electrical characteristics of devices A and B and the nanocrystalline Ge formed from rapid thermal annealing of oxidized polycrystalline and amorphous $Si_{0.54}Ge_{0.46}$ films. The results will be reported in a future publication.

IV. Conclusion

The difference of dry and wet oxidation of $Si_{0.54}Ge_{0.46}$ films was studied. Upon further annealing of the wet oxidized $Si_{0.54}Ge_{0.46}$ film, formation of nanocrystalline Ge was observed. We have also shown that a MIS device with nanocrystalline Ge embedded within the insulator was able to exhibit charge trapping phenomena.

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References

[1] Y.H. Xie, Mater. Sci. Eng., R. **25**, 89 (1999).
[2] D.J. Paul, Thin Solid Films **321**, 172 (1998).
[3] J. Eugene, F.K. LeGoues, V.P. Kesan, S.S. Iyer, and F.M. d'Huerle, Appl. Phys. Lett. **59**, 78 (1991).
[4] S.-G. Park, W.S. Liu, and M.-A. Nicolet, J. Appl. Phys. **75**, 1764 (1994).
[5] P.E. Hellberg, S.L. Zhang, F.M. d'Heurle and C.S. Petersson, J. Appl. Phys. **82**, 5773 (1997).
[6] C. Tetalin, X. Wallart, J.P. Nys, L. Vescan, and D.J. Gravestejin, J. Appl. Phys. **83**, 2842 (1998).
[7] Y.S. Lim, J.S. Jeong, J.Y. Lee, H.S. Kim, H.K. Kim, and D.W. Moon, Appl. Phys. Lett. **79**, 3606 (2001).
[8] S.-K. Kang, D.-H. Ko, K.C. Lee, T.W. Lee, Y.H. Lee, T.H. Ahn, I.S. Yeo, S.H. Oh, and C.G. Park, J. Vac. Sci. Tech. A **19**, 1617(2001).
[9] W.K. Choi, A. Natarajan, L.K. Bera, A.T.S. Wee and Y.J. Liu, J. Appl. Phys. **91**, 2443 (2002).
[10] D.K. Nayak, K. Kamjoo, J.S. Park, J.C.S. Woo, and K.L. Wang, Appl. Phys. Lett. **57**, 369 (1990).
[11] L.K. Bera, W.K. Choi, C.S. Tan, S.K. Samanta, and C.K. Maiti, IEEE Electron Device Lett. **22**, 387 (2001).
[12] W.S. Liu, J.S. Chen, M.-A. Nicolet, V. Arbet-Engeis, and K.L. Wang, Appl. Phys. Lett. **62**, 4444 (1992).
[13] D.C. Paine, C. Caragianis, T.Y. Kim, Y. Shigesato, and T. Ishahara, Appl. Phys. Lett. **62**, 2842 (1993).
[14] G. Taraschi, S. Saini, W.W. Fan, and E.A. Fitzgerald, Mater. Res. Soc. Symp. Proc. Xxx (2001).
[15] Y.-C. King, T.-J. King, and C. Hu, IEEE Trans. Electron Devices **48**, 696 (2001).
[16] W.K. Choi, W.K. Chim, C.L. Heng, L.W. Teo, V. Ho, V. Ng, D.A. Antoniadis, and E.A. Fitzgerald, Appl. Phys. Lett. **80**, 2014 (2002).
[17] L.W. Teo, W.K. Choi, W.K. Chim, V. Ho, C.M. Moey, M.S. Tay, C.L. Heng, Y. Lei, D.A. Antoniadis, and E.A. Fitzgerald, Appl. Phys. Lett. **81,** (2002).
[18] W.K. Choi, L.K. Teh, L.K. Bera, W.K. Chim, A.T.S. Wee, Y.X. Jie, J. Appl. Phys. **91**, 444 (2002).
[19] Tae-Sik Yoon, Ki-Bum Kim, J.Vac. Sci. Technol. B **20(2)** 2002.