Development of Monolithic CMOS-Compatible Visible Light Emitting Diode Arrays on Silicon

by

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Bachelor of Technology in Electrical Engineering
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Submitted to the Department of Materials Science and Engineering
in Partial Fulfillment of the Requirements for the Degree of

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ABSTRACT

The synergies associated with integrating Si-based CMOS ICs and III-V-material-based light-emitting devices are very exciting and such integration has been an active area of research and development for quite some time now. SiGe virtual substrate technology presents one way to integrate these materials. A more practical approach to monolithic integration based on the SiGe virtual substrate technology was followed in this work which involves wafer bonding and hydrogen-induced exfoliation to transfer a thin layer of device-quality silicon on top of the SiGe graded buffers to produce Silicon on Lattice Engineered Substrate (SOLES). SOLES wafers are suitable for the practical fabrication of SOI CMOS circuits and III-V-based photonic devices on a common silicon substrate. A novel monolithic CMOS compatible AlGaInP visible LED array on the SOLES platform was developed, fabricated and demonstrated in this work. The prototype array is an important breakthrough in the realization of the ultimate objective – monolithically integrated optical interconnects in high speed digital systems.

Thesis Supervisor: Eugene A. Fitzgerald
Title: Merton C. Flemings –SMA Professor of Materials Science and Engineering

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TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1

Introduction

1.1 Introduction and Scope of the thesis

Silicon (Si) has the advantage of well-developed process and design technologies, availability of large size, high quality, inexpensive substrates, and a stable native oxide suitable for dielectric passivation. All these features have contributed to silicon ICs dominating the electronics industry for the past four decades. Silicon, however, is an indirect bandgap semiconductor incapable of emitting light by conventional methods. The invention of III-V compound-based light-emitting devices in the 1960's ushered in a bright new era for the semiconductor industry. The possible synergies that can be developed by integrating Si-based ICs with III-V-compound-based light-emitting devices are very exciting and such integration has been an active area of research and development for quite some time now.

There are two general categories of optoelectronic integration, hybrid and monolithic. Whereas hybrid integration involves the alignment and mounting of pre-fabricated III-V components on a host Si IC, monolithic integration utilizes a common semiconductor substrate on which both optical and electrical devices are built. Monolithic integration has the advantage of economies of scale compared to hybrid integration which is labor intensive and volume-limited.

Though monolithic integration sounds attractive it is not easy. First, the lattice mismatch between Si and III-V compounds like GaAs makes the direct growth of good quality GaAs on Si impossible. One alternative to obtain low defect density GaAs on silicon is to use compositionally graded SiGe buffer layers to bridge the gap between Si and GaAs lattice constants (i.e., creating a virtual SiGe substrate, closely lattice-matched to GaAs). Though in theory the SiGe layers can be etched in selective areas to reveal the underlying silicon for CMOS circuit fabrication, the resulting 10 μm step makes high resolution lithography on this substrate difficult. Second, III-V materials traditionally use gold-based contact metallurgies. Gold is considered unsuitable for silicon electronic devices since it introduces deep level traps in the Si energy bandgap that deteriorate

device performance. Third, the introduction of III-V materials in Si fabrication facilities could compromise the standard CMOS process.

The aim of this work is to successfully integrate Si and III-V material by overcoming the above barriers. This is realized through the development of a CMOS-compatible visible light-emitting diode (LED) array on silicon. Chapter 2 presents the work done to develop a novel substrate called Silicon on Lattice Engineered Substrate (SOLES) that enables practical monolithic integration. For CMOS compatibility, the electrical properties of the n-GaAs/n-Ge, p^{++}-Si/p^{+}-GaAs and p^{++}-Ge/p^{+}-GaAs junctions are studied in Chapter 3. The design, fabrication and characterization of silicon-encapsulated AlGaInP LEDs on bulk GaAs and SiGe virtual substrates is described in Chapter 4. The LEDs are finally integrated on SOLES to make the prototype LED array as discussed in Chapter 5. Chapter 6 concludes the thesis and gives direction for future work.

The prototype LED array developed in this work is an important milestone towards achieving the ultimate objective – monolithically integrated optical interconnects inside digital systems. Before proceeding with the practical aspects of this work, a technology evaluation of board level optical interconnects is presented in the following, in order to identify useful applications.

1.2 Board Level (Chip to Chip) Optical Interconnects

For long distance communication links the use of optical signaling has been preferred to electric signaling because of lower attenuation for optical signals. These optical links employ serial communication in which the data bits are sent over a single communication channel (typically optical fiber) in a serial fashion one after the other.

However, using light for communication within the computer system is markedly different because attenuation over such short link lengths is not of major consequence. Rather the issues are latency, power consumption and bandwidth. Latency considerations favor board level (chip to chip) communication being parallel as opposed to serial. Though multi-channel electrical interconnects have so far been satisfactory, optical interconnects with low timing skew (important for parallel communication), low crosstalk and high bandwidth seem to be promising. A comparison of electrical and optical interconnects is performed in the next section.

1.3 Latency, Power and Bandwidth Comparison

The latency in an optical interconnect link is due to the latency associated with the laser driver and laser-diode at the transmission side and with the photo-diode, trans-impedance amplifier (TIA), signal level restorer at the receiver end, besides the time of flight (ToF) latency which is dictated by the speed of light.

Bitzaros *et al.* [1] found that for optical link lengths in the few-centimeter range latency is dominated by the interface circuits since the ToF latency is negligible for such short lengths. At board level lengths (10 cm) the ToF latency dominates the link latency of optical interconnects. For electrical interconnects, relatively wide and thick wires available at the board level can result in latencies close to ToF. Thus, optical and electrical interconnects can have comparable latencies at the board level.

"Optoelectronic links can be superior to electrical links in terms of power dissipation in highly parallel interconnections. When multiple channels of optoelectronic links are considered, the biasing circuitries of the TIA and laser driver can be common for all channels. As a result, in multiple-channel optoelectronic links, the total power consumption is not a direct multiple of the single-channel consumption, as is the case with electrical interconnects. Therefore, the optoelectronic links can be more efficient than electrical interconnects in multi-channel links"[1]. However, reducing the voltage swing of electrical interconnects can make the energy dissipation of electrical and optical interconnects comparable [2].

Though latency and power consumption do not provide any great advantage to favor the use of optical interconnects at the board level, the substantially large bandwidth is a factor in their favor. According to Naeemi *et al.* "While bandwidth of an electrical interconnect is determined by its length and cross-sectional dimensions, the bandwidth of a typical board level waveguide is independent of its physical dimensions, and is determined by the driver and receiver. To have a fair comparison between electrical and optical interconnects, bandwidth and interconnect density should be considered simultaneously. This means that data flux density (defined as bandwidth per unit width of interconnect) should be compared. A large data flux density is desirable so as to transfer as many bits per second as possible using a constant routing area." [2].

Naeemi *et al.* [2] identify a partition length beyond which optical waveguides can offer a larger data flux density or larger aggregate inter-chip bandwidth in comparison to electrical interconnects when constrained by a fixed routing area. In their analysis, it is assumed that optical drivers and receivers will eventually mature and become comparable with their electrical counterparts in terms of power, size, and cost. Their comparison, therefore, emphasizes the interconnect media, or "wires versus waveguides," rather than the interface circuits.

Figure 1.1 plots the partition length for different technology nodes. As technology advances, the partition length decreases, because of reduction in linewidth and increase in operating frequency. It is seen that the partition length is expected to reduce to 10 cm by the year 2008, indicating that optical interconnects will then provide a higher bandwidth flux than electrical interconnects at the board level.

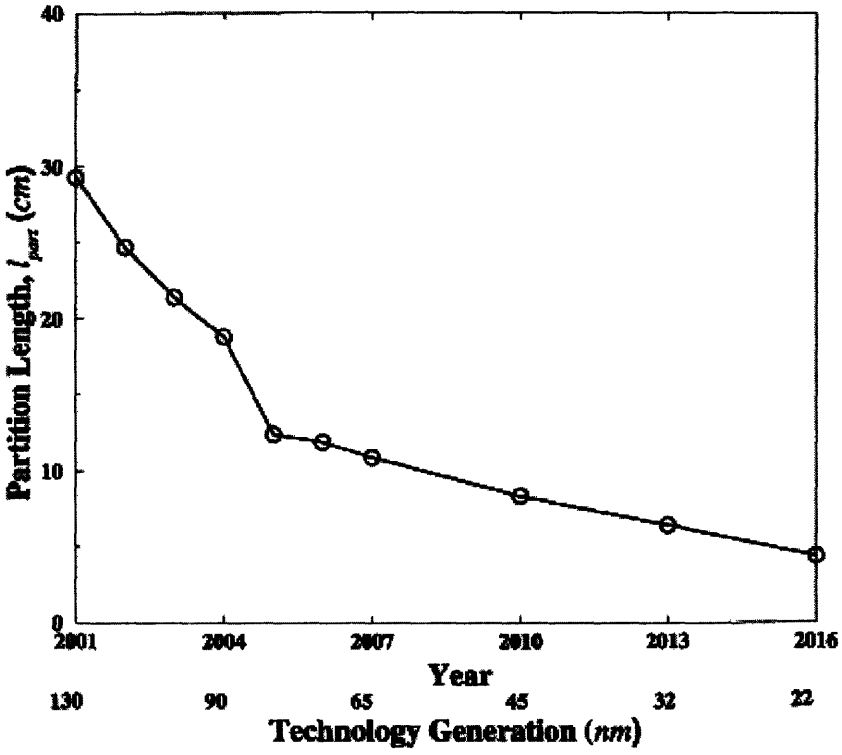


Figure 1.1 Partition length vs. technology generation. [2]

In summary, comparison of electrical and optical interconnects has shown that optical interconnect technology is attractive at the board level due to its capability of

sustaining a high bandwidth density. Signal latency and power consumption are not compelling factors in favor of optical interconnects.

1.4 Optical Interconnects in Monoprocessor and Symmetric Multiprocessor machines

Though optical interconnects have revolutionized telecommunications they have hardly found applications within computer systems. According to Collete *et al.*[3] the reason is that optics does not shorten the access time to the memory (Memory Access Latency, MAL), which is the most crucial issue for stored-program machines. Latency is the critical factor when considering the interactions between the memory and the processor, more than bandwidth, because the processor exchanges very short bursts of information with the memory.

Collete *et al.* argue that "the performance of microprocessors has increased much more rapidly than that of memory systems. Processor speeds have doubled every few years, while the speed of dynamic random access memory (DRAM) has increased only marginally. This means that the time needed by the processor to fetch instructions or data from the main memory has increased compared with the processor cycle time. The speed of DRAM is limited by the circuits used for detecting the stored charge on a memory cell. There is a trade-off between the size of the memory and the rate at which the stored charge can be sensed. In monoprocessor machines the dominant term to the MAL is the intrinsic MAL, which depends on the internal architecture and on the technology of the DRAM. Thus the high bandwidth provided by optical interconnects cannot help improve the performance of monoprocessor machines."[3]

"In order to enhance computer performance several processors can be connected through an interconnection network. In such multiprocessor machines, the additional terms of coherence latency and contention latency contribute to the MAL. In order to maintain the coherence of the caches, coherence messages need to be broadcast through the communication network. This slows down the memory access and adds coherence latency to the MAL. Coherence latency strongly depends on the network topology. Snooping protocols for maintaining cache coherence, usually implemented with bus topology, are much simpler and faster than directory-based protocols that have to be implemented in distributed networks."[3].

"In symmetric multiprocessor designs a single address bus is shared (this enables snooping to maintain cache coherence) among the processors and memory controllers. If the address bus is busy when a processor needs data, that processor must wait for its turn, causing contention latency. Therefore, there is only a marginal improvement when more processors or faster processors are added to a system without increasing the address bus bandwidth. Increasing the bus operation frequency is complicated because the bus being used is a multipoint electric line."

"High bandwidth optical interconnects offer an alternative solution. Address bus speed can be increased using optical interconnects without the effects of crosstalk, impedance mismatch and signal degradation encountered in electrical solutions. Parallel transmission through optical lines is almost skew-free in the gigahertz domain for transmission over a few tens of centimeters thus simplifying data recovery. However there are limitations to the use of optical interconnects. Increasing the bus operating frequency will also require each cache controller to check and update its directory at the bus operation frequency. Speeding up the bus will also generate a physical integration issue because the bus length has to be limited to make sure that the optical signals can be stationary within a single bus period. The light propagation velocity (c = 20 cm/ns) requires the bus to be shorter than 10 cm at 2 GHz, shorter than 5 cm at 4 GHz, etc."[3]. Thus optical buses do not seem to be a solution to the MAL in symmetric multi-processor machines. New computer architectures will have to be developed to attain any benefit.

1.5 Optical Interconnects in dedicated processors

The most viable application of optical interconnects at present seems to be in dedicated optoelectronic processors. Collete *et al.* declare that "Dedicated processors do not generally execute stored programs unlike general purpose monoprocessors or multiprocessors. They are designed for a specific task, involving the processing of optical information. The MAL is no longer a problem as there is no memory or almost no exchange with the memory. Some examples of applications for dedicated processors are image-processing-primitive operations (Fourier transformation, 2-D convolution and correlation, and dot-product and dot-matrix multiplications)" [3].

In summary, optical interconnects can provide huge bandwidth. But this cannot be exploited in monoprocessor machines. In multiprocessor machines, a high bandwidth will

decrease the MAL but a new computer architecture has to be employed to attain this benefit. Thus within the constraints of the present architecture the most promising applications of optical interconnects seem to be in dedicated microprocessors.

CHAPTER 2

Development of the SOLES Integration Platform

2.1 Introduction

In order to implement optical interconnects in digital systems, optoelectronic integrated circuits (OEICs) must be developed. OEICs depend on the integration of electrical devices such as transistors which are typically fabricated in silicon and optical devices that are fabricated in compound semiconductors such as GaAs. This integration can be achieved by monolithic or hybrid means. Commercial devices till date have relied upon costly hybrid mounting schemes. Historically monolithic integration has been attempted via the epitaxial growth of GaAs directly on Si, but the nearly 4% lattice mismatch between Si and GaAs results in defect densities on the order of 10^{10} cm^{-2} in the GaAs epilayers, rendering the material useless for device applications.

2.2 Monolithic Integration via the SiGe Graded Buffer

Monolithic integration requires growth of low defect density III-V material on a Si substrate. Si_xGe_{1-x} alloys present one way to bridge the lattice mismatch between Si and GaAs by acting as a template for lattice matched GaAs growth. The lattice parameter of the Si_xGe_{1-x} alloy can be engineered by varying the composition 'x' of the alloy from 1 to 0 thereby starting with 100% Si at the bottom and obtaining 100% Ge on top. The resulting Ge cap is closely lattice matched to GaAs.

However, the Ge cap obtained by this method is not defect-free. As the thickness of a mismatched film increases, the misfit strain energy stored in the film increases. At a certain film thickness, termed the critical thickness, misfit dislocations are nucleated to relieve the strain associated with lattice mismatch. Dislocations must terminate outside the epitaxial film so the dislocations have to either terminate at the wafer edge or on the film surface. Those dislocations that end on the film surface have to "thread" through the film thickness and hence are termed threading dislocations. Figure 2.1(a) shows misfit and threading dislocations. High densities of threading dislocations (10^{10} cm^{-2}) can seriously degrade the efficiency of a semiconductor device by acting as non-radiative recombination centers for electrons and holes.

One way to control the threading dislocation density in the SiGe graded buffer to the desired order of 10^6 cm^{-2} is to reduce their nucleation. This is achieved by maintaining a low strain state during growth. Thus, the highly mismatched Ge target layer is approached gradually via the deposition of many intermediate layers of low lattice mismatch. Each layer in the buffer relaxes to its intermediate lattice constant, and a low strain state is maintained throughout, minimizing dislocation nucleation. Additionally, threading dislocations from previous layers are "recycled" at each subsequent interface as they glide to create misfit dislocations. A high growth temperature is employed to maximize the glide length of each threading dislocation at each interface, obviating the need for additional dislocation nucleation for strain relief. Figure 2.1(b) illustrates the recycling of threading dislocations in the graded buffer.

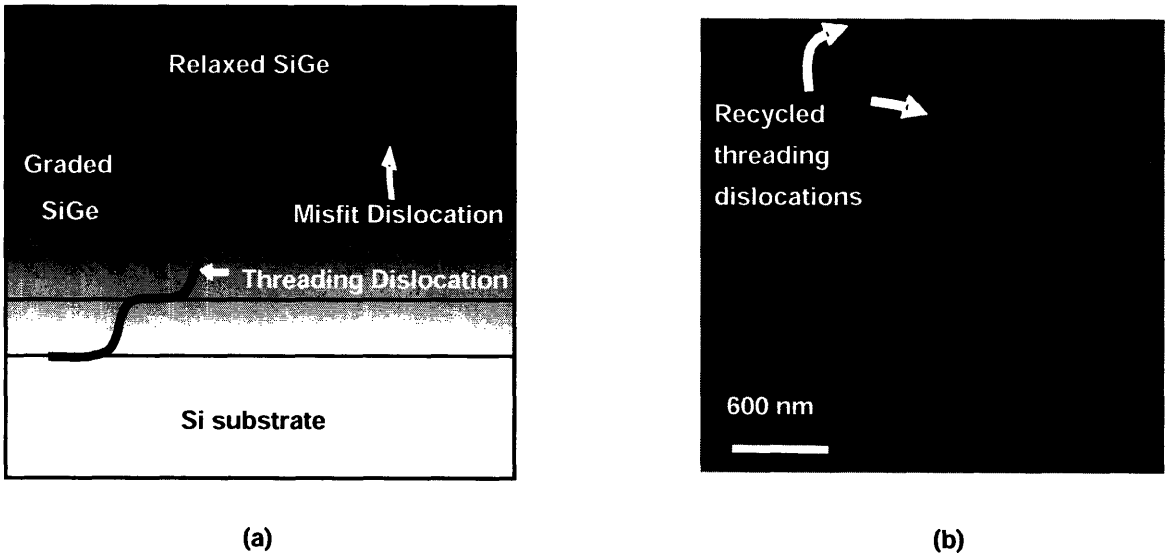


Figure 2.1: (a) Schematic of compositionally graded buffer. (b) Cross-sectional transmission electron micrograph (TEM) of a compositionally graded SiGe region showing recycling of threading dislocations. Image courtesy Thomas Langdo.

A cross-sectional transmission electron microscope (TEM) image of a SiGe graded buffer on Si with a 1 μm Ge cap suitable for III-V integration is shown in Figure 2.2. The batch process nature of the ultra high vacuum chemical vapor deposition (UHVCVD) system permits high-quality Ge/SiGe/Si graded buffer growths on multiple 4" or 6" Si substrates with grading rates of 10% Ge per μm and growth temperatures between 550 °C-800 °C.

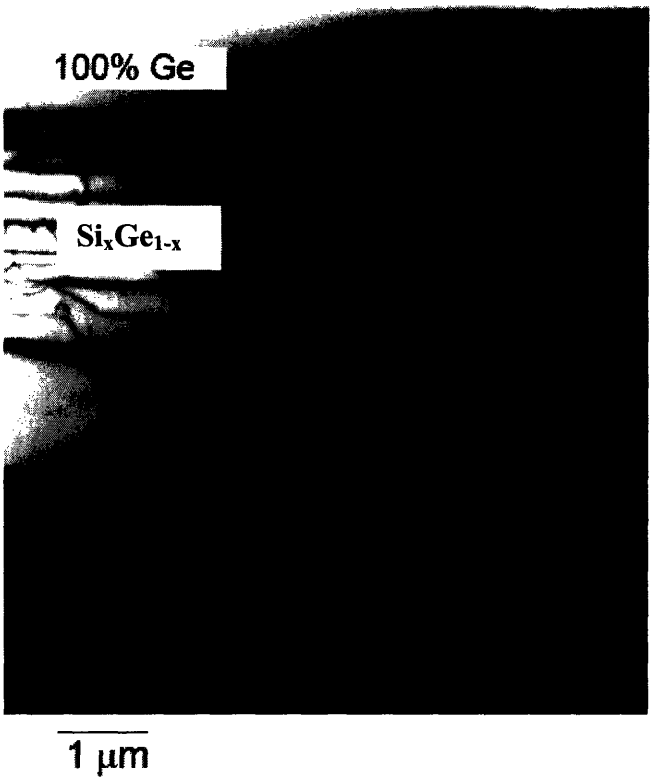


Figure 2.2:Cross-sectional TEM image of Ge capped Si_xGe_{1-x} graded buffer grown in the Fitzgerald group UHVCVD reactor.

2.3 Silicon on Lattice Engineered Substrate (SOLES)

Though the SiGe graded buffer can bring GaAs and Si to the same wafer, it is not a practical way for achieving monolithic integration. A grading rate of 10% Ge per μm for the SiGe buffer will result in a graded buffer thickness of 10μm. Capped with 1 μm Ge and assuming a 1 μm III-V layer, a total thickness of 12 μm is obtained.

Though in theory a III-V/SiGe mesa can be etched to access the underlying silicon for transistor fabrication as shown in Figure 2.3, in practice a 12 μm mesa will introduce nonplanarity which will negatively impact the lithography resolution. To achieve high resolution, the wafer has to be planarized but this involves deposition of very thick oxide (about 3 times the step height) and a chemical-mechanical polish step.

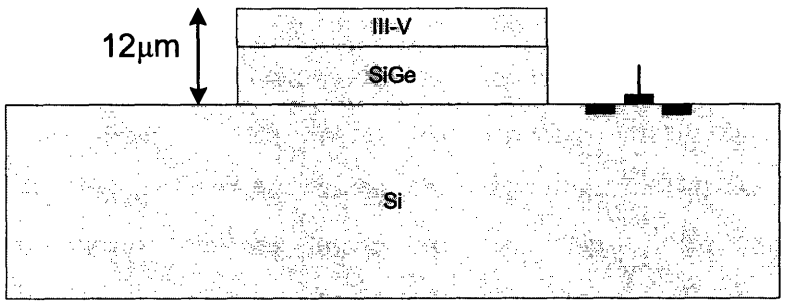


Figure 2.3: A III-V/SiGe mesa etched to reveal the underlying Si substrate creates a 12μm step between electronic devices and III-V material.

One way to overcome this drawback is to add a device-quality silicon layer on top of the SiGe buffer using intervening oxide layers, thereby reducing the step height between Si and III-V material to 0.5μm or less and making the integration process more tractable (Figure 2.4). This approach was adopted to demonstrate monolithic integration in this work. The next section details the fabrication process used to make this platform.

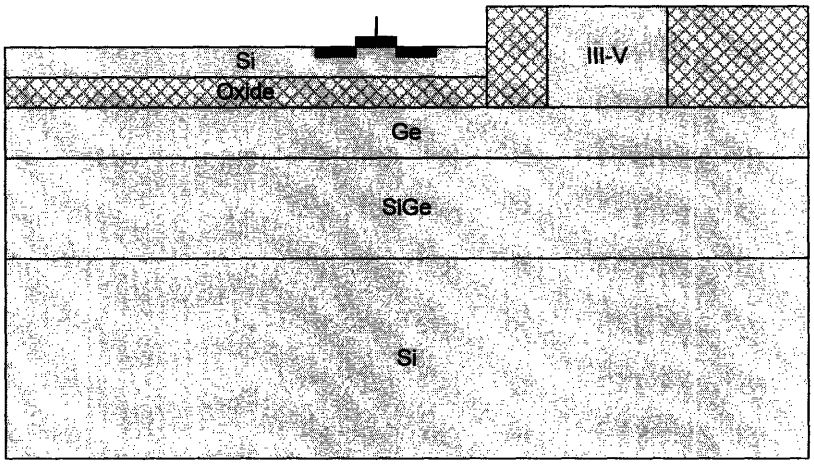


Figure 2.4: Schematic showing practical monolithic integration using the SOLES wafer.

2.4 Fabrication of SOLES

The process used to fabricate the structure shown in Figure 2.4 (Silicon on Lattice Engineered Substrate, also called SOLES) is essentially a modified version of the SMART-CUT® process [4]. The key steps in this process are hydrogen implantation, low temperature oxide growth, chemical mechanical polishing, wafer bonding and annealing to cause hydrogen-induced exfoliation and transfer of the silicon layer. In the traditional

SMART-CUT® process, silicon is bonded to silicon dioxide whereas in the modified process, oxide-to-oxide bonding occurs. Since the graded buffer surface is unusually rough and is marked by a representative crosshatch pattern, oxide layers are used to make the surfaces smooth for bonding. Besides facilitating bonding, the silicon dioxide layer isolates the thin Si film from the underlying Ge layer, thus preventing crosstalk between the CMOS driver and III-V optical devices.

The starting materials in the process are a 6" SiGe virtual substrate (henceforth called the handle wafer) and a 6" Si prime wafer (henceforth called the donor wafer because it donates the thin Si layer to the handle wafer).The first step is wafer cleaning prior to growth of the oxide layer. The donor wafer was cleaned using the standard RCA clean and a 200 Å thin layer of thermal SiO_2 was grown. The donor wafers were then sent to an external vendor for hydrogen ion implantation. (Dose = $5x10^{16}$ cm^{-2}, Implant energy = 80 KeV, Tilt = 7°). These implant conditions create a hydrogen-rich layer at a depth of about 0.3 μm from the surface.

The standard RCA clean could not be used for cleaning the handle wafer since hydrogen peroxide (H_2O_2) attacks Ge. Therefore the handle wafers were cleaned using a modified RCA clean that has a reduced exposure time to H_2O_2. The modified RCA clean recipe is given in Appendix C. A 7500 Å thick low temperature oxide (LTO) at 400 °C was next deposited on the handle wafers. The LTO deposition ensured that there was no temperature-related damage to the Ge virtual substrate. However, LTO films suffer from two drawbacks – one, they contain significant amounts of residual hydrogen from the deposition process which can lead to pockets of trapped gas at the bonded interface during wafer bond annealing, causing the bond to fail. Second, their surface roughness is too high for bonding. The first problem was overcome by annealing the wafers at 650 °C for 2 hours to expel the trapped gas and densify the oxide layer. The second hurdle was overcome by chemical-mechanical polishing (CMP). A brief description of the CMP process follows.

A Strasbaugh 6EC laboratory polisher (Figure 2.5) was used to reduce the roughness of the handle wafers to levels acceptable for bonding. The setup consists of a 22" polishing table with a Rohm and Haas IC1000 layered CMP pad. The pad is conditioned with a diamond-grit disc that lifts the nap of the CMP pad during wafer

polishing, thereby maintaining a constant material removal rate. Cabot's Semisperse-25 fumed silica slurry, diluted (1:1) with deionized water (DI) was used for polishing the LTO film. The wafer is held in place in the quill that rotates in the same direction as the polishing table. The downforce (P_d) is applied by a hydraulic piston to the entire wafer carrier, thereby setting the contact pressure between the wafer and the CMP pad. The backpressure (P_b) is a pneumatic pressure applied to the back of the wafer to maintain polish rate uniformity across the wafer surface.

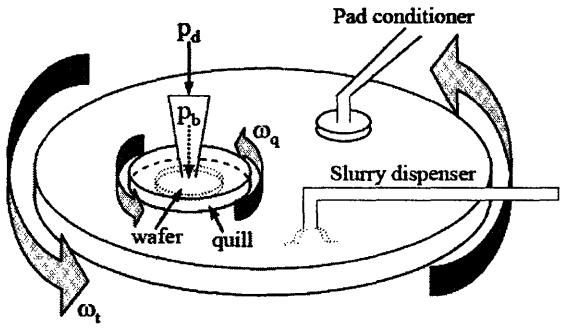


Figure 2.5: Schematic of the Strasbaugh 6EC laboratory polishing system. Courtesy Arthur Pitera.

The chemical component of oxide CMP is water, which serves to weaken the oxide bonds by the hydrolysis reaction given by

$$(SiO_2)_X + 2H_2O \rightarrow (SiO_2)_{X-1} + Si(OH)_4 \qquad \text{Equation 2.1}$$

This reaction is accelerated by the compressive stress induced by the interaction of the CMP pad and slurry particles with the wafer surface. The reaction products are subsequently removed by the additional mechanical action of slurry particles. As a result, both chemical and mechanical removal mechanisms are enhanced at surface asperities leading to high planarization efficiency.

The material removal rate by CMP for the parameters of the recipe given in Appendix C was determined as ~ 20Å/s. The wafers were polished for 250 seconds to remove about 5000 Å of oxide. After polishing, the wafers were immediately cleaned with a polyvinyl sponge and rinsed with DI water to remove the slurry deposits and

transported immersed in DI water to the piranha acid hood to prevent any residual slurry from drying on the surface. If the slurry dries, chemical bonds are formed between the particulates in the slurry and the wafer surface making it hard to remove. The wafers were piranha cleaned and spin-rinse dried using the recipe given in Appendix C. A similar CMP step for the donor wafers was not required since the thermal oxide on the donor wafers is smooth enough for bonding.

The next step involves bonding the donor and handle wafers. Before bonding, it is necessary to clean the donor and handle wafers to make the surfaces hydrophilic. A modified RCA clean (only SC1, no SC2 or HF dip) was used for this purpose. Once cleaned, the wafers were aligned and placed in a bonding chuck using the EV620 wafer aligner, transferred to the EV501 wafer bonder, and bonded. The wafer bonder performs two primary functions. Flags are used to keep the wafers separated at the edges until contact is initiated at the center of the two wafers. It also allows the application of force by applying pressure via a pressure chamber. The wafers were removed from the bonder and inspected with an IR camera. A picture of the bonded wafers is shown in Figure 2.6.

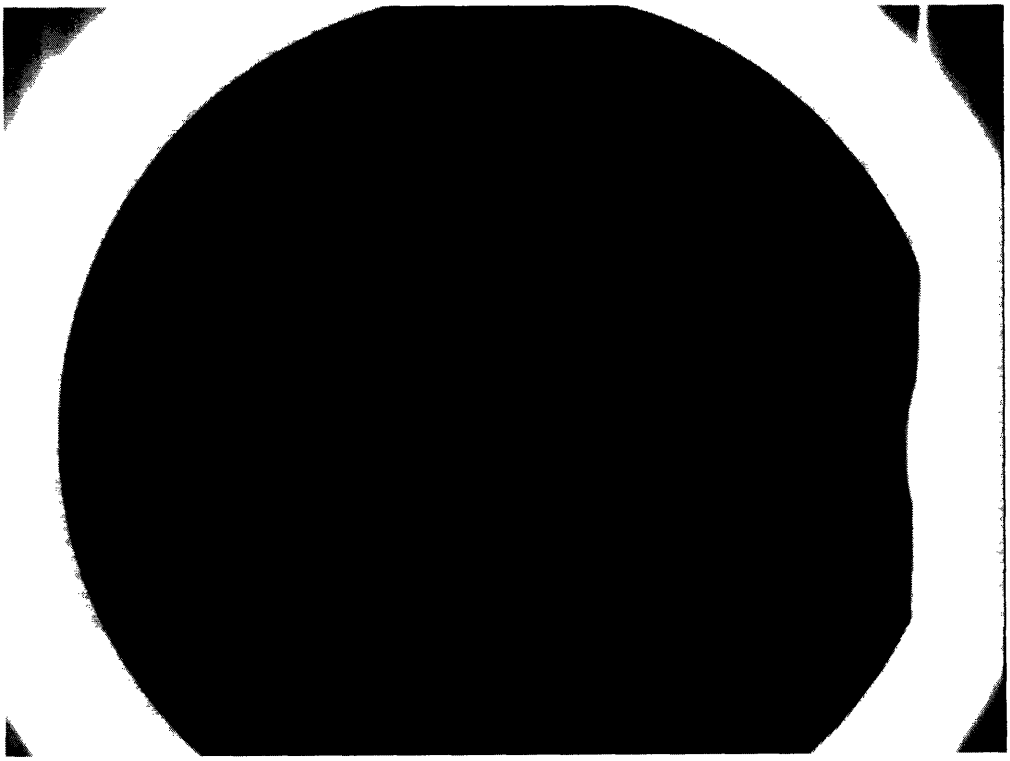


Figure 2.6: Infrared camera image of oxide-coated SiGe handle wafer bonded to a Si donor wafer.

Although the room temperature bond is strong enough to permit handling of the wafers, it is necessary to anneal the wafers to enable the oxide layers to fuse together and form stronger bonds. The wafers were furnace annealed at 250 °C for 1 hour for this purpose. While in the furnace, the temperature was ramped up to 450 °C and held for 1 hour to cause hydrogen-induced exfoliation and Si layer transfer. A schematic of the fabrication process flow is shown in Figure 2.7.

2.5 Results

The Si layer transfer was successful and was uniform across the 6" SiGe virtual substrate. A cross sectional TEM image of the fabricated SOLES wafer is shown in Figure 2.8. Exfoliation-related damage can be seen in the top regions of the transferred Si layer. For device fabrication, the damaged silicon can be removed either by a touch polishing step as in the SMARTCUT® process or by a timed wet/dry etch.

In summary, the SOLES material platform was successfully fabricated by wafer bonding and annealing to cause hydrogen-induced exfoliation and transfer of a thin device quality silicon layer on top of the graded buffer substrate. The fabricated SOLES wafer will be used to demonstrate practical monolithic integration.

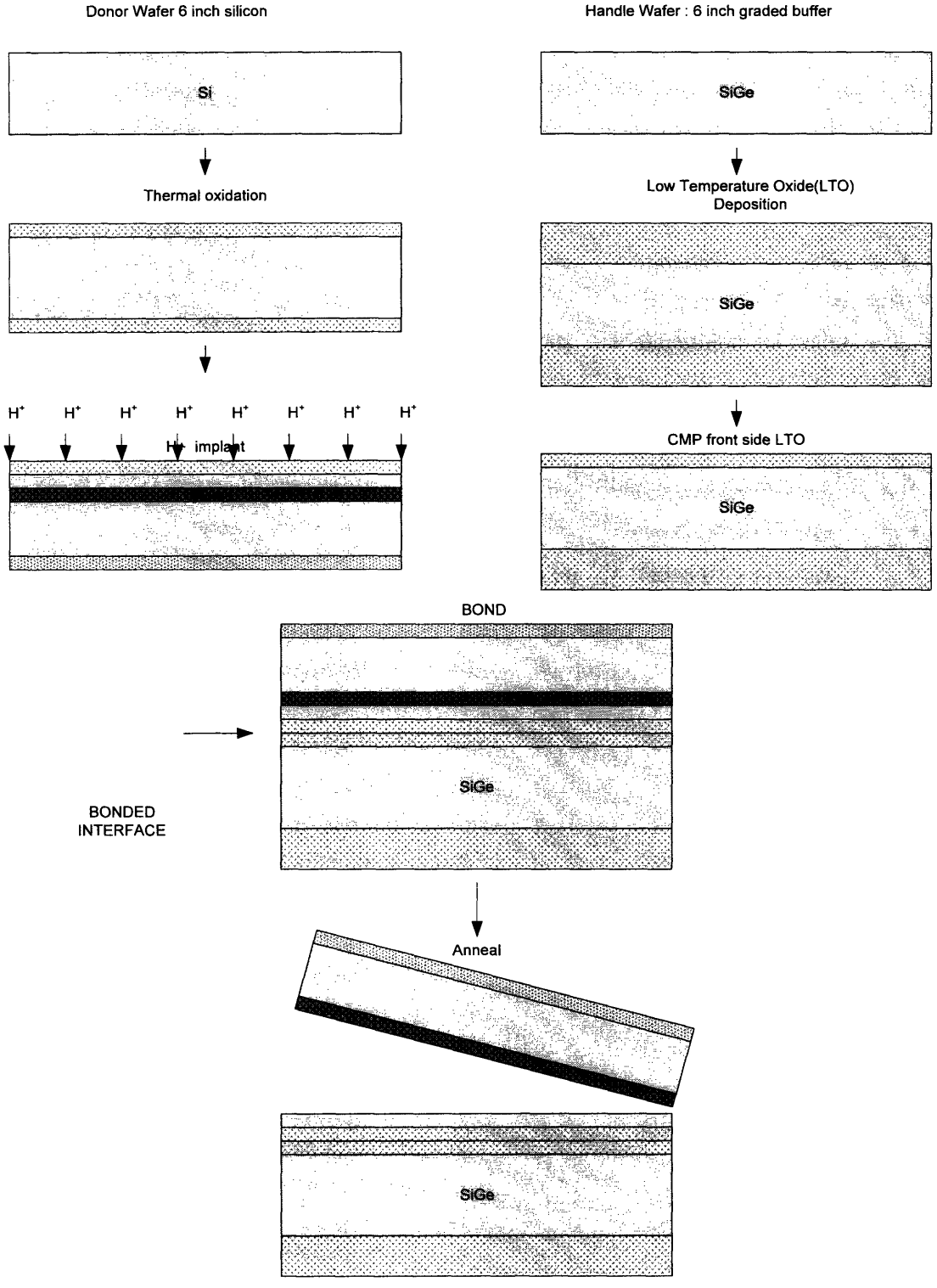


Figure 2.7: The SOLES fabrication process sequence.

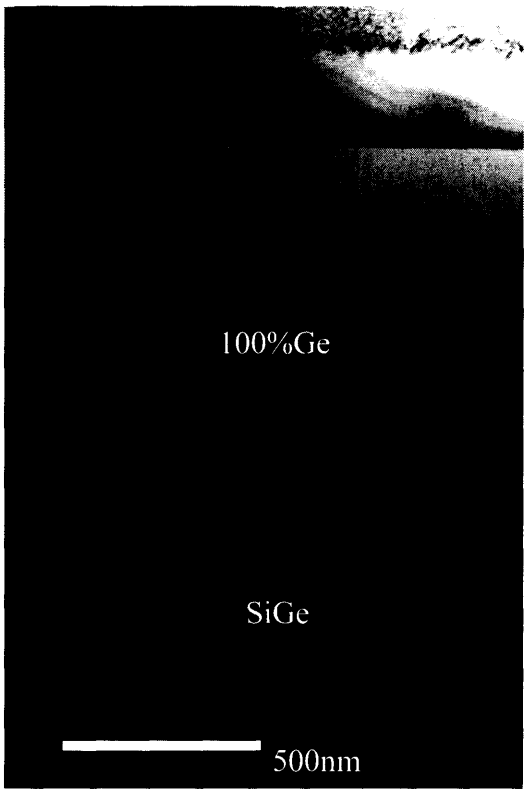


Figure 2.8:Cross-sectional TEM image of the fabricated SOLES wafer. Courtesy Carl Dohrman

CHAPTER 3

Development of CMOS-Compatible Contact Technology for III-V LEDs

3.1 Introduction

Following the successful fabrication of SOLES substrates suitable for practical monolithic integration, III-V materials must be introduced into a commercial Si CMOS fabrication facility without compromising the standard CMOS process. Such an introduction requires that the III-V material is not etched or exposed during processing in CMOS compatible tools. Also, the conventional gold-based ohmic contact metallurgy for III-V compounds/Ge cannot be used since gold forms deep level traps within the bandgap of silicon.

CMOS compatibility as outlined above was achieved in this work by accessing the n-GaAs cathode of the LED through the underlying n-Ge layer rather than etching through the III-V material of the LED stack. Further, encapsulating the LED with a thin film of CMOS-compatible material (like Si) prevents the exposure of III-V material while processing in CMOS compatible tools. Figure 3.1 shows a schematic of an LED structure employing this contacting scheme.

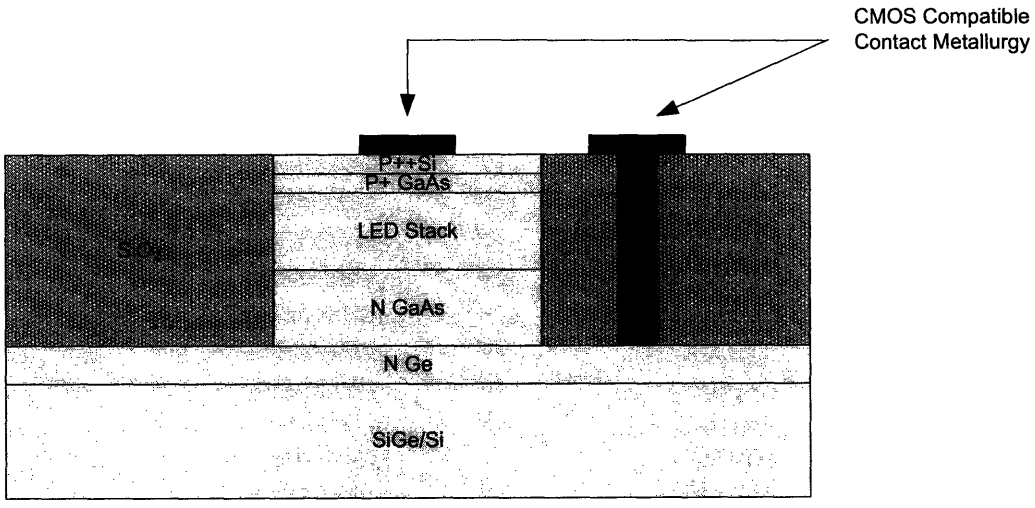


Figure 3.1: Schematic of the CMOS compatible III-V LED.

Using such a scheme introduces an n-GaAs/n-Ge and p-Si/p-GaAs heterojunction in series with the LED stack. For a given current, the extra voltage drop across these junctions will increase the joule heating of the device thereby degrading its efficiency. It is therefore important to understand the contribution of these heterojunctions to the overall voltage drop between the anode and cathode metal contacts of the LED.

3.2 The n-GaAs / n-Ge heterojunction

To understand the properties of the n-GaAs/n-Ge heterojunction, 1 μm nominally undoped GaAs was grown by MOCVD on epi-ready double-side polished two inch n-type Ge substrates (Sb doped, resistivity = 0.1 ohm-cm) misoriented 6° towards <111>. GaAs growth was undertaken at a high temperature (650 °C) and with a high ratio of AsH_3 to $(CH_3)_3Ga$ source gas flow rates in order to eliminate antiphase boundaries (APBs). APBs can serve as large-scale trapping sites to reduce minority carrier lifetime in GaAs device layers and also act to increase majority-carrier scattering in electronic circuits [5].

3.2.1 Interdiffusion at the GaAs/Ge interface

A difficulty with GaAs on Ge epitaxy is the interdiffusion of atoms at the GaAs/Ge junction. Whereas Ga and As can move down into the Ge substrate via solid state diffusion during growth, doping the Ge p- and n- type respectively, Ge atoms mainly contaminate GaAs epilayers through vapor phase transport during the deposition process, doping it n-type.

Ge out-diffusion can counter-dope p-type epi-layers, thus reducing device efficiency. This problem can be overcome by limiting the vapor phase transport of Ge during MOCVD growth [6]. It has not been possible to reduce Ga and As diffusion into the Ge substrate since the conditions that eliminate APB formation (high temperature and high AsH_3 to $(CH_3)_3Ga$ ratio) cause significant solid state diffusion of these species [7].

3.2.2 Material characterization - SIMS Analysis

Interdiffusion at the GaAs/Ge heterointerface was investigated by secondary ion mass spectroscopy (SIMS). SIMS is a powerful tool for the quantitative measurement of dopant and impurity levels in semiconductors. The technique relies on bombardment of the sample surface with a primary ion beam followed by mass spectrometry of the

emitted secondary ions [8]. For the GaAs on Ge sample in this work, Cs^+ primary ions were accelerated to an energy of 2 keV and the mass spectral peak intensity of the emitted ions was analyzed. The resulting concentration profile is shown in the semi-log SIMS plot of Figure 3.2. Note that zero on the x-axis corresponds to the GaAs surface and the GaAs/Ge interface is at a depth of approximately 1000 Å from the surface.

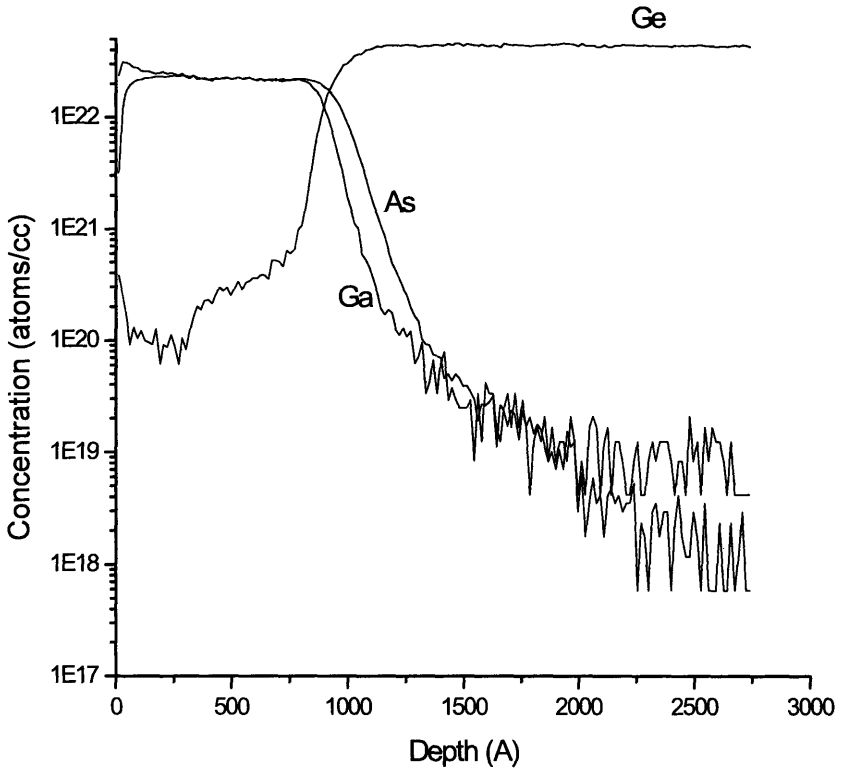


Figure 3.2: Semilog SIMS concentration profile for Ga, As and Ge atoms.

It is seen that Ge heavily autodopes GaAs epilayers greater than 10^{20} cm^{-3} throughout the film. The SIMS profile of Figure 3.2 is accurate only for the Ge concentration. The long As tail in Ge near the interface is an artifact of SIMS called the "knock in" effect wherein the high energy primary ions knock the Ga and As atoms from GaAs into the Ge substrate increasing their concentration over and above that due to solid state diffusion alone. Accurate results for the As and Ga concentrations near the interface were obtained by sputtering the sample from the Ge side after thinning the 160 μm substrate down to a few microns. The As and Ga concentration profiles obtained using this method are shown in Figure 3.3. The SIMS plot for the same atoms near the

Ge/GaAs interface is shown on a linear scale in Figure 3.4. It is seen that the Ga concentration is higher than that of As for about 1000 Å near the interface on the Ge side after which the As concentration exceeds that of Ga. Thus Ge gets autodoped p-type for the first 1000 Å and then becomes n-type. Since SIMS gives the total concentration of impurity atoms and usually only a fraction of these are electrically active, electrical measurements have to be performed and interpreted in order to corroborate the As and Ga doping profiles in Ge as suggested by SIMS data. The next section discusses the mesa diodes fabricated for this purpose.

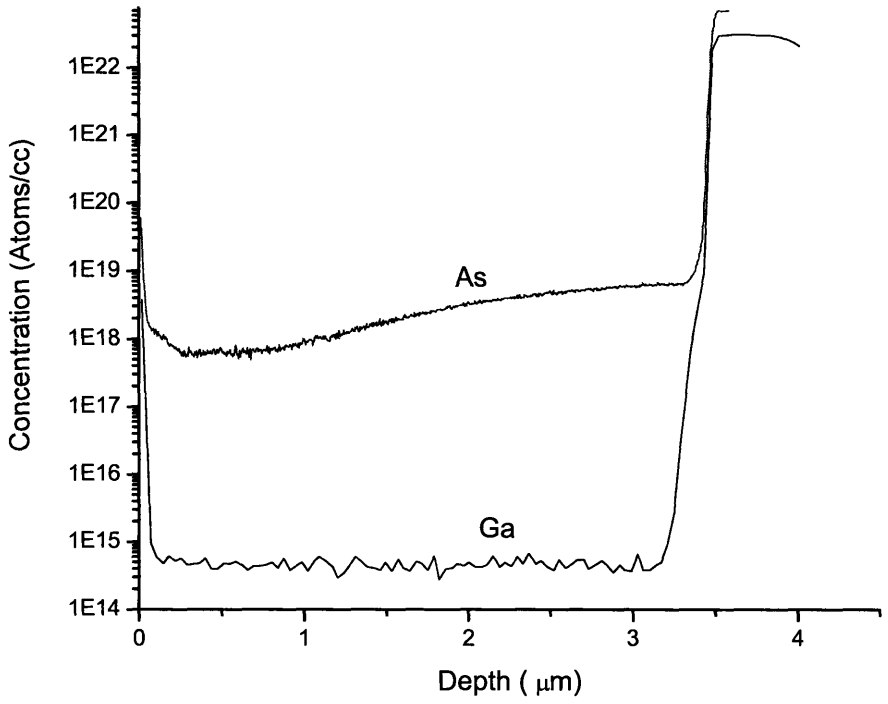


Figure 3.3:Semilog plot of the concentration profiles of As and Ga obtained by backside SIMS

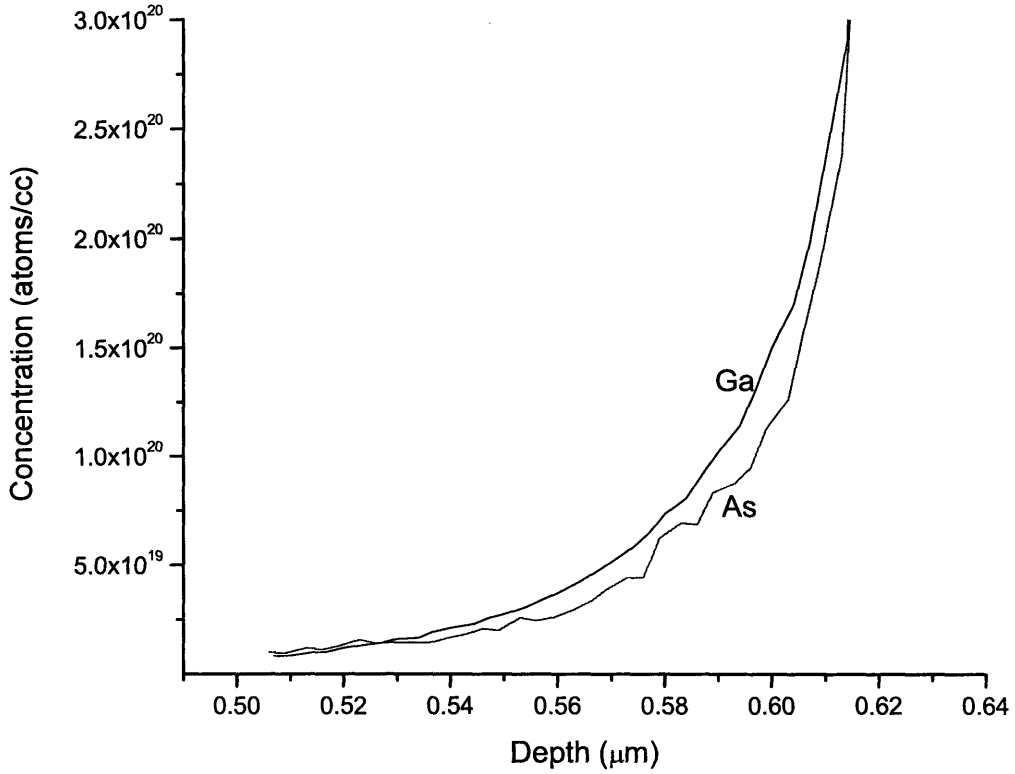
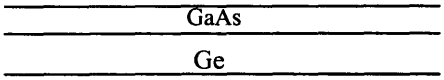


Figure 3.4: Plot of Ga and As concentration vs. depth on a linear scale obtained by backside SIMS.

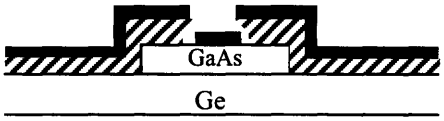
3.2.3 Electrical characterization – Mesa diode fabrication

A photomask originally designed for fabricating oxide stripe laser diodes was used to fabricate the GaAs mesas diodes [6]. Though the mask was meant to fabricate stripe lasers, square geometries were obtained by first exposing the substrate vertically in the contact aligner and then rotating it by ninety degrees for the second exposure.

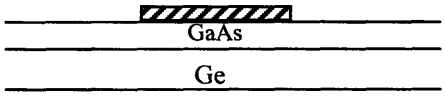
Figure 3.5 shows schematically the individual steps of the mesa diode fabrication process. The process consists of three modules, each module corresponding to one photo-mask level. Process Module I is the GaAs mesa formation. 200 μmx200 μm square GaAs mesas were etched with a phosphoric acid: hydrogen peroxide: DI water (3:1:50) solution using positive photoresist as a mask. This etchant is selective to GaAs and stops automatically when Ge is reached. Etch completion is easily observed because of the color difference between Ge (light green) and GaAs (dark blue).



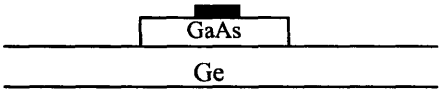
(1) MOCVD growth of nominally undoped GaAs on N Ge substrate



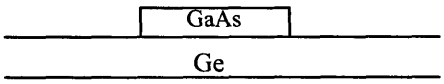
(5) E-beam evaporate metal



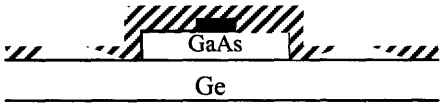
(2) Module I: Pattern positive photoresist mask



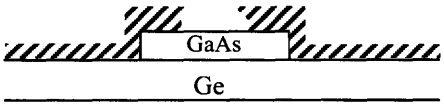
(6) Liftoff



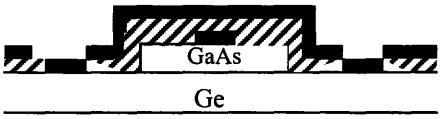
(3) Wet etch GaAs mesa and strip photoresist.



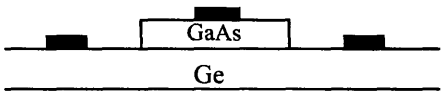
(7) Module III: pattern image reversal resist over Ge.



(4) Module II: Pattern image reversal resist over the GaAs mesa



(8) e-beam evaporate Ge ohmic contact metal.



(9) Liftoff

Figure 3.5: Schematic showing the GaAs/Ge mesa diode fabrication sequence.

Process Module II is the GaAs ohmic contact formation using 'liftoff'. Liftoff is a convenient micro-fabrication process that is used to pattern metallic films on a wafer. Metal is blanket-evaporated on the wafer and the metal deposited on top of the patterned photoresist is lifted away with the photoresist when soaked in acetone. Effective liftoff requires a break between the metal deposited on the photoresist and the metal deposited on the wafer. Image reversal photoresist with a negative slope profile accomplishes this. Also, as a rule of thumb the thickness of the deposited metal must be one-third the photoresist thickness for liftoff to be successful. n-GaAs ohmic contacts were formed by e-beam evaporating 500 Å Ni/ 2000 Å AuGe. Alloyed ohmic contacts can be formed by heating to temperatures above the AuGe eutectic temperature of 356 °C. During alloying the Ge from the AuGe dopes the surface of the GaAs n^+ which promotes carrier tunneling and makes the contact ohmic.

Process Module III is the n-Ge ohmic contact formation. This is identical to Module II except that 300 Å Au/100 Å Ni/2000 Å AuGe/500 Å Ni was e-beam evaporated to form the n-Ge contact. After liftoff of the deposited metal, the wafers were subjected to a rapid thermal anneal at 425 °C for 20s to make alloyed ohmic contacts.

3.2.4 Electrical characterization – Results and Discussion

A photomicrograph of the n-GaAs/n-Ge mesa diode is shown in Figure 3.6. The diode was directly micro-probed and the semilog I-V characteristic measured with a HP 4156C parameter analyzer is shown in Figure 3.7. The curve shows rectifying behavior and the series resistance estimated as the inverse slope of the I-V curve, drawn on a linear scale, at high forward bias is 10.7 Ω.

It is seen from Figure 3.7 that the magnitude of the current in reverse bias is high. Thus our GaAs/Ge junction is "leaky". C-V measurements for leaky junctions to extract diode built-in voltage are not meaningful and hence were not conducted.

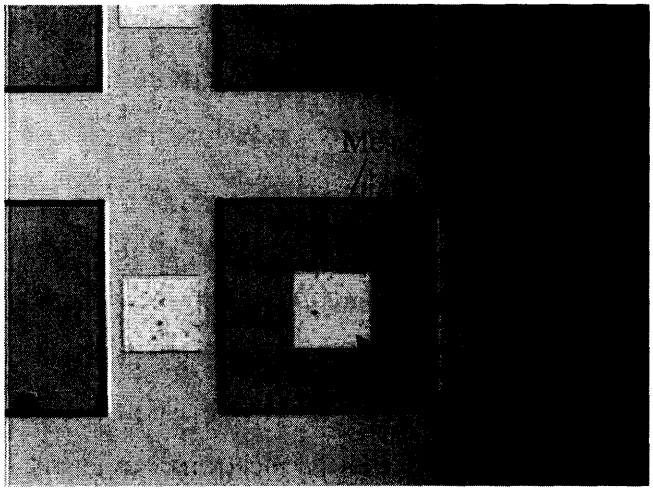


Figure 3.6: Photomicrograph of the fabricated GaAs/Ge mesa diode. The mesa size is 200μmx200μm and the contact pad size is 75μmx75μm.

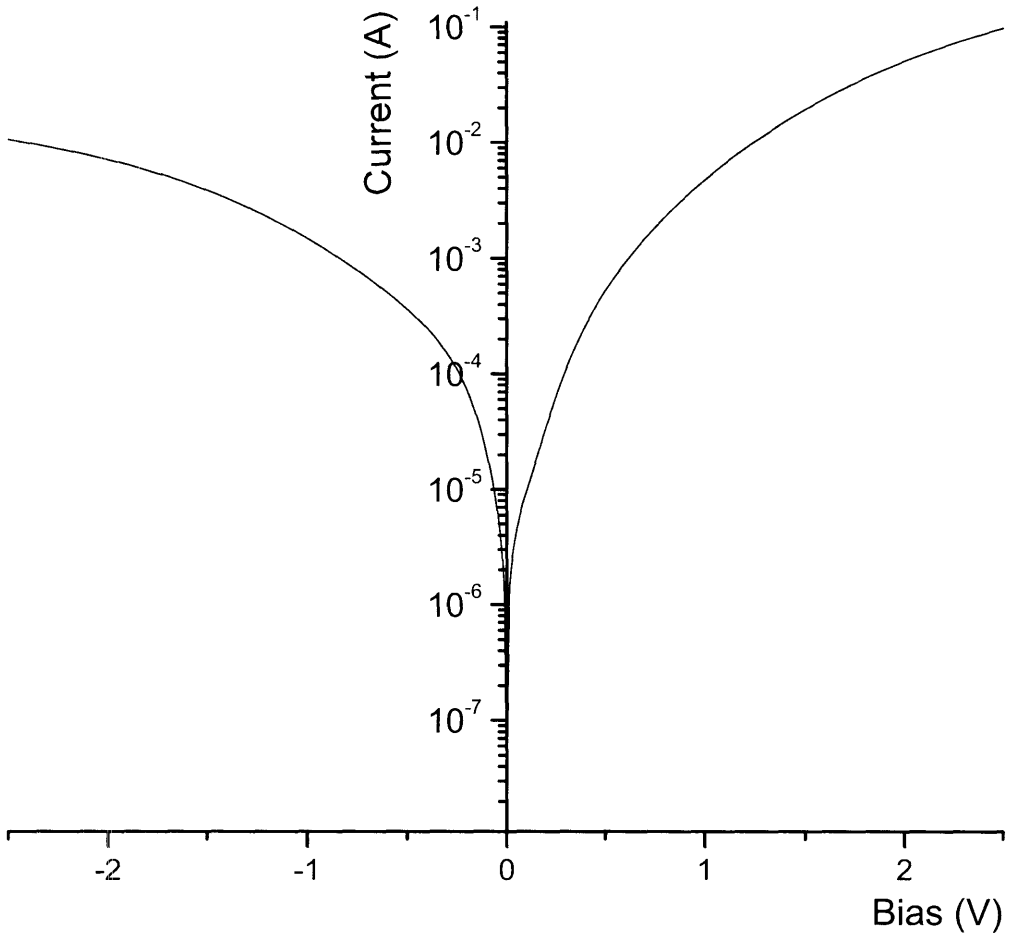


Figure 3.7: Semi- log I-V characteristic of the GaAs/Ge diode of Figure 3.6. The Ge contact was grounded and bias on the GaAs contact was swept from negative to positive.

The theoretical I-V characteristic of the n-GaAs/n-Ge isotype junction can be predicted from the band lineups when these materials are in metallurgical contact. Figure 3.8 shows a band lineup using Anderson's rule for this material system [10, 11]. The band lineup shown is for typical doping levels. The electron work function depends on the doping level and thus the extent of band-bending will vary with doping.

For an n-n isotype junction, the majority carriers on both sides of the junction are electrons. Therefore most of the current is carried by electrons. The discontinuity in the conduction band is very small therefore, if Ge is biased negative with respect to GaAs, the electron energy in Ge increases and the electrons can easily flow in the conduction band from Ge into GaAs. On biasing GaAs negative with respective to Ge, electrons from GaAs flow into Ge. Thus the electron flow is not impeded much in either state of bias. Hence in the ideal theoretical case the n-GaAs/n-Ge diodes should not rectify. This has also been experimentally found by Hudait *et al.* [7].

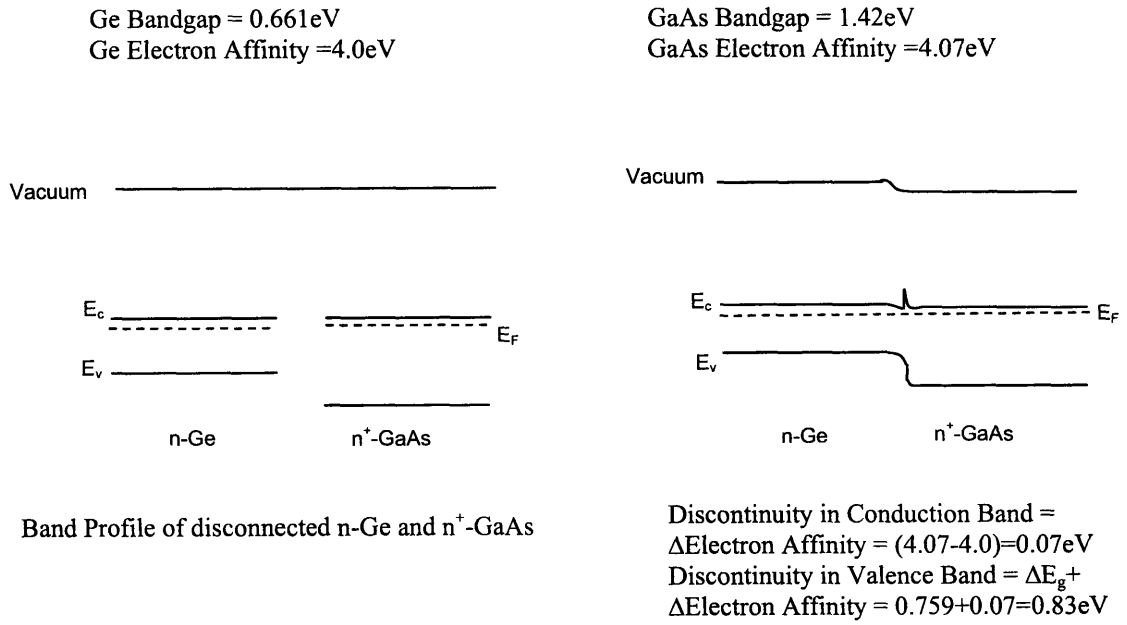


Figure 3.8: Band lineup for the n-Ge/ n^+-GaAs heterojunction.

The rectifying I-V curve of Figure 3.7 suggests that a thin layer of p^+-Ge is sandwiched between n-GaAs and n-Ge due to autodoping by Ga atoms. Thus the structure is actually n^+-GaAs/p^+-Ge/n-Ge rather than simply n^+-GaAs/n-Ge. A similar

observation has been made by Wojtczuk *et al.* [9].The rectifying I-V can be explained by modeling the n-p-n structure as two diodes of opposing polarities in series as shown in Figure 3.9. The I-V plot of Figure 3.7 was obtained by grounding terminal 2 (Figure 3.9) and sweeping the bias on terminal 1 from negative to positive. When a negative bias is applied to terminal 1, the n^+-GaAs/p^+-Ge diode is forward-biased and the p^+-Ge/n^+-Ge homodiode is reverse biased. Since these diodes are in series, the net current is limited by the reverse biased homodiode and hence is small. When a positive voltage is applied to n^+-GaAs, the n^+-GaAs/p^+-Ge diode is reverse biased and the p^+-Ge/n^+-Ge homodiode is forward biased. It is believed that the observed high current in this configuration is because the reverse-biased n^+-GaAs/p^+-Ge junction behaves as a tunnel diode since both the GaAs and Ge are autodoped in excess of their effective density of states. A tunnel diode in reverse bias does not impede current as much as a reversed biased conventional diode. Hence with the n^+-GaAs biased positive, the n-p-n structure effectively behaves as a forward biased Ge p-n homodiode and passes high current. At sufficiently high forward bias, the diode resistance can be assumed to be zero, and the resistance between the terminals equals the bulk resistance (R_{GaAs}+R_{Ge}).

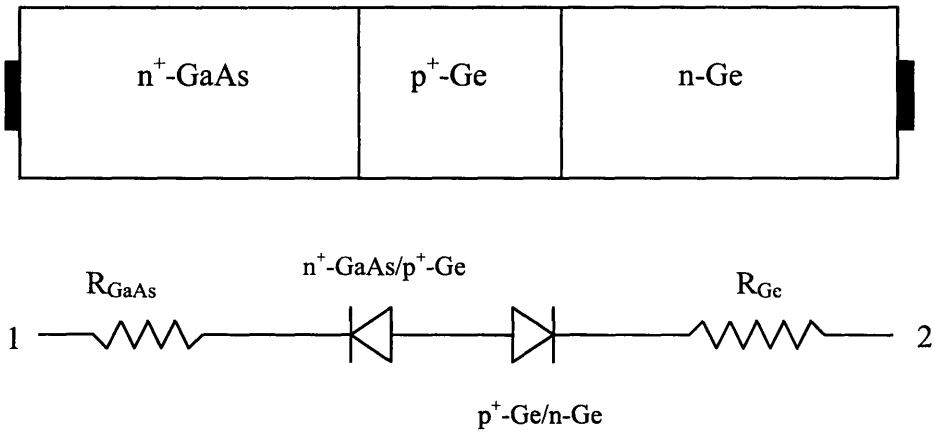


Figure 3.9: The n-p-n diode structure and the equivalent electrical circuit.

In summary, it can be concluded that Ga does indeed diffuse into Ge during the MOCVD growth of GaAs on Ge and acts as an electrically active p-type dopant. The voltage drop across the n-GaAs/n-Ge junction is attributed to the forward biased p^+-Ge/n-Ge homodiode. Since the homodiode will be positively biased during the LED operation,

the forward resistance is small and a bias current can be passed through the LED without incurring a huge voltage drop across the GaAs/Ge junction.

3.3 The p^{++}-Si /p^{+}-GaAs heterojunction

In order to study the electrical characteristics of the p^{++}-Si/p^{+}-GaAs heterojunction, a 0.5 μm p^{++}-Si (boron doped)/ 2μm p^{+}-GaAs (zinc doped) stack was grown by MOCVD on a semi-insulating GaAs substrate. The heavy doping should cause carrier tunneling and make the Si/GaAs heterojunction nearly ohmic with a low resistance.

3.3.1 Material characterization - SIMS Analysis

The SIMS profile of B, Ga and As species in the p^{++}-Si/p^{+}-GaAs stack is shown in Figure 3.10. Note that zero on the x-axis corresponds to the Si surface and the Si/GaAs interface is approximately 0.45 μm from the surface. In the Si layer, the boron concentration is very high and the gallium concentration is higher than arsenic away from the Si/GaAs interface. It is seen that though Si is autodoped by Ga and As, the high intentional boron doping swamps the Ga and As concentrations and so the p^{++}-Si preserves its doping level and type.

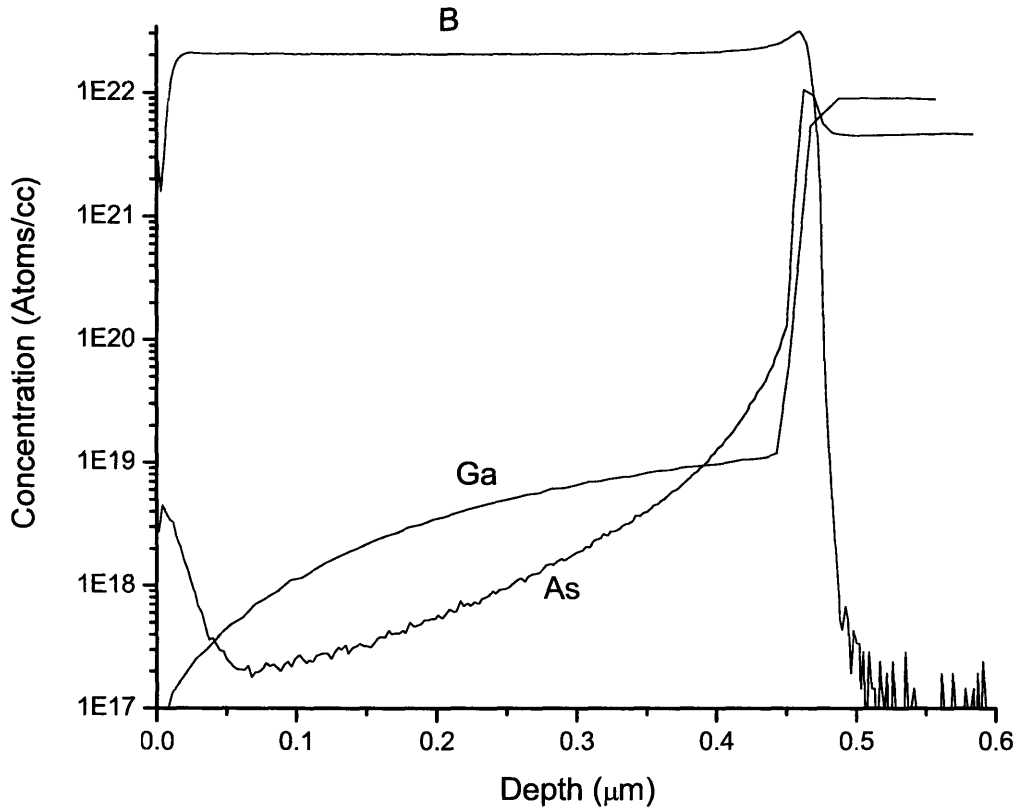


Figure 3.10: SIMS profile of Ga, As and B species in the p^{++}-Si/p^{+}-GaAs stack.

3.3.2 Electrical characterization – Mesa diode Fabrication

The mesa diode structure (see Figure 3.11) and basic fabrication sequence are similar to the GaAs/Ge diode process with a few modifications to accommodate the new material system. The mesa formation step first required the dry etching of 0.5 μm p^{++} Si in an ECR enhanced RIE system using a SF_6/O_2 plasma for 200s. The removal of the Si layer is easily visible as there is a color difference between Si (native silicon dioxide formed on Si is yellow green) and GaAs (dark blue). The dry etch recipe can be found in Appendix C. After the Si dry etch, 0.4 μm of p^{+}-GaAs was wet chemical etched for 4 minutes (etch rate ~ 0.1 μm/min) using H_3PO_4: H_2O_2: H_2O (3:1:50). Thus a 0.9 μm Si/GaAs mesa was formed. After patterning the top contact area, a quick dilute HF dip (1:10 HF:DI) was used to remove the Si native oxide and the wafer was immediately loaded in the e-beam chamber for metal deposition. A 500 Å Ti/1000 Å Al stack was used to contact the p^{++}-Si. After patterning the bottom contact area, a 50 Å Ti/200 Å Pt/2500 Å Au stack was e-beam evaporated to form the p^{+}-GaAs ohmic contact. Subsequent to the metal deposition and liftoff processes, the wafer was furnace annealed

at 400 °C for 40 minutes in a forming gas (90% N_2:10% H_2) ambient to form good ohmic contacts.

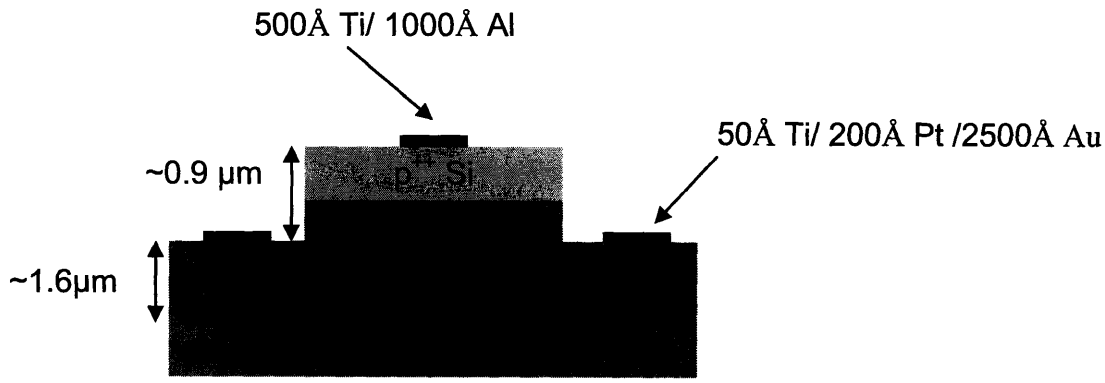


Figure 3.11: Schematic of the p^{++}-Si/ p^{+}-GaAs mesa diode.

3.3.3 Electrical characterization – Results and Discussion

The fabricated diodes were directly micro-probed and I-V characteristic measured with a HP 4156C parameter analyzer. Figure 3.12 shows the I-V characteristic. The characteristic is near linear (ohmic) over a wide range of applied voltages. It is believed that this is due to the tunneling of carriers across the heavily doped Si/GaAs junction.

In a p-GaAs/p-Si isotype junction the majority carriers on both sides of the junction are holes. Therefore the discontinuity in the valence band dictates the current flow (see Figure 3.13). Since the electron affinity of Si and GaAs are nearly the same, the discontinuity in the valence band is relatively large and approximately equal to the difference in bandgap energy of the materials (0.32 eV). Hence in theory the p-Si/p-GaAs junction should be non-ohmic. Since we have doped the Si and GaAs very heavily, we expect the holes to tunnel through the valence band discontinuity (Figure 3.14) and therefore the observed turn on voltage is very small.

The band diagrams in Figure 3.13 and 3.14 are for an ideal junction with no interface states. In reality, the 4% lattice mismatch for the Si/GaAs system leads to a high density of dangling bonds and correspondingly a high density of interface states. These interface states are a major factor in determining the energy band diagram of the p^{++}-Si/p^{+}-GaAs heterojunction [10, 11].

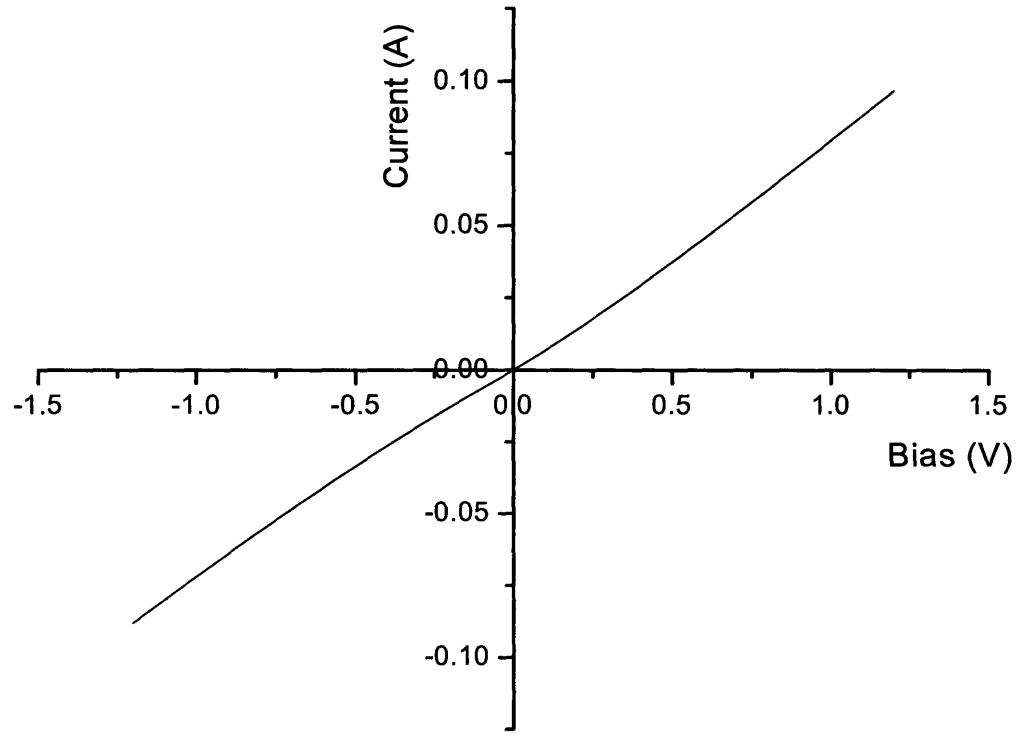
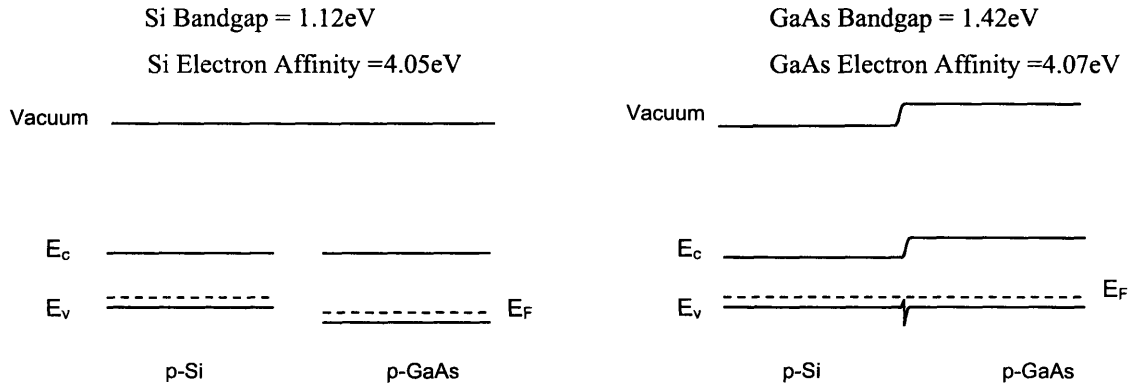


Figure 3.12: I-V characteristic for the p^{++}-Si/ p^{+}-GaAs diode.



Band Profile of disconnected P-Si and P- GaAs

Discontinuity in Conduction Band = ΔElectron Affinity =(4.07-4.05)=0.02eV
Discontinuity in Valence Band = ΔE_g+ ΔElectron Affinity = 0.3+0.02=0.32eV

Figure 3.13: Band lineup for p-Si /p-GaAs material system.

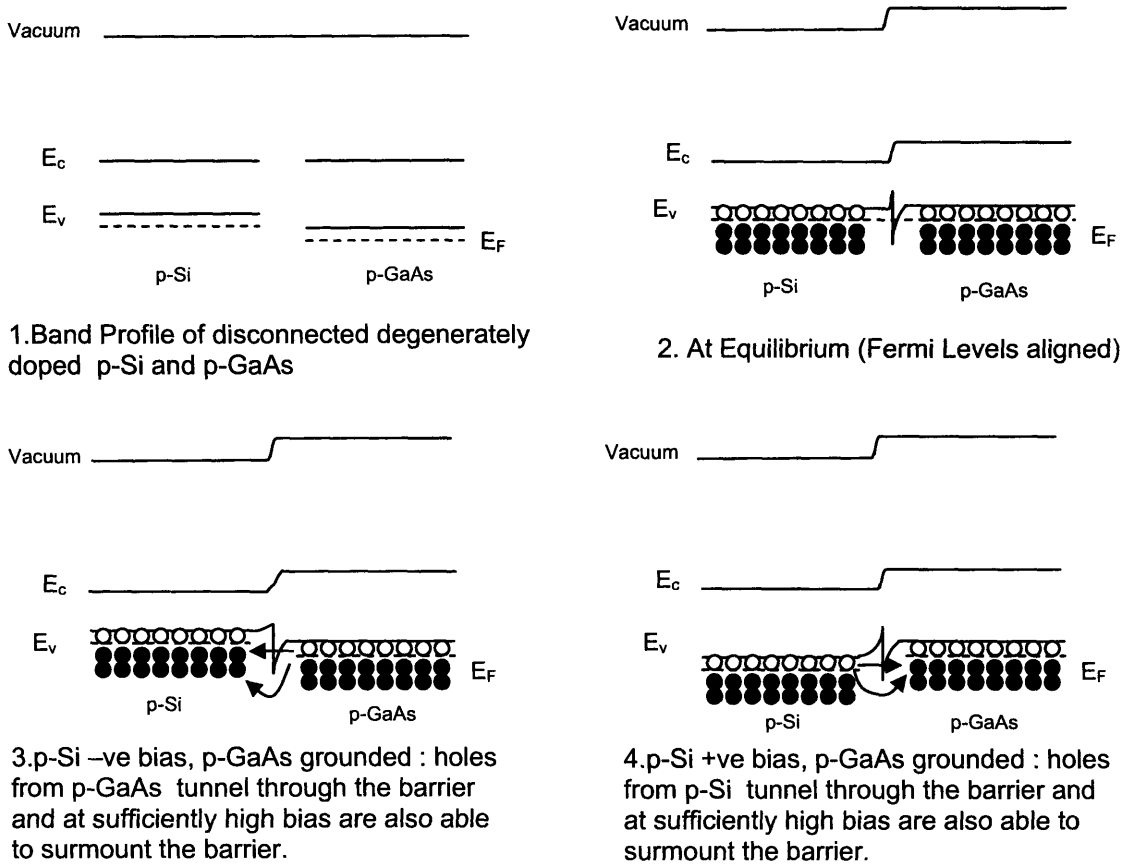


Figure 3.14: Schematic explaining the carrier tunneling theory for heavily doped Si/GaAs junction.

3.4 The p^{++}-Ge/p^{+}-GaAs heterojunction

One alternative to encapsulating the LED with Si is to use Ge which is also considered CMOS compatible. To investigate the p^{++}-Ge/p^{+}-GaAs heterojunction, 0.5 μm boron doped Ge/1 μm Zn doped GaAs was grown by MOCVD and processed into diodes. The fabrication of the p^{++}-Ge/p^{+}-GaAs mesa diode is identical to the previous diodes except for a few changes to accommodate the new material system. The mesa was formed by dry etching the Ge using an SF_6/O_2 plasma. The p^{++}-Ge was contacted using 500 Å Ti/ 250 Å Al. The SIMS data and I-V characteristic for this heterojunction are shown in Figures 3.15 and 3.16. The linear I-Vs indicate an ohmic junction.

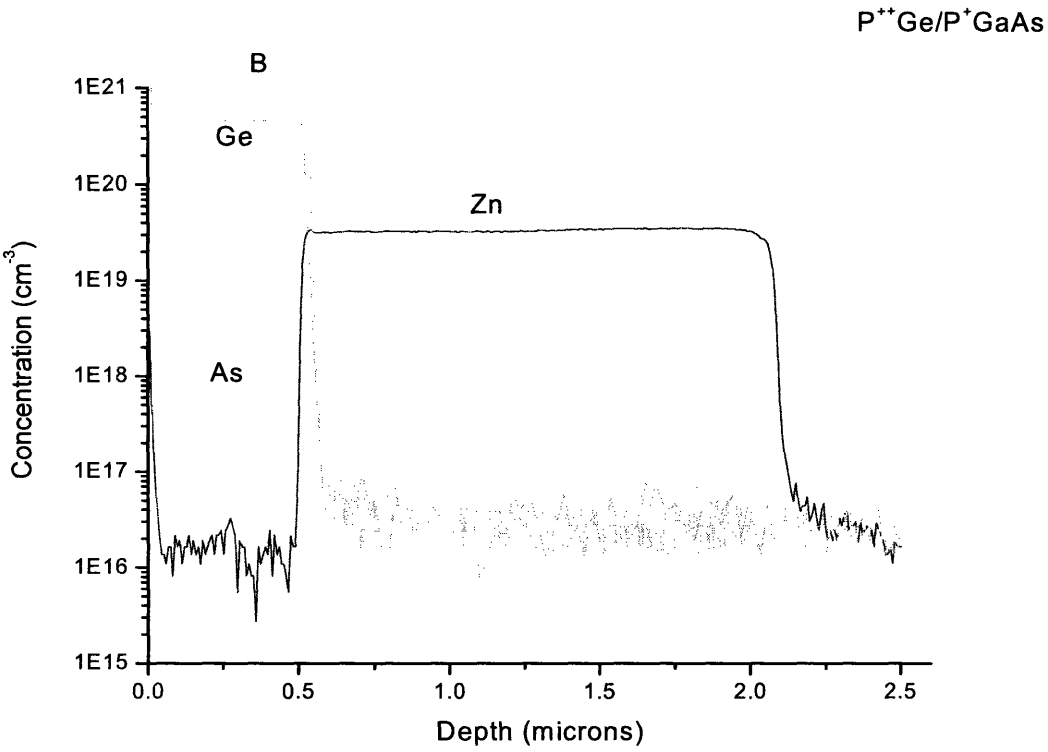


Figure 3.15: SIMS profile of the B, Zn concentrations in the p^{++}-Ge/p^{+}-GaAs stack.

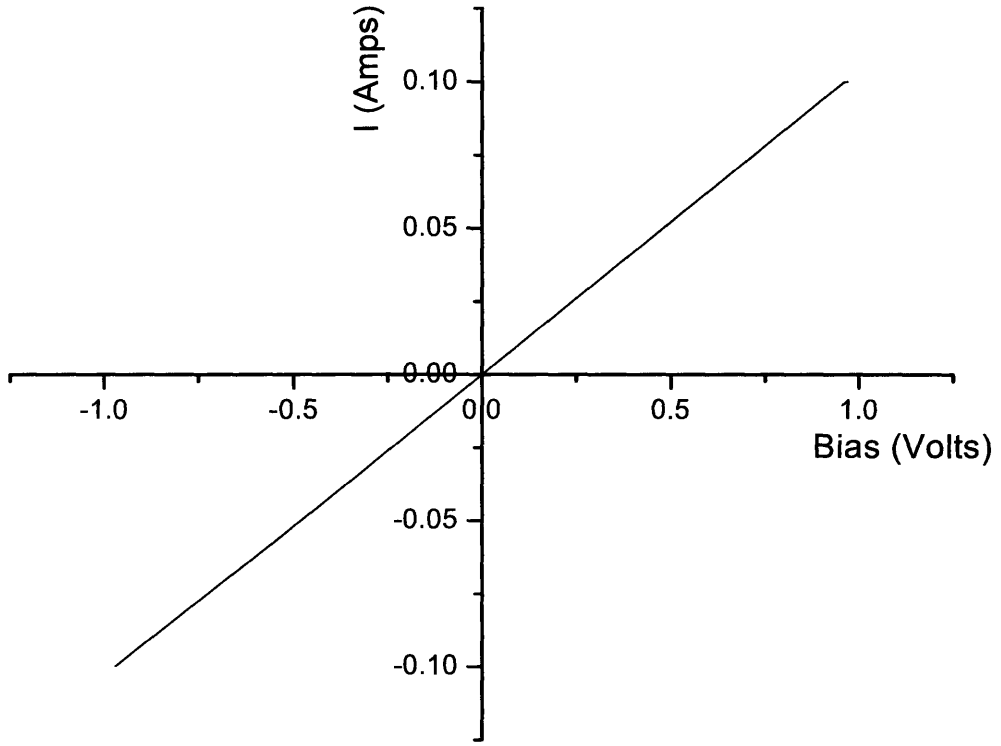


Figure 3.16: I-V characteristic of the p^{++}-Ge/p^{+}-GaAs heterojunction.

3.5 CMOS-compatible ohmic contacts to Ge

Referring back to the CMOS-compatible LED design in Figure 3.1, the n-GaAs cathode of the LED is contacted through the underlying n-Ge film to avoid etching the III-V material. Since the usual ohmic contacts to n-Ge are non CMOS compatible other alternatives have to be studied.

Two metal systems namely Ni and Ti were investigated. Ge wafer with n-type doping densities on the order of $5x10^{18}$ cm^{-3} were used for this study. Due to the limited availability of Ge substrates in our facilities, the Ge substrates used for this study were recycled by selectively etching the epitaxial n-GaAs and revealing the underlying heavily As autodoped (Figure 3.3) n-Ge substrates. Liftoff and e-beam evaporation were used to deposit 100 μmx100 μm square metal contacts on the wafer.

Figure 3.17 shows the I-V curves for NiGe-contacted Ge obtained for different annealing temperatures. It is seen that low resistance (15 Ω) NiGe ohmic contacts are

formed for 350 °C, 40 min anneal conditions. Figure 3.18 is the I-V characteristic for TiGe-contacted Ge. The series resistance is 18.9 Ω. Though TiGe contacts show a higher resistance than NiGe contacts, TiGe was ultimately used in this work as the CMOS-compatible contact metallurgy due to nonavailability of a Ni source in the sputtering system.

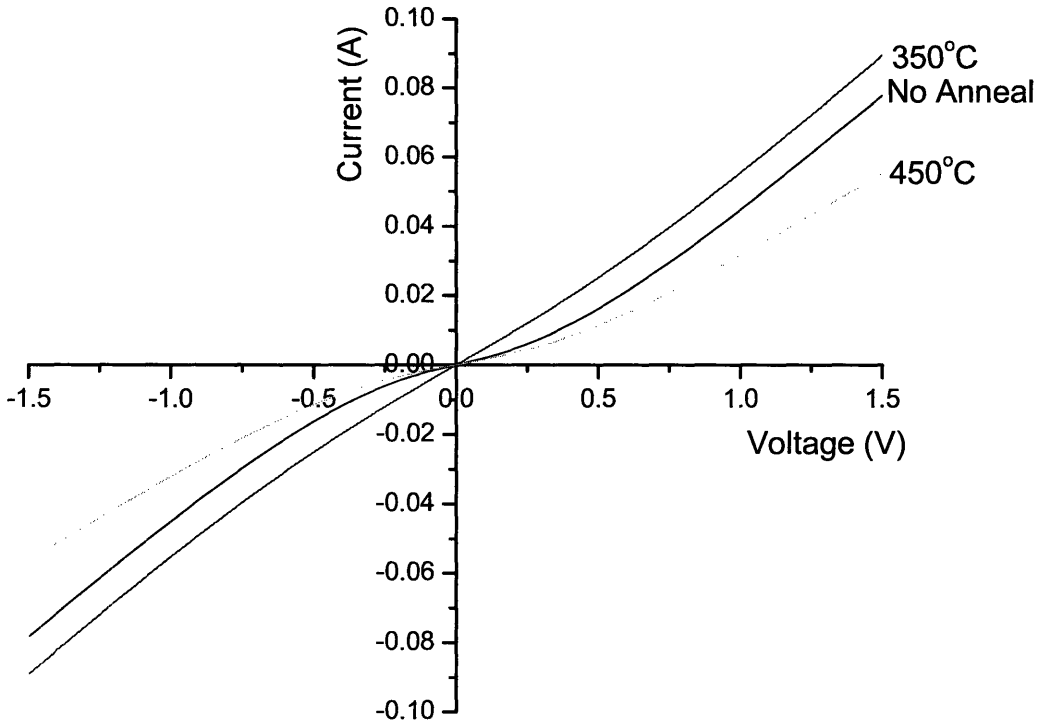


Figure 3.17: I-V characteristic for NiGe contact for different annealing conditions.

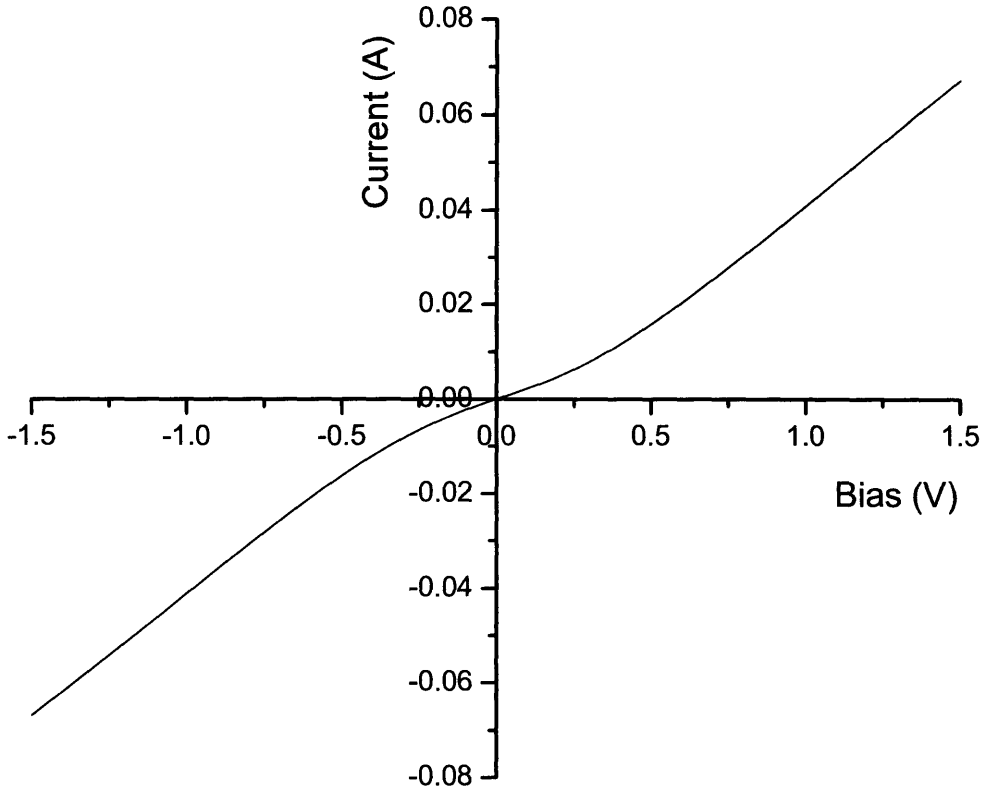


Figure 3.18: I-V characteristic of TiGe contacted Ge. Ti/Al was annealed in forming gas ambient at 400 °C for 40min to form TiGe.

In summary, a better understanding of the n-GaAs/n-Ge and p^{++}-Si/p^{+}-GaAs heterojunctions was gained in this chapter. The current-voltage characteristic of the n-GaAs/n-Ge junction showed rectification indicating presence of a p^{+}Ge layer and suggests that the n-GaAs/p^{+}-Ge interface is a tunnel junction. Thus, the forward voltage drop across the n-GaAs/n-Ge junction can be attributed to the forward biased p^{+}-Ge/n-Ge homodiode. The current-voltage characteristic of the p^{++}-Si/p^{+}-GaAs heterojunctions are nearly linear showing that carrier tunneling helps reduce resistance.

CHAPTER 4

Design and Fabrication of AlGaInP Visible Light Emitting Diodes

4.1 Introduction

This chapter discusses the operating principle and device design of the AlGaInP double heterojunction light emitting diode, including material choice and issues related to high quality material growth. The effect of the Si encapsulation layer on the LED electrical and optical characteristics is investigated and LEDs fabricated on SiGe virtual substrates and bulk Ge substrates are compared.

Semiconducting materials can be classified into two categories depending on their energy bandgap, direct and indirect. In an indirect bandgap semiconductor, electrons and holes recombine nonradiatively and the energy released is dissipated into the lattice as heat. For a similar recombination in direct bandgap semiconductors, momentum is conserved in the electron transition from the conduction to the valence band and a photon is released. Unfortunately, silicon has an indirect bandgap and is therefore unsuitable for light emission. Many III-V semiconductors like (Al)GaInP have direct band gaps and can be used to make light-emitting devices.

4.2 The (Al)GaInP material system

It is seen from Figure 4.1 that GaP and InP can be alloyed to form $Ga_xIn_{1-x}P$. As x is varied from 1 to 0 (GaP to InP) the lattice constant increases from 5.45 Å to 5.86 Å. For x=0.5, $In_{0.5}Ga_{0.5}P$ (point A) having an energy gap of 1.9 eV corresponding to a wavelength of 0.65 μm (Red) is obtained. In a similar fashion, $Al_{0.5}In_{0.5}P$ can be obtained by alloying AlP and InP (point B). $In_{0.5}Ga_{0.5}P$ and $Al_{0.5}In_{0.5}P$ can be alloyed further to form the quaternary $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ that lies on the dashed vertical line connecting points A and B in Figure 4.1. Increasing y from 0 to 1 causes movement along this line from $In_{0.5}Ga_{0.5}P$ to $Al_{0.5}In_{0.5}P$. For $y > 0.7$ (point C) the material transitions to an indirect energy gap regime (shaded region).

It is clear from Figure 4.1 that GaAs and $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ have approximately the same lattice constant. Lattice matching of the different material layers of the LED stack is crucial for high internal efficiency LED designs. Lattice mismatched layers induce the formation of threading dislocations that act as nonradiative recombination centers for electrons and holes. Though having a higher defect density than bulk Ge substrates, the Ge cap of the virtual substrates is nearly lattice matched to GaAs and $(Al_yGa_{1-y})_{0.5}In_{0.5}P$,thus the GaAs/Ge/SiGe/Si material system is a suitable choice for growing the AlGaInP LED stack.

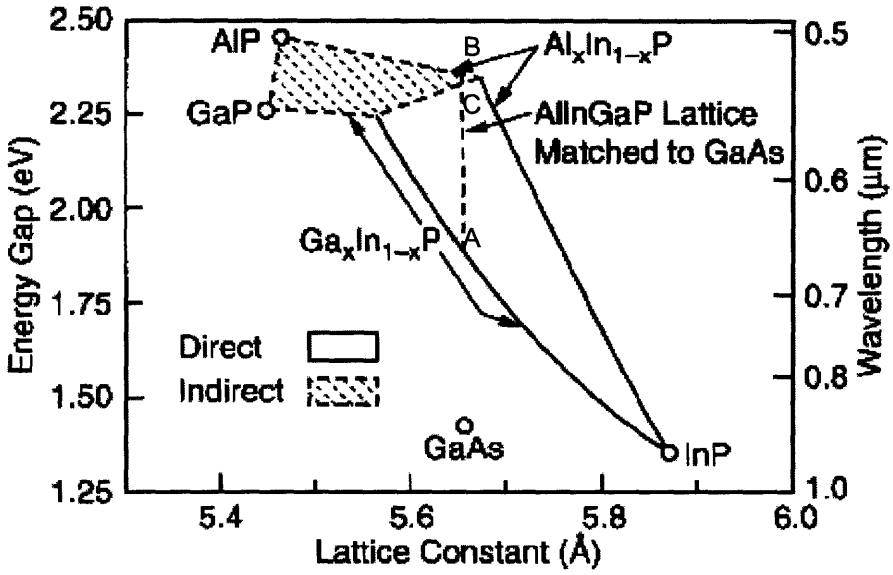
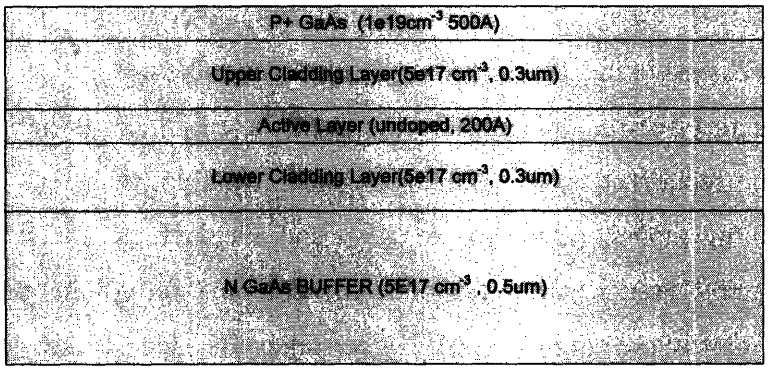


Figure 4.1: The energy gap of the AlGaInP alloy vs. lattice constant [12].

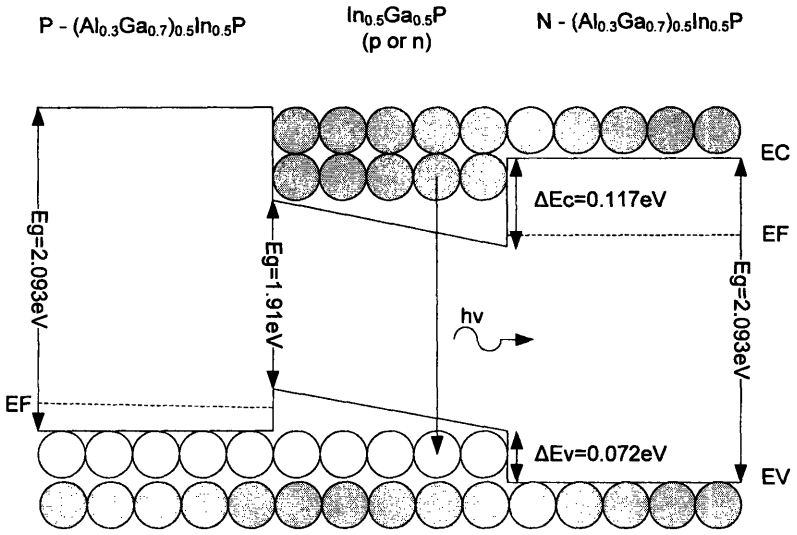
4.3 Double-Heterojunction (DH) AlGaInP LED design

High internal efficiency in an LED can be achieved by employing a double heterojunction (DH) structure (Figure 4.2(a)). DH LEDs are more efficient than simple homojunction devices due to inherent advantages associated with the double heterojunction. In a DH LED an active region consisting of a material possessing a lower energy bandgap is sandwiched between two cladding layers with larger bandgap. The material in the active region where the electrons and holes recombine determines the wavelength of light emitted. Because of the high energy gap cladding on both sides,

electrons and holes are trapped in the active region and the probability of electron-hole recombination increases thereby increasing the efficiency compared to that of a p-n homojunction LED. Also, since the cladding layers have a higher bandgap than the active region, absorption of the generated light is reduced compared to a p-n homojunction device.



(a)



(b)

Figure 4.2 (a): The DH LED stack (b): Schematic of the free carrier distribution in a Double Heterojunction under forward bias

4.3.1 Active Layer Design

The wavelength of emitted light in an LED is determined by the bandgap of the semiconductor material wherein the electron-hole recombination takes place (the active region) as well as quantum confinement effects in thin quantum well active region designs. The active region in this design was grown nominally undoped. However, the optimal doping level for the active region has been reported in the literature [13] to be lightly n- or p- doped less than 10^{17} cm^{-3} since this helps increase the injection efficiency of carriers as discussed in the cladding layer design section below.

After minority carrier injection occurs at the heterojunction, the injected carriers might recombine radiatively or nonradiatively within the active layer or escape to the adjoining confining layers. According to Kish and Fletcher [13] "confinement of the carriers to the active layer results in a reduced recombination volume and an increased injected carrier density (see Figure 4.2b). Higher injected carrier density generally results in increased radiative efficiency due to the saturation of the nonradiative recombination centers". The benefits of the DH are realized provided the active layer thickness is less than the minority carrier diffusion length. Thicker active regions also result in a reduction in LED efficiency caused by the absorption of light in the active layer. A 200 Å $In_{0.5}Ga_{0.5}P$ layer having bandgap energy of 1.9eV and thus emitting in the red region of the visible spectrum (650nm) was chosen as the active region.

4.3.2 Upper and Lower Cladding Layer design

Though nominally undoped, the active region of the LED stack gets autodoped n-type by Si or p-type by Zn during growth. Thus either an N-p-P or N-n-P structure is formed (Figure 4.2(b)).

The electron-hole injection ratio at the N-p heterojunction is given by [13]

$$\frac{J_e}{J_h} \propto N_D . e^{\frac{\Delta E_g}{kT}} \qquad \textbf{Equation 4.1}$$

where ΔE_g is the difference in band gap energy between the N-cladding layer and p-active layer. Equation 4.1 neglects the effects of interfacial recombination and any conduction and valence band offset spikes (ΔE_c and ΔE_v) at the heterointerface. A similar equation holds for the P-n heterojunction. These equations indicate that the injection of

electrons at the N-p junction and holes at the P-n junction is maximized by maximizing the energy gap difference between the cladding layer and active region.

According to Kish and Fletcher [13] "in order for these injected carriers to be confined to the active layer, they must lack sufficient thermal energy to leak over the potential barrier at the active-confining layer interface. Carrier leakage in a DH device can consist of either drift or diffusion of carriers that possess sufficient thermal energy to be transported from the active layer to the confining layers. Since the injected current density in an LED is low, diffusive leakage is the primary concern. Further, hole leakage at the n-N heterojunction is usually small since the hole mobility is usually one order of magnitude less than that of electrons. Also, the density of states effective mass of holes is significantly larger than that of electrons in the direct bandgap active region. As a result the density of holes with sufficient thermal energy to surmount the same confining layer potential barrier is significantly less than that of electrons. Therefore electron diffusive leakage is the primary carrier confinement issue for AlGaInP DH LEDs".

The electron diffusive leakage at a p-P active–confining layer heterointerface is given by [13]

$$J_L \propto e^{\frac{E_{fn,act}-\Delta\varepsilon}{kT}} \qquad \textbf{Equation 4.2}$$

where $E_{fn,act}$ is the electron quasi–Fermi level in the active layer and is a function of the injected minority carrier (electron) density in the active layer. $\Delta\varepsilon$ is the effective barrier for electrons in the active–confining layer interface, and is given by [13]

$$\Delta\varepsilon = (E_{gap}^{conf} - E_{gap}^{act}) + (E_{fp}^{act} - E_{fP}^{conf}) \qquad \textbf{Equation 4.3}$$

wherein the first term represents the difference in bandgap energy between the confining layer and the active layer and the second term is the difference in hole quasi-Fermi levels in the active and confining layers. These equations assume an ideal heterojunction with no interface states and that any conduction band offset spike present is negligible.

It is evident from Equation 4.3 that the electron diffusive leakage can be minimized at the p-P heterointerface if the difference in band gaps between the confining and active layers is large. Thus, in order to maximize both carrier injection and confinement, the bandgap energy difference must be maximized.

The bandgap energy of $(Al_yGa_{1-y})_{0.5}In_{0.5}P$ increases linearly with y. In light of the above, this means that y=1 having the highest Al concentration and bandgap energy is the ideal choice for the cladding layer to maximize injection and confinement efficiency. But a higher Al content would lead to increased oxygen incorporation. Oxygen incorporation causes nonradiative recombination centers or deep levels in the bandgap deteriorating device performance [12]. For this reason material with a lower Al content (y = 0.3) and bandgap energy of 2.093eV was chosen for the cladding layers.

Also, from Equation 4.3, the P confinement layer must be heavily doped to ensure that the difference between the Fermi levels in the active and confining layers is maximized. High doping also maximizes current spreading and minimizes series resistance. However, high doping can also lead to an increase in the nonradiative recombination centers introduced by the dopants at the cladding-active interface. From the literature [13], the electron diffusive leakage is negligible for doping levels greater than 10^{17} cm^{-3}.Also, for maximum injection efficiency the doping density has been reported to be 10^{16} to $5x10^{18}$ cm^{-3} for n-type and $4x10^{17}$ to $2x10^{18}$ cm^{-3} for p-type. Thus a doping density of $5x10^{17}$ cm^{-3} was chosen for the cladding layers.

4.3.3 Current spreading layer design

The cladding layer doping is intentionally kept low to reduce nonradiative recombination centers at the cladding-active interface. This means the injected carriers will not spread laterally due to high resistance and hence the current is injected into the active region mostly under the top electrode. Consequently the light is generated under the opaque metal electrode resulting in low extraction efficiency. A current-spreading layer avoids this problem by spreading the current to regions not covered by the opaque top electrode. The resistance of the current spreading layer is kept low by increasing the doping and thereby decreasing the resistivity or by increasing the area of cross-section of the lateral current flow by increasing the layer thickness. But a thicker cap layer can also absorb the emitted light and reduce the extraction efficiency of the device. Thus a trade-

off exists between current spreading and light absorption. For a doping density of 10^{19} cm^{-3}, a 500 Å thick p-GaAs cap layer is sufficient for current spreading [14].

4.3.4 Encapsulation layer design

It is necessary to encapsulate the p^{+}-GaAs current spreading layer with p^{++}-Si or p^{++}-Ge in order to make the LED fabrication process CMOS compatible. The presence of such a cap layer could be detrimental to the operation of the surface emitting LED because it absorbs the emitted light but at the same time it can help current-spreading.

A p^{++}-Ge cap has the advantage that a single metal ohmic contact recipe (Ni Germanide formed by annealing Ni at 350°C for 40mins) can be used to contact both the anode and the cathode of the LED. But the optical absorption coefficient of Ge at 650nm is appreciably higher than that of Si. Therefore silicon was used as the encapsulation layer. When annealed at 400°C in forming gas ambient, Ti reacts with Si forming titanium silicide. For 500Å Ti about 1200Å of Si is consumed in the silicide reaction [15]. Therefore the silicon cap thickness must be at least 1200Å.

The thickness of the cap must be kept as low as possible since there is exponential dependence of the transmitted light intensity on the layer thickness given by

$$I = I_0 e^{-\alpha . l} \qquad \textbf{Equation 4.3}$$

Where α is the absorption coefficient of silicon, I_0 is the intensity of incident light and l is the layer thickness. The absorption coefficient for heavily doped Si ($3x10^{20}$ cm^{-3}) at 1.9 eV is 6000 cm^{-1} [16]. Using this value for a 1200Å Si cap doped to 10^{21} cm^{-3} we find that 7% of the light is absorbed by the cap.

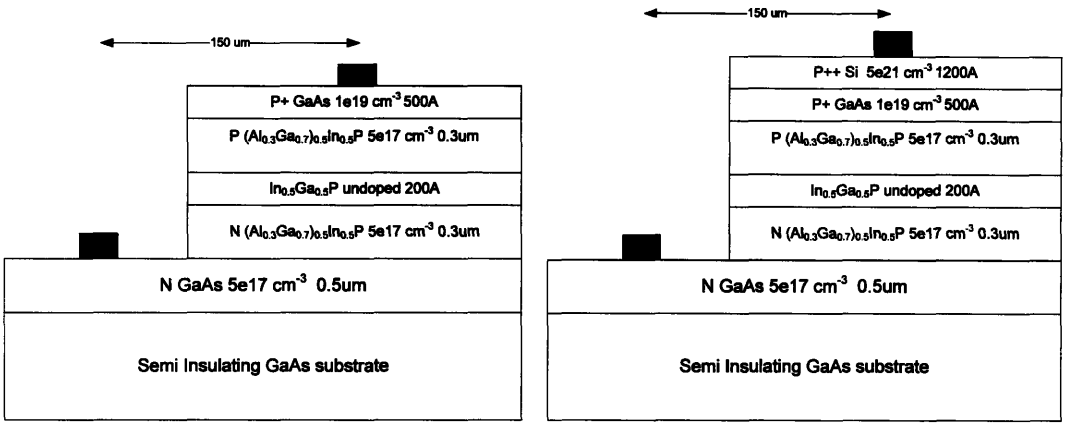
4.4 AlGaInP Growth Issues

The growth of high quality AlGaInP can be quite difficult. Because it is a quaternary system, careful control is required to ensure lattice-matching of AlGaInP to the GaAs substrate. Also, aluminum is very reactive and binds easily with oxygen. One way to suppress oxygen incorporation is to increase the growth temperature. The temperature used in our growths was 650 °C. The V/III ratio was maintained at ~83. Another important issue for the growth of AlGaInP epilayers is the switching from AsH_3

gas for the growth of GaAs to PH_3 for the growth of phosphide-based materials. Rapid switching of the group V gases is necessary and the precise switching sequence and its timing are critical. Also, since Ge has a slightly higher lattice constant (5.6575 Å) compared to GaAs (5.6533 Å), for the optimization of AlGaInP layers, it is important that the In fraction of the AlGaInP material is slightly increased when growing on Ge substrates.

4.5 Effect of the p^{++}-Si encapsulation layer

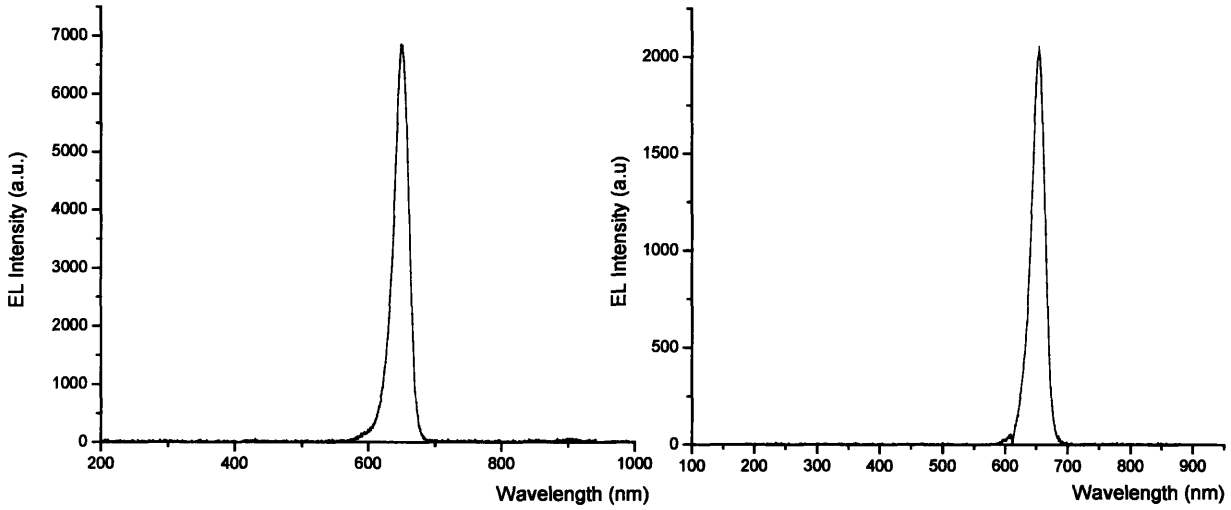
AlGaInP DH LED structures were grown on semi-insulating GaAs wafers at 100 Torr pressure and 650 °C. A heavily doped Si-capped AlGaInP DH LED structure was also grown for comparison. The Si cap was doped p^{++} with boron. The p^{+}-GaAs and p-AlGaInP layers were doped using dimethylzinc precursors. The n-AlGaInP and n-GaAs were doped with 1% dilute silane in hydrogen. The uncapped AlGaInP LED was processed into mesa diodes by wet chemical etching the p^{+}-GaAs current spreading layer and the AlGaInP symmetric DH stack and stopping at the n-GaAs layer. The recipes used are given in Appendix A4. 500 Å Ni/2000 Å AuGe was used for the n^{+}-GaAs ohmic contact and 50 Å Ti/200 Å Pt/2500 Å Au was used for the p^{+}-GaAs ohmic contact. The mesa diode structure is shown in Figure 4.3(a). The Si capped AlGaInP LED was processed into mesa diodes by dry etching the p^{++}-Si cap, wet chemical etching the p^{+}-GaAs current spreading layer and the AlGaInP symmetric DH stack and stopping at the n-GaAs layer. 500 Å Ni/2000 Å AuGe was used as the n^{+}-GaAs ohmic contact and 500 Å Ti//1000 Å Al was used as the p^{++}-Si ohmic contact. The mesa diode structure is shown in Figure 4.3(b).



(a) (b)

Figure 4.3: (a) Schematic of LED mesa diode structure without Si cap. (b) with Si cap.

The devices were directly micro-probed and the room temperature spectral response and I-V characteristic were measured. Figure 4.4 shows the spectral response of the LEDs with and without the Si cap at 30mA bias. The peak for the uncapped device occurs at 649nm and the FWHM is 25nm. The silicon-capped device shows a peak at 654nm and a FWHM of 24nm. Red emission from the devices was clearly visible to the unaided eye in ambient room light (Figure 4.5).



(a) (b)

Figure 4.4: (a) Device with no Si cap - peak at 649nm and FWHM = 25nm (b) Device with Si cap – peak at 654nm and FWHM =24nm.

Figure 4.5: Photomicrograph of an AlGaInP LED grown on semi-insulating GaAs substrate biased at 30mA.

The I-V characteristics of the LEDs are shown in Figure 4.6. The devices with the p^{++}-Si cap show a higher forward voltage compared to uncapped devices. This could be attributed to the additional voltage drop at the Si/GaAs heterojunction. The difference could also likely be attributable to variations from growth to growth, and in this case, one key variation might be autodoping from having Ge-containing substrates in the reactor during the growth of the Si-capped LED.

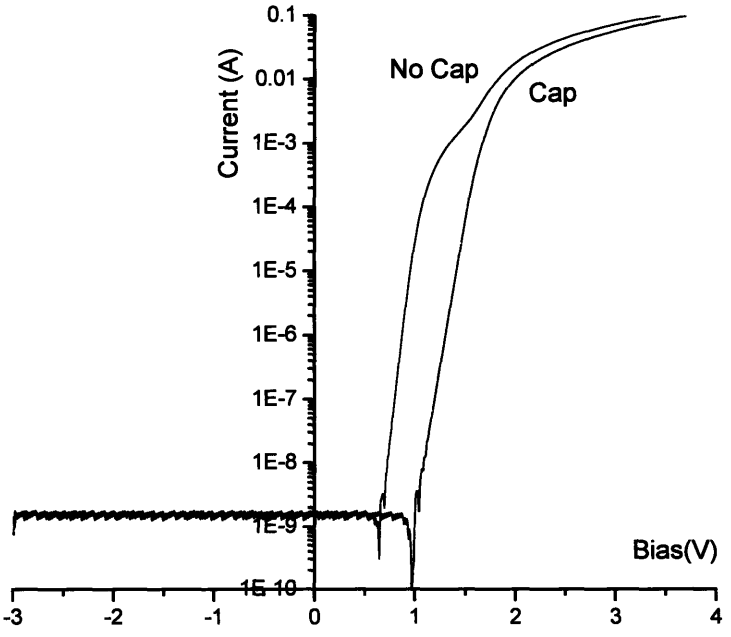


Figure 4.6:Semilog I-V curves for AlGaInP LED on GaAs substrate with and without Si cap

Figure 4.7 shows the fiber coupled power vs. current for the devices at 650nm wavelength. Optical measurements were made on-wafer by coupling a portion of the LED emission onto a calibrated Si photodetector via a 600 μm core optical fiber (numerical aperture = 0.22) placed 735 μm vertically above the devices. It should be noted that the light output reported in Figure 4.6 is not calibrated to reflect the collection efficiency of the measurement setup. Also, no attempts to prevent current induced heating were made. Though the devices with the Si cap have a higher forward voltage for a given current and therefore higher joule heating, they are more efficient than uncapped devices. The higher light output could be attributed to enhanced current spreading due to the heavily doped Si cap that improves light extraction efficiency.

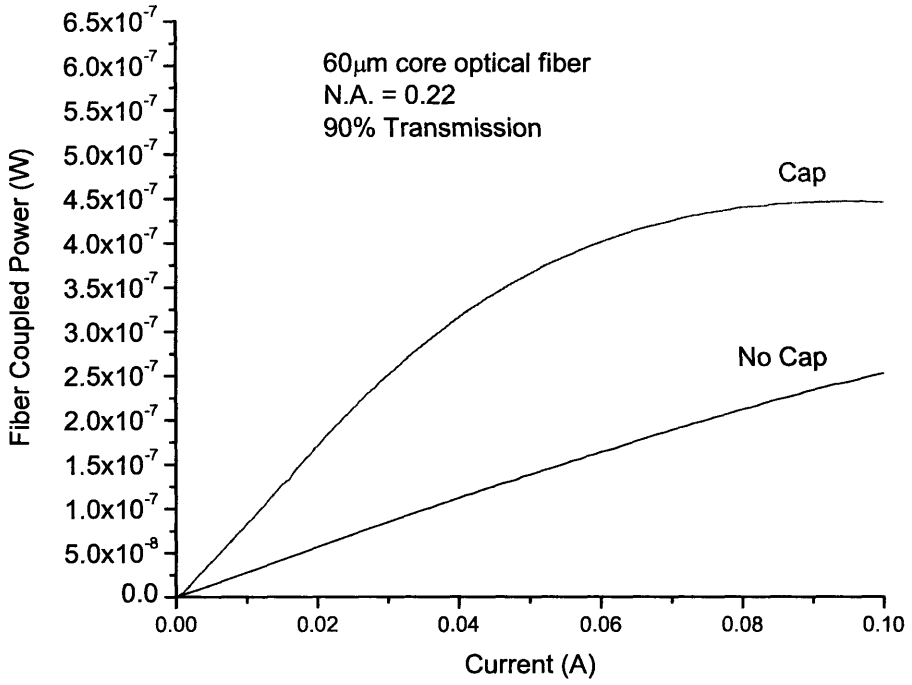


Figure 4.7: Fiber coupled power vs. bias current for devices with and without Si cap.

4.6 p^{++}-Si encapsulated AlGaInP LED on SiGe graded buffers

A p^{++}-Si encapsulated DH LED was grown on a 6° off-cut bulk, 2" Ge substrate (doped to ~ 10^{17} cm^{-3}) and on a piece of a 6" Si wafer that comprised a SiGe graded buffer with a undoped 100%Ge cap. The doping of the n-GaAs buffer layer was intentionally kept low ($5x10^{17}$ cm^{-3}) since the Ge out diffusion is expected to dope it

heavily n-type. Figure 4.8 shows a cross-sectional TEM image of the LED layers grown on the graded buffer.

The LED material stack on Ge and SiGe substrates was processed into mesa diodes by dry etching the p^{++}-Si cap, wet chemical etching the p^{+}-GaAs current spreading layer, the AlGaInP symmetric DH stack and the n-GaAs layer to expose the underlying Ge. We expect the Ge to be autodoped n-type from As indiffusion from GaAs epi layers. 50 Å Ni/200 Å Pt/2000 Å Au/100 Å Ni was used to contact the n-Ge and 500 Å Ti/500 Å Al was used as the p^{++}-Si ohmic contact. Figure 4.9 shows the normalized electroluminescence spectra at 30mA bias for the two devices. Devices on bulk Ge show peak intensity at 653nm and have a FWHM of 32nm. Devices on SiGe (i.e., Ge-capped SiGe graded buffer on Si) show a peak at 661nm and have a FWHM of 40nm.

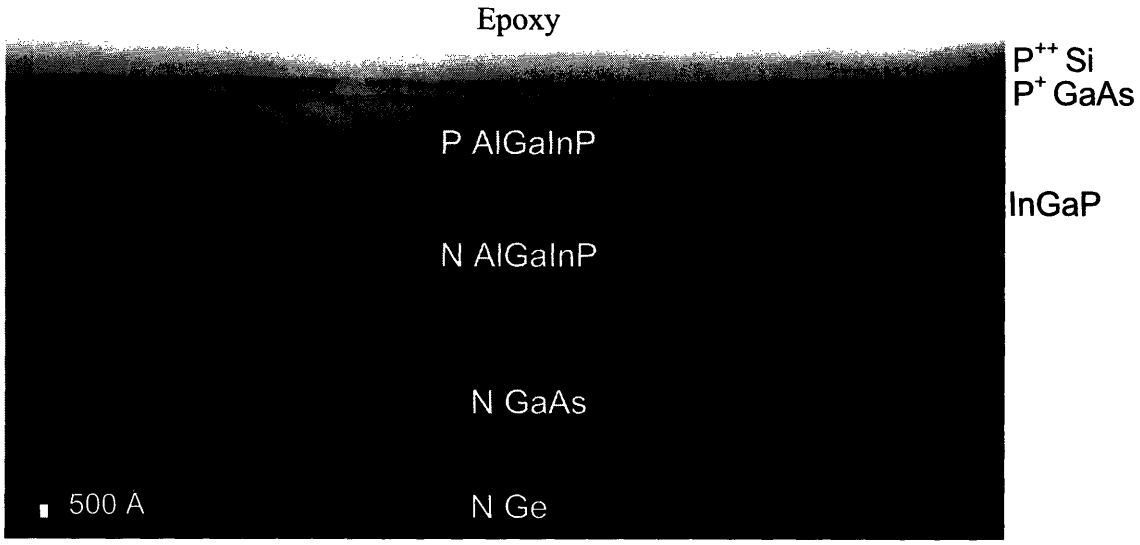


Figure 4.8: Cross-sectional TEM image of the LED layers grown on the graded buffer substrate. The Si cap was grown in-situ in the MOCVD reactor. Image courtesy Mike Mori.

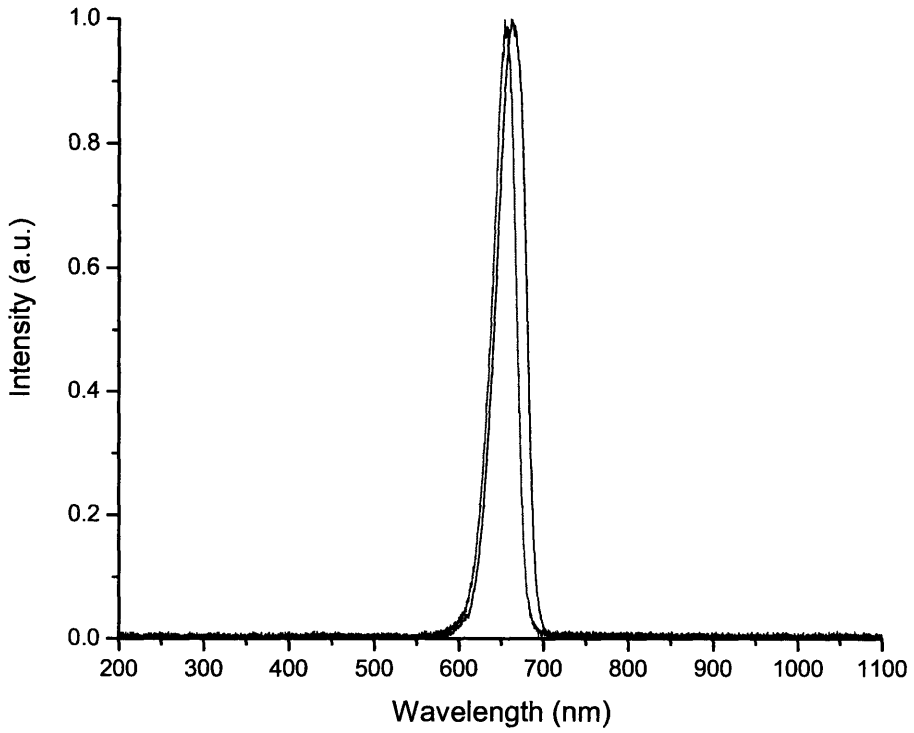


Figure 4.9: Spectral response of Si-capped LEDs on bulk Ge and SiGe graded buffer substrate at 30mA bias.

Semi-logarithmic I-V characteristics for the silicon capped LED on Ge and SiGe substrates are plotted in Figure 4.10. Devices on SiGe show a lower forward voltage and higher reverse leakage current than similar devices on bulk Ge. The increase in the leakage current for reverse bias greater than 1V for LEDs on SiGe suggests that the decrease in the ideality factor in forward bias is related to defects. We therefore assume that the threading dislocations are the likely reason for the increased leakage and forward current.

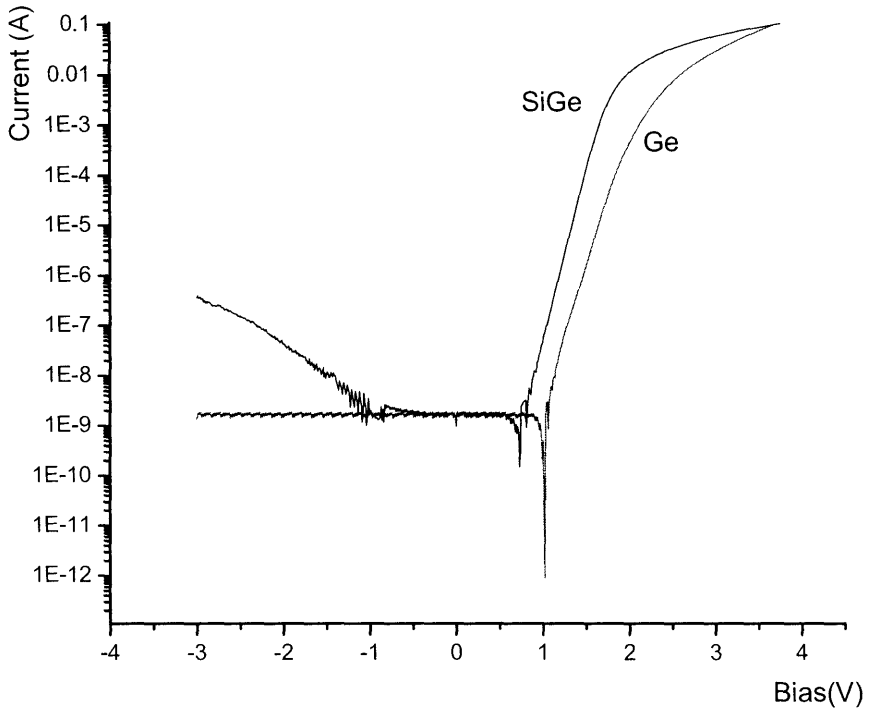


Figure 4.10: Semi-log I-V plot of p^{++}-Si capped LED on SiGe buffers and bulk Ge substrates.

L-I curves for the p^{++}-Si capped LEDs on Ge and SiGe virtual substrates are shown in Figure 4.11. It should be noted that the light output reported is not calibrated to reflect the collection efficiency of the measurement setup. Despite the increased leakage currents for devices on SiGe, these devices have a higher light output than similar devices on bulk Ge. There are a few possible explanations for this. For a given current level, the devices on SiGe have a lower forward voltage, and therefore lower joule heating. Further, the higher thermal conductivity of Si on which the SiGe buffer is grown could play a role in the removal of generated heat, thereby causing an increase in the light output.

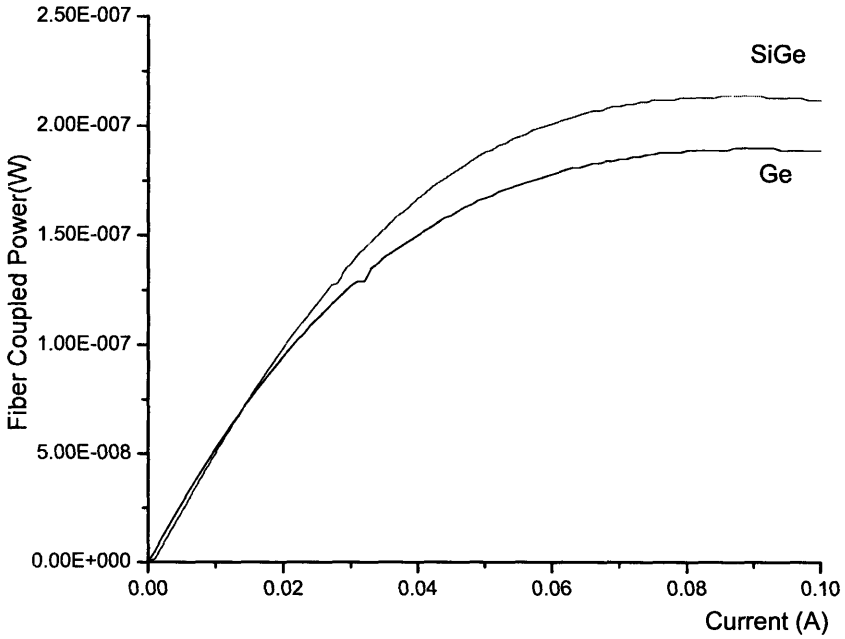


Figure 4.11: L-I curves of p^{++}-Si capped LED on SiGe buffers and bulk Ge substrates.

Figure 4.12 shows the concentration profile of Si, Ge, As and Al in the P^{++}-Si capped LED stack on SiGe graded buffer substrate obtained by SIMS. The large Si tail into GaAs might be a SIMS artifact, namely the knock-in of Si by ion bombardment. The n-GaAs and n-AlGaInP were intentionally doped with Si to about $5x10^{17}$ cm^{-3} whereas the active region was nominally undoped. It is seen that the Si dopant atoms redistribute during growth doping the active layer in the process. Similarly, the Ge atoms also autodope the epitaxial layers. The Ge concentration in (Al)InGaP layers is actually lower than that shown; the inaccuracy arising due to nonavailability of a calibration standard for Ge in (Al)InGaP. Figure 4.13 shows the concentration profile of the intentional dopant species (B and Zn) for the same sample. It is seen that the Zn dopant atoms redistribute during growth doping the active layer in the process.

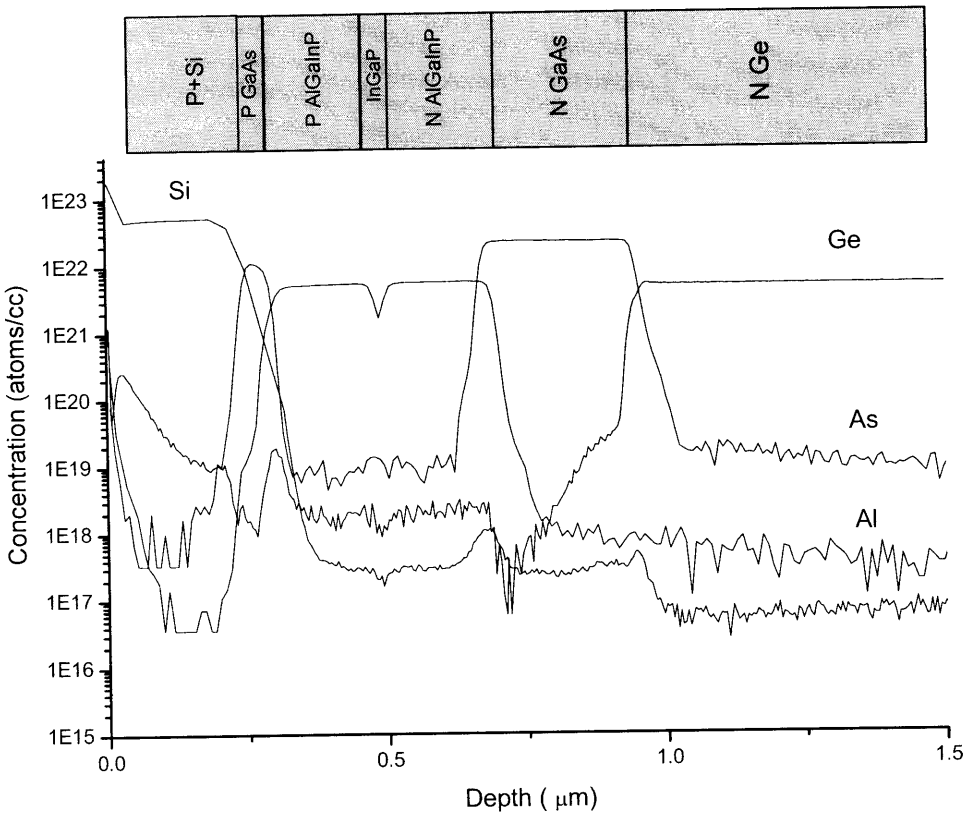


Figure 4.12: SIMS data for P^{++}-Si capped LED stack on SiGe graded buffer substrate.

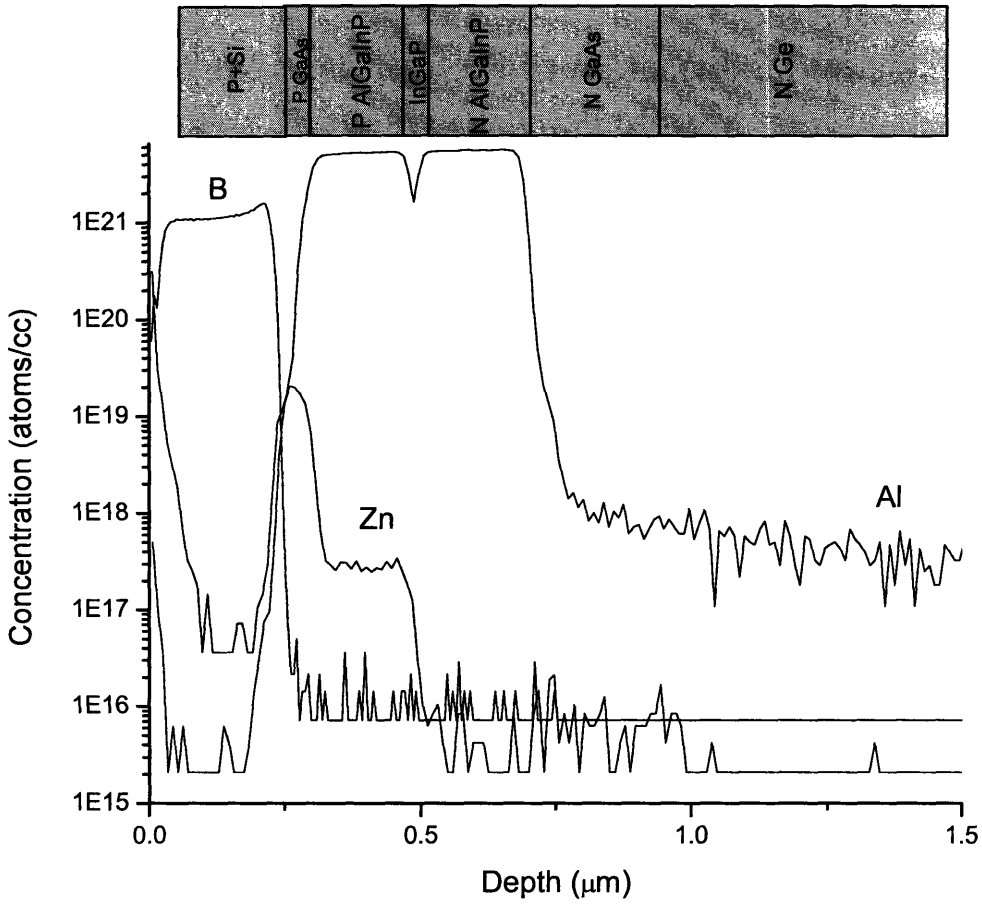


Figure 4.13: SIMS data for P^{++}- Si capped LED stack on SiGe graded buffers showing the B and Zn concentrations.

In summary, it is seen that Si capped devices have a higher forward voltage compared to uncapped devices, indicating an additional voltage drop at the Si/GaAs junction. The light output was higher for Si capped devices which might be due to increased current spreading attributable to the Si cap. Comparison of Si capped LEDs on SiGe virtual substrates with similar devices on bulk Ge substrates showed that the devices on SiGe substrates have a lower forward voltage and higher reverse leakage currents. Despite the leakage, light output power of these devices was higher than that of devices on bulk Ge. Spectral response showed a shift of the peak intensity to higher wavelengths for the devices on SiGe virtual substrates.

CHAPTER 5

Design and Fabrication of Monolithic CMOS-Compatible Visible LED Arrays on Silicon

5.1 Introduction

Armed with a better understanding of the p^{++}-Si/p^{+}-GaAs, n-GaAs/n-Ge heterojunctions and the results from the design and fabrication of the AlGaInP LED on SiGe virtual substrates, we now move on to the ultimate objective of this work – the design and fabrication of CMOS compatible visible LED arrays on silicon. This chapter begins with a description of the different LED array schemes used in contemporary designs and then discusses challenges that are unique to our material system. Next, the LED array photomask design and corresponding microfabrication process development are presented.

5.2 Two Dimensional LED arrays

Matrix addressed two-dimensional LED arrays are basically of two types, active matrix and passive matrix. In the active matrix scheme of addressing, each pixel has a dedicated transistor that actively maintains the LED state (ON or OFF) while other pixels are being addressed. This prevents crosstalk from inadvertently changing the state of an unaddressed pixel. Active matrix addressing is very popular in contemporary solid state displays where thin film transistors are used to maintain the pixel state. In a passive matrix scheme, each LED does not have a dedicated transistor to maintain its state. Thus passive matrix addressing schemes rely on persistence of vision of the human eye or on a bi-stable pixel, which maintains its state indefinitely without the need for individual transistor elements.

Since device-quality silicon for transistor fabrication is not present underneath the III-V material, our material system inevitably calls for a passive matrix LED array wherein the AlGaInP LED will be fabricated on Ge using a GaAs buffer layer and the driver transistors can be located in the adjacent silicon, thus achieving monolithic integration. One important requirement for correct operation of the passive matrix addressing scheme is device isolation. Isolation in commercial displays is achieved by

fabricating III-V LEDs on semi-insulating GaAs substrates or organic LEDs on insulating glass substrates. This choice of substrate allows for isolation of the individual LEDs. Since the SiGe virtual substrate used in this work is not insulating, the array design should incorporate some sort of an isolation scheme. One such scheme popular in the silicon VLSI industry is "junction isolation". To achieve junction isolation, the SiGe graded buffers are doped p^- ($\sim 10^{16}$ cm^{-3}) during growth and the Ge cap is doped n^+ ($\sim 1.5 \times 10^{18}$ cm^{-3}). This doping scheme presents an n-p-n structure underneath the LEDs and ensures that at least one of the p-n junctions is reverse biased during operation, thereby isolating the LEDs at the bottom (Figure 5.1). The SiGe was doped lightly (p^-) to reduce conduction through the bulk in case the reverse biased n^+-Ge/p^--SiGe junction is leaky. One-dimensional arrays do not require such an isolation scheme and dielectric isolation at the sides is sufficient for their successful operation.

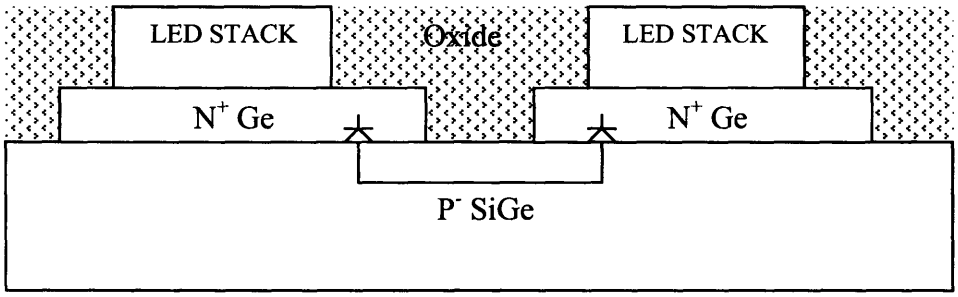


Figure 5.1: Schematic showing the concept of junction isolation to prevent cross-talk between pixels.

5.3 LED Array Photomask Design

A total of eight photomask levels were required to implement a two-dimensional LED array process and six photomask levels for a one-dimensional array. The mask layout was done using Tanner L-EDIT® Pro, a commercial CAD layout software. L-EDIT® converts the layout into machine-readable format called "GDSII" wherein each mask level is assigned a unique GDSII number. The unique GDSII number helps the mask writer differentiate between the different mask levels. This GDSII file was sent to the vendor for mask fabrication.

A 1:1 chrome on soda-lime substrate photomask was ordered. In a 1:1 contact mask, the features on the mask are transferred to the wafer without any scaling. The eight mask levels were tiled on two 5 inch soda-lime plates as shown in Figure 5.2. Note that the mask patterns are located inside a half inch border from the plate periphery. This is specific to the contact aligner. The mask holder used is a 6" x 6" flat piece of metal that holds the photomask in place. It has a 2"x2" square hole in the center through which the wafer can be exposed to UV light. A vacuum groove spaced by 0.5" from the periphery of this hole firmly secures the mask in place during alignment.

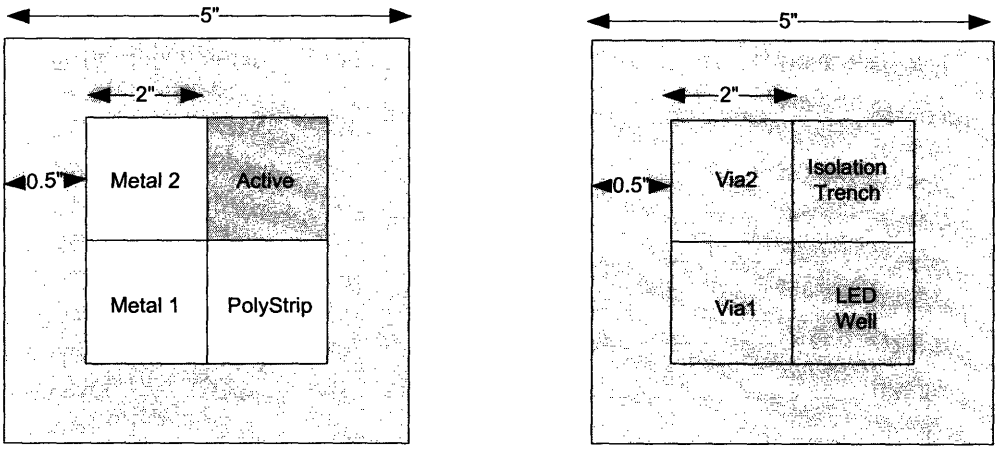


Figure 5.2: Schematic of the Photomasks. Levels Polystrip, Metal 1 and Metal 2 are bright field while Active, Isolation trench, LED well, Via 1 and Via 2 are dark field.

5.3.1 LED Array Mask Layout

Good mask layout design must take into account the "critical dimension" and "critical overlay tolerance" of the microfabrication process. Critical dimension is the minimum feature size that can be successfully transferred from the mask onto the photoresist. This is governed by diffraction limits of the optics, development/UV exposure time, exposure energy level etc. All feature widths in the mask layout were kept greater than or equal to 3 μm (critical dimension). The critical overlay tolerance is the accuracy with which the features on the mask can be aligned with those on the wafer. This depends on the user skill and equipment used. The smaller the separation between the mask and wafer, the easier it is for the microscope to resolve features on the photomask and wafer at the same time which is important for high resolution alignment. With 20X microscope objectives and a separation of 30 μm between the wafer and mask

during alignment, a critical overlay tolerance of about 2μm can be achieved on the contact aligner.

Figure 5.3 shows the photomask layout for a 2" wafer. There are a total of eight dies on the layout, two dies per quadrant, all located inside a 40mm diameter circle. It is not prudent to pattern the wafer upto the edges since wafer handling and beading up of photoresist can reduce device yield at the edges. Four sets of global alignment marks can also be seen along the horizontal and vertical diameters. The surrounding dies have 4x4 and 1x5 LED arrays drawn with 3 μm, 5 μm or 10 μm design rules. Each die has its own set of local alignment marks that can be useful when working with wafer pieces. TLM structures and mesa diode patterns are also included in each die (Figure 5.4). A 100x100 LED array drawn with 10 μm design rules is located at the center of the wafer. A cross-section and plan view of a pixel in the 100x100 array is shown in Figure 5.5.

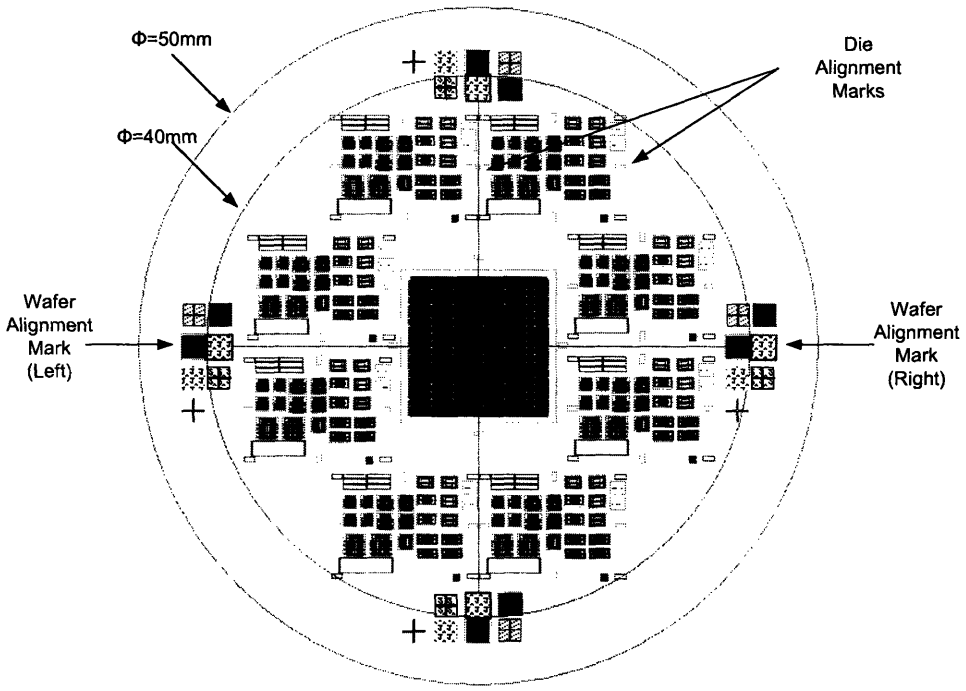


Figure 5.3 : Photomask layout for a 2" wafer.

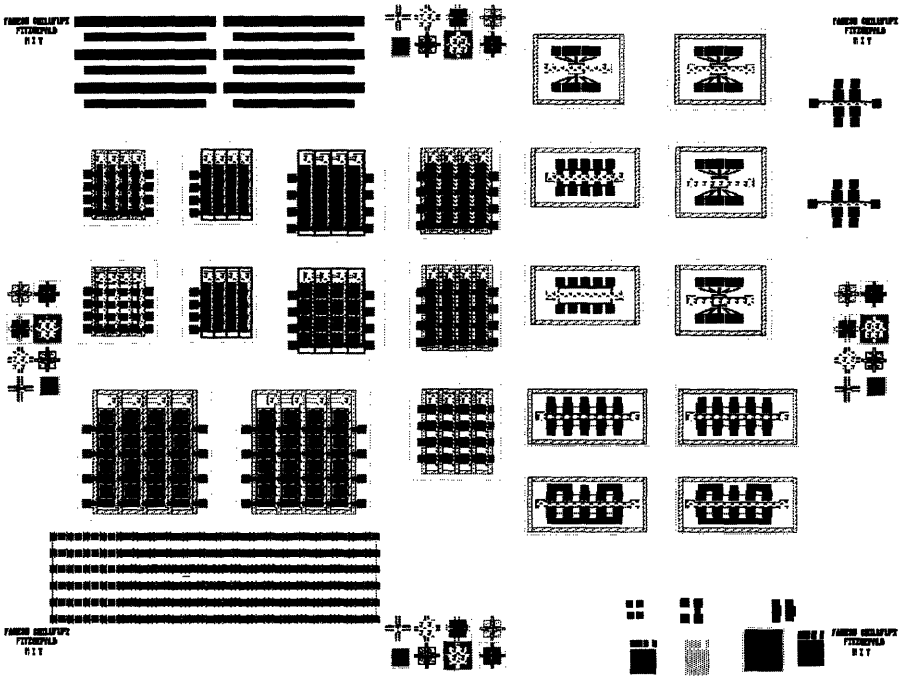


Figure 5.4: Layout of the die showing different LED arrays, the TLM and mesa diode structures and alignment marks.

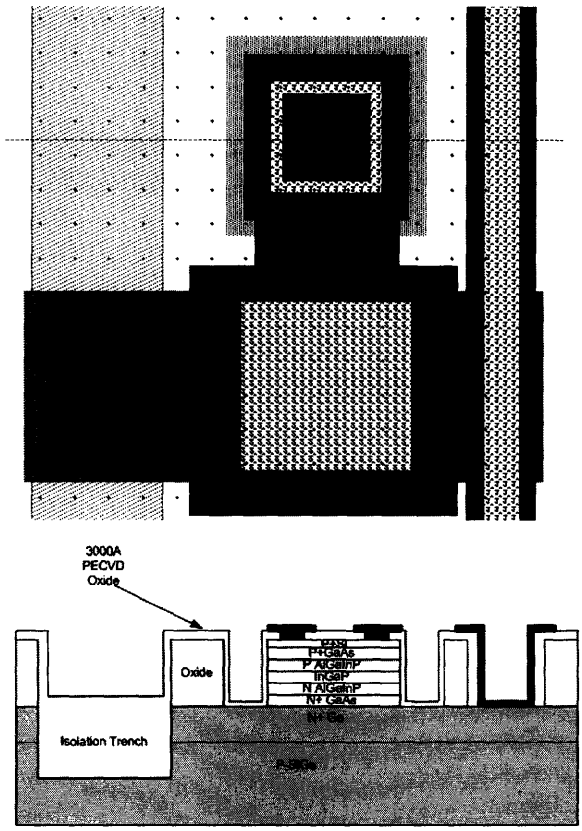


Figure 5.5: A pixel in the 100x100 central LED array - plan and cross-section views.

In photomask design, care must be taken to ensure that the layout design fits the LED array fabrication process and vice versa. The features in the layout were drawn with wet etch undercut compensation. A BOE solution etch of oxide is usually isotropic and thus 1 μm vertical etch causes a 1 μm lateral etch. A 1 μm bias was added to the features in the LED growth well, Via1 and Via2 levels to compensate for this undercut. It was assumed that the polycrystal material etch was isotropic and compensation was added here as well.

5.3.2 Alignment Mark design

Alignment marks are necessary to overlay the eight mask levels with minimal X, Y or 'θ' misalignment. While a single set of alignment marks (left/right/top/bottom) are sufficient for alignment in the X and Y directions, two sets of alignment marks (left and right or top and bottom) are required for both translational and rotational alignment.

Since the range of motion of the contact aligner microscope objectives is limited; *i.e.*, the left and right microscope objectives cannot be brought closer than about 40mm, the center-to-center separation of wafer level alignment mark pairs should be at least 40mm. Die level alignment can be done with a single microscope objective therefore a separation of less than 40 mm is acceptable for die alignment mark pairs.

Alignment marks are typically written onto the wafer (henceforth called 'target marks') and layer to layer registration is achieved by 'matching marks' on the next layer. Matching marks on the mask align to targets already etched on the wafer in the previous mask level. Contact aligners can use any shape as alignment marks. In this design, a cross was used as the target mark and its complement was used as the matching mark. Though having all target marks in the first level is convenient from the process point of view, when layer pair alignment is critical (as in LEDwell-Polystrip, Polystrip-Via 1, Via 1-Metal 1 layers of this process), it is best to have a layer provide the target mark only for the immediately succeeding layer.

Alignment marks should be designed to ensure that they are not removed during processing. A safe alignment mark thickness in order to prevent the undercut associated with isotropic etching from wiping away the marks is 10μm. Target marks on a dark field layer should have abutting clear areas to facilitate finding the underlying target marks.

The alignment marks were designed according to the above guidelines. A global alignment mark set consists of eight alignment marks as shown in the figure in Appendix D. Typical bright field target and matching marks are used in level 4 and typical dark field matching and target marks are used in level 2. The alignment marks are 1.6mm on a side to facilitate viewing the features on the wafer through big clear windows on a dark field mask.

5.4 LED Array fabrication

The CMOS compatible LED array process is outlined in the table given in Appendix B where each step corresponds to a photomask level. The schematic process sequence is also given in Appendix B. The detailed processing recipes can be found in Appendix A.4.

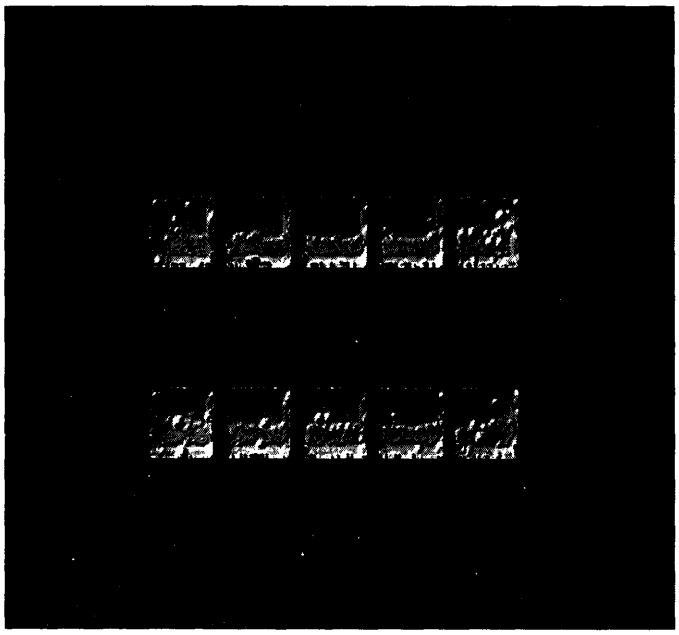
The LED array process begins with spin-coating positive photoresist on a 6" SOLES wafer and pre-baking it at 90°C for 30 mins. The wafer was then diced into square pieces of side 36mm. This corresponds to a 2" diagonal which is just the right size to fit in the 2" susceptor of the MOCVD reactor. The square pieces were then soaked in acetone for 2 hours and a subsequent 10 min Piranha clean and thorough DI water rinse was employed to remove the photoresist and any particles lodged in the resist during the wafer sawing process.

Next, a SF_6:O_2 (10:1) plasma dry etch and DI: BOE (3:1) solution wet etch were used to etch the Si and SiO_2 respectively to reveal the underlying germanium cap of the SiGe buffer. A wet chemical etch was selected to remove the SiO_2 since a dry etch could possibly roughen the Ge surface making it unfit for subsequent epitaxial growth. This etch also writes the level 1 target mark in the Si/SiO_2 and exposes the underlying Ge cap of the SOLES wafer in two boxes in the alignment mark area as shown in Appendix D. Using an SF_6:O_2 (10:1) plasma the exposed n^+-Ge was next dry-etched in designated areas to define 1 μm deep isolation trenches. The absence of an etch stop layer in the graded buffer necessitated a timed etch for this step. In order to better control the etch depth, ECR reactive ion etching was selected in preference to wet chemical etching. Level 2 target marks were also written into the Ge in this step.

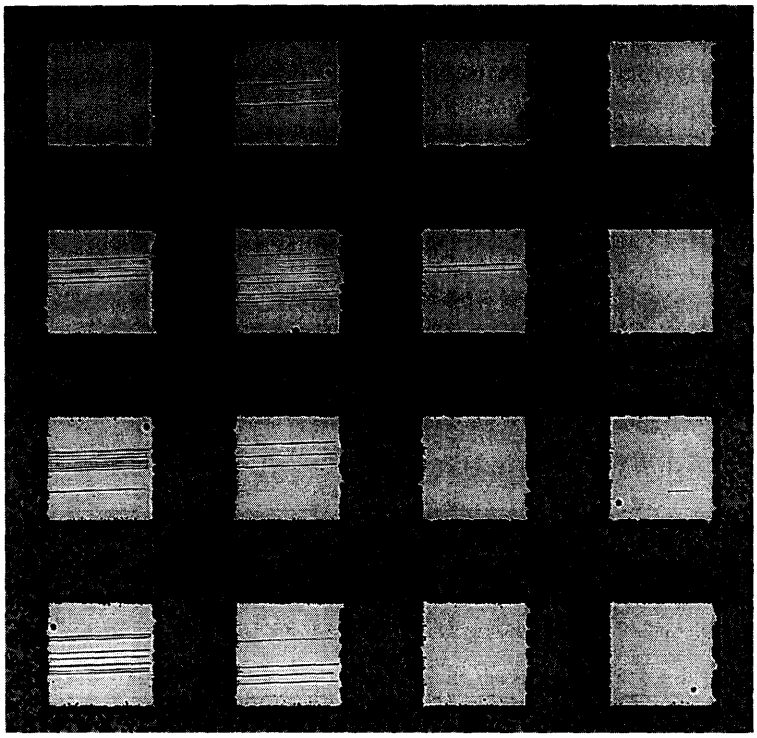
A 1.2 μm conformal PECVD oxide was next deposited on the wafer. This oxide serves two purposes. It provides a template for epitaxy and at the same time fills up the

isolation trenches. A DI: BOE (3:1) solution was then employed to etch square shape growth wells in the oxide layer and expose the underlying n^+-Ge for epitaxial growth. An oxide target mark was also written in this step and an adjacent square oxide well was etched. After this step, it is imperative that the wafer be free from all photoresist residues for MOCVD growth. To ensure this, commercial photoresist stripper (Microstrip 2001® by Fujifilm) in addition to a 1 hour ash step was used. 1-methyl-2-pyrolidinone (NMP) is a good solvent for photoresist and is an active component of Microstrip 2001®. The strip sequence used was Microstrip 2001® 10 min, methyl alcohol 30s, isopropanol 30s, DI water rinse 1min and nitrogen blow dry. Upto this step the process is CMOS compatible.

After a 1 hour ash step, the patterned wafers were transferred from the clean room to the substrate engineering laboratory for MOCVD growth of the LED stack. After an optional pre-growth clean using 10:1 DI: HF 15s, H_2O_2 15s, 10:1 DI: HF 15s the wafers were loaded into the MOCVD reactor for growth. While single crystal material growth occurred in the oxide wells, polycrystalline material was deposited on the oxide. A Nomarsky micrograph showing the single crystal material in the oxide wells and polycrystal deposits on the surrounding oxide is shown in Figures 5.6 (a) and (b).



(a)



(b)

Figure 5.6: Nomarski image showing single crystal material in (a) 36 µmx36 µm growth wells (poly-etch mask size will be 22µmx22µm). (b) 122 µmx 122µm growth wells (poly-etch mask size will be 102µmx102µm) of a portion of the central LED array.

After MOCVD growth, the wafers were transferred back into the clean room for all subsequent processing starting with the removal of the polycrystalline deposits. Since this involves etching III-V material and possibly contaminating CMOS tools, a dedicated etching tool can be used for this step. Both a wet etch (HCl: H_3PO_4: H_2O 1:1:1) and dry etch (CH_4:H_2) with a positive photoresist mask were tested for the AlGaInP LED stack etch. Inspection under the microscope revealed that the photoresist mask was easily attacked and eroded by both the dry and wet etch chemistry. Therefore the photoresist mask was replaced with a 3000 Å PECVD oxide hard mask. The oxide mask was patterned using a positive photoresist mask and 3:1 DI: BOE solution. Repeating the dry and wet etch and observation under microscope showed that the oxide mask was not damaged. A dry etch was investigated since it promised a single etch chemistry to etch the entire LED stack. Though the material could be dry etched, the CH_4/H_2 gas chemistry left a hydrocarbon residue on the wafer surface. Further, the hydrocarbons deposited on the oxide mask hindered the subsequent removal of the mask by BOE wet etch. The

CH_4/H_2 chemistry was also slow and took about 30 minutes to etch 1 μm of the LED stack. Therefore, the dry etch was discarded.

The HCl-based wet etch on the other hand, is cleaner, faster (requiring 2 minutes to etch the AlGaInP LED stack) and yields smoother surfaces. A wet etch also causes lateral undercut which can be useful. As detailed in the mask design section, the minimum critical overlay accuracy used for mask design was 2 μm. In some arrays of the die, the polystrip oxide hard mask was designed to overhang the LED well by 2 μm. Thus, in such arrays, a 2 μm polycrystalline lip will remain along the perimeter of the LED well after the polycrystalline material etch. An anisotropic wet etch causes lateral undercut that partially eats through the lip reducing its thickness.

Considering all these advantages, ultimately the wet etch method was chosen to etch the AlGaInP stack. It was found that the HCl-based wet etch chemistry was selective to the p-AlGaInP/InGaP/n-AlGaInP stack and did not etch GaAs. A 3:1:50 H_3PO_4:H_2O_2:H_2O solution was used to etch the p-GaAs current spreading and n-GaAs buffer layers. The Si cap was dry etched using a SF_6/O_2 (10:1) plasma. During this step a target mark was also etched into the single crystal material grown in the oxide well in the alignment mark area. After the combination of dry and wet etch was complete, the oxide hard mask was stripped using a DI: BOE (3:1) wet etch. For wells with oxide mask overhang, poor adhesion of the polycrystalline material to oxide caused the polycrystalline lip to be completely removed during the wet etch removal of the oxide hard mask, yielding a planar surface.

The next step was to insulate the LED mesa sidewall by depositing 0.3 μm PECVD SiO_2. Sidewall insulation reduces the diode leakage current and prevents metal 1 from shorting the LED p-n junction at the mesa sidewall. Via 1 was next etched in the oxide to expose the p^{++}-Si encapsulation layer and the n-Ge layer for subsequent ohmic contact formation. It should be noted that while the anode oxide cut is only 0.3 μm deep, the cathode cut is about 1μm deep. Thus the anode cut is laterally undercut by 1 μm and not 0.3 μm during the wet etch. Target marks for level 6 were also written into the oxide in this step.

Next 500 Å Ti and 1 μm Al was sputtered on the wafer and patterned using a 1000: 15 DI: BOE solution and the PAN (77% Phosphoric acid, 20% Acetic acid, 3%

Nitric acid) etch respectively. Cathode/anode contacts and the row/column interconnect were defined in this layer. The anode metal was designed as an annular ring to promote current spreading and improve the uniformity of light emitted from the diode. Sputtering and wet etch which is CMOS compatible and yields better step coverage was preferred over e-beam evaporation and non-CMOS compatible liftoff process for the Ti/Al metal contact formation. Ti/Al target marks for both level 7 and level 8 were written in this step One-dimensional LED arrays were ready to be tested at this stage.

Via 2 and metal 2 are required for fabricating a two-dimensional array. Though these steps were not performed on the actual wafer, the process was developed on a dummy wafer. A conformal interlevel dielectric layer consisting of 3000 Å oxide was deposited by PECVD. Conventional BOE cannot be used to etch via 2 in the insulating interlevel dielectric since the HF in BOE attacks the underlying aluminum, so "Silox Vapox III" etchant from Transene® was used. Silox Vapox III has been designed to optimize etching of a deposited oxide passivation layer over an aluminum metallized silicon substrate. This etchant has been saturated with aluminum to minimize its attack on the metallized substrate. It was seen that 0.3 μm of interlevel dielectric (PECVD oxide) was etched by the chemical in about 60 seconds and no significant damage to the aluminum metal could be observed under the microscope (20x magnification). 1 μm Al was next sputter-deposited and patterned with the PAN etch to complete the metal 2 level.

5.5 Results and Discussion

The LED array fabrication was successful. The large bond pads (100 μmx100 μm) permitted the LEDs in the array to be directly micro-probed. Figure 5.7 shows pixels of a ~600dpi LED array biased at 50mA. The LEDs are 20 μmx20 μm in size and the array pitch is 40μm. Device-quality silicon is present in the crosshatch region at the LED array periphery. Thus device-quality Si and working III-V semiconductor based LEDs have been successfully brought together on a common substrate achieving monolithic integration. Figure 5.8 shows a LED array fabricated using 5 μm design rules. The LEDs are 100 μmx100 μm in size and the array pitch is 200 μm. The five LEDs in the bottom row and two pairs of LEDs in the top row have been shorted.

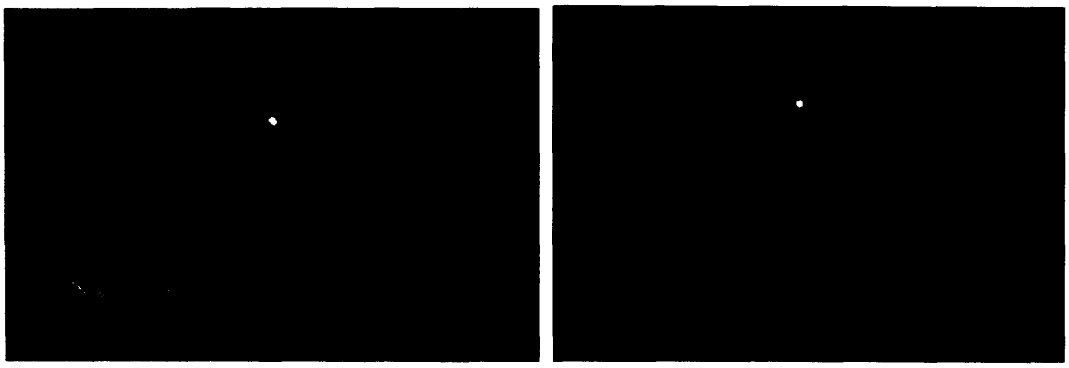
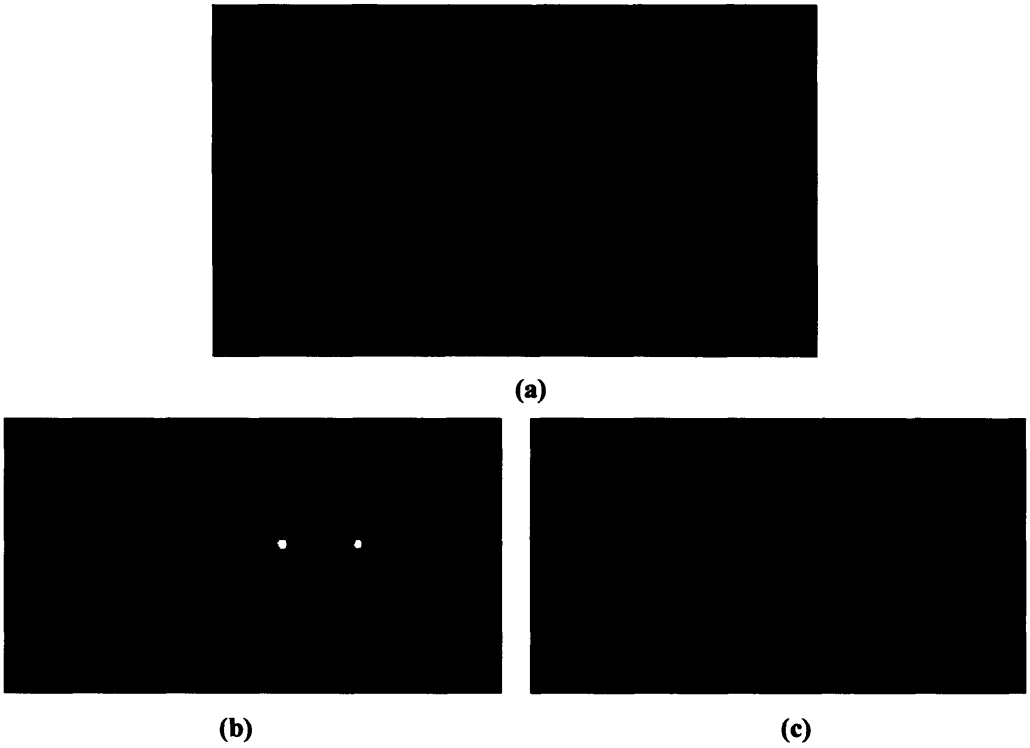


Figure 5.7: 20 μmx20 μm LED; 3 μm critical dimensions;Array pitch =40 μm (~ 600dpi) driven at 50mA current. The contact pads are 100 μmx100 μm squares.



(a)

(b) **(c)**

Figure 5.8: (a) Unbiased LED array. (b) Top LED pair at 50mA bias (c) Bottom row at 50mA bias. In (b) and (c) all ambient light sources have been turned off.

Figure 5.9 shows a pixel in the 100x100 central LED array biased with a drive current of 50mA. The electro-luminescence spectrum for the pixel is shown in Figure 5.10. The peak intensity occurs at 671 nm and the FWHM is 30 nm. The higher-than-target wavelength could be attributed to selective area epitaxy which leads to increased

Indium incorporation and active region thickness in the oxide growth wells. A cross-sectional TEM image of the material in the oxide wells is shown in Figure 5.11. The thickness of the layers in the heterostructure was quite different from the target. For example, the n-GaAs layer is 888nm thick whereas the target thickness was 500nm.

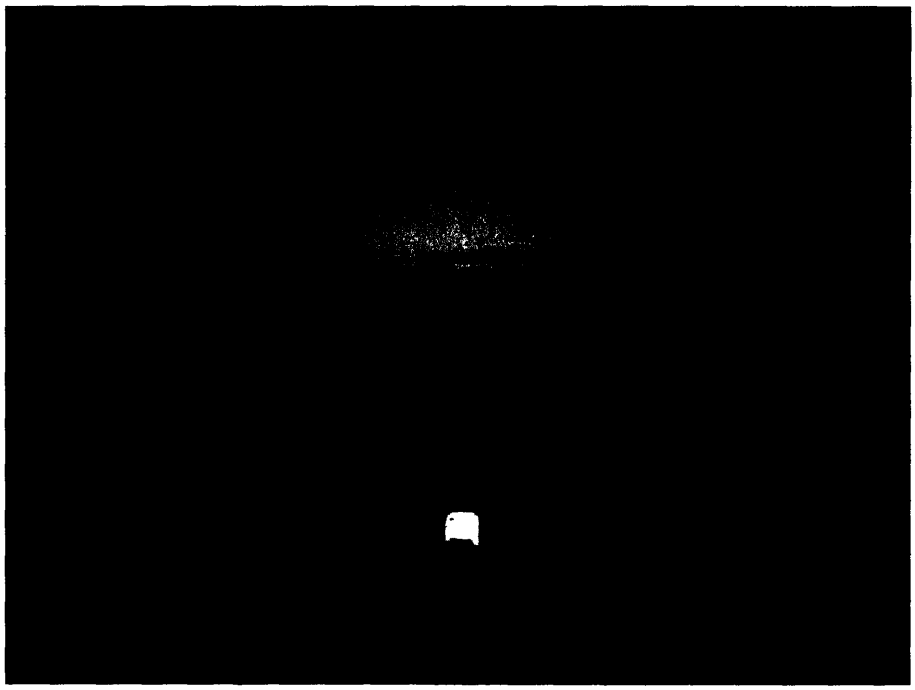


Figure: 5.9 A pixel in the central 100x100 array biased at 50mA.

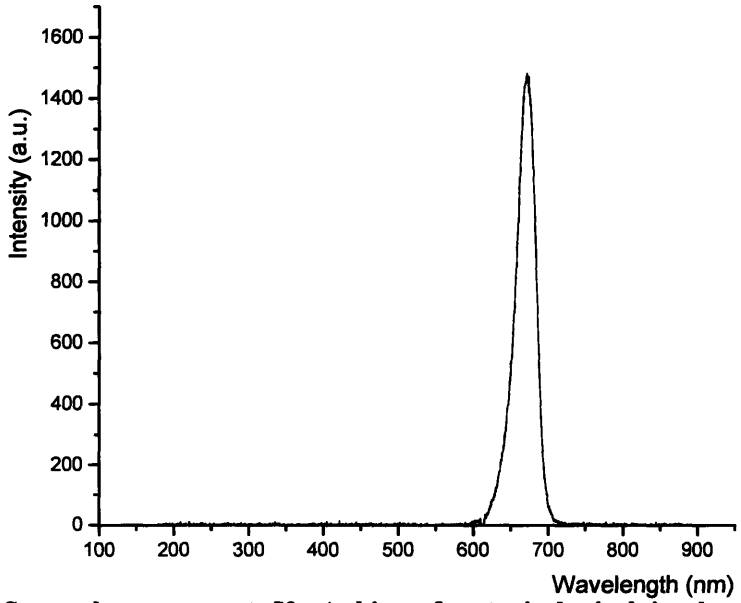


Figure 5.10: Spectral response at 50mA bias of a typical pixel in the central array

Figure 5.11: Cross-sectional TEM image of the material grown in a typical oxide well of the central 100x100 array. Courtesy Mike Mori.

The I-V curve for the pixel is shown in Figure 5.12. The forward voltage at 50mA is 4.9V. The relatively high forward voltage can be attributed to a Schottky Ti/Al contact to the n-Ge which was doped to $1.5x10^{18}$ cm^{-3}, the maximum that can be obtained in our UHVCVD reactor. Doping by ion implantation at a dose of $4x10^{15}$ cm^{-2} (about 10^{20} cm^{-3}) is required to obtain ohmic Ti/Al contacts to n-Ge [19].

The L-I curves for the pixel are shown in Figure 5.13. It should be noted that the light output reported is not calibrated to reflect the collection efficiency of the measurement setup. The L-I curves are near linear till about 70mA current after which they peak and the light output falls with further increasing current. This could be due to joule heating at high current densities causing device efficiency to drop.

In summary, a micro-fabrication process for making the one-dimensional and two-dimensional LED arrays on SOLES platform was developed and a corresponding eight-level photomask was designed. Using six of the eight mask levels, a monolithic CMOS-compatible visible LED array was successfully fabricated and demonstrated.

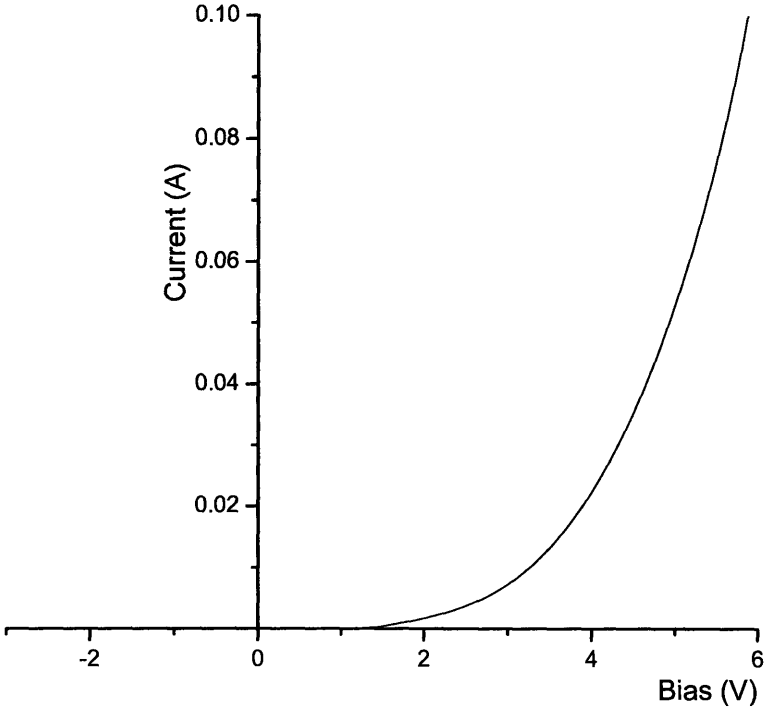


Figure 5.12: I-V characteristic of a typical pixel in the central 100x100 array.

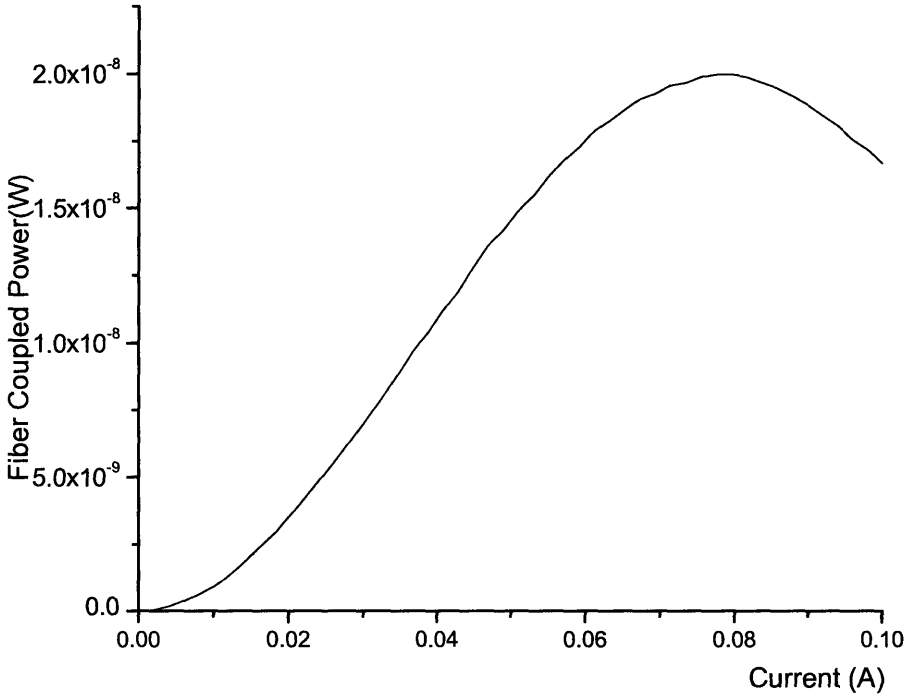


Figure 5.13: L-I curve for a typical pixel in the central 100 x 100 array.

CHAPTER 6

Conclusions and Future Work

6.1 Summary of accomplishments

This work has demonstrated the first prototype monolithic CMOS compatible visible AlGaInP LED array on silicon. One-dimensional LED arrays were fabricated as proof of concept. Potential applications for the one-dimensional arrays are in low cost, high performance, high resolution integrated optical printer heads.

Monolithic integration brings Si and III-V material to a common substrate and is attractive due to lower parasitics and cost than labor intensive hybrid integration schemes. In this work, a novel substrate called Silicon On Lattice-Engineered Substrate (SOLES) was successfully fabricated as the substrate for practical monolithic integration. SOLES comprises a compositionally graded SiGe virtual substrate on which a thin layer of device quality Si has been transferred by wafer bonding and hydrogen-induced exfoliation.

For the visible LED, a double-heterojunction structure was developed with AlGaInP cladding layers and InGaP active layer. The LED was encapsulated with heavily doped p-silicon to facilitate CMOS compatibility by preventing III-V exposure during processing. The n-GaAs cathode of the LED was accessed through the Ge cap of the SiGe graded buffers instead of etching III-V material. As a consequence, n-GaAs/n-Ge and p^{++}-Si/p^{+}-GaAs heterojunctions are introduced at the bottom and top of the LED stack respectively. To better understand the effect of these junctions on the resistance of the LED, mesa diodes were fabricated and current-voltage characteristics were measured. The n-GaAs/n-Ge junction showed rectification. This, along with SIMS data indicates the presence of a thin layer of p^{+}-Ge sandwiched between n-GaAs and n-Ge due to Ga autodoping. Evidence suggests that the n-GaAs/p^{+}-Ge interface is a tunnel junction and the forward voltage drop across the n-GaAs/n-Ge junction can be attributed to the forward biased p^{+}-Ge/n-Ge homodiode. The current-voltage characteristic of p^{++}-Si/p^{+}-GaAs heterojunctions was nearly linear indicating ohmic behavior. It is believed that since the Si cap is heavily doped, the holes tunnel through the junction resulting in a

straight line I-V curve. Similarly, the p^{++}-Ge/p^{+}-GaAs heterojunction showed ohmic behavior.

AlGaInP DH LEDs were fabricated on bulk GaAs substrates to evaluate the effect of the Si cap on the electrical and optical characteristics of the LED. Devices with the Si cap have higher forward voltage compared to uncapped devices, indicating an additional voltage drop in the LED series circuit. L-I curves show that the light output is higher for devices with Si cap which might be due to higher extraction efficiency resulting from increased current spreading attributed to the Si cap. The spectral response showed that the peak wavelength for devices with Si cap was higher than for devices without the cap.

AlGaInP LEDs with heavily-doped Si cap grown by MOCVD on SiGe virtual substrates were demonstrated for the first time. Comparison with similar devices on bulk Ge substrates showed that the devices on SiGe have a lower forward voltage and higher reverse leakage currents. Despite the leakage, light output power of these devices was higher than that of similar devices on bulk Ge. The spectral response showed a shift of the peak intensity to higher wavelengths for the devices on SiGe graded buffer.

A micro-fabrication process for making the one-dimensional and two-dimensional LED arrays on SOLES platform was developed and a corresponding eight-level photomask was designed. Using six of the eight mask levels, a one-dimensional monolithic CMOS-compatible visible LED array was successfully fabricated and demonstrated.

6.2 Suggestions for future work

With LED arrays successfully integrated on the SOLES platform, the next step is to demonstrate monolithic optoelectronic integrated circuits by combining the LED with CMOS driver circuits fabricated in the device-quality Si adjacent to the III-V material. The fabrication process and photomask developed for two-dimensional arrays can be used to demonstrate an integrated passive matrix display on the SOLES platform in the future.

Despite the high pixel forward voltage and lower process yield for the first generation one-dimensional prototype LED arrays, great promise holds for future improvement. Doping the Ge cap of the graded buffer to 10^{20} cm^{-3} by ion-implantation will help form better ohmic contacts, thus reducing the forward voltage of the LEDs in

the array in addition to reducing the Ge bulk resistance. Implant simulations have to be performed and the implant dose and energy must be designed to take into account the dopant redistribution that will occur during the 650 °C, 43 minute growth of the LED stack. Further, using Ni Germanide instead of Ti Germanide for the ohmic contact will reduce the contact resistance. TLM structures incorporated in the photomasks can be used to extract the contact resistance for different metallurgies.

The silicon cap technology needs to be investigated further. Autodoping effects have to be investigated at the p^{++}-Si/p^{+}-GaAs interface. The I-V characteristics of p^{++}-Si/p^{+}-GaAs junction have to be studied and the Si doping density required to obtain a low resistance junction has to be explored. Cross-sectional TEM studies are required to gauge the thickness of the silicon cap consumed in the silicide reaction.

The LED device efficiency can be improved by increasing the aluminum content in the cladding layers to 70% and also by controlling the Ge autodoping of device layers in future work. Suitable cleaning procedures can be employed to remove Ge sources in the reactor environment thereby reducing Ge contamination of device epilayers [6]. Further research is also required to control the active layer thickness and composition of the LED material grown in oxide wells.

Demonstration of LED arrays on full 6" wafers is important to prove the commercial feasibility of this process. Using 6" or higher diameter wafers with separate dedicated tools for etching the polycrystalline III-V material can transfer the process developed in this work to existing commercial Si CMOS fabs. After etching the polycrystalline deposits, the wafer can be coated with oxide and the remaining processing can be carried out in CMOS compatible tools. The Si encapsulation layer will prevent III-V exposure during further processing.

The prototype array demonstrated in this work is an important milestone towards the realization of the ultimate objective – monolithically integrated optical interconnects in high speed digital systems.

APPENDIX A.1

SOLES PROCESS SEQUENCE

Starting Material : 6" Silicon (Prime) , 6" Graded Buffer wafer.

Step	Process	Description	Lab	Machine
1	Modified RCA clean for Ge	Clean in preparation for LTO deposition	ICL	ICL RCA
2	7500Å LTO deposition on handle wafers		ICL	LTO tube 6C
3	Anneal wafers 600 °C, 2hours	Densify LTO	ICL	ICL – Tube 5B
4	CMP	Polish wafer surface	ICL	CMP
5	10 min 3:1 Piranha Clean (blue)	Post-CMP clean	ICL	Pre-metal hood
6	10 min 3:1 Piranha Clean (green)	Post-CMP clean	ICL	Pre-metal hood
7	RCA clean of donor wafers	Clean in preparation for thermal oxide growth	ICL	ICL RCA
8	Grow 20nm thermal oxide on donor wafers		ICL	ICL tube 5A
9	Implant donor wafers with H_2^+ for layer transfer		Outside vendor	
10	SC1 clean	Modified RCA clean of donor and handle wafers.(replace wafer box w/ a new one)	TRL	RCA-TRL
11	Bonding	SiO_2-SiO_2 bonding of donor and handle wafers	TRL	EV620 / EV501
12	Anneal in tube B3 (250 °C, 1 hour, 450 °C 1 hour.	Post-bond anneal and hydrogen induced exfoliation	TRL	Tube B3

APPENDIX A.2

GaAs/Ge Mesa Diode Process Sequence

Starting Material : MOCVD grown n-GaAs layers on bulk n-Ge substrates

Step	Process	Description	Lab	Machine
	Module I : "Diode Mesa"			
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)
2	a. Apply HMDS : resist adhesion promoter. b. Spin Coat Positive Photoresist (OCG 825) Spin speed 3 Krpm for 30sec. c. Soft-Bake at 90 °C for 30 min. d. Expose with Bright Field Contact Mask 1.5 s. e. Develop with OCG 934 1:1 for 1 min. f. Check for complete development under microscope. g. Hard-Bake at 120 °C for 30 min.	Pattern Diode Mesa (200 μm square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner Post-bake Oven
3	Immerse sample in H_3PO_4: H_2O_2: H_2O (3:1:50) solution (etch rate ~0.1 μm/minute) for 18 minutes. Sample was over-etched to ensure complete removal of GaAs.	Wet Etch 1 μm GaAs	TRL	Acid Hood 1(Red)
4	Ash wafer for 2 hours in Oxygen Plasma	To strip Resist	TRL	Barrel Asher
	Module II: " N GaAs ohmic contact"			
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)
2	a. Apply HMDS : resist adhesion promoter b. Spin Coat Image Reversal Photoresist (AZ 5214E) Spin speed 3.5 Krpm for 30sec. c. Soft-Bake at 90 °C for 30 min d. Expose with Bright Field Contact Mask 1.5 s e. Soft-Bake at 90 °C for 30 min f. Flood expose for 60 sec g. Develop in AZ 422 for 90 sec	Pattern n-GaAs contact(75 μm square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner
3	Ash wafer for 5 min in Oxygen Plasma	De-scum	TRL	Barrel Asher
4	Evaporate 500 Å Ni and 2000 Å AuGe eutectic alloy	n-GaAs Ohmic Metal	TRL	e-beam Au

5	Soak wafer in acetone bath for 10 min	Liftoff Photoresist	TRL	Photo Wet Station (Red)
Module III : " N Ge ohmic contact"				
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)
2	a. Apply HMDS : resist adhesion promoter b. Spin Coat Image Reversal Photoresist (AZ 5214E) Spin speed 3.5 Krpm for 30sec. c. Soft-Bake at 90C for 30 min d. Expose with Bright Field Contact Mask 1.5 s e. Soft-Bake at 90 C for 30 min f. Flood expose (No mask) for 60 sec g. Develop in AZ 422 for 90 sec	Pattern n-Ge contact (75 um square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner
3	Ash wafer for 5 min in Oxygen Plasma	De-scum	TRL	Barrel Asher
4	Evaporate 100A Au,500 A Ni, 2000A AuGe,300 A Ni	n-Ge Ohmic Metal	TRL	E-beam Au
5	Soak wafer in acetone bath for 10 min	Liftoff Photoresist	TRL	Photo Wet Station (Red)
6	Rapid Thermal Anneal 425 °C, 20 sec	Forms Alloyed Ohmic contacts	TRL	RTA35
7	Remove wafers for I-V characterization			

APPENDIX A.3

p^{++}-Si/p^{+}-GaAs Mesa Diode Process Sequence

Starting Material : MOCVD grown p^{++}-Si/p^{+}-GaAs stack on semi-insulating GaAs substrate.

Step	Process	Description	Lab	Machine
Module I : "Diode Mesa"				
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)
2	a. Apply HMDS : photo resist adhesion promoter b. Spin Coat Positive Photoresist (OCG 825) Spin speed 2 Krpm for 30sec c. Soft-Bake at 90C for 30 min d. Expose with Bright Field Contact Mask 1.5 s – Rotate wafer 90 degrees and expose again for 1.5s. 365-450nm wavelength at 10 mW/cm^2. e. Develop with OCG 934 1:1 for 1 min f. Check for complete development under microscope g. Hard-Bake at 120C for 30 min	Pattern Diode Mesa (200 μm square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner Post-bake Oven
3	Load Wafer is Dry etch system and etch with SF_6, O_2 Plasma for 200s.	Dry etch Si	TRL	PlasmaQuest
4	Check for complete Si dry etch using stylus profilometer	Check dry etch depth	TRL	Dektak Au
5	Immerse sample in H_3PO_4: H_2O_2: H_2O (3:1:50) solution (etch rate ~0.1 um/minute) for 4 minutes to wet etch any damaged GaAs.	Wet Etch 0.4 μm GaAs	TRL	Acid Hood 1 (Red)
6	Ash wafer for 2 hours in Oxygen Plasma	Strip Resist	TRL	Barrel Asher
Module II: " P^{+} GaAs ohmic contact"				
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)

2	a. Apply HMDS : resist adhesion promoter b. Spin Coat Image Reversal Photoresist (AZ 5214E) Spin speed 3.5 Krpm for 30sec. c. Soft-Bake at 90C for 30 min d. Expose with Bright Field Contact Mask 1.5 s e. Soft-Bake at 90 C for 30 min f. Flood expose (No mask) for 60 sec g. Develop in AZ 422 for 90 sec	Pattern n-GaAs contact (75 μm square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner
3	Ash wafer for 5 min in Oxygen Plasma	De-scum	TRL	Barrel Asher
4	Evaporate 50 A Ti 200A Pt and 2500 A Au.	p-GaAs Ohmic Metal contact	TRL	E-beam Au
5	Soak wafer in acetone bath for 10 min	Liftoff Photoresist	TRL	Photo Wet Station (Red)
Module III : " P^{++}-Si ohmic contact"				
1	Acetone/Methanol/Isopropanol/DI H_2O and Blow Dry with N_2 Gun	De-Grease Wafers	TRL	Photo Wet Station (Red)
2	a. Apply HMDS : resist adhesion promoter b. Spin Coat Image Reversal Photoresist (AZ 5214E) Spin speed 3.5 Krpm for 30sec. c. Soft-Bake at 90C for 30 min d. Expose with Bright Field Contact Mask 1.5 s e. Soft-Bake at 90 C for 30 min f. Flood expose (No mask) for 60 sec g. Develop in AZ 422 for 90 sec	Pattern n-Ge contact (75 μm square)	TRL	HMDS Oven Coater Pre-bake Oven EV1 Aligner
3	Dip wafer for 15s in 2% HF solution (480ml DI Water+ 20ml HF (49%))	Strip native oxide	TRL	Acid Hood 1 (Red)
4	Evaporate 500Å Ti, 1000Å Al	p-Si Ohmic Metal Contact	TRL	e-beam Au
5	Soak wafer in acetone bath for 10 min	Liftoff Photoresist	TRL	Photo Wet Station (Red)
6	Furnace anneal at 400°C for 40 min in forming gas ambient.	Forms Ohmic contacts	TRL	Tube B1
7	Remove wafers for I-V characterization			

APPENDIX A.4

AlGaInP LED Array Process Sequence

Starting Material: 6 inch SOLES wafer made using "SOLES process" (Appendix A.1)

Step	Process	Description	Lab	Machine
1	HMDS Spin-coat positive photoresist Prebake 30min 90 °C		TRL	TRL Photo Tools (Green) HMDS Coater Prebake Oven
2	Diesaw	Saw 6 inch wafer into squares of side 36mm	ICL	Diesaw
3	Acetone/Methanol/Isopropanol/DI	Post die-saw Clean	TRL	Solvent Hood(Red)
4	Dip in H_2SO_4:H_2O_2 (3:1) 10mins, DI water rinse, blow dry.	Post die-saw Piranha clean	TRL	Acid Hood 1 (Red)
5	Spin-coat positive photoresist at 3Krpm, Expose with Dark Field Contact Mask "Active" for 1.8s and Develop for 60s. Inspect pattern under microscope.	Pattern LED Array Area	TRL	TRL Photo Tools : (Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
6	Dry etch 0.25 μm Si	RIE etching : SF_6/O_2 plasma	TRL	Plasmaquest
7	Wet etch SiO_2	Buffered Oxide Etch	TRL	Acid Hood 1(Red)
8	Ash sample for 1 hour	Strip resist	TRL	Barrel Asher
9	Spin coat positive photoresist at 3Krpm, Expose with dark-field contact mask "Trench" for 1.8s and develop for 60s. Inspect pattern under microscope.	Pattern LED Array area	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
10	Dry etch 1.5 μm Ge. Inspect etch depth with profilometer.	RIE etching : SF_6/O_2 plasma	TRL	Plasmaquest
11	Ash sample	Strip resist	TRL	Barrel Asher

12	Deposit 1.2 μm PECVD oxide		TRL	STSCVD
13	Spin-coat positive photoresist at 3Krpm, Expose with dark field contact mask "Led-Well" for 1.8s and develop for 60s. Inspect pattern under microscope.	Pattern LED growth wells in oxide	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
14	Wet etch oxide, DI water rinse, blow dry	BOE etch	TRL	Acid Hood
15	Wet etch photoresist	Microstrip solvent	TRL	Solvent Hood (Red)
16	Ash sample	Strip remaining resist	TRL	Barrel Asher(Red)
17	Surface profiling	Measure etch depth	TRL	Dektak Au
18	15 sec HF: H_20 1:10, 15 sec H_2 0_2, 15 sec HF:H_20 1:10.	Optional pre-growth clean	TRL	Acid Hood 1 (RED)
19	Grow P^{++}-Si/P^{+}-GaAs/ p-AlGaInP/ InGaP/ n-AlGaInP/ n-GaAs.	LED heterostructure growth.	Substrate Engineering Lab : Building 13 first floor	MOCVD reactor
20	Deposit 0.3 μm PECVD oxide	Hard mask	TRL	STSCVD
21	Spin-coat positive photoresist at 3Krpm, Expose with Bright Field Contact Mask "Polystrip" for 1.8s and Develop for 60s. Inspect pattern under microscope.	Strip polycrystal deposits	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
22	Dip in 3:1 DI:BOE for 2 minutes	Pattern oxide hard mask	TRL	Acid Hood 1(Red)
23	SF_6/O_2 dry etch	Etch P^{++} Si cap	TRL	Plasmaquest
24	Ash 1 hour	Strip resist	TRL	Barrel asher
25	(H_3PO_4:H_2O_2:H_2O 3:1:50) Dip, (H_3PO_4: HCl: H_2O 1:1:1) Dip, (H_3PO_4:H_2O_2:H_2O 3:1:50) Dip DI water rinse, spin dry.	Wet etch p-GaAs , p-AlInGaP/ InGaP/ n-AlGaInP, n-GaAs respectively	TRL	Acid Hood 1(Red)
26	Dip in 3:1 DI:BOE for 2mins	Strip oxide hard mask	TRL	Acid Hood 1(Red)
27	Deposit 3000 Å PECVD Oxide	LED Mesa	TRL	STSCVD

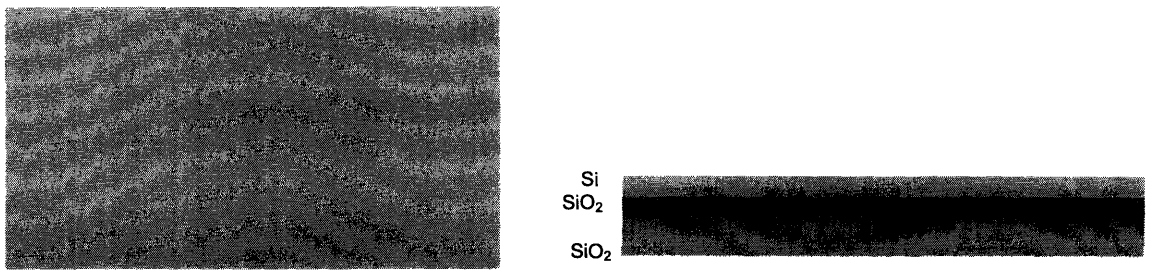
		Sidewall Passivation		
28	Spin Coat Positive Photoresist, Expose with Dark Field Contact Mask "Via1" and Develop.	Pattern Via 1	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Post-bake Oven
29	Buffered Oxide Etch dip, DI water Rinse, Spin Dry	Wet Etch Oxide	TRL	Acid Hood 1(Red)
30	Strip photoresist		TRL	Barrel Asher (Red)
31	Sputter 500 Å Ti and 1 μm Al	Metal level 1	TRL	Perkin Elmer
32	Spin Coat Positive Photoresist, Expose with Clear Field Contact Mask "Metal 1" and Develop.	Pattern metal level 1	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
33	Dip in PAN etch 25minutes(room temperature), DI water rise 2 minutes, 1000:500 DI:BOE for 1 minute	Wet etch Ti/Al stack.	TRL	Acid Hood 1 (Red)
34	Strip resist		TRL	Barrel asher(Red)
	1-D array process complete			
35	Deposit 3000 Å PECVD Oxide	Inter-metal dielectric	TRL	STSCVD
36	Spincoat positive photoresist, expose with dark field contact mask "Via 2" and develop.	Pattern Via 2	TRL	TRL Photo Tools :(Red) HMDS Coater Prebake Oven EV1 Aligner Develop Postbake Oven
37	Silox-Vapox III etchant dip, DI water Rinse, Spin Dry	Wet etch oxide	TRL	Acid Hood 1(Red)
38	Strip photoresist		TRL	Barrel Asher (Red)
39	Sputter 1 μm Al	Metal level 2	TRL	Perkin Elmer/

40	Spincoat positive photoresist, Expose with Clear Field Contact Mask "Metal 2" and Develop.	Pattern metal 2	TRL	TRL Photo Tools :(Red) HMDS Coater PrebakeOven EV1 Aligner Develop Postbake Oven
41	Dip in PAN etch 25minutes, DI water rinse	Wet etch Al	TRL	Acid Hood (Red)
42	Strip resist		TRL	Barrel asher(Red)
43	Remove from TRL			

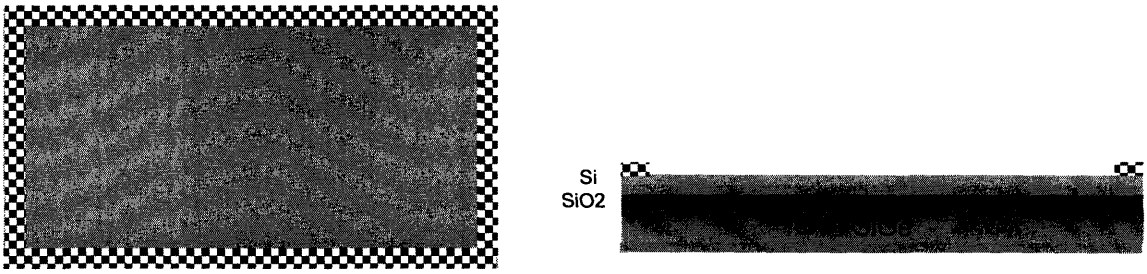
APPENDIX B

AlGaInP LED array Microfabrication Sequence

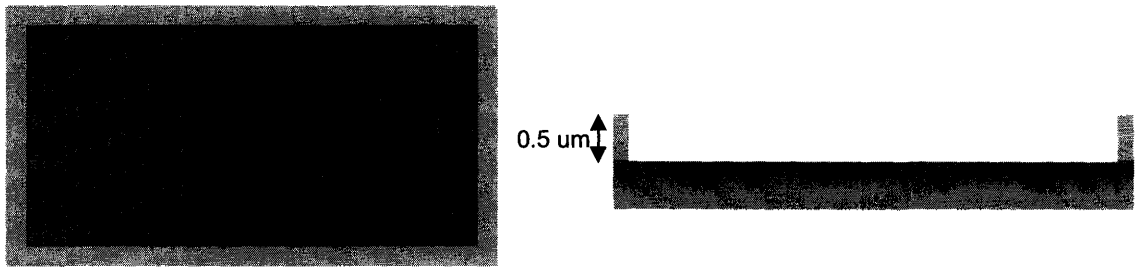
Step Number	Objective	Process	Mask Name	Mask Polarity
1	LED array Area definition	Etch Si and SiO_2 in selected areas to expose underlying Ge	Mask Level I "Active"	Dark Field
2	Isolation Trench	Etch 1 μm deep trench in Ge to isolate the array columns.	Mask Level II "Trench"	Dark Field
3	LED growth well	Deposit 1 μm PECVD oxide and etch LED growth wells to expose Ge	Mask Level III "Well"	Dark Field
4	Poly Strip	Etch Polycrystalline deposits while protecting single crystal material.	Mask Level IV "Poly Strip"	Bright Field
5	Via1	Deposit 0.3 μm PECVD oxide and wet etch	Mask Level V "Via 1"	Dark Field
6	Metal1	Sputter and Pattern 500Å Ti/1 μm Al	Mask Level VI "Metal 1"	Bright Field
7	Via2	Deposit 0.3 μm PECVD oxide and wet etch	Mask Level VII "Via 2"	Dark Field
8	Metal2	Sputter and pattern 1 μm Al	Mask Level VIII "Metal2"	Bright Field



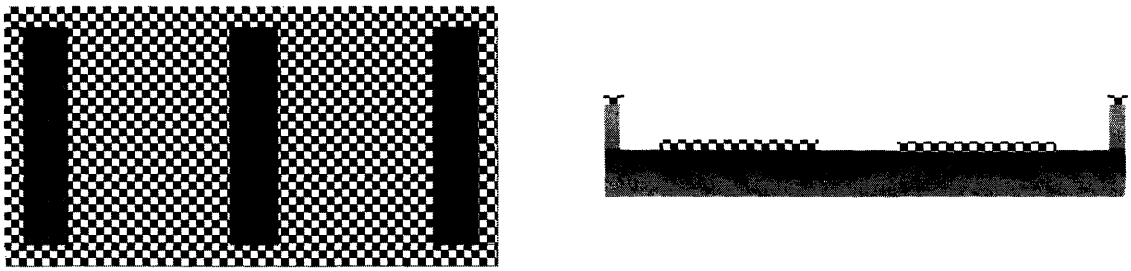
1 .Starting Substrate: Diced SOLES Wafer



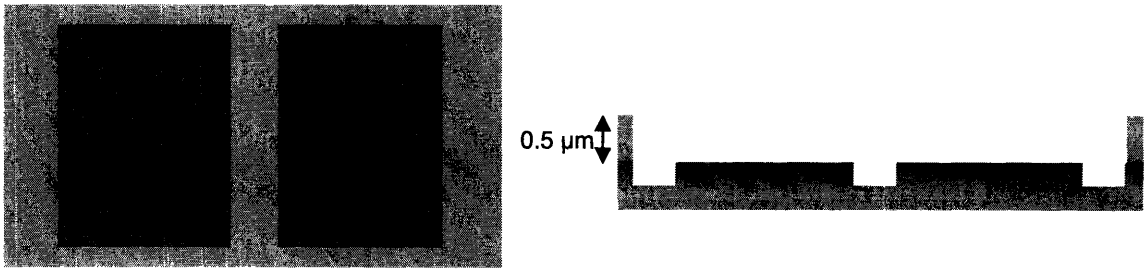
2. Spin-Coat and Pattern Positive Photoresist using Level 1 Dark-Field Mask



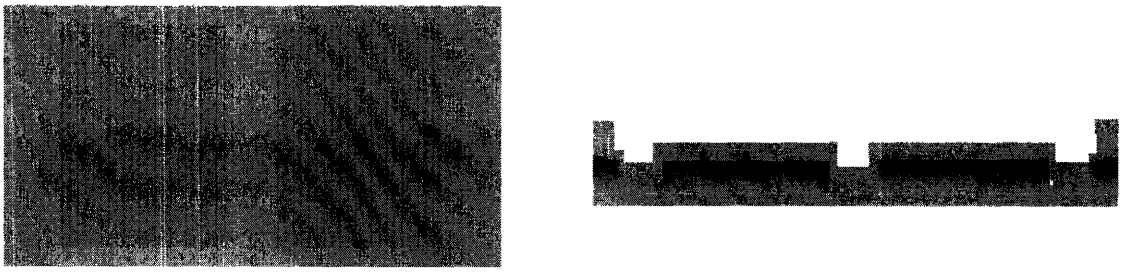
3. Dry etch Si (SF_6/O_2 plasma) and wet chemical etch oxide (using BOE) to expose the underlying Ge, strip photoresist using barrel asher.



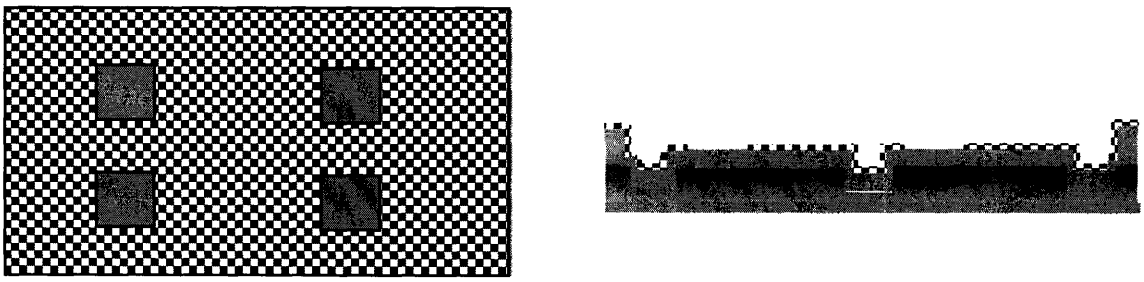
4. Spin-coat and pattern positive photoresist using dark-field Mask "Trench"



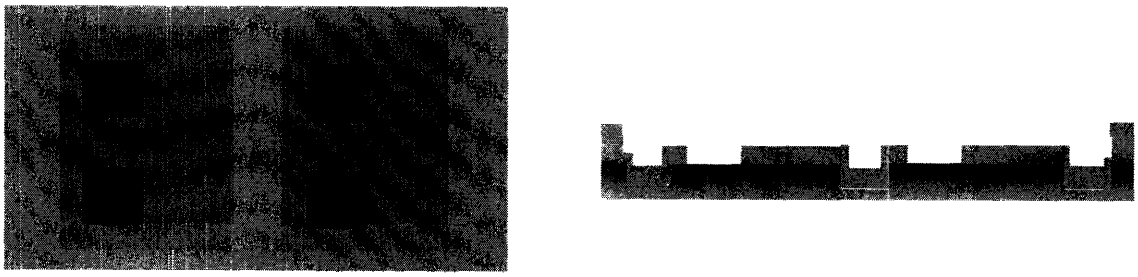
5. Dry etch Ge isolation trench using (SF6/O2) plasma and strip photoresist



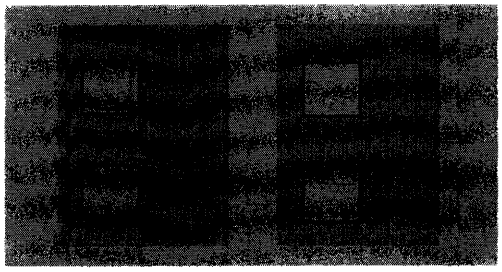
6. Deposit 1.2 µm PECVD Oxide



7. Spin coat and pattern positive photoresist with dark field mask "Ledwell"

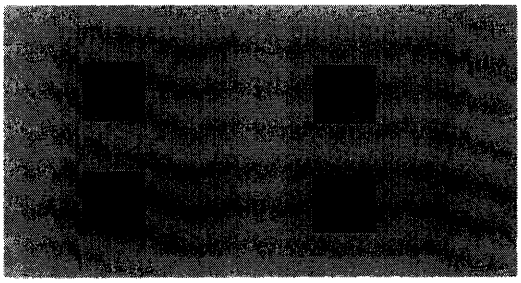


8. BOE wet chemical etch oxide wells and microstrip®/Ash photoresist. This step also strips the LTO oxide on the backside of the wafer.

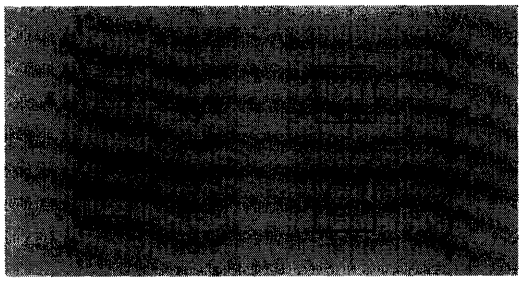


9. Grow 1.1 μm P^{++} Si capped AlGaInP LED stack.

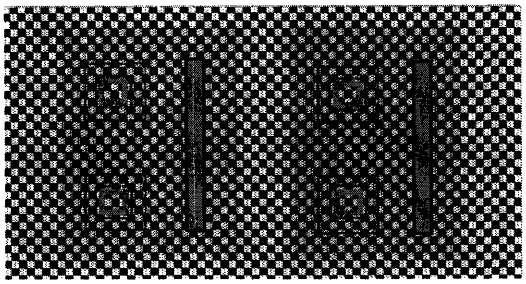
10. Deposit and pattern 0.3 μm SiO_2 hard mask using positive photoresist and bright field mask "PolyStrip"



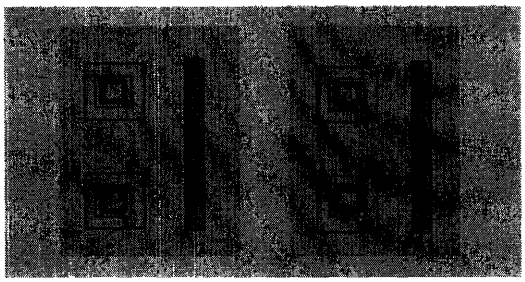
11. Dry etch P^{++}Si cap, wet etch GaAs and AlGaInP LED stack.



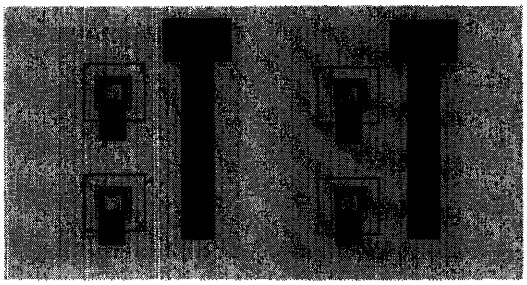
12. Deposit 3000 Å PECVD OXIDE to insulate MESA sidewall.



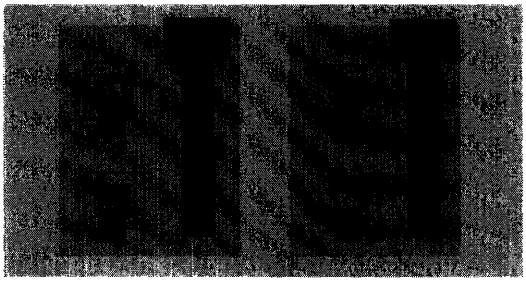
13. Spin coat and pattern positive photoresist with "Via1" dark field mask



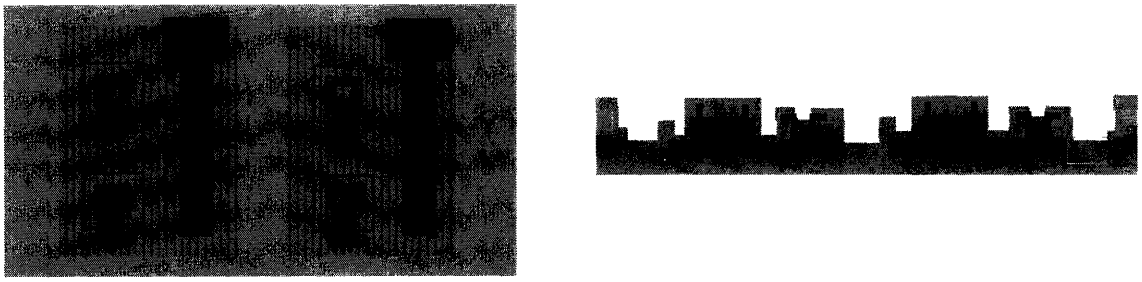
14. BOE wet chemical etch SiO_2 and strip photoresist



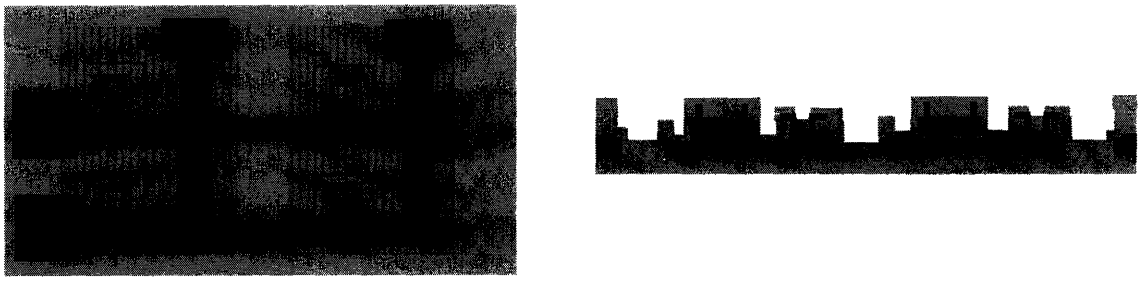
15. Sputter 500 Å Ti and 1 µm Al, Spin-coat and pattern positive resist using bright field mask " Metal 1", Pattern Ti/Al, Strip Resist.
1-D array processing complete at this stage.



16. Deposit 3000 Å PECVD Oxide (Inter Level Dielectric)



17. Spin-coat and pattern photoresist with dark field mask "Via2". Wet etch Oxide via using Silox Vapox III etchant by Transene Chemicals. Strip resist.



18. Sputter 1 um Al. Spin-coat and pattern Photoresist with bright field mask "Metal2". Wet etch Al and Strip resist. Anneal Wafers.

Appendix C

Process Parameters and Recipes

CMP Process Recipe

Parameter	Value
Table rpm	35
Quill rpm	15
P_{down}	5psi
P_{back}	3psi
Slurry 1	150 ml/min

Piranha Clean Recipe

Step	Clean	Time
1	H_2SO_4:H_2O_2 (3:1) blue	10 minutes
2	DI Rinse	5 minutes
3	H_2SO_4:H_2O_2 (3:1) green	10 minutes
4	DI Rinse	5 minutes

RCA Clean Recipe

Step	Clean	Time
1	H_2O:H_2O_2:NH_4OH (5:1:1) 80 °C	10 minutes
2	Dump Rinse 1	5 cycles
3	H_2O: HF (50:1)	15 seconds
4	Dump Rinse 1	5 cycles
5	H_2O:H_2O_2:HCl (6:1:1) 80 °C	15 minutes
6	Dump Rinse 2	5 cycles
7	Spin Dry	

Modified RCA Clean Recipe for Ge

Clean at room temperature

Step	Clean	Time
1	NH_4OH :H_20 1:4 (Tank 1)	15 minutes
2	Dump Rinse 1	5 cycles
3	H_2O_2 (Tank 1)	30 seconds
4	Dump Rinse 1	5 cycles
5	H_2O: HF (50:1)	30 seconds
6	Dump Rinse 1	5 cycles
7	H_2O_2 (Tank 1)	30 seconds
8	Dump Rinse 1	5 cycles
9	HCl: H_20 1:4	30 seconds
10	Dump Rinse 2	5 cycles
11	Spin Rinse Dry	

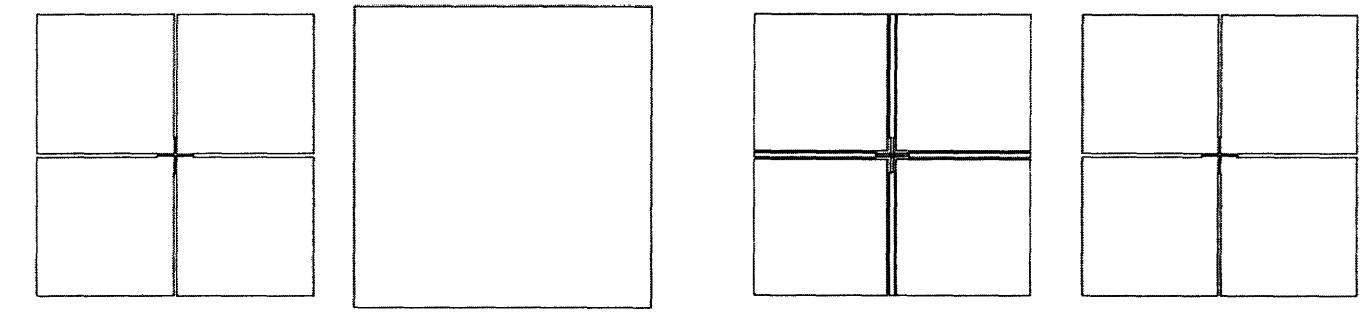
Silicon / Germanium Dry etch recipe

Parameter	Value
SF_6	30 sccm
O_2	5 sccm
Pressure	30 mTorr
Source Power	400W
Bias Power	30W
Mask	Positive photoresist

AlGaInP Dry Etch Recipe

Parameter	Value
CH_4	12sccm
H_2	24sccm
Ar	40sccm
Pressure	15mTorr
Source Power	250W
Bias Power	25W
Mask	SiO_2

APPENDIX D



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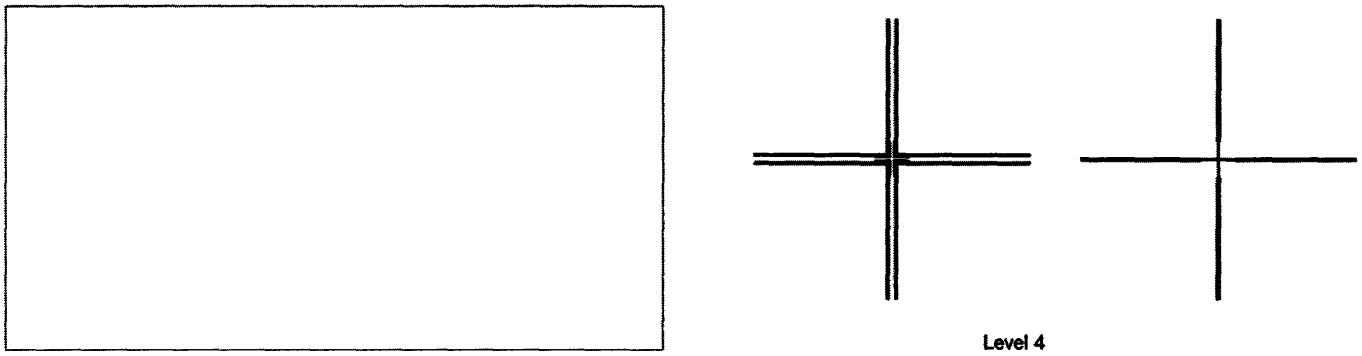
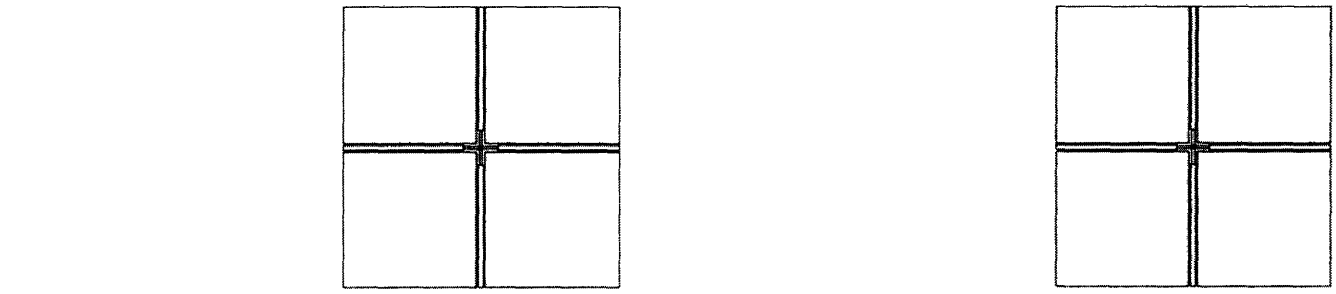
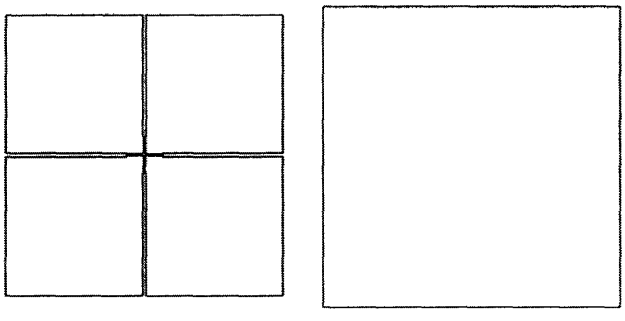


Level 4

Level 1





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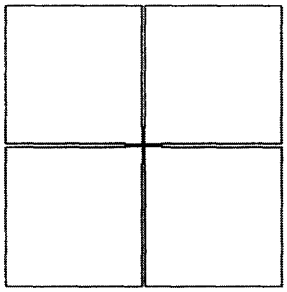
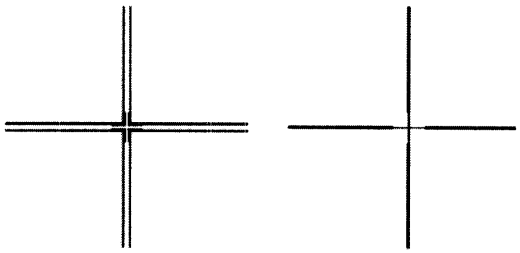
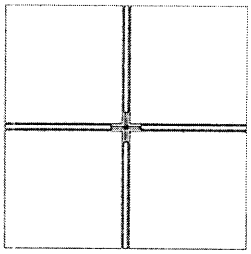


Level 5





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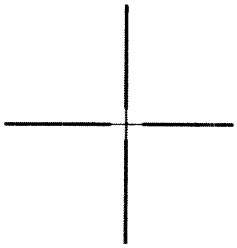

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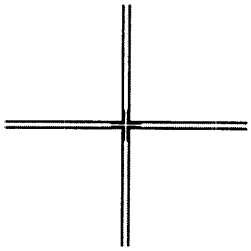

Level 8

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