Fatal Void Size Comparisons in Via-Below and Via-Above Cu Dual-Damascene Interconnects

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Abstract — The median-times-to-failure (t_{50}'s) for straight dual-damascene via-terminated copper interconnect structures, tested under the same conditions, depend on whether the vias connect down to underlaying leads (metal 2, M2, or via-below structures) or connect up to overlaying leads (metal 1, M1, or via-above structures). Experimental results for a variety of line lengths, widths, and numbers of vias show higher t_{50}'s for M2 structures than for analogous M1 structures. It has been shown that despite this asymmetry in lifetimes, the electromigration drift velocity is the same for these two types of structures, suggesting that fatal void volumes are different in these two cases. A numerical simulation tool based on the Korhonen model has been developed and used to simulate the conditions for void growth and correlate fatal void sizes with lifetimes. These simulations suggest that the average fatal void size for M2 structures is more than twice the size of that of M1 structures. This result supports an earlier suggestion that preferential nucleation at the Cu/Si_3N_4 interface in both M1 and M2 structures leads to different fatal void sizes, because larger voids are required to span the line thickness in M2 structures while smaller voids at the base of vias can cause failures in M1 structures. However, it is also found that the fatal void sizes corresponding to the shortest-times-to-failure (STTF's) are similar for M1 and M2, suggesting that the voids that lead to the shortest lifetimes occur at or in the vias in both cases, where a void need only span the via to cause failure. Correlation of lifetimes and critical void volumes provides a useful tool for distinguishing failure mechanisms.

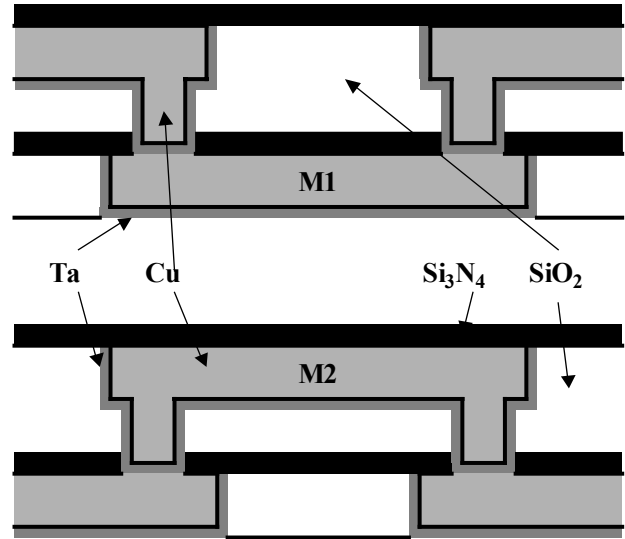*Index Terms*—Copper, interconnect, electromigration, reliability

Figure 1. Schematic diagram of M1 and M2 structures

TABLE I
t_{50}'S AND STTFS

Length (μm)	Type/current density ($\times 10^6$ A/cm^2)	MTTF / STTF (hours)
50	M1 / 2.3	20.8 / 1.38
50	M2 / 3.6	68.7 / 3.13
100	M1 / 2.3	25.2 / 4.53
100	M2 / 3.6	116 / 5.73
100	M1 / 2.5	20.5 / 7.33
100	M2 / 2.5	122.8 / 10.01
800	M1 / 2.3	14.5 / 7.36
800	M2 / 3.6	48.5 / 11.67
800	M1 / 2.5	28.7 / 4.44
800	M2 / 2.5	107 / 3.98

The widths of all lines are 0.28μm; All lines are single via terminated; the thickness of M1 is 0.34μm and of M2 is 0.24μm. All tests were done at T = 350 ºC [4]
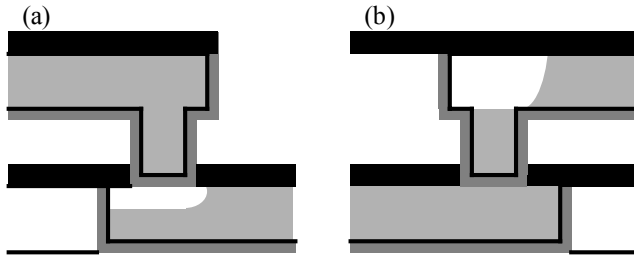
Figure 2. Preferential void nucleation and growth at the Cu/Si₃N₄ interface in (a) M1 and (b) M2 structures.

Figure 2. Preferential void nucleation and growth at the Cu/Si_3N_4 interface in (a) M1 and (b) M2 structures.

(a)

(b)

Figure 3. Normalized R vs t plots showing steady resistance increase region for (a) M1-type structures; (b) M2-type structures

I.   INTRODUCTION

IT is well understood that electromigration, atomic diffusion driven by a momentum transfer from conducting electrons, leads to serious reliability concerns for integrated circuits. The failure mechanisms due to electromigration are well characterized in aluminum (Al) interconnect technology. [1-3] As industry migrates to lower resistance copper (Cu), different failure mechanisms have been discovered, due to different material properties and processes. One of the failure characteristics in Cu interconnects that differs from that of Al is the asymmetry of the median-times-to-failure (t_{50}'s) in M1 and M2 structures, terminating in vias to upper levels (via-above) and vias to lower levels (via-below), respectively. The terminating vias for these two types of dual-damascene copper interconnects, are illustrated in Figure 1. In earlier studies [4], it has been shown that the t_{50} for M2 structures of various lengths, widths, and numbers of vias are higher than those of analogous M1 structures tested under the same current density and temperature conditions (Table I). It has been proposed that the cause of this asymmetry in lifetimes is due to the preferential nucleation of void at the Cu-overlayer (Si_3N_4) interface [4].   The critical tensile stress for the void nucleation at the Cu/ Si_3N_4 interface is reported to be about 40MPa [5].   The stress in an interconnect evolves non-uniformly when it is subjected to continuous electromigration stressing. The critical tensile stress for void nucleation will first be reached at the cathode end of the line [6]. While for M2 structures, the maximum tensile stress is expected to develop at the base of the C-filled via, if the critical stress required for void nucleation at the Cu/S_3N_4 interface is significantly lower than that of the Cu-liner (Ta) interface, a void will nucleate and grow on the Cu/ Si_3N_4. To cause failure, a void that nucleates at the Cu/Si_3N_4 interface in M2 structures must span the width and thickness of the line to cause failure (Figure 2b). Once current must shunt through the thin Ta liner, it is assumed that Joule heating rapidly leads to failure.   In M1 structures, voids that nucleate at the Cu/Si_3N_4 interface need only grow to span the base of the via to cause failure [4,5], because of the Si_3N_4 overlayers do not provide a shunting path for current as TiN anti-reflection coating (ARC) layers did in Al technology [Figure 2a]. In this paper, the critical void sizes at the TTFs of M1 and M2 structures are calculated using a numerical simulation tool.
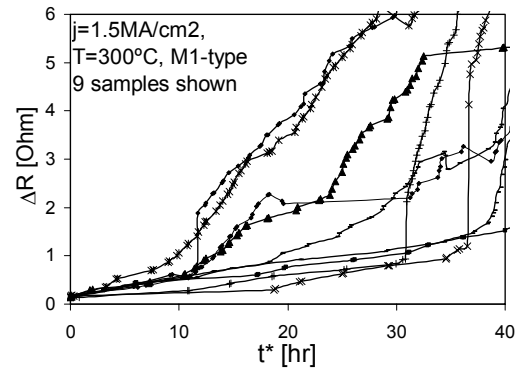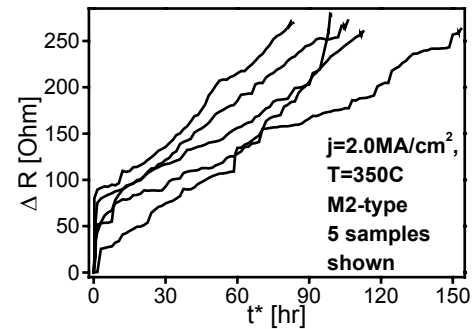
The experimental results reported earlier for failure times for straight Cu dual-damascene lines of type M1 and M2 are listed in Table I [4] The median time to failure (t_{50}) and shortest time to failure (STTF) are listed for each test population. These Cu test structures were fabricated by IME in Singapore and had Ta liners and Si_3N_4 overlayers. The lengths for both M1 and M2 lines are 50μm, 100μm, and 800μm. The thicknesses for M1 and M2 line are 0.36μm and 0.24μm, respectively. The width of all lines is 0.28μm and the cylindrically shaped vias have diameters of 0.26um. For the analysis, only data for lines terminated with a single via was used. The wafers were diced and packaged in ceramic packages. Gold wires were used to connect the bond pads to package lead frames. The structures were stressed in an electromigration test system at various current densities and a temperature of 350°C.

II.   DRIFT VELOCITIES INVIA-ABOVE AND VIA-BELOW STRUCTURES

T (ºC) j (x10^{6}A/cm^2)	M1 250	M1 300	M1 350	M2 350
1.0	5.6±3.0	xxx	88±16	xxx
1.5	6.4±1.8	18.1±3.6	106±41	xxx
2.0	11.8±4.7	26.4±6.4	213±108	300±56*
2.5	18.8±7.1	xxx	191***	250±150**
j-exponent	**1.2±0.3**	**1.3±0.4**	**0.9±0.3**	

j-exponent was obtained from linear fitting of log-log plots of v_d vs j at the same temperatures.

*, ** The M2 structures used at the two different current densities shown here were fabricated by two different organizations, both of which were different from the organization that fabricated the M1 structures.

*** This v_d value was extrapolated using *j*-exponent=0.9, at T=350ºC.

In a separate set of studies [7], we have investigated the electromigration drift velocities as measured in M1 (via-above) and M2 (via-below structures) prior to failure. After voids have nucleated, but before they grow large enough to cause failure, their growth often leads to a steady resistance increase. Characterization of this resistance increase can be related to the rate of void growth, which is also often referred to electromigration drift, in which the rate of drift of the void edge is related to the drift velocity, which can, in turn be related to the effective electromigration induced diffusivity, or more specifically the effective z*D product, where z* and D are the effective charge and diffusivity, respectively, that characterize electromigration.

A. EXPERIMENT

In finding the drift velocity (v_d), constant current experiments were carried out using dual-damascene interconnect structures fabricated by Intel Corp. and International Sematech Corp. in the U.S., and the Institute of Microelectronics in Singapore. Both M1 and M2-type structures were tested. For the M1 structures, the refractory metal diffusion barriers surrounding the Cu interconnect lines at the sides and bottom consisted of a bi-layer of 100Å Ta above 150Å TaN. For the M2 structures, the barriers were a single layer of 250Å-thick Ta. For all structures, Si$_3$N$_4$ overlayers were used as interlayer diffusion barriers. For M1 structures, the structures that were studied had lengths of 70µm, had widths of 0.46µm, and had square vias with side lengths of 0.18µm. For M2 structure, the lengths were 500µm and 1000µm, width were 0.30µm, and the square via had side lengths of 0.25µm.

In these experiments, the failure criterion was a 100% change of the initial resistance, with a tolerance of 0.1% fluctuations. In the M1-type structures, such a change corresponds to about 0.1Ω at 300°C. We used a number of combinations of conditions in testing the M1-type structures, sown in Table II. We tested the M2 structures with *j*= 2.0 and 2.5MA/cm^2 at 350ºC.
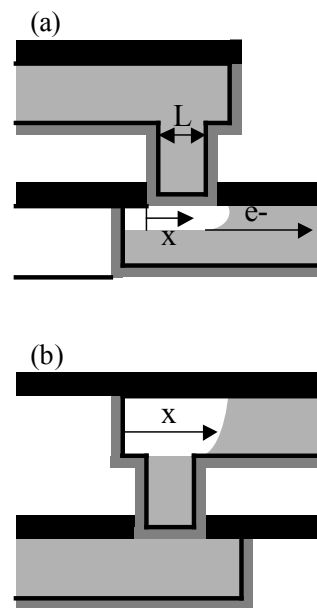

Figure 4. Side view illustrations of void growth in M1 and M2 structures, *x* denotes the position of the void front.

B. RESULTS

For both M1- and M2-type structures, we observed time domains in which the resistance of the structures increased steadily over time. In the M1-type interconnects, the resistance of the metal lines remained constant for a period to be referred to as the incubation period. Following this period, we observed that the resistance gradually increased over a period of time prior to failure. This can be easily shown in a *normalized R* verses *t* plot (Figure 3). The *y*-axis corresponds to the resistance increase, $\Delta R = R - R_0$. For the *x*-axis, *t** designates the difference between the actual test time and the incubation period, t_0. Here, t_0 was measured as the time required for the first non-zero ΔR to occur.

The resistance of M2 interconnect lines also remained constant for a period. Following this period, however, only a fraction of the population of M2 interconnects showed a domain of steady resistance increase. This region ranged over a much longer period of time than in the case of M1 interconnects (Figure 3). For M2 structures, the drift regime was preceded by a 'jump' in resistance ranging from 15 to 70Ω in magnitude.

C. DISCUSSION

In current Cu technology, void nucleation occurs at relatively low stresses, about 40MPa, which translates to a value of *(jL)$_{crit}$*. less than 2100A/cm [5]. The lowest value of the *jL* product in our experiments is 7000A/cm, which is much larger than *(jL)$_{crit}$*. This suggests that voids are likely to form inside all of the tested structures. Therefore, we postulate that the observed steady resistance increase observed is due to void growth in the interconnects. The simple models to be discussed below have been used to correlate the rate of resistance increase to the rate of void

growth, i.e., the drift velocity for electromigration. As discussed in section I, M1 and M2 interconnects are thought to have different void nucleation and growth processes [4, 5]. In both cases, the critical stress for void nucleation is lowest at the Cu/Si$_3$N$_4$ interface, which also provides the fastest diffusion path. Consequently, failures in M1-type structures are due to small-volume voids that form directly below the cathode-end via and only partially span the line. This suggests that the resistance increase observed in the M1 experiments was due to the decrease in contact area between the via and the Cu line below it, as a result of growth of the void below it. If we assume that at $t^*=0$, the void front uniformly propagates below the cathode end via (Figure 4(a)), and define the distance of the void front from the edge of the via to be x, it follows that the contact area between the via and the line is $A=L(L-x)$. Therefore, we can correlate $v_d=dx/dt$ to the rate of resistance increase using

$$v_d = \frac{dx}{dt} = \frac{(\frac{dR}{dt}) \cdot L}{R_{via,0}}, \qquad (1)$$

where $R_{via,0}$ is the via resistance at T_{test}.

In order for failures to occur in M2 interconnects, partially-spanning voids that nucleate at the Cu/Si$_3$N$_4$ interface must grow to span the entire cross section of the line (Figure 4(b)). This forces the electron flow to be carried by the thin Ta diffusion barrier. If the barrier is unable to sustain the high current density, failure occurs. However, if the liner is able to act as a shunt layer and carry the electron flow, the fully-spanning void would continuously grow along the line, exposing a longer and longer section of the high-resistivity refractory liner in the M2 line. Therefore, we can correlate the rate of resistance increase to the rate of void growth in M2 lines using

$$v_d = \frac{dR}{dt}\left[\frac{W_{Ta}h_{Ta}}{\rho_{Ta}}\right], \qquad (2)$$

where W_{Ta} is the width of the Ta liner, which is equal to the width of the Cu line plus the twice the thickness of Ta liner; h_{Ta} refers to the thickness of the Ta liner. Table II summarizes the v_d values obtained by correlating the rates of the gradual resistance increase in M1 and M2 interconnects. From these measurements, we calculated an activation energy for electromigration of 0.80±0.06eV. This value is not only in good agreement with that extracted from the lifetime data for the same structures, but also with the activation energies reported by Hu *et al.* and Liniger *et al.* [8, 9] (E_a=0.7 to 0.9eV). The *j*-exponent obtained from the v_d measurements confirms that v_d is linearly proportional to the current density, which is in agreement with the Nearnst-Einstein relationship. Lastly, the values of v_d obtained using the M1 interconnects are in agreement with the value measured using the M2 interconnects, even among the samples fabricated by different organizations. Therefore, the median lifetimes are significantly different in M1 and M2 structures, the drift
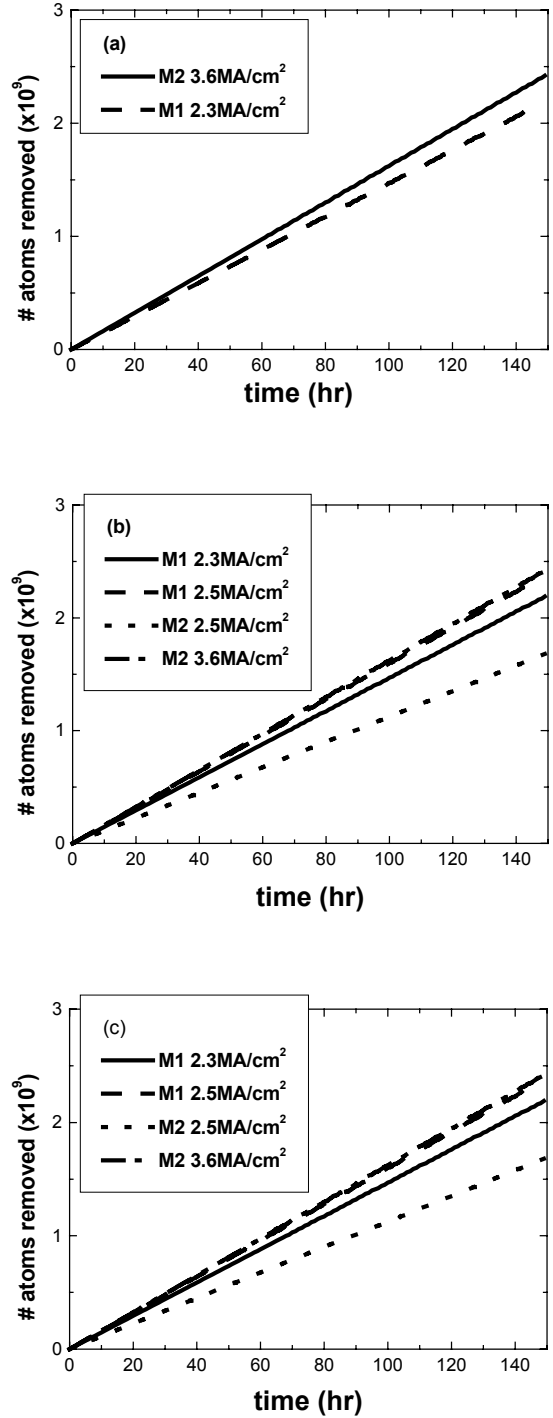

Figure 5. The number of atoms removed from a void nucleation site vs. time in (a) 50μm, (b) 100μm, and (c) 800μm lines, as determined through simulations.

velocity is not. This supports the postulate the difference in lifetimes is associated with differences in the fatal void volumes, and further indicates that electromigration in

these two types can be modeled using the same effective z*D product.

III. NUMERICAL SIMULATION

Korhonen *et al.* have proposed an equation describing the electromigration-evolution of stress in a one dimensional conductor [10],

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left[\frac{D_{eff}B}{kT}\left(\Omega\frac{\partial \sigma}{\partial x} + Z_{eff}^{*}e\rho j\right)\right], \quad (3)$$

where σ is the stress, x is the position along the line length, D_{eff} is the effective diffusivity, Ω is the atomic volume, B is an effective modulus, which depends on the conducting material as well as the material surrounding the conducting material, k is Boltzmann's constant, T is the temperature, Z_{eff}^{*} is the effective charge number, e is the fundamental electron charge, ρ is the electrical resistivity of the conducting material, and j is the current density. D_{eff} is expressed as [11]

$$D_{eff} = D_{o}\exp\left(-\frac{\Delta H}{kT}\right)\exp\left[\left(\frac{\Omega}{kT}+\frac{1}{B}\right)\sigma\right], \quad (4)$$

where ΔH is the activation energy for diffusion and D_{o} is the temperature independent constant. Because D_{eff} depends on stress, Eq. (3) is non-linear. Therefore, rather than analytically solving Eq. (3), we have developed a simulation tool to predict the time evolution of stress as well as the atomic concentration.

The atomic concentration as a function of space and time is obtained by solving the continuity equation

$$\frac{\partial C}{\partial t} + \frac{\partial J}{\partial x} = 0, \quad (5)$$

where C is the atomic concentration and J is the flux of atoms. The flux of atoms by electromigration and the stress gradient is expressed as [12]

$$J = \frac{D_{eff}C}{kT}\left(\Omega\frac{\partial \sigma}{\partial x} + Z_{eff}^{*}e\rho j\right). \quad (6)$$

For the simulation, the Cu interconnect structure is discretized into a given number of cells where the length of each cell is Δx as shown in Figure 3. Stress is related to the vacancy concentration and also the concentration of lattice sites by [11]

$$C_{v} = C_{vo}\exp\left(\frac{\Omega\sigma}{kT}\right) \quad (7)$$

and

$$C_{l} = C_{lo}\exp\left(-\frac{\sigma}{B}\right), \quad (8)$$

respectively, and C_{lo} and C_{vo} are stress independent constants. In addition, the atomic concentration is given by

$$C = C_{l} - C_{v}. \quad (9)$$

Thus, the stress of each cell can be calculated with the relationship between the stress and the atomic concentration given as

TABLE III
NUMBER OF REMOVED ATOMS AND VOID VOLUMES

Length (μm)	Type/current density (x10^6 A/cm²)	# atoms removed (x10⁸) / void volume (μm³) (t₅₀)	# atoms removed (x10⁸) / void volume (μm³) (STTF)
50	M1 / 2.3	3.05 / 0.0052	0.20 / 0.0003
50	M2 / 3.6	11.1 / 0.0190	0.51 / 0.0009
100	M1 / 2.3	3.69 / 0.0063	0.67 / 0.0011
100	M2 / 3.6	11.9 / 0.0203	0.93 / 0.0016
100	M1 / 2.5	3.27 / 0.0056	1.17 / 0.0020
100	M2 / 2.5	11.4 / 0.0195	1.13 / 0.0019
800	M1 / 2.3	2.13 / 0.0036	1.08 / 0.0018
800	M2 / 3.6	5.47 / 0.0094	1.90 / 0.0032
800	M1 / 2.5	4.58 / 0.0078	0.71 / 0.0012
800	M2 / 2.5	12.1 / 0.0207	0.45 / 0.0007

$$C = C_{lo}\exp\left(-\frac{\sigma}{B}\right) - C_{vo}\exp\left(\frac{\Omega\sigma}{kT}\right). \quad (10)$$

The atomic fluxes are calculated along the line with the approximation dx = Δx. The simulation utilizes the Backward Euler finite-discretization method, which calculates the maximum increment of dt within the stability limit and solves for a change in atomic concentration after time dt. With the simulated concentration and the dimension of the interconnect structure, the number of atoms in each cell is calculated. If the critical tensile stress for the nucleation of a void is reached at any position in the line, a void is assumed to nucleate and the stress is assumed to relax to zero at the site of the void. Assuming each atom has the atomic volume $\Omega = 1.18 \times 10^{-29}$m³, the size of the void is estimated as the total volume of the atoms removed from the void nucleation site. D_{eff} was calculated to be 2.99×10^{-16} m²/s for M1 structure and 4.23×10^{-16} m²/s for M2 structure at T = 350°C and σ=0, which is the diffusivity at the Cu/Si₃N₄ interface, the dominant diffusion path for Cu interconnects [13]. The following values were used for the simulation: σ_{crit} = 40MPa [5]; Z_{eff}^{*} = 1 [8]; B = 28GPa; $\Omega = 1.18 \times 10^{-29}$ m³; $\rho = 4.1 \times 10^{-8}$ Ω-m; ΔH = 0.8eV.

IV. ANALYSIS AND DISCUSSION

The number of atoms removed from the void nucleation site for each structure was simulated as shown in Figure 5. The numbers of atoms removed at t₅₀ and at the shortest-times-to-failure (STTFs) of each structure have been determined and are shown in Table III. The critical void volumes for failure were calculated at each t₅₀ and the STTF and are also shown in Table III. From the calculated critical void sizes, it is clear that the M2 structures require larger void sizes for failure than the M1 structures. This supports the earlier conclusion that the reason for the difference in void sizes is due to preferential void nucleation at the Cu/ Si₃N₄ interface which cause the void size required for failure in M2 to be larger than that of M1, as shown in Figure 2. The void in M2 must fully span in
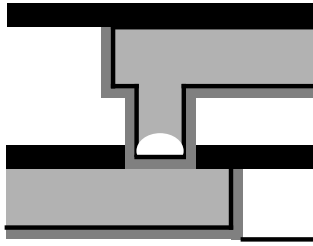
Figure 6. Void nucleation and growth at via an M2 via. Nucleation in the via can result in an early time of failure.

the line in order to cause an open circuit failure, where as only partially spanning voids directly below the via can cause failure in M1 structures. It is important to note that the thickness of M2 is smaller than that of M1. If the thickness of M2 is increased to that of M1, the t_{50} of M2 should also increase. This will result in an even larger difference in fatal void sizes. When comparing the critical void sizes at the STTF, however, it can be seen that failure of M2 structures does not *necessarily* require a larger void than for failure of M1 structures. We predict that the reason for the similarity in critical void sizes for failure at the STTF is due to the void forming near in the via in M2 structures and at the base of the vias in M1 structures. If the void forms right in the via in M2 structures, even a small void size can lead to a fatal failure, as shown in Figure 6. Also, in the case of M1, as shown in Figure 2, if a void nucleates at the end of the line it must grow first to the via, and then across it to cause failure. If the void nucleates "downwind" of the via, it must grow to span the line width and thickness, as in the case of M2 structures, the void can grow towards the via and cover the bottom of the via to cause an open circuit failure at relatively small volume. Fatal void volumes depend critically on the site for void nucleation, so that critical void volumes and lifetimes can vary over broad ranges for both M1 and M2 structures. While the Cu/Si3N4 interface is the most probable site for void nucleation in M2 structures, it is possible to have a defect inside the via, such as a pre-existing void present before the test, that can lead to void growth and the resulting line failure.

V. CONCLUSIONS

We have developed a simulation tool for electromigration modeling. The tool was utilized to simulate the number of atoms removed from the site of void nucleation. The number of atoms removed was used to estimate the fatal void size. The simulation results corresponding to observed t_{50}'s of straight M1 and M2 lines confirm that the average void sizes required for failure in M2 structures is larger than for M1 structures. This is due to the preferential nucleation of voids at the Cu/Si_3N_4 interface. On the other hand, the simulation results for STTFs show that the fatal void sizes for M1 and

M2 do not show asymmetric behavior. The similarity in void sizes suggests that the minimum fatal void sizes correspond to nucleation in the via in M2 structures, and at the base of the voids in M1 structures. The simulation suggests that while in most cases M2 structures are more reliable than M1 structures, the minimum lifetimes for the two structures might generally be similar if a few flaws exist in the vias. These results show that the variations in the location of void nucleation lead to large variations in the lifetimes of Cu-based interconnects, not only from line-to-line, but from structure-to-structure. These variations are larger than in the case of Al, and complicate the task of accurate reliability projections for large populations of interconnects. These results also demonstrate the usefulness of simulations, in combination with experimental data, in differentiating complex variations in failure mechanisms.

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