ELECTRON TRANSPORT IN ULTRATHIN-BODY FULLY DEPLETED N-MOSFETS FABRICATED ON STRAINED SILICON DIRECTLY ON INSULATOR WITH BODY THICKNESS RANGING FROM 2NM TO 25NM

by
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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering at the Massachusetts Institute of Technology 2006

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Submitted to the Department of Electrical Engineering and Computer Science on June 10, 2006 in partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering.

Abstract

The electron effective mobility in ultrathin-body (UTB) n-MOSFETs fabricated on Ge-free 30% strained-Si directly on insulator (SSDOI) is mapped as the body thickness is scaled. Effective mobility and device body thickness were extracted using current-voltage and gate-to-channel capacitance-voltage measurements as well as cross section transmission electron microscopy. Devices with body thicknesses ranging from 2 nm to 25 nm are studied. Significant electron mobility enhancements (~1.8x) are observed in SSOI compared to unstrained SOI for body thicknesses above 3.5 nm. The mobility exhibits a sharp drop as the body thickness is scaled below 3.5 nm.

Thesis Supervisor: Judy L. Hoyt
Title: Professor of Electrical Engineering and Computer Science
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**INTRODUCTION**

Ultrathin-body strained silicon directly on insulator (SSDOI) is a promising substrate for deeply scaled MOSFETs. SSDOI provides enhanced electron and hole transport as well as the superior electrostatic control that unstrained silicon on insulator (SOI) exhibits in ultrathin-body (UTB) MOSFETs [1,2,3]. The electron mobility dependence on body thickness has been theoretically and experimentally reported for MOSFETs fabricated on unstrained SOI [4,5]. Electron mobility in SSDOI has been well documented for thick substrates, but has not been mapped in detail as the body thickness is reduced. In this work the electron mobility is mapped as the body thickness is scaled for UTB n-MOSFETs fabricated on 30% SSDOI [1,2,6]. Determining the lower thickness limit upon which SSDOI provides a substantial mobility enhancement over unstrained SOI is of interest as device body thickness is reduced to mitigate short channel effects that arise from gate length scaling. As gate lengths are scaled to dimensions below 45 nm the body thickness in UTB MOSFETs must be scaled correspondingly, to dimensions on the order of 10 nm or less [7]. In this work a device fabricated in SSDOI with a body thickness of 3.6 nm is shown to exhibit a significant mobility enhancement (~1.8x) over 15 nm unstrained SOI. Subthreshold characteristics for UTB MOSFET fabricated in this work are also observed to be comparable in both SOI and 30% SSDOI, < 70 mV/dec. The results presented are promising for the use of SSDOI in future technology nodes.
CHAPTER 1

BIAXIAL STRAIN IN SI

In this chapter, background information on biaxial strain in Silicon (Si) is introduced. The changes induced in the band structure by applied biaxial strain will be discussed. The impact of these changes in the conduction and valence bands on mobility enhancement will be explained. Mobility results from the literature for holes and electrons in bulk strained Si and strained Si directly on insulator (SSDOI) will then be reviewed. Subthreshold characteristics for SSDOI n-MOSFETs measured in previously reported work will also be presented.

1.1 Biaxially Strained Si

Small changes in the lattice constant of Si can result in significant changes to its electrical properties. Silicon has a lattice constant of 5.432Å. The lattice constant of Germanium is 4.1% larger. Vegard’s law provides a linear interpolation for the lattice constant of Silicon Germanium alloys [8], \( a(x) \), given by:

\[
a(x) = x \cdot a_{Ge} + (1 - x) a_{Si}
\]

Equation 1.1

where \( x \), \( a_{Ge} \), and \( a_{Si} \) are the Ge fraction in the silicon germanium, the lattice constant of Si, and the lattice constant of Ge respectively. Psuedomorphic growth of Si on a \( Si_{1-x}Ge_x \) alloy causes the in-plane Si lattice to stretch and take on the lattice constant of the underlying \( Si_{1-x}Ge_x \). By increasing the Ge fraction in the \( Si_{1-x}Ge_x \) more strain can be introduced into the Si. It should be noted that the level of strain in Si is usually indicated by the atomic fraction of Ge in the underlying relaxed \( Si_{1-x}Ge_x \) substrate, assuming fully pseudomorphic growth of the strained Si. For Si growth on relaxed \( Si_{0.7}Ge_{0.3} \) the Si is often referred to as being strained to a 30% SiGe substrate. A basic depiction of the Si, Ge,
and Si$_{1-x}$Ge$_x$ lattice is shown in Fig. 1.1 as well as the means by which tensile strain is introduced into the Si. Compressive strain can be introduced into Si$_{1-x}$Ge$_y$ similarly by pseudomorphically growing it on unstrained Si or on relaxed Si$_{1-x}$Ge$_x$ where $y > x$. The equilibrium lattice constant of Si$_{1-x}$Ge$_y$ is greater than that of Si or Si$_{1-x}$Ge$_x$ and thus it experiences biaxial compression to conform to the smaller lattice constant of the underlying material.

The mobility characteristics and strain-induced changes in the band structure of strained Si and strained Si$_{1-x}$Ge$_x$ have been well documented [9,10,11,12,13,14,15,16,17,18]. In subsequent sections, historical mobility results and a brief explanation of the strain-induced modulations in the band structure of Si is presented.

![Figure 1.1](image-url)

**Figure 1.1** (a) A basic two-dimensional depiction of the Si, relaxed Si$_{1-x}$Ge$_x$, and Ge lattice indicates the relation in lattice size between the three. The equilibrium lattice constant of Si$_{1-x}$Ge$_x$ varies depending upon the Ge fraction in the alloy. The introduction of tensile strain in Si by pseudomorphic growth onto relaxed Si$_{1-x}$Ge$_x$ is illustrated in (b).
1.1.1 Strained Si Substrates

Strained Si substrates are available in several different varieties, the first of which is a bulk substrate where Si is pseudomorphically grown on an epitaxial relaxed Si$_{1-x}$Ge$_x$ layer on a Si wafer. Another strained-Si substrate is strained Si directly on insulator (SSDOI). This substrate consists of a strained-Si film on a buried oxide. Although SSDOI is completely free of Ge, the notation “x % SSDOI” is used to indicate the Ge atomic percentage in the relaxed SiGe donor substrate, used to originally strain the Si. This designation will be used throughout this thesis. There are a variety of methods that can be used to form this material [19,20,21,22], but the method utilized in this work is referred to as the bond and etch-back approach [23]. Substrate fabrication utilizing this approach will be discussed in greater detail in chapter 3. Fig. 1.2 depicts these two strained Si substrates.

**Figure 1.2** Schematic illustration of (a) bulk substrates where Si is pseudomorphically grown on relaxed Si$_{1-x}$Ge$_x$ and (b) strained Si directly on insulator (SSDOI).

1.2 Hole Mobility in Strained Si

The band offset that exists between Si and Si$_{1-x}$Ge$_x$ in the valence band results in holes preferentially occupy the Si$_{1-x}$Ge$_x$ buried layer at low vertical effective fields. This complicates the study of hole transport in bulk strained Si substrates at low vertical fields, though the issue has been mitigated for strained Si on Si$_{0.8}$Ge$_{0.2}$, by grading-out the band discontinuity [24]. SSDOI has no underlying SiGe, and therefore holes can only reside in the strained Si. In this section hole mobility results in SSDOI from the literature are reviewed.
The valence band of Si consists of Heavy Hole (HH), Light Hole (LH), and Split-Off (SO) bands. The light hole and heavy hole bands are degenerate at \( k=0 \). In strained Si the LH and HH band degeneracy is lifted and the bands are warped. For Si strained to relaxed SiGe (30% Ge) the LH band is the lowest energy band and is separated from the HH band by 128 meV [25]. Lifting the band degeneracy reduces phonon scattering and warping the bands causes a reduction in effective mass. These two modulations in the valence band result in a larger hole mobility. The hole mobility enhancement is reduced at high vertical fields because the separation between the LH and HH bands is reduced, resulting in increased phonon scattering. Hole mobility characteristics measured by Åberg [2] in 30% and 40% SSDOI as well as unstrained SOI are presented in Fig. 1.3 as a function of vertical effective electric field (\( E_{\text{eff}} \)). The effective field is given by:

\[
E_{\text{eff}} = \frac{1}{\varepsilon_{\text{Si}}} \left( Q_B + \eta Q_{\text{inv}} \right) \tag{1.2}
\]

where \( \varepsilon_{\text{Si}} \), \( Q_B \), and \( Q_{\text{inv}} \) are the permittivity of Si, the charge layer density in the depletion region, and charge layer density in the inversion layer respectively [26]. The fitting parameter \( \eta \) is taken to be 1/3 for holes and 1/2 for electrons.
Figure 1.3 Hole effective mobility in moderately thick (~15 nm) 40% and 30% SSDOI, SOI, and the universal mobility in Si. A mobility enhancement can be seen for low effective fields, but as the field strength is increased the enhancement is reduced. From Åberg [2].

1.3 Electron Mobility in Strained Si

Si has six ellipsoidal valleys with the minimum centered approximately (in units of the reciprocal lattice constant) at the (1,0,0) point of the Brillouin zone, called the $X$-point. Fig. 1.4 illustrates the constant-energy surfaces associated with these ellipsoids. The $\Delta_2$-valley ellipsoids lie on the axis perpendicular to transport in a planar MOSFET and the $\Delta_4$-valleys ellipsoids lie along the two axes parallel to transport. In a MOSFET where quantization is induced by the vertical electric field, two sets of subbands exist in the conduction band corresponding to the $\Delta_2$ and $\Delta_4$-valleys. To better understand the subband structure corresponding to these valleys the well-known quantum structure of the infinite square potential well can be used. In a square potential well the subband energy of the nth subband is given by:

$$E_n = \frac{\hbar^2 \pi^2}{2m_s W^2} n^2$$

Equation 1.3
where m\textsubscript{z} is the effective mass of the particle in the well, quantized in the z direction, and W is the width of the potential well. Subbands with a larger effective mass will have a lower energy and thus be populated first. In the conduction band of unstrained Si the effective mass perpendicular to the growth plane is larger in the \Delta_2-valleys, and therefore this subband energy is lower than that of the \Delta_4-valleys. With applied strain the symmetry between the \Delta_2-valleys and the \Delta_4-valleys is broken and these subbands are separated in energy even further. The strain induced splitting increases by \textasciitilde 67 meV for every 10\% of Ge in the relaxed Si\textsubscript{1-x}Ge\textsubscript{x} substrate [15,16]. Fig. 1.5 provides a depiction of the \Delta_2- and \Delta_4-valley subbands before and after biaxial tensile strain is applied. As the subbands are separated in energy, inter-valley phonon scattering is suppressed, as discussed in more detail in Chapter 5. When the valley degeneracy is lifted carriers preferentially occupy the lower energy \Delta_2-valley subbands. In the direction of transport these valleys have a lower effective mass compared to the \Delta_4-valley subbands. Effective mobility is given by:

\[
\mu = \frac{q\tau}{m^*}
\]

Equation 1.4

where m^* is the effective mass and \( \tau \) is the time between scattering events. As is evident from equation 1.3 both the reduced mass and increase in time between scattering events is expected to result in a larger electron mobility in biaxial tensile strained Si.
**Figure 1.4** Constant energy diagram of the 6 degenerate ellipsoidal $\Delta$-valleys in the Si conduction band. Strain breaks the degeneracy of these valleys, resulting in a mobility enhancement.

**Figure 1.5** The subband structure in strained and unstrained Si. In unstrained Si $\Delta E_0$ is the energy difference between the first energy level in the $\Delta_2$ and $\Delta_4$ subband ladders. With applied biaxial tensile strain the energy separation between the subband ladders increases. The energy separation with applied strain increases 67 meV for every 10% of Ge in the relaxed Si$_{1-x}$Ge$_x$ substrate. After Takagi, et al. [27].

### 1.3.1 Electron Mobility in Bulk Strained Si MOSFETs

Electron transport in strained Si was initially investigated on bulk substrates. Fig. 1.6 presents effective mobility data for devices fabricated on bulk substrates where a mobility enhancement of 1.8x over unstrained Si is observed [28]. The maximum electron mobility enhancement in strained Si is observed when the Ge fraction in the underlying relaxed Si$_{1-x}$Ge$_x$ is ~20% or higher [29]. At ~20% the strain-induced band splitting is enough to significantly reduce inter-valley scattering relative to other scattering mechanisms. Since the mobility at this point is limited by other scattering mechanisms which do not depend upon the valley splitting, the mobility enhancement reaches a plateau. Fig. 1.7 illustrates calculated and measured mobility enhancement factor with increasing Ge fraction in the Si$_{1-x}$Ge$_x$ substrate [29].
Figure 1.6 Electron mobility in bulk strained Si substrates on a 28% relaxed SiGe virtual substrate compared to the universal mobility. A 1.8x mobility enhancement is observed, compared to unstrained Si. Enhancement can be seen at low and high vertical fields. From Rim, et al. [28].

Figure 1.7 Mobility enhancement in strained Si as a function of Ge fraction in the virtual substrate. A plateau is seen above 20% Ge, where strain induced band splitting does nothing to further mitigate the inter-valley scattering that limits the mobility in unstrained Si. After Hoyt, et al. [29].
1.3.2 Electron Mobility in SSDOI MOSFETs

Aggressive scaling of the gate length in planar MOSFETs results in a reduction in electrostatic control of the channel. Ultrathin-body SOI and device architectures such as planar double gate MOSFETs and FinFETs are effective means to improve electrostatic control of the channel [30,31,32]. Strained-Si directly on insulator (SSDOI) provides the electrostatic benefits of a material like SOI and also exhibits enhanced electron and hole transport characteristics. Subthreshold characteristics are nearly ideal in long-channel MOSFETs fabricated on SSDOI. Fig. 1.8 illustrates measured subthreshold characteristics from Aberg [25] where the sub-threshold swing (SS) is observed to be 64 mV/dec for an n-MOSFET fabricated on 25% SSDOI. The improvement in electrostatic control over bulk substrates and enhancement in carrier transport indicates that SSDOI holds promise for deeply scaled MOSFETs [1,33,34]. Fig. 1.9 illustrates measured electron mobility results for both 25% and 30% SSDOI [2]. The effective mobility in SSDOI is observed to be ~1.8x higher than observed for SOI at both low and high vertical fields. The mobility results provided in Fig 1.8 are for moderately thick (~15 nm) SSDOI. Although Lauer measured the electron mobility in a device fabricated in 2 nm-thick SSDOI [6], a detailed study to map the electron mobility as a function of body thickness has not been conducted. The aim of this work is to map the mobility as the body thickness is scaled for UTB n-MOSFETs fabricated on 30% SSDOI.
Figure 1.8 Subthreshold characteristics in long-channel UTB n-MOSFETs fabricated on SSDOI. The SS measured is 64 mV/dec. This is close to the ideal value of 59.6 mV/dec. The improved electrostatic control over bulk devices is attributed to the fully-depleted nature of the substrate. IV characteristics are provided for drain/source biases of 50 mV and 1 V. From Aberg, [25]

Figure 1.9 Electron effective mobility in 30% and 25% SSDOI, SOI, and the universal mobility in Si. A mobility enhancement (≈1.8x) can be seen for all effective fields. The SSDOI thickness is ~15 nm. From Aberg, et al. [2].
1.4 Chapter Summary

In this chapter the origin of the electron and hole mobility enhancement in strained Si was explained. The corresponding changes in the conduction and valence bands induced by strain were described. Strain is introduced in Si by pseudomorphic growth on Si$_{1-x}$Ge$_x$. Mobility enhancement in strained Si for electron and holes stems from the strained induced modulations in the conduction and valence bands. In the valence band of strained Si the LH and HH band degeneracy is lifted and the bands are warped. These two modulations result in a larger effective hole mobility at low fields. This enhancement is reduced in p-MOSFETs at high vertical effective fields. In the conduction band the applied strain breaks the symmetry between the $\Delta_2$-valleys and the $\Delta_4$-valleys. As the subbands are separated in energy intervalley scattering is reduced resulting in a higher mobility. The structures of bulk strained-Si and SSDOI substrates were also described. Mobility results for these substrates were presented. The hole effective mobility is enhanced over unstrained SOI at low effective field, but the enhancement is reduced at high field strengths. The enhancement is increased in 40% SSDOI compared to 30% SSDOI. An electron mobility enhancement of $\sim$1.8x is observed in both substrates at both low and high vertical effective fields. Near ideal subthreshold characteristics have been reported for n-MOSFETs fabricated on SSDOI.
CHAPTER 2

SUBSTRATE FABRICATION

This chapter describes the substrate fabrication process utilized in this work to create 30% SSDOI. The structures utilized to fabricate these substrates were epitaxially grown in an Applied Materials “Epi Centura” system. The substrates were fabricated in MIT’s Microsystems Technology Laboratory using a bond and etch-back technique. The epitaxially grown etch-back structure is initially described. Details of the wafer bond process are then presented. The substrate etch-back process is then explained in detail.

2.1 Epitaxial Growth of Etch-Back Structure

The method by which SSDOI was fabricated in this work is known as the bond and etch-back process [23,35]. This process begins with the epitaxial growth of an etch-back structure in an Applied Materials Epi Centura LPCVD reactor. Before growth wafers are clean with a pre-epi cleaning sequence consisting of: 10 minutes in 5:1:1 DI:NH₄OH:H₂O₂ (80°C), 15 seconds in 50:1 HF:DI, 15 minutes in 6:1:1 DI:HCl:H₂O₂ (80°C), 15 seconds in 50:1 HF:DI, and a spin-rinse dry (SRD) cycle.

The epitaxial structure consists of a SiGe graded layer grown at 900°C, ramping from SiₓGe₀.₀ to Si₀.₇Ge₀.₃ over at thickness of roughly 3 μm. The high growth temperature and graded layer is utilized to reduce the density of threading dislocations in the substrate [36,37,38]. The grade is then capped with a Si₀.₇Ge₀.₃ layer, referred to as a relaxed buffer, of uniform composition matching the maximum composition in the grade. The relaxed buffer sets the level of strain that is present in the Si device layer and reduces the number of dislocations that reach the surface [39]. A strained Si etch-stop layer is subsequently grown on the relaxed buffer. This layer is utilized to controllably approach the strained Si device layer during the etch-back process. Another etch-stop layer is grown, consisting of a relaxed
Si$_{0.7}$Ge$_{0.3}$ layer where the composition matches that of the relaxed buffer. The ability to selectively etch Si over Si$_{0.7}$Ge$_{0.3}$ and vice-a-versa is the reason that alternating Si and Si$_{0.7}$Ge$_{0.3}$ etch-stop layers are used. This structure is ultimately capped with the strained Si device layer. The upper limit of the strained layer thickness is set by critical thickness constraints. The Mathews-Blakeslee criterion sets the equilibrium critical thickness limit for Si strained to 30% at a thickness of ~10 nm [40]. Strained Si can be growth thicker in the meta-stable regime as long as thermal process is limited to avoid relaxation. The device layers in the substrates fabricated in this work were grown in meta-stable regime at an as-grown thickness of 35 nm. All layers in this structure were un-doped. Fig. 2.1 depicts the etch-back structure grown for this work.

![Etch-back structure](image)

**Figure 2.1** The as-grown etch-back structure employed in this work. The SiGe grade is used to minimize the number of threading dislocations that reach the surface. The subsequent 0.5µm Si$_{0.7}$Ge$_{0.3}$ layer acts as a virtual substrate. The 100Å Si and 0.15µm Si$_{0.7}$Ge$_{0.3}$ etch-stop layers are in place to controllably approach the 350Å strained Si device layer during the etch-back process.

### 2.2 Wafer Bond Process

Once the etch-back structures are grown the wafers are prepared for bonding. Prior to bonding wafers are cleaned using a modified RCA clean. In this modified RCA cleaning sequence the SC-1 bath is replaced with a piranha solution. The cleaning sequence is as follows: 10 minutes in 3:1 H$_2$SO$_4$:H$_2$O$_2$ (110°C), 15 seconds in 50:1 HF:DI, 15 minutes in 6:1:1 DI:HCl:H$_2$O$_2$ (80°C), and a SRD
cycle. The modified clean minimizes the amount of Si loss incurred during the cleaning process. Low temperature oxide (LTO) is then deposited on the as-grown etch-back structure after wafer cleaning. The LTO will ultimately serve as a portion of the buried oxide in the SSDOI substrate. 5000 Angstroms of LTO is deposited followed by a densifying anneal. The densifying anneal was 6 hours at 650°C followed by 1 hour at 750°C. Chemical mechanical polishing (CMP) of the LTO was then conducted to reduce the crosshatch induced roughness on the surface of the oxide. Crosshatch is a relaxation mechanism involving surface undulations visible on the epitaxial layer surface in the form of a grid pattern aligned along the (110) directions on the wafer. As LTO deposition is conformal, the LTO surface mirrors the epitaxial surface to a certain extent. Crosshatch does not affect carrier transport due to the long-range nature of the surface undulations [41]. Removal of 2000Å of LTO by CMP is enough to bring the surface roughness down to acceptable levels for wafer bonding. After CMP a double piranha clean is used to remove any residual CMP slurry than may be on the LTO surface. The post-CMP cleaning sequence consists of the following: 10 minutes in 3:1 H₂SO₄:H₂O₂ (110°C) bath 1, 10 minutes in 3:1 H₂SO₄:H₂O₂ (110°C) bath 2, and a SRD cycle. Prior to bonding a handle wafer is also prepared. A 1000Å thermal oxide is grown on a p- CZ wafer. The 1000 Angstroms of thermal oxide will become a portion of the buried oxide in the final SSDOI substrate. It has been observed that oxide-to-oxide bonds are very robust [42]. The handle wafer will ultimately accept the strained Si device layer and the LTO portion of the buried oxide after layer transfer.

The bond process begins by cleaning the handle and etch-back wafers. These wafers are cleaned and prepared for bonding by undergoing a wet preparation sequence consisting of: 5 minutes in 5:1:1 DI:NH₄OH:H₂O₂ (80°C), 10 minutes 6:1:1 DI:HCl:H₂O₂ (80°C), 10 minutes in 5:1:1 DI:NH₄OH:H₂O₂ (80°C), and a SRD cycle. After wet bond preparation the wafer pairs are brought into contact in a wafer bonding apparatus which aligns the wafer pairs and brings them into forced contact for 120 seconds. Once intimate contact is made between the bond pairs the bond formed at the surface is enough to hold them together. A post bond anneal is conducted to strengthen this bond. The post
The bond anneal sequence used on the substrates in this work was 3 hours at 300°C, 3 hours at 400°C, and 20 minutes at 550°C in a nitrogen ambient.

After the post bond anneal wafers are packaged and shipped to a commercial vendor for grind back [43]. The grinding is conducted on the back-side of the wafer that the etch-back structure was grown on. The purpose of grinding is to remove most of the Si substrate on this structure. Grind-back makes the etch-back process simpler in that less material has to be removed chemically. Fig. 2.2 depicts the bond process described above.

**Figure 2.2** The bond sequence used in this work. (a) The as-grown etch-back structure is epitaxially grown in an Applied Materials Epi Centura LPCVD reactor. (b) This structure is prepared for bonding by depositing 5000Å of LTO. 2000Å of the LTO is CMP-ed away to obtain a surface smooth enough for bonding. A 1000Å thermal oxide is grown on a p-handle wafer. (c) The handle wafers is bonded to the epi etch-back wafer. (d) The bonded wafer pair is sent for grind-back at GDSI and the Si substrate on the etch-back wafer is ground away.
2.3 Etch-Back Process

The etch-back process begins once the wafers are returned from the grind back vendor. Before any further processing is conducted wafers are cleaned using a double piranha clean to remove any surface contamination that may have been introduced during grind back. The post-grind-back cleaning sequence consists of the following: 10 minutes in 3:1 H₂SO₄:H₂O₂ (110°C) bath 1, 10 minutes in 3:1 H₂SO₄:H₂O₂ (110°C) bath 2, and a SRD cycle. CMP is then conducted to remove the scratches introduced during the grinding process. The next step in the etch-back process is to chemically etch away the Si substrate until the SiGe grade is exposed. Tetra-methyl ammonium hydroxide (TMAH) heated to 80°C etches Si and stops on Si₀.₈Ge₀.₂ with a high level of selectivity (20:1) [44]. When the grade is exposed CMP is once again conducted to planarize any roughness induced by the initial etch-back process. After CMP the remaining material in the grade and the relaxed buffer is removed using a (3:2:1) solution of acetic acid: hydrogen peroxide: hydrofluoric acid [45]. This etch has a selectivity of 23:1 for Si₀.₇Ge₀.₃:Si, and etches Si₀.₇Ge₀.₃ at a rate of ~40 nm/min. The Si etch-stop layer is removed in a bath of tetra-methyl ammonium hydroxide heated to 80°C. The remaining SiGe etch stop layer is removed in a 5:1:1 solution of de-ionized water: ammonium hydroxide: hydrogen peroxide heated to 80°C. The selectivity of this etch is 18:1 over Si and etches Si₀.₇Ge₀.₃ at a rate of ~3 nm/min. Once the final SiGe etch-stop layer is removed the remaining structure is a strained Si layer directly on an oxide layer, SSDOI. Fig. 2.3 depicts the etch-back sequence described above.
The SiGe grade and relaxed buffer are removed in an acetic acid based etch to reveal the structure depicted in (b). The Si etch stop is removed with a dip in TMAH (80°C) (c). The remaining SiGe etch-stop layer is removed in an SC-1 bath to reveal the final SSDOI substrate (d).

2.4 Chapter Summary

In this chapter the fabrication sequence utilized to make 30% SSDOI substrates was described in detail. The as-grown structure consisting of a SiGe grade, Si$_{0.7}$Ge$_{0.3}$ relaxed buffer, double Si/Si$_{0.7}$Ge$_{0.3}$ etch-stop layers, and the strained-Si device layer was described. The SiGe grade and relaxed buffer reduce the number of threading dislocations that reach the surface and set the level of strain present in the device layer. The wafer bond process begins by depositing and planarizing LTO on the etch-back wafer. A Si handle wafer is then oxidized and bonded to the etch-back wafer. An annealing sequence is then used to strengthen the bond at the oxide interface. Grind-back is then conducted to thin the wafer pair. After grind-back a TMAH etch is used to remove the remaining Si substrate on the etch-back wafer. An acetic acid based etch is used to remove the SiGe grade and relaxed buffer. The subsequent Si etch-stop layer is then removed in with a dip in TMAH. The final SiGe etch-stop is
removed in an SC1 solution. The remaining structure is a Ge free strained Si film directly on a buried oxide, or SSDOI.
ULTRATHIN-BODY SSDOI N-MOSFET FABRICATION AND DATA EXTRACTION

MOSFETs fabricated on UTB FD SOI have inherently high source/drain series resistance. Although this series resistance can be mitigated by elevated source/drains and sophisticated contact schemes, to reduce process complexity in this work, long channel MOSFETs were fabricated utilizing a device architecture that allows accurate mobility extraction, independent of this series resistance [46]. In this chapter, the device design and fabrication flow of these devices is described, followed by a discussion of the mobility and thickness extraction methods. Some preliminary electrical results are also presented.

3.1 MOSFET Device Fabrication

When the resistance in the source/drain is large, as is the case in UTB MOSFETs, a significant voltage drop appears in the source/drain regions. This source/drain voltage drop makes it difficult to determine the intrinsic channel voltage drop. Knowing the channel voltage drop from the source to drain is essential when calculating the mobility. To bypass this issue a special long channel mobility extraction MOSFET device design was utilized [46]. This device architecture incorporates voltage tabs in the channel that are used to measure the intrinsic channel voltage. This channel voltage measurement is conducted independent of the applied source/drain voltage. Fig. 3.1 provides a diagram of the mobility extraction MOSFET design.
Figure 3.1 A diagram depicting the device architecture utilized in this work. The gate, source, drain, and channel voltage measurements tabs are indicated in the diagram. The channel voltage measurements tabs are utilized to measure the intrinsic channel potential independent of the source/drain series resistance. The MOSFET gate length and width are 100 μm and 15 μm respectively.

Devices were fabricated on 30% SSDOI substrates with an initial strained-Si thickness of 30 nm. Commercial unstrained SOI substrates from SOITEC were processed inline with the SSDOI substrates and served as controls [47]. The SOI substrates were thinned by sequential oxidation and chemical etching to 30 nm prior to device processing. This work was successfully completed because a wide range of MOSFET body thicknesses were obtained on a single substrate. To obtain a large range in channel thickness a channel thinning approach was used for both the SSDOI and SOI substrates. The channel thinning process began by depositing 220 nm of LTO onto the substrates. Holes were opened in the LTO that correspond to the channel of the mobility extraction MOSFETs. The exposed substrate was wet etched in a 5:1:1 solution of de-ionized water: ammonium hydroxide: hydrogen peroxide heated to 80°C. This solution will oxidize approximately 1 nm of Si in 1 minute. The oxide formed was removed with a 10 second dip in a 50:1 bath of HF:de-ionize water. Initially only a subset of the total number of die were exposed and had their channels thinned. More die were subsequently exposed and thinned along with the initially exposed die. This process was continued, exposing more die along the way, until the channel thicknesses on the die exposed initially were approximately 5 nm thick. All
thicknesses measurements were conducted on a spectroscopic ellipsometer. The cumulative exposure and etch approach provided a variety of channel thicknesses ranging from 5 nm to 30 nm on SSDOI. The channel thinning on the SOI substrates was excessive and the entire channel region was removed in the ultra-thin regime, sub-7 nm. Therefore only moderately thin channels (9 nm) were realized on SOI.

The device fabrication flow began by removing the LTO hard mask used during the channel thinning process. Device isolation was then accomplished by mesa dry etching. The mesa dimensions are greater than 10 microns, and therefore strain relaxation induced by patterning effects is assumed to be negligible [48,49]. A 3.4 nm gate oxide was formed by dry oxidation at 800°C. In-situ phosphorus doped polycrystalline Si was subsequently deposited to form the gate. The gate was anisotropically etched in a Cl₂ plasma. After the gate etch a forming gas anneal was conducted for 30 minutes at 500°C. Then 20 nm of LTO was deposited. The LTO served as a screen oxide during the subsequent source/drain implant. Ion implantation was conducted at Innovion [50]. The source/drain implant was conducted at 0° tilt with 4x10¹² ions/cm² at 15.5 keV. Dopant activation was achieved with an annealing sequence consisting of 2 minutes at 625°C and 10 seconds at 1000°C. Previous work indicates that strain is retained in SSDOI substrates for significant thermal processing above 1000°C [1,23,34]. Following implantation the screen oxide was removed and a 150nm LTO dielectric inter-layer was deposited. Contact vias were subsequently opened in the LTO. Metalization consisted of 500 nm of Al₀.₉₆Si₀.₀₂ with 150nm of underlying Ti to prevent Al spiking. Finally a forming gas anneal was conducted for 25 minutes at 425°C.

3.2 Preliminary Electrical Results

After the device fabrication process was completed, valid device operation was verified by conducting electrical measurements. MOSFET transfer characteristics were measured and are presented in Fig. 3.2. These devices were found to exhibit standard IV characteristics that can be observed in a conventional long channel MOSFET. Drive current is higher for MOSFETs fabricated on
30% SSDOI compared to those on unstrained SOI. This enhancement is attributed to the higher electron mobility in strained-Si.

![Graph showing drain current vs. drain voltage characteristics for UTB FD SOI and UTB FD SSDOI n-MOSFETs.](image)

**Figure 3.2** Drain current vs. drain voltage characteristics for n-MOSFETs fabricated in this work. Drive current is higher for devices fabricated on SSDOI compared to those on unstrained SOI. This enhancement is attributed in part to the higher electron mobility in strained Si.

Additional measurements were conducted to determine the quality of these devices. Subthreshold slope measurements, interpreted correctly, can indicate whether excessive levels of interface traps (D_it) exist at the substrate/gate-oxide interface. Fig. 3.3 presents representative subthreshold measurements conducted on UTB n-MOSFETs fabricated on 30% SSDOI (SS = 67 mV/dec) and SOI (SS = 65 mV/dec). The subthreshold swing observed in these two devices is nearly ideal. The theoretical value for SS is 59.6 mV/dec at room temperature for a UTB fully-depleted MOSFET fabricated on SOI [51]. Deviation from ideal can be attributed to a finite interface trap capacitance.
Figure 3.3 Subthreshold characteristics on n-MOSFETs fabricated on UTB SOI and SSDOI. The subthreshold swing for both devices is nearly ideal. Deviations from the ideal SS, 59.6 mV/dec, can be attributed to interface traps [51].

3.3 Mobility Extraction

The mobility extraction devices fabricated in this work have a gate length of 100 µm and a width of 15 µm. Due to the large scale of these dimensions these devices are assumed to obey the classic long channel MOSFET current equations. Drain current for a conventional long channel MOSFET is given by:

\[ I_D = W Q_c \mu E \]

Equation 3.1

where \( I_D \), \( W \), \( Q_c \), \( \mu \), and \( E \) are the drain current, device width, channel charge, effective mobility, and lateral electric field from drain to source. Effective mobility is extracted utilizing this basic relation in the linear region of operation of the MOSFET. The effective extracted mobility is given by:

\[ \mu = \frac{I_D L}{W Q_c V_{DS}} \]

Equation 3.2

where \( I_D \) and \( V_{DS} \) are the measure drain current and intrinsic drain-to-source voltage. This relationship is applied for small values of \( V_{DS} \) (< 100 mV) where the drain current is directly proportional to \( V_{DS} \).
As mentioned earlier the devices fabricated have voltage measurements tabs that are utilized to measure the intrinsic channel potential. Devices were operated in the linear regime where the assumption of a linearly varying channel potential between the voltage tabs is valid. The intrinsic drain-to-source potential drop is calculated by 

\[ V_{DS} = \frac{V_{tab} L_{gate}}{L_{tab}}, \]

where \( V_{tab} \), \( L_{gate} \), and \( L_{tab} \) are the potential drop between the voltage tabs, the gate length, and the distance between the tabs, respectively. In equation 3.2, \( Q_c \) is the inversion charge density determined by integrating the gate-to-channel capacitance-voltage (C-V) characteristics of the MOSFET gate:

\[ Q_c = \int_{-\infty}^{V_c} C_G dV_G \]  

Equation 3.3

C-V measurements were conducted at a frequency of 100 kHz to determine the gate-to-channel capacitance characteristics. Interface states can track low frequency signals, and thus C-V measurements were conducted at a frequency of 100 kHz to minimize stretch out in the C-V characteristics due to interface traps. Fig. 3.4 illustrates the extracted mobility for devices fabricated in this work and prior work conducted by I. Aberg [25]. The mobility results on SSDOI perfectly overlay the results reported by I. Aberg, but the mobility results on SOI are slightly degraded.
Figure 3.4 Electron effective mobility for 30% SSDOI and the SOI control devices for both this work and that of I. Aberg [25]. The mobility result for the SOI control is slightly degraded compared to that previously reported. For the devices in this work, the SSDOI body thickness is 25 nm and the SOI control is 16 nm thick. A mobility enhancement factor of ~1.8x is seen in SSDOI over the unstrained SOI devices.

3.4 Device Body Thickness Extraction

Accurate determination of the device body thickness was essential for the successful completion of this study. Two gate-to-channel capacitance-voltage (C-V) fitting schemes were utilized in extracting the device body thickness by fitting simulated C-V curves to measured data. One scheme was utilized for devices with a body thickness greater than 3 nm and the other for devices with a body thickness less than 3 nm. The one dimensional Schrödinger-Poisson solver Schred was used in fitting simulated C-V characteristics to measured results [52]. Schred input files were modified to simulate C-V characteristics for an UTB SSDOI MOS structure by assuming carriers only fill the unprimed $\Delta_2$-valley subbands. This is a reasonable assumption because strain induced band splitting (~200 meV) in 30% SSDOI results in carriers preferentially occupying the $\Delta_2$-valleys [27]. For body thicknesses above 3 nm back-bias C-V measurements were used to extract the body thickness. A back bias voltage of 30V was utilized for all back bias C-V measurements. Applying a back bias to the Si substrate results in inversion charge initially forming at the back buried oxide/Si interface. As the front gate bias
is swept further into inversion the charge shifts to the front gate oxide/Si interface. This shifting of the inversion charge produces a plateau in the C-V characteristics, and fitting the shape of these curves enables unique extraction of the body thickness. The gate oxide thickness, 3.4 nm, was obtained from XTEM imaging (see for example Fig. 3.7) and held as a fixed parameter during simulations. It should be noted that the oxide thickness extracted from XTEM is consistent with the value extracted from C-V measurements, ~3.4 nm. The plateau height is very sensitive to the Si body thickness and the corresponding value is a series addition of the gate-oxide and the Si-body capacitance as given by:

\[
C_{\text{plateau}} = \left( \frac{1}{C_{\text{SOI}}} + \frac{1}{C_{\text{gox}}} \right)^{-1}
\]

Equation 3.4

In Fig. 3.5 (a) back bias C-V characteristics simulated in Schred illustrate the high level of sensitivity of the C-V curve to Si body thickness. The shape of the plateau in the C-V characteristics was found to be fairly sensitive to SOI thickness for dimensions as low as 3 nm. Figure 3.5 (b) shows the sensitivity of the C-V characteristics to the buried oxide thickness. The buried oxide thickness has a relatively small impact on the threshold voltage for the back Si/BOX interface, and does not affect the height of the plateau in the C-V measurement. Figure 3.6 illustrates two fits that were used to extract the device body thickness in this thickness regime.
**Figure 3.5** Simulated C-V characteristics using Schred. A sensitivity analysis was performed using the Schred simulator to determine the effect of the SSDOI body thickness on back bias C-V characteristics. Varying the body thickness alters the shape of the C-V characteristics, and a 1 nm change in thickness has a significant impact on the curve. The effect of varying the BOX thickness is also visible in the right-hand plot where the thickness of the buried oxide is seen to determine the onset of inversion of the bottom Si/BOX interface. The back bias voltage in these simulations was 30V.

![Figure 3.5](image)

**Figure 3.6** Measured and simulated C-V characteristics for devices with body thicknesses greater than 3 nm, using the back bias method. The body thicknesses extracted are 12 nm and 5.3 nm. C-V characteristics are plotted with and without the back bias. Simulated results in Schred were utilized to extract the body thickness. The simulations were conducted assuming a fixed 3.4 nm gate oxide and 390 nm buried oxide thickness for both devices. The back bias voltage in these measurements and simulations was 30V.

For devices below 3 nm C-V characteristics were also fitted using the Schred simulator. As the body thickness is scaled below 3 nm the subband energy increases resulting in a larger threshold voltage ($V_t$) [53]. The larger $V_t$ shifts the C-V characteristics. For devices with body thickness below 3 nm, C-V characteristics were fitted using the Schred simulator by fitting simulated C-V characteristics to the shifted C-V characteristics. As the body thickness is scaled the inversion charge is essentially squeezed making the C-V characteristics more abrupt. These quantum confinement induced effects can be simulated in Schred and were utilized to extract the body thicknesses for dimensions less than 3 nm. Cross section transmission electron microscopy was conducted to determine the average body thickness of one device in the sub-3nm thickness regime and utilized to calibrate the simulations. One of several XTEM images taken is shown in Fig. 3.7. The average SOI thickness was extracted from
several high magnification images taken along the channel. The images revealed an average thickness of 2 nm and a standard deviation of 0.5 nm. The apparent variation in the body thickness in the imaged device was larger than expected, based upon surveys of high resolution XTEM micrographs from previous work, obtained from Åberg [54]. The origin of the larger variation observed in the thickness by XTEM in this experiment is unknown. The impact of this thickness variation on the extracted mobility is discussed in Chapter 4.

The thickness of the gate oxide was also extracted from XTEM imaging and was determined to be 3.4 nm. The thickness of the buried oxide for the device imaged was measured to be 370 nm. The buried oxide (BOX) does vary across the wafer due to the variation in thickness of the deposited LTO on the etch-back wafer. A BOX thickness variation from 370 nm to 430 nm was extracted from back bias C-V measurements. Recall that the buried oxide thickness does not affect the extracted Si layer thickness therefore this thickness was allowed to vary to provide the best fit. The devices with a body thickness less than 3 nm were all located on the same die and therefore the amount of fixed charge and gate oxide thickness. The SOI thickness was the only parameter varied between these devices. Fig. 3.8 presents the measured and simulated C-V results for the imaged device along with another device located on the same die. XTEM was used to assist in calibrating the fixed charge shift of the simulated C-V characteristics.
Figure 3.7 Low and high magnification cross section transmission electron micrographs of an UTB n-MOSFET on 30% SSDOI. The low magnification image provides a good indication of the variation present in the thinned-back film on this device. The high magnification image is of a 2 nm section of the channel. The average channel thickness on this device is 2 nm and the standard deviation is 0.5 nm.

Figure 3.8 Measured and simulated C-V curves for (a) a device in the ultrathin regime and (b) for the device imaged using XTEM. In (b) the body thickness in Schred was forced to be 2 nm to match the XTEM data. The dominant effect used in fitting to these different devices is the shift in threshold voltage associated with scaling the body thickness.

3.5 Chapter Summary

In this chapter the device fabrication process was described. A special device design was utilized to bypass the high source/drain series resistance. The channel was thinned on these devices to obtain a large range in body thickness. Thinning occurred on a die by die basis and a cumulative thinning sequence resulted in a range in channel thickness from 5 nm to 30 nm. After channel thinning
the gate stack was formed and metallization was conducted to contact the source, drain, gate, and channel voltage tabs. Preliminary electrical data was provided. Fundamental current voltage characteristics were presented and are consistent with predicted MOSFET behavior. Subthreshold characteristics were provided and a subthreshold swing of < 70 mV/dec was reported for 30% SSDOI and the SOI control. Deviations in the SS from the ideal value were attributed to interface traps. The process to extract the effective mobility was described and preliminary mobility results were provided. Initial mobility results on 30% SSDOI exhibit a ~1.8x enhancement over unstrained SOI and are consistent with previously reported results. The methods used in extracting the device body thickness were also described in this chapter. The device body thickness extraction process consists of two extraction methods where one scheme was used on devices with a body thickness greater than 3 nm and another for thicknesses less than 3 nm. Fits to the measured CV characteristics were then provided for two devices in each thickness regime. XTEM was used to image one device to assist in calibrating the fixed charge shift of the simulated C-V characteristics.
CHAPTER 4

ELECTRON MOBILITY IN UTB SOI AND SSDOI N-MOSFETS

In this chapter electron transport in n-MOSFETs fabricated on ultrathin-body SOI and 30% SSDOI is discussed. The dominant scattering mechanisms that limit mobility in these two substrates are explained. Previously reported results on the mobility dependence on body thickness for n-MOSFETs fabricated on UTB SOI are presented and explained. New experimental measurements of the dependence of mobility on thickness for UTB n-MOSFETs fabricated on 30% SSDOI are presented and a theoretical explanation is provided.

4.1 Scattering Mechanisms in UTB SOI/SSDOI N-MOSFETS

As carriers traverse the channel they undergo scattering events. These scattering events, along with the effective mass, limit the effective mobility of carriers. Phonon, coulombic, carrier-carrier, surface roughness, and thickness fluctuation scattering are mechanisms that determine the effective mobility. These scattering mechanisms occur as parallel processes and therefore add as such. Reducing some of these scattering components is in part the reason that strained-Si provides a mobility enhancement over unstrained-Si. Some of the scattering mechanisms mentioned above do not play as dominant a role in limiting the mobility as others do. The low doping of the channel material in the MOSFETs fabricated in this work suggests that Coulombic scattering from ionized impurities is not a dominant scattering mechanism although excessive interface traps at the gate and buried oxide interfaces may act as Coulombic scattering centers when the body thickness becomes comparable to the inversion layer thickness. Surface roughness and carrier-carrier scattering events are primarily of concern at high carrier densities. In this work, the emphasis of the mobility measurements was for moderate to low carrier densities due to the fragile nature of the gate dielectric. Thus, in the theoretical
analysis, these two scattering mechanisms are assumed to be negligible. When high quality dielectric interfaces are used, electron transport in SOI and SSDOI thicker than \(-3\) nm is limited predominantly by phonon scattering. In the following section phonon scattering is explained and the trend that the phonon-limited mobility follows as the body thickness is reduced is described.

4.1.1 Phonon Scattering

From the description provided by Lundstrom [55] when carriers enter the channel they can be described as having a momentum \(p_0\). As these carriers are swept across the channel they undergo scattering events. The effective scattering rate, \(1/\tau(p_0)\), is a culmination of scattering rates between \(p_0\) and other states \(p'\). The scattering rates for parallel processes can be calculated as follows:

\[
\frac{1}{\tau(p_0)} = \sum_{p'} S(p_0, p')
\]

Equation 4.1

Where the transition rates, \(S(p_0, p')\), are determined by evaluating Fermi’s Golden Rule. The initial step in evaluating the transition rate is to determine the matrix element of the scattering potential:

\[
H_{p' p} = \int_{-\infty}^{\infty} \varphi_{p'}^* U \varphi_p \, d^3r
\]

Equation 4.2

where \(U\) is the scattering potential. The transition rate can now be determined by:

\[
S(p, p') = \frac{2\pi}{\hbar} \left| H_{p' p} \right|^2 \delta(E(p') - E(p) - \Delta E)
\]

Equation 4.3

where \(\Delta E\) is the change in energy that results from the scattering event.

For 2D carriers, as for electrons in UTB SOI and SSDOI, the acoustic phonon scattering rate between an initial subband \(i\) and a final subband \(f\) is given by:
Equation 4.4

\[
\frac{1}{\tau_0} = \frac{\pi D_A^2 k_B T_c}{\hbar C_i} \frac{1}{W_h} g_{2Df}(E)
\]

where \(D_A\), \(1/W_h\), and \(g_{2Df}(E)\) are the acoustic deformation potential, the effective width of the envelope function, and the two dimensional density of states, respectively. For two-dimensional carriers the density of states is given by:

\[
g_{2Df} = \frac{m^*}{\pi \hbar^2}
\]

Equation 4.5

The effective width of the envelope function is calculated as:

\[
\frac{1}{W_h} = \lim_{z \to \infty} \int F_i(z) |F_j(z)|^2 \, dz
\]

Equation 4.6

where \(F_i(z)\) and \(F_j(z)\) are the envelope functions in the initial and final state. In an infinite square potential well, the effective widths of the envelope function for both intra- and inter-subband transitions are:

\[
\frac{1}{W_h} = \lim_{z \to \infty} \int F_j(z) |F_j(z)|^2 \, dz = \frac{3}{2W} \quad i=j
\]

Equation 4.7a

\[
\frac{1}{W_h} = \lim_{z \to \infty} \int F_j(z) |F_j(z)|^2 \, dz = \frac{1}{W} \quad i\neq j
\]

Equation 4.7b

where \(W\) is the width of the potential well. Combining equations 4.7a, 4.7b, and 4.4 we obtain the intra-subband scattering rate:

\[
\frac{1}{\tau_0} = \frac{\pi D_A^2 k_B T_c}{\hbar C_i} \frac{3}{2W} g_{2Df}(E)
\]

Equation 4.8a

and the inter-subband scattering rate:
With the scattering rate defined we can see how it relates to the mobility. Effective mobility is given by:

$$\mu = \frac{q \tau}{m}$$  \hspace{1cm} \text{Equation 4.9}

As the width of the infinite potential well is scaled the mobility reduces in a linear fashion for both intra- and inter-subband scattering. The profile of the finite potential well in UTB SOI and SSOI has a triangular shape, and thus the above analysis is an approximation of the dependence of mobility on body thickness. Above a certain thickness the inversion charge is confined by the triangular shape of the conduction band, rather than by the SOI structure. Therefore, for thicker substrates, it is expected that the mobility should exhibit little or no dependence on body thickness. In the ultra-thin regime, however, where the film thickness is confining the inversion charge, a decrease in mobility with body thickness is expected, based upon the above analysis.

### 4.1.2 Thickness Fluctuation Scattering

As the body thickness is scaled to very small dimensions (< 5 nm) slight variations in the device layer thickness, even variations on the order of a few atomic planes, constitute a significant portion of the total film thickness. These fluctuations result in significant variation in the subband energy levels in the conduction band. For a square potential well the n\textsuperscript{th} subband energy is given by:

$$E_n = \frac{\hbar^2 \pi^2 n^2}{2 m_c T^2}$$  \hspace{1cm} \text{Equation 4.10}

where $m_c$ and $T$ are the effective mass perpendicular to the transport plane and the thickness of the potential well. In Equation 4.10 for small dimensions even a small variation in the well thickness can result in a significant change in the subband energy. The variation in subband energy for the $\Delta z$-
valleys (0.916\textit{m}_0) and \Delta_4-valleys (0.19\textit{m}_0) with a film thickness fluctuation of +/- 0.2 nm (+/~1 monolayer) is plotted versus body thicknesses in Fig. 4.1. The low mass (0.19\textit{m}_0) \Delta_4-valley subband energy is affected more severely by the fluctuation in thickness. Electrons in SSDOI predominantly reside in the \Delta_2-valley, so fluctuations in the \Delta_2-valley subband energy are of greater concern. Fig. 4.1 indicates that thickness fluctuation scattering should be visible when the film thickness is less than \sim 3 nm. When the fluctuation in conduction band energy exceeds the thermal energy of the inversion charge carriers, thickness fluctuation induced scattering begins to become a significant scattering mechanism that drastically limits the mobility. The mobility dependence on thickness is rooted in the potential variations induced by the thickness fluctuation and is given by:

$$\Delta V = \frac{\partial E}{\partial T_{Si}} \Delta$$

where \Delta is the height of the fluctuation in the Si. This potential variation translates into a carrier scattering mechanism with a mobility dependence of

$$\mu \sim \left(\frac{1}{\Delta V}\right)^2 \propto T_{Si}^{6}$$

Equation 4.12

At low temperatures phonon scattering is suppressed and the mobility is predominantly limited by the thickness fluctuations induced scattering. Previous experimental work in UTB SOI and GaAs/AlAs quantum wells shows that the mobility at low temperatures follows the \textit{T}^{6}, where \textit{T} is the film thickness, dependence that was theoretically predicted [4,56].
Figure 4.1 The estimated change in conduction band energy for the $\Delta_2$-valley (0.916$m_e$) and the $\Delta_4$-valley (0.19$m_e$) subbands. The low mass $\Delta_4$-valley subband energy is affected more severely by the fluctuation in thickness. The change in conduction band energy was calculated by taking the difference in energy for a +/- 1 monolayer variation in SOI thickness. A square potential well approximation was made for these calculations. The thermal energy of carriers is indicated by the dashed line.

4.2 Electron Mobility in UTB SOI MOSFETs

Electron mobility in MOSFETs fabricated on SOI where the SOI thickness is much larger than the thickness of the inversion layer is essentially unchanged from that of bulk Si. As the SOI thickness is reduced and becomes comparable to the inversion layer thickness the effective mobility is reduced. This degradation stems from confining the carriers in the direction perpendicular to transport. In section 4.1.1 it was shown that confining the carrier wavefunction results in a spreading of the carriers in momentum space resulting in a higher level of phonon coupling. The increased phonon coupling results in a higher phonon scattering rate. As was mentioned previously, effective mobility is inversely proportional to the phonon scattering rate and therefore the mobility is reduced as a result of decreasing the SOI thickness.

An initial reduction in mobility is observed as the body thickness is scaled in UTB SOI n-MOSFETs, but as the thickness is reduced even further a modulation occurs in the conduction band of
Si resulting in a mobility peak, as shown in Fig. 4.2 By making the infinite quantum well approximation, as we did in section 4.1.1, we see that the subband energy is inversely proportional to the SOI thickness squared and the carrier effective mass. Therefore as the SOI thickness is reduced the subband energy increases. The effective mass of the $\Delta_4$-valleys is smaller than that of the $\Delta_2$-valleys resulting in the subband energy of the $\Delta_4$-valleys increasing more rapidly as the SOI thickness is reduced. This increased energy difference between the $\Delta_4$-valley and $\Delta_2$-valley subbands results in a reduction in inter-valley scattering. Fig. 4.3 illustrates nextnano simulated results for subband occupation as the body thickness is scaled [57]. Below 3 nm, nearly all the inversion charge resides in the $\Delta_2$-valley subbands. The reduction in intervalley scattering coupled with the carriers occupying the low transverse mass $\Delta_2$-valleys results in a mobility increase as the body thickness is scaled. Further scaling of the body thickness should result in an increase in intra-valley and thickness fluctuation scattering. The increase in these scattering components should result in a significant mobility drop below $\sim$3.5 nm.

The calculated phonon-limited mobility is observed to exhibit a mobility enhancement peak at 3 nm [58,59]. Uchida et al. have experimentally documented this behavior on UTB SOI [4,53]. Below $\sim$3 nm at room temperature, thickness fluctuation and intra-valley scattering are the dominant mobility limiting mechanisms. In this thickness regime the mobility is significantly degraded as the body thickness is scaled further, as illustrated in Figure 4.2.
Figure 4.2 Electron mobility in UTB SOI (at an effective field of 0.3 MV/cm) as a function of body thickness. The mobility peak observed near 3.5 nm is a result of the quantum confinement induced subband slitting. From Uchida, et al [4].

Figure 4.3 Subband occupancy in SOI for various body thicknesses. nextnano was utilized to calculate the subband occupational fraction for an inversion charge density of $3 \times 10^{12} \text{ cm}^{-2}$. As the body thickness is reduced carriers preferentially occupy the $\Delta_2$-valley subbands.
4.3 Electron Mobility in UTB SSDOI MOSFETs

UTB FD MOSFETs are very attractive from an electrostatic standpoint. As the gate length is scaled on these devices the body thickness is scaled in a corresponding fashion to help maintain electrostatic performance. The mobility behavior as the body thickness is scaled has been well documented in unstrained SOI and was presented in section 4.2. In chapter one the merits of SSDOI were presented. The enhanced carrier transport characteristics and equivalent electrostatic control provided by SSDOI in comparison to unstrained SOI makes it a promising substrate for deeply scaled devices. In this section new results are provided which show the electron mobility dependence on body thickness for UTB n-MOSFETs fabricated on 30% SSDOI. The lower thickness limit upon which SSDOI provides significant mobility enhancements over SOI is also identified.

![Figure 4.4](image)

**Figure 4.4** Measured effective electron mobility for UTB MOSFETs fabricated on 30% SSDOI in this work. The mobility decreases as the body thickness is scaled, particularly below 4 nm. The mobility of 15 nm UTB n-MOSFET control devices on SOI is also plotted for comparison. A mobility enhancement of ~1.8x is seen over the device on unstrained-SOI, for thick SSDOI films.

The successful completion of this work was contingent upon obtaining mobility results for UTB n-MOSFETs fabricated on SSDOI with a large range in body thickness. Channel thinning results
presented in Chapter 3 revealed a set of devices with initial SSDOI film thickness ranging from 5 nm to 30 nm. Fig. 4.4 illustrates the extracted electron mobility as a function of vertical effective field, with peak mobility ranging from \( \sim 300 \text{ cm}^2/\text{Vs} \) to \( \sim 1000 \text{ cm}^2/\text{Vs} \). The lowest peak mobility corresponds to the device that endured the most channel thinning and the largest mobility corresponds to a device that was not thinned. This observation suggests the existence of thickness dependent mobility degradation. After extracting the mobility of several devices the corresponding body thickness was extracted utilizing the methods outlined in section 3.4. Extracting the body thickness revealed a range in body thickness from 2 nm to 25 nm. In Fig. 4.4 the corresponding body thickness is indicated next to each curve. The mobility is observed to decrease as the body thickness is scaled. It is interesting to note that even with body thickness of 3.6 nm, 30% SSDOI provides a \( \sim 1.8x \) mobility enhancement over 15 nm unstrained SOI.

![Figure 4.5](image.png)

**Figure 4.5** Electron effective mobility in UTB NMOS fabricated on SSDOI as a function of body thickness for devices in this work (solid symbols) and as published by Uchida (open symbols). Effective mobility at an effective field of 0.3 MV/cm is plotted for each body thickness. A monotonic reduction in mobility occurs from 18 nm to 3.6 nm. Below 3.6 nm thickness fluctuation induced scattering limits the mobility, resulting in stronger thickness dependence. The electron mobility thickness dependence is also plotted for the UTB SOI control devices in this work. A 2x enhancement is seen for body thicknesses above 7 nm. Experimental data published by Uchida for NMOS devices fabricated on UTB SOI is also plotted [4]. As discussed in the text, due to large scale thickness
variation present in the SSDOI film in this work, the mobility observed for UTB SSDOI may be overestimated for devices below 3 nm.

In Fig. 4.5 the measured effective mobility is plotted as a function of body thickness. This graph reveals a monotonic reduction in mobility as the body thickness is scaled from 16 nm to 3.6 nm. It is interesting to note that in this thickness range 30% SSDOI exhibits a mobility enhancement of ~1.8x over unstrained SOI, for an effective field of 0.3 MV/cm. The origin of the monotonic reduction in mobility is rooted in the thickness dependence of the relevant scattering mechanisms in this thickness regime. In 30% SSDOI the large energy difference between the Δ₂-valley and Δ₄-valleys (~200 meV) results in the mobility being limited primarily by phonon scattering which is dominated by intra-valley transitions. Fig. 4.6, a plot of subband occupancy, supports this and reveals that as the body thickness is scaled essentially all carriers at an inversion density of 3x10¹² cm⁻² reside in the Δ₂-valleys at all thicknesses. In an infinite square potential well the intra-subband scattering rate is given by:

\[
\frac{1}{\tau} = \frac{\pi D_k^2 k_B T_L}{\hbar c} \frac{3}{2W} g_{2D}(E)
\]

Equation 4.1

Recalling that the effective mobility is inversely proportional to the carrier scattering rate reveals the phonon-limited mobility in an infinite square well is linearly proportional to the well width. Esseni has calculated the phonon-limited mobility for transport in the Δ₂-valleys for UTB n-MOSFETs on SOI. These calculations reveal that the phonon-limited mobility is independent of body thickness when the body thickness is greater than ~8 nm [60]. In this thickness regime the inversion charge is only confined by the triangular shape of the conduction band, rather than by the SOI structure. Therefore, for thicker substrates, the calculated phonon-limited mobility has no dependence on body thickness. The slight mobility dependence observed in UTB n-MOSFETs on 30% SSDOI may result from the presence of other thickness dependent mobility-limiting mechanisms such as Coulombic scattering. As the body thickness is scaled interface traps at the front and back oxide-Si interface can become a significant scattering mechanism as the Coulombic scattering centers encroach on the inversion layer.
Figure 4.6 Subband occupancy in SSDOI as a function of body thickness. The strained induced band splitting present in biaxial strained Si results in carriers preferentially occupying the low transverse mass Δ2-valley subbands. The band splitting also acts to suppress inter-valley scattering resulting in a higher effective electron mobility.

For body thicknesses below 3.6 nm the observed mobility degrades much more drastically as the body thickness is scaled. From direct comparison of results obtained from this work for 30% SSDOI with reports by Uchida for SOI in Fig. 4.5, it appears that 30% SSDOI exhibits higher mobilities compared to unstrained SOI in the sub-3 nm thickness regime. Below 3 nm the subband structures in the case of SOI and 30% SSDOI are very similar. Electrons in both materials predominantly reside in the Δ2-valley subbands, as is shown in Fig. 4.3 and 4.6, and intra-valley scattering is the dominant phonon scattering mechanism. The correlation in subband structure between these two substrates translates to similar phonon-limited mobility dependences. Phonon-limited mobility calculations reported by Esseni supports this [60]. The other mobility limiting mechanism present in this thickness range is thickness fluctuation induced scattering which was described in detail in section 4.1.2. To obtain the mobility enhancement in the sub-3 nm thickness regime that exists in Fig. 4.5 the severity of the thickness fluctuation must be improved for SSDOI over SOI, which is unlikely. A more plausible explanation for the apparent mobility enhancement may be rooted in the
presence of large-scale variations in the film thickness in addition to the small scale thickness fluctuations, which result in an overestimation of the mobility for body thicknesses below 3 nm, as explained below.

![Normalized thickness distribution](image)

**Figure 4.7** A representation of the thickness distribution for the device imaged using cross-sectional transmission electron microscopy. A normalized thickness distribution is assumed.

Fig. 4.7 is a normal probability density function representing the thickness distribution of the device imaged in Fig. 3.7. From the XTEM imaging of this device the mean film thickness and standard deviation were extracted to be 2 nm and 0.5 nm respectively. The C-V extracted body thickness for the imaged device corresponds to the mean of the normalized distribution. The extracted mobility corresponds to the expectation value of the mobility as given by:

$$
\langle \mu \rangle = \int_{\delta}^{\infty} \mu(T)P(T)dT
$$

Equation 4.3

where $\mu(T)$ is the mobility dependence on body thickness and $P(T)$ is the normalized thickness probability density function. In this thickness regime the mobility thickness dependence appears to be non-linear, $\mu(T)=AT^b$ where $b>1$, even at room temperature for holes and electrons in untrained SOI.
When the dependence of mobility on thickness is strong, and a variation exists in the film thickness, the extracted mobility will be larger than the mobility corresponding to the mean thickness of the SSDOI. Thus, the extracted mobility at a given average thickness may be overestimated in the sub-3 nm thickness regime. In Fig. 4.8 a piecewise continuous mobility model is used to illustrate that the extracted mobility is overestimated in the thin regime when the mobility thickness dependence is strong and large-scale variation exists in the film thickness. The piecewise model has a mobility thickness dependence where $\mu \propto T_s^p$ below 3 nm and a logarithmic dependence is utilized above 3 nm. The extracted mobility overestimate increases below ~3 nm as the mobility dependence on thickness increases. For thicknesses above ~4 nm the mobility has a much weaker dependence on body thickness and the difference between the extracted mobility and the mobility corresponding to the piecewise model is minimal. Therefore the extracted mobility and thickness provided in Fig. 4.5 should be accurate above 4 nm. The conclusion can then be drawn from the results provided in Fig. 4.5 that above ~4 nm a significant electron mobility enhancement (~1.8x) can be observed for SSDOI compared to unstrained SOI.
Figure 4.8 Piecewise continuous mobility model versus body thickness illustrates the extracted mobility overestimate in the sub-3 nm thickness regime. The dashed line represents a likeness of the mobility thickness dependence for UTB n-MOSFETs and the symbols represent the extracted mobility when a finite film thickness variation is present. The mobility overestimate increases as the film thickness variation increases for body thicknesses less than ~3 nm. Above ~4 nm the extracted mobility tracks the piecewise mobility model because of the weak thickness dependence.

4.4 Chapter Summary

In this chapter the dominant scattering mechanisms in UTB SOI and SSDOI were presented and explained. The mobility thickness dependence in UTB SOI was then explained and experimental data collected by Uchida was presented. New mobility results on SSDOI were then presented. A significant mobility enhancement, ~1.8x, is observed for body thicknesses greater than 3 nm over 15 nm unstrained SOI. Below 3 nm the mobility in SSDOI degrades quickly as the body thickness is scaled. The results are encouraging for the use of SSDOI in future technology nodes.
CHAPTER 5

SUMMARY

In Chapter 1 the origin of the observed mobility enhancement in strained Si was discussed. Changes in the conduction and valence band are the origin of the mobility enhancement strained Si provides for both electrons and holes compared to unstrained Si. Device results for MOSFETs fabricated on bulk strained-Si and SSDOI were presented. Observed electron mobility enhancements in Si strained to $\text{Si}_{0.8}\text{Ge}_{0.2}$ is $\sim 1.8x$. SSDOI provides enhanced electron and hole transport as well as the superior electrostatic control that unstrained SOI exhibits in ultrathin-body (UTB) MOSFETs. The substrate fabrication process for 30% SSDOI used in this work was outlined in Chapter 2. The epitaxial growth process, bond, and etch-back sequence were described in detail. A Kelvin-type mobility extraction long channel MOSFET design was utilized in this work to bypass the high series resistance in UTB MOSFETs. The design and fabrication sequence of these MOSFETs was outlined in chapter 3. Preliminary electrical data was presented and revealed normal MOSFET device performance and excellent subthreshold characteristics (< 70 mV/dec). Details of the mobility extraction process were then provided.

The body thickness extraction method was also described in chapter 3. Two extractions schemes were utilized in this work. One scheme was used for devices with a body thickness below 3nm and another for those with a body thickness above 3 nm. Body thickness in device with dimensions greater than 3nm was based on back bias C-V measurements. For devices with body thickness dimensions below 3 nm a threshold voltage shift resulting from quantum confinement effects was used to extract the body thickness. In the sub-3 nm regime XTEM imaging was used to determine the body thickness of one device and calibrate the simulator for use in extracting the body thickness for
other devices in this regime. In chapter 4 the dominant scattering mechanisms in UTB SOI and SSDOI were presented and explained. The mobility thickness dependence in UTB SOI was explained and experimental data collected by Uchida was presented. New mobility results on 30% SSDOI were then presented. A significant enhancement in mobility, ~1.8x, is observed for body thicknesses greater than 3 nm over unstrained SOI. Below 3 nm the mobility in 30% SSDOI degrades quickly as the body thickness is scaled. Some large-scale variations in the body thickness were observed by XTEM and result in some overestimation of the mobility for film thicknesses below 4 nm (i.e. in the regime where the mobility depends strongly on film thickness). The mobility versus thickness results presented reveal that the lower bound upon which 30% SSDOI provides a substantial mobility enhancement (~1.8x) over unstrained SOI is approximately 3 nm.


43. GDSI, Grinding and Dicing Services Inc., http://www.wafergrind.com


47. SOITEC SA, http://soitec.com


50. Innovion Inc., http://www.innovion.cc


52. Schred 2.0 User’s Manual [online]. Available at: http://www.nanohub.org


54. I. Åberg, private communication.


57. nextnano3 available at http://nextnano.de

