Micromachined Printheads for the Direct Evaporative Patterning of Organic Materials

By

Valérie Leblanc

Diplôme d’ingénieur de l’Ecole Polytechnique

Submitted to the Department of Materials Science and Engineering
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Materials Science and Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

June 2007

© Massachusetts Institute of Technology, 2007. All Rights Reserved.
Micromachined Printheads for the Direct
Evaporative Patterning of Organic Materials

By
Valérie Leblanc

Submitted to the Department of Materials Science and Engineering on
May 23, 2005, in partial fulfillment of the requirements for the Degree of
Doctor of Philosophy in Materials Science and Engineering

Abstract

Organic optoelectronic devices are appealing for low-performance applications on very
low cost and flexible substrates, due to their low-temperature processing. However, it still
remains a challenge to develop suitable fabrication techniques to pattern organic thin
films on low-cost, large-area substrates. The two techniques used commercially are ink-
jet printing of polymers, which limits the morphology and performance of devices, and
shadow-masking of vacuum sublimation for small molecule materials, which is not
scalable to large-area substrates.

In this thesis, we investigate the use of MicroElectroMechanical Systems (MEMS) to
provide new ways of patterning organic materials deposited by an evaporative process.
We present the design, fabrication, modeling and characterization of two generations of
micromachined printheads developed to expand the possibilities of printing of organic
optoelectronics.

The design and fabrication of a compact electrostatic actuator enabling the first
generation of printhead is first presented. It is then used to actuate a microshutter, and
modulate the flux of evaporated organic materials in a vacuum chamber. We prove the
feasibility of evaporative printing of small molecular organic materials at resolutions of
the order of 800 dpi with high-throughput on large areas. We demonstrate that
MicroElectroMechanical Systems can be used to pattern organic thin films in a way that
combines the advantages of ink-jet printing and thermal evaporation.

We also present the design and fabrication of a microevaporator for molecular organics,
and show its suitability for the ambient printing of devices on low-cost substrates,
without the limitations of ink-jet printing due to the drying of solvent on the substrate.
We demonstrate the feasibility of using an array of pores in a membrane to capture
molecular organic materials delivered by a solvent and an integrated microheater to
release them by evaporation onto a substrate. This second generation of printhead enables
 evaporative printing of organic materials at ambient pressure.

This thesis also provides a study of the failure of thin film platinum heaters used in the
second generation printheads. We study the effect of current level, temperature, presence
of a membrane, anneal conditions, and adhesion layer thickness on the failure of the
heaters.
Thesis Committee:

Martin A. Schmidt
Thesis Supervisor, Professor of Electrical Engineering

Vladimir Bulović
Thesis Co-advisor, Associate Professor of Electrical Engineering

Francesco Stellacci
Finmeccanica Assistant Professor of Materials Science and Engineering

Michael F. Rubner
TDK Professor of Polymer Materials Science and Engineering
Acknowledgements

Since the first draft of this thesis didn’t have an acknowledgements section, my advisors joked that I had nobody to thank, had done everything on my own, and might even blame them for standing in the way of the even better work that I could have done without them!

Fortunately for me, I didn’t have to do everything on my own and consequently I have a lot of people to thank.

The genesis of this project is due to great insight on the part of my two advisors, Professor Martin Schmidt and Professor Vladimir Bulović, as well as from a number of people from the Hewlett-Packard site in Corvallis, OR. I was fortunate to show up in Marty’s office looking for a research project at the right time.

I believe that it is difficult to realize how much you learn from an advisor the same way that it is difficult to realize how much parents teach you, so I would like to thank Marty and Vladimir not only for everything that I know they taught me but also for all the things that I will realize later that I learned from them. I am particularly grateful to Marty as my main advisor for showing a lot of concern for my progress in classes, research and all the milestones that go with working towards a PhD, and helping me build up confidence along the way.

I would also like to thank Professor Francesco Stellacci and Professor Michael Rubner for being on my thesis committee and giving me feedback on the project and the manuscript, Professor Marc Baldo for many useful discussions at the beginning of the project, and Professor Carl Thompson for discussions of the metallization failure.

I am very grateful to Hewlett-Packard and in particular Dr. Sam Angelos and Dr. Tim Weber from the Imaging and Printing Group in Corvallis, Oregon, not only for funding the research, but also for making me feel part of a bigger picture and giving me the occasion to meet a lot of great people through my interactions with HP, and in particular during my internship in the summer 2004. I greatly appreciated learning from Tony Fern, who taught me how to use the modeling software CoventorWare and shared a lot of his insight with me. It has also been a pleasure to interact with Dr. Paul Benning, Dr. Thomas Lindner, Dr. Peter Mardilovich, Dr. Jim Stasiak and Dr. Murali Charapala, and I would like to thank them for their help and support.
Many thanks go to the staff of the Microsystems Technology Laboratories, for their
tireless help and guidance in the use of the microfabrication equipment.

I would also like to thank Prof. Dennis Freeman, Salil Desai and Shih-Chi Chen for help with the microvision system and MMA measurements, Peter Mayer for 3-omega measurements, Libby Shaw from CMSE for help with several surface analyses, and David Neiman and Jay Van Hoff from HP for performing analyses on my samples.

I am indebted to Anne Wasserman for her help in a lot of areas as well as for her support and friendship. Thanks to all the Schmidt Group members, many of which are now close friends, including Gwen and Kent Gerhardt, and to Vladimir’s group for welcoming me as one of them.

I would also like to thank a number of people for making my PhD years very enjoyable including a lot of MTL students and postdocs, Debb and the MTL social committee, many MIT friends both new and imported from France, the MIT Women’s Ice Hockey Club and in particular Coach Reggie Hebert and my co-student-captain Liz Young, the MIT underwater hockey club and in particular Jason LaPenta for creating it.

I would like to thank my family, and especially my parents and grandparents, for supporting me across the oceans and being proud of me without questions.

Finally, I would like to thank my husband Blaise Gassend for more things than can be written on those pages, including making me apply to MIT and supporting me morally and emotionally throughout our PhD experiences.
# Table of contents

**TABLE OF CONTENTS**

- Organic optoelectronic devices fabrication issues ................................................................. 19
- Limitations of ink-jet printing of organic materials ................................................................. 21
- MEMS as patterning tools ........................................................................................................ 22
- Summary: advantages of MEMS for organic optoelectronic fabrication .................................. 22
- Thesis organization .................................................................................................................. 23
- References .............................................................................................................................. 24

**INTRODUCTION**

- Organic optoelectronic devices fabrication issues ................................................................. 19
- Limitations of ink-jet printing of organic materials ................................................................. 21
- MEMS as patterning tools ........................................................................................................ 22
- Summary: advantages of MEMS for organic optoelectronic fabrication .................................. 22
- Thesis organization .................................................................................................................. 23
- References .............................................................................................................................. 24

**MOJET 1: ELECTROSTATICALLY ACTUATED MECHANICAL SHUTTER**

- 2.1 PRINCIPLE OF MOLECULAR JET PRINTING 1 (MOJET 1) .................................................. 25
- 2.2 MOJET 1 PRINthead DESIGN
  - Design constraints and requirements .................................................................................. 26
  - Design implementation and parameters ............................................................................. 26
  - Analytical model of first electrostatic actuator design ......................................................... 28
  - First resonant frequency ....................................................................................................... 38
  - Summary .............................................................................................................................. 38
- 2.3. SIMULATIONS AND NEW ACTUATOR DESIGN
  - Redesign for greater compactness....................................................................................... 43
  - Simulation results for thermal actuators .............................................................................. 44
  - Compact electrostatic actuator design ................................................................................. 45
  - Further possible improvements on actuator design ............................................................. 48
- 2.4. CHARACTERIZATION / TESTING RESULTS
  - Displacement measurements ............................................................................................... 49
  - Frequency measurements ................................................................................................... 50
  - Discussion ............................................................................................................................ 51
  - Printing Results .................................................................................................................. 51
  - Printing speed ..................................................................................................................... 54
  - Summary .............................................................................................................................. 54
- 2.5. DISCUSSION
  - Limitations ........................................................................................................................ 55
  - Improvements and future work .......................................................................................... 57
- 2.6. CONCLUSION
  - References .......................................................................................................................... 58

**MOJET 2: ELECTROTHERMAL MICROSCALE EVAPORATOR**

- 3.1 PRINCIPLE AND MOTIVATION ......................................................................................... 61
  - Principle ............................................................................................................................... 61
  - Advantages over MoJet1 ..................................................................................................... 62
  - Proof of concept experiments ............................................................................................ 62
- 3.2 DESIGN AND SIMULATIONS
  - Design requirements for application .................................................................................. 63
List of Figures

Figure 1-1: Conceptual representation of thermal imaging from reference [8].................. 20
Figure 1-2: Schematic of Organic Vapor Jet Printing apparatus from reference [11]...... 20
Figure 1-3: Left: Nanostencil with integrated shutter from reference [14]. Right: Electrostatically actuated shutter used for direct patterning of metals at the nanoscale [15]............................................................................................................. 22
Figure 2-1 Schematic of the printing principle.............................................................. 25
Figure 2-2. Definition of relevant design parameters..................................................... 27
Figure 2-3. Schematic of zipper curved actuator........................................................... 28
Figure 2-4. Schematic and picture of comb-drive actuator............................................ 29
Figure 2-5. Schematic of folded flexure with displaced structure in blue..................... 29
Figure 2-6. Parameters definition for stiction / vertical pull-in calculations............... 31
Figure 2-7. Parameters definition for displacement calculations................................. 32
Figure 2-8. Parameters definition for side instability calculations................................. 33
Figure 2-9. Schematic of the actuator........................................................................... 34
Figure 2-10 Minimum length to avoid side instability before 40 microns of displacement. ........................................................................................................................................... 35
Figure 2-11 Area $A$ as a function of $n$ for 3 different values of $L$................................. 35
Figure 2-12. Maximum number of fingers according to the stiction criterion, for $g = 2$ μm. ................................................................................................................................................. 36
Figure 2-13. Maximum number of fingers according to the stiction criterion, for $g = 4$ μm. ............................................................................................................................................... 36
Figure 2-14. Maximum number of fingers according to the stiction criterion (in green) and minimum $n$ to achieve the desired displacement (in red), for $g = 2$ μm. There is no possible value of $n$ and $L$ ................................................................. 37
Figure 2-15. Maximum number of fingers according to the stiction criterion (in green) and minimum $n$ to achieve the desired displacement (in red), for $g = 4$ μm. There is a range of possible values for $n$ and $L$. .......................................................................................................................... 37
Figure 2-16. Fabrication process..................................................................................... 39
Figure 2-17. Picture of an empty package (left) and a packaged device (right)............. 42
Figure 2-18. Microscope images of the first kind of actuator. On the right, the device is actuated. ........................................................................................................................................ 42
Figure 2-19. Geometry and temperature distribution in a thermal actuator envisioned for the compact design. Right: Displacement of the two arms is shown as well. .......... 43
Figure 2-20. Displacement of a thermal actuator based on two arms of different lengths. ......................................................................................................................... 44
Figure 2-21. Geometry of the chosen thermal actuator. .............................................. 44
Figure 2-22. Temperature distribution in thermal actuator. Left: In air. Right: In vacuum (no gas conduction)........................................................................................................ 45
Figure 2-23. Temperature distribution along the “arms” in a thermal actuator. Left: In air. Right: In vacuum (no air conduction)........................................................................................................ 45
Figure 2-24. Schematic and SEM picture of the electrostatic actuator presented in reference [11] ............................................................................................................. 46
Figure 2-25. Geometry of the compact electrostatic actuator...................................... 47
Figure 2-26. Simulation of the displacement of the compact electrostatic actuator........ 47
Figure 2-27. SEM pictures of the two electrostatic actuators. The compact design is on
the right ............................................................................................................................. 48
Figure 2-28. Optical microscope images and simulation results of micro-printhead at
different actuation voltages............................................................................................... 49
Figure 2-29. Comparison of measured displacement as a function of actuation voltage
with simulation results. ..................................................................................................... 50
Figure 2-30. Frequency response of a microshutter with the second actuator design. The
resonant frequency is 4.1 kHz........................................................................................... 50
Figure 2-31. SEM picture of the center beam of the second design device with electrode
comb fingers sticking out ................................................................................................. 51
Figure 2-32. Profile of deposited silver pixel on oxidized silicon ................................ 52
Figure 2-33. Fluorescent microscope picture of silver printed pattern............................ 53
Figure 2-34. Optical microscope picture of silver printed pattern .................................. 53
Figure 2-35. Fluorescent microscope images of electroluminescence of OLED array
printed using our printhead and schematic of the layer structure of the OLED array ...... 53
Figure 2-36. Fluorescent microscope images of the aperture, and the backside of the
microshutter seen through the aperture. The green color indicates the present of Alq3
material. ............................................................................................................................ 56
Figure 2-37. WYKO profilometer measurement of microshutter after deposition of
pentacene. The shutter is stuck down to the silicon base layer ...................................... 56
Figure 3-1. Schematic of the printing principle ................................................................. 61
Figure 3-2. Schematic of the cross-section and membrane top view of a MoJet 2
printhead chip.................................................................................................................... 64
Figure 3-3. Plot of thermal time constant (in ms) of a membrane as a function of its width
in μm .................................................................................................................................. 65
Figure 3-4. Plot of maximum aspect ratio to avoid buckling versus temperature .......... 66
Figure 3-5 Schematic of the heater top view with dimensions ......................................... 68
Figure 3-6. Three-dimensional views of the designed chip (left) and membrane area
(center and right). On the right, the membrane is rendered as partially transparent........ 68
Figure 3-7 Temperature distribution on the membrane and heater for a current of 1A.... 69
Figure 3-8. Current density distribution in the heater for a current of 1A......................... 69
Figure 3-9. Schematic of the two types of MoJet 2 printhead chips fabricated................. 70
Figure 3-10. Illustration of the fabrication process ............................................................. 71
Figure 3-11: Microscope images of a microfabricated printhead chip. Left: Top view of
the membrane area. Right: Zoomed view of the pores area ............................................ 71
Figure 3-12: Lift-off issues during fabrication of MoJet2 chips. Some metal deposited in
areas that were supposed to be masked by photoresist .................................................... 72
Figure 3-13: Optical microscope pictures showing 3 locations on a wafer after the back
side oxide etch. The front side oxide near the pores shows different degrees of etching. 73
Figure 3-14. Picture of fabricated chip (back and front) and packaged chip .................. 73
Figure 3-15 Temperature profile of the printhead chip obtained with an infrared
microscope. The picture on the right is a zoom on the membrane region (actuation current
of 0.85A). .......................................................................................................................... 74
Figure 3-16 Temperature as a function of normalized resistance for a Pt thin film heater
(from [5]). ........................................................................................................................ 75
Figure 3-17: Temperature of the printheads with no oxide barrier layer obtained by different measurement techniques, and compared to simulation results. .............................. 76
Figure 3-18: Temperature of the devices with an oxide barrier layer obtained by electrical resistance measurements. ........................................................................................................ 76
Figure 3-19: Test setup (left) and oscilloscope measurement of the input signal (right) for the thermal time constant measurements. ........................................................................ 77
Figure 3-20: Voltage across a resistor in series with the MoJet2 heater.......................... 78
Figure 3-21: Simulation of the temperature of the membrane as a function of time (left) and measurement of the heater resistance as a function of time (right)........... 78
Figure 3-22: Pictures of the printing setup...................................................................... 79
Figure 3-23: Images of the porous area of a MoJet2 chip: (a) Photoluminescent microscope image of pores filled with Alq3 solids after a drop of Alq3 in solvent was deposited on the back of the membrane and (b) back illuminated optical microscope picture of the empty pores after heating and complete evaporation of Alq3. ............... 80
Figure 3-24: Pixel of organic material Alq3 printed with our setup (fluorescent image). 80
Figure 3-25: Comparison of printed Alq3 pixels. (a) Ink-jet printed pixels (with coffee ring effect). (b) Pixels printed using Molecular Jet Printing. ............................................. 82
Figure 4-1: Microscope images of MoJet2 heaters (no oxide barrier layer) after self-heated failure (left) and after anneal for 2 hours in N2 at 500°C (right) ...................... 86
Figure 4-2: SEM pictures of MoJet2 heaters. Left: self-heated failure. Right: annealed. The bottom pictures correspond to the areas defined by the red rectangles in the top pictures. ......................................................................................................................... 87
Figure 4-3: Elemental Auger maps of Pt and Si on the self-heated MoJet2 chip............ 87
Figure 4-4: Sputtered Auger profile of heater chip before failure ................................. 88
Figure 4-5: Sputtered Auger profile of heater in a failed region ................................... 88
Figure 4-6: Microscope images of a MoJet 2 heater with an oxide barrier layer after some degradation due to self-heating (left) and after complete failure (right). ................. 89
Figure 4-7: Scanning electron microscope images of a failed MoJet2 heater with an oxide barrier. ....................................................................................................................... 89
Figure 4-8: Scanning electron microscope images of the pores area of a failed MoJet2 heater with an oxide barrier layer. ........................................................................ 90
Figure 4-9: SEM pictures of Focused Ion Beam cross-sections of a failed MoJet2 heater with an oxide barrier layer. (The Cr layer is added and used as a masking layer for the FIB process.) .................................................................................................................. 90
Figure 4-10: Electrical measurements showing average temperature as a function of power for two samples each of MoJet2 heater type 1 and 2 ........................................ 91
Figure 4-11: Comparison of optical microscope images of failed MoJet2 chips of type 1 and 2. Left: no oxide barrier layer (type 1). Right: with an oxide barrier layer (type 2). 91
Figure 4-12: Geometry of the two resistors on a 1 mm wide membrane (thicknesses not to scale). ...................................................................................................................... 96
Figure 4-13: Temperature distribution on the membrane when heating the outer resistor. ................................................................................................................................. 96
Figure 4-14: Detail of the temperature distribution at the center of the membrane. The solid lines show the position of the outer resistor and the dotted line that of the outer resistor................................................................. 96
Figure 4-15: Layout of the test device. The red contour shows the position of the silicon membrane.

Figure 4-16: Resistance as a function of voltage for the outer resistor of a test device on a chip without a membrane.

Figure 4-17: Electrical characteristics and failure conditions of the inner resistor in the two experiments described in Figure 4-18.

Figure 4-18: Voltage conditions on the inner and outer resistors for the two measurements.

Figure 4-19: Left: Top view SEM of a test device. Right: Cross-section of a test device without membrane (top) and with a membrane (bottom).

Figure 4-20: Temperature distribution on the top surface of a device without a membrane.

Figure 4-21: Temperature distribution on the top surface of a device with a membrane.

Figure 4-22: Temperature as a function of current through a test device resistor for devices on a membrane (blue points) and without a membrane (green and black points).

Figure 4-23: Scanning Electron Microscope images of the failure spot on a device with a membrane.

Figure 4-24: Elemental maps of test device failure spot obtained by Auger Electron Spectroscopy.

Figure 4-25: SEM images of the failure spot for a device without a membrane.

Figure 4-26: SEM images of the failure spot for a device on a membrane for different step voltages.

Figure 4-27: Comparison of the failure spot for resistors failed by increasing the voltage until failure (left) and by applying a voltage step of 40V (middle and right).

Figure 4-28: Measurements of time to failure for test devices subjected to step voltages of 40 to 60V.

Figure 4-29: Plots of the time to failure as a function of step voltage (Left) and the inverse of the failure time as a function of the voltage squared (Right).

Figure 4-30: Temperature and current density at failure as a function of step voltage.

Figure 4-31: Temperature versus voltage for test devices with 10 nm and 50 nm Ta adhesion layers.

Figure 4-32: SEM pictures of metal lines after an 80V voltage step with 10 and 50nm Ta thicknesses.

Figure 4-33: SEM pictures of metal lines after a voltage ramp until failure for 10 and 50nm Ta layers.

Figure 4-34: Resistance of the outer resistor as a function of the chuck temperature for different films (10 and 50 nm Ta adhesion layer, anneal in air and in nitrogen).

Figure 4-35: Normalized resistance as a function of the chuck temperature for different films.

Figure 4-36: Temperature versus voltage for test devices with 10 nm and 50 nm Ta adhesion layers with and without a post-fabrication anneal in nitrogen.

Figure 4-37: Images of resistors with 10 nm (top) and 50 nm (bottom) Ta layer, after anneal in nitrogen ambient and self-heated failure in air.

Figure 4-38: SEMs of failed devices that hadn’t been annealed before testing.
Figure 4-39: SEMs of failed devices that had been annealed before testing in air and in nitrogen. .......................................................................................................................... 114
Figure 4-40: Optical microscope picture of an alumina capped sample. Left: picture of the chip showing the round area where alumina is deposited. Right: picture of the membrane area after failure of the outer resistor................................................................. 115
Figure 4-41: Resistance versus current characteristics for test devices with and without membranes and with and without an alumina capping layer.................................................. 116
Figure 4-42: SEM pictures of failed alumina capped samples. Left: no membrane, right: membrane........................................................................................................................ 116
Figure 4-43: Pictures of permanent deformations of MoJet2 membranes after failure. Left: SEM picture showing wrinkles on the silicon membrane and deformation of the central area comporting the pores. Center: Pictures of the front side after failure (top), and back side before (middle) and after (bottom) failure of a MoJet2 device. Right: Front side (top) and back side (bottom) pictures of a MoJet2 membrane after failure............... 119
Figure 4-44: Comparison of average temperature at failure for MoJet2 and test devices ......................................................................................................................................... 120
Figure 4-45: SEM of test device (left) and MoJet 2 (right) resistor after failure (no initial anneal)................................................................................................................... 120
List of Tables

Table 1. A comparison of solution processed and thermally-evaporated devices demonstrating the clear need for a printing technique capable of patterning devices by an evaporative technique. Despite their superior characteristics in devices, thermally evaporated materials must be patterned by shadow masks.............................................. 21
Table 2: Comparison of thermal and electrostatic actuators envisioned for the compact design. .......................................................................................................................................... 48
Table 3: Advantages of Molecular Jet Printing ........................................................................................................ 82
Table 4: Effect of anneal on the outer resistor of the test device (average over 3 chips). 99
Table 5: Temperature Coefficient of Resistance for Ta/Pt films annealed in air or nitrogen ........................................................................................................................................ 112
Table 6: Comparison of failure conditions for MoJet2 and test devices. ......................... 119
Suppose we use the small machines as adjustable masks for controlling the evaporation process. If I could open and close these masks mechanically, and if I had a source of some sort of atoms behind, then I could evaporate those atoms through the holes. Then I could change the hole by changing the voltages - in order to change the mask and put a new one on for the next layer.

Richard Feynman,
Infinitesimal Machinery, 1983
1. Introduction

This thesis investigates the use of MicroElectroMechanical Systems (MEMS) to provide new ways of patterning organic materials deposited by an evaporative process. We will present the design, fabrication, modeling and characterization of several micromachined printheads developed to expand the possibilities of printing of organic optoelectronics. In this chapter, we will first present the existing fabrication techniques for organic optoelectronics and their limitations. We will then show examples from the literature of MEMS used as patterning tools and finally show how MEMS printheads can be used to overcome the limitations of the existing fabrication techniques.

Organic optoelectronic devices fabrication issues

Organic optoelectronic devices can be fabricated on a variety of substrates due to their low-temperature processing, and in particular on flexible and very low cost substrates. Therefore, they are of interest in a number of applications where those advantages over conventional silicon devices overcome the need for performance. Possible applications include flexible displays and ubiquitous electronics, i.e. low performance circuits incorporated within everyday items, such as smart identification tags on consumer goods, driving circuits for cheap flexible video screens, or even the next generation of mobile computing devices.

However, it still remains a challenge to develop suitable fabrication techniques to pattern organic thin films on low-cost, large-area substrates [1].

Conventional photolithographic techniques cannot directly be used for the patterning of organic thin films, because the solvents and oxygen plasma used to remove photoresist also attack the organic thin film [2]. Therefore, alternate patterning techniques have to be developed.

Small molecular weight organic materials are typically deposited by vacuum thermal evaporation and patterned through shadow masks. However, shadow masking is not scalable to very large area substrates, because the flatness requirements are difficult to achieve for thin shadow masks on large areas [3].

Polymeric materials can be deposited by ink-jet printing: an inkjet printhead is used to
print drops of solvated polymers, which become pixels of polymer thin film once the solvent evaporates. Cost effective components can be realized on a large scale, and inkjet printing is therefore a promising fabrication technique for industry [4].

Microcontact printing, stamping, screen printing and similar techniques can also be used to pattern organic layers [5, 6, 7].

In thermal imaging, a laser is used to transfer pixels of a thin solid layer from a donor film onto a substrate, as shown on figure. An organic conductor was printed via thermal imaging and patterned as source and drain electrodes for a TFT backplane containing 5000 transistors with 20 micron channels [8].

![Figure 1-1: Conceptual representation of thermal imaging from reference [8].](image)

Another alternative method for patterning small molecular weight materials is organic vapor jet printing (OVJP) [9, 10]. An inert carrier gas stream flows into a hot source container where it picks up the molecular organic species. The molecules enter a mixing chamber, and subsequently pass through a nozzle to form a highly directional jet. The organic molecules selectively physisorb onto a cooled substrate, which can be translated transverse to the nozzle. Printing resolutions of about 10 μm can be achieved, and OLEDs printed with this technique are comparable to vacuum-deposited OLEDs [11].

![Figure 1-2: Schematic of Organic Vapor Jet Printing apparatus from reference [11].](image)
Limitations of ink-jet printing of organic materials

Ink-jet printing of an organic material limits the achievable film morphology and is difficult to apply to the fabrication of multilayer films, since the solvent used to deposit one layer can redissolve the previously deposited layers. This has serious practical implications since optoelectronic devices need well defined heterostructure contacts between specified materials of specified thickness.

It also limits the range of achievable materials. Small molecular weight organic materials can exhibit higher transistor mobilities and OLED efficiencies than polymers but cannot be inkjet printed.

<table>
<thead>
<tr>
<th>Thin film morphology</th>
<th>Thermal evaporation</th>
<th>Solution processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strained layers</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Purity</td>
<td>High</td>
<td>Depends on solvent</td>
</tr>
<tr>
<td>Multilayer devices</td>
<td>Yes</td>
<td>Bilayer possible</td>
</tr>
<tr>
<td>Molecular doping</td>
<td>Yes</td>
<td>Dopants phase separate</td>
</tr>
<tr>
<td>Max. LED efficiency</td>
<td>0.87 (photons/electron)</td>
<td>0.2 (photons/electron)</td>
</tr>
<tr>
<td>TFT mobility</td>
<td>&gt;1 cm²/Vs</td>
<td>&lt; 0.1 cm²/Vs</td>
</tr>
<tr>
<td>Inkjet</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 1. A comparison of solution processed and thermally-evaporated devices demonstrating the clear need for a printing technique capable of patterning devices by an evaporative technique. Despite their superior characteristics in devices, thermally evaporated materials must be patterned by shadow masks.

Overall, the restrictions imposed by ink-jet printing limit the materials that can be used and the structures that can be obtained, and therefore the performance of achievable devices.
MEMS as patterning tools

Microsystems for the patterning of vapor deposited materials have previously been fabricated. Microstenciling [12] uses micromachined shadow masks for patterning on unconventional substrates at the microscale. Nanoscale shadow masks have previously been integrated with a scanning probe to allow parallel nanodevice fabrication [13]. Such shadow masks can also be integrated with a microactuator and provide active shuttering. Electrostatically actuated shutters were previously fabricated [14] and used for direct patterning of metals at the nanoscale [15] (See Figure 1-3).

![Figure 1-3: Left: Nanostencil with integrated shutter from reference [14]. Right: Electrostatically actuated shutter used for direct patterning of metals at the nanoscale [15].](image)

Summary: advantages of MEMS for organic optoelectronic fabrication

As discussed above, a fabrication technique combining the flexibility of printing with the high performance of evaporation would be highly beneficial to organic optoelectronics. This can be realized using a MEMS microshutter as an active shadow mask during evaporation of small molecular organics, similarly to techniques described above. Compared to a traditional macro shuttering technique used in conjunction with a silicon stencil, the use of integrated microshutters could allow high-throughput printing of arbitrary patterns, potentially on large areas, by combining individual nozzles into an array of individually addressable nozzles. This is particularly valuable in the domain of organic optoelectronic devices, since it would allow capturing the low-cost promise of organic materials by providing a way of printing them on a multitude of substrates.

Moreover, using even more integration, MEMS can be used to make the printing even
more compact and economical by allowing microscale evaporation of the materials.

**Thesis organization**

In this thesis, we will present two kinds of micromachined printheads that were designed and fabricated for applications to the evaporative printing of organic materials, also called Molecular Jet Printing (or MoJet).

The first chapter is devoted to MoJet I, the first printhead based on an electrostatically actuated microshutter. The second chapter describes MoJet II, which is basically a microscale evaporator. Both chapters discuss the specific design constraints, design, fabrication, modeling, results and limitations of the printheads.

Finally, in the last chapter, a more detailed study of the temperature limitation of the second kind of printheads, also applicable to other MEMS devices using a thin film microheater on a silicon membrane, is presented.
References

2. MoJet 1: Electrostatically actuated mechanical shutter

2.1 Principle of Molecular Jet Printing 1 (MoJet 1)

The first evaporative printing technique for organic materials presented in this thesis, called MoJet I, is based on an electrostatically actuated microshutter.

The principle of the printing method is showed in Figure 2-1. The substrate on which material is to be deposited is placed in a vacuum chamber. Organic material is sent to the substrate by vacuum sublimation, using a K-cell to heat up a solid material source. A MoJet I printhead is placed in front of the substrate. The micromachined printhead consists of an aperture in a silicon membrane (dark area on Fig. 1.b and 1.c) over which an actuated free-standing microshutter is suspended (see Fig. 1.b, 1.c and 1.e).

Before reaching the substrate, the material travels through the aperture in the printhead. When the microshutter is not actuated (Fig. 1.a and 1.b), the material deposits on the substrate. When a voltage is applied across the electrostatic actuator (Fig. 1.d and 1.e), the microshutter blocks the deposition. The substrate is attached to an x-y-z manipulator to allow arbitrary patterns to be printed.

Figure 2-1  Schematic of the printing principle.
2.2 MoJet 1 printhead design

Design constraints and requirements

Contrary to similar devices used to pattern materials down to the nanoscale, our applications do not require a very high printing resolution. We chose a pixel size of around 25 micrometers, which would correspond to an 800 dpi monochrome display. This larger pixel size relaxes many of the constraints associated with having the substrate in contact with the device, and with having a very thin layer in which the aperture is defined. On the other hand, this requires a larger displacement of the microshutter to obstruct the aperture, and therefore puts more constraints on the actuator.

The upper surface of the MEMS printhead must be close to the deposition substrate to minimize the broadening of printed patterns. This requires particular attention in the design of the packaging, as wire-bonded contacts on the top surface would not allow the substrate-to-printhead distance to be less than about 500 micrometers. It also requires a certain robustness of the actuator, since the substrate is going to move very close to the top surface of the actuator. As we will see in the next part, the first actuators we designed were not robust enough and were damaged very easily.

Some of the design parameters influence how much material is wasted and how fast the printing takes place. The thicker the membrane, the more deposition occurs inside the aperture, therefore the membrane must be as thin as possible to maximize the material use efficiency as well as the printing speed, and increase the lifetime of the device with respect to clogging of the aperture. However, since the aperture must be defining the deposition pattern, the solid angle of material coming through the large back side hole defining the membrane must be larger than the solid angle defined by the aperture. Therefore, the depth to width ratio of the backside hole must be smaller than the same ratio for the aperture.

Design implementation and parameters

We chose to implement our printheads on silicon-on-insulator (SOI) wafers. The actuator and shutter are defined in the silicon device layer, and released by removing some of the buried oxide (BOX) layer. The aperture and membrane are defined in the
In this process, the membrane is defined by Deep Reactive Ion Etching (DRIE) without an etch stop layer. Due to the large etch rate non-uniformities across the wafer, it is difficult to obtain a very thin membrane. We chose to limit the membrane thickness to a minimum of 50 micrometers to get acceptable process robustness. We then chose the width of the membrane so that it would be large enough for the depth to width ratio of the backside hole to be smaller than the same ratio for the aperture as discussed in the previous part.

The vertical gap below the actuator and shutter, defined by the buried oxide thickness of the SOI wafer, should be as large as possible to reduce stiction problems, in which the free-standing shutter sticks to the underlying silicon base layer after the release. We used SOI wafers with the thickest BOX layer that was commercially available, which was 3 micrometers thick.

The features in the silicon device layer are defined by DRIE, and we limited the minimum feature to 3 microns to limit the variability in the dimension due to the process, since it affects the variability in values such as the required actuation voltage. We also limited the silicon device layer to about 10 microns thick, so that the walls of features etched through this layer would have relatively straight walls. The SOI wafers we used had a silicon device layer of 11 microns.

Since the aperture is a 25 micrometer square in our design, we designed the shutter to be 45 micrometers wide, so that it covers the aperture with a 10 micrometers overlap on each side. This corrects for the fact that the 3 micrometers gap could allow material coming through the membrane aperture at an angle to pass through the shutter during the
deposition, taking into account possible misalignment between the aperture and the shutter.

**Analytical model of first electrostatic actuator design**

**Selection of actuator type**

We considered several classical electrostatic actuators design to use in the MoJet 1 printheads. We first considered a zipper curved actuator such as the one shown in Figure 2-3 (see reference [1]). We didn’t use this design because the actuation voltage and therefore the position of the microshutter for a given voltage are very dependant on the initial gap, i.e. the insulating layer thickness. This layer needs to be thin to limit the required actuation voltage.

![Figure 2-3. Schematic of zipper curved actuator](image)

We then considered the comb-drive electrostatic actuator with folded flexure presented in reference [2]. Figure 2-4 shows a schematic of a comb-drive actuator.

A mobile electrode is linked to a compliant structure (spring). A voltage difference applied between the fixed and mobile electrode creates an electrostatic attraction between them, and the mobile electrode moves towards the fixed electrode.
Figure 2-4. Schematic and picture of comb-drive actuator

Figure 2-5 is a schematic of the compliant structure in the folded flexure design. L is the length of one beam segment and b the beam width. The black squares represent the parts of the structure that are fixed to the substrate. The blue lines on the right part of the figure show the displacement of the structure with the beams bending and each of the two trusses moving as a rigid structure.

For small deflections of the folded flexure, the spring constants in the $x$, $y$ and $z$ directions, $k_x$, $k_y$ and $k_z$ are given by the following expressions (from reference [2]):
\[
    k_x = \frac{2Eb}{L}, \quad k_y = \frac{2Eb^2h}{L^3} \quad \text{and} \quad k_z = \frac{2Eb^3}{L^3}
\]
where \( E \) is the Young modulus of silicon and \( b \) is the beam width and \( L \) the length of one beam segment.

The stiffness ratio \( \frac{k_x}{k_y} = \left( \frac{L}{b} \right)^2 \) of the spring constants in the x and y directions can be very high, \( 1.78 \times 10^4 \) for a beam of length 400 \( \mu \text{m} \) and width 3 \( \mu \text{m} \).

**Design requirements**

We have chosen the aperture to be 25 by 25 microns, and the shutter to be 45 microns wide, so that there is a 10 microns overlap allowing for process variations. For the same reason, we want the shutter to displace by 35 microns, and we will design for a maximum displacement of 40 microns.

For practical issues during the use of the printhead, we limit ourselves to a maximum voltage of 100 to 150V.

Therefore our first requirement is that the mobile electrode must displace by 40 microns with less than 150V applied voltage.

We also want the first resonant frequency of the structure to be of the order of several kHz so that it doesn’t limit the printing speed.

Another requirement is that we want to avoid stiction of the free-standing parts to the substrate both during and after fabrication.

**Stiction considerations**

Before we derive expressions for the displacement as a function of voltage and the different geometry parameters, let’s discuss a no-stiction criterion.

It is possible to use models to predict stiction in MEMS (See references [3] and [4]). However, these models are very involved, and depend on a number of factors such as humidity, temperature, surface roughness. We use a simple criterion based on the pull-in voltage between the two surfaces in question.
The pull-in voltage $V_{pi}$ for the mobile parallel plate depicted in Figure 2-6 is the voltage difference between the two plates at which the equilibrium of the top plate becomes unstable [5].

$$V_{pi} = \frac{8k_z g^3}{27\varepsilon_0 A}$$

where $A$ is the area of the plate, $g$ is the gap between the plate and a similar fixed plate and $k_z$ is the spring constant.

Stiction, similarly to pull-in, is favored by large surface areas (large $A$), small gaps (small $g$) and by weak restoring forces (small $k_z$). Our design criteria to limit stiction problems is to impose that the pull-in voltage between the free-standing part and the substrate be higher than 10-20V.

Vertical pull-in itself is not an issue in our case: we can ensure that the voltage difference between the substrate and the free-standing part (the mobile electrode and shutter) stays smaller than the pull-in voltage by grounding them both and applying voltage on the fixed electrode.

In our design, $k_z = \frac{2Eh^3b^3}{L^3}$. The area $A$ of the suspended part increases with the number of comb-fingers $n$.

For a given $L$, the non-stiction criterion corresponds to imposing a limit on the number of fingers $n$. 
**Displacement calculations**

We consider a mobile electrode with \( n \) fingers. Figure 2-7 defines some of the parameters useful for the displacement calculations. \( h \) is the device thickness, \( y \) is the comb displacement, \( y_0 \) is the initial comb finger overlap and \( d \) is the gap spacing between the fingers.

![Diagram of a mobile electrode with parameters](image)

Figure 2-7. Parameters definition for displacement calculations

The following analysis is from reference [2], and 3D effects such as fringing fields or the ground-plane levitation effect are neglected.

The capacitance between the stator (fixed electrode) and rotor (mobile electrode) is:

\[
C = \frac{2n\varepsilon_0 h(y + y_0)}{d}
\]

where \( \varepsilon_0 \) is the dielectric constant in air.

When a voltage \( V \) is applied between the stator and the rotor, the lateral electrostatic force in the \( y \) direction is:

\[
F_{el} = \frac{1}{2} \frac{\partial C}{\partial y} V^2 = \frac{n\varepsilon_0 h}{d} V^2
\]

At equilibrium, \( F_{el} = k_y y \) where \( k_y \) is the spring constant of the folded flexure in the \( y \) direction. The lateral deflection is

\[
y = \frac{F_{el}}{k_y} = \frac{n\varepsilon_0 h}{k_y d} V^2
\]
For small deflections of the folded flexure:

\[ k_y = 2Eb^3h/L^3 \]

where \( E \) is the Young modulus of silicon and \( b \) is the beam width and \( L \) the length of one beam segment.

The lateral deflection is therefore

\[ y = \frac{n\varepsilon_0 h}{k_y d} V^2 = \frac{n\varepsilon_0 L^3}{2E b^3 d} V^2 \]

for small deflections, ie the displacement is proportional to \( nL^3 \).

This expression is valid as long as pull-in instability in the \( y \) direction and side instability (in the \( x \) direction) don’t happen.

**Side instability calculations**

Figure 2-8 shows the parameters relevant for side instability calculations.

\[ y + y_0 \]

\[ d - x \quad d + x \]

\[ y \]

\[ x \]

Figure 2-8. Parameters definition for side instability calculations

The electrostatic force in the axial direction is

\[ \frac{n\varepsilon_0 h(y + y_0)}{2(d - x)^2} V^2 - \frac{n\varepsilon_0 h(y + y_0)}{2(d + x)^2} V^2 \]

When the derivative of that force with respect to \( x \) is larger than the restoring spring constant in the \( x \)-direction, \( k_x \), there is a side-instability of the comb-drive, which means that the mobile electrode will move to the right or the left in the \( xy \) plane and come into contact with the fixed electrode.

At the onset of side instability, the voltage is \( V_{SI} \) and the displacement is \( y_{SI} \). They are defined by the following relations:

\[
\frac{2n\varepsilon_0 h(y_{SI} + y_0)}{d^3} V_{SI}^2 = k_x \text{ ie } V_{SI}^2 = \frac{d^2 k_y}{2\varepsilon_0 hn} \left( \sqrt{\frac{k_x + y_0^2}{k_y d^2} - \frac{y_0}{d}} \right) \text{ and } y_{SI} = d \sqrt{\frac{k_x}{2k_y} - \frac{y_0}{2}}.
\]
To avoid side instability, we must have $y_{SL} \leq y_{max}$, where $y_{max}$ is the desired maximum displacement (40 microns for our design).

For the folded flexure $k_s = 2Eb/h/L$. Avoiding side instability imposes that $L$ be larger than a minimum value.

**Selecting geometry parameters**

![Figure 2-9. Schematic of the actuator](image)

As discussed earlier, the minimum feature size was limited to 3 microns to increase the process robustness to variations. The width of the beams in the folded flexure, the comb fingers width and the lateral distance between the fingers therefore chosen to be 3 micrometers, to get the maximum displacement out of the actuator.

All the features are 11 micrometers high, which was chosen as the silicon device layer thickness. The vertical gap is 3 microns.

In terms of parameters used in the analysis, $b=3 \mu m$, $d=3 \mu m$, $g=3 \mu m$, $h=11 \mu m$.

We can now choose the parameters $L$ and $n$.

Figure 2-11 shows how to select the minimum length $L$ to avoid side instability (for a maximum voltage of 100V).

Choosing the geometry except for $L$ and $n$ allows to express the area $A$ as a function of $n$ and $L$, as shown on Figure 2-11. Using this relation, we can find the maximum $n$ as a function of $L$ which verifies the non-stiction criterion. This is shown on Figure 2-12 and Figure 2-13 for 2 different values of $g$ (2 and 4 $\mu m$).

As shown on Figure 2-14, the criteria to avoid stiction and side instability might be
incompatible for low values of g. For \( g = 4 \, \mu m \), however, it is possible to verify the two criteria for some values of \( L \) and \( n \) (see Figure 2-15).

Finally, we can express \( n \) as a value of \( L \) such that the displacement at 100V is 40 microns (red curve on Figure 2-15). The points above the red curve and below the green curve correspond to values \((L, n)\) that meet all of our requirements.

To reduce \( L \) and \( n \), ie the size of the actuator, we allowed a maximum voltage of 150V. We also took into account possible variations in the dimensions due to the process: +/- 0.5 \( \mu m \) for the 3 \( \mu m \) dimensions, and +/- 1 \( \mu m \) for the other dimensions.

![Figure 2-10 Minimum length to avoid side instability before 40 microns of displacement.](image)

![Figure 2-11 Area \( A \) as a function of \( n \) for 3 different values of \( L \).](image)
Figure 2-12. Maximum number of fingers according to the stiction criterion, for $g = 2 \, \mu m$. 

Figure 2-13. Maximum number of fingers according to the stiction criterion, for $g = 4 \, \mu m$. 

36
Figure 2-14. Maximum number of fingers according to the stiction criterion (in green) and minimum $n$ to achieve the desired displacement (in red), for $g = 2$ $\mu$m. There is no possible value of $n$ and $L$.

Figure 2-15. Maximum number of fingers according to the stiction criterion (in green) and minimum $n$ to achieve the desired displacement (in red), for $g = 4$ $\mu$m. There is a range of possible values for $n$ and $L$. 
First resonant frequency

We can estimate the resonant frequency of the device analytically by calculating its spring constant $k_y$ and estimating its mass $m$. The resonant frequency is then

$$f = \frac{1}{2\pi} \sqrt{\frac{k_y}{m}}.$$  

We find a value of about 6 kHz, which meets our requirements.

Summary

We identified an electrostatic actuator geometry suitable for our requirements and calculated the required geometry parameters.

The desired displacement can be achieved under less than 150V for 480 micrometers long beams and a rotor electrode with 50 fingers.

Mechanical stops limit the allowed displacement to avoid contact between the two comb electrodes.

In the next part, we will describe the fabrication of printheads using this actuator geometry.

2.2. Fabrication and packaging

Fabrication Process

The fabrication starts from an SOI wafer with an 11 μm thick SOI layer and a 3 μm thick buried oxide. The process uses 3 masks.

One of the issues that could create problems due to process variations in the fabrication process is the alignment of the aperture and the microshutter. If they were misaligned, this would affect the displacement of the shutter needed to obstruct the aperture, and therefore the actuation voltage. Therefore we designed the fabrication process so that the aperture is self-aligned to the actuator layer. We etch the aperture through the actuator layer and through the rest of the membrane at the same time, and use a nested mask to etch the features in the SOI layer.

The membrane is defined by DRIE without an etch stop. The front to back alignment doesn’t require a high precision since the back side features are very large compared to the apertures (600 and 25 micrometers respectively) and their positions can therefore be
moved by several tens of micrometers without affecting the performance of the printhead. The fabrication process is depicted in Figure 2-16.

Figure 2-16. Fabrication process

First, a layer of 500 nm of silicon dioxide is thermally grown. Photolithography and wet etch in buffered oxide etch (BOE) define a nested mask for the device layer (step 2). A second photolithography step on the back side using a thick photoresist (AZ 4620P) then defines the back side holes etched by Deep Reactive Ion Etching in the silicon base layer (step 3). The last photolithography step defines self-aligned apertures on the front that are etched through the device, oxide and base layers by DRIE and dry oxide etch (step 4). The photoresist is then stripped and the oxide mask used to pattern the device layer by DRIE (step 5). The wafer is subsequently covered with thin photoresist and diced, then cleaned in an oxygen plasma. Finally, a timed etch is performed on the oxide buried layer in hydrofluoric acid (HF) to release the structure, followed by a cleaning step in isopropanol (step 6).

Fabrication Results

Although we tried to account for stiction in our analysis when designing the actuator, we still encountered stiction problems during the wet release and subsequent drying. On
most of the devices, the shutter was collapsed onto the substrate after fabrication. In some instances, it was possible, using a microprobe, to release the suspended part, and the shutter and actuator would function normally after drying and not exhibit stiction, at least for a certain time. But this was possible only on a limited number of dies, and it wasn’t a very satisfying process due to the low yield and necessity for a manual step.

To overcome these problems, we replaced the wet HF etch step by a vapor HF etch: we placed the chips face down above a 49% solution of HF. This etch was less uniform than the wet etch, and the etching time was more difficult to predict, but the yield increased to more than 50% compared to about 10% of successfully released devices for wet etching. It would be possible to further increase the yield of the release step by adjusting the temperature difference between the substrate and the HF/H₂O liquid source of vapor to control vapor condensation [6], or by using techniques such as critical point drying or freeze sublimation [7] or low-surface-energy coatings (see Discussion).

We also encountered several problems related to the etching of the suspended structure and mobile electrode due Deep Reactive Ion Etching uniformities.

First, during DRIE, the thin 3 micrometers wide beams of the folded flexure etched faster than the 3 micrometer wide electrode comb fingers because they were surrounded by more empty space. This is due to the uniformity effect called microloading: features in low pattern density areas etch faster than features in high pattern density areas [8]. Consequently, the beams were sometimes underetched, due to footing effects, before etching of the electrode comb fingers were completely etched [9].

Another problem, on the first set of masks, was that one of the suspended beams of the folded flexure was too close (3 micrometers) to the surrounding silicon, and tended to stick to it once released. We designed a new mask to remove this problem, but the underetch needed to release the mobile electrode and microshutter was larger in that design, which resulted in the fixed electrode being completely undercut as well. Since its pull-in voltage was about 100V, we were not able to observe the full range of motion of the comb-drive actuator, as the “fixed” electrode would move toward the substrate.

Finally, probably because of the large etched area around the flexure beams, they tended to break very easily when something came in contact with the surface at an angle. The second type of electrostatic actuator that will be presented later was much more
robust than the first one both during fabrication and afterwards. Whereas the suspended structure tended to break whenever something touched the surface on the first design devices, the second design devices presented a very high yield of fabrication, and had a much longer lifetime once fabricated.

Packaging

For our MEMS printheads, the only requirements on packaging were to be able to make electrical contact to the electrostatic actuator, and to be able to position the chip in a vacuum chamber, close to a printing substrate. The electrical contacts are subjected to high voltages of the order of 100V but very low current (only potential leakage currents).

As discussed previously, standard packaging solutions for electrical contacts couldn’t be used for this device, because wire-bonds would impose a minimum distance of about 500 micrometers between the chip top surface and the printing substrate, whereas the distance we used when printing was about 100 microns. One solution to this problem would be to make electrical contacts to the backside of the chip, so that the printing substrate can be placed arbitrary close to the microshutter. This can be achieved using Through-Wafer Vias [10, 11]. However, this would complicate the fabrication process.

We used a conductive tape, 3M 9703 Electrically Conductive Tape, covered with aluminum foil to add electrical contact in the xy plane, to make electrical contact to the two contact pads on the chip. This allows for low-profile electrical contacts.

The chips were placed in a Kyocera ceramic package in which a custom aperture was added to allow the evaporated material to reach the back of the chip (See Figure 2-17). We also used the z-conductive tape to contact the backside of the chip to an underlying electrode. This was also sufficient to fix the chip to the package.
Figure 2-17. Picture of an empty package (left) and a packaged device (right).

**Summary**

We were able to fabricate printhead chips based on the first design described in this section and to actuate the microshutters (see Figure 2-18).

However, stiction problems were limiting the fabrication yield and interfering with the actuation as well. Detailed characterization of those devices was difficult, and since we designed a second kind of actuator, we characterized only those second printheads which were more robust.

Figure 2-18. Microscope images of the first kind of actuator. On the right, the device is actuated.
2.3. Simulations and new actuator design

Redesign for greater compactness

An important limitation of this first design is the large area taken up by the actuator. Since an array of microshutters would be necessary for practical implementation of the printer, it would be beneficial to increase the density of nozzles per area on the chip, i.e. to decrease the area taken up by one microshutter.

We explored alternate designs for the actuator that could lead to more compact designs. A category of actuators that can lead to compact actuators and large strokes is thermal actuators (see reference [12]).

Thermal actuators use resistive (Joule) heating to generate thermal expansion and movement. A typical actuator consists of two beams or “arms” joined at one end and each anchored at the other end (see Figure 2-19). When current is passed through the actuator from anchor-to-anchor, the current density is larger in the narrower "hot" arm and causes it to heat and expand in length more than the "cold" arm, causing the tip of the actuator to move.

![Figure 2-19. Geometry and temperature distribution in a thermal actuator envisioned for the compact design. Right: Displacement of the two arms is shown as well.](image)

Thermal actuators can also be based on two beams of same width but different length [13, 14]; Joule heating also results in different expansion of the two arms in that case (See Figure 2-20).
Simulation results for thermal actuators

We simulated the performance of several thermal actuators using the simulation software CoventorWare. For the geometry shown on Figure 2-21, the overall dimensions of the actuator (without anchors / contact pads) are 50 $\mu$m by 400 $\mu$m. This actuator achieves a displacement of 10 $\mu$m at 5 V, for a power consumption of 50 mW and a maximum temperature in the actuator of 650 °C. The mechanical resonant frequency of the actuator is 25 kHz, and the cooling time is on the order of 5 milliseconds.

However, there is an inherent limitation in using a thermal actuator for our application. Since we will be using the chip in a vacuum chamber, the thermal conductivity of the surroundings of the actuator will be smaller than in air. This changes the temperature
distribution on the cold arm and decreases the temperature difference between the two arms (see Figure 2-22 and Figure 2-23). To get the same displacement in vacuum than in air, we need to get to much higher and possibly physically unreachable temperatures. Also, since we are using a thermal source to evaporate our materials, the ambient temperature will be higher than room temperature, and we will need to reach higher temperatures in the silicon to get the same actuator displacement.

![Temperature distribution in thermal actuator. Left: In air. Right: In vacuum (no gas conduction).](image)

**Figure 2-22.** Temperature distribution in thermal actuator. Left: In air. Right: In vacuum (no gas conduction).

![Temperature distribution along the “arms” in a thermal actuator. Left: In air. Right: In vacuum (no air conduction).](image)

**Figure 2-23.** Temperature distribution along the “arms” in a thermal actuator. Left: In air. Right: In vacuum (no air conduction).

**Compact electrostatic actuator design**

We also investigated electrostatic actuators inspired by the design presented in
reference [15], in which a comb-drive actuator is attached directly to a cantilever beam (See Figure 2-24). These actuators were used in an array with a 500 microns period.

Figure 2-24. Schematic and SEM picture of the electrostatic actuator presented in reference [15].

The actuators presented in this paper have a beam length of 2.9 mm and achieve a displacement of 50 microns at 24V.

We studied actuators with much shorter cantilever beams (around 400 micrometers). When the beam deflects, the fingers of the mobile electrode are rotated with respect to the fixed electrode. For long beams, the angle of rotation is small, but for shorter lengths, the angle can be large enough that the tips of the mobile fingers move by more than the distance between two fingers and get in contact with the fixed finger before the range of motion has been reached.

To overcome this problem, we designed the electrodes to have curved fingers instead of straight ones. The radius of the fingers is equal to the beam length. The shorter distance between the fixed and curved fingers stays about the same during the deflection of the beam.

For the geometry shown on Figure 2-25, the overall dimensions of the actuator (without anchors / contact pads) are 100 μm by 400 μm. The beam is 3 microns wide. This actuator achieves a displacement of 25 μm at 100 V. The mechanical resonant frequency of the actuator is 5 kHz.
Table 2 summarizes advantages and limitations of the thermal actuator presented in Figure 2-21 and the electrostatic actuator shown on Figure 2-25.

The thermal actuator is more prone to stiction because of the large area of the cold arm. It also consumes more electrical power, and has a slower response time. Most importantly, it presents thermal management in a reduced pressure environment, as discussed in the previous section.

The electrostatic actuator occupies a slightly larger area, and need a higher actuation voltage. Its displacement and resonant frequency are quite sensitive to variations in the beam width. Also, one of the limitations compared to the thermal actuator, which will be discussed in section 2.5, is that it doesn’t have a self-cleaning feature.
<table>
<thead>
<tr>
<th>Thermal actuator</th>
<th>Electrostatic actuator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Higher power consumption</td>
<td>High voltage</td>
</tr>
<tr>
<td>Temperature management problem</td>
<td>Sensitive to beam width</td>
</tr>
<tr>
<td>Smaller displacement for same length (limited by stiction)</td>
<td>Larger area used (without contacts)</td>
</tr>
<tr>
<td>Long thermal time</td>
<td>Might need to provide heating to avoid material accumulating on back side of shutter during deposition.</td>
</tr>
</tbody>
</table>

Table 2: Comparison of thermal and electrostatic actuators envisioned for the compact design.

As can be seen on Figure 2-27, the compact electrostatic actuator is much smaller than the initial actuator. The area is reduced by about a factor of 5.

![SEM pictures of the two electrostatic actuators. The compact design is on the right](image)

**Figure 2-27. SEM pictures of the two electrostatic actuators. The compact design is on the right**

**Further possible improvements on actuator design**

The actuation voltage could be lowered by decreasing the thickness of the beam (3 micrometers in our design), decreasing the gap between electrode combs fingers, increasing the number of comb fingers or increasing the length of the beam. Changing those parameters might however impact negatively the device robustness, its resistance to stiction during fabrication or operation, and the compactness of the design.
2.4. Characterization / Testing Results

In the following part, we present characterization only for the compact design. As was mentioned earlier, the first design wasn’t very robust and testing it was difficult. The printing experiments were done with both kinds of actuators.

Displacement measurements

We measured the electrical response of devices by applying a voltage across a packaged device, and taking optical microscope pictures of the microshutter. We then obtained the displacement by measuring it on the pictures (compared to some calibrated dimension). The upper half of Figure 2-28 shows 3 of those pictures.

Figure 2-28. Optical microscope images and simulation results of micro-printhead at different actuation voltages.

Figure 2-29 shows a comparison of measured displacement with simulation results. We did not modify the model to take into account the difference between the expected and measured resonant frequency of the device (see next section). The experimental results are nevertheless comparable to the simulations.
Frequency measurements

Figure 2-29. Comparison of measured displacement as a function of actuation voltage with simulation results.

![Shutter displacement for curved-comb actuator](image)

We measured the frequency response of two of the second design devices using a Umech Technologies MEMS Motion Analyzer. The measured frequencies were 3.9 and 4.1 kHz. This means that we can use the printhead with an operating frequency up to about 1 kHz.

Figure 2-30. Frequency response of a microshutter with the second actuator design. The resonant frequency is 4.1 kHz.
Discussion

Our simulations predicted a first mechanical resonant frequency of 5.6 kHz. The mismatch between the predicted and measured resonant frequency could be due to footing effects during the DRIE etch stopping on the buried oxide layer. If the thickness of the thin (3 micrometers) cantilever beam is reduced due to underetch compared with the thickness of the proofmass, then the resonant frequency would decrease. Figure 2-31 is an SEM picture of comb fingers. A different device was used for this picture than for the frequency measurements. The picture shows significant footing effect, even though the thickness was not reduced in this case. Since the etch rate when using DRIE presents a large non-uniformity across the wafer, footing effects can be very different on two devices coming from two different parts of the wafer. It is possible that the devices we tested may have a reduced thickness, although we were not able to determine if this was the case.

Figure 2-31. SEM picture of the center beam of the second design device with electrode comb fingers sticking out.

Printing Results

For the printing experiments, the packaged device was placed in a vacuum chamber, and held between the material source and a substrate. The substrate is driven by a stepper motor in the horizontal plane, and can be manually adjusted in the vertical direction. The distance between the top surface of the device and the substrate was kept fixed at around
150 micrometers. The base pressure of the chamber was between $10^{-6}$ and $10^{-7}$ Torr. While the material to be printed was evaporated, the substrate was moved in the x and y directions by a computer programmable manipulator, and the microshutter was simultaneously actuated by a voltage source to define patterns.

We evaporated semiconductor organic materials tri(8-hydroxyquinoline) aluminum, noted Alq3, by heating up the source to 230°C. Apart from small molecular weight organic materials, we were also allows able to print silver, with a source temperature of 1100°C. The ability to deposit metals is very valuable for optoelectronic applications, since metals have superior performance compared to the conductors that can be deposited using ink-jet printing.

Figure 2-32 shows the profile of a deposited silver pixel on oxidized silicon. The deposited pixel is about 25 micrometers wide which corresponds to the size of the aperture. More details about the printing process and results can be found in [16].

![Figure 2-32. Profile of deposited silver pixel on oxidized silicon.](image)

The minimal resolvable resolution is determined as two Alq3 pixels are printed next to each other closer and closer. The center to center distance in the leftmost case on Figure 2-33 is 25 micrometers. Two individual pixels can still be distinguished in that case, and the minimal resolvable resolution is determined as equal to one single pixel size, about 25 micrometers. The glowing region in Figure 2-33 is smaller than the pixel size because the thickness of the pixel is not perfectly uniform as can be seen on Figure 2-32.
We were able to print arbitrary patterns, as shown on Figure 2-34.

We also successfully printed active organic optoelectronic devices in which the electroluminescence layer, the semiconducting channel or the metal contacts features have been patterned. Figure 2-35 shows the electroluminescence of a monochromatic OLED (Organic Light Emitting Device) array printed with our setup. See [16].

The 800 ppi pattern resolution corresponding to a pixel size of 30 microns is typical for display applications.
**Printing speed**

In our experiments, the evaporation rate of Alq3 during printing was 1 to 3 nm/s for a source temperature of 230°C and a base pressure of 5x10^{-6} Torr. Material evaporates from the source at a molar rate, $r_{evap}$, proportional to the equilibrium vapor pressure of the organic material, $P_{org}^{eq}$:

$$r_{evap} = k_{evap} P_{org}^{eq}$$

where $k_{evap}$ is a kinetic factor for evaporation.

The equilibrium vapor pressure of the organic material depends exponentially on the source temperature, $T_{source}$:

$$P_{org}^{eq} = P_0 \exp\left(\frac{-\Delta H_{vap}}{RT_{source}}\right),$$

where $\Delta H_{vap}$ is the enthalpy of evaporation and $P_0$ an empirical constant specific to each compound [17].

The temperature to which the source can be heated up is limited to about 400°C for most molecular organic compounds. For example, Alq3 decomposes at about 430°C [18]. If the source temperature is too high, the materials can also be sent to the substrate as clusters instead of individual molecules, which must be avoided to obtain pixels of uniform thickness. This can also create particles contamination in the vacuum chamber.

For a source temperature of 300°C, using values of $\Delta H_{vap}$ given in [17], the evaporation rate of Alq3 could increase to 300 nm/s. A 30 nm thick layer would be deposited in 100 ms, corresponding to a rate of 10 Hz.

Since the possible operating frequency of the actuator is 1 kHz, the speed of printing is limited by the evaporation rate of materials and not by the speed at which the shutter can move.

If using an array of compact actuators and apertures, the printing speed can be increased, and large-area printing can be enabled. A typical XVGA display panel with 1024 x 768 x 3 RGB subpixels can then be printed in less than 5 minutes using R, G and B printheads with 800 nozzles at deposition rates of 300 nm/sec and assuming 100 nm thick pixels.

**Summary**

We verified that the fabricated printheads function as predicted. The microshutter
obstructs the aperture for a voltage of 90V, and the displacement as a function of voltage was correlated with simulations. The resonant frequency of the device is on the order of 4 kHz, which means that it can be used to print at quite high frequency, probably on the order of 1 kHz. The printing speed is limited by the evaporation rate of the materials.

The printheads were used to print small molecular organic materials with a pixel size and resolution of 25 microns. Metals were also printed with the same printheads.

2.5. Discussion

Limitations

There were a number of issues which we anticipated in applying this structure to actual printing.

First, because the printhead must be kept in close proximity to the substrate for optimal printing conditions, there is a risk of the suspended structure contacting the moving substrate and being damaged.

Also, a common challenge in active shuttering is that material deposits on the active structure as well as the substrate. As material builds up on the inside walls of an aperture, it reduces the effective opening and the size of printed patterns. Moreover, material depositing on the shutter and active structure can prevent it from functioning normally. In our design, the actuator structure is on the substrate side and is therefore shielded from the deposition. Material can deposit only on the walls of the through-wafer hole and on the back side of the shutter when it obstructs the aperture. We therefore expected to observe clogging of the aperture and build-up of material on the back of the microshutter.
We printed with Alq3 for several tens of hours at rates of 1 to 10 Angstroms per second, and the size of the patterns obtained didn’t decrease noticeably due to clogging of the aperture. However, after the shutter had obstructed a few micrometers of deposition, the microshutter stayed stuck in closed position. Organic material Alq3 deposited on the back of the microshutter could be seen under the microscope (see Figure 2-36) and was probably causing stiction of the suspended structures to the underlying membrane. Solvent cleaning successfully removed the organic material and freed the shutter, but, after drying, the suspended structure was stuck to the membrane once again. Figure 2-37 shows a similar situation where the microshutter is stuck to the silicon base layer after pentacene deposition.

Other limitations to the technique include the fact that the printing occurs in vacuum and that the material efficiency is very low because the materials are evaporated several
inches away from the MEMS and deposit mostly onto the walls of the chamber. However, the vacuum level is not very high in our experiments ($10^{-5}$ Torr) and simulations show that the pattern would be well defined for base pressures up to $10^{-2}$ Torr [19]. Using an array of apertures and microshutters would lead to a material efficiency similar to shadow masking. The material deposited on the walls of the chamber could also be recovered and reused.

**Improvements and future work**

The problem of damage to the comb-drive actuator and flexure due to contact between the upper surface of the MEMS chip and the printing substrate could be avoided by incorporating shutter protection structures at the wafer level.

For the deposition of organic materials, an in-situ cleaning procedure could be developed as is done for conventional inkjet printers. However, the use of liquids can lead to stiction of the microshutter. A possible cleaning scheme would be to periodically heat the microshutter to re-evaporate the material deposited on its back. This was mentioned when comparing the thermal actuator and electrostatic actuator for the compact design: a thermal actuator would avoid this kind of problem if the shutter was heated to a sufficient temperature.

The problem of stiction of the shutter during operation could be reduced by incorporating bumps under the microshutter or by roughening its surface [20] to reduce the effective contact area with the underlying substrate.

Using a low-surface-energy coating could at the same time reduce the clogging and stiction problems. The silicon surface is hydrophilic because of the presence of native oxide. Adhesion to the surface can be minimized by coating it with thin or monolayer organic coatings with low surface energy.

Chlorosilane based self-assembled monolayer (SAM) coatings, such as those derived from the precursor molecules octadecyltrichlorosilane (OTS) and 1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS) have been showed to alleviate release-related stiction and reduce the work of adhesion of the surfaces [21].

Vapor phase deposition of such coatings reduces problems associated with the use of organic solvents, and decreases particulate contamination of the surfaces. It has been
demonstrated that monolayer films produced from tridecafluoro-1,1,2,2-tetrahydrooctyltrichlorosilane (FOTS) in a low-pressure CVD style reactor exhibit low adhesion energies and good thermal stability [22, 23, 24]. A “layered” vapor deposition scheme of two different molecular films was also developed and provides molecular organic coatings with improved stability to immersion applications, higher temperature stability and overall improved durability as a result of an increased surface coverage [25].

It has been shown that CF-Si(OEt3) coatings reduced the adhesion of evaporated gold on the walls of silicon nitride nanostencils, and therefore reduced clogging problems. However, gold still deposited on the flat outer surface of the coated stencil, but peeled off more easily from the coated samples than from uncoated ones [26].

Other possible improvements to the printing include delivering the materials to the MEMS and heating them locally. This would decrease the amount of heat received by the substrate due to heating of the material source, and decrease risks of re-evaporating the deposited film or altering its structure. It would also increase the material use efficiency and provide a more compact printing system. Similarly, creating a local vacuum environment between the printhead and the printing substrate would allow a compact system by getting rid of the requirement for the printing to occur in a vacuum chamber.

**2.6. Conclusion**

We successfully designed and fabricated a MEMS printhead based on an electrostatic actuator. It was used inside a vacuum chamber to pattern evaporated Alq3, pentacene and silver. We demonstrated the ability to pattern small molecule organic materials and metals used in light emitting devices at resolutions typical for display applications. Directions were provided to improve the performance of this printhead and overcome the limitations of this first implemented version.

The fabricated printheads enable a new patterning technique for organic materials which combines the advantages of ink-jet printing and thermal evaporation. The quality and performance of the printed materials are those of thermally evaporated films, and therefore can lead to high performance optoelectronic devices that are not limited by the presence of solvent during fabrication. At the same time, this printing technique is scalable to large areas and suitable for low-cost and flexible substrates.
References

3. MoJet 2: Electrothermal microscale evaporator

3.1 Principle and motivation

Principle

In the MoJet 2 printing technique, compared to the MoJet 1 technique, we also deposit materials on substrates directly from the gas phase, but without the use of moving micromachined parts.

The micromachined printhead consists of a silicon membrane comporting a central area with macropores, which are 2 microns diameter through holes, and a surrounding thin film platinum heater. The microfabricated device is shown in Figure 3-1.

The material to be printed is first delivered onto the central porous region of the silicon membrane, and deposits inside the pores (number 1 on Figure 3-1). The delivery can be performed either in gaseous or liquid phase. The organic materials could be delivered in gaseous phase by thermal evaporation, or by using a flow of gas (nitrogen for example) to carry molecules to the MoJet 2 chip pores. In our experiments, we only used liquid phase delivery: the organic material is dissolved in a solvent and a drop is deposited on the back side of the membrane. Once the solvent evaporates, organic molecules in solid phase are left inside the pores.

In the second step of the printing, the integrated heater is used to heat up the porous area and the material is re-evaporated from the pores onto the substrate (number 2 on Figure 3-1).

Figure 3-1. Schematic of the printing principle
Using ink-jet technology to deliver the materials in liquid phase allows to precisely control the quantity delivered, and therefore the thickness of the printed pixel.

Also, to speed up the drying, the heater can be used at a lower power to drive the solvent off from the pores.

**Advantages over MoJet1**

Compared to our previous printing technique, the problems of crashing and stiction associated with the moving microshutter are avoided, since there is no moving part.

Also, a number of limitations inherent to the principle of the first technique are avoided. The MoJet 2 printing technique doesn’t require a vacuum ambient during printing. It is a lot less wasteful of materials since the materials are evaporated locally instead of coating the whole chamber.

We will see later that clogging of the aperture is not an issue because the material is completely removed from the pores during each printing cycle.

We will also discuss the possible printing speed using this technique, and see that it is comparable to the printing speed using the first technique (and using commercial ink-jet printers).

**Proof of concept experiments**

We used porous alumina disks to test the ability of a porous medium to retain organic materials and release them upon heating.

![Figure 3-2: SEM pictures of top view (left) and cross-section (right) of a porous alumina disk](image)
The disks were about 60 microns thick and the pores about 200 nm in diameter. Figure 3-2 shows SEM pictures of the top view and cross-section of one of the porous alumina disks.

We deposited a drop of Alq3 dissolved in chloroform at 50mg/mL onto a porous alumina disk. Figure 3-3 shows that the liquid deposited on the top surface filled the pores and Alq3 photoluminescence can be seen throughout the cross-section of the pores. This shows that organic material can be loaded into a porous layer.

We then placed a shadow mask on the opposite side of the disk and a substrate about 100 microns away form the disk and shadow mask. We heated up the disk in a vacuum. The material was found to evaporate from the pores and deposit onto the substrate. Figure 3-3 right shows the pattern obtained on the substrate.

![Figure 3-3: Fluorescent microscope images of the cross-section of an alumina disk after ink loading (left) and of a Alq3 pattern transferred onto a substrate through a shadow mask.](image)

These experiments prove that the principle of MoJet2 printing works with 200 nm pores on a 60 microns thick membrane.

### 3.2 Design and Simulations

#### Design requirements for application

When designing the MoJet2 printheads, the main requirements are for the pores to be able to retain the material after the initial loading step, and to be heated to temperatures sufficient to evaporate the material, with limited spatial non-uniformity and power
consumption. Also, it is preferable if the membrane doesn’t buckle at the temperature of operation, since this could deform the pores and therefore the printed pattern.

For a gas delivery of materials by evaporation, the pores would need to be long enough and have a large enough aspect ratio for enough material to condensate inside the pores. This is what we initially designed for. For liquid delivery however, the liquid is sucked inside the pores by capillary forces. The only requirement is that the total volume of the pores be able to contain the quantity of material that we want to deposit at the dilution level necessary for the ink-jet delivery.

The sublimation temperatures for typical small molecule organic materials are on the order of 200 to 400°C, so the minimum requirement for the heater to be able to heat up the center area of the membrane to that range of temperatures. It would also be interesting to achieve higher temperatures as will be explained later.

**Design parameters selection**

Figure 3-4 shows some of the parameters that were selected during the design, including the pores array and membrane dimensions, as well as the heater geometry.

![Figure 3-4. Schematic of the cross-section and membrane top view of a MoJet 2 printhead chip.](image-url)
The size and aspect ratios of the pores are two of the design parameters. Using electrochemical etching of silicon, it is possible to obtain pores going through a membrane of sizes down to tens of nanometers [1]. However, for our first implementation we used photolithography and DRIE to define the pores. We designed the pores to be 2 microns in diameter, which we considered to be the smallest size that could be repeatably achieved using in house lithography and photomask capabilities.

The overall size of the pores array will determine the size of printed pixels. As in the first generation of MoJet, we chose a nozzle size of about 30 microns. This is achieved by an 8 by 8 array of the 2 \( \mu \text{m} \) diameter pores, with center to center distances of 4 microns.

The standard aspect ratio that can be achieved using DRIE is 10:1. Since our pores are 2 \( \mu \text{m} \) in diameter, this would correspond to a membrane thickness of 20 microns. This seems high enough to retain materials delivered both in gas or liquid phase to the pores.

The large thickness of the silicon membrane makes it more difficult to reach high temperatures than for thinner membranes. The thickness of a membrane heated by thin film microheaters for applications such as microhotplates is typically on the order of 1 micron or less.

The heater design is also easier the larger the membrane is, since the thermal insulation increases with the membrane width. However, if the membrane is too large, its thermal time constant increases, its buckling temperature decreases and the potential packing density of printing nozzles decreases.

![Figure 3-5. Plot of thermal time constant (in ms) of a membrane as a function of its width (in \( \mu \text{m} \))]
The thermal time constant of the membrane is the characteristic time it takes to heat up
the membrane. It shouldn’t be too long for practical applications of the printer. If we
approximate the thermal resistance of the membrane as only its conduction component,
the thermal time constant is independent of the membrane width and thickness. Figure
3-5 shows how the thermal time constant increases with the membrane width.

Buckling is an instability phenomenon that happens as a compressive stress is applied
on a membrane. When the membrane is heated up, it is subject to a thermal stress
compared to the rest of the silicon substrate. The buckling temperature is the temperature
at which the membrane buckles because of this thermal stress. It is possible to operate
membranes in the post-buckling regime at high temperatures [2]. However, for our
specific application, a mechanical deformation of the membrane would change the shape
of the pores and interfere with printing, so we designed the membrane so that its buckling
temperature would be higher than its operating temperature.

Assuming a uniform temperature $T$ of the membrane, the thermal strain in the
membrane is $\varepsilon = \alpha (T - T_0)$. From reference [3], for a square membrane of width $w$ and
thickness $t$, made out of a material of Poisson ratio $\nu$, mechanical stability is attained if

\[
\left( \frac{w}{t} \right)^2 < \frac{-4\pi^2}{9(1+\nu)}.
\]

This means that there is a maximum membrane width over which the
membrane will buckle for a given thermal stress, i.e. a given operating temperature.

Figure 3-6 is a plot of the maximum aspect ratio (width over thickness) of the
membrane to avoid buckling at a given temperature. It shows that the width of the
membrane must be less than 45 times its thickness to avoid buckling at 500°C.

Figure 3-6. Plot of maximum aspect ratio to avoid buckling versus temperature
In the next section we will describe the design of the heater. We chose a membrane width of 400 microns as a trade-off between a small membrane and a large power consumption of the heater.

**Electrothermal simulations and heater design**

To design the heater, we used Finite Element Method (FEM) simulations to predict the current density in the metal layer and the temperature distribution in the membrane as a function of electrical power input.

To avoid electromigration in the Platinum film, the current density shouldn’t exceed the order of $10^{10}$ A/m$^2$ [4].

Microheaters designs in MEMS typically use thin lines with meandering designs to maximize the length that can fit on a given membrane area. However, to heat up our thick membrane, we need to produce a large amount of Joule heating with a limited current density. Therefore we used large lines (50 microns) on each side of the porous region. The temperature distribution in an area of a membrane is more uniform when the heat is produced around the area and not at its center, because most of the heat loss happens by conduction through the membrane and towards the edges of the membrane.

We used the commercial software CoventorWare to run electrothermal simulations of the membrane and heater. We modeled both the whole chip and membrane alone. In both cases, the boundary conditions for the thermal analysis assumed that room temperature was preserved at the external part of model (whole chip or membrane). On the other surfaces, the heat is dissipated through convective and conductive exchange with air and through radiation. The convective coefficient of air used in the simulation is 10 W/m$^2$K (the coefficients for free convection in gas range from 2 to 25 W/m$^2$K). The chip or membrane is considered as a grey emitter with an emissivity of 0.5. The temperature coefficient of resistance (TCR) of the metal film is taken into account.

Figure 3-7 shows the geometry of the final heater.
Figure 3-7 Schematic of the heater top view with dimensions.

Figure 3-8 shows a three-dimensional solid model of the complete chip (left) and the membrane area (center and right), seen from the front (top) and back (bottom). On the zoomed views on the right, the membrane is rendered as partially transparent.

Figure 3-8. Three-dimensional views of the designed chip (left) and membrane area (center and right). On the right, the membrane is rendered as partially transparent.

Figure 3-9 and Figure 3-10 show the temperature and current density profiles obtained for a current of 1.08 A, corresponding to a power consumption of 7W on a device with a 100 nm oxide layer and 200nm of platinum. The temperature coefficient of resistance (TCR) was taken into account so that the resistance of the heater is 3.5 Ohms at room temperature and 6.5 Ω for a current of 1A. The maximum current density in the heater is $10^{11}$ Am$^{-2}$. The maximum and minimum temperatures for the 30 μm x 30 μm central region containing the pores are 664 K and 658 K (391°C and 385°C).
Figure 3-9 Temperature distribution on the membrane and heater for a current of 1A.

Figure 3-10. Current density distribution in the heater for a current of 1A.
### 3.3 Fabrication

**Fabrication Process**

We fabricated two different kinds of MoJet 2 printheads. The first ones didn’t have a silicon dioxide layer between the silicon substrate and the metal layer. We will refer to this optional layer as the oxide barrier layer (See Figure 3-11).

![Figure 3-11. Schematic of the two types of MoJet 2 printhead chips fabricated](image)

The fabrication of the second kind (with oxide barrier layer) is now presented. It starts from a Silicon-on-Insulator (SOI) wafer, with a 20 micron thick silicon device layer, a 1 micron buried oxide layer and a 500 microns base layer (see Figure 3-10, step 1).

First, 1000 Angstroms of silicon dioxide are thermally grown on the SOI wafer (step 2). Then, the metal layer (10 nm Ta and 200 nm Pt) is deposited by e-beam evaporation and patterned by lift-off (steps 3 and 4). The silicon dioxide layer is patterned by a wet etch in Buffered Oxide Etch (BOE) and the pores are etched through the silicon device layer using Deep Reactive Ion Etching (DRIE) (steps 5 and 6). The membrane is then created by etching the back side of the wafer through DRIE to the buried oxide layer which acts as an etch stop (steps 7 and 8). Finally, the front side is protected with photoresist and the buried oxide layer is removed from the back of the membrane through a wet etch in BOE (steps 9 and 10).
Figure 3-12: Illustration of the fabrication process

Fabrication Results

Figure 3-13: Microscope images of a microfabricated printhead chip. Left: Top view of the membrane area. Right: Zoomed view of the pores area.
One of the main problems encountered during fabrication was the low yield of the metal film deposition step. Films thicker than 200 nm would often peel off the wafer (with or without oxide layer). The photoresist used for lift-off patterning was also sometimes peeled off in some areas during deposition so that metal could deposit on areas that were meant to be masked by the photoresist (see Figure 3-14). Both of these problems are probably due to excessive stress in the film caused by the high temperature of the wafer during deposition. The platinum film on top of the photoresist could peel the underlying photoresist off when curling off because of thermal stress.

![Figure 3-14: Lift-off issues during fabrication of MoJet2 chips. Some metal deposited in areas that were supposed to be masked by photoresist.](image)

The photoresist protecting the front side of the chip for the last BOE etch tends to flake off during the wet etch, and BOE attacks the silicon oxide layer present on the front side of the chip. If using HF instead of BOE, the photoresist peels off even more and the wet etch attacks the metal layer a well as the oxide layer. On Figure 3-15, the optical images of three locations on a wafer after the back side oxide etch show different degrees of etching of the front side oxide near the pores. On the left, it has not been touched during the back side oxide etch. In the center picture, the oxide has been partially attacked and on the right picture it has been completely removed.
Figure 3-15: Optical microscope pictures showing 3 locations on a wafer after the back side oxide etch. The front side oxide near the pores shows different degrees of etching.

Packaging

For the printing tests, the chip was attached to a ceramic package and the two heater contact pads were connected to the pins on the package using silver paste. The conductive tape used for MoJet 1 couldn’t be used because it didn’t have a high enough current-carrying capacity. The package was held upside down during printing: the back side of the chip, where the ink is delivered is facing up, and the front with the heater and pores on the membrane faces down, and are held in proximity to the printing substrate. For the other characterization and testing, the chip was simply placed on a probe station.

Figure 3-16. Picture of fabricated chip (back and front) and packaged chip

3.4 Testing Results

Temperature measurements

Our first characterization of the chip was to determine its temperature. We want the
porous region of the membrane to be able to reach temperatures higher than the sublimation temperature of the organic material to be deposited. However, if the temperature is too high, the material can be decomposed. It is therefore important to characterize the temperature and relate it to simulations in order to predict and control it.

We used different techniques to characterize the temperature of the printhead. Using an infrared microscope (Quantum Focus “InfraScope II”), we were able to obtain the temperature profile of the top surface of the printhead chip under different actuation currents. The temperature profile measured for an actuation current of 0.85A for a chip of type 1 (no oxide barrier layer) is shown on Figure 3-17.

![Figure 3-17 Temperature profile of the printhead chip obtained with an infrared microscope. The picture on the right is a zoom on the membrane region (actuation current of 0.85A).](image)

We also measured the temperature using two other techniques: by using a thermocouple, and by measuring the resistance of the device. The temperature of the heater is related to its resistance by the Temperature Coefficient of Resistance (TCR) of the metal film. The TCR \( \alpha \) is defined as follows:

\[
R = R_0 (1 + \alpha (T - T_0))
\]

where \( R_0 \) is the resistance at the initial temperature \( T_0 \), and \( R \) is the resistance at the temperature \( T \).

The temperature is then given by:
\[ T = T_0 + \frac{1}{\alpha} \frac{R - R_0}{R_0} , \text{ where } \frac{R - R_0}{R_0} \text{ is the normalized resistance.} \]

We used a previously measured [5] value of \( \alpha = 0.0034 \text{ K}^{-1} \) \( \frac{1}{\alpha} = 292 \text{ K} \) for the TCR of the Ta/Pt stack (see Figure 3-18). The relationship between the temperature of platinum and its normalized resistance is linear for a wide range of temperatures (up to 1000°C).

![Figure 3-18](image)

**Figure 3-18** Temperature as a function of normalized resistance for a Pt thin film heater (from [5]).

The temperature obtained by electrical measurement is averaged over the length of the heater. It is possible to relate it to the maximum temperature in the metal and to the temperature at the center of the silicon membrane using simulations.

The thermocouple we use has a small measuring spot of 70 microns. However, this is still large compared to the size of the area we are interested in measuring the temperature of. Therefore, it is measuring a spatial average of the temperature. Also, the thermal mass of the thermocouple is not negligible compared to that of the membrane, so that the thermocouple perturbs the measurement by modifying the temperature of the membrane.

The Infrared microscope measurement is not accurate at low temperatures because silicon is transparent at the infrared wavelengths detected by the instrument. It was also
difficult to compare data points obtained using this technique and the other techniques because of contact resistances in the setup.

We compared measurements obtained using the 3 techniques to simulation results obtained using the software CoventorWare. The results are shown on Figure 3-17. The device reaches a temperature of 200°C at about 5 Watts of electrical power.

The printheads of type 2 (no oxide barrier layer) exhibit better temperature performance, reaching almost 500°C (average temperature) for about 0.8A of current and 5 Watts of power as shown on Figure 3-20.

Figure 3-19 Temperature of the printheads with no oxide barrier layer obtained by different measurement techniques, and compared to simulation results.

Figure 3-20 Temperature of the devices with an oxide barrier layer obtained by electrical resistance measurements.
The membrane area reaches the temperature needed to evaporate the organic material present in the pores. Small molecule organic materials typically have sublimation temperatures in the range of 150°C to 300°C.

**Thermal time constant measurements**

The thermal time constant of the device was estimated by monitoring its resistance as a function of time as it is heated up.

The test setup is shown in Figure 3-19 left. The MoJet2 heater is placed in series with a 1 Ω resistor. The signal generator for a portable thermal ink-jet printer (noted TIPS) and a transistor are used as the power source. The source signal is captured by a digital oscilloscope (see Figure 3-19 right).

![Figure 3-21. Test setup (left) and oscilloscope measurement of the input signal (right) for the thermal time constant measurements.](image)

The MoJet2 chip is initially at room temperature. The TIPS controller then applies a train of short pulses to the heater. This is equivalent to a step voltage of lower voltage since the duration of the pulses is much shorter than the time constant of the device. As the silicon membrane is heated up, the resistance of the thin film metal heater increases and the voltage across the serial resistor decreases, as shown in Figure 3-22. This measurement is used to calculate the resistance of the heater as a function of time. The resistance of the device is linearly related to its temperature, through the thermal coefficient of resistance.
Both simulations and measurements show that the thermal time constant of the silicon membrane, and therefore the time necessary to heat up the pores area, is of the order of a millisecond (see Figure 3-23). This suggests that our printhead could be used with a firing frequency of the order of 1 kHz, which is comparable to the nozzle firing rate of commercial ink-jet printers (1 to 50 kHZ). If array of nozzles of sizes comparable to the arrays used in ink-jet printheads can be used, then the printing speed would be comparable to that of commercial ink-jet printers.
Printing test setup and results

The printing experiments and results are described in detail in [6]. The following is a short summary.

For printing tests, a MoJet 2 printhead was used in conjunction with a handheld ink-jet printer for the delivery of droplets, as shown on Figure 3-24.

![Figure 3-24. Pictures of the printing setup.](image)

The MEMS chip is placed between the fixed ink-jet printer and the substrate, the front side of the MEMS chip facing the substrate. The ink-jet nozzle is aligned to the porous region of the MEMS chip using a video camera placed below the MoJet chip. The substrate is mounted on an X-Y stage and moved relative to the MoJet printhead to print arbitrary patterns.

The heater is powered by a computer controlled pulsed DC power supply. For typical Alq3 depositions, we use about 10 pulses of 10 μs duration to drive off the solvent followed by about 150 pulses of 10 μs at 12V with a 2 ohm resistor in series. The voltage is higher than the steady-state voltage needed to heat up the chip to the same temperature.

The printing experiments showed that organic material could indeed be loaded in the pores and re-evaporated as described on Figure 3-25.

Figure 3-25 (a) shows a fluorescent microscope image of the porous region seen from the front of the device after a drop of organic material Alq3 in solvent was deposited on
the back of the device. Green fluorescent material Alq3 is loaded in the pores.

The integrated metal heater was then used to heat up the central area of the silicon membrane, in order to re-evaporate material from the porous area. No fluorescence was detected from the pores afterwards. Figure 3-25 (b) shows an optical microscope image of the porous region of the device illuminated from the back. It can be seen that the pores are empty, and therefore Alq3 has successfully been removed from the pores.

![Figure 3-25](image)

Figure 3-25. Images of the porous area of a MoJet2 chip: (a) Photoluminescent microscope image of pores filled with Alq3 solids after a drop of Alq3 in solvent was deposited on the back of the membrane and (b) back illuminated optical microscope picture of the empty pores after heating and complete evaporation of Alq3.

After several of printing cycles in an air ambient, oxidized organic materials can stay inside the pores. However, the printing needs to be done in nitrogen to avoid rapid degradation of the organic films, and this prevents oxidation and clogging problems.

![Figure 3-26](image)

Figure 3-26. Pixel of organic material Alq3 printed with our setup (fluorescent image).

We can achieve 60 micron pixels at ambient pressure (see Figure 3-26) for a distance
of 100 microns between the substrate and the MEMS printhead [7]. The size of our nozzle, the array of pores in the center of the silicon membrane, is about 25 microns by 25 microns. This corresponds to a broadening factor of about 2 compared to printing in a $10^{-6}$ Torr vacuum with a 25 micron aperture.

### 3.5 Summary

**Achievements and advantages of MoJet Printing**

We designed and fabricated MoJet 2 printheads that enabled the evaporative printing of molecular organic materials with 60 microns resolution at ambient pressure.

Since the materials are deposited directly from the gas phase, they exhibit the high purity and functionality of evaporated thin films. There is no liquid solvent in contact with the substrate during the material deposition, in contrast with ink-jet printing. Multilayer films can therefore be printed easily, without the concerns about solvent compatibility that arise with ink-jet printing. Small molecular organic materials can also be easily printed whereas they are difficult to deposit using ink-jet printing.

Pixels of materials printed using ink-jet printing often exhibit the coffee ring effect [8]. After evaporation of a printed solution droplet, most of the solute is deposited as a ring that marks the original contact line, leading to a non-uniform thickness in the printed pixels. It is possible to limit this effect for example by modifying the surface properties of the substrate or by using a mix of solvents [9]. By dissolving a polymer in a mixture of two solvents, the first solvent having a high boiling point and a low solubility for the polymer, and the second solvent having a low boiling point and a high solubility for the polymer, the dissolving potential of the solvent gradually decreases during evaporation and the polymer precipitates before a ring is formed [10]. However, Molecular Jet printing creates pixels with a uniform thickness without difficult solvent formulation or use of intermediate layers to control the substrate surface properties.

Figure 3-27 shows the superior thickness uniformity of pixels deposited with our technique compared to ink-jet printed pixels. Figure 3-27(a) shows the photoluminescence image of an array of Alq3 pixels printed using a thermal ink-jet printhead. Typical “coffee ring” patterns can be seen indicating non-uniformity in the film thickness of the printed films. Figure 3-27(b) shows pixels printed starting from the
same solution using the MoJet 2 printer. The thickness of the pixel is much more uniform for MoJet printing.

![Figure 3-27. Comparison of printed Alq3 pixels. (a) Ink-jet printed pixels (with coffee ring effect). (b) Pixels printed using Molecular Jet Printing.](image)

We saw that the printing speed of a MoJet printhead could be comparable to that of an inkjet printer. Also, no vacuum is necessary for the printing, so that the printing setup is very comparable for ink-jet and MoJet printing. MoJet printing is therefore scalable to large areas, and can be used to print on low-cost substrates as well.

Table 3 summarizes how MoJet printing combines the advantages of thermal evaporation and ink-jet printing.

<table>
<thead>
<tr>
<th>Properties</th>
<th>Deposition and Patterning Techniques</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vacuum Sublimation and Shadow masking</td>
</tr>
<tr>
<td>Ambient printing</td>
<td>No</td>
</tr>
<tr>
<td>Best film functionality</td>
<td>Yes</td>
</tr>
<tr>
<td>Thickness uniformity</td>
<td>Yes</td>
</tr>
<tr>
<td>Scalability</td>
<td>No</td>
</tr>
</tbody>
</table>

Table 3: Advantages of Molecular Jet Printing
In ink-jet printing of a material, when the solvent dries off after printing, the material can clog the printing nozzle and limit the ability to reuse the printhead. When using a shadow mask to pattern an evaporated film, some of the material deposits on the sides of the shadow mask and progressively decreases the aperture size. This is particularly a problem for small features. As seen earlier, there is no nozzle clogging issue when printing small molecule organic material with MoJet2, because the material evaporates completely from the pores at each printing cycle. Therefore one of the advantages of MoJet2 is that the number of times that the printhead can be used is not limited by clogging of the nozzle.

The fraction of used material that is deposited in the printed pixel is much better than for shadow masking, where it is equal to the fraction of the substrate that is covered by the pattern. It is comparable to that of ink-jet printing, although some of the material present in the pores evaporates towards the back of the printhead instead of towards the front where the substrate is. Some material also stays on the back of the membrane if part of the drop deposited there doesn’t end up inside the pores.

**Limitations**

The smallest printed pixel we obtained with MoJet2 printing was 60 microns wide. Ink-jet printing can get down to about 10 micron pixels. It would probably be possible to define smaller features by decreasing the size of the pores array but, at ambient pressure, diffusion plays a large role in the size of the printed pixel. The temperature of the membrane and the aspect ratio of the pores might be able to be optimized in this respect, and adding a pressure drop or gas flux through the pores might also increase the precision of the printing. The uniformity of the pixel might however not be as good if making such changes.

The printing speed that can be achieved depends on the density of nozzles that can be used in an array. The membrane is 400 micron wide, and the membranes need to be separated by thick silicon to allow heating up one nozzle and not having the others heat up at the same time, i.e. avoid thermal cross-talk. Heating up one of the membranes takes only 1 millisecond, but the time it takes for the drop to be deposited, for the solvent to evaporate and for the membrane to cool down must also be taken into account.
The range of materials that can be deposited using the MoJet2 technique needs to be determined. While this technique is very useful since it expands the capabilities of ink-jet printing of organics by allowing the evaporative printing of small molecule organic semiconductors, it couldn’t be applied to all materials that can be printed using ink-jet printing. MoJet2 wouldn’t work to print high viscosity polymers, as well as materials that can’t withstand high temperatures, such as metal nanoparticles that typically have a low sintering temperature.

The material efficiency is less than 100% and this might be an issue for very expensive materials. It could possibly be increased by heating the membrane from the back or using pores with tapered sidewalls, which would reduce the amount of material directed away from the substrate.

The reliability and lifetime of the printhead chip is not limited by the mechanical strength of the silicon membrane. Mechanical forces exerted on the membrane, such as for example the pressure exerted on the membrane during the liquid deposition of material on its back side, are very small compared to the burst pressure of the membrane. The burst pressure is calculated below for a square membrane of dimensions 20 μm by 400 μm by 400 μm, without pores.

According to [11], the burst pressure for a membrane with no prestress is:

\[ P = c_2 M t \frac{\delta^3}{l^4} \]

where \( c_2 = 1.981 - 0.585\nu \) for a square membrane, and \( \sigma_{\text{edge}} = \frac{E}{(1-\nu^2)}\varepsilon_{\text{edge}} \)

is equal to the fracture stress 1.5 GPa, \( \varepsilon_{\text{edge}} = R \frac{\delta^2}{l^2} \) with \( R = 0.872 \) for a square membrane. For silicon, \( \nu = 0.2, \) \( E=150 \text{ GPa}, M=180.5 \text{ GPa}. \) For our membrane, the half-span is \( l = 200 \mu\text{m} \) and the thickness is \( t = 20 \mu\text{m}. \) The deflection at the onset of burst is \( \delta = 20.9 \mu\text{m}, \) and the burst pressure is \( P = 38.8 \text{ MPa} = 383 \text{ atm}. \)

The burst pressure of the silicon membrane is larger than 300 atm, and therefore the pressures exerted on the membrane during the printing process are not an issue.

The most important limitation of the MoJet2 chip is its failure due to temperature, and in particular the degradation of the thin film metal heater. This will be the topic of the next chapter.
References

4. High Temperature limits of MoJet2: heater degradation study

4.1 MoJet heater temperature degradation and failure

On type 1 devices: no oxide barrier layer

When the electrical power input on the MoJet2 heater is increased progressively, the metal layer degrades and the heater eventually fails: the current drops dramatically as the resistance increases.

Figure 4-1 shows a microscope image of two MoJet2 heaters without oxide barrier layers. The Ta/Pt layer is deposited directly on top of silicon. The picture to the left shows a heater that was self-heated until some degradation happened. The picture to the right shows a heater that was annealed in nitrogen at 500°C for 2 hours. The degraded metal looks similar in the two cases: it is roughened which makes it appear dark on the microscope images.

![Figure 4-1: Microscope images of MoJet 2 heaters (no oxide barrier layer) after self-heated failure (left) and after anneal for 2 hours in N\textsubscript{2} at 500°C (right)]

Figure 4-2 shows Scanning Electron Microscope images of the same two heaters. The lower half pictures at 2,000 X magnification show similar structure.

Auger electron spectroscopy was performed on both samples. The discolored areas show 10-20% silicon, as opposed to nearby smooth areas that show much less silicon (see Figure 4-3).
Figure 4-2: SEM pictures of MoJet2 heaters. Left: self-heated failure. Right: annealed. The bottom pictures correspond to the areas defined by the red rectangles in the top pictures.

Figure 4-3: Elemental Auger maps of Pt and Si on the self-heated MoJet2 chip.

Depth profiles of a smooth and roughened area show the source of the roughening (See Figure 4-4 and Figure 4-5). In the smooth area there are discrete layers of Pt, Ta, and Si, while the roughened areas show a Pt-Ta-Si layer over Si with a broad diffusion-type interface. The failure appears to initiate from partial silicidation of the Pt film or Pt-Si interdiffusion. There was sufficient interdiffusion in the hot areas to disrupt the surface morphology and layer integrity. The Ta is not found as a discrete layer in the failure areas, and Si is found throughout the Pt film.
Figure 4-4: Sputtered Auger profile of heater chip before failure

Figure 4-5: Sputtered Auger profile of heater in a failed region
This is consistent with the observations reported in [1] that, when a tantalum film on silicon is annealed, there is inter-diffusion at the Ta/Si interface at a temperature lower than 600°C, and a silicide (Ta₅Si₃) is formed after annealing at 750°C.

This suggests that using a barrier layer between the silicon substrate and the metal stack would improve the high temperature performance of the heater.

**On type 2 devices: with an oxide barrier layer**

The devices fabricated with an oxide barrier layer also exhibited a degradation of the metal layer at high input power as shown on Figure 4-6. The silicon membrane also often cracks during the failure, but this happens after the heater as failed and might be due to the fast cooling of the membrane as the heating stops.

![Figure 4-6: Microscope images of a MoJet 2 heater with an oxide barrier layer after some degradation due to self-heating (left) and after complete failure (right).](image)

Figure 4-7 shows SEM pictures of such a failed device. The structure of the failed metal film shows a lot of blistering.

![Figure 4-7: Scanning electron microscope images of a failed MoJet2 heater with an oxide barrier.](image)
Figure 4-8 shows part of the pores area. The silicon dioxide layer isn’t damaged (except for cracks where the membrane cracked) but silicon filled in the pores. The silicon layer used as the membrane is initially a single crystal. The modification of the silicon layer structure indicates that the membrane was heated to very high temperatures during the failure process. However, the silicon dioxide layer is still intact, as can be seen on the Focused Ion Beam cross-sections of Figure 4-9.

Figure 4-8: Scanning electron microscope images of the pores area of a failed MoJet2 heater with an oxide barrier layer.

Figure 4-9: SEM pictures of Focused Ion Beam cross-sections of a failed MoJet2 heater with an oxide barrier layer. (The Cr layer is added and used as a masking layer for the FIB process.)
As in chapter 3, the average temperature measurements presented in this chapter are obtained by resistance measurements and calculations using the TCR of the metal film. The corresponding maximum temperature in the heater is obtained by simulations.

Figure 4-10 shows a comparison of the average temperature of MoJet2 heaters as a function of power input for two samples of type 1 (no oxide barrier layer) and 2 samples of type 2 (with oxide barrier layer). The measurements stop when the heater fails, so that the last points of each curve correspond to the highest temperatures reached before failure. It can be seen that the presence of an oxide barrier layer increases the maximum temperature that can be reached by the MoJet heater.

![Figure 4-10: Electrical measurements showing average temperature as a function of power for two samples each of MoJet2 heater type 1 and 2.](image)

Figure 4-11: Comparison of optical microscope images of failed MoJet2 chips of type 1 and 2.

Left: no oxide barrier layer (type 1). Right: with an oxide barrier layer (type 2).
4.2 Motivation for heater degradation study

Advantages of higher temperature range

As can be seen on Figure 4-10, the MoJet heaters that we fabricated can reach temperatures sufficient for the printing of small molecule organic materials (200°C to 400°C range). However the onset of degradation starts at temperatures lower than the failure temperature shown on the plot. Once the heater has started to degrade, its electrical properties change with time, and this affects the reproducibility of temperature and the reliability of the chip. Therefore, if we can increase the failure temperature of the heaters, we will also improve the range of reliable operation of the printer.

Higher temperatures could also enable a wider range of materials to be printed using the MoJet2 technique. For example, it might be possible to print low melting temperature metals, such as Sn (melting point 232°C) and Sn alloys or Indium (melting point 157°C).

Such a heater could also be used for other applications related to non-lithographic direct fabrication of optoelectronic devices or MEMS. For example, it could be used to provide a local annealing capability after a film or pixel has been printed on a substrate. In that case, it would be interesting to be able achieve temperatures as high as possible.

Also, microheaters on membranes are common in MEMS applications, and often made out of platinum. Studies about platinum thin film heaters degradation and failure are therefore of general interest to the field of MEMS.

Background

Platinum is often used for thin film heaters and temperature sensors in MEMS devices because it is inert and stable at high temperature, and because its variation of resistance with temperature is linear over a wide range of temperatures.

The adhesion of platinum on silicon, silicon oxide or nitride layers is known to be problematic, since platinum peels off from the silicon surface. At high temperatures, too much stress is present in the platinum layer resulting in its detachment from the surface. A titanium or tantalum interlayer is typically used as an adhesion layer between the platinum layer and the substrate.

Ti adhesion layers fail at temperatures higher than 700°C by diffusing into the Pt layer
along grain boundaries [2, 3, 4, 5]. The Ti oxidizes at the surface in an oxygen ambient or forms TiN with nitrogen diffusing in the platinum in a nitrogen ambient, and reacts with underlying SiO2 when it is the underlying layer. Pt/Ti films also degrade by agglomeration at temperatures above 500°C [6].

Tantalum interlayers are found to give a better adhesion than titanium interlayers for platinum on silicon [6]. Agglomeration is found to be the main degradation phenomenon for long exposures of Ti/Pt and Ta/Pt to high temperatures.

Stress is also found to have a role in Pt films degradation, in particular through the formation of hillocks and holes, and film delamination [6, 7, 8].

Oxygen exposure enhances the degradation. Oxygen can diffuse to the Ti/Pt or Ta/Pt interface and reduce the adhesion of the platinum layer. It is possible to reduce the degradation by depositing a protective layer above the platinum layer.

The thermal history of the sample influences its degradation. Exposure to higher temperature and for longer times increase the degradation whereas initial anneals in non-oxidizing ambients reduce degradation [9, 10].

Microhotplates are microstructures typically comporting a microheater on a silicon or silicon nitride membrane [11]. They can be used in applications such as microsensors to heat up a small area.

Reference [12] looked at the reliability of microplates with platinum heaters. The authors studied heaters made of platinum or platinum-iridium with a tantalum adhesion layer. They used backscattered SEM observations, mechanical deformation measurement and thermal laser stimulation techniques to study accelerated ageing of the self-heated devices. The heater failure is attributed to electro-stress migration of platinum atoms. They also found that the platinum heaters with iridium exhibited a longer lifetime than heaters made only of platinum.

Thicker adhesion layers are found to affect the Pt films negatively, whereas thicker platinum layers exhibit less degradation for the same conditions. The degradation of Pt thin films used as heaters seems to be mainly caused by reactions and diffusion processes related to the adhesion layer.

Some techniques have been developed to obtain pure platinum films (no adhesion layer) with good adhesion to oxide and nitride films. One technique consists of exposing
a silicon nitride layer to an SF₆-O₂ plasma before depositing a platinum film by sputtering. This improves adhesion by removing contamination from the surface and roughening it [10, 13].

The electrical behavior at high temperatures of Pt thin films without adhesion layer was found to be better than that of Ta/Pt films. However, structural degradation was more pronounced than in Ta/Pt films for identical anneal conditions. For example, the development of holes in the film began at a lower temperature. Also, the comparison of failure temperatures and powers for Ta/Pt and pure Pt heaters wasn’t conclusive because the two thin films had different heating histories. The authors attributed the heater failure at high temperatures to physical degradation as the thin film agglomerates.

**Summary**

The main limitation of our MoJet2 printhead chip is the failure of the thin film Pt heater at high voltages and temperatures. Previous studies of Pt microheaters have found that Ta/Pt heaters with a Ta layer of about 10nm show the less degradation during high temperature anneals. There are few studies of the degradation of self-heated Pt heaters on membranes and they advance different mechanisms as being the cause of failure: electromigration, stress-induced failure and agglomeration.

**4.3 Test device motivation and design**

**Test device motivation**

To study the degradation of thin film platinum heaters, we didn’t use the MoJet heaters directly but designed a test device. The device comports two similar heaters on a silicon membrane. This allows us to decouple the temperature and the current density level in a heater. The idea is that any of the two heaters can heat up the silicon membrane. We can design the two resistors to have a very similar temperature distribution when only one of them is powered, by positioning them close to each other on the membrane. By powering only one of the heaters, we can therefore compare two resistors with similar temperature, one with a high current density and the other with no current.

We want to measure the temperature of the two heaters by monitoring their resistance variations. In that regard, having two resistors is also helpful since we can measure the
temperature of the silicon membrane using the non-powered resistor, which gives a more accurate measurement of resistance. The microheater on the MoJet2 printhead chip has a resistance of only about 5 Ohms, which makes it difficult to detect changes in resistance as the temperature increases, and parasitic resistances can not be neglected.

We designed the resistors on the test device to have a much higher resistance of about 100 Ohms, so that there would be less noise in the measurements of resistance variation and temperature. We also connected each resistor to four pads on the chip, in order to use four-point probe configurations to measure the resistances of the two heaters.

**Test device fabrication**

We fabricated the test devices using the same process than for the MoJet2 chips, except that we omitted the etching of pores through the membrane. The oxide barrier layer thickness ranged from 100 nm to 1 μm. The other layers have the same thickness than for the MoJet2 chips. The silicon membrane is 20 μm thick, the resistors films are 10 nm of tantalum adhesion layer and about 150 nm of platinum deposited using an e-beam evaporator at a pressure of 2x10^{-6} Torr, without breaking the vacuum between the deposition of the two layers.

We also fabricated test device chips with no membrane using a silicon wafer (~ 600 microns thick) instead of a silicon-on-insulator wafer.

**Test device design**

Using the simulation software CoventorWare, we studied different resistor designs.

We used 20 microns wide lines for the resistors, and gaps between them of 10 microns, so that the requirements on the lift-off process for metal patterning wouldn’t be too stringent. The closer the resistors are, the more similar their temperature profile will be. Also, the narrower they are, the more resistive they will be.

We increased the membrane size to 1 mm x 1mm (compared to 400 x 400 μm for the MoJet2 membrane). The geometry of the resistors is shown in Figure 4-12. The outer resistor has a resistance of 213 Ω and the inner one of 203 Ω.

The temperature distributions of the two resistors are similar when heating only the outer resistor as shown on Figure 4-13 and Figure 4-14. The maximum temperatures of the outer and inner resistors are within 3% and the average temperatures within 5%.
Figure 4-12: Geometry of the two resistors on a 1 mm wide membrane (thicknesses not to scale).

Figure 4-13: Temperature distribution on the membrane when heating the outer resistor.

Figure 4-14: Detail of the temperature distribution at the center of the membrane. The solid lines show the position of the outer resistor and the dotted line that of the outer resistor.
**Test device layout**

Figure 4-15 shows the layout of the test device chip. The overall chip is the same size than the MoJet1 and MoJet2 chips (4.6 x 4.6mm).

The two resistors are each connected to four contact pads, for 4-point probe measurements of the resistance. We minimized the metal length between the end of each resistor line and the two lines leading to the two pads, one of which is used to pass current and the other one to measure voltage.

We also made sure that the two power-carrying lines were wider than the other lines, to avoid excessive heating and degradation of those lines.

Other design considerations included minimizing current crowding that localizes heating and metal damage by rounding out corners.

![Diagram of test device layout](image)

**Figure 4-15: Layout of the test device. The red contour shows the position of the silicon membrane.**

**Post-fabrication annealing**

Platinum resistors present a hysteresis effect in their electrical characteristics if they are not annealed after deposition.

Figure 4-16 shows the resistance of the outer resistor of a test device (without a
membrane) as the voltage is increased from 0 to 20 Volts, then decreased to 0V, increased to 25V and back to 0V and finally increased to 30V and back to 0V again. The blue curve shows the changes in resistance of a device that hasn’t been annealed. It can be seen that the resistance at 0V decreases after each increase in the maximum voltage applied to the resistor. The green curve shows the resistance of a device that has been annealed in air at 500°C for an hour. The resistance is the same for the 3 voltage loops.

In order to be able to calculate the temperature from resistance measurements, the device must therefore be annealed after deposition.

Figure 4-16: Resistance as a function of voltage for the outer resistor of a test device on a chip without a membrane.

Table 4 shows the resistance of the outer heaters of devices with and without membrane before and after anneal at 500°C in air for an hour. The resistance after anneal is the same in both cases, but the resistance before anneal of the devices with membranes is lower than that of the devices without membranes. This is probably due to the fact that the temperature reached during processing is higher for the devices with membranes, since they are submitted to an oxygen plasma after the DRIE etch step. Therefore, the heaters on membrane are partially annealed during processing, and this lowers their initial resistance.
<table>
<thead>
<tr>
<th></th>
<th>Resistance before anneal</th>
<th>Resistance after anneal 500°C 1hr in air</th>
<th>Ratio of resistance before and after anneal</th>
</tr>
</thead>
<tbody>
<tr>
<td>No membrane</td>
<td>165 +3 Ω</td>
<td>103+2 Ω</td>
<td>1.6</td>
</tr>
<tr>
<td>Membrane</td>
<td>124+5 Ω</td>
<td>103+4 Ω</td>
<td>1.2</td>
</tr>
</tbody>
</table>

Table 4: Effect of anneal on the outer resistor of the test device (average over 3 chips)

All heaters were submitted to an anneal at 700°C in air prior to testing to ensure that the resistance measurements could be used to calculate the temperature of the heaters.

### 4.4 Characterization of the failure mechanism

**Comparison of the effects of current and temperature**

In the failure of metal lines, current density can play a role in phenomena such as electromigration. To see whether the current density level plays a role in the degradation of the metal on the test devices, we compared the failure conditions of a self-heated resistor and a resistor at the same temperature but experiencing a lower current density.

We weren’t able to heat up one of the resistors to its failure temperature by using the other heater only, because the heater would fail before the resistor. Simulations show that, when current is passed through only one of the heaters, its temperature is always higher than that of the other resistor.

In the experiment, we therefore passed some current through the inner resistor and achieved the rest of the heating by actuating the outer resistor from the same chip.

We kept the voltage on the inner resistor at 18V, and increased the voltage on the outer heater from 0V until the inner resistor failed.

We compared the failure conditions to those achieved when increasing the voltage on the inner resistor from 0V until failure.

Figure 4-17 shows the resistance as a function of current in the two cases. The resistance of the self-heated resistor increases as the voltage across it is increased (green...
data points), because the temperature of the membrane increases and the TCR of platinum is positive. When a constant voltage of 18V is applied across the inner resistor, as the voltage is increased on the other resistor, the resistance of the inner resistor increases as the membrane is heated up, and the current through it decreases (blue data points).

Figure 4-17: Electrical characteristics and failure conditions of the inner resistor in the two experiments described in Figure 4-18.

Figure 4-18: Voltage conditions on the inner and outer resistors for the two measurements.
We observed that in the two experiments the inner resistor failed at similar resistance values but for very different current levels. This means that the temperature of the inner resistor at the failure point is similar in the two cases, but the current density in the resistor is 1.5 times higher in the first experiment.

We therefore conclude that the current density in the resistor doesn’t play an important role in the degradation, and that the degradation is mainly determined by temperature.

**Comparison of device on membrane and not on membrane**

The thermal stresses generated when heating up a membrane can be partially relieved by deformation of the membrane. We fabricated samples without a membrane, but where all the other dimensions and film thicknesses are the same as for the test devices with membranes (see schematics on Figure 4-19). By comparing the failure conditions for the two kinds of devices, we can investigate the role of stress in the heater degradation, because there is no stress relief in the devices without membrane.

![Figure 4-19: Left: Top view SEM of a test device. Right: Cross-section of a test device without membrane (top) and with a membrane (bottom).](image)

In the absence of a membrane, the passive resistor is heated to a lower temperature than the resistor through which current is passed, as can be seen on Figure 4-20 and Figure 4-21. The temperature distribution along the self-heated resistor is more uniform, and the maximum temperature is lower than for devices on a membrane at the same input power.
Figure 4-20: Temperature distribution on the top surface of a device without a membrane.

Figure 4-21: Temperature distribution on the top surface of a device with a membrane.
Figure 4-22 shows the average temperature of the self-heated resistor as a function of the current applied to it. The last data points correspond to the heater failure conditions. It can be seen that in the two cases the heater fails at similar temperatures but different current levels.

![Graph showing temperature as a function of current](image)

**Figure 4-22**: Temperature as a function of current through a test device resistor for devices on a membrane (blue points) and without a membrane (green and black points).

This reinforces the findings of the previous part that the current level is not a determining factor for the heater failure.

Moreover, it shows that the temperature of failure is the same for heaters on membrane and on bulk silicon substrates, and therefore that there is no substantial effect of stress relief on the failure temperature.

We also observed that the failure spot (see next section) was always positioned in the middle of the membrane. For samples without a membrane, the failure spot is at random locations along the resistor. This is consistent with the hypothesis that the failure spot happens at the highest temperature point along the resistor, since the highest temperature occurs at the middle of the membrane for devices with a membrane, but the temperature is much more uniform along the resistor for devices without a membrane.
Failure spot characterization

Figure 4-23 shows SEM pictures of a test device on a membrane after the voltage across the outer resistor was increased until failure occurred. A failure spot can be seen on the resistor. For devices on a membrane, the failure spot is always located at the middle of the membrane on the resistor. Close-up pictures of the failure spot show some metal beads on one side of the opening and some streaks leading to the beads. Auger electron spectroscopy shows that the streaks are made of tantalum (see Figure 4-24).

Figure 4-23: Scanning Electron Microscope images of the failure spot on a device with a membrane.

As mentioned in the previous part, for devices without a membrane the failure spot appears in random places along the resistor. Figure 4-25 shows an example of such a failure spot. The close-up view also shows that the failure spot is longer than for a device on a membrane.

When we apply a step voltage across the resistor instead of increasing the voltage until failure, we find that the failure spot length increases as the voltage used increases. This is shown on Figure 4-26, where we can see failure spots for step voltages of 35, 40, 60 and 75 Volts with lengths of about 5, 10, 20 and 40 microns. For step voltages, especially higher values of the voltage, there are less or no beads but the edges of the failure spot show an accumulation of metal.
Figure 4-24: Elemental maps of test device failure spot obtained by Auger Electron Spectroscopy.

Figure 4-25: SEM images of the failure spot for a device without a membrane.
Figure 4-26: SEM images of the failure spot for a device on a membrane for different step voltages.

Figure 4-27: Comparison of the failure spot for resistors failed by increasing the voltage until failure (left) and by applying a voltage step of 40V (middle and right).
Test device time to failure

One important characteristic of the failure mechanism is that it is very fast. When increasing the voltage progressively until failure, the failure happens in a time shorter than the measuring time step (about 1 second). If the voltage is held at a value slightly smaller than the value causing instantaneous failure, the failure will usually occur after a longer time, for example several seconds. However, this is difficult to characterize because the voltage needed for failure varies slightly from one sample to the next, and the time to failure varies a lot with a small variation in voltage.

We characterized the time to failure for devices submitted to a step voltage. The voltage across the outer resistor of a device is increased from 0V to a value causing failure (35V and higher). By measuring the voltage across a resistor placed in series with our device, we can detect when the current drops to zero and measure the time it takes for the device to fail.

Figure 4-28 shows oscilloscope captures of the source voltage and the voltage across the series resistor for step voltages of 40V, 50V and 60V.

![Figure 4-28](image)

The time to failure is of the order of a millisecond, and decreases with step voltage (see Figure 4-29 Left). Moreover, there is a linear relationship between the voltage squared and the inverse of the voltage (see Figure 4-29 Right). This is consistent with the hypothesis that the failure happens when the resistor reaches a specific temperature.

The heat flow equation governing the temperature $T$ of the resistor is given by:

$$C_T \frac{dT}{dt} = \frac{V^2}{R} - \frac{T}{R_T},$$

where $V$ is the voltage, $R$ is the electrical resistance and $R_T$ the thermal resistance of the device, and $C_T$ is its thermal capacitance [16].
For large voltages, the conduction can be neglected, and the equation simplified to: \[
\frac{dT}{dt} = \frac{V^2}{C \cdot R_0 (1 + \alpha T)},
\]
where \( R_0 \) is the initial electrical resistance of the device and \( \alpha \) is the Temperature Coefficient of Resistance of the metal film defined by \( R(T) = R_0 (1 + \alpha T) \).

The solution to this equation is: \[
T + \frac{\alpha}{2} T^2 = \frac{V^2}{C \cdot R_0} t + A,
\]
where \( A \) is a constant. If we assume that the resistor fails when reaching the specific temperature \( T_{\text{fail}} \), then the time to failure \( t_{\text{fail}} \) and the failure voltage \( V_{\text{fail}} \) are related by \( V_{\text{fail}}^2 t_{\text{fail}} = \text{cste} \).

![Figure 4-29: Plots of the time to failure as a function of step voltage (Left) and the inverse of the failure time as a function of the voltage squared (Right).](image)

The temperature at failure can also be calculated from the measured resistance variation of the device, and is found to be similar regardless of the voltage (see Figure 4-30 Left). The current level is found to differ for different voltages (Figure 4-30 Right), confirming our previous findings that the current density is not a determinant cause of failure.

![Figure 4-30: Temperature and current density at failure as a function of step voltage.](image)
**Effect of Ta adhesion layer thickness**

To learn about the role of the tantalum adhesion layer in the failure, we fabricated samples with 50 nm of tantalum instead of 10 nm.

Figure 4-31 shows the temperature as a function of voltage for several samples with 10 nm and 50 nm adhesion layers (no membrane). We can see that the samples with a thicker adhesion layer fail at lower temperatures.

![Figure 4-31: Temperature versus voltage for test devices with 10 nm and 50 nm Ta adhesion layers.](image)

![Figure 4-32: SEM pictures of metal lines after an 80V voltage step with 10 and 50nm Ta thicknesses.](image)
Figure 4-32 and Figure 4-33 show a comparison of the metal lines morphologies after self-heated failure of the outer resistor for samples with 10 nm and 50 nm Ta adhesion layer thicknesses. More degradation can be seen on the samples with the thicker adhesion layer after degradation. The samples don’t have membranes, so the inner resistor is not heated to as high temperatures as the outer one, but the difference in degradation can also be seen on the inner metal lines. This is consistent with reports that a thicker tantalum adhesion layer enhances high temperature degradation in Ta/Pt films [6].

**Anneals in nitrogen ambient**

We annealed some of the samples in nitrogen prior to their testing in air. This has previously been reported to delay high temperature degradation of Pt films [10].

We measured the resistance of the resistors annealed in air and annealed in nitrogen. We used a probe station with a heated chuck that can be heated up to 200°C to measure the Temperature Coefficients of Resistance (TCR) of the films. Figure 4-34 shows the resistances measured as a function of the chuck temperature. Figure 4-35 shows the normalized resistances as a function of temperature.

The normalized resistance $\frac{(R - R_0)}{R_0}$ is related to the temperature by:

$$\frac{(R - R_0)}{R_0} = \alpha(T - T_0)$$

where $R_0$ is the resistance at the initial temperature $T_0$, $R$ is the resistance at the temperature $T$, and $\alpha$ is the TCR.

The slope of a line on Figure 4-35 is the TCR of the corresponding metal film.
Figure 4-34: Resistance of the outer resistor as a function of the chuck temperature for different films (10 and 50 nm Ta adhesion layer, anneal in air and in nitrogen).

Figure 4-35: Normalized resistance as a function of the chuck temperature for different films.
The resistance of the samples increased after anneal in nitrogen, by a factor of 2 for the 10 nm Ta samples and a factor of 2.5 for the 50 nm samples, compared to a resistance of about 165 Ohms before anneal (see Figure 4-16 and Table 4), whereas they had decreased after anneal in air.

The TCR of the metal stacks decreased as summarized in Table 5. This effect is also more pronounced in the case of the thicker Tantalum layer. The decrease in TCR could be due to the formation of tantalum nitride as nitrogen diffuses through the platinum and then reacts with the tantalum layer. Tantalum nitrides can have negative TCRs [14, 15].

<table>
<thead>
<tr>
<th>Sample Description</th>
<th>TCR $\alpha$ (K$^{-1}$)</th>
<th>$1/\alpha$ (Kelvins)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 nm Ta annealed in air 1 hour at 700°C</td>
<td>0.0033</td>
<td>301</td>
</tr>
<tr>
<td>50 nm Ta annealed in air 1 hour at 700°C</td>
<td>0.0034</td>
<td>292</td>
</tr>
<tr>
<td>10 nm Ta annealed in nitrogen 1.5 hour at 600°C</td>
<td>0.0011</td>
<td>905</td>
</tr>
<tr>
<td>50 nm Ta annealed in nitrogen 1.5 hour at 600°C</td>
<td>0.0010</td>
<td>1045</td>
</tr>
</tbody>
</table>

Table 5: Temperature Coefficient of Resistance for Ta/Pt films annealed in air or nitrogen

Figure 4-36: Temperature versus voltage for test devices with 10 nm and 50 nm Ta adhesion layers with and without a post-fabrication anneal in nitrogen.
We then tested the resistors in air by passing current in the outer resistor and increasing it until failure. Figure 4-36 shows the temperature as a function of voltage calculated using the previously measured TCRs.

For the 10 nm Ta samples, the failure conditions are similar after an anneal in air and an anneal in nitrogen. For the 50nm Ta samples, the failure temperature is significantly lower for the nitrogen anneal. The resistance also decreases at high temperature before failure for the 50nm Ta sample annealed in nitrogen.

We didn’t measure the failure conditions of non-annealed samples because the electrical characteristics of non-annealed resistor vary as the resistor temperature increases, and it isn’t possible to measure temperature using the TCR of the film.

When self-heating the resistors in air, the 50nm Ta adhesion layer sample showed a lot more degradation that the 10nm Ta one, as shown on Figure 4-37. The physical damage around the failure spot is similar for samples failed after anneals in air and in nitrogen (See Figure 4-39). However, when the sample is not annealed prior to testing, the metal degradation next to the failure spot is worse. Figure 4-38 even shows a loss of adhesion of the metal film to the substrate in the case of a 10 nm Ta layer (top left).

Figure 4-37: Images of resistors with 10 nm (top) and 50 nm (bottom) Ta layer, after anneal in nitrogen ambient and self-heated failure in air.
Figure 4-38: SEMs of failed devices that hadn’t been annealed before testing.

Figure 4-39: SEMs of failed devices that had been annealed before testing in air and in nitrogen.
Alumina capping layer

Previous work on Ta/Pt films [10] has shown that Ta doesn’t react with the underlying SiO₂, and that Ta gets oxidized during high temperature anneals in O₂ but doesn’t diffuse into the Pt layer. O₂ and N₂ can diffuse through the platinum layer and react with the Ta adhesion layer. Depositing a capping layer on top of the platinum layer could help reduce the heater degradation by preventing oxygen from getting through the platinum layer.

We deposited a sputtered alumina capping layer on top of some heaters, after the chips had been fully fabrication. We used aluminum foil as a shadow mask to deposit alumina on top of the resistors on the membrane but mask part of the contact pads. On Figure 4-40 left, alumina is seen in the center of the chip while the probes connect to the metals pads.

Figure 4-40: Optical microscope picture of an alumina capped sample. Left: picture of the chip showing the round area where alumina is deposited. Right: picture of the membrane area after failure of the outer resistor.

Figure 4-41 shows the resistance versus current characteristics for samples with and without alumina. Both for samples on membranes and without membranes, there is no significant difference in the failure conditions between samples with and without an alumina capping layer.

The failed resistor look more damaged than samples without alumina. The alumina layer is damaged, and the failure spot is very long for samples without a membrane (Figure 4-42 , left). For samples on a membrane (Figure 4-42, right), the alumina layer is cracked between the metal lines. This is consistent with a previous report that alumina sputter-deposited on top of a Ta/Pt layer caused adhesion problems at high temperatures due to shear stress between the Al₂O₃/Pt/Ta layer and the substrate [10].
Figure 4-41: Resistance versus current characteristics for test devices with and without membranes and with and without an alumina capping layer.

Figure 4-42: SEM pictures of failed alumina capped samples. Left: no membrane, right: membrane.
4.5 Summary of heater degradation study

Possible failure mechanisms

Previous studies have determined that agglomeration is the main high temperature degradation mechanism for Pt thin films [6, 10]. However, when self-heating a platinum resistor to failure, the timescale of degradation is much shorter than that of agglomeration. We will now summarize the findings of the previous section and draw conclusions regarding the mechanisms of degradation in our test devices.

Electromigration is sometimes mentioned as a possible failure mechanism in platinum heaters. However, we found that our test devices failed at different current levels depending on the conditions, but always for the same range of temperatures. Therefore, we conclude that the current density is not determinant for failure, and that the failure is not caused by electromigration. This is consistent with the fact that the current density in the devices is of the order of $10^{10}$ A.m$^{-2}$ ($10^6$ A.cm$^{-2}$), and that damage by electromigration at these current density levels would occur on a much longer timescale.

The temperature of the thin film appears to be the most important factor governing failure: the devices fail when reaching a specific range of temperatures for otherwise differing conditions. Also, the failure of devices on a membrane happens in the middle of the membrane, which is the point of highest temperature on the heater.

The melting points of bulk Pt and Ta are 1768 °C and 3017 °C respectively. Ta$_2$O$_5$ has a melting point of 1872°C. The lowest temperature eutectic between Ta and Pt is 1760°C [17]. Our measurements found that the resistor average temperature is on the order of 700°C at failure. Using simulations modeling the metal film as uniform, we calculated that this corresponds to a maximum temperature on the metal resistor of about 1100°C. These simulations don’t take into account the fact that the temperature can locally be much higher. For example, if part of the film delaminated from the substrate, this part would be thermally isolated from the substrate, and its temperature would increase. Once a part of the metal line melts, the effective width of the line is reduced, and the current density in the rest of the line increases, increasing the metal temperature. It is therefore possible for a hot spot to cause a failure spot interrupting the metal line. The morphology of the edges of failure spots and the presence of beads in and around the failure spots
seem to point to a melting phenomena.

Other possible failure mechanisms include interlayer diffusion, interlayer reaction and stress-induced morphological changes.

We observed that when a thicker Ta adhesion layer was used, the surface morphology degradation around the failure spot was worse and the failure temperature was lower than for a thinner Ta layer, although this effect was not very significant for samples annealed in air. This suggests that the adhesion layer plays a role in the failure.

It has been previously found that tantalum doesn’t diffuse into an overlying platinum film [10] and doesn’t react with an underlying SiO₂ layer at temperatures below 1000°C during vacuum annealing [18]. Tantalum does not form eutectics with platinum and silicon below 1635 and 1400°C respectively [6]. However, oxygen is found to diffuse through the platinum layer and oxidize the tantalum layer [10]. Therefore, one of the ways that the adhesion layer can contribute to failure is by getting oxidized when the metal film is heated (and maybe nitridized in a nitrogen environment). It has been shown that compressive stresses develop in tantalum films during oxidation [1, 19] and can result in films peeling from the substrate. Ta/Pt films have been found to be tensile as deposited in our facilities evaporator [6]. The compressive stresses in the Ta adhesion layer when it gets oxidized could be responsible for the degradation and blistering seen in the resistors, and loss of adhesion of the metal film to the substrate could be at the origin of the creation of the failure spots.

**Comparison between test device and MoJet2 degradation**

Before we apply the findings of the test device to the MoJet2 heater, we need to consider the differences between the two devices and see if they likely have the same failure mechanism.

There are several geometry differences between the two devices. The membrane is smaller on the MoJet2 device: 400 x 400 microns instead of 1 mm x 1 mm for the test device. The thinner part of the resistor is wider for the MoJet2 device: 50 microns wide instead of 20 microns wide for the test device. And there are no pores on the test device.

The smaller size of the membrane makes it stiffer, and therefore there is less stress relief than for the test device. This could increase the role of stress in the failure. We saw
some evidence of deformation of the membrane (see Figure 4-43). The permanent deformation seen from the back side of the membrane likely happens due to the high temperatures reached locally during the heater failure, as can be seen on the rightmost pictures. However, this shows that stress might play more of a role in the failure of MoJet2 heaters than in the failure of test devices. Some of the failure spots on MoJet2 chips start at the corners in the metal layer, this could be due to stress concentration at the corners, and indicate the role of stress in assisting in the failure.

![Figure 4-43: Pictures of permanent deformations of MoJet2 membranes after failure. Left: SEM picture showing wrinkles on the silicon membrane and deformation of the central area comporting the pores. Center: Pictures of the front side after failure (top), and back side before (middle) and after (bottom) failure of a MoJet2 device. Right: Front side (top) and back side (bottom) pictures of a MoJet2 membrane after failure.](image)

<table>
<thead>
<tr>
<th></th>
<th>MoJet2 resistor on membrane</th>
<th>Test resistor on membrane</th>
<th>Test resistor no membrane</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current density at failure</td>
<td>7-8 $10^{10}$ Am$^{-2}$</td>
<td>2-2.5 $10^{10}$ Am$^{-2}$</td>
<td>~5.5 $10^{10}$ Am$^{-2}$</td>
</tr>
<tr>
<td>Temperature (from R) at failure</td>
<td>~600°C</td>
<td>~700°C</td>
<td>~700°C</td>
</tr>
<tr>
<td>Calculated maximum temperature at failure</td>
<td>~950°C</td>
<td>~1100°C</td>
<td>~1050°C</td>
</tr>
</tbody>
</table>

Table 6: Comparison of failure conditions for MoJet2 and test devices.

Table 6 and Figure 4-44 show a comparison of failure conditions for MoJet2 and test
devices heaters annealed in air at 700°C.

The current density level is of the same order for the two devices. Since current density is not a significant factor in the failure of test devices, we can assume that it is not significant for MoJet2 failures either.

The failure temperatures are lower by about 100°C for MoJet2 heaters. This suggests that some factor other than temperature is assisting in the failure, for example stress.

![Figure 4-44: Comparison of average temperature at failure for MoJet2 and test devices](image)

Figure 4-44: Comparison of average temperature at failure for MoJet2 and test devices

Figure 4-45 shows that the morphology of the metal film around the failure spot is similar for test device resistors and for MoJet2 resistors with no anneal prior to failure.

![Figure 4-45: SEM of test device (left) and MoJet 2 (right) resistor after failure (no initial anneal).](image)
Possible improvements to the MoJet heater

We can now conclude on how to modify the MoJet2 chip design to increase the maximum temperature it can reach.

Since the current density level in the heater is not determinant for failure, it is not necessary to redesign the heater to decrease current concentration. However, the corners might be creating stress concentrations and reduce the temperature of failure, so that a heater design that minimizes stress concentrations might reach a higher maximum temperature.

Annealing the devices before self-heating use might increase their temperature range [10]. However the effects of ambient, temperature and duration of anneal need to be studied further, since the nitrogen anneal we performed affected the performance of the heaters negatively compared to an anneal in air, which is opposite to previous findings on high temperature degradation [6].

We showed that increasing the tantalum adhesion layer thickness reduced the temperature range. A thickness of 10 nm is usually considered optimal for the adhesion layer [6, 10]. Exploring the performance of pure platinum films fabricated using techniques described in [10] to get good adhesion to the substrate without the use of an adhesion layer could be valuable. Increasing the thickness of the platinum layer would also probably increase the temperature range [6, 10], although we were not able to test this due to limitations of our e-beam evaporator setup.

Protecting the platinum film with a capping layer preventing oxygen diffusion to the Ta adhesion layer would likely increase the temperature range of the device. However, we found than sputtered alumina did not have the expected beneficial effect as a capping layer. Other materials would need to be evaluated for this use. Silicon nitride doesn’t work as a passivation layer: the high deposition temperature of LPCVD silicon nitride causes the platinum film to agglomerate before being passivated [10], and PECVD silicon nitride reacts with the platinum film at elevated temperatures [6, 20]. Evaporated alumina would be a good candidate since it increased the resistance of Ta/Pt films to agglomeration, by preventing oxygen from diffusing to the adhesion layer [6].

If much higher temperatures need to be reached, it might be necessary to explore other materials than platinum. Platinum alloys with Ir, W or Rh are good candidates because
they have higher melting points than Pt, they don’t form low melting point eutectics with Pt, and precipitates forming in the grain boundaries of these alloys prevent grain boundary diffusion of reactive gases (like oxygen) [10]. Platinum-iridium heaters with a tantalum adhesion layer were found to exhibit a longer lifetime than Ta/Pt heaters under accelerated aging tests [12]. However, experiments with PtW and PtIr showed that tungsten oxidizes throughout the Pt-layer at temperatures around 400 °C and the formed oxide sublimates, leaving tungsten-free porous Pt. Iridium also oxidizes, and above 900°C this Ir-oxide is volatile [20]. Therefore these alloys would need to be capped by a layer preventing oxygen contact to the layer.
References


5. Conclusion

Principal accomplishments

This thesis provides a study of a new fabrication technique for patterned organic films. The impact of materials and structures used for the MEMS printheads enabling the techniques was presented. Four main contributions of the thesis are identified below:

1. Demonstration of MEMS devices enabling the first evaporative printing of organics:

One of the contributions from this thesis work to the field of organic optoelectronic devices fabrication is to prove the feasibility of evaporative printing of small molecular organic materials at resolutions of the order of 800 dpi. We demonstrated that MicroElectroMechanical Systems can be used to pattern organic thin films in a way that combines the advantages of ink-jet printing and thermal evaporation.

2. Design, modeling and fabrication of a compact electrostatic actuator:

One of the contributions of this thesis to the field of MEMS is the design and fabrication of a compact electrostatic actuator that can be used to actuate a microshutter, with an operating frequency of 1 kHz, operating voltage of 90V for a displacement of 30 μm, with a size of 100 μm by 400 μm. We also showed that a thermal actuator would not be suitable for use in a vacuum. Compact actuators enable the fabrication of dense arrays of microshutters. For the printing of organic devices, arrays of nozzles would allow high-throughput printing on large areas.

3. Proof of concept demonstration of a microevaporator chip:

Another contribution to the field of MEMS is the design and fabrication of a microevaporator for molecular organics. This extends the field of applications for MEMS
as microfabrication tools. We demonstrated the feasibility of using an array of pores in a membrane to capture molecular organic materials delivered by a solvent and an integrated microheater to release them by evaporation onto a substrate. The demonstration of this printing principle is also a considerable contribution to the field of organic devices fabrication, since it provides a fabrication technique suitable for the ambient printing of devices on low-cost substrates, without the limitations of ink-jet printing due to the drying of solvent on the substrate.

4. Investigation of the failure of platinum thin films microheaters:

This thesis also provides a study of the failure of thin film platinum heaters on silicon membrane and chips. Such heaters are widely used in MEMS applications such as microhotplates, and the conclusions of the study are therefore a useful contribution to the field of MEMS. We proved that the failure of our heaters was predominantly due to temperature and not linked to current density levels. We studied the effect of different parameters on the failure and provided directions for improvement.

Limitations and Future Work

Although the MoJet 1 printing system is not very compact and material efficient when used in a vacuum chamber with a conventional evaporation source for the materials, it might be possible to improve it by integrating it with a micro-evaporator or by delivering the material with a stream of inert gas at ambient pressure. Our experiments showed that the printhead design could be improved by integrating anti-crash structures above the microactuator to decrease the damage to the suspended structure during printing and using anti-stiction coatings or a heater on the microshutter for in-situ cleaning. Integrating microshutters into arrays would be necessary for practical applications.

In future work concerning the printing of molecular organic materials with the MoJet2 printhead, it would be interesting to learn more about the physical mechanism of the printing. This could give insight into how a number of modifications of the printhead
design would affect the printing and the printed pixel size and thickness profile.

For example, it might be possible to get a more uniform thickness of the pixel by varying the position and sizes of the pores. Instead of a square array of identical and regularly spaced pores, having a round array with smaller pores or more densely packed pores at the edge of the array might lead to a more uniform pixel thickness.

Heating the silicon membrane from the back instead of the front side could decrease the amount of material that is evaporated backwards instead of towards the printing substrate. Changing the sidewall angle of the pores so that they are smaller on the back side of the membrane might also help in this regard. Investigating different materials and pores fabrication processes might enable more control over the pores array characteristics.

Arrays of MoJet2 nozzles would need to be integrated for practical applications of the printing technique. Each nozzle, or array of pores, needs to be on its own membrane to be individually addressable. The membranes also need to be sufficiently thermally isolated from each other so that heating up one doesn’t affect the temperature of another too much. The size of the membranes and the separation between them will limit the maximum density of nozzles; however, reducing the membrane width further than 400 μm would decrease the thermal insulation between the heated region and the outside of the membrane and increase the power consumption, temperature gradients and thermal stresses. Other materials could be investigated for the membrane, to provide more thermal insulation and to be more resistant to high temperatures.

Another challenge of the MoJet2 technique is the integration of the ink-jet nozzle with the MoJet2 chips. The quantity of ink delivered to the porous region as well as the solvent drying step between the ink-jet delivery and the thermal evaporation influence the printing and have to be controlled in order for the printing to be reproducible.

It is also possible that the MoJet2 printing technique can be used to print other materials than small molecule organic material. The main difficulty in testing this would be to find a way to deliver the material to the pores. At this point it is difficult to say how the printhead would need to be modified for printing of other materials, except for extending the temperature range. In that regard, we saw that exploring post-fabrication anneals and capping layers could lead to increased temperature range.
Appendix A: Process Flows

Fabrication Process for MoJet1 chips

Starting wafers: 6” SOI wafers

1. RCA clean (TRL rca)
2. Thermal oxidation (TRL, Tube A2) Thickness 0.5 μm: 85 min O₂
3. Photolithography
   HMDS vapor deposition (TRL HMDS)
   Spin standard thin photoresist 1 μm at 3000 rpm (TRL coater)
   Pre-bake 30 min 95ºC (TRL pre-bake)
4. Mask 1 (SOI)
   Exposure for 2 sec (TRL EV1)
   Develop: 55 sec (TRL photo-wet)
   Post-bake: 30 min at 120 ºC (TRL post-bake)
5. Etch SiO₂ 0.5um (ICL AME5000 chamber A)
6. Piranha clean 10 min (TRL acid-hood)
7. Photolithography
   Dehydrate 30 min plus HMDS vapor deposition #3 (TRL HMDS)
   Spin thick photoresist AZ9260 (TRL coater): 60s at 2k rpm, 10s at 3k rpm
   Soft bake 60 min 95 ºC (TRL pre-bake)
8. Mask 2 (FRONT)
   Exposure for 4 x 15 sec with 15 s intervals (TRL EV1)
   Develop 1 min 30 to 2 min (TRL photo-wet)
   Spin dry
   Cover alignment marks with thin photoresist and teflon tape
   Hard bake 30 min at 95 ºC (TRL pre-bake)
9. Etch oxide 0.5 microns (ICL AME5000 chamber A)
10. Etch Si (TRL sts2), 11 microns, Recipe STSSHALLOW_A
11. Etch SiO₂ (ICL AME5000 chamber A), 3 microns
12. Etch Si (TRL sts2) 50 microns, Recipe OLE3
13. Ash 30 min to 1 hour (TRL asher)
14. Piranha strip Photoresist (TRL acidhood)
15. RCA clean
16. Grow oxide 0.1 micron (TRL tube A2)
17. Photolithography on back side
   HMDS vapor deposition #3 (TRL HMDS)
   Spin thick photoresist AZ9260 at 1500 rpm (TRL coater)
   Pre-bake 60 min 90 °C (TRL pre-bake)
18. Mask 3 (BACK)
   Exposure for 20s (TRL EV1)
   Develop 3 min (TRL photo-wet)
   Post-bake 30 min at 90 °C (TRL pre-bake)
19. Coat frontside with 3 layers thin photoresist (TRL coater)
   Pre-bake 60 min 90 °C (TRL pre-bake)
20. Etch Oxide in BOE (1.5 um) (TRL acidhood)
21. Etch Si backside (TRL stds2) recipe OLE3 ~565 microns (target mount to 6” Quartz wafer)
22. Piranha dismount and Photoresist strip (TRL acid-hood)
23. Separate dies (ICL DieSaw)
24. Timed HF vapor etch of oxide (Schmidt Group Lab)

**Fabrication Process for MoJet2 chips with oxide barrier layer**

Starting wafers: 6” SOI wafers

1. RCA clean (TRL rca)
2. Thermal oxidation (TRL, Tube A2)
3. Photolithography
   HMDS vapor deposition #5 (TRL HMDS)
   Spin coat image reversal photoresist (TRL coater)
   Bake 30 min at 95°C (TRL pre-bake)
4. Mask 1 (HEATER)
   - Exposure 1.5 s (TRL EV1)
   - Bake 30 min at 95 °C (TRL pre-bake)
   - Flood exposure 1 min (TRL EV1)
   - Develop (TRL photo-wet-L)
5. Descum 7 minutes (TRL asher)
6. Deposit 0.1 kA Ta and 0.15 microns Pt (TRL e-beamAu)
7. Lift-off photoresist in acetone (TRL photowet-Au)
8. Photolithography
   - HMDS vapor deposition (TRL HMDS)
   - Spin standard thin photoresist 1 um at 3000 rpm (TRL coater)
   - Pre-bake 30 min 95°C (TRL pre-bake)
9. Mask 2 (PORES)
   - Exposure for 1.6 sec (TRL EV1)
   - Develop: 1 min 10 sec (TRL photo-wet, red dot)
   - Post-bake: 30 min at 120°C (TRL post-bake)
10. Etch oxide in BOE (TRL acidhood red dot)
11. Etch silicon 20 microns (TRL sts1, recipe ole3, 7 to 12 minutes)
12. Ashing 30 min to 1 hr (TRL Asher - red dot)
13. Photolithography on back side of wafer (TRL – red dot)
   - HMDS vapor deposition #3 (TRL HMDS)
   - Spin standard thick photoresist @2k rpm (TRL coater)
   - Bake 20 min at 95C after first coat.
   - Spin standard thick photoresist @3k rpm (TRL coater)
   - Pre-bake 60 min 95°C (TRL pre-bake)
14. Mask 3 (BACK)
   - Exposure for 5 x 15 s with 15 s intervals (TRL EV1)
   - Develop: ~2-4 min (photo-wet, red dot)
   - Cover alignment marks with thin photoresist and teflon tape
   - Post-bake: 30 min at 95°C (TRL post-bake)
15. Deposit C₄F₈ on front side of wafer (TRL sts1, polymer recipe, 10 min)
16. Cover front side with blue die saw tape
17. Etch silicon ~500 microns from back (TRL sts1, recipe ole3)
18. Remove tapes
19. Ashing 60 min – 3 hrs (TRL Asher - red dot)
20. Protect front of wafer with photoresist (paint using Q-tips)
   Bake 30 min at 120C (TRL postbake)
21. Etch oxide in BOE (TRL acidhood, red dot glassware)
22. Ashing 30 min – 2 hrs (TRL Asher- red dot)
23. Die saw (ICL diesaw)
Appendix B: Mask Layouts

MoJet 1: Mask 1 (SOI) version 1

Layout of the 4 different chips (each chip is 4.6 x 4.6 mm)

Details of the 4 actuators
MoJet 1: Mask 1 (SOI) version 2

Layout of the 4 different chips (each chip is 4.6 x 4.6 mm)

Details of the 4 actuators
MoJet 1: Mask 2 (FRONT)

Layout of the 4 different front side apertures

Details of the 4 different front side apertures (the smaller dimension is 25 microns)

MoJet 1: Mask 3 (BACK)

Layout of the 4 different back side apertures
MoJet 2: Mask 1 (HEATER)

Layout of the mask (7 inch x 7 inch plate)

Layout of the 9 different heaters
MoJet 2: Mask 2 (PORES)

Layout of 9 chips

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Detail of the pores region of the chip (pores are 2x2 microns)
MoJet 2: Mask 3 (BACK)

Layout of the mask (7 inch x 7 inch plate)

Layout of 9 chips
Test device: Mask 1 (HEATER)

Layout of the mask (7 inch x 7 inch plate)

Layout of one chip (4.6 mm x 4.6 mm)
Test device: Mask 2 (BACK)

Layout of the mask (7 inch x 7 inch plate)

Layout of one chip (4.6 mm x 4.6 mm)