A Design for an RGB LED Driver with Independent PWM Control and Fast Settling Time

by

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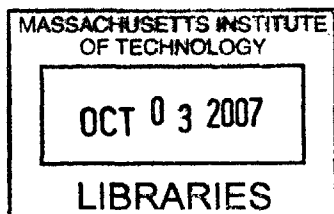   [John Killy, Senior Design Engineer]
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A Design for an RGB LED Driver with Independent PWM Control and Fast Settling Time

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Submitted to the Department of Electrical Engineering and Computer Science
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Abstract
A small sized and efficient method to power RGB LEDs for use as backlights in flat panel displays is explored in this thesis. The proposed method is to drive a parallel switched connection of LEDs with a single Average Mode Controlled buck regulator. Specifications for the switching regulator and control circuitry are described. The application circuit demonstrates current settling times between 7μs and 30μs at a switching frequency of 290kHz. Current settling is improved at higher switching frequencies, with settling times approaching a 2μs to 4μs range at 1MHz switching.

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Chapter 1 - Introduction

a. Display Technologies of Today

Flat panel televisions are no longer a luxury item. Today, the average television store can boast of an eclectic stock of High Definition (HD) televisions, Liquid Crystal Display (LCD) televisions, Plasma Screen televisions and Digital Light Processing (DLP) televisions, to name a few. Sales of flat screen TVs alone hit a $17 billion figure in 2005, and are projected to continue on an upward trend. This boom in the television business is only a microcosm of a greater innovation in the display industry. Besides TV sets, we enjoy very fine, life-like pictures off minute screens in PDAs, cell phones and other tiny consumer portables. These novel displays are expected to permeate business areas too; there is good reason to believe that medical imaging devices will be upgraded to these sharper displays, and so will computers, spectroscopes, microscopes, 3-D visual displays, holographic storage devices, and professional photographic devices.

The new display technologies make up for the deficiencies of CRT technology such as its bulkiness and poor contrast in large screens. These innovative screens also deliver digital television which CRT cannot provide. Though the new screens are all improvements to the CRT screen, they each have their own setbacks, and as a result, it is still early to select one technology as the overall best. That is why we still see many types of flat screens on the market. We discuss a number of these screen technologies below.

Thin, lightweight and silent, LCD screens run on low power and provide good text contrast. They also offer a wide viewing angle and low electromagnetic radiation. What's more, since 1999, the prices of LCD sets have been declining steadily, largely, as a result of improvement in the LCD manufacturing process. The negative aspects of LCD technology include poor image contrast. LCD technology cannot create rich black colors. Its inherent fixed resolution, limited peak brightness, caused by the fixed brightness of the backlight, and its notorious motion blur makes the viewing experience less than heavenly. The size-cost ratio unfortunately remains prohibitively high, even though this ratio is on a downward trend.

Plasma screens also have many advantages comparable to the LCD: wide viewing angle, as well as a flat and compact shape. Moreover, there is no flicker effect[1] in plasma screens. Additionally, its architecture has no need for a backlight or a projection of any kind, making for very thin (albeit heavy) devices. Plasma screens also emit rich colors that the LCD screens cannot match. That said, they do not come cheap.

The advantages of DLP technology include its light weight, high gamut of color, and excellent contrast ratios. Unfortunately, DLP screens require at least 12" - 24" depth. This renders the monitors bulky. Furthermore, in single chip DLP systems, there is the potential of having the "Rainbow Effect". This problem is unique to DLP. A rainbow forms briefly in the viewer's peripheral vision. It occurs when viewers rapidly shift their focus from a very bright area to a dark area.

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[1] Flicker is visible fading between image frames displayed on cathode ray tube (CRT) based monitor.

The use of LEDs in Displays

It is reported that replacing the fluorescent backlight with LEDs corrects the "rainbow effect" in DLP TVs [1]. Other screen manufacturers like Samsung and Acer are also installing LEDs as backlights in LCD screens, to improve (dynamic) contrast ratios and thereby enrich color production. Compared to CCFL backlit LCDs, LCD panels with LED backlights can easily be divided into subsections. The brightness of each subsection is controlled independently to produce many levels of brightness and with it, a high contrast ratio. LEDs also eliminate the warm-up time and color instability of screens since they have an instant turn-on. An additional advantage to consumers is that LEDs have longevity.

b. About this Thesis

i. Minimizing the settling time of a Multiple LED driver

The intention here is to design a compact and cheap way to drive LEDs for use in flat panel displays. The key feature of this compact, cheap LED driver is its fast current settling. Allow me to explain why this property is important.

If one could develop a single affordable and small-size LED driver that could drive many types of LEDs, i.e. LEDs of different current ratings and forward voltages, one could eliminate many LED drivers in the display, replacing them with a single circuit that switches among several LEDs. In order for this multiple LED driver to be useful, the output current must settle to its nominal value quickly. There is no point in using a multiple LED driver if the current settles slowly. This is because the colors of the

different LEDs will reach the requisite hue slowly. If the colors settle slowly such that we have to cycle through these LEDs at a frequency lower than 100Hz, the eye will be unable to blend the distinct colors. The ability to blend colors to form a wider spectrum of colors is lost. Evidently such an LED driver is inappropriate for lighting applications.

In the DLP screen for example, a driver could drive RGB LEDs in the backlight. In a given cycle (at a frequency higher than a 100Hz), the driver turns on the red LED for 30% of the time, the green LED for another 30% and the blue LED another 30%. Because the red, green and blue LEDs may require different forward voltages and current, our multiple fast settling LED driver must reset its output current and voltage quickly each time we switch between the LEDs. See Figure 1.1. When the red, green and blue lights reach the DLP chip, they are pulse-width modulated. The red light may hit the DLP chip first and is reflected onto the screen for the required amount of time to illuminate the right amount of red light. The green light may hit the DLP chip next and may be reflected for a different amount of time. The blue light then follows and may also be sent to the screen for a different duration. If the red color is reflected onto the screen longest, the resultant color appears reddish, if the blue light is reflected for the longest duration within a cycle, the resultant color appears bluish, and so on.
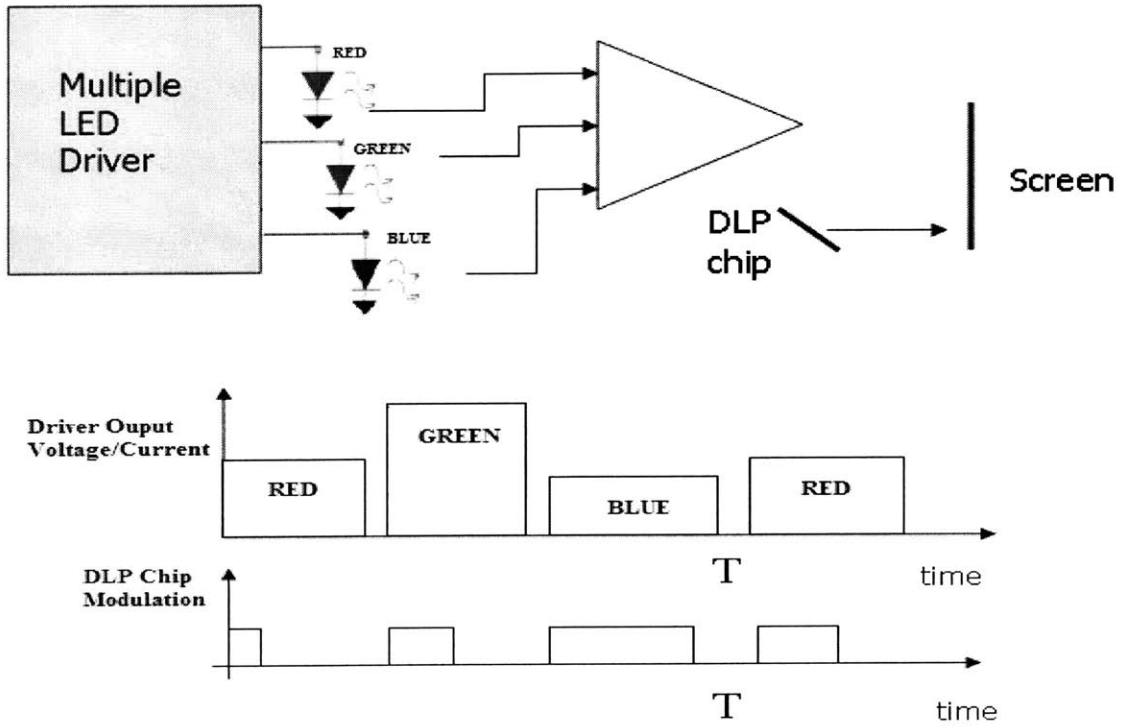
Figure 1.1: DLP incorporating the fast-current-settling multiple LED driver. Output voltage and output current are reset whenever we shift between LEDs. In the first cycle, a dominant bluish color is produced.

This technology is suitable only if the RGB currents settle fast, otherwise as Figure 1.2 depicts, we cannot cycle through the three primary colors at a rate faster than a 100Hz. The human eye will see the distinct red, green and blue colors, rather than one integrated color [2].
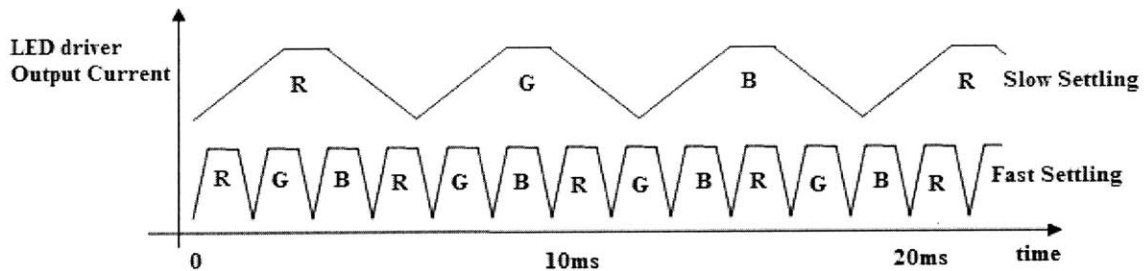
Figure 1.2: Fast settling output current allows faster frequency, a higher refresh rate and better contrast pictures on DLP screen.

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The benefits of using our small-size inexpensive multiple LED driver in DLP screens are plentiful. First, we eliminate the color wheel and all the mechanical circuitry involved in combining color. We shrink the size of the DLP screen as a consequence. We can also guarantee a longer life for the screen due to the longevity of LEDs. The screen runs on lower power because one, LEDs are more efficient than white lamps and two, because we eliminate the color wheel. The color wheel in DLP TV wastes a lot of energy in its operation. To create non-white colors, it filters out the unwanted color components of the white light. The light components that are filtered out are wasted in the form of heat energy. Also, if the output current settles very quickly, we can cycle through the LEDs at a frequency much higher than 100Hz. DLP manufacturers claim that there are many advantages associated with operating at higher frequencies [3]. That is why we place enormous emphasis on the fast current settling characteristic of our multiple LED driver.

ii. Other performance criteria

Traditionally, what we term as a multiple LED driver is in fact several distinct LED drivers packaged into one chip. This multiple driver is characterized by several distinct output ports illustrated by Figure 1.3. The idea is that if we could create a real multiple driver, that is, a driver with one output port serving multiple LEDs, we size down the LED driver and possibly its cost by a great margin. Compare the traditional multiple LED driver in Figure 1.3 to the proposed multiple LED driver of Figure 1.4.
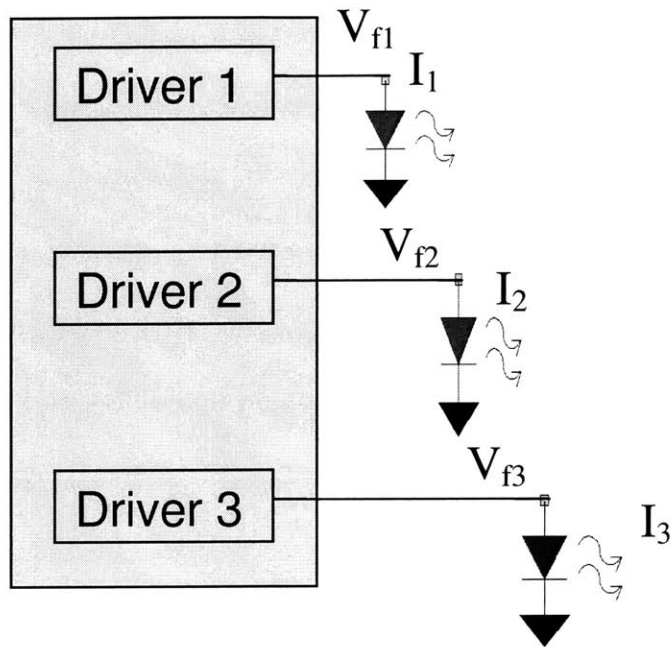
Figure 1.3: Traditional Multiple LED driver has distinct drivers encapsulated into one chip.
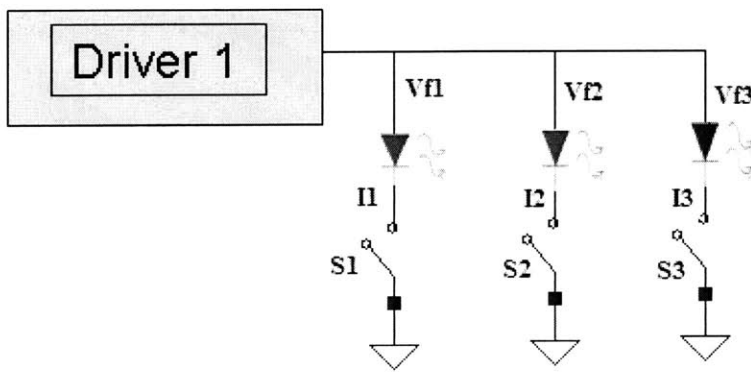
Figure 1.4: Proposed Multiple LED driver with one output port serving multiple LEDs.

In addition to a smaller sized solution, we seek a driver that is efficient and beats the efficiency or at least matches the efficiency of existing lighting solutions. The more efficient the system, the less costly it is to operate, since it expends less energy. The efficiency of the system also impacts the size of the solution. A grossly inefficient

lighting system will demand larger heat sinks and will make the screen very bulky and unattractive for use in flat panel displays.

We see this fast current settling multiple LED driver playing a major role in all applications that require fast settling multiple output currents. Its use is not limited to display applications.

iii. Thesis organization

Chapter 2 of this thesis presents an overview of several design strategies and considerations for multiple LED drivers.

Chapter 3 presents the specifications of the multiple LED driver.

Chapter 4 is a rigorous discussion of the design selected for the implementation of the multiple LED driver.

Chapter 5 describes methods used to test a prototype built from discrete components and presents a summary of the results obtained on the bench.

Chapter 6 summarizes the concepts learned from this thesis and proposes future work.

Chapter 7 is a bibliography of references cited in this thesis

Appendix I contains the circuit description in SPICE.

Appendix II contains the MATLAB code used to simulate the circuit.

Appendix III contains the PCB board layout of the prototype and the Bill of Materials.

Chapter 2- Overview of Design Approaches

a. Theoretical Solutions

There are a number of recommendations pertaining to fast transient DC/DC converters which apply to the design of the multiple LED driver of Figure 1.4, repeated here as Figure 2.1. In recent years, some designers have proposed means of increasing the bandwidth of the systems and some have even proposed changing the inherent topologies of the converters. We discuss a few of these schemes: switching at higher frequencies, multi-phase converters, the fast response double buck converter (FRDB), the average current mode control scheme and the peak current mode control method. In the next few pages, we examine each proposition closely to select the most suitable scheme for the work at hand - a compact and efficient fast current multiple LED driver.
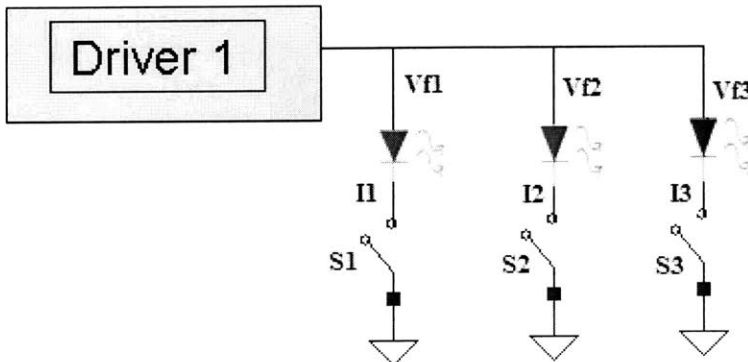
Figure 2.1: Proposed Multiple LED driver with one output port serving multiple LEDs.

Switching at higher frequencies

A high switching frequency means that the control loop of the system is able to correct errors more rapidly. The output current as a result will settle to the correct value quickly. Another benefit of switching at a higher frequency is a reduction in the output ripple.

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This means that one can get away with smaller and inexpensive filtering devices at the output node. Indeed, these advantages do not come at zero cost. Higher switching frequencies cost efficiency. Since some components' switch power loss are proportional to frequency, higher switching frequency translates to higher power losses. Also, when one switches at a higher frequency, one runs into noise coupling issues and the layout design is greatly complicated.

Multi-phase converters

Multi-phase converters work by interleaving more than one distinct converter operating out of phase with each other [4], [5]. The purpose is to reduce ripple on the output without using massive filtering elements at the output stage, which slow down the settling of the output current. By avoiding big inductors and capacitors, the output responds more quickly to changes in the system than it would otherwise. Multi-phase converters produce low output ripple and fast settling current. It is for among these reasons that the multi-phase synchronous buck converter has become the dominant topology for microprocessors [6]. Figure 2.2 below shows a two-phase buck converter.
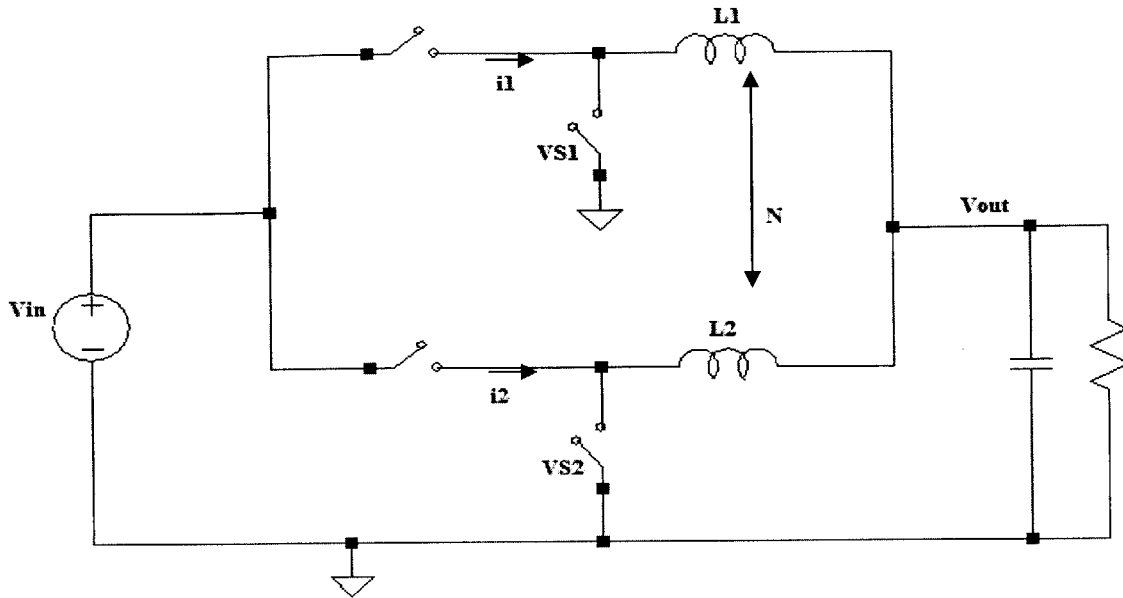
Figure 2.2: 2-phase synchronous buck converter. Adapted from [7].

Consider the two-phase converter of Figure 2.2. Assuming that the size of the inductors L1 and L2 are the same, and that the gate signals VS_1 and VS_2 are exactly 180 degrees out of phase, and that the system is operating near 50% duty cycle, the current through L1 and L2 will resemble that drawn in Figure 2.3. As shown in the picture, the resultant output current has only small ripple, with a fundamental frequency of twice the switching frequency of each power stage. For constant total energy storage, interleaving N stages reduces ripple current by a factor greater or equal to N and increases fundamental ripple frequency by a factor of N [4], [5].
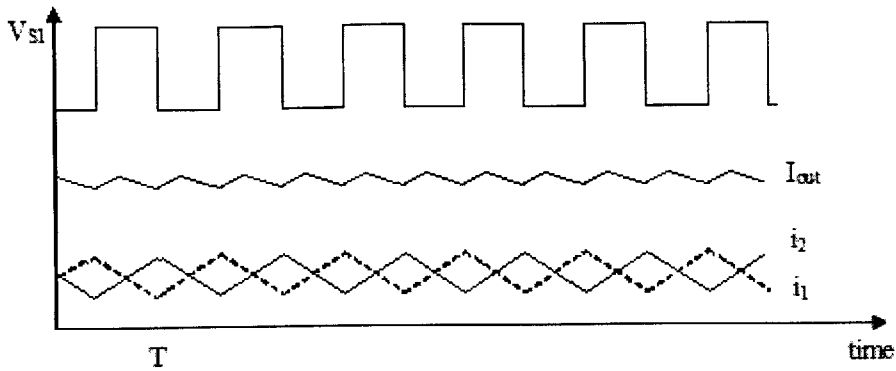
Figure 2.3: Waveforms of the 2-phase synchronous buck converter.

This implies in turn that the designer can generate an output current having a given ripple with reduced inductors and capacitors as compared to a single power stage. Moreover, because the individual inductors are small, one can slew the operating current quickly compared to a single buck converter with the same ripple current. Additionally, because we now have essentially two buck stages, we spread the power consumption across more converters. This distribution allows the chip to withstand larger total power consumption.

One problem with the multi-phase converters is that we add another layer of complication. That is to say, we have to carefully synchronize the gate signals to avoid an open at the input, significant delays, and uneven power sharing [8]. Our layout is also made complex. In this thesis, we focus on a single-phase design, but recognize that a multi-phase approach may be valuable in some applications.

Fast transient response dc/dc converter

Reference [9] considers a "Fast transient response" dc/dc converter. The fast transient response dc/dc converter is very similar to the 2-phase converter in that it employs two power stages. The difference is that while all the converter stages in a multi-phase

converter are identical, converters of the fast transient buck are not identical. The two converter stages in the "fast transient response" converter have different functionalities. The linear or main buck converter operates like a typical buck converter. The novel addition is the second "auxiliary" stage. What does it do? Because the output filter is a low pass filter, it removes all high frequency components at the output. By so doing, it limits fast transitions at the output. The purpose of the auxiliary stage is to inject extra current to speed up such transitions at the output, while maintaining low output ripple. See Figure 2.4 for a block diagram of the circuit.
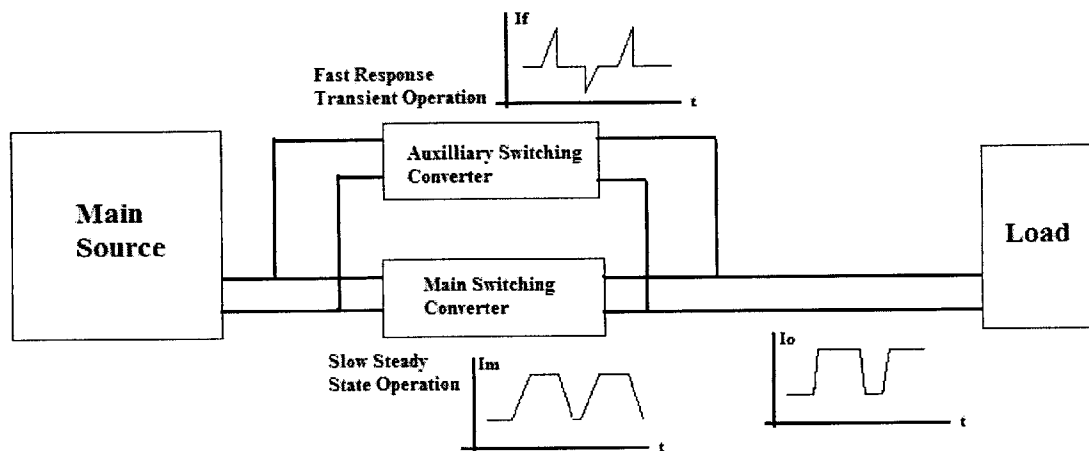
Figure 2.4: Basic structure and operation of FRDB converter. Adapted from [9]

The sum of the filtered output of the buck stage plus the injected current from the non-linear converter provides a fast transient, low ripple response at the output. In principle, if the two power stages operate independently of each other, there is no stability issue if each control loop is independently stable.

It should be recognized that the control of the auxiliary converter is not trivial. How much current should it inject or take out during a step of the output current? Since our

application calls for a variable output current step, the control of the auxiliary converter must be dynamic as well – a nontrivial exploit. For reasons of complexity, this design strategy is not considered further.

Average Current Mode Control

We have held a discussion of a few relevant topologies. Let us describe how the control scheme can influence the transient response of the driver. We first take a look at the Average Current Mode Control, (ACMC) [10]. ACMC is popular for its simple feedback technique. The control consists of two loops. There is a fast internal current feedback loop and a slower voltage feedback loop. The fast current feedback circuit measures a low-pass filtered version of the inductor current and compares it to an error signal generated by the slower voltage error amplifier. The signal from the current error amplifier is fed to a PWM comparator whose other input is a sawtooth ramp. This PWM comparator produces a pulsating signal. The duty ratio of this signal serves to modulate the output power. When output current is too low, the duty ratio of the pulse increases; as a result, the converter switch stays on for a longer time period, and consequently, the output power ramps up. When output current is too high, the converse occurs. Via this feedback, the circuit maintains output voltage and current at the prescribed value.
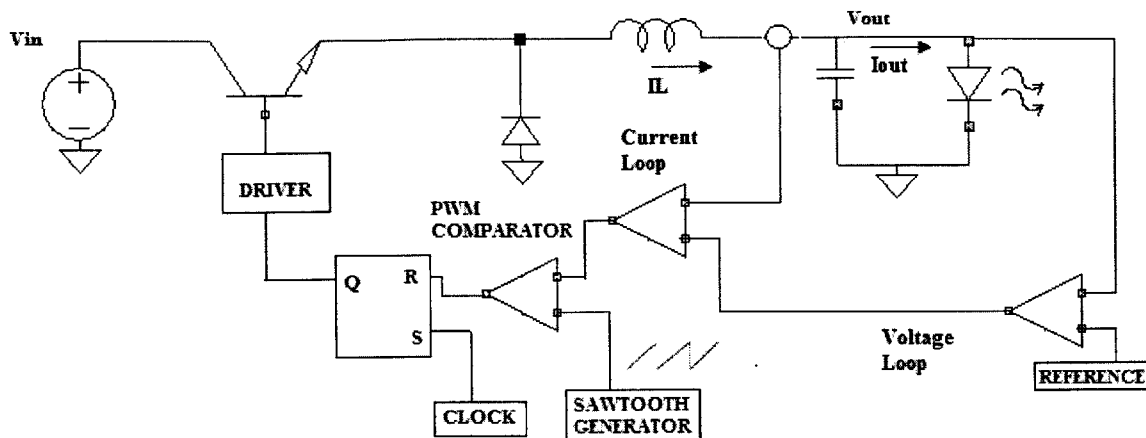
Figure 2.5: In this Average Current mode buck regulator, the error signal and a modulating ramp form a pulse-width modulator, which controls the buck switch.

In order to generate fast transient responses and accurate output, the control path is made fast by proper dynamic compensation of the (current) error amplifier. By providing full state feedback (of both inductor current and capacitor voltage) better dynamics are achievable than can be obtained with a voltage feedback alone.

Peak Current Mode Control

Similar to ACMC, under Peak Current Mode Control (PCMC) one utilizes feedback of both inductor current and capacitor voltage to improve dynamic performance. What differentiates the two modes is the origin of the modulating ramp. Under PCMC, the modulating ramp is a signal proportional to the buck switch current, or equivalently, the inductor current. Each cycle, the switch is turned on, and then turned off when the inductor (or switch) current reaches a peak value set by the voltage loop. An additional modification is that a compensating ramp is also sometime required to prevent subharmonic oscillations [11].
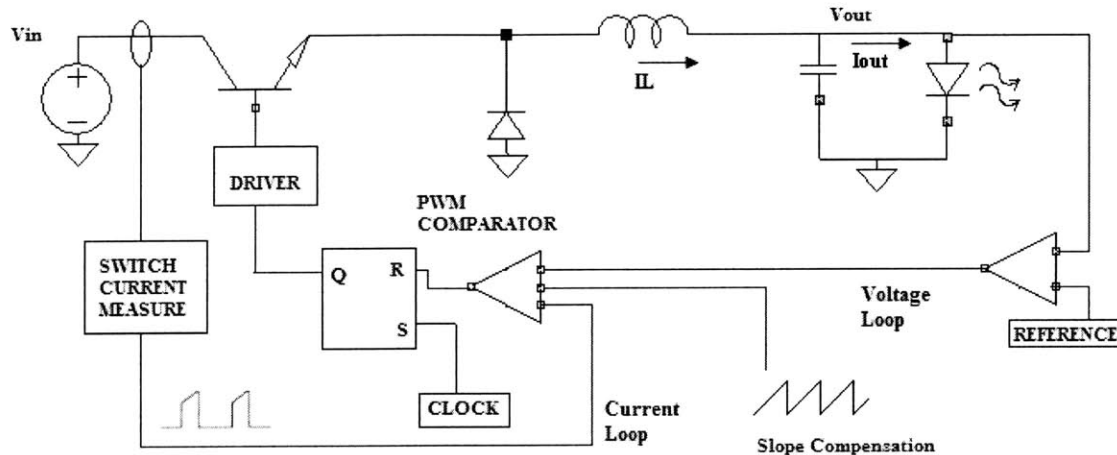
Figure 2.6: The principal difference between this current mode regulator and the voltage mode circuit is in the source of the modulating ramp. Adapted from [10].

Evidently, for PCMC to run correctly, it requires an accurate yet fast measurement of the inductor current to create the modulating ramp signal. This measurement is no trivial feat. One could capture the buck switch current. The mechanism draws on the fact that when the buck switch is on, the inductor current equals the switch current. Other measurement choices include placing a sense resistor in series with the inductor, a current sense transformer across the on-resistance of the switch, or a current mirror circuit coupled to the switch. Each of these methods requires a level shift to transpose the measured signal down to the ground reference for application to the PWM comparator, since the buck regulator modulating switch is floating. None of the switch's terminals is connected to ground. The source terminal of the switch is either at the input voltage potential when the switch is on or at approximately 0.7V when off.

One perceived advantage of Average Current Mode Control over Peak Current Mode control is noise sensitivity. As the comparator is driven from the wide-bandwidth current sense, there is the potential for noise to trigger the PWM comparator. Under Average Current Mode control, only a low pass filtered version of the current is sent to the PWM comparator, providing noise immunity. Conversely, however, Peak Current Control provides "instant" pulse-by-pulse current limiting, where Average Current Mode Control does not.

Another advantage of Average Current Mode Control over Peak Current Mode Control is accuracy. Since the output current is exponentially dependent on the output voltage in the LED driver application, it is extremely important that the reference voltage setting the output voltage is precise. Furthermore, because the multiple LED driver of Figure 2.1 is designed to drive many LEDs of different forward voltages, over different currents, the output voltage is expected to step to several different values. Thus, the reference voltage must accurately predict the output voltage needed for the many LED types and output currents. In order to keep the control scheme for the driver of Figure 2.1 simple, a single (current) loop control method is considered in which one directly regulates the average output current. Both the ACMC and PCMC if used, will be stripped of its voltage loop entirely. A one (current) loop ACMC control without the voltage loop, still regulates the average output current with remarkable accuracy. However, PCMC without its voltage loop, regulates the *peak* output current. Additional circuitry needs to be added to remove the peak to average current error. This supplementary circuit further complicates the PCMC control circuitry.

Table summarizing tradeoffs

Property\Topology	Multi-phase	FRDB
Transient Response	Fast	Fast
Efficiency	Moderate	Moderate
Ripple Current	Depends on number of phases and duty cycle.	Low
External Component count	High	High
Die size	Big	Big
Total cost	High	High

Property\Control	ACMC without voltage loop	PCMC without voltage loop
Transient Response	Fast	Fast
Noise sensitivity	Low	High
Accuracy	High	Low

Table 2.1: Tradeoffs of theoretical solutions.

Considering our evaluation of the solutions at hand, it appears that the most likely successful candidate is a single synchronous buck power stage employing average current mode control. The reason behind this choice is that a single buck power stage will enable the basic approach to be tested out with the greatest simplicity. This could be extended (e.g. to a multiphase interleaved design) later if higher performance is deemed necessary. ACMC provides the best combination of precision, fast transient response and low noise.

b. Commercial Solutions

Here are some examples of ways that manufacturers design power converters to generate multiple fast settling currents.

Separate topology

One solution in industry is to drive the individual LEDs with separate converters from one power supply. There are n converters for n LEDs. Each converter provides the right amount of current to its corresponding LED. This topology does not demand fast settling currents, since the LEDs are on the entire time that the driver is on. The problem with this solution is that the size of the die is large and numerous inductors are required. Consequently, it is an expensive solution.
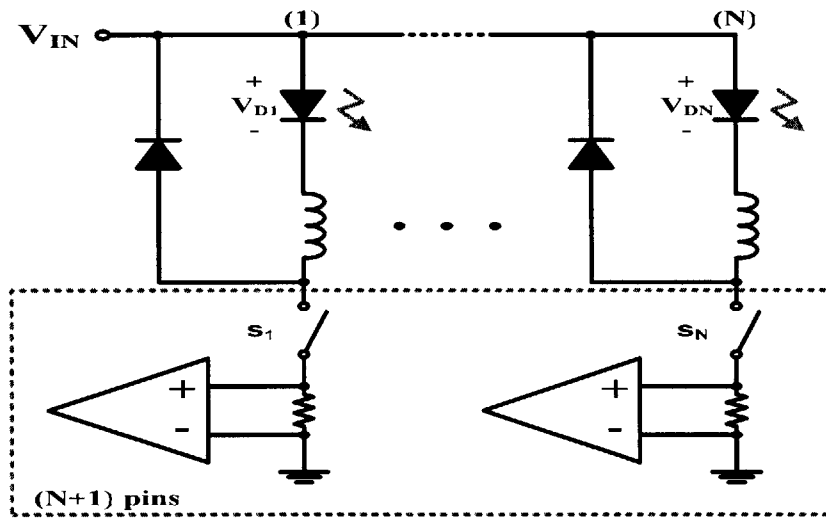
Figure 2.7: LEDs driven by separate converters.

Parallel topology

Here, one buck stage serves one distinct output node connected to multiple LEDs. The output voltage is modulated, but the different currents are set by the resistors added onto the LED strings. The resistor size controls the voltage across the LED, and by so doing, it fixes the LED current.
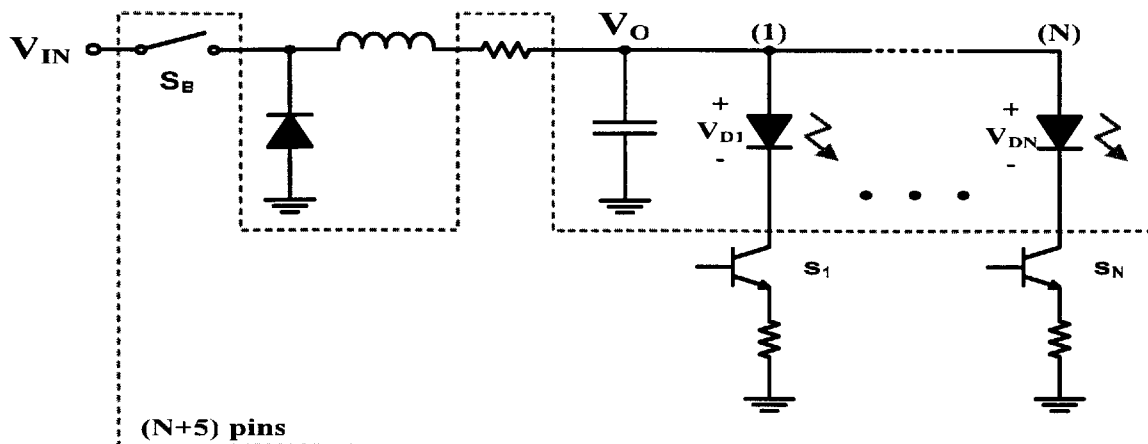
Figure 2.8: Parallel topology

Gate signals sent to switches S_1 through to S_n turn the LEDs on and off almost instantaneously. Because the parallel topology uses fewer elements than the separate topology, it is a much smaller and less costly solution. It is moderately efficient. The power wasted by the resistor ballasts aggregate to a significant sum that raises concern.

Series topology

Like the parallel topology, the series topology has one main converter stage. However unlike in Figure 2.8, the LEDs are connected in series. There are n switches. Each is connected in parallel with one LED. When a switch turns on, the diode is shorted out and is turned off. One big challenge here is the switch implementation. It will require level shifting since only one switch is referenced to ground. All the others are referenced to a varying voltage. Even though the die size appears smaller than that of the separate topology, the complicated switching circuitry increases the die size considerably, and renders the series topology expensive and large. It is relatively efficient because no power is wasted through ballast resistors. Unfortunately, the current running through any two LEDs cannot be different.
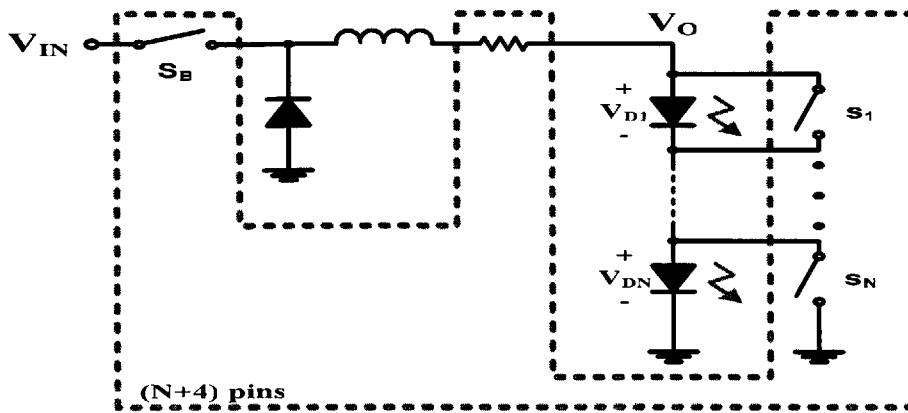
Figure 2.9: Series Topology.

Table summarizing tradeoffs

	Separate Topology	Parallel Topology	Series Topology
Transient Response	**Fast**	**Fast**	Moderate
Efficiency	High	**Moderate**	High
External Component Count	High	**Low**	Moderate
Die size	Control big Switch **small**	Control **small** Switch big	Control moderate Switch big
Total cost	High	**Low**	Moderate
Individual LED Current Adjustable	**Yes**	**Yes**	No

Table 2.2: Tradeoffs of commercial solutions.

The parallel topology appears to be the best suited to our purpose.

In conclusion, an ACMC approach with a parallel topology without the ballasted current sources may best answer our quest. A one loop, current loop ACMC will be used. This is because we expect the output voltage to vary a lot as we switch between several LEDs and also vary the output current. This makes it difficult to pin an output reference voltage for the voltage loop.

Chapter 3 - Systems and Specifications

Given the tradeoffs described in the preceding chapter, the best compromise between speed, size, cost and efficiency is to operate a single central control switch with one output node that sources several LEDs. These LEDs will be individually controlled with separate pulse signals (PWM). Since the different LEDs may require different DC output currents, the reference voltage that sets the output current will be pulsed to different voltages any time we switch between LEDs. The control circuit will adopt the single current loop Average Current Mode Control, which we shall loosely refer to as the Average Current Mode Control (ACMC).
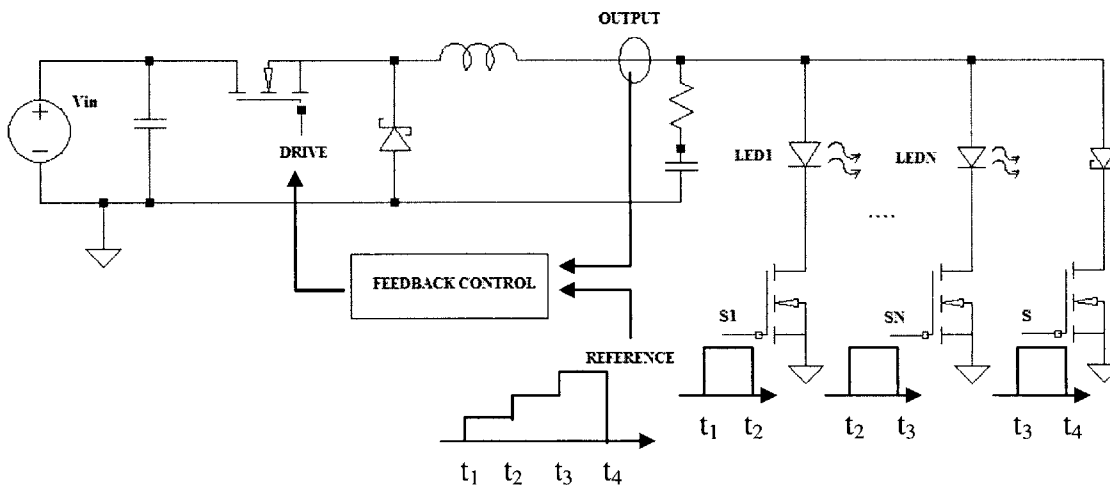
Figure 3.1: Multiple LED driver

The gate signals S1 to SN and S do not have significant overlap. However, because they are being switched at a very fast frequency, the eye averages the independent colors into one color. Signal S turns on the Schottky when none of the LEDs are on. By using a Schottky we waste less power during the turn off time at the output because the Schottky

has a low forward voltage. (One could select a different device or just use a "shorting" fet to tradeoff loss for output voltage deviation.)

Below is a set of practical electrical operating conditions at which we expect the multiple LED driver to meet. These requirements are based on commercial requests.

Multiple LED Driver

PARAMETER		MIN	TYP	MAX	UNITS
Input Voltage		10	15	30	V
Settling time		1	10	30	µs
Switching Frequency		0.15	0.6	2	MHz
Switch Duty Cycle		0		95	%
Output Current		0		3	A
Output Current ripple				150	mA
Output regulation			1	4	%
Quiescent Current			5	6	mA
Reference Voltage		0		1.25	V
Efficiency		85	92		%

Figure 3.2: Specifications for Multiple LED Driver

Chapter 4 - Design and Simulation

Because of time constraints, the circuit is designed and implemented using discrete components instead of in an integrated circuit. There is good reason to believe that the results obtained from the breadboard will provide great insight into a design on transistor level. This section explores how to achieve fast settling time with an ACMC controlled multiple LED driver based on a synchronous buck. Some suggestions to improve the settling time are also presented. This is followed by a discussion on the limitations of these design choices.

a. Average Current Mode Controlled LED Driver

Shown in Figure 4.1a is the simulation schematic of an ACMC controlled multiple LED driver. The output stage of the buck is a simple low-pass LC filter. The driver is designed for fast transient response at a 290 kHz switching frequency without exceeding the ripple specification (maximum 150mA peak to peak output current ripple). Specific circuit values and tradeoffs will be discussed in the following text.
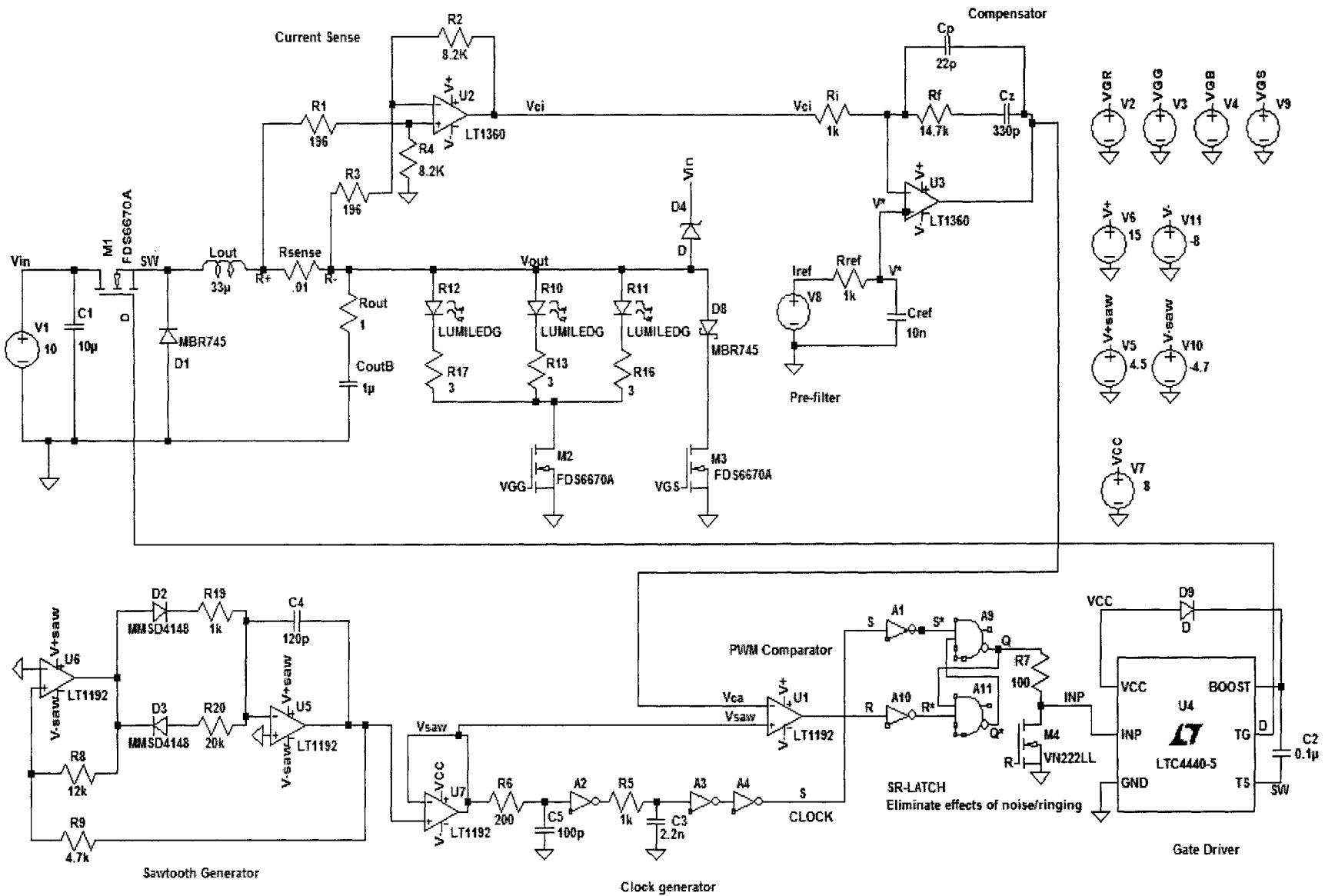
Figure 4.1a: Schematic of Average Current Mode Controlled LED Driver. See Appendix I for circuit description in SwitcherCAD.

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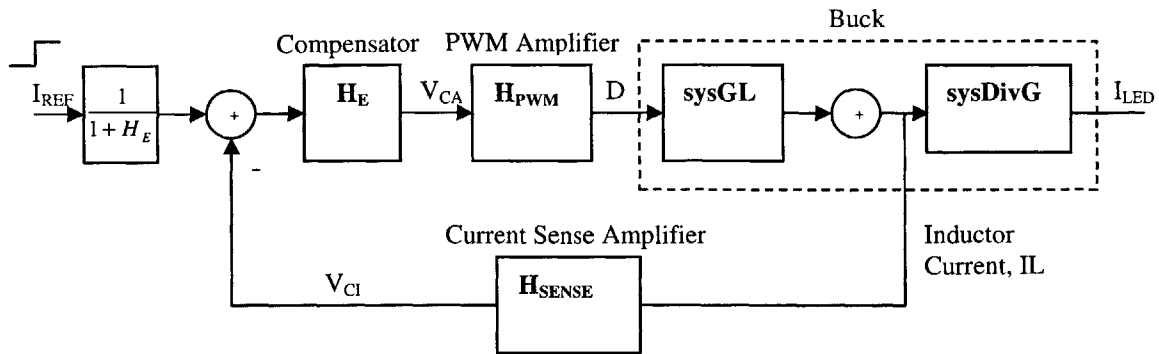
Figure 4.1b: Block diagram of Average Current Mode controlled multiple LED driver. This circuit is for a step in reference current. See Appendix II for block descriptions in MATLAB.
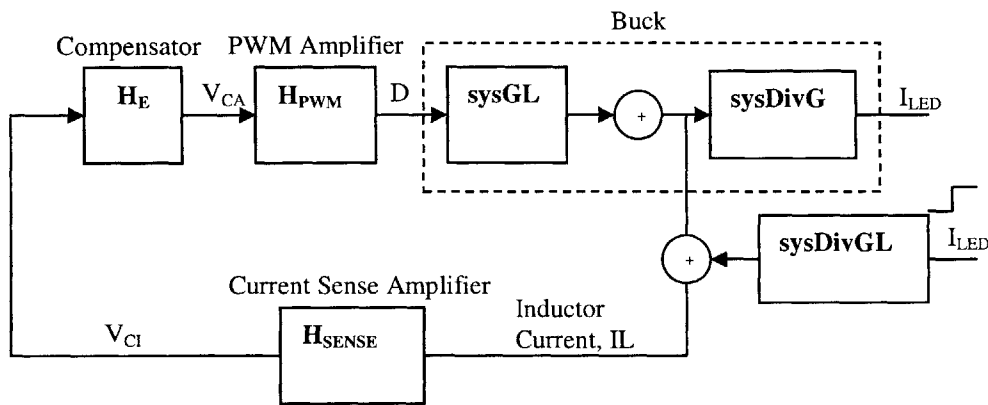
Figure 4.1c: Block diagram of Average Current Mode controlled multiple LED driver. This circuit is for a step in the load. See Appendix II for block descriptions in MATLAB.

Figure 4.1b shows the control block diagram of the system. I_{REF} sets the output current.

The inductor current sensed by $H_{SENSE} = Rsense * \dfrac{R2}{R1}$ gives V_{CI}, which is compared to

I_{REF} at the compensator. The difference is multiplied by the compensator transfer

function $H_E(s) = \dfrac{sR_f C_z + 1}{R_i[s(C_z + C_p) + s^2 R_f C_z C_p]}$, where s= jω. The output of the

compensator, V_{CA}, is sent to the PWM comparator, approximated as $f_{sw}*V_{SAW}$, where

fsw is the switching frequency and Vsaw, the amplitude of the sawtooth signal. The

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approximation H_{PWM} stems from the assumption that V_{CA} is a DC signal. Suppose this assumption is accurate, as Figure 4.2 below illustrates, the duty cycle D can be

approximated as $V_{CA}/(V_{SAW}*f_{SW})$ since $\dfrac{V_{CA}}{D} = \dfrac{V_{SAW}}{T}$.

VSAW
VCA

0   D   T   2T   3T
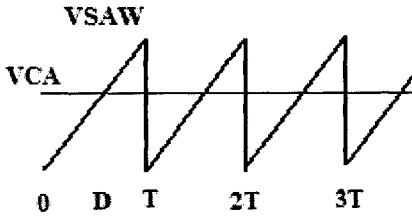
Figure 4.2: Assuming VCA is a constant, the transfer function of the PWM comparator can be linearized.

The next block models operation of the buck converter. At the buck, the duty cycle

multiplies sysGL $\approx \dfrac{V_{IN}/R_{OUT}}{s^2 * L_{OUT} * C_{OUT} + s * \dfrac{L_{OUT}}{R_{OUT}} + 1}$ to give the inductor current. A fraction

of the inductor current determined by sysDivG $= \dfrac{1 + s * C_{OUT} * R_{OUT}}{1 + s * C_{OUT} * (R_{OUT} + R_{LED})}$, flows into

the LED. R_{LED} is the dynamic resistance of the LED. For our purposes, the value of the

dynamic resistance is in the range of 0.02Ω and $0.6\ \Omega$.

Figure 4.1c shows a linearized model of the system during a load switch. Arguably, this

model is flawed in many respects, however it provides an insight into the dynamics of the

system during a load switch. The assumption is that the dynamic resistance of the LED

and the output voltage are almost constant such that sysGL and sysDivG remain constant

during the load switch. The idea behind the model in Figure 4.1c is that when the load

switches from an LED to another diode of a different forward voltage, the output current

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will jump or drop instantaneously primarily because of the exponential relationship between the output voltage and output current. This is valid if we assume the output voltage remains relatively constant at time t=0 when the load steps. This change in output current is reflected in the inductor current via sysDivGL, a current division of the output

current. $\text{SysDivGL} = \dfrac{sR_{OUT}C_{OUT} + 1}{s^2 L_{OUT}C_{OUT} + sR_{OUT}C_{OUT} + 1}$.

In seeking the "fastest" transient response, we mean the fastest 5% settling of the output current to, one, steps in the reference current, characterized by a step in I_{REF} in Figure 4.1a and 4.1b, and two, a load (or LED) switch at the output. Solving for the settling time exactly involves very involved non-linear calculations. In order to avoid detailed computation, we design for the highest possible bandwidth and a decent phase margin, a phase margin in the vicinity of 60° using linearized models and MATLAB as a tool. With the aid of SPICE simulations the settling time is calculated more accurately.

While filtering out ripple at the output, we jeopardize our mission to achieve a high bandwidth. The large filtering components we select for the output ripple attenuation present low frequency poles to the system. Without any dynamic compensation, these low frequency poles drag the bandwidth of the system to a low frequency too. The role of the compensator is to provide sufficient drive to compensate for these low frequency poles. The consequence is a higher bandwidth and faster settling. However, it needs to be recognized that the control authority to rapidly slew the output is limited by the inductor size, input and output voltages, and allowable duty ratio (0 to 1). The compensator not only adjusts the dynamics of the buck output but increases the gain and desensitizes the

system to changes in system parameters such as input voltage, output voltage and component values. With this compensation scheme, the buck stage parameters have limited impact on the small-signal bandwidth, though large signal changes are still (slew-rate) limited by the components. For simplicity, however, the design of the power stage and the controller are decoupled and designed sequentially. These design decisions are then studied and revisited where needed.

Initial Design

The output stage of the buck is constructed using a $33\mu H$ inductor and a $1\mu F$ capacitor in series with a 1Ω damping resistor. This initial design adequately filters out the output ripple. Figure 4.3 confirms that this choice of output filter attenuates output ripple sufficiently. But the small-signal bandwidth is fairly low, meaning that the transient response of the open-loop buck is not fast.
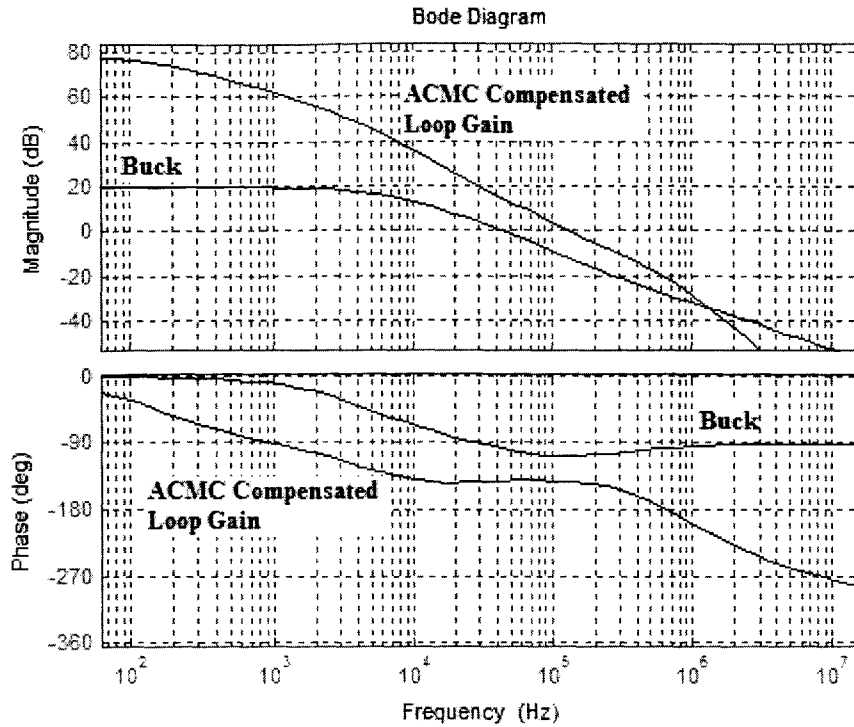
Bode Diagram

Figure 4.3: Bode plot of open-loop buck (= sysGL*sysDivG) and ACMC compensated open-loop gain (= sysHE*sysHPWM*sysGL*sysDivG) from MATLAB. ACMC Compensation shifts bandwidth from 5kHz to 110kHz. The values used in the converter and compensator are

$$\frac{1.373e^{-39}s^7 + 2.72e^{-33}s^6 + 1.676e^{-27}s^5 + 3.3e^{-22}s^4}{9.245e^{-45}s^8 + 1.374e^{-38}s^7 + 6.948e^{-33}s^6 + 1.263e^{-27}s^5 + 3.432e^{-23}s^4}$$

and

$$\frac{1.848e^{-17}s^8 + 4.035e^{-23}s^7 + 2.999e^{-29}s^6 + 9.026e^{-34}s^5 + 9.029e^{-39}s^4}{(1.128e^{-38}s^{15} + 4.527e^{-29}s^{14} + 6.826e^{-20}s^{13} + 4.599e^{-11}s^{12} + 0.01186s^{11} + 1.457e^5s^{10}}$$

$$+ 4.931e^{11}s^9 + 5.348e^{17}s^8 + 2.388e^{23}s^7 + 4.085e28s6 + 1.131e33s5 + 1.09e36s4)$$

respectively. The computation of these transfer functions is indexed in Appendix II.

ACMC modifies the slow small-signal behavior of the open-loop buck regulator by injecting a zero before the switching frequency. This compensation is implemented as a type II compensator. With the driver powered by a 10V input voltage and switching at 290kHz, the result is a 7μs settling time response to a step in reference current (at a constant 1Ω load), and a 27μs settling time when we change the load from a Schottky diode to an LED having an approximately 3.9V drop at approximately 250mA output current. Figures 4.4 and 4.5 illustrate the current settling of the RGB driver.

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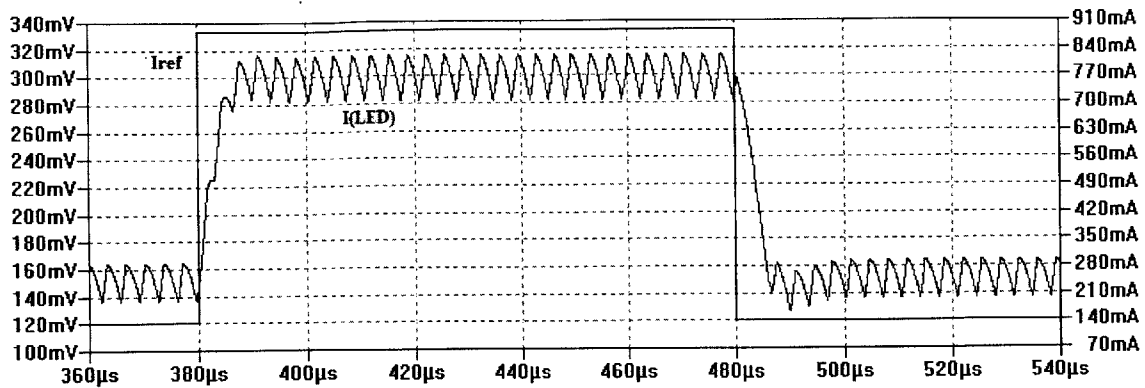
Figure 4.4: LED current settles to 5% of final value in 7μs in response to a reference current step. Upward settling time and downward settling time both equal 7μs.
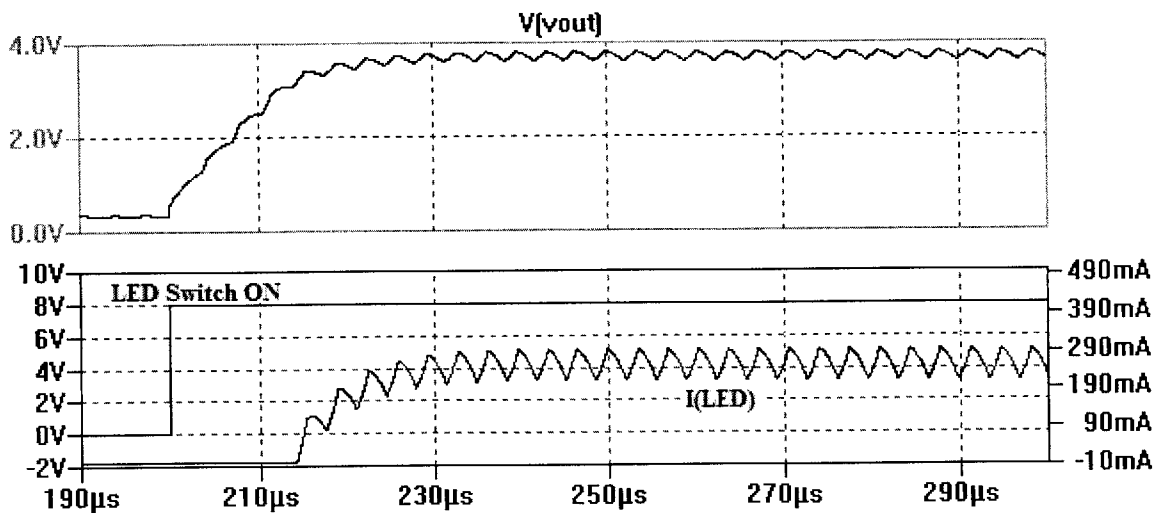
Figure 4.5: Transient response of output current when load is changed from a Schottky to an LED of approximately 3.9V drop. Output current settles within 27μs to 5% of final value.

Since the RGB driver is to be used under varying duty cycle operations, it is important that the settling time remain reasonable for all possible reference current step amplitudes. We subject the driver to a 10% to 90% step in reference current and examine the current settling. With this large reference current step, the settling time deteriorates considerably. This phenomenon occurs for reference current steps greater than 0.9A. As Figure 4.6 depicts, this slow reference current settling stems from duty cycle saturation. When the

reference current makes a huge jump suddenly, the system falls out of small signal operation. Consequently, the settling time is no longer determined by the small signal bandwidth of the system, but rather, the settling time is dominated by a large signal slew rate, which is closely related to the passive component values.
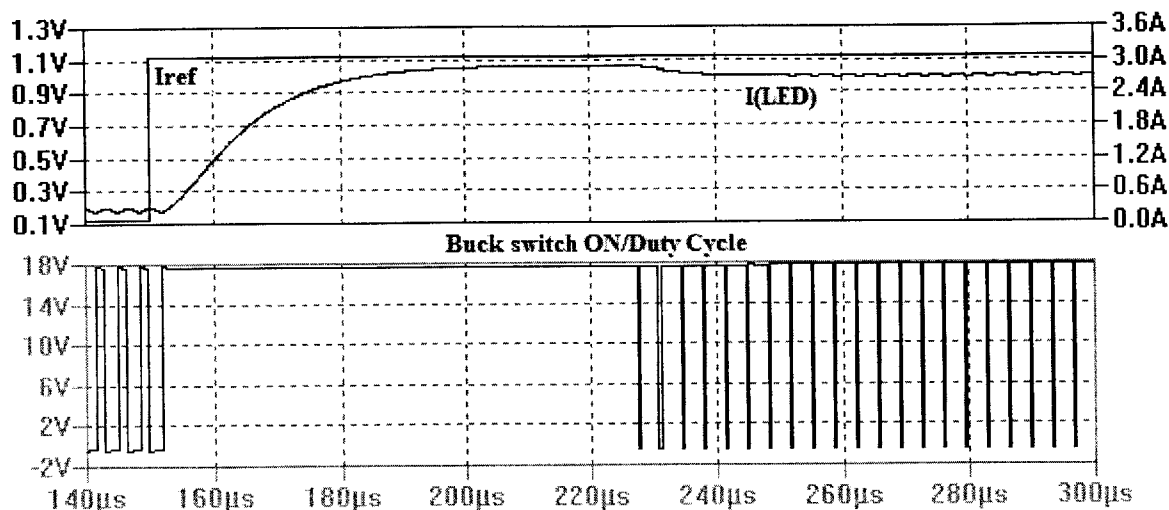
Figure 4.6: For reference current excursions beyond 0.9A, the duty cycle saturates and settling time worsens dramatically. For a 2.4A step in output current, settling time is 80μs compared to 7μs when reference current steps by 500mA.

In summary, settling time is 7μs in response to small reference current steps, 80μs in response to large reference current steps and 27μs when load is changed from a Schottky of approximately 0.2V drop to an LED of approximately 3.9V drop.

b. Improvements to ACMC Controlled LED Driver

We now explore the limitations of the initial design. Armed with an understanding of where the limitations stem from, we can improve the settling time by fine-tuning our initial design or introducing different solutions that resolve the limitations of the initial design.

Improving small reference current step settling

The first item for improvement is the small reference current step settling time. In [12], P-L. Wong et al. (2002) describe a design method, critical inductance design, as a means to design a fast transient and efficient converter. The authors of *Critical inductance in voltage regulated modules* claim that in a fast DC/DC converter, there exists a critical inductance above which the transient response of the converter is drastically degraded. The idea behind the critical inductance is that as long as one avoids duty cycle saturation, by limiting inductor size to the "critical inductance", the converter exhibits superior transient performance compared to other conventional design methods such as the continuous conduction mode (CCM) or quasi-square wave (QSW) design. Typically, the critical inductance design solution yields a faster transient response in comparison to the other design schemes, and where the transient responses are comparable, the critical inductance technique offers lower output ripple. The authors of [12] define the critical inductance, L_{CRIT} as the largest inductor that permits the largest needed change in duty cycle. $L_{CRIT} = \dfrac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}}$; ΔD_{MAX} is the maximum change in duty cycle, ΔI_{OUT} is the corresponding change in output current, V_{IN} is the input voltage and ω_{BW} is the bandwidth.

Given that our application calls for a $\Delta D_{MAX} \approx 0.95$, $\Delta I_{OUT} \approx 2.85A$, $\omega_{BW} = 2\pi*29kHz$ at $V_{IN} = 10V$, L_{CRIT} calculates to be a $29\mu H$ inductor.

With L_{OUT} at $29\mu H$, the output capacitance is set at $1\mu F$, so as to meet the ripple specification. The damping resistor is maintained at 1Ω. The small reference current step settling time stays at $7\mu s$ and the output current settling time stays at $27\mu s$. Meanwhile,

for large reference current steps, the settling time reduces from 80μs to 73μs. Figures 4.7 through to 4.9 illustrate these results.

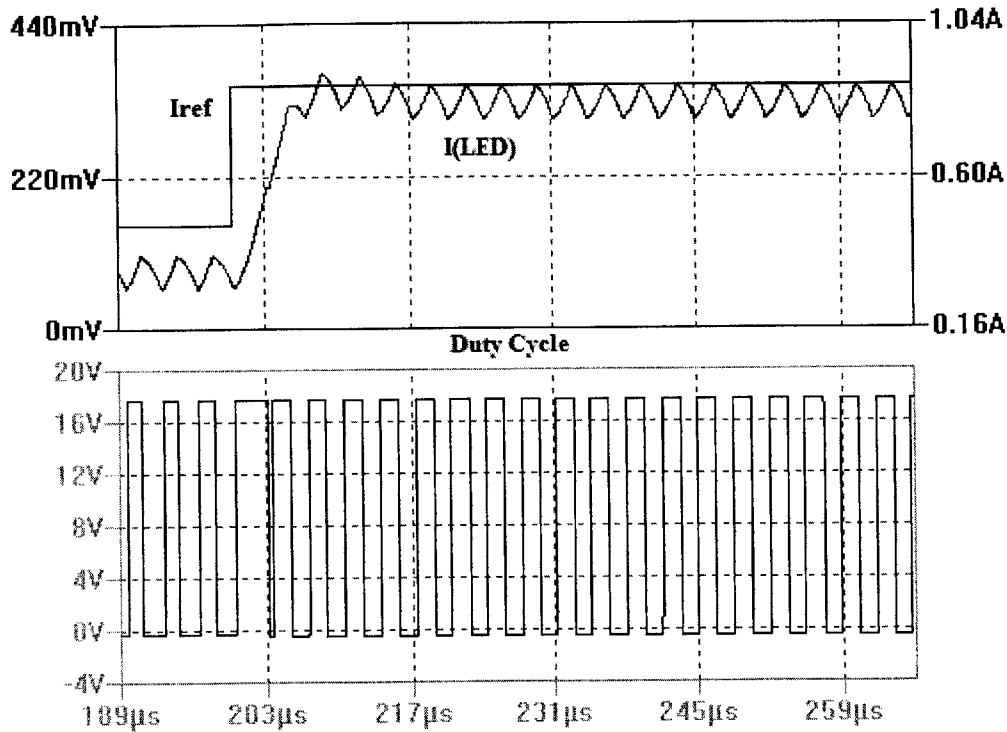**Figure 4.7:** The critical inductance design scheme keeps the small signal settling time at 7μs.
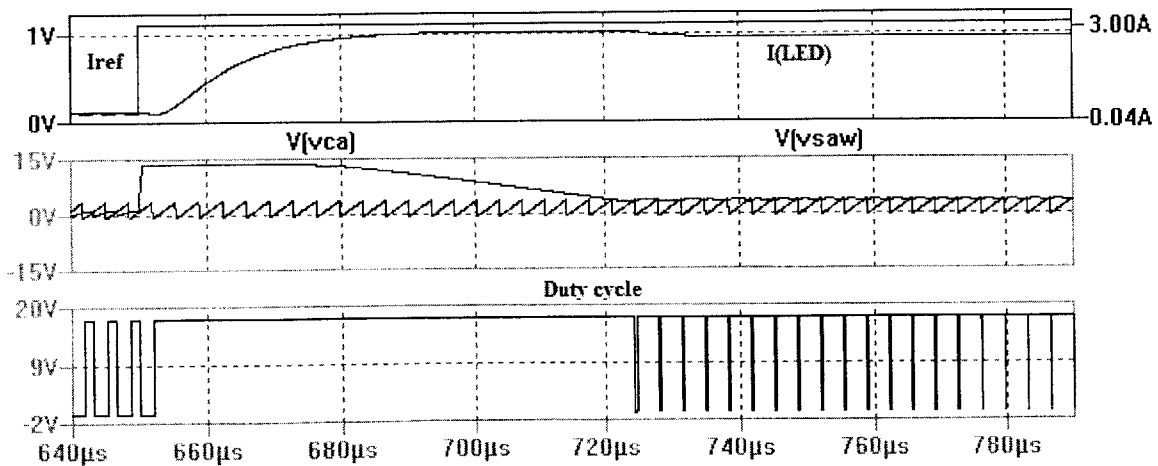

Figure 4.8: After applying the critical inductance technique, the settling time for large output current steps improves from 80μs to 73μs.

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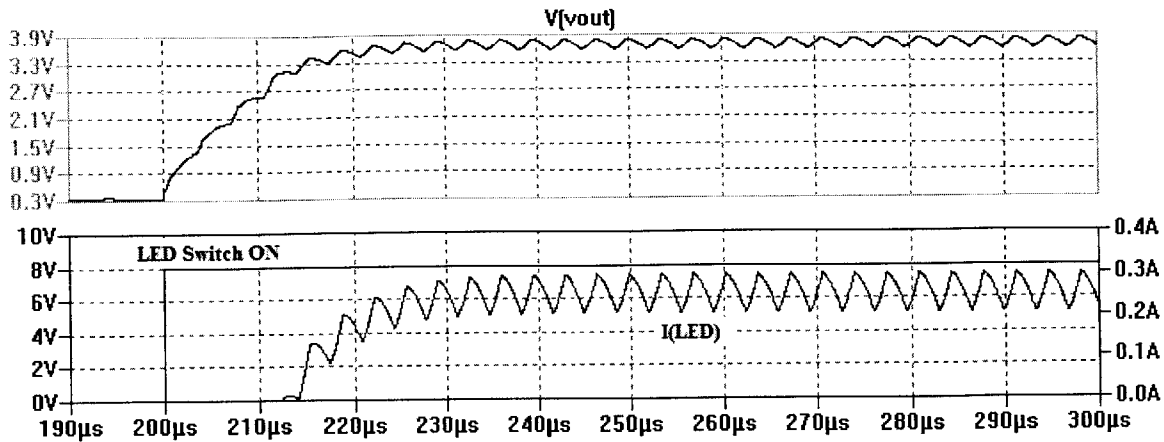
Figure 4.9 After applying the critical inductance rule, the output current settling time stays at 27μs.

The critical inductance design method does not improve the small reference current step settling time. This raises the question as to whether the 29μH inductor is the true critical inductance. Suppose 7μs is the optimal small reference current step settling, it implies that the critical inductance is not 29μH but rather is an inductance equal or greater than 33μH. For, with a 33μH inductor, we still managed to avoid duty cycle saturation.

Improving large reference current step settling

Although the critical inductance design method is said to prescribe an inductor size such that duty cycle saturation is avoided, contrary to expectations, Figure 4.8 points out that the saturation problem persists for large reference current steps, even after the conservative critical inductance design. This apparent controversy is resolved by examining the root cause of the duty cycle saturation. It turns out that the duty cycle saturation observed in Figure 4.8 is not directly related to the output inductor size. The saturation here is different from that which is referred to by [12]. This saturation arises from the slewing of the integrating capacitors at the compensator. As Figure 4.8 depicts,

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when the reference current steps, signal V_{CA}, the compensator output voltage, swings to the supply rail immediately. Afterwards, the large integrating capacitors slow down the slew of V_{CA}. It takes over 70μs slewing down to meet with the sawtooth signal, V_{SAW}. Even at time 680μs, 30μs after the reference current steps, the duty cycle wrongfully remains at 100%, although the output current has overshot its target - all because the slow slewing V_{CA} is still well above the sawtooth.

One workaround is to add on an anti-windup circuit [13]. Two zener diodes connected back to back across the compensator capacitor Cp serve to clamp the integration error of the compensator, and prevent V_{CA} from hitting the rails. Similarly, the amplitude of the sawtooth can be increased to reduce the voltage potential between the supply rails and the sawtooth. When a 4.7V zener anti-windup circuit is added, V_{CA} clamps at 4.7V. The settling time drops down to 22μs. This settling time is much better than the settling time attained by the initial design and the settling time attained by the "critical inductance" circuit. This improved settling is captured in Figure 4.10.
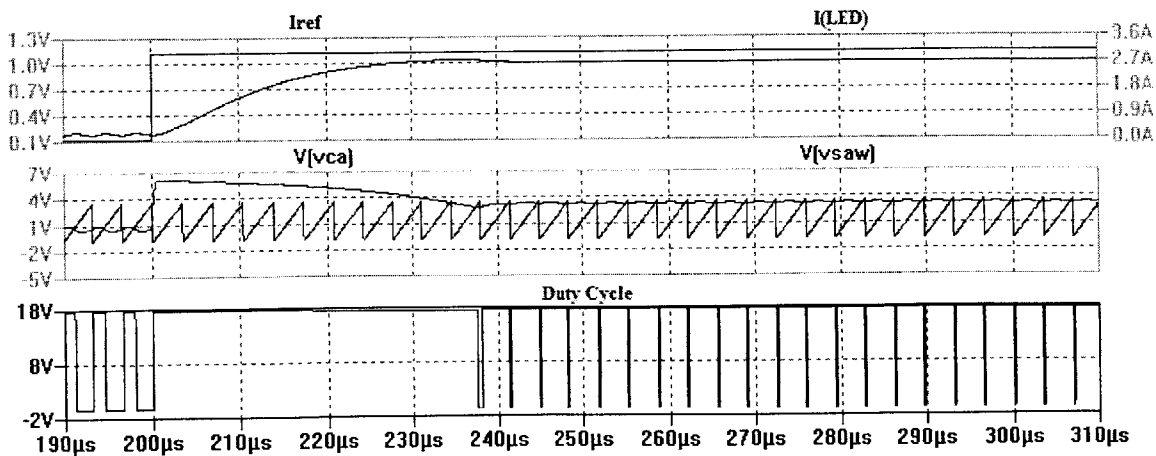

Figure 4.10: The anti-windup circuit reduces large reference current step settling time from 73μs to 22μs.

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An equally efficient remedy is to filter the reference current (or voltage) with a low pass filter. The compensator sees a smoother jump in the reference current (or voltage), and so does not provide needless gain that sends the output current overshooting its target. Figure 4.11 shows that by smoothing the large reference current step, the delay caused by the slewing of the integrating capacitors is truncated to 28μs.
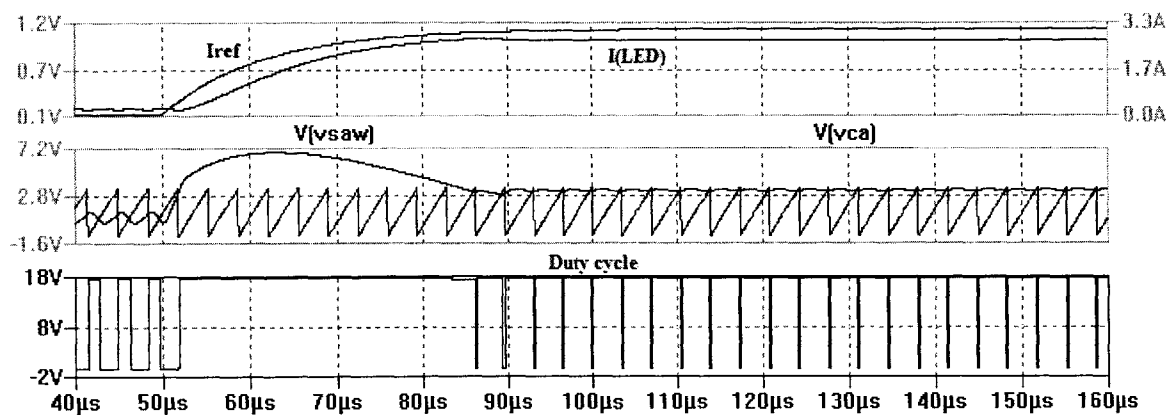
Figure 4.11: Slowly ramping up the reference current also reduces settling time from 73μs to 28μs.

Figures 4.10 and 4.11 beg the question as to whether we can shrink the duty cycle saturation time further, possibly to zero microseconds. We expect that by using a smaller output inductor, we can use smaller integrating capacitors, and as a result speed up the slew of the integrating capacitors. This argument implies that reducing the output inductance should improve the large reference current step settling. Former observations of the large reference current step confirm this argument. Without an anti-windup circuit, when the output inductor is at 29μH, the large reference current step settling time is 73μs and at 33μH the settling time is 80μs. We combine the positive effects of using an anti-windup and using a lower output inductor size, and run the driver with an anti-windup

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circuit and a 20μH inductor. The saturation time reduces to 17μs, pushing the large

reference current step settling time to 17μs. See Figure 4.12. The small reference current

step settling time of the driver still remains at 7μs. The output current settling time also

remains at 27μs.
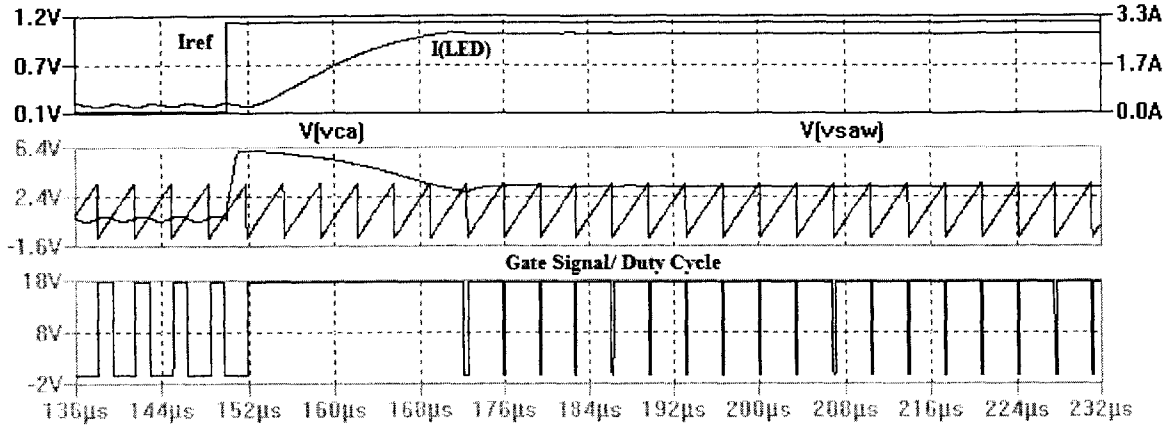
Figure 4.12: For a 2.4A reference current step, reducing output inductor to 20μH lowers the settling time further to 17μs.

Unfortunately, we cannot blindly reduce the output inductor size, because there is a

minimum inductance needed to keep the driver stable. This minimum inductance is the

minimum inductance needed to keep the slope of the inductor current as seen at the input

of the PWM comparator from exceeding the slope of the sawtooth signal [10]. Hence,

$\dfrac{V_{OUT}}{L_{OUT}} * sysHsense(j\omega_{sw}) * sysHE(j\omega_{sw}) \leq V_{SAW} * f_{sw}$; sysHsense and sysHE are the

amplification at the current sense amplifier and compensator respectively. Therefore,

$L_{OUT} \geq \dfrac{V_{OUT} * sysHsense\ (j\omega_{sw}) * sysHE\ (j\omega_{sw})}{V_{SAW} * f_{sw}}$. For the present system, this

represents $L_{OUT} \geq 20\mu H$.

Combining this minimum inductance criterion with the maximum inductance constraint provides a range of output inductor sizes that yield the minimum reference current step settling time. Any inductor within this range offers excellent small reference current step settling, while the minimum in the range provides the best large reference current step settling and real estate savings.

$$\frac{V_{OUT} * sysHsense(j\omega_{SW}) * sysHE(j\omega_{SW})}{V_{SAW} * f_{SW}} \leq L_{OUT} \leq \frac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}} \tag{4.1}.$$

For our values, we find $20\mu H \leq L_{OUT} \leq 29\mu H$

Improving load step settling

Altogether, the techniques discussed so far have improved the reference current step settling. The settling time in response to a load step, on the other hand, appears to stick around 27μs for output inductors sized between 20μH and 33μH. Why is this? A second pertinent question is, if the same control circuitry controls the output current (or more correctly the inductor current) during reference current steps and during load steps, why is the output current step response not as fast as the reference current step response?

In answer to the second question, we compare the block diagram of the system in Figure 4.1b to that illustrated in Figure 4.1c. The loop transfer function to the two step inputs, I_{REF} and load are not the same. While the reference current goes through a prefilter labeled 1/(1+sysHE) before entering the closed loop, any disturbance to the output current due to a load switch is first treated by sysDivGL. Since these two blocks are not identical, we do not expect the same transient response to the two step inputs.

Now, to why the output current step response sticks around 27µs. A few simulation runs reveal that the load settling performance derails with higher output inductance and/or higher output capacitance. For example, with the output inductor at 72µH, the output current settles within 140µs. This slow down is because high output capacitors and high output inductors push the poles of sysDivGL to very low frequencies. These low frequency poles contribute to the slow responses to output current steps.

All these statements have been made with the assumption that the small signal model of Figure 4.1c accurately describes the system when the output current steps. Arguably, this assumption is flawed, since the LEDs are not linear devices. When we switch LEDs the descriptions of sysGL and sysDivG change. One reason is because the output voltage moves during the transition. SysGL is defined under the assumption that the output voltage stays fixed. Secondly, the buck model changes during the output current step because the dynamic resistance of the load changes. The fact that the output voltage only swings within an order of magnitude, and the fact that the dynamic resistances of the LEDs are all fairly low, mean sysGL and sysDivG remain unchanged to some degree. Secondly, if one adds on a resistor in series to the output capacitor, a resistor whose value is much less than all the dynamic resistances of the LEDs, then this added on resistor dominates the output resistance, sysGL and sysDivG are more robust when the load steps, and the small signal model applied does convey some truth about the behavior of the circuit.

Another reason for adding on the resistor in series to the output capacitor is to lower the peaking of the output current when we step from a high forward voltage LED to a low forward voltage LED. SPICE simulations show that a 1Ω resistor serves the purpose quite dutifully. Additionally, the efficiency of the system remains almost unchanged after this modification.

In summary, low output inductors and low output capacitors improve the output current settling time. Ripple specifications together with stability issues and reference current step settling specifications do not permit us to reduce the output inductor and/or output capacitor too low. Since the objective is to achieve both excellent current step settling and output current step settling, we resort to the output inductor range set by equation 4.1;

$$\frac{V_{OUT} * sysHsense(j\omega_{SW}) * sysHE(j\omega_{SW})}{V_{SAW} * f_{SW}} \leq L_{OUT} \leq \frac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}}$$

One must not jump to the smallest inductor in the range, as this may call for a very high output capacitor in order to meet output ripple specifications. The high output capacitor will derail the settling and defeat the purpose of picking a low output inductor.

Higher switching Frequency

The preceding sub-chapters seem to imply that we cannot improve upon the 7μs small signal settling and the 27μs output current settling at 290kHz switching. The only alternative left to shrink the settling times is to scale the entire design up in frequency. Scaling the frequency by a factor of 3 to 970kHz, sets the reference current step settling time at 2.5μs, the 2.4A reference current step at 6μs and the output current step at 9μs. With a 2μs reference current settling time target, we run the circuit at 1MHz, and indeed

we achieve a 2us for a 600mA step in output current. At 1MHz, the 2.4A reference current step, settles within 4µs and the load settling time measures to be 7µs. See Figures 4.13 through to 4.16.
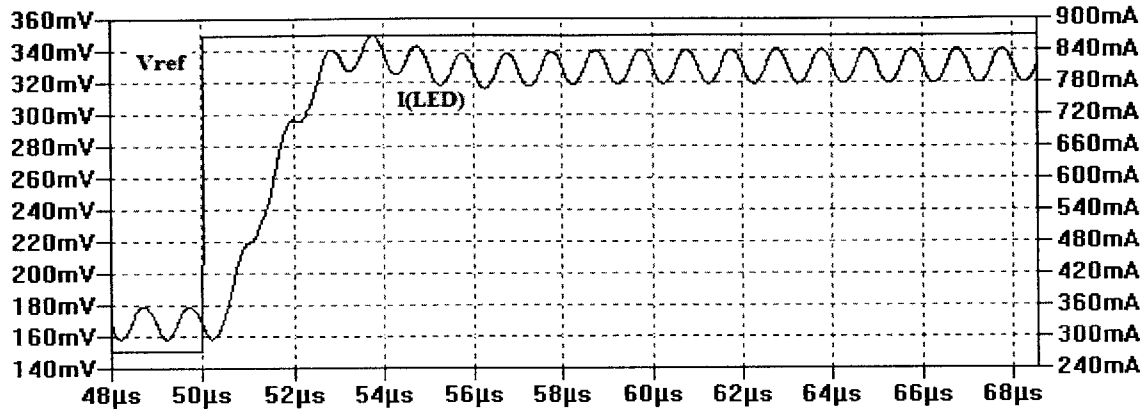
Figure 4.13: Switching at 1MHz results in a 2µs settling time for a 600mA step in reference current. This simulation uses circuit values $V_{IN}=10V$, $L_{OUT} = 5.8\mu H$, $C_{OUT} =.29\mu F$, $R_{OUT} = 1\Omega$ and compensator values Ri=1k, Rf = 15k, Cp = 6.38pF, Cz=95.7p and a 4.7V zener anti-windup circuitry.
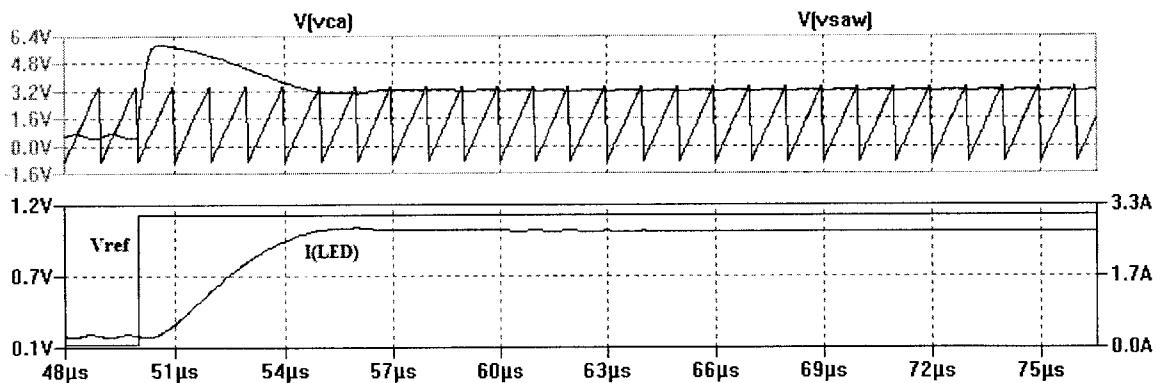
Figure 4.14: And for a 2.4A step in reference current, switching at 1MHz yields a 4µs settling time. This simulation uses circuit values $V_{IN}=10V$, $L_{OUT} = 5.8\mu H$, $C_{OUT} =.29\mu F$, $R_{OUT} = 1\Omega$ and compensator values Ri=1k, Rf = 15k, Cp = 6.38pF, Cz=95.7p and a 4.7V zener anti-windup circuitry.

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Figure 4.15: At 1MHz switching, output current settling time is 7µs. This simulation uses circuit values V_{IN}=10V, L_{OUT} = 5.8µH, C_{OUT} =.29µF, R_{OUT} = 1Ω and compensator values Ri=1k, Rf = 15k, Cp = 6.38pF, Cz=95.7p and a 4.7V zener anti-windup circuitry.

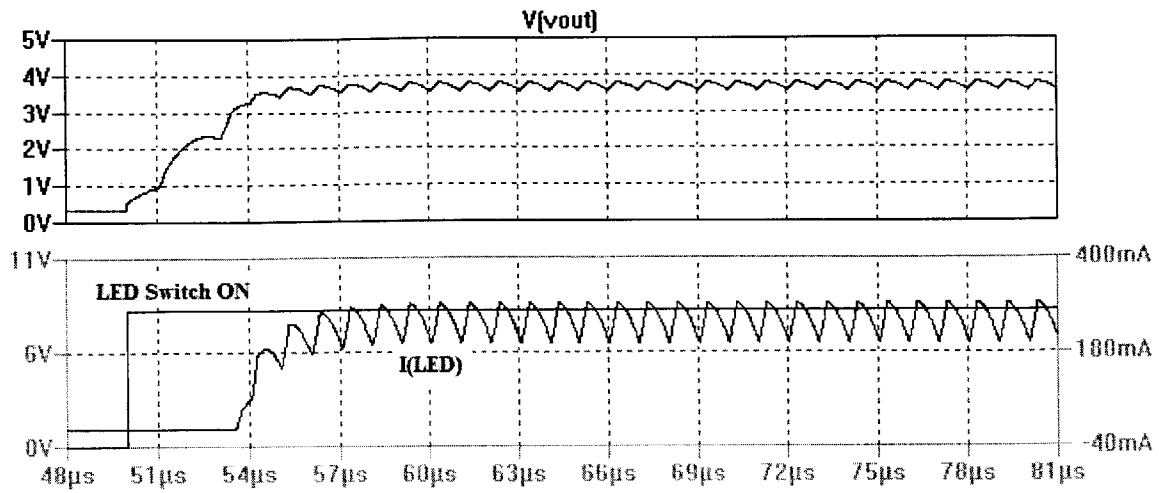## Summary of design choices and settling times

Circuit: V_{IN}=10V	Settling time/μs		
	Small Reference Current Step	Large Reference Current Step	Output Current Step
Initial design: f_{SW}=290kHz L_{OUT} = 33μH, C_{OUT}=1μF, R_{OUT}=1Ω Cp=22pF, Cz=330pF	7	80	27
Critical inductance : f_{SW}=290kHz L_{OUT} = 29μH, C_{OUT} =1μF, R_{OUT} = 1Ω cCp=22pF, Cz=330pF	7	73	27
Zener Anti-windup/ Prefilter: f_{SW}=290kHz L_{OUT} = 29μH, C_{OUT} =1F, R_{OUT} = 1Ω Cp=22pF, Cz=330pF	7	22/28	27
Zener Anti-windup: f_{SW}=290kHz L_{OUT} = 20μH, C_{OUT} =1μF, R_{OUT} = 1Ω Cp=22pF, Cz=330pF	7	17	27
Higher switching frequency: 970kHz L_{OUT} = 6.7μH, C_{OUT} =.33μF, R_{OUT} = 1Ω Zener Anti-windup Cp=7.3pF, Cz=110pF	2.5	6	9
Higher switching frequency: 1MHz L_{OUT} = 5.8μH, C_{OUT} =.2μF, R_{OUT} = 1Ω Zener Anti-windup Cp=6.38pF, Cz=95.7pF	2	4	7

Table 4.1: Summary of design choices and settling times

Conclusion - Settling time

1. For small signal reference current steps, an inductor size within the range specified by equation 4.1,

$$\frac{V_{OUT} * sysHsense\,(j\omega_{SW}) * sysHE\,(j\omega_{SW})}{V_{SAW} * f_{SW}} \le L_{OUT} \le \frac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}}, \quad \text{offers}$$

the minimum settling time in response to both reference current and output current steps.

2. For fast large reference current step settling, the smallest inductor size in the range should be selected. An anti-windup circuit also improves the large reference current step settling. If the designer can cook up an anti-windup circuit that always keeps the integration capacitors from hitting the supply rails, the large reference current step settling will equal the small reference current settling time and would not be a topic needing special attention.

3. The load step settling time is improved by restricting inductor size and output capacitor size to low values. The best output current settling time is also achieved by selecting an inductor size L_{OUT} such that

$$\frac{V_{OUT} * sysHsense\,(j\omega_{SW}) * sysHE\,(j\omega_{SW})}{V_{SAW} * f_{SW}} \le L_{OUT} \le \frac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}}$$

4. Adding a low resistor in series to the output capacitance serves to keep the transfer function of the buck system relatively constant under different LEDs. It also serves to lower the peaking of the output current when one switches from an LED of a high forward voltage to an LED of a lower forward voltage. Adding on a damping resistor has no impact on the settling times.

5. Scaling the circuit up in frequency improves all settling times.

6. In our application since we step both the reference current and the load step settling at the same time, we are ultimately concerned with the maximum of the two settling times. The initial design of the output stage of the buck – a 33μH inductor connected to a 1Ω resistor in series with a 1μF output capacitor yields the best overall settling time with reasonable efficiency, since we are using a reasonably large inductor.

Efficiency

Power is lost primarily through the conduction losses of the switch mosfets M1, MS1 to
MSN and MS and the catch diode. The sense resistor, the ESR of the inductor and ESR
of the output capacitor also contribute to the power losses. Furthermore, the switching
losses of the mosfets and gate driver circuits also add to the inefficiency of the system.

The capacitor and inductor in the circuit also burn power via their parasitic resistance.
The capacitor values used in the circuit are less than 1μF, as a result, we expect them to
be of the ceramic type, to have negligible ESR and to burn negligible power. Because of
this argument, the capacitors are modeled without ESR in SPICE. The on-resistance of
the inductor is also neglected in simulation because the on-resistance of the inductor is
very specific to the inductor: its shape, size and other manufacturing conditions. It is
therefore unreasonable to fix the on-resistance of the inductor in simulation.

Since the ESR of the capacitors and the on-resistance of the inductor are always kept at
zero in simulation, it is not surprising that the efficiency measured in simulation is almost
constant across the design schemes proposed.

$$Efficiency = \left(\begin{array}{c} \dfrac{1W}{1.7W} = 59\%; I_{OUT} = 0.36A \\ \dfrac{25W}{26.1W} = 95\%; I_{OUT} = 2.7A \end{array} \right)$$

It must be noted that the true efficiency is lower since all of the controller power
consumption is not accounted for here. The other reason is that the inductor and
capacitors are also modeled without any parasitic resistance.

c. Modeling of External Components

As indicated earlier the capacitors and inductors are modeled as ideal components. The inductor is modeled as a pure inductor. It has neither parasitic resistance nor parasitic capacitance. In the same vein, the capacitor is modeled as a pure capacitor. It has neither parasitic resistance nor parasitic inductance. The consequence is that the efficiency estimated from simulation is higher than it will be on breadboard. That being said, because we expect the capacitors to be of the ceramic type with very low ESR, by ignoring the capacitors' ESR only negligible errors are introduced to the SPICE simulation results.

The amplifiers and gate drivers are selected from the LTC SwitcherCAD library. A few modifications are added to the models to make them more realistic. One such modification is limiting the output current of the operational amplifiers in the circuit to their true maximum output current.

d. Modeling of Power Dissipation

The efficiency measurements are made by averaging power dissipated at the input and at the sawtooth generation circuit as input power. Output power is calculated by averaging power dissipated by the LED alone.

Chapter 5 – Testing

Testing the design solutions proposed in Chapter 4 on the bench allows us to validate the computer models and conclusions drawn. Since the models are as accurate as we make them, performance in simulation may deviate from real life performance if the models are inaccurate. Measurements on the bench should give a more realistic picture of solutions proposed.

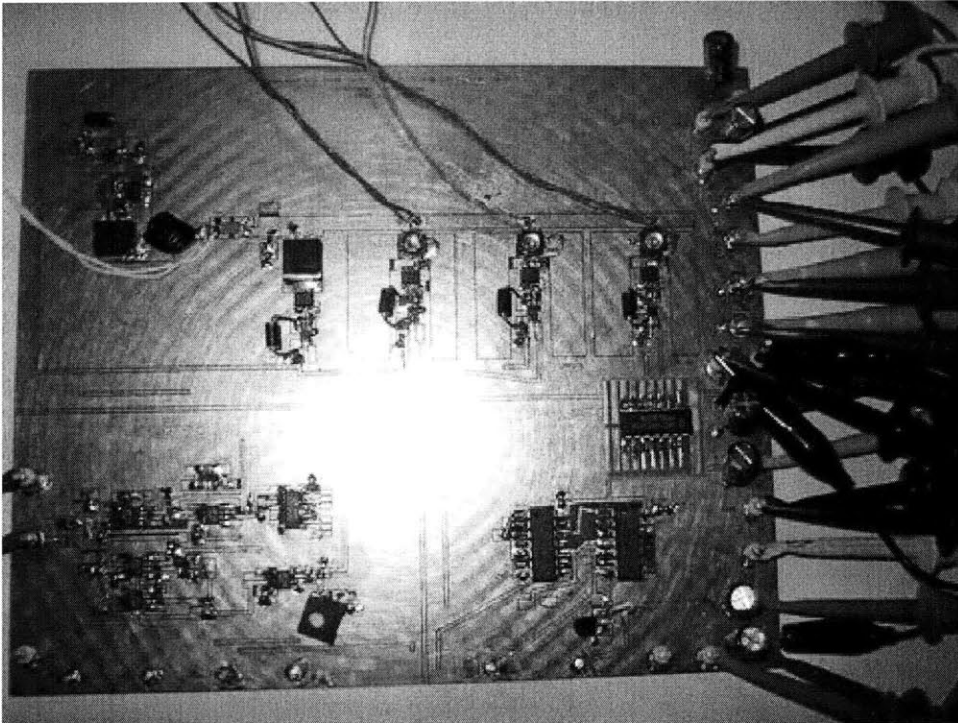A picture of the breadboard of the initial solution is displayed below in Figure 5.1.

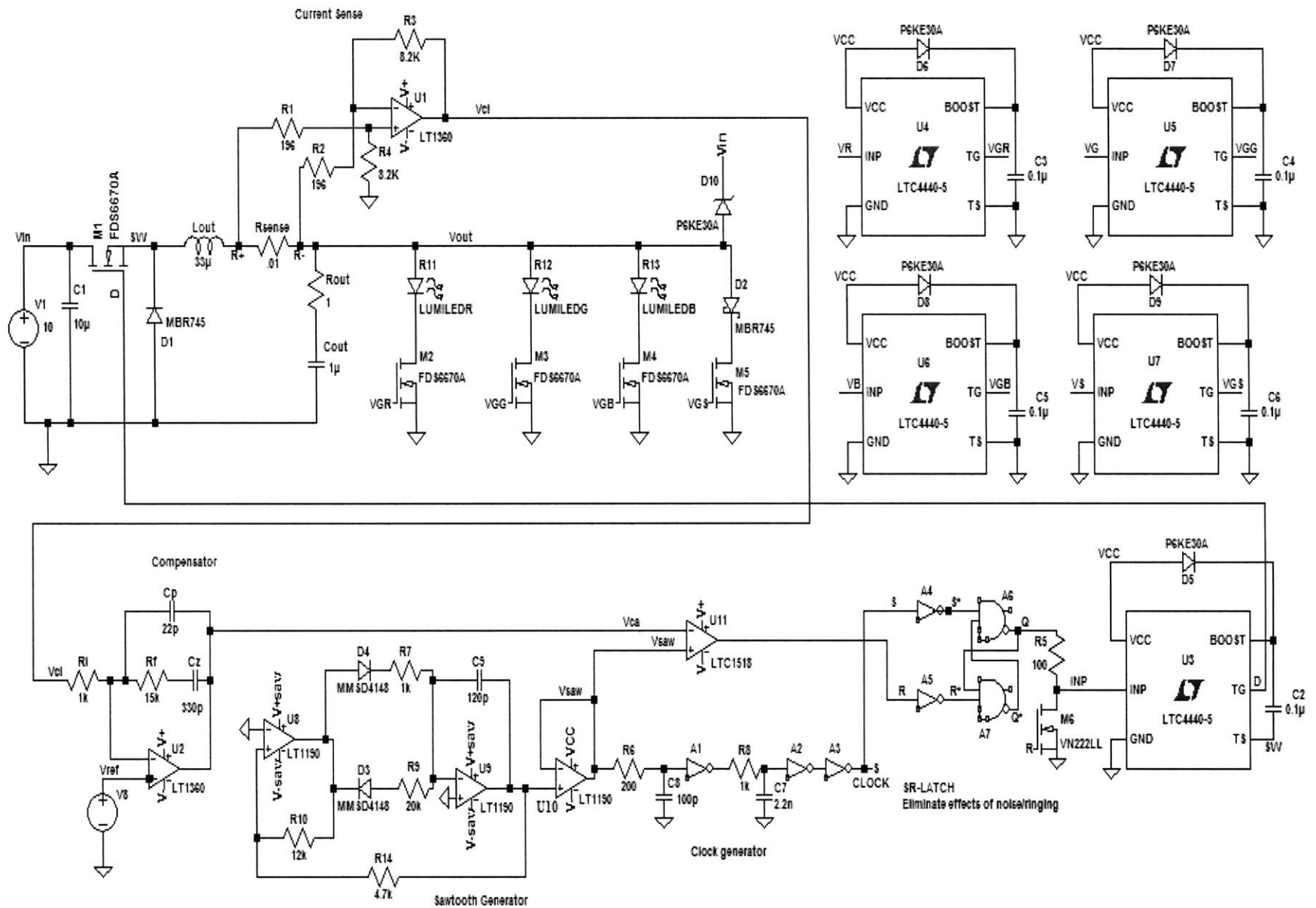**Figure 5.1:** PCB board of initial design. The PCB board layout and Bill of Materials are indexed in Appendix III

Figure 5.2: Full Circuit Schematic of the prototype system

Operating parameter	Value
Input voltage, V_{IN}	10V- 30V
Switching frequency	101kHz, 179kHz, 290kHz, 430kHz, 592kHz, 620kHz, 702kHz, 870kHz, 1.07MHz, 1.41MHz
Output Inductor, L_{OUT}	7.1µH, 12.9µH, 17.2µH, 32.2µH, 44.9µH, 94.7µH, 131.5µH, 187.3µH (All inductors are of type DO3316P)
Output Capacitor, C_{OUT}	11nF, 41nF, 74nF, 430nF, 852nF, 4.25µF, 7.53µF, 52.93µF, 97.16µF
Output Resistor, R_{OUT}	0.01Ω, 0.05Ω, 0.1Ω, 0.6Ω, 1.3Ω, 5.2Ω, 10Ω, 50Ω, 100.6Ω
Load All LEDs listed are connected in series with a FDS6670A Fet	MBR74 Schottky LXK2-PD12-Q00 (Red LED) LXK2-PM14-U00 (Green LED) LXK2-PB14-N00 (Blue LED) Three parallel connected LXHL_PW09, each in series with a 1Ω resistor (for high current tests)
Vref	0-1.25V
V+	15V
V-	-8V
V+saw	4.5V
V-saw	-4.7V
Vcc	8V
VR	PULSE 0V-5V, variable on-time, 1kHz
VG	PULSE 0V-5V, variable on-time, 1kHz
VB	PULSE 0V-5V, variable on-time, 1kHz
VS	PULSE 0V-5V, variable on-time, 1kHz

Table 5.1: Prototype operating parameters

a. Measurement Techniques

Here we indicate how the quantities of interest are measured. Measurements using these techniques are applied in subsequent subsections.

i. Settling time

At low currents, the output current ripple is larger than 10% of the final output current. This makes it difficult to spot what the 5% settling time is.
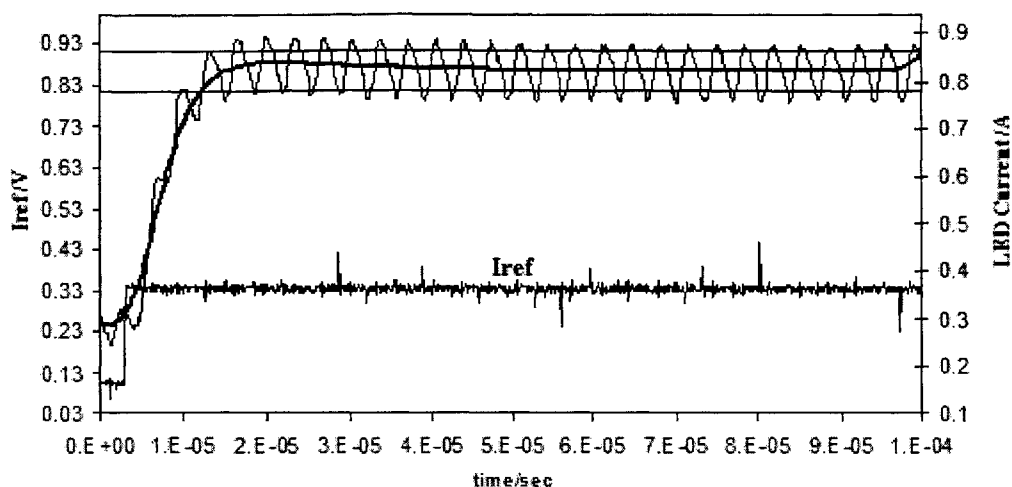
Reference voltage settling

Figure 5.3: The large ripple on the output current makes it difficult to spot the 5% settling time. After smoothing output current with a moving average, settling time is easily read off plot as 9μs. V_{IN}=15V, L_{OUT}= 33uH, C_{OUT}=850nF, f_{SW}=290kHz, LED = LXHL_PM09.

In order to circumvent this difficulty, a moving average was used to smoothen out the ripple of the LED current. The equation for the moving average used was

$$\bar{x} = \frac{1}{T} \int_{t-T/2}^{t+T/2} x(\tau)d\tau,$$ where $\bar{x}$ is the average LED current and T is the switching period.

With a smoother LED current, the 5% settling time is easily read off the plot as illustrated in Figure 5.3.

ii. Efficiency

On the bench, efficiency is measured by using digital multimeters to measure the currents through and voltages across all elements in the circuit. The efficiency was then calculated as the power delivered to the LEDs alone normalized to the total power delivered to the RGB driver.

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b. Performance in Application Circuits

The initial design as illustrated in Figure 4.1a meets all the specifications set in chapter 3, repeated here as table 5.2. The circuit runs stable and accurately at input voltages ranging between 10V and 30V. The settling time never exceeds 30μs. The switch duty cycle ranges between 0% and 95% without causing inaccuracies or instabilities. The output current range is between 0A and 3A as specified and the output current ripple is always below 150mA. Efficiency is almost always greater than 85% and the output regulation is roughly within 4%[2].

PARAMETER		MIN	TYP	MAX	UNITS
Input Voltage		10	15	30	V
Settling time		1	10	30	μs
Switching Frequency		0.15	0.6	2	MHz
Switch Duty Cycle		0		95	%
Output Current		0		3	A
Output Current ripple				150	mA
Output regulation			1	4	%
Quiescent Current			5	6	mA
Reference Voltage		0		1.25	V
Efficiency		85	92		%

Table 5.2: Specifications for Multiple LED Driver

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[2] The 4% output regulation was systematic and is probably a result of the inaccuracies of the 1% resistors in the current sensing circuit.

On a system level, the RGB performs very well in producing a myriad of colors, by one, changing the amplitude of current running through the RGB LEDs and two, changing the on-time of the red, green and blue LEDs. See Figures 5.4 and 5.5 for some sample colors.
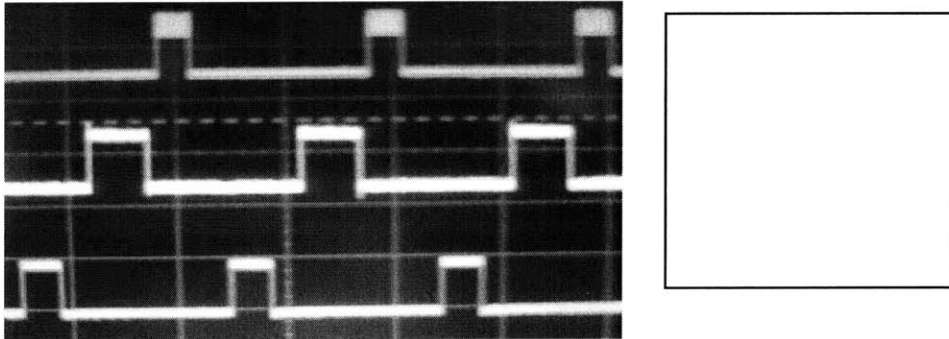

Figure 5.4: The top trace is the PWM signal sent to the switch on Fet connected in series to the red LED, the middle trace is the voltage signal sent to the green LED and the bottom signal lights up the blue LED. The vertical scale is 5V/div and the horizontal scale is 500µs/div. The reference voltage/current is constant at 0.3V. These on-times of the RGB LEDs and magnitude of the reference current produce a white color.
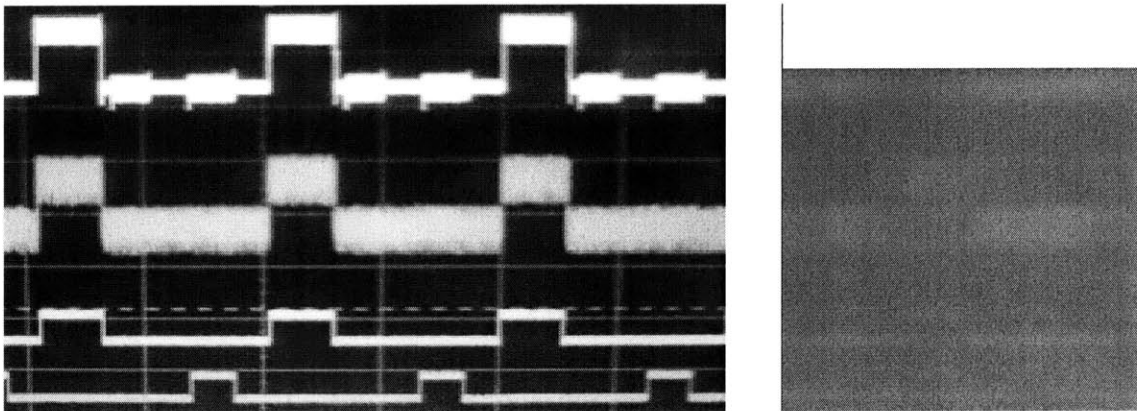

Figure 5.5: The top trace represents the current through the inductor. The second trace from the top represents the reference current. The third from the top waveform is the switch on Green LED voltage signal and the bottom waveform represents the switch on blue LED voltage signal. By doubling the amplitude of the current through the green LED to 750mA, the output color is green. The vertical scale is 500mA/div for the inductor and reference current waveforms, and 5V/div for the LED switch on voltage signals. The horizontal scale is 500µs/div.

The waveforms predicted in the SPICE model are very close but do not exactly match the waveforms of the breadboard circuit. For example, with the input voltage set at 15V, the

output inductor at 33μH, the output capacitor at 850nF, the damping resistor at 1Ω and the switching frequency at 290kHz, the SPICE waveforms mimic the bench results but only to a certain degree. This is illustrated if Figures 5.6 to 5.9.
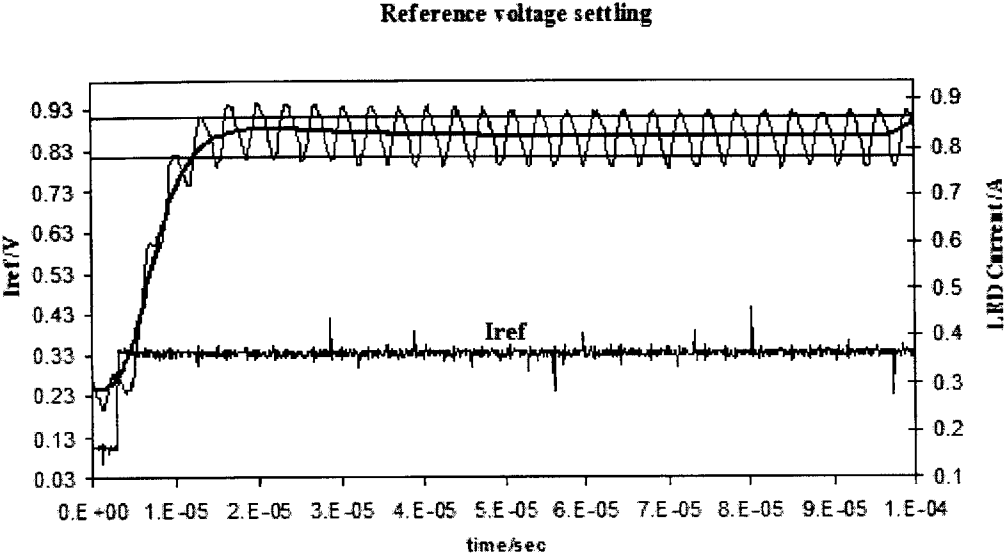

Reference voltage settling

Figure 5.6: Transient performance of the breadboard circuit for $V_{IN}=15V$, $L_{OUT}=$ 33uH, $C_{OUT}=850nF$, $f_{SW}=290kHz$, LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The reference current settles within 9μs.

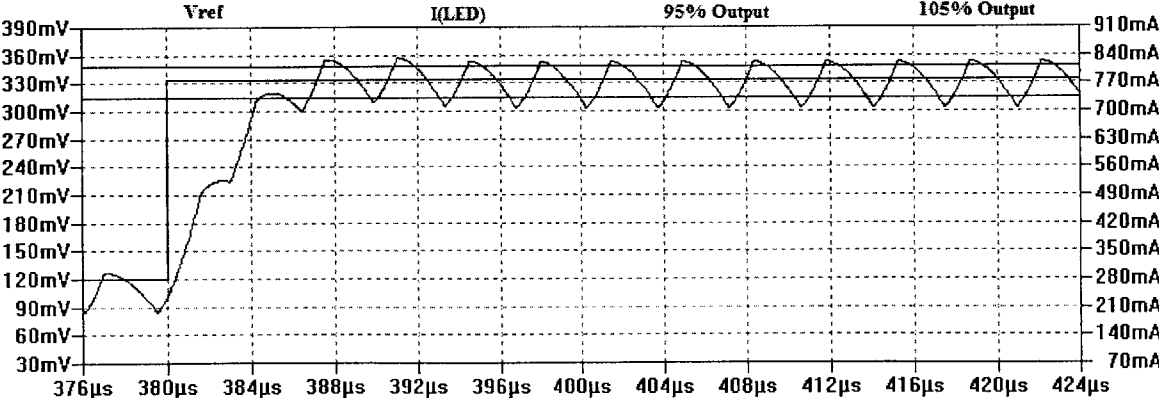**Figure 5.7**: SPICE model predicts a 7μs settling time. This is a simulation of the experiment of Figure 5.6.

One reason why the bench pictures may not exactly match the SPICE pictures is that the current settling also depends on the exact time when the step occurs. For instance in

Figure 5.6, the step occurs in the middle of a switching period. Meanwhile the step occurs almost at the beginning of a switching cycle in Figure 5.7. This adds a difference of roughly a half of a period to the settling times and reflects the time-varying nature of the switching system. If this error is accounted for, one can confidently say that the SPICE simulations do follow the bench results very closely.
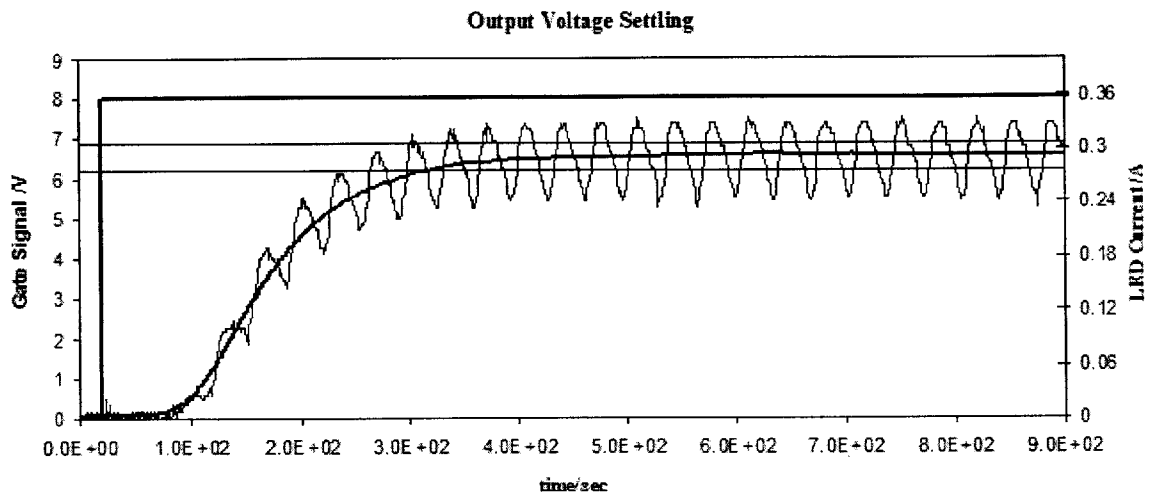

Figure 5.8: Breadboard circuit yields a 30μs load step settling time. V_{IN}=15V, L_{OUT}= 33uH, C_{OUT}=850nF, R_{OUT}=1Ω, f_{SW}=290kHz, LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor.
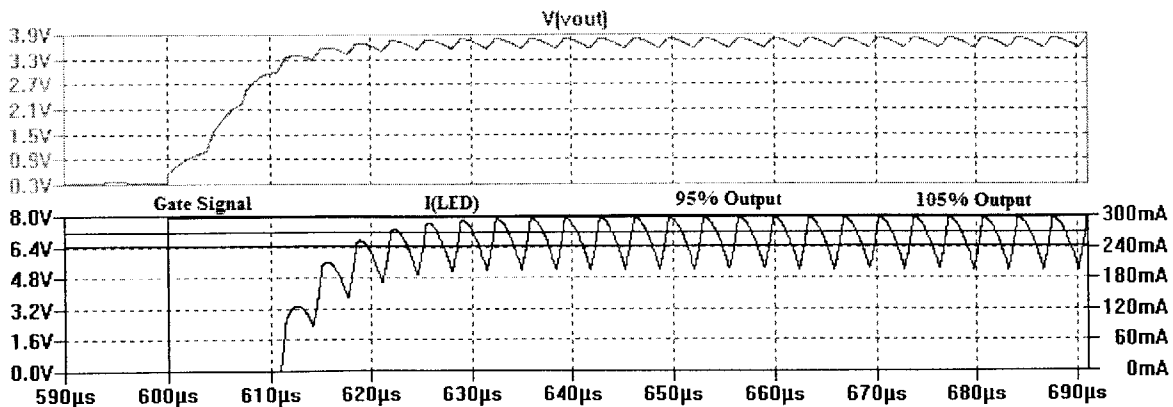

Figure 5.9: Simulation yields a 27μs output current step settling time. This is a simulation of the experiment of Figure 5.8.

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The large reference current step transient performance is ignored in this chapter. The reason behind this decision is that, the experiments did not include anti-windup circuitry in the compensator. To achieve the anticipated performance, the circuit designer will have to include anti-windup circuitry or design the compensator such that duty cycle saturation never occurs. Hence, we concentrate on the small reference current step settling and the output current settling in this chapter. We reserve the rest of this chapter examining how the settling time varies under different operating conditions.
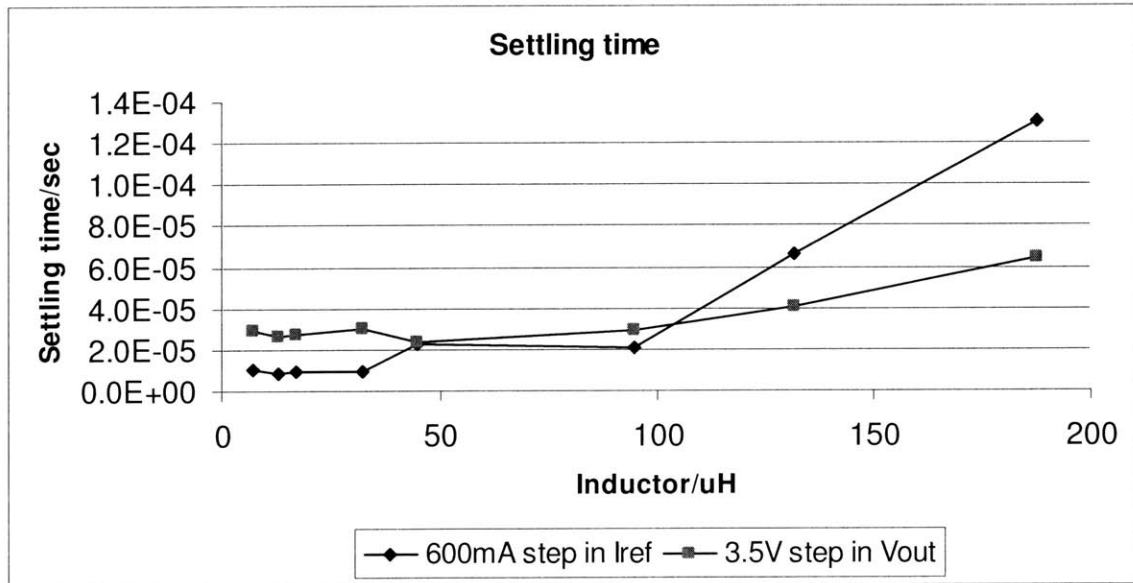
i. Settling time

Inductor size

Figure 5.10: Experimental results showing LED current settling to 5% of final value vs. inductor size for the circuit of Figure 5.1. V_{IN}=15V, C_{OUT}=1μF, R_{OUT}=1Ω, f_{SW}=290kHz, load for the reference current step is LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The load step is a switch from a Schottky to the 3 parallel connected LXHL_PM09.

Figure 5.10 shows the settling time responses to reference and output voltage steps. (Steps are from 250mA to 770mA in reference current, and from 0.37V to 3.7V in output current). With an output inductor sized below 33μH, the settling times for reference current steps and output current steps stay relatively constant at 7μs and 30μs respectively. Sized above 95μH, the output inductor appears to control the settling times in a monotonic (approximately linear) fashion. This is an indication that the slew rate of the inductor is setting the settling times. At this point the circuit has entered large signal mode, the duty cycle is saturating, and the inductor size is beyond the critical inductance level. That being said, the amount of ripple when the inductor sizes lower than 33μH, violate the output ripple specification, thereby limiting the practical inductor size to the range (33μH, 95μH).

Output Capacitance

Figure 5.11 below shows settling time responses to reference current steps and load steps for different capacitor values. (Steps are from 250mA to 770mA in reference current, and from 0.37V to 3.7V in output current). Examining these results, it may be concluded that it does not make sense to control output ripple with output capacitance greater than 1μF, as this greatly impedes settling. With large capacitors, the settling times are no longer determined by a high bandwidth provided by the compensation, but is controlled by how fast the output capacitor can slew to the output voltage needed for the LED to sink the correct current. The fact that the output ripple is decent with a 1μF output capacitor in series with a 1Ω resistor confirms that designing with the 1μF capacitor is a good solution.
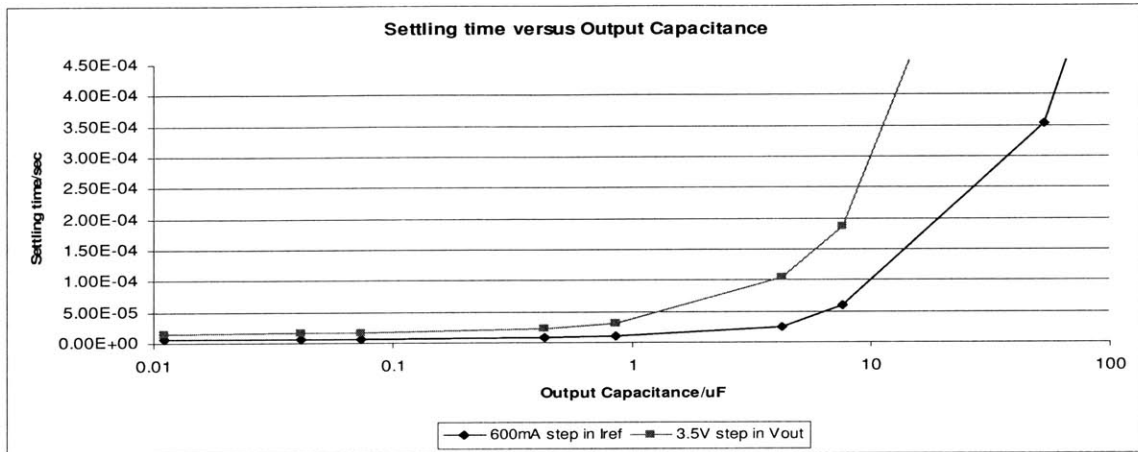
Figure 5.11: Experimental results showing LED current settling to 5% of final value vs. capacitor size for the circuit of Figure 5.1. V_{IN}=15V, L_{OUT}=33µH, R_{OUT}=1Ω, f_{SW}=290kHz, load for the reference current step is LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The load step is a switch from a Schottky to the 3 parallel connected LXHL_PM09. Output capacitors larger than 1µF greatly increase settling times.

Output Resistor

Figure 5.12 shows how variation in the damping resistance in series with the output capacitor affects settling time. As predicted in the *Design and Simulation* chapter, to first order the settling times do not vary with the output resistor size. Furthermore, efficiency is set independent of the output resistor size (note scale ranges). Figure 5.13 shows how the damping resistor affects efficiency for the condition: V_{IN}=15V, L_{OUT}=33µH, R_{OUT}=1Ω, f_{SW}=290kHz, frequency of switching between different LEDs≈8kHz. This proves that adding on the damping resistor to improve the peaking of the currents is a clever strategy as neither settling times nor efficiency is compromised. Figures 5.12 and 5.13 prove that both settling times and efficiency remain relatively constant.

V_{IN}=15V, L_{OUT}=33µH, C_{OUT}=1µF, f_{SW}=290kHz.

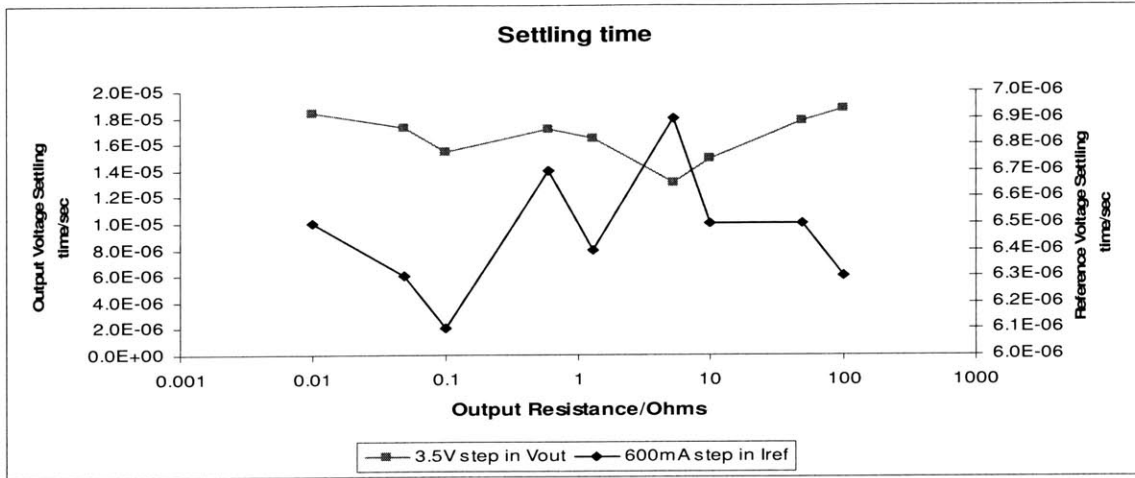**Figure 5.12:** Experimental results showing LED current settling to 5% of final value vs. damping resistor size. V_{IN}=15V, L_{OUT}=33µH, C_{OUT}=1µF, f_{SW}=290kHz, load for the reference current step is LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The load step is a switch from a Schottky to 3 parallel connected LXHL_PM09. Settling times remain relatively constant with different output resistor sizes.
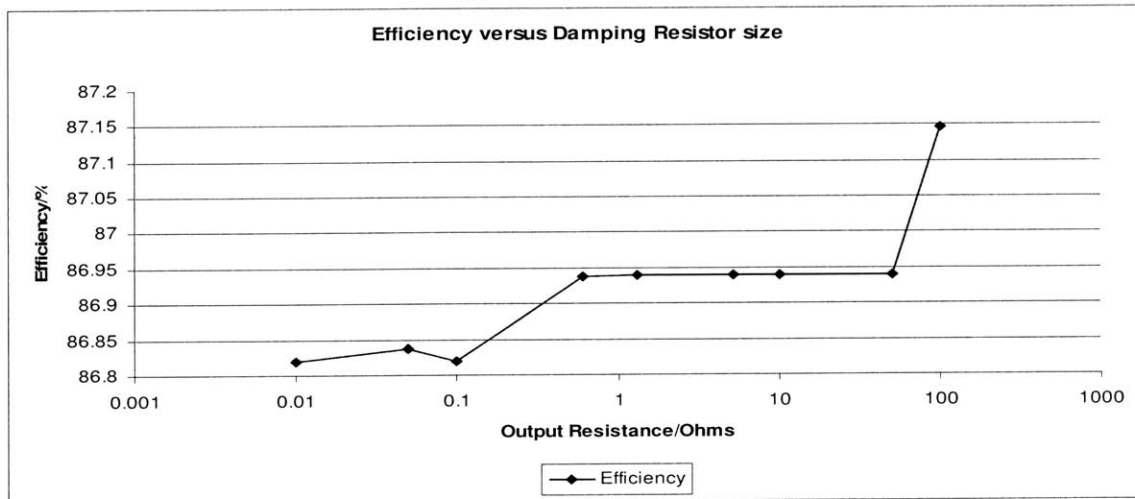

Figure 5.13: Experimental results showing efficiency vs. damping resistor size. V_{IN}=15V, L_{OUT}=33µH, C_{OUT}=1µF, f_{SW}=290kHz, load for the reference current step is LED = 3 parallel connected LXHL_PM09 in series with a 1Ω resistor. The load step is a switch from a Schottky to 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The LEDs are switched at a frequency≈8kHz. The output resistor size has very little or no impact on efficiency.

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Input Voltage

Response speed to positive steps in reference current and output voltage were measured as a function of input voltage, As expected, positive slew rate of current increases with input voltage. (Negative slew rate of output was not measured.) Generally, the settling times fall with higher input voltages. This is because the positive slope of the inductor current is steeper with higher input voltages. The steeper inductor current slope corresponds to higher gain at the compensator stage and faster current correction for the positive step only.
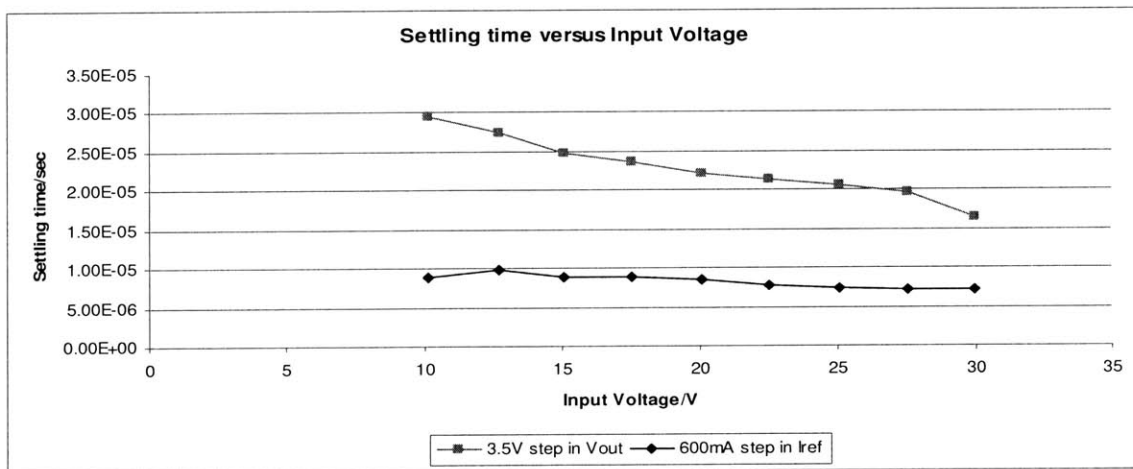

Figure 5.14: Experimental results showing LED current settling to 5% of final value vs. input voltage for positive steps in reference current from 250mA to 770mA and output voltage from 0.3V to 3.7V. L_{OUT}=33μH, C_{OUT}=1μF, R_{OUT}=1Ω, f_{SW}=290kHz, load for the reference current step is LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The load step is a switch from a Schottky to the 3 parallel connected LXHL_PM09. Higher input voltage translates to higher gain at the compensator and faster current correction.

Frequency

Scaling the circuit up in frequency, scales down the settling times. For this experiment, the frequency of the sawtooth was reset from 290kHz to a different frequency. The amplitude of the sawtooth was kept constant, while the sizes of capacitors and inductors in the circuit were scaled using this formula: $Newsize = Originalsize * \dfrac{290kHz}{Newfrequency}$.
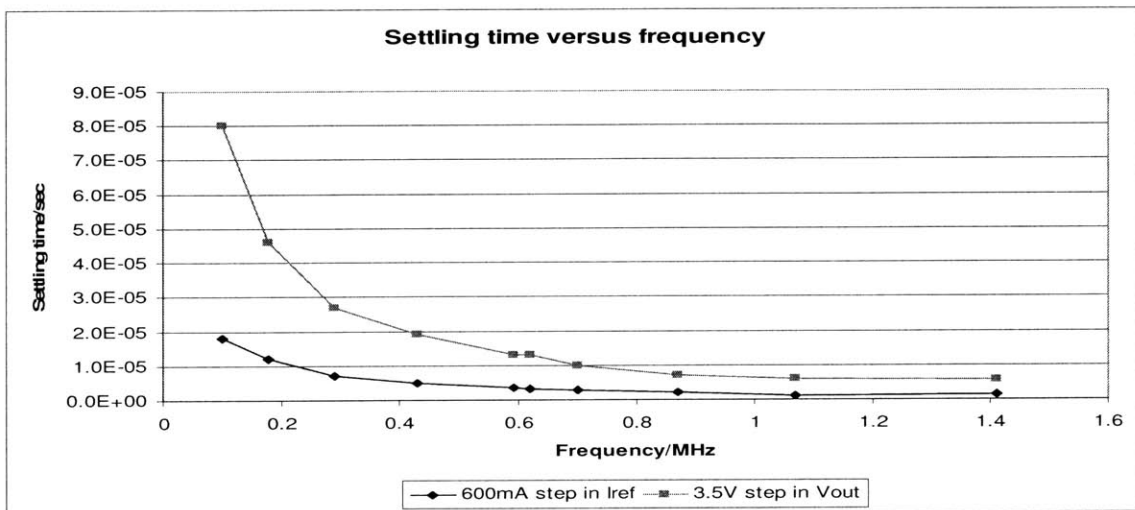

Figure 5.15: Experimental results showing LED current settling to 5% of final value vs. frequency for positive steps in reference current from 250mA to 770mA and output voltage from 0.3V to 3.7V. At 290kHz switching frequency, L_{OUT}=33μH, C_{OUT}=1μF, R_{OUT}=1Ω, Cp= 22pF, Cz=330pF. The load for the reference current step is LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. The load step is a switch from a Schottky to 3 parallel connected LXHL_PM09. These results were obtained by running the circuit at a 15V input voltage. Scaling up frequency scales down the settling time.

ii. Efficiency

Here we experimentally explore the impact of the input voltage, the output current, the

output inductor size and the switching frequency on the efficiency of the circuit.

Input Voltage

Figure 5.16 shows efficiency vs. input voltage. At higher input voltages we have larger
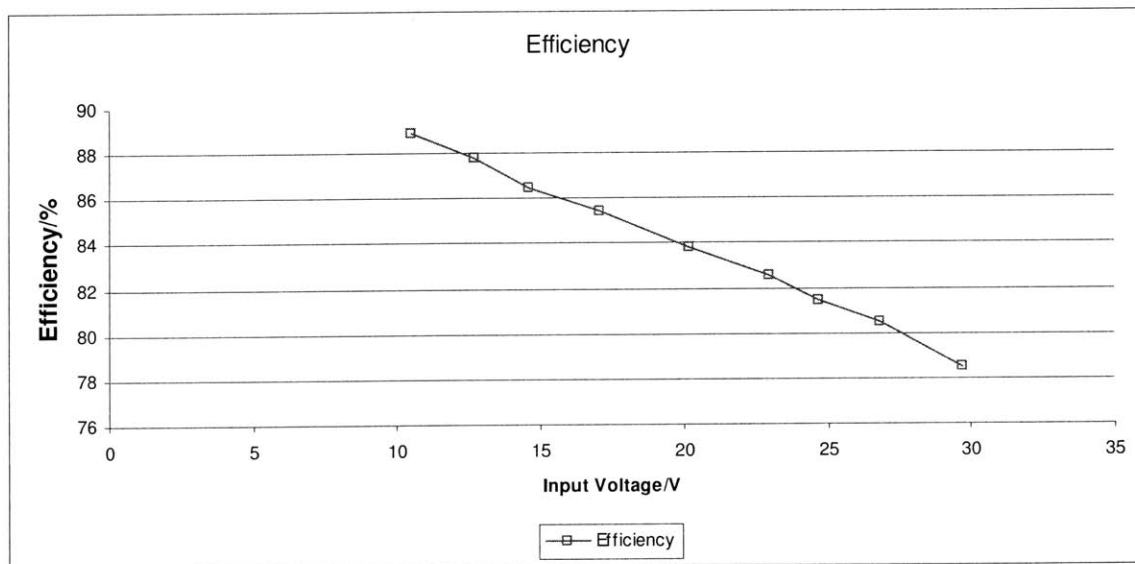
stress on the buck switch, wasting power.

Figure 5.16: Experimental results showing efficiency vs. input voltage. $L_{OUT}=33\mu H$, $C_{OUT}=1\mu F$, $R_{OUT}=1\Omega$, $f_{SW}=290kHz$, load/LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. Frequency of switching between LEDs $\approx$ 8kHz. Higher input voltage operation degrades efficiency

Output Current

Figure 5.17 shows efficiency vs. output current. At low output currents, the fixed losses in the system contribute to a higher percentage of the overall total power dissipation.
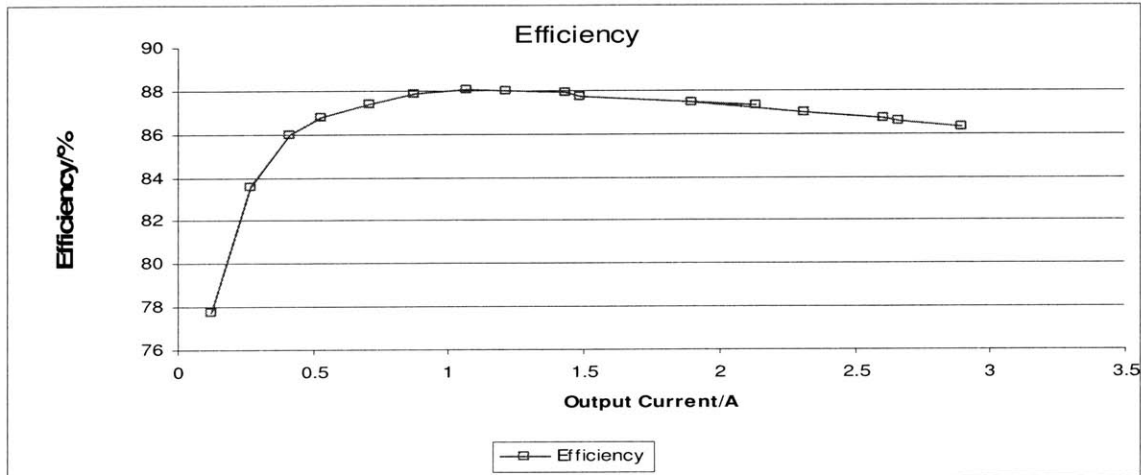

Figure 5.17: Experimental results showing efficiency vs. output. V_{IN}=15V, L_{OUT}=33μH, C_{OUT}=1μF, R_{OUT}=1Ω, f_{SW}=290kHz, load/LED is 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor. Frequency of switching between LEDs ≈ 8kHz.

Output Inductor

Here, we see how Figure 5.18 shows the system efficincy vs. inductor size. (Inductor types are indicated in table 5.1.) The on-resistance of the output inductor influences efficiency. There is also added loss effect of increased ripple in the devices for low inductance values Figure 5.18 should be interpreted as particular case. It in no way describes a general trend, as the on-resistance of the inductors is very specific to the specific inductors used in the circuit. However, all things being equal we expect efficiency to fall as the inductor size shrinks below a certain limit, because the conduction losses increase due to an increase in the RMS of the inductor current and device currents.
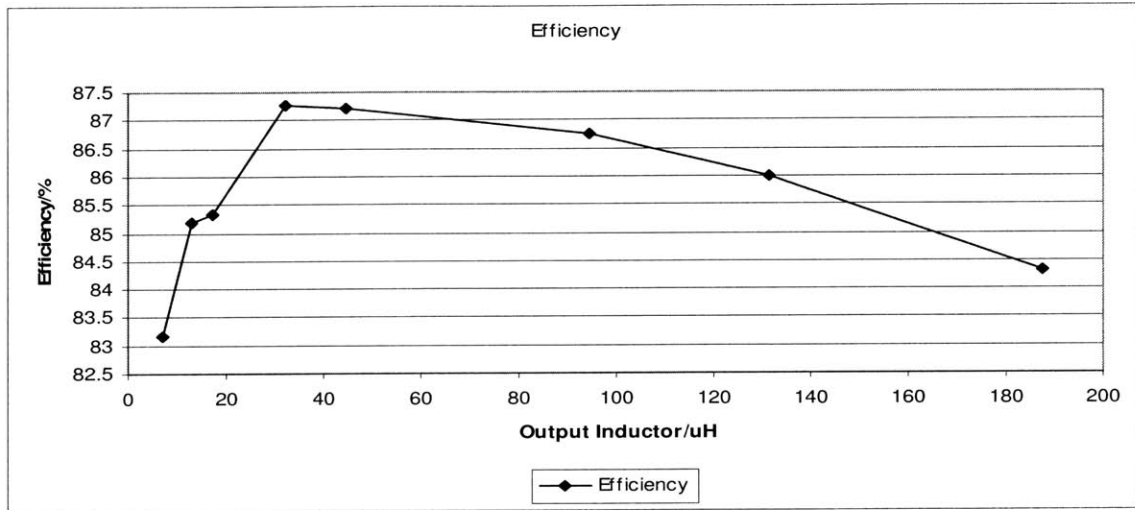
Figure 5.18: Experimental results showing efficiency vs. inductor size. V_{IN}=15V, C_{OUT}=1μF, R_{OUT}=1Ω, f_{SW}=290kHz, load/LED = 3 LXHL_PM09 in series with a 1Ω resistor. Frequency of switching between LEDs ≈ 8kHz.

Frequency

The power dissipated by the core of the inductor and the switch losses increase with increasing switching frequency. Conduction losses on the other hand decrease with increasing switching frequency because of lower RMS inductor current ripple. The combination of these two relationships produces the plot below (Figure 5.19). For this experiment, the frequency of the sawtooth was reset from 290kHz to a different frequency. The amplitude of the sawtooth was kept constant, while the sizes of capacitors and inductors in the circuit were scaled using this formula:

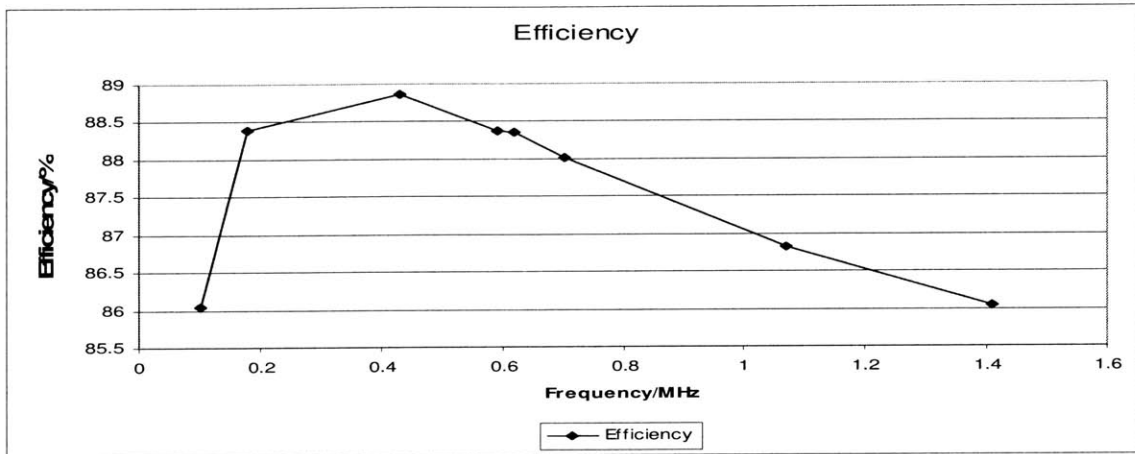$$Newsize = Originalsize * \frac{290kHz}{Newfrequency}.$$

Figure 5.19: Experimental results showing efficiency vs. frequency. At 290kHz switching frequency, L_{OUT}=33µH, C_{OUT}=1µF, R_{OUT}=1Ω, Cp=22pF, Cz=330pF. The load/LED = 3 parallel connected LXHL_PM09, each in series with a 1Ω resistor Frequency of switching between LEDs ≈ 8kHz. These results were obtained by running the circuit at a 15V input voltage.

c. Solution integration in IC

When implemented on an integrated circuit, the solution should be considerably more efficient than its PCB counterpart. For one, a more efficient yet simple sawtooth generation circuit can easily be implemented in IC. The sawtooth generator circuit implemented on breadboard was with a high current comparator and an integrator connected in a loop. Although ideal for a discrete component circuit board because of its remarkable simplicity, this design is sorely inefficient. In an integrated chip however a simple, cheaper and efficient alternative can be easily designed in. Furthermore, on the PCB board, some latches and buffer stages were added to keep the sawtooth and clock signal robust against noise. In IC all these can be marginalized to save on power.

All amplifications needed by the control circuit were done using operational amplifiers. For instance, the inductor current sense circuit was implemented using an operational amplifier and sense resistor. This need not be so on an integrated chip.

Additionally, needlessly large switches were used in the circuit. 30V-13A NMOS switches (FDS6670A) were used as the buck power switch and the LED turn on switches. 4A switches would have worked well.

Chapter 6 – Conclusion

a. Summary

The multiple RGB LED driver with independent PWM control is a feasible solution for backlighting flat panel displays. The ACMC control approach coupled with a parallel topology without ballasted current sources yields a fast and efficient solution. The settling times are reasonable and allow the driver to produce a very wide range of colors. Ultimately, the inductor size dictates the settling time of the output. For fast responses, the output inductor should be chosen from the range specified by equation 4.1,

$$\frac{V_{OUT} * sysHsense\,(j\omega_{SW}) * sysHE\,(j\omega_{SW})}{V_{SAW} * f_{SW}} \le L_{OUT} \le \frac{\Delta D_{MAX} * V_{IN} * \pi/2}{\Delta I_{OUT} * \omega_{BW}}, \quad \text{to} \quad \text{ensure}$$

minimum reference current step settling time. A high inductor in the range improves efficiency. Too high an inductor size or capacitor size will hurt the output current settling time.

b. Contributions

The work accomplished here has confirmed that a cheap, fast efficient multiple LED driver can be realized to drive the backlights of flat panel displays. Results obtained in simulation and on breadboard have provided great insight that indeed such a product is feasible.

c. Future Work

The next step will be to implement this solution in IC and to verify if it is a practical commercial product. Resources could also be invested into adding on an active ripple cancellation or use of a parallel interleaved power stage to see if that relaxes the constraints set by the design rules drafted in this paper.

d. Acknowledgements

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Appendix I

Schematic of Average Mode Controlled Multiple LED driver

```
V1 Vin 0 10
V6 V+ 0 15
Rf N002 N003 14.7k
Ri Vci N002 1k
Cz N003 Vca 330p
V7 VCC 0 8
XU4 VCC 0 INP SW D N014 LTC4440-5
R1 N004 R+ 196
R2 Vci N001 8.2K
R3 N001 Vout 196
R4 N004 0 8.2K
Lout SW R+ 33µ
D1 0 SW MBR745
V2 VGR 0 0
V3 VGG 0 10
V4 VGB 0 0
CoutB N008 0 1µ
M3 N010 VGS 0 0 FDS6670A
V9 VGS 0 PULSE(0 10 .4m 10n)
Rsense R+ Vout .01
M1 Vin D SW SW FDS6670A
V11 V- 0 -8
XU3 V* N002 V+ V- Vca LT1360
XU2 N004 N001 V+ V- Vci LT1360
V8 Iref 0 PWL(0 .5 .1m .5 .1001m 1 .2m 1 .2001m .1)
Rref V* Iref 1k
Cref V* 0 10n
D8 Vout N010 MBR745
C2 N014 SW 0.1µ
D9 VCC N014 D
XU1 Vsaw Vca V+ V- R LT1192
M2 N009 VGG 0 0 FDS6670A
D$R10 Vout N006 LUMILEDG
D$R11 Vout N007 LUMILEDG
D$R12 Vout N005 LUMILEDG
R13 N006 N009 3
R16 N007 N009 3
R17 N005 N009 3
R8 N011 N016 12k
R9 N015 N016 4.7k
C4 N015 N013 120p
R19 N013 N012 1k
D2 N011 N012 MMSD4148
V5 V+saw 0 4.5
V10 V-saw 0 -4.7
R20 N013 N017 20k
D3 N017 N011 MMSD4148
XU5 0 N013 V+saw V-saw N015 LT1192
XU6 N016 0 V+saw V-saw N011 LT1192
Cp N002 Vca 22p
A2 N018 0 0 0 0 P001 0 0 BUF
C3 N019 0 2.2n
A3 N019 0 0 0 0 N020 0 0 BUF
```

```
A4 N020 0 0 0 0 S 0 0 BUF
A1 S 0 0 0 0 S* 0 0 BUF
A9 0 S* Q* 0 0 Q 0 0 AND
A10 R 0 0 0 0 R* 0 0 BUF
A11 0 Q R* 0 0 Q* 0 0 AND
R7 INP Q 100
M4 INP R 0 0 VN222LL
XU7 N015 Vsaw VCC V- Vsaw LT1192
C5 N018 0 100p
R6 N018 Vsaw 200
Rout Vout N008 1
C1 Vin 0 10µ
R5 N019 P001 1k
D4 Vout Vin D
.model D D
.lib C:\Program Files\LTC\SwCADIII\lib\cmp\standard.dio
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Program Files\LTC\SwCADIII\lib\cmp\standard.mos
* Pre-filter
* Current Sense
* Sawtooth Generator
* Clock generator
* SR-LATCH\nEliminate effects of noise/ringing
* CLOCK
* Compensator
* PWM Comparator
* Gate Driver
.model IRF730 NMOS(Rg=3 Rd=8.8m Rs=6.6m Vto=3 Kp=66  Is=84p Rb=11.0m
mfg=International_Rectifier Vds=400 Ron=1 Qg=21n)
.model FDS6670A NMOS(Rg=3 Rd=8.8m Rs=6.6m Vto=3 Kp=66  Is=84p Rb=11.0m
mfg=International_Rectifier Vds=400 Ron=8m Qg=21n)
.model VN222LL NMOS(Rg=3 Rd=8.8m Rs=6.6m Vto=3 Kp=66  Is=84p Rb=11.0m
mfg=International_Rectifier Vds=400 Ron=7.5 Qg=21n)
.model LUMILEDG D(Ron=1  Vfwd=3.42 Iave=1.5 Ipk=1.5)
.lib LTC.lib
.lib LTC4440-5.sub
.backanno
.end
```

Appendix II

```
%ACMC Controlled Multiple LED Driver

%buck
Vin = 10;
Lout = 33E-6;
Cout=1E-6;
Rout=1;
RLED=1.04; %.017+(3.08/3)
Rs=.01;
fs=290E3; %switching frequency


s = tf('s');


%IL vs D, Transfer function of Inductor Current vs. Duty Cycle
CoutRout = 1/(s*Cout) + Rout;
ParallelZ = (RLED*CoutRout)/(RLED+CoutRout);
sysDivZ=(ParallelZ)/(s*Lout + ParallelZ);
sysGL=Vin*(1-sysDivZ)/(s*Lout);


%ILED vs IL, Transfer function of LED Current vs. Inductor Current
sysDivG= CoutRout/((CoutRout+RLED)); %bode(sysDivG);
sysG= sysGL*sysDivG;


%IL vs VCI, Transfer function of Sensed Current, VCI vs. Inductor
Current
R1=196;
R2=8.2E3;
sysHsense= R2*Rs*.8E7*(100E7)^4/(R1*(s+.8E7)*(s+100E7)^4);


%ACMC Control
%compensator

fGain=fs*Lout/(600e3*15e-6);


CZ=330E-12;
CP=22E-12;
RI = 1E3;
RF= 14.9E3;


ZF = 1/(s*CZ) + RF;
ZP = 1/(s*CP);
ZFparZP = ZF*ZP/(ZF+ZP);
sysD=ZFparZP/RI;


fz=zero(sysD);
fz=fz(3,1);
fp=pole(sysD);
fp=fp(4,1);


RDC=7.08E3; %DC gain of LT1360
```

```
sysHE = RDC*1000*-fp*.8E7*(100E7^4)*(s-fz)/(-fz*(s-
fp)*(s+1E3)*(s+.8E7)*(s+100E7)^4);


Vs=6; %Amplitude of Vsaw
sysHPWM=tf([1],[Vs])*fGain;
%fGain makes the PWM comparator model more accurate

%Open Loop to IL
sysL=sysHE*sysHPWM*sysGL*sysDivG;
sysLA = feedback(sysHE*sysHPWM*sysGL,sysHsense);

%Reference voltage or Reference current step
%Closed Loop to ILED
sysCL= sysLA*(1+(1/sysHE))*sysDivG;

figure;
grid;
hold;
step(sysCL, 'k');
x=10e-5*[0:1:10];
y=2.4*ones(1,11);
ylow=0.95*y;
yhi=1.05*y;
plot(x,ylow,'-');
plot(x,yhi,'-');
title('Reference voltage step response');


%Output current step
sysDivGL= CoutRout/(CoutRout + s*Lout);
sysLAV = -sysHE*sysHPWM*sysGL*sysHsense;

%Closed Loop to ILED
sysCLV=-sysDivGL*feedback(1,sysLAV,+1)*sysDivG;

figure;
grid;
hold;
step(sysCLV, 'k');
x=10e-5*[0:1:10];
y=-.1E-10*ones(1,11);
ylow=0.95*y;
yhi=1.05*y;
plot(x,ylow,'k');
plot(x,yhi,'k');
```

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Appendix III

Bill Of Materials

Component	Description	Device	Quantity
M1-M5	MOSFET	FDS6670A	5
M6	MOSFET	VN222LL	1
D1-D2	Schottky	MBR745	2
D3-D4	Diode	MMSD4148	2
D5-D10	Diode	P6KE30A	5
R11	LED	LXK2-PD12Q00	1
R12	LED	LXK2-PM14-U00	1
R13	LED	LXK2-PB14-N00	1
LXHL_PWO9 in series with 1Ω connected in parallel as load for high current tests	LED	LXHL_PWO9	3
U1-U2	Op-amp	LT1360CS8	2
U3-U7	Op-amp	LTC4440ES6-5	5
U8-U10	Op-amp	LT1190CS8	3
U11	Comparator	LTC1518CS	1
A1-A5	Inverter	DM74LS00N	1
A6-A7	Nand gate	SN74LS04N	1
Rsense	Resistor	0.01Ω, 5W, 0.1%	1
R1-R2	Resistor	196Ω, 1%, 1/8W	2
R3-R4	Resistor	8.2kΩ, 1%, 1/8W	2
Rout	Resistor	1Ω, 1%, 1/8W	1
R5	Resistor	100Ω, 1%, 1/8W	1
R6	Resistor	200Ω, 1%, 1/8W	1
Ri, R7, R8	Resistor	1kΩ, 1%, 1/8W	3
R9	Resistor	20kΩ, 1%, 1/8W	1
R10	Resistor	12kΩ, 1%, 1/8W	1
R14	Resistor	4.7kΩ, 1%, 1/8W	1
Rf	Resistor	15kΩ, 1%, 1/8W	1
Cp	Capacitor	Ceramic capacitor, 24pF 50V	1
Cf	Capacitor	Ceramic capacitor, 330pF 50V	1
Cout	Capacitor	Ceramic capacitor, 1μF 50V	1
C2-C6	Capacitor	Ceramic capacitor, 0.1μF 50V	5
C7	Capacitor	Ceramic capacitor, 2.2nF 50V	1
C8	Capacitor	Ceramic capacitor, 100p 50V	1

C9	Capacitor	Ceramic capacitor, 120p 50V	1
C1	Capacitor	Ceramic capacitor, 10μF 50V	1
Lout	Inductor	Inductor, SMT, 33μH, D03316P	1
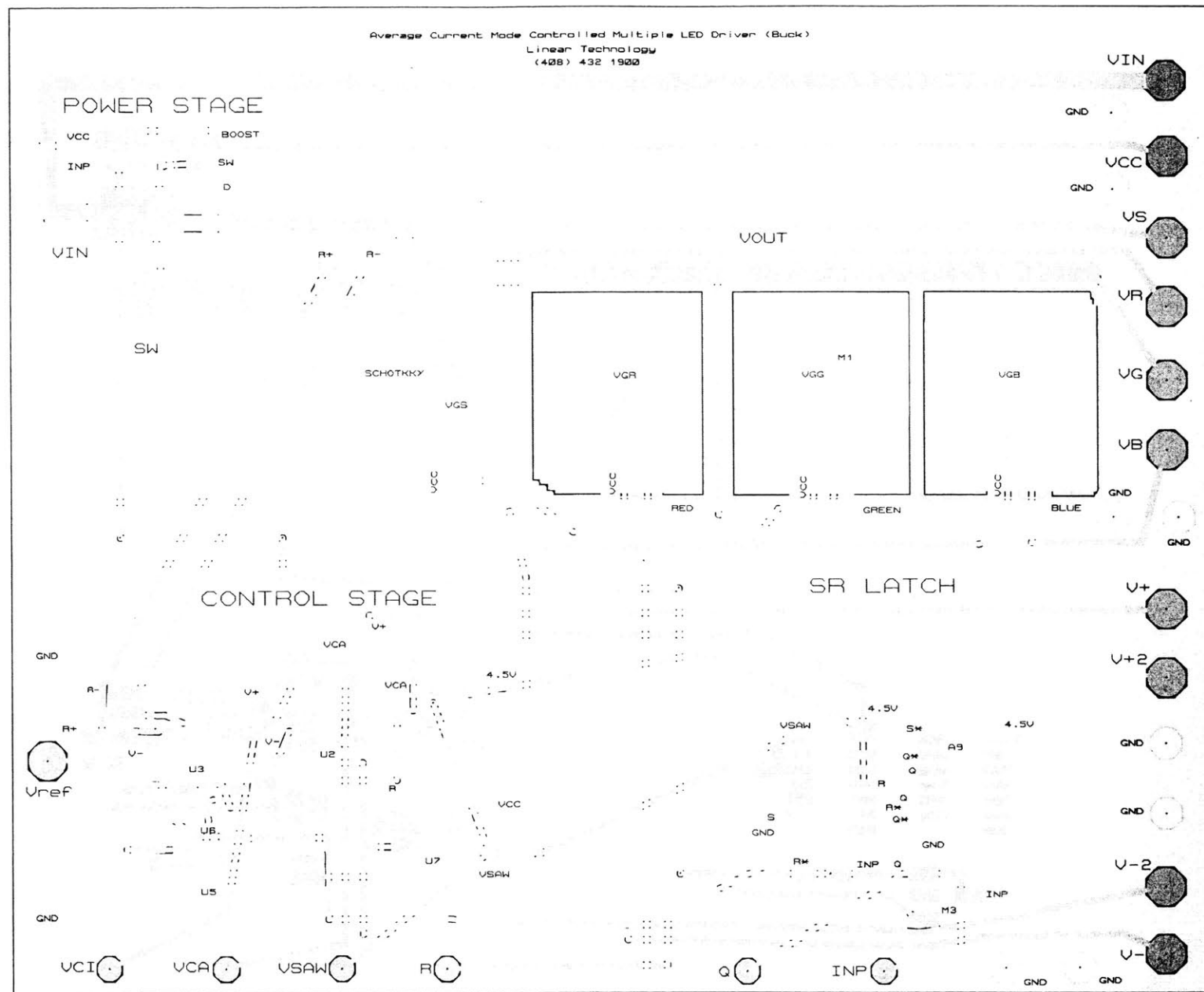
Prototype PCB Board Layout – Top and Bottom Layers

Prototype PCB Board Layout – Top Layer

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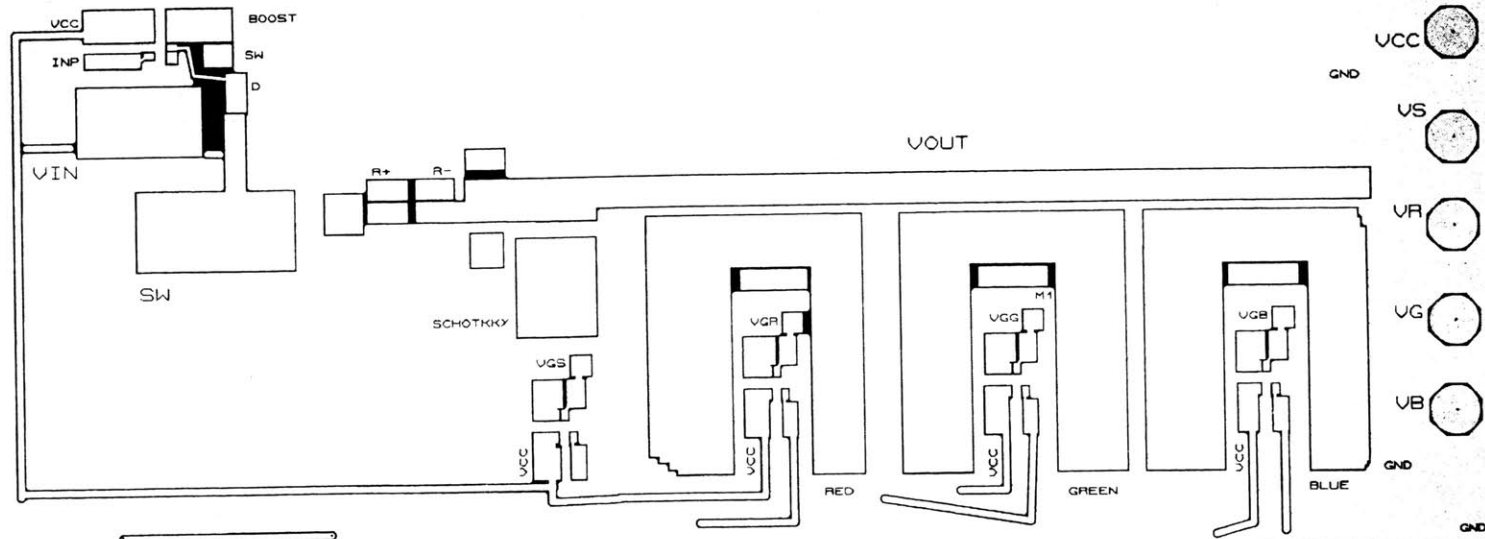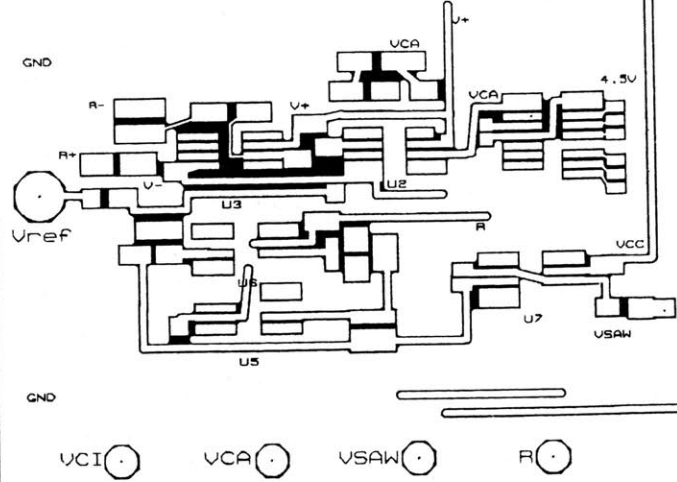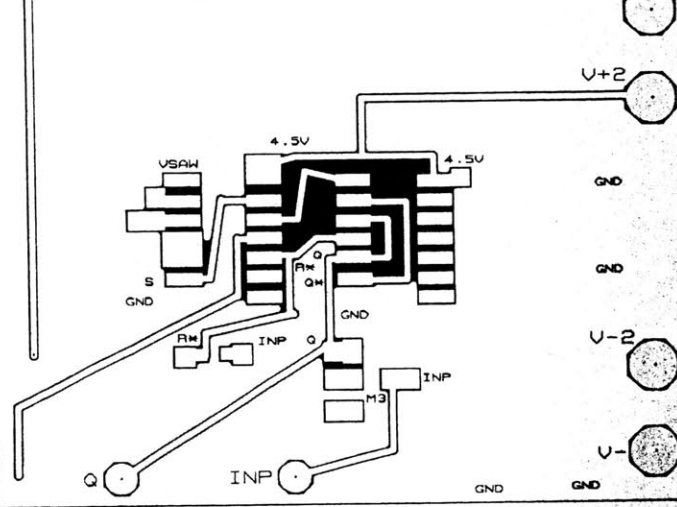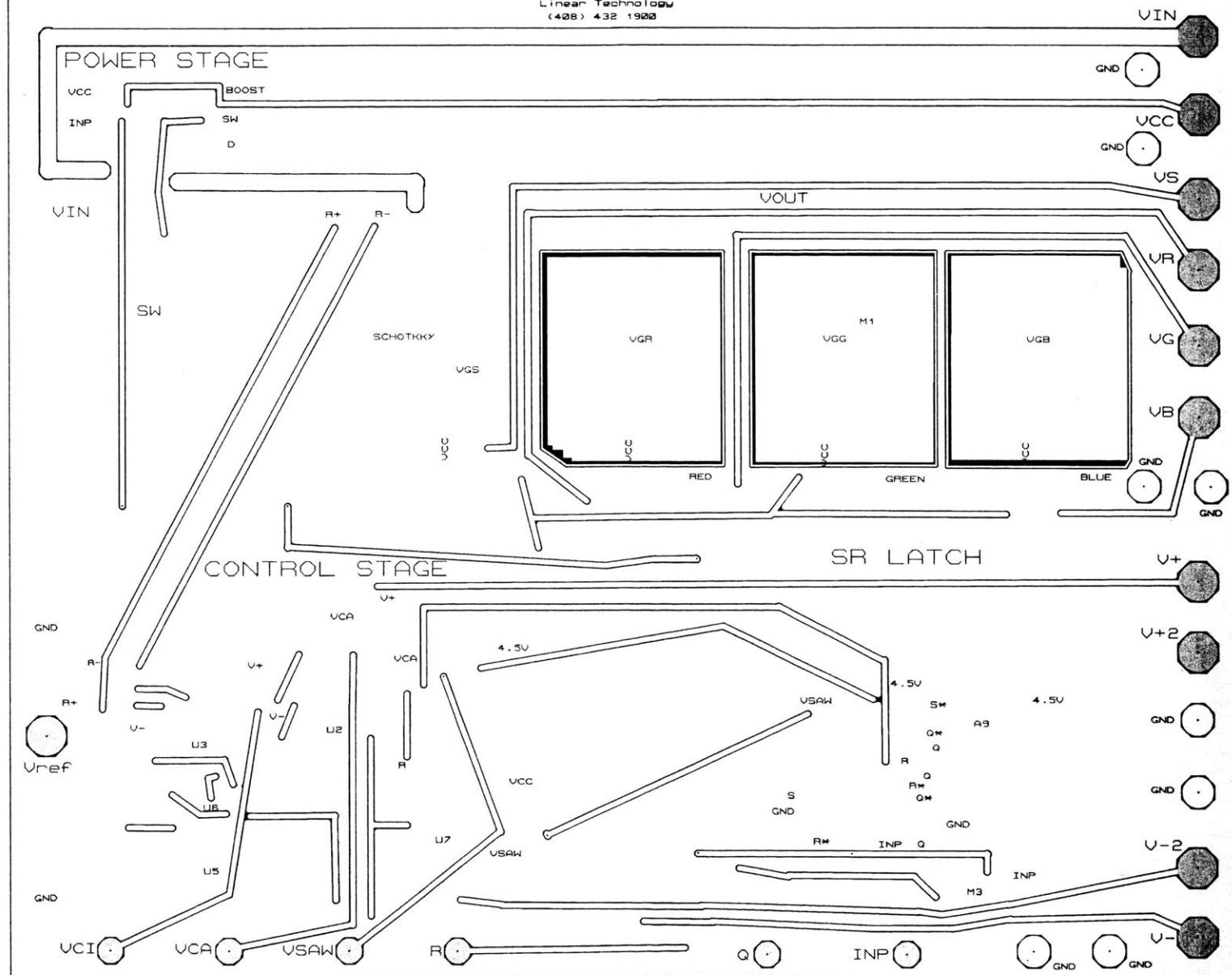
Prototype PCB Board Layout – Bottom Layer