

**A Statistical Metrology Framework for Characterizing
ILD Thickness Variation in CMP Processes**

by

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Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 1st, 1996.

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Abstract

Statistical metrology is a methodology for characterizing and modeling various sources of process variation. It uses electrical measurements, simulations, Design of Experiments, and interpolations to efficiently gather the large amount of data needed for statistical modeling and decomposition of variation into its constituent components. However, the implementation of statistical metrology can be prone to errors because there are many intricacies involved in designing a statistical metrology experiment. Therefore, this thesis presents a framework for the implementation of statistical metrology for characterizing ILD thickness in CMP processes. The framework encompasses test structure design, probe-layout design, die-layout design, advanced test structure design, process characterization, simulations, electrical characterization, interpolations, data organization, data conversion, and analysis. An application of this framework is also presented for an experiment performed on an advanced CMP process at LSI Logic Inc.

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Acknowledgements

I am truly thankful to Professor James Chung and Professor Duane Boning for their support throughout the project. Working for you both was a great experience.

Thanks very much to Brian Stine and Rajesh Divecha who have been instrumental in helping evolve statistical metrology into its current form. Brian was responsible for the development of the variation decomposition and analysis methods. Thank you also to Daniel Maung for spearheading the initial work on statistical metrology.

I thank Ashok Kapoor for supervising and encouraging my work at LSI Logic. Thank you to Sharad Prasad, Tom Mallon, and William Loh who have been very supportive in many aspects of my work. Many thanks to John Jensen, Reenie Ardans, and Julie Beaty for their invaluable help during the layout of the test chip. Jambu Palaniappan, Jon Owyang, Evelyn Nguyen, Emma Smith, and Lisa Phlegar have been very helpful in pushing the wafers through the fabrication process. Ana Ley and Minh Nguyen were instrumental during process characterization. Thanks also to Norman Pham, Wei-Mein Swen, Vera Li, and Peter Nguyen for their help with the electrical characterization. Jim Graf, Sanford Whitehouse, and Kevin O'Connor were helpful for the computer systems and programming support. Thanks also to Stanley Yeh, Roberto Sung, Ratan Choudhury, Satish Menon, Michael Lyu, Neal Callan and many others for the intriguing discussions.

My life at MIT would have been terrible without the companionship of my friends. Thank you to all my buddies for the wonderful times we had together. A note of thanks to Huy Le and Alicia Tan for helping me print and submit my thesis in time.

Without the love and support from my parents and my brother, I would never have achieved as much as I have today. They have sacrificed a great deal for my well-being, and I will eternally be grateful.

I dedicate this thesis to my loving wife, Michelle. Her love, devotion, and support has been the back-bone of my sanity at MIT. As I look back at my years at MIT, there is no doubt in my mind that she was the main reason why I succeeded in graduating from “Hell”. Thank you Michelle. You are the most wonderful thing that has ever happened to me.

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Chapter 1.

Introduction

1.1 Statistical Metrology and its Impact

Interconnect delay will dominate transistor gate delay as scaling continues into the sub-half-micron regime [1]. Interconnect delay dominance will dictate that better methods be developed to replace the “worst-case” interconnect design rules that are currently prevalent in industry. These “worst-case” design rules originate from the problem that interconnect variation is difficult to characterize, and is thus poorly understood and controlled. For instance, inter-level dielectric (ILD) thickness’ dependence on underlying interconnect features is difficult to characterize due to low measurement throughput¹ and measurement errors². Without the correct ILD thicknesses, capacitance and delay simulations will inevitably be incorrect, hence the reliance on “worst-case” design rules. There is thus an obvious need for a methodology to better characterize and model interconnect variation. With better interconnect models, designers can predict and account for the variation, hence decreasing the margin of error in their design tolerances. In addition to improving circuit design, process engineers can make use of the models to help control and reduce the process variation.

Statistical metrology is a technique which can be used to characterize and model interconnect variation, as well as other types of process variation³. It stresses the use of electri-

1. Cross-sectional SEMs cannot be used to collect the large amount of die-level data needed due to its destructive nature.

2. The beam spot-size for optical thickness measurements is about the same dimension as minimum pitched interconnect lines, hence beam misalignment and dispersion causes the beam to overlap the line-spacing regions. Thus, the ILD thickness values calculated by the equipment is incorrect.

3. Statistical metrology can be used to characterize process variation such as contact and via resistance variation. Its advantage over other types of metrology is greatest when utilized for characterizing variation of small structures, and when large amounts of data are needed.

cal test structures to generate the large amount of data needed for statistical modeling of variation. In the case of ILD thickness statistical metrology, capacitance simulations are also necessary to extract the ILD thickness from the electrical data. In addition, signal processing is performed on the data to decompose the ILD thickness variation into its constituent components, such as die-level and wafer-level components. These components are useful for statistical circuit design using Monte Carlo simulators. Statistical tools such as Analysis of Variation (ANOVA) are also applied to the ILD thickness data to model the different sources of variation.

1.2 Review of CMP Pattern Dependencies

Chemical Mechanical Polishing (CMP) is a widely used method for planarizing inter-level dielectrics. CMP utilizes a rotating pad to polish and planarize the dielectric in a slurry environment. CMP variation is not just location dependent wafer-scale variation, but includes pattern and location dependent die-scale variation as well. For example, a large M1 structure will generate a thicker ILD thickness above it than a small M1 structure after CMP. In addition, similar structures within a die may have different ILD thickness above it because of their different locations in the die. Some work on CMP pattern dependencies can be found in references [11, 12, 13, 14].

1.3 Thesis Motivation

The drawback of statistical metrology is that it can be a complicated process. Since statistical metrology is a recent and ongoing research effort at M.I.T. [2], there are numerous undocumented subtleties which should be heeded for statistical metrology to succeed. Without a guided framework on how to apply statistical metrology, the method is prone to measurement, simulation or analysis mistakes. This thesis presents a statistical metrology framework for characterizing the ILD thickness variation in CMP processes. It is the hope

of this author that the intricacies and procedures described in this thesis will make statistical metrology become accepted in industry as a reliable, efficient, and easily implementable tool for controlling interconnect variation.

1.4 Scope of Thesis

This thesis describes the procedures and subtleties involved in statistical metrology of ILD thickness. It spans from test structure design and measurements, to capacitance simulations and ILD thickness extrapolations, and to data organization and validation of assumptions. A framework application is also detailed for an experiment at LSI Logic Inc. which utilized the thesis procedures. As mentioned before, statistical metrology also includes signal processing for variation decomposition and statistical analysis for variation modeling. It is beyond the scope of this thesis to include detailed descriptions of how to perform the signal processing and statistical analysis. However, an overview of the variation decomposition and modeling is presented. Furthermore, normalized results from using the signal processing and statistical analysis are illustrated from the framework application example at LSI Logic Inc.

1.5 Organization of Thesis

This thesis is organized into two main parts. The first part is in Chapter 2. It describes the experimental design framework and the design and application issues involved in it. The important points include test structure and die layout design, process flow, simulations, electrical characterization, process characterization, data organization, and analysis.

The next chapter, Chapter 3, contains the second part of the thesis. It presents an example of an application of the statistical metrology framework at LSI Logic. It illustrates applications of the points in the Chapter 2, as well as oversights in the experiment at

LSI Logic. Finally, it presents the statistical analysis and signal processing results of the experiment.

Chapter 4 summarizes the important issues in statistical metrology of ILD thickness in CMP processes. It reemphasizes that statistical metrology is a powerful tool which can help model and control variation, if it is used carefully and within an organized framework.

Chapter 2

Experimental Design Framework

This chapter details the experimental design framework. The framework includes test structure design, probe layout design, and die layout design in sections 2.1 to 2.3. As will be explained consequently in section 2.4, the ILD thickness test structures used in previous masks, and in most portions of the current mask, have a few shortcomings. Some advanced test structures in the current mask which have been designed to correct these shortcomings are also described in that section. These advanced test structures are also used for verification purposes.

This chapter also contains process flow information and how it affects simulations and electrical measurements (section 2.5). Process characterization is important to determine the dimensions of the simulation structures, as well as confirm that the raw and interpolated data are correct. Section 2.6 describes different types of process characterization such as SEM-CDs (scanning electron microscopy critical dimensions), optical ILD thickness measurements, and profilometry.

ILD thickness is extrapolated using electrically measured data and capacitance simulations. Subsection 2.7.1 describes the procedures involved in the electrical characterization. The electrical measurements include capacitance as well as resistance measurements. The next subsection describes what structures are simulated, and how batch jobs are used to automate simulations. The subsections that follow explain how the electrical characterization is correlated with the simulations and how mathematical interpolations are used to yield the ILD thickness.

Since statistical metrology generates a large amount of data, care must be taken to organize the data so that it is easily read and analyzed. Some suggestions on how to do this are also presented in subsection 2.8.

The last section in this methodology chapter discusses validation of assumptions. Some assumptions which are investigated include confirming that the variation of field oxide thickness and first-level metal (M1) is small and easily neglected in simulations; yet another assumption is that large-area capacitors and small-area capacitors in dummy-line environments are virtually identical when it comes to ILD thickness variation.

2.1 Test Structure Design

Statistical metrology's back-bone is electrical test-structures. Without them, it is currently impossible or impractical for large amounts of data to be collected for statistical analysis and signal processing. For ILD thickness statistical metrology, there are capacitance and resistance test structures - the capacitors are used to measure capacitance which will be correlated with simulations, and the resistors are used to measure sheet resistance, and calculate critical dimensions of the interconnect lines. The resistors need to "look" like and be close to their corresponding capacitors since critical dimension variation is dependent on layout and die location.

2.1.1 Capacitance Test Structure

The basic capacitance test structure consists of a top metal (M2) plate and a bottom metal (M1) ladder-structure as shown in Figure 2.1. The M1 plate can be varied for different finger widths, spacings, and lengths, number of fingers, geometric orientation and neighborhood distances. The neighborhood distance is defined as the distance from the edge of the capacitor to the closest structure on M1, which will typically be dummy-lines. Examples of these capacitance test structures are the "L" capacitors, Block capacitors,

Uni-edge capacitors, and Area capacitors. The naming of these types of capacitor structures will be explained in consequent sections.

Some other capacitance test structures are the ILD blanket capacitors whereby the bottom plate is not fingered. These capacitors are used to characterize the wafer-scale ILD thickness, as well as characterize the ILD dielectric constant. Another kind of blanket capacitor is the field-oxide blanket capacitor, whereby the upper plate is M1 and the silicon substrate is the bottom plate. This capacitor can characterize the wafer-scale field-oxide thickness.

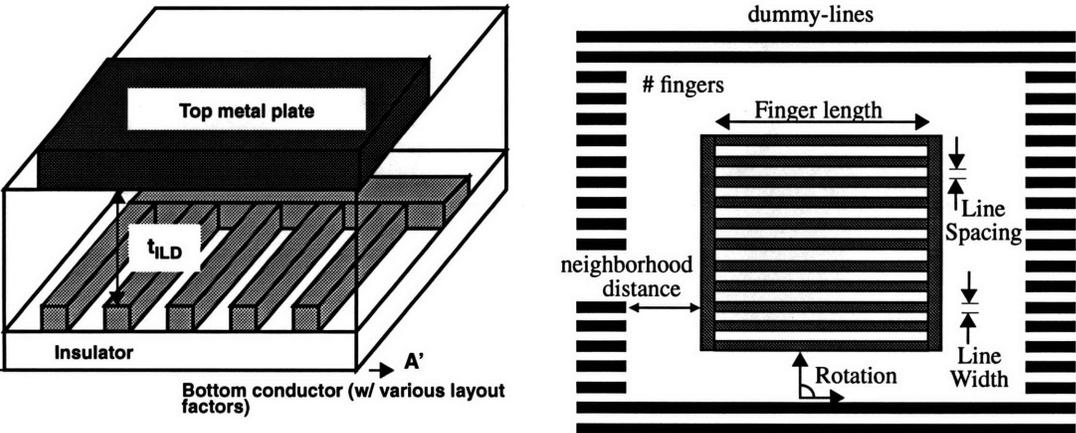


Figure 2.1: Capacitance test structure.

2.1.2 Resistance Test Structures

There are two types of resistors used which can be seen in Figure 2.2. The first is a symmetric van der Pauw structure, which resistance can be calculated to yield the sheet resistance. The right van der Pauw shown is superior to the left one because its center square is less susceptible to current crowding and electromigration effects (described consequently).

The second is a Kelvin structure, which is used in conjunction with the sheet resistance to calculate the critical dimension of the interconnect line widths [3]. Since critical dimension of interconnect lines vary with pitch and number of lines, the Kelvin structure is surrounded by dummy-lines which are pitched similar to its corresponding capacitor structure. For the sake of clarity, the dummy-lines are not shown in Figure 2.2.

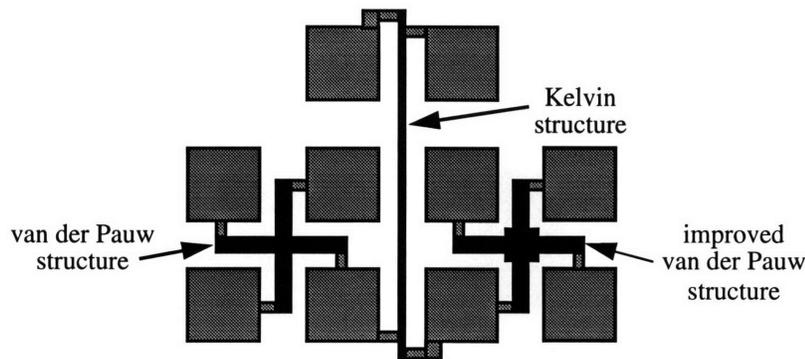


Figure 2.2: Resistance test structures.

2.1.3 Layout Factors

As mentioned in the previous subsection, the layout factors of interest are finger width, spacing, length, number of fingers, geometric orientation, and neighborhood distance. In order to model these layout factors and their effects on the ILD thickness variation, a Design of Experiments technique is used.

2.1.3 a) Design of Experiments (DOE)

DOE is a statistical technique that determines the appropriate experimental points to model a particular response, given a number of sources / factors and levels [4]. It allows the experimenter to trade-off the number of unique data points with the number of interactions which can be modeled. A full-factorial experiment allows all levels of interaction to be modeled, and it is recommended when there is no constraint on the number of data

points. A two-level full-factorial experiment for the six factors of concern, requires that there be 2^6 or 64 unique structures.

If certain factors require more than two levels, the design can be modified so that there are more levels for certain factors. This is because having only two data points to model some factors may not be sufficient, especially when their response may be non-linear. For instance, neighborhood distance is deemed an important factor which spans a large range. The size of the LSI test chip allows there to be four levels for the neighborhood distance, making the total number of unique structures to be 128 (with five other factors having two levels).

2.1.3 b) Centerpoint Structures

One way of modeling non-linear responses while not making the number of unique data points too large, is to use a centerpoint structure. A centerpoint structure is essentially a unique structure which has the center levels for all the factors.⁴ The centerpoint is useful for determining whether the response curve for the high and low factors is linear, concave or convex.

2.1.3 c) Structure Replications

Replications serve two purposes. The first is so that a die and wafer map can be generated for one type of structure to see how location affects the response. The second is to ensure that there are extra structures to rely on if any errors occur in the first set of structures. The first purpose can be achieved by replicating the centerpoint structure. It is best to have about one replicate for every 1 mm x 1mm area so that the location effects can be modeled to a fine-grain. The second purpose is important, yet costly because it doubles (at

4. Since most layout tools cannot accommodate diagonal layout, a center level for geometric orientation might not be feasible (even if it is feasible, it is not a simple task). In such a case, two centerpoints can be designed, each with one geometric orientation.

least) the number of structures. Depending on how much space there is on the die, the designer must decide if it is worthwhile doubling the number of structures to ensure that errors do not cripple the experiment.

2.1.4 Setting the Factor Levels

When deciding what values to assign the factor levels, there are a number of issues to keep in mind. The concerns include practicality, measurability, and layout area [5].

2.1.4 a) Realistic Factor Levels

First and foremost, factor levels must span a range which is used in real-life chips. For example, it is possible but foolish to set finger width levels at 0.4 μm and 100 μm . With current technology, 0.4 μm interconnect widths cannot be reliably implemented, and 100 μm interconnect widths are never used in lower metal layers.

It is best to have the most commonly used interconnect width and spacing as two of the factor levels. Most of the time, the most commonly used widths and spacings are the minimum dimensions allowed by the design rules (to save area). Therefore, they are usually feasibly used in the test structures since they do not violate any area or process constraints.

Setting the maximum interconnect width should be influenced by the typical clock-line widths in real-life chips. Power bus lines are less important since there is not much concern about their capacitance or delay performance.

The maximum interconnect spacing should also be affected by the maximum spacing value that is repeated for several lines on real-life chips. Spacings that happen once for a particular area are better modeled by the neighborhood distance. The minimum level for neighborhood distance should be set at the minimum spacing allowed by the design rules.

Typical maximum values go into the hundreds of microns, such as when blocks of interconnect lines are separated from another block by a few hundred microns.

2.1.4 b) Measurable Capacitance Values

The next concern is that the capacitors must yield a capacitance that is large enough to be measured reliably (at least 0.5 - 1.0 pF). Therefore, the capacitors must have a large enough area to yield the needed capacitance. This minimum area is of course dependent on the process which is used to fabricate the devices, particularly the ILD thickness and dielectric constant. It also depends on how much parasitic capacitance the probe-card yields; the equipment error is proportional to the magnitude of the total capacitance, hence if the parasitic capacitance is too large, the error might be significant when compared to the device capacitance. Parasitic capacitances of 1.5 pF or less is usually acceptable. Probe-card parasitic capacitances can be minimized by using co-axial tips and traces (wires), or blade traces, and low capacitance board material. For a typical ILD thickness of one micron, and a dielectric constant value of four, the capacitor plate should be 150 μm x 150 μm large.

2.1.4 c) Layout Area Trade-offs

The amount of layout area available also affects how one sets the factor levels. For example, consider a design which requires 32 capacitors to be lined up along a die edge with their fingers parallel to that die edge. 16 capacitors have a finger length of L , and the other 16 have a finger length of $2L$. All the capacitors have a neighborhood distance of ND which is defined as the distance from capacitor to capacitor, as well as capacitor to die edge. It is simple to see that the design is constrained by die length, $DL = 32\left(\frac{L+2L}{2}\right) + 33ND$. The designer must thus decide how to trade-off finger length and neighborhood distance, for fixed die size and number of structures.

2.1.5 Layout Considerations

When designing the layout of the test structures, there are several points to consider. This subsection describes some of these points, which include the need for metal plate overlap [5], the minimum Kelvin length, and the minimum width of the van der Pauw lines. Neglect of these issues may lead to errors in the capacitance and resistance measurements.

2.1.5 a) Capacitor Plate Overlap

During the fabrication process, each mask layer is aligned to the previous one by the stepper. There is inevitably a stepper misalignment error which ranges from about 0.1 micron to around 0.3 micron for a typical 0.5 micron gate length technology. For two equally sized capacitor plates (fingered bottom plate), this misalignment means that the capacitance measured between M1 and M2 is inversely proportional to the misalignment error (Figure 2.3). However, if the top capacitor plate is larger than the bottom plate by the misalignment error on each side, then the measured capacitance is not as dependent on the misalignment error. This is because the fringe capacitance is smaller than parallel-plate capacitance. Since the motive is to measure capacitance which varies due to different ILD thicknesses instead of misalignment error, the capacitor with differently sized plates is the superior test structure.

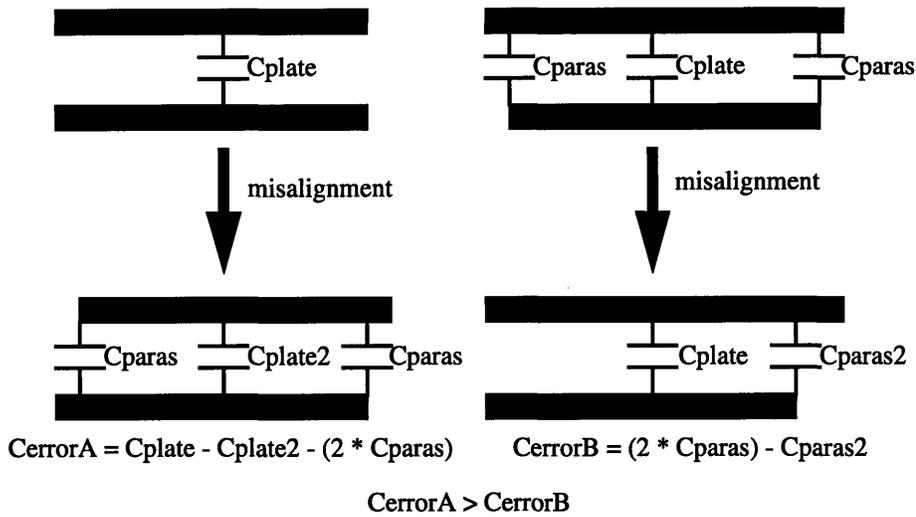


Figure 2.3: Using overlapping plates to minimize misalignment error.

2.1.5 b) Minimum Kelvin Length

The Kelvin resistor is essentially a long metal line with two probes at each end. It is used together with the van der Pauw structure to calculate the critical dimension (or width) of the line. The following is the well-known resistance formula used for critical dimension calculation [3]:

$$R_{\text{kelvin}} = R_{\text{sheet}} \frac{(L \pm \Delta L)}{(W \pm \Delta W)} \quad (2.1)$$

where R_{kelvin} is the Kelvin resistance, R_{sheet} is the van der Pauw sheet resistance, L is the drawn length of the Kelvin, W is the drawn width of the Kelvin, ΔL and ΔW are the variation of the Kelvin length and width respectively.

Bringing the width to the other side yields the following:

$$W \pm \Delta W = \frac{R_{\text{sheet}}}{R_{\text{kelvin}}} (L \pm \Delta L) \quad (2.2)$$

Since we calculate $W \pm \Delta W$ assuming $\Delta L = 0$, the percentage error in calculating the $W \pm \Delta W$ is:

$$W_{error} = \frac{2\Delta L}{L \pm \Delta L} \quad (2.3)$$

Therefore, assuming the error in calculating the critical dimension should be kept within one percent, and the length variation is 0.5 micron peak to peak, then the Kelvin resistor length must be a minimum of fifty microns long. In addition, from Equation 2.2, it can be seen that if $L \rightarrow W$, then the error in calculating ΔW , approaches ΔL . Since this error is large with respect to W , the L/W ratio must be about ten or more.

2.1.5 c) Minimum van der Pauw Line Width

The van der Pauw's resistance is always much smaller than the Kelvin structure's resistance because a van der Pauw is essentially a one square long Kelvin. This resistance is determined by dividing a measured voltage by a forced current. If the resistance is too small for a particular current value, the voltage may be too small to be accurately measured by a voltmeter. Therefore, in order to measure the small van der Pauw resistance, a large current must be forced. Some values illustrate this problem. Voltmeters usually have error values about a hundred microvolts or more. Sheet resistance of metal is about fifty or more milliohms/square. To have less than one percent error, the current forced must be at least 0.2 amperes. Note that many current sources in parametric test systems have limits of about 0.1 - 0.2 amperes.

However, if the current applied to the van der Pauw is too large, electromigration problems may arise. This typically happens for current densities of around $10 \text{ mA}/\mu\text{m}^2$ or more. For short duration resistance measurements, this limit can be increased to about $100 \text{ mA}/\mu\text{m}^2$. For a 0.8 micron thick metal and a current of 0.2 amperes, the van der Pauw width must be larger than 2.5 micron. A conservative width will be about twice the minimum calculated width which prevents electromigration, however, the wider the structure, the better.

2.1.5 d) Neighborhood Distance Definition with Dummy Lines

Dummy lines are placed around the capacitors to define their neighborhood distance. A design question is which orientation to lay out the dummy-lines, i.e. whether the lines are horizontal or vertical.

Since the lines within the test structures are actually simulating interconnect lines, the solution should be based on how interconnect lines are laid out in a real-life chip. An aspect to consider is that the existing test structures simulate global interconnect lines, and not local interconnect lines which typically lie on top of device regions.⁵ Another aspect which is important is that global interconnect on each metal layer is usually in one orientation, with alternating orientations for each consecutive metal layer. This is so that routing is organized and feasible to all locations in the die.

Therefore, the solution is to lay out the dummy-lines in the same orientation as the lines in the capacitor test structure. Considering that the test structures have two types of orientations, the dummy-lines need two orientations too. Although it is not like a real-life chip to have two orientations for lines on the same metal layer, the CMP polishing of the statistical metrology test chip will approximate that of a real-life chip as long as each uni-orientation section is large enough (larger than CMP planarization length). Undoubtedly, there will be some effects at the edges where the two line orientations meet, but these effects can be minimal if the capacitors are relatively far from these edges.

2.2 Probe Layout Design

Probe layouts are layouts of metal pads which are connected to the test structures for the probe-card pins to contact. These probe layouts can connect to several capacitors and

5. At the present time, statistical metrology capacitor test structures cannot be placed on top of non-planar device regions. This is because the non-planarity and variety of the device features brings about additional complications when modeling the ILD thickness. Therefore, the capacitor test structures only simulate global interconnect.

resistors or to as few as one device. It is however necessary that all probe layouts for the die can be probed by one probe-card. One probe-card design that can connect to many types of probe layouts is the T probe-card layout.

2.2.1 T Probe-card Layout

As shown in Figure 2.4, the T probe-card layout looks like an asymmetric “t”. It contains sixteen pins in total which can be connected to multiple and varied devices in different ways.

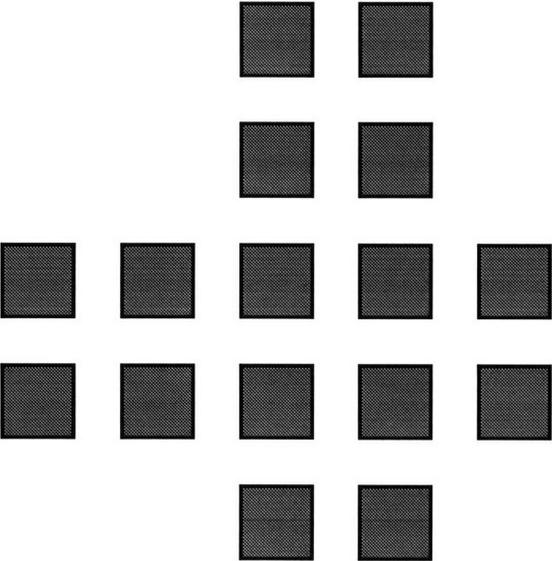


Figure 2.4: T probe-card layout.

2.2.2 Advantages of the T Probe-card Layout

The T probe-card layout was conceptualized when the need arose for a probe-card configuration that could probe instances and their copies that were rotated a quarter-way around. This is because layout of the test chip is considerably easier if instances with a particular orientation could just be copied and rotated a quarter-way around (Figure 2.5).

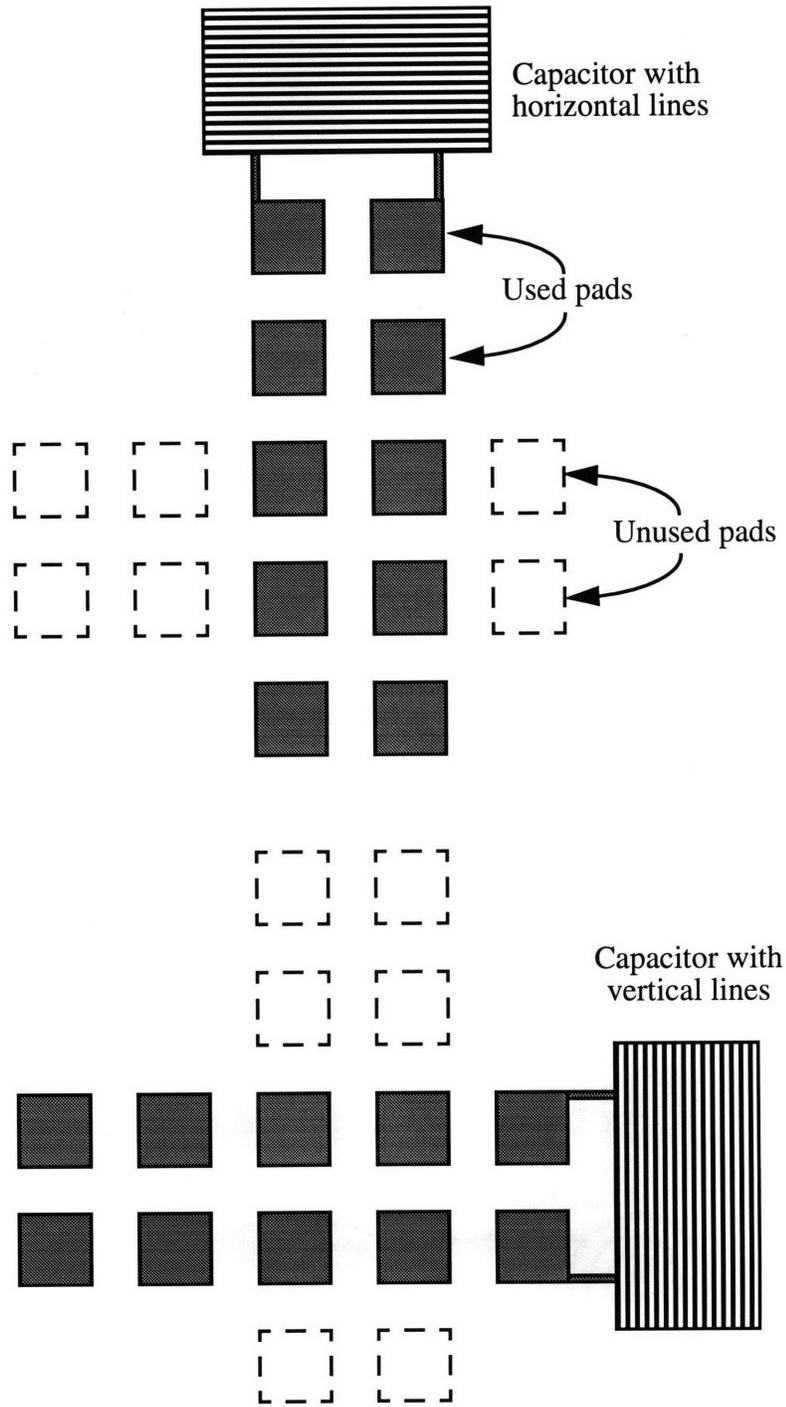


Figure 2.5: T probe-card use for different capacitor orientations.

In addition, the T probe-card layout can be efficiently used to probe many devices. An example of the efficiency of the T probe-card is shown in Figure 2.6. In that layout, four

capacitors, a Kelvin structure, a van der Pauw structure, and a pad capacitor are connected to the sixteen pads. As described in subsection 3.3.2, the pad capacitor is no longer necessary when a certain electrical characterization method is used.

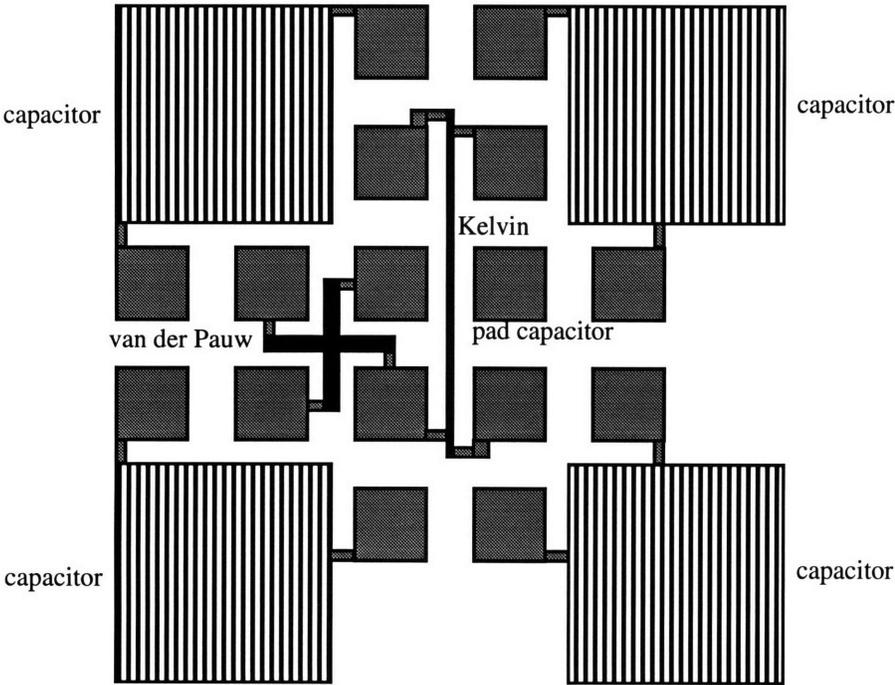


Figure 2.6: T probe-card efficiency in measuring devices.

Finally, as long as there is a passivation oxide on top of the top metal, the T probe-card layout can be easily used to probe a few structures which only need a few pins (Figure 2.7). The passivation oxide will prevent the unused pins from damaging the underlying metal.

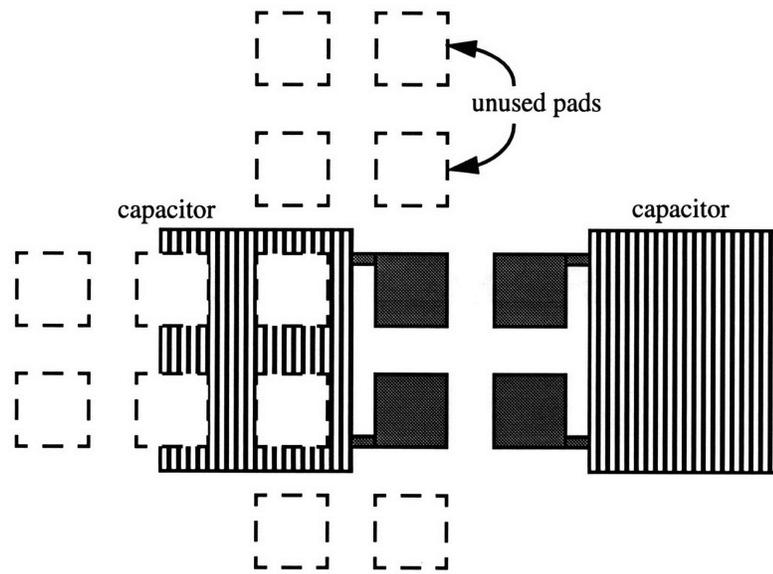


Figure 2.7: T probe-card using only a few pins.

2.2.3 Making the Probe Layout an Instance of the Die

It is good practice to lay out the test chip in a hierarchical manner using instances. Instances are small layouts that are parts of a larger layout. They can be individually edited and they automatically update the higher levels in the hierarchy. For example, capacitors and resistors can be instances within a probe layout. Instances can be contained within instances too, such as capacitor instances within probe layout instances, and probe layout instances within a die layout. In addition to the automatic updating after editing, another reason to use instances is that similar layouts can use the same instance and thus save additional work.

While laying out the test chip, probe layouts should definitely be designed as instances. This is because much work can be saved by exploiting the similarities between probe layouts. This is also the case for capacitor and resistor test structures which should be designed as instances.

2.2.4 Probe Layout Considerations

As shown in the previous subsection, there are many probe layout configurations that can be probed by the T probe-card design. All of these probe layouts have similar design considerations, which will be discussed in this subsection.

2.2.4 a) Pad Size and Spacing

Pads connect the devices to the probe-card pins. Therefore, the pads have to be at least $100\ \mu\text{m} \times 100\ \mu\text{m}$ large. For successful automatic probing, it is recommended that the pads are larger than $120\ \mu\text{m} \times 120\ \mu\text{m}$.

Spacing between the pads is also important. If the spacing is too small, then leakage might occur between pads. Capacitance measurements may also be affected by the increase in same-layer capacitance between pads. The pad spacing should be a minimum of about sixty microns.

2.2.4 b) Capacitors and Resistors in Close Proximity

Capacitors and their corresponding resistors must be in close proximity since the resistors are approximating the capacitor's critical dimension. To achieve close proximity, they must be placed in the same probe layout. Assuming a probe layout area of $1\ \text{mm} \times 1\ \text{mm}$ or less, one pair of Kelvins and van der Pauws should suffice per probe layout, especially if interpolation of critical dimensions is performed (described in Section 2.6).

It is best to have Kelvins and van der Pauws closer to each other than Kelvins and capacitors, or van der Pauws and capacitors. This is because calculation of the critical dimension assumes that the Kelvin and van der Pauw are at the same location.

2.2.4 c) Pad Sharing of the Devices

Pads can be shared intelligently for Kelvins and van der Pauws. However, a conservative design should avoid any pad sharing between capacitors and Kelvins or van der

Pauws. Sharing pads would effectively make the capacitor a larger structure which might have a different capacitance. Although the majority of the capacitance measured is between the parallel plates (assuming the substrate is grounded), the fringing capacitance might in certain cases be large enough to cause errors in the measurement. On the practical side, if the resistor and its connecting pads are not very close to the capacitor or its unconnected pad, then the capacitance error is negligible.

Kelvins and van der Pauws can share pads as long as the pad sharing does not create an extra current path in the devices. Figure 2.8 illustrates how sharing two pads between a Kelvin and van der Pauw would create an extra current path, i_2 . This extra current path decreases the current that flows in the real resistor path, hence the resistance calculation is erroneous.

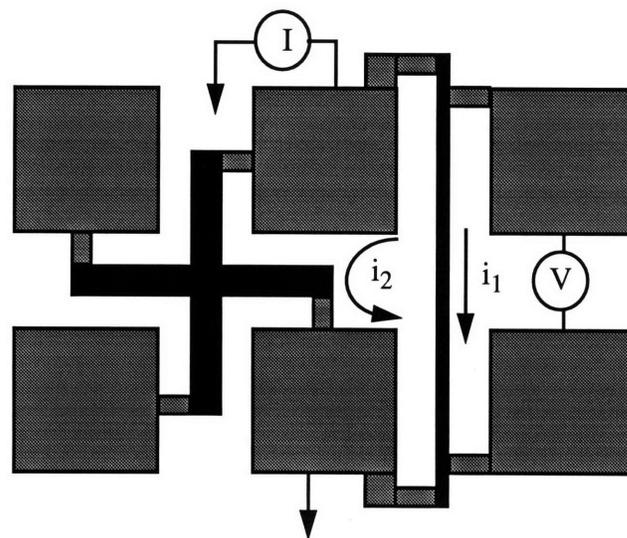


Figure 2.8: Extra current path along i_2 when measuring Kelvin resistor.

2.2.4 d) Dummy-lines Within Each Probe Layout

Lower metal layers in real-life chips are typically densely packed. This is because much routing is needed at the lower levels. Furthermore, upper-level planarity is improved when the lower levels are well covered with metal lines.⁶

In order to emulate a real-life chip, the test chip M1 layer should be mostly covered with lines, except for the areas which are defined as neighborhood distances. Thus, the probe layout area must also contain M1 dummy-lines. To make each instance of a probe layout self-containing, the dummy-lines should be designed into each probe-layout instance, instead of being added at the die level. Using this abstraction, the self-containing feature of each instance makes designing global dummy-lines much easier.

To have dummy-lines within a probe-layout, the M2 pads must lie on top of M1 dummy lines in the probe layouts. These dummy-lines should have the same pitch and orientation as the capacitor and the Kelvin structure within that probe layout. This ensures that the Kelvin resistor sees the same environment as the capacitor fingers. The dummy-lines should also come relatively close to the resistors as allowed by the process design rules. A recommended distance from resistor to dummy-line is about 1.5 to two times the minimum M1 spacing. An example of this is the van der Pauw resistor in Figure 2.9.

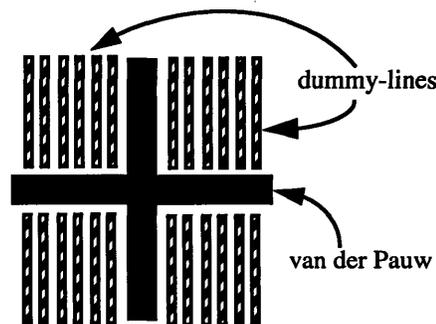


Figure 2.9: Dummy-lines surrounding a van der Pauw resistor.

2.3 Die Layout Design

There are many ways to design a die layout. However, not all the ways maximize the total number of structures, systematically probe factors such as neighborhood distance, allow

6. Some industry processes even insert dummy-lines into layers which have too little metal coverage.

easy automatic probing, simplify cross-sectional SEMs, allow randomization, and allocate space for replicates across the die. One die layout that tries to address all these issues is the L die layout.

2.3.1 L Die Design

The L die layout was first conceived as an efficient and systematic layout to probe neighborhood distances. As seen in Figure 2.10, the crux of the design is to line up probe-layers that each have one similarly orientated capacitor with one neighborhood distance. Each series of probe-layers can be placed parallel to each other so that each series characterizes different neighborhood distances. Of course, the other orientation for the capacitor warrants that the probe-layout line be perpendicular to the previous orientation's line, hence the shape L.

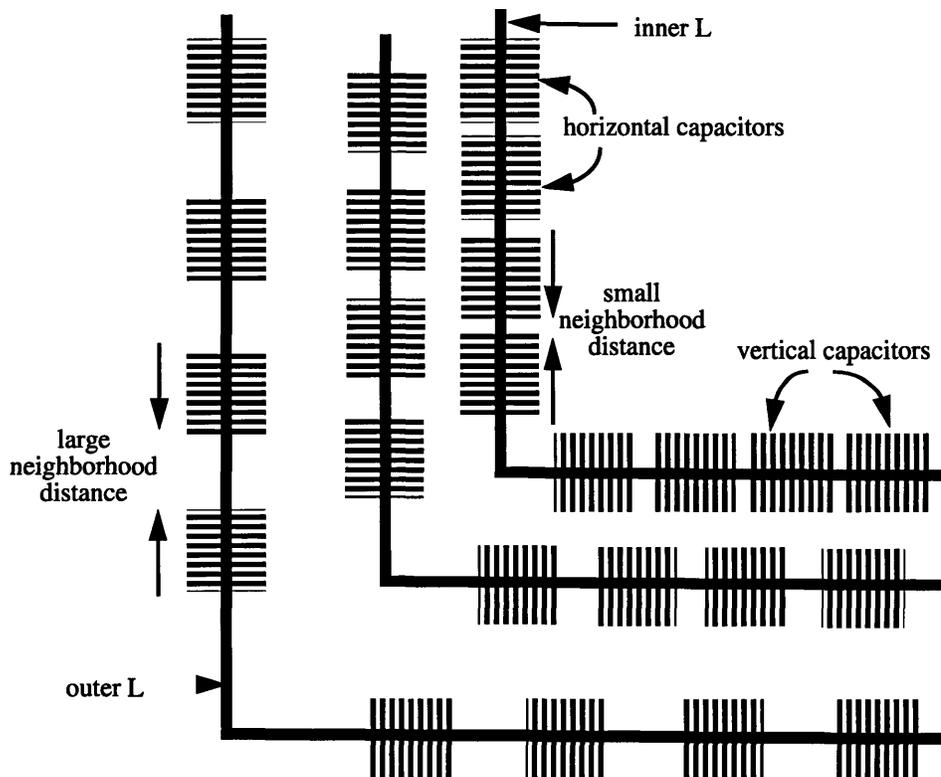


Figure 2.10: L die layout

Since neighborhood distance is defined all around the capacitor, the larger the neighborhood distance, the larger the L. As a consequence, it is logical to place the L with the smallest neighborhood distance at the center of the die, and L's with larger neighborhood distances closer to the die edge respectively.

A justified concern is that systematically placing larger neighborhood distances closer to the die-edge might confuse neighborhood distance effects with die location effects. The L design tries to prevent this by ensuring that the L closest to the die-edge has as much dummy-line area as possible to the die-edge, making the total distance of L capacitor to die edge at least one millimeter, or preferably the CMP planarization length. Since the whole die is mainly covered with dummy-lines, the CMP polishing pad should not distinguish as much of the die-location effect, as it should the neighborhood distance effect. Even if there is some die-location effect, it can be captured by the replicated structures which are spread throughout the die.

2.3.2 Advantages of the L Die Layout

The L layout is more efficient and systematic for characterizing neighborhood distance than probe-layouts that have multiple capacitors with different neighborhood distances and orientations [5, 6]. This is because having different neighborhood distances, orientations and capacitor sizes on the same probe layout creates wasted space around the probe-layout.

Additionally, having the probe-layouts laid out in a line allows easy automatic probing. While the prober must step to many more locations within the die, modern automatic probers step from location to location very quickly and stepping is not a measurement time limiting factor.

Laying out capacitors in a series also allows cross-sectional SEMs to be easily performed to measure the ILD thickness. A SEM sample from an L die design can have many cross-sections of the capacitors in series, which simplifies the measurement.

Layout randomization is important to ensure that systematic layout locations do not introduce additional errors when characterizing layout factors. On the other hand, pure randomization is less ideal for interpolating critical dimensions at capacitor locations using similarly pitched Kelvins. An extreme example is when pure randomization places all but one of the Kelvin structures of type A in just one section of the die, and the last type A Kelvin in a far-edge of the die. Interpolation of the critical dimension of the capacitor at the far-edge will not be as good as when the Kelvins are evenly spaced out.

The L die layout uses partial randomization which enables good interpolation as well as minimizes systematic location error. Partial randomization exploits the fact that there are only four unique pitches for Kelvins in a two level factorial experiment (finger length and number of fingers are not varied for resistors). Therefore, the L die-layout randomizes *groups* of the four unique Kelvins, while keeping each group similar.

Lastly, as will be described in section 2.4, the empty quad in the top right hand corner of the L die-layout has ample space to place other test structures which investigate next-generation test structure / probe design. If the die size is 18 mm x 18 mm, then the empty quad is approximately 9 mm x 9 mm, a considerably large area.

2.3.3 Other Die Layout Considerations

Laying out a large die is not trivial, and requires thoughtful design. Firstly, an appropriate die-layout (such as the L design) should be chosen or designed to meet the needs of the experiment. There are however, other layout considerations which should be heeded while laying out the die.

2.3.3 a) Die Size

When the die is larger, more test structures can be placed on it, making the experiment better. However, when the die size is increased, the number of die per wafer is decreased. Signal processing of the data requires that there be a minimum of 36 die per wafer to prevent noise from interfering with the analysis. Furthermore, dies are not printed at the edge of the wafer because there is a forbidden region about fifty millimeter from the wafer edge. Therefore, an 18 mm x 18 mm die will yield about 37 full die per six inch wafer. Another limitation for the die size is the maximum stepper field, which is typically about 20 mm x 20 mm at the current technology. It is not advised to approach the maximum stepper field because of imperfect exposure at the fringes of the field.

2.3.3 b) Device Names Laid-out Next to Devices

Although it may appear to be a trivial issue, placing names next to devices becomes critical when one needs to do cross-sectional SEMs. If one has to measure ILD thicknesses for sixteen capacitors in one SEM sample, having names next to structures helps the measurements go more smoothly. It is best to use a text library in the layout tool to lay-out the devices names, otherwise, one has to construct one's own text library. Since there are dummy-lines on the M1 layer throughout the chip, text should be placed on the M2 layer.

2.3.3 c) Spread-out Location of Centerpoints and Blanket Capacitors

Replications of centerpoints and blanket capacitors are mainly used for characterizing location effects. Hence, centerpoints and blanket capacitors should have spread-out locations throughout the die. This cannot take priority though, otherwise die-layout design (such as the L design) may not be possible.

This author recommends that a die-design be used as a frame, and centerpoints and blanket capacitors be squeezed into areas which are left empty by the frame. Typically, the frame or a slightly adjusted frame can yield ample space throughout the die to have spread-out centerpoints and blanket capacitors.

2.4 Next Generation and Verification Test Structures

In the empty upper-right quad of the test chip, there is enough area to locate several types of test structures; some for research for a next-generation test chip, and some for verification purposes. Furthermore, some parts of the L section have empty area which can contain a few of these structures. This section explains several kinds of test structures that can be placed in these available locations.

2.4.1 Block Test Structures

Block test structures are next generation test structures currently investigated for future test chips. They are essentially blocks of nine, sixteen, or more similar capacitors placed at minimum spacing from each other. These blocks have their own larger than minimum neighborhood distance which is defined from the block edge to surrounding structures. All the capacitors have approximately the same area even if they have different pitches. An illustration of the block capacitor test structure versus the current L capacitor test structure can be seen in Figure 2.11.

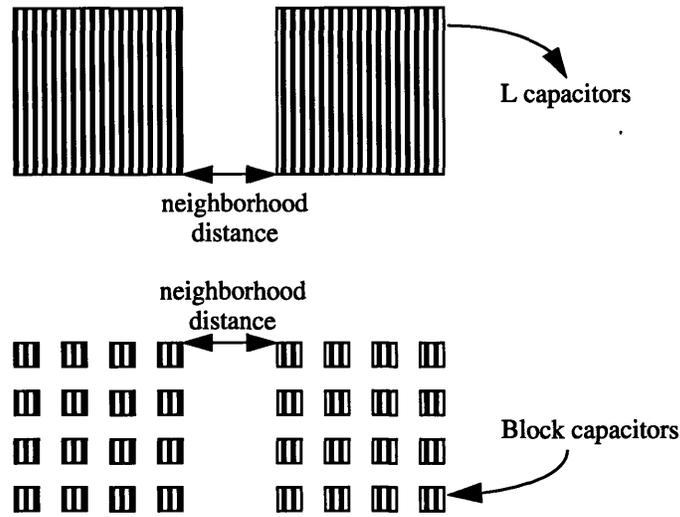


Figure 2.11: Block capacitor test structures.

The rationale for block test structures is that the current capacitors yield an average ILD thickness for the whole capacitor area. Unfortunately, this is not realistic because a block of interconnect lines is commonly known to yield “rounding” at the edges, and hence a smaller ILD thickness. Current capacitor structures will not be able to measure that difference in ILD thickness. Using a block of x capacitors can increase the resolution of the ILD thickness across the whole block area x times.

Defining the neighborhood distance as the distance from the block edge to surrounding structures is also beneficial because it is more realistic. Real-life metal layers typically have regions with minimum spaced lines, and then a large gap (neighborhood distance) before another region with minimum spaced lines. Those layouts are similar to that of the Block capacitor test structure.

2.4.2 Uni-edge Test Structure

A less drastic change from the current test structure is the Uni-edge capacitor. It is a next generation test structure which is different from the current test structure by the way neighborhood distance is defined. Current capacitors define neighborhood distance as the

distance from the capacitor to surrounding structures for all four edges of the capacitor. However, following the argument for block capacitors, neighborhood distance is probably best defined along one edge since it is common to have large spacings separating blocks of interconnect lines. The Uni-edge capacitor therefore has neighborhood distance defined along the outer edge of the capacitor (furthest from the probe layout) and thus has four geometric orientations (facing up, down, left, and right). A row of four Uni-edge capacitors with orientation facing upwards can be seen in Figure 2.12.

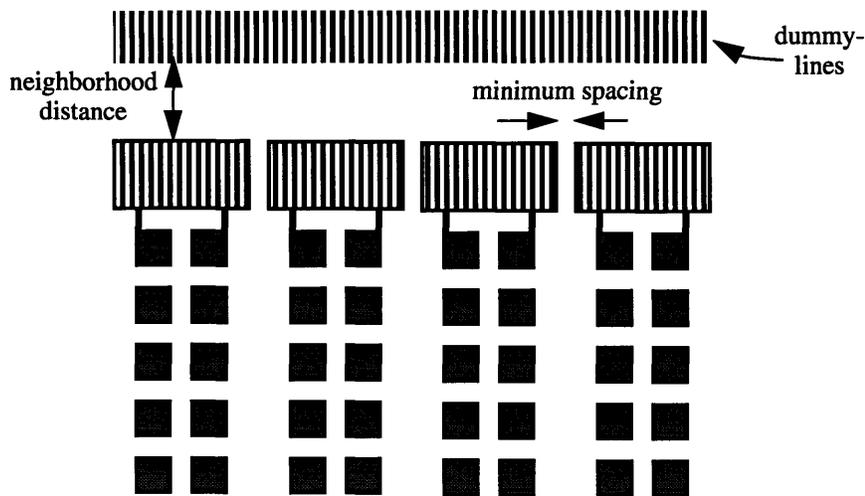


Figure 2.12: Uni-edge test structures.

It is also interesting to analyze the data from Uni-edge test structures because they are in essence, a hybrid of the L and Block test structures. Analysis of these structures should give additional insight to why L and Block test structures have differences in data.

2.4.3 Area Test Structures

Differently sized capacitors (with similar factors) may show an ILD thickness dependence on capacitor area, especially if the capacitors are not in a dummy-line environment. In a dummy-line environment that is similarly pitched as the capacitors, it is likely that the

CMP polishing pad will not know the difference between a small and a large capacitor. Nevertheless, there is no data to verify this theory, hence the need for Area test structures.

Area test structures can be designed as a row of three capacitors - the middle capacitor with a large area, and the side capacitors with a small area (Figure 2.13). The size of the large area capacitor should be comparable to or larger than the CMP planarization length, while the size of the small area capacitor should be considerably less. Two pairs of Kelvin and van der Pauw structures can be placed with the two small capacitors, so that critical dimension can be interpolated for the center capacitor. Simple statistical t-tests can distinguish if ILD thickness has a dependence on capacitor area in a similarly pitched dummy-line environment.

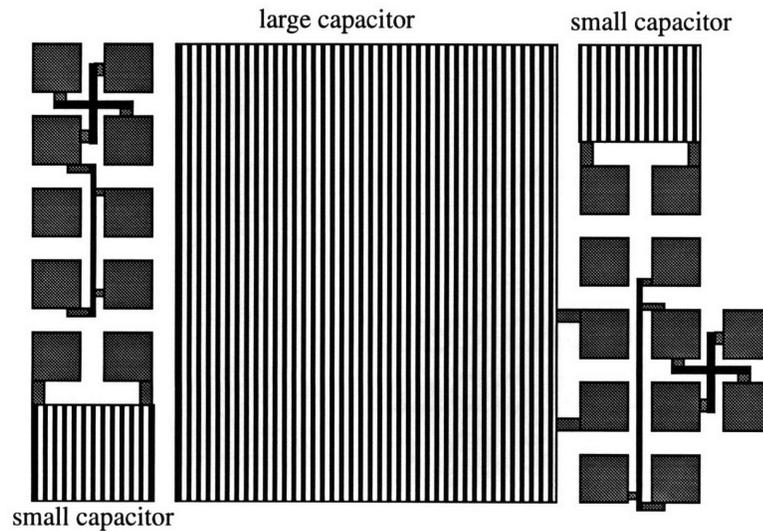


Figure 2.13: Area test structures.

Area test structures can also be used in another way. Since area structures are inherently large, they do not have the area constraints when deciding factor levels like regular capacitors do. In other words, one can set the finger width to be twenty microns and still

not violate area constraints. This is useful for methodology verification purposes using external metrology schemes as described next.

Optical ILD thickness measurements can be used to verify and calibrate the statistical metrology methodology. However, optical measurements are limited by the minimum spot size of the optical beam which is typically around $4\ \mu\text{m} \times 4\ \mu\text{m}$. If the spot size is larger than or about the same dimension as the interconnect width, then the ILD thickness calculation yields an incorrect larger value. Due to stepping, offset, and dispersion errors, it is not recommended to do such measurements on interconnect lines with widths less than three to five times the beam spot size.

2.5 Process Flow and Characterization

The basic process flow to fabricate the test structures should be similar to the flow for the process that is being investigated. There is little use generating models for process variation that are not representative of real processes. Therefore, all of the test chip metal and oxide thicknesses should be similar to the thicknesses in the process of interest.

Process characterization such as SEM critical dimension measurements, optical oxide thickness measurements, and profilometric measurements, are useful for verification and simulation purposes. External verification is important to validate and calibrate statistical metrology as the method of choice for modeling process variation. Simulations also need structural data such as metal and field-oxide thicknesses which can best be determined by process characterization.

2.5.1 Process Flow

The basic process flow begins with a deposited film of field oxide (typically TEOS). Although not critical, the field oxide thickness should be similar to the sum of the field oxide thickness and ILD1 thickness in the process of interest.

An M1 layer is then deposited, patterned, and etched using the M1 test reticle. Next, an ILD oxide is deposited on top of the metal and CMP planarized. In most processes, deposition of ILD oxide over narrowly spaced M1 lines may cause creation of air-filled “key-holes” because of imperfect filling of the narrow spaces (Figure 2.14). Some processes CMP planarize until the key-holes are exposed, then do a redeposition of ILD oxide to regain the lost oxide thickness. Therefore, processes may or may not have keyholes depending on whether the gap fill processing is done. In addition, the key-hole size also depends on the process and minimum spacing used. It might be small enough to be neglected in simulations or it might not, therefore care has to be taken to understand the process being used.

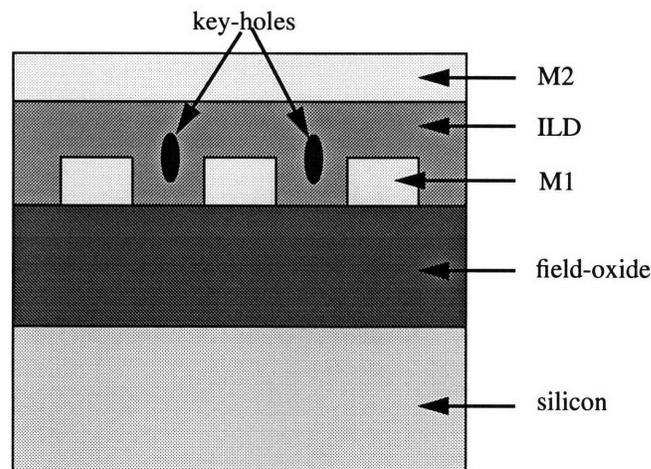


Figure 2.14: Key-holes between narrowly spaced M1 lines.

The next step is the filling, patterning, and etching of the vias. This is followed by the deposition, patterning, and etching of M2. A passivation oxide is then deposited, patterned, and etched. The passivation is an oxide cover which has gaps where M2 pads are to allow contact to the probe-card pins. It is important so that the probe-card pins will not accidentally contact parts of M2 which are not to be contacted.

2.5.2 Process Characterization

Process characterization is useful for verification and simulation purposes. The following is a list of process characterizations that can be used to enhance and validate statistical metrology.

2.5.2 a) SEM Critical Dimension Measurements

This measurement is useful for validating the critical dimension values calculated by the Kelvins and van der Pauws. The SEM also has the advantage of being able to measure the critical dimension of the lines in the capacitor. Therefore, since Kelvin critical dimensions are used to interpolate the critical dimension for the capacitor, SEM measurements are excellent tools for validating the interpolation process.

2.5.2 b) Optical Oxide Thickness Measurements

Optical measurements can be performed using a machine similar to the Prometrix FT750. Such measurements are useful for gathering wafer-scale and lot-scale oxide thickness data, but are still not practical to measure many oxide thicknesses at the die-level.

The variation of the deposited field-oxide thickness within a wafer is typically small (less than three percent) for industrial processes. However, the variation across a lot may be larger (less than ten percent). It is acceptable for simulation purposes to use the mean of the field-oxide thicknesses because a ten percent variation in field-oxide thickness probably translates to less than a percent error in the simulations. However, performing these measurements are important as sanity checks.

If enough field oxide thicknesses per wafer are collected, the data can also be used to correlate with the field-oxide blanket test structures. If the blanket capacitor data correlates well with the optical data, the electrical data can then be utilized with confidence for process control purposes.

As discussed in the Area test structure section, optical oxide thickness measurements can also be used to measure ILD thicknesses on top of capacitors with wide M1 lines. The data can be used to validate statistical metrology as a reliable metrology tool.

2.5.2 c) Profilometric Measurements

Profilometric measurements are useful for determining the step height thickness of metal lines and are typically performed using systems such as the Tencor P2. This measurement, however, has a low throughput and should probably be used for approximately five points per wafer, for only a few wafers.

2.6 ILD Thickness Extraction

The process of extracting ILD thickness consists of capacitance simulations, electrical measurements, and mathematical interpolations. The electrical measurements include capacitance and resistance measurements. The interpolations are used for critical dimension estimation, as well as ILD thickness determination. Figure 2.15 shows an example of how these simulations, electrical measurements, and interpolations combine to yield an extracted ILD thickness.

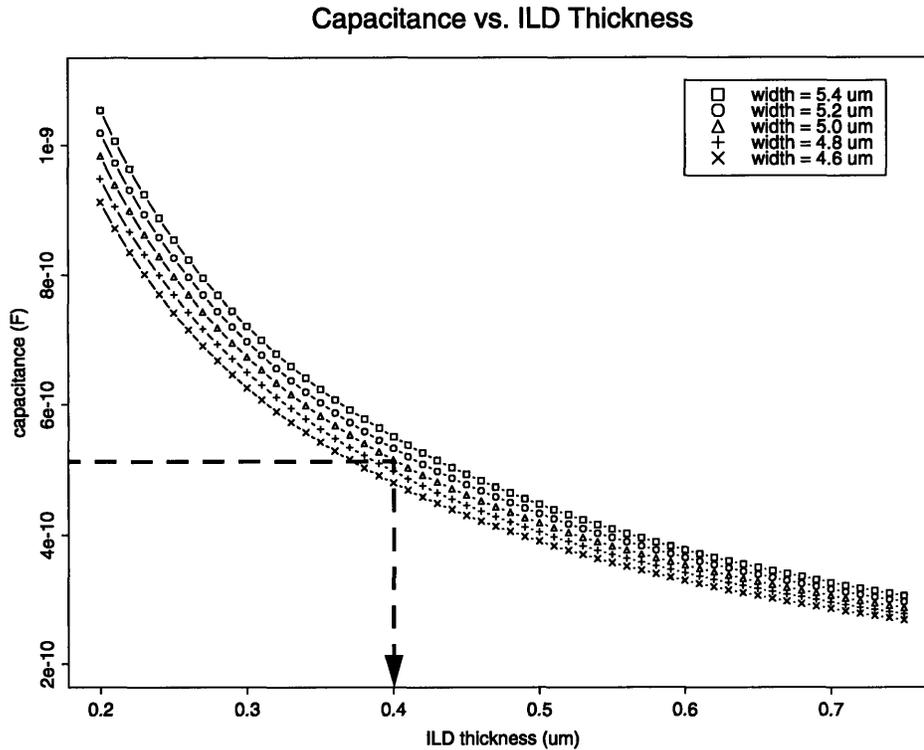


Figure 2.15: ILD thickness extraction.

2.6.1 Capacitance Simulations

Capacitance simulations can be run on programs such as Raphael, METAL, or FAST-CAP. Two-dimensional capacitance simulations are performed on structures such as the one shown in Figure 2.16. The capacitance simulations are run in batch mode, whereby many simulations are run for different ILD thicknesses and critical dimensions. A batch program needs to be written which can automatically vary the ILD thickness and critical dimensions in the input simulation file before simulating. The step size when varying ILD thickness should typically be 0.01 micron for about 0.2 micron above and below the targeted thickness. Thicknesses outside this range can have larger steps. Likewise, critical dimensions should vary at small steps like 0.02 micron for about 0.2 micron above and below the targeted critical dimension, especially for minimum critical dimensions. For

field-oxide blanket capacitors (discussed consequently), the field-oxide thickness can also be varied like for the ILD thickness.

It is wise to simulate extreme values, even if the step size near the extreme is large. This is so that the interpolation program will not crash if there are some extreme data points and thus require that simulations be rerun. Even if extrapolation outside the loci of data points is allowed by the interpolation program, this is not encouraged because such extrapolation is prone to errors. Note that the pitch of a particular structure is fixed. Therefore, if simulating for a particular critical dimension, the line spacing is equal to the critical dimension subtracted from the pitch.

Some programs such as Raphael can simulate for charge on conductors as well. Since it is a faster simulation, it is recommended over generating a complete capacitance matrix. The capacitance can easily be calculated from the charge by dividing the charge by the applied potential.

The two-dimensional simulation structure must correctly represent the real-life structure. To simulate the fingered capacitor, two structures must be simulated: the fingers, and the line connecting the fingers. The total capacitance of these two structures can then be combined and correlated with the measured capacitance of the capacitor.

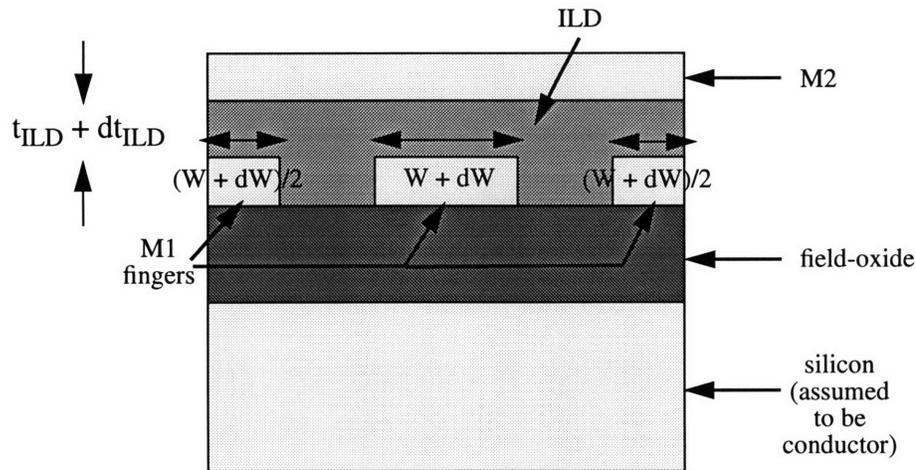


Figure 2.16: Fingered simulation structure.

2.6.1 a) Fingered Simulation Structure

Figure 2.16 shows the fingered simulation structure. It does not simulate all the fingers in the capacitor, rather it exploits the replication of the fingers by only simulating a center finger and two adjacent half-fingers. The two adjacent half-fingers account for the fringing fields in the capacitor. The capacitance of the fingered portion of the capacitor is therefore the capacitance from M2 to the center M1 finger, multiplied by the number of fingers.

2.6.1 b) Connecting Line Simulation Structure

The line connecting the fingers is simulated as shown in Figure 2.17. Note that M2 is overlapping M1 by a few tenths of a micron as discussed in section 2.1.5. When simulating the edge of a structure, include a dielectric region next to the device to allow the simulator to account for fringing fields at the edge.

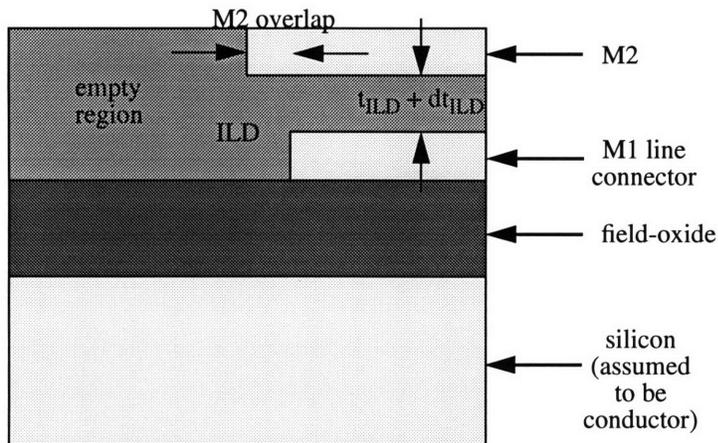


Figure 2.17: Simulation structure for line connecting the fingers.

2.6.1 c) Blanket Capacitor Simulation Structure.

There are two types of blanket capacitors, i.e. the ILD blanket capacitor, and the field-oxide blanket capacitor. These two capacitors should be simulated as shown in Figures 2.18 and 2.19 respectively. Note again, that additional space should be left empty at the edges to account for fringing fields, and that the ILD blanket capacitor has an M1-M2 overlap.

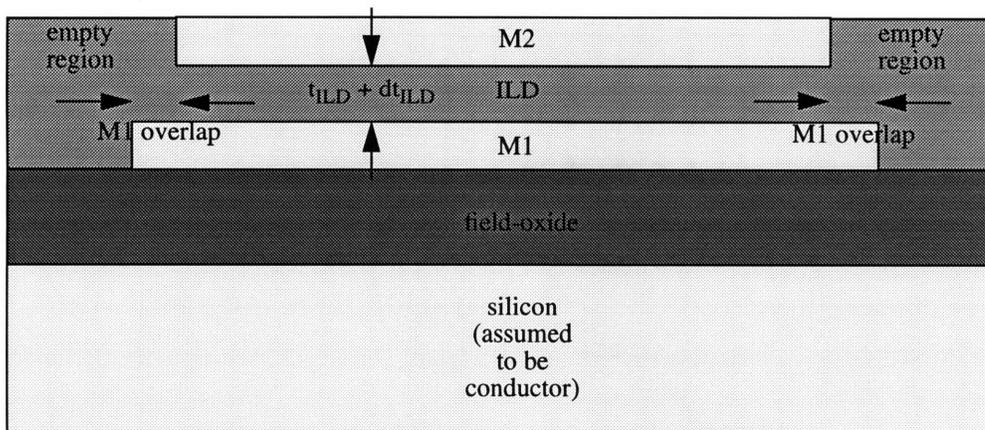


Figure 2.18: ILD blanket capacitor simulation structure.

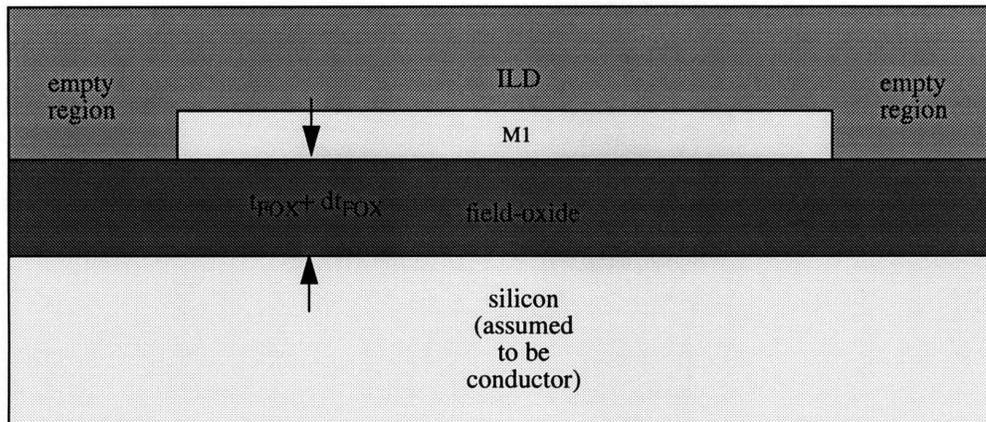


Figure 2.19: Field-oxide blanket capacitor simulation structure.

2.6.1 d) Simulation Bias Values

Since the simulated capacitors are metal-metal capacitors, the capacitance matrix generated by the simulation is not dependent on the bias values. The bias values only affect the amount of charge on each conductor in the simulations. Likewise, the measured capacitance should also not depend on the bias values because of the metal-metal capacitors. For all the capacitors except the field-oxide blanket capacitors, the capacitance meter High and Low probes are connected to M2 and M1 respectively, thus the simulated capacitance of interest is the M2-M1 capacitance, and not the M2-substrate or the M1-substrate capacitances.

The simulations are performed using one volt on the top plate and zero volts on the bottom plate and substrate (unless the bottom plate is the substrate). This is a matter of convenience so that M2-M1 capacitance is exactly the negative charge on M1. When the top plate is M1 and the bottom plate is the substrate, the M1-substrate capacitance is exactly the negative charge on the substrate, and also the positive charge on M1. Using this convention, the fingered and connecting line structures, and the ILD blanket capacitor

structures are simulated by connecting M2 to a one volt potential, while M1 and substrate are connected to ground. For the field-oxide blanket capacitor, a one volt potential is applied to M1, while the substrate (which is the bottom plate) is grounded.

2.6.1 e) Simulation Output

After the simulations are performed with varying ILD thicknesses and pitches, a plot for capacitance versus ILD thickness for various pitches can be generated as previously shown in Figure 2.15. This simulation output will be used together with capacitance and critical dimension measurements to yield the estimated ILD thickness.

2.6.2 Electrical Characterization

Electrical characterization of a statistical metrology test-chip is performed with an automatic prober controlled by a parametric analyzer system. An example is the Electro-Glass 2001 automatic prober which is controlled by a Keithley S400UX parametric test system. The parametric test system must be able to perform current-voltage (i.e. resistance) measurements, as well as high-frequency capacitance measurements. A probe-card must be fabricated according to the dimensions of the chip's probe-layout.

2.6.2 a) Resistance Measurements

Resistance measurements are carried out on both Kelvin and van der Pauw structures. They both use the principal of forcing current and measuring voltage. Figure 2.20 shows that the outer Kelvin probes are forced with current, while the inner probes are measured with a voltmeter. In Figure 2.21, the van der Pauw resistor is forced with current by two adjacent probes, and voltage is measured by the remaining two probes. Since the van der Pauw is a symmetric structure, the measurement is usually made a second time with the

probes rotated ninety degrees, and the results averaged. Sheet resistance for the van der Pauw can be calculated from the following formula:

$$R_{sheet} = \frac{\pi}{\ln 2} \left(\frac{R_{vdp1} + R_{vdp2}}{2} \right) \quad (2.4)$$

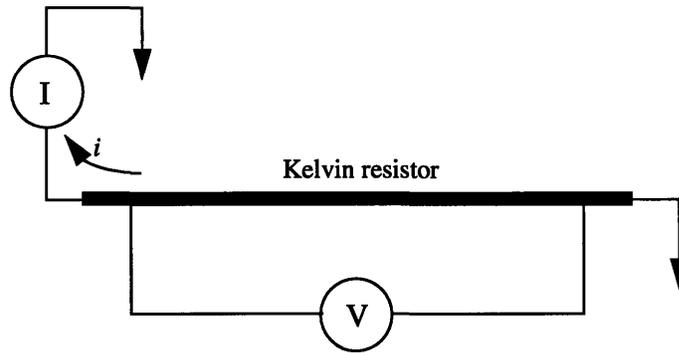


Figure 2.20: Measuring resistance of a Kelvin structure.

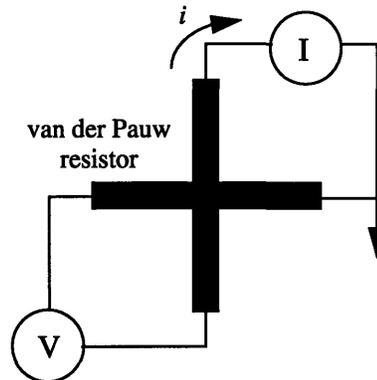


Figure 2.21: Measuring resistance of a van der Pauw structure.

2.6.2 b) Capacitance Measurements

Capacitance measurements can be performed using a two-terminal measurement method. The High terminal transmits a high frequency signal (100 kHz - 1 MHz) to the Device Under Test (DUT). The Low terminal is connected to an ammeter, which measures the change in current due to the high frequency signal. The meter integrates with respect to time, the change in current due to the change in voltage, to yield the capacitance.

It is standard for the upper-level metal to be connected to the capacitance High terminal, whereas the lower-level metal to be connected to the Low terminal. The substrate can be either connected to the Low terminal, electrically grounded, connected to guard or left floating. Since the capacitance of interest is the M2-M1 capacitance, measuring the substrate capacitances in addition to the M2-M1 capacitance only decreases the resolution of the M2-M1 capacitance values. Therefore, connecting the Low terminal to the substrate in addition to M1, is discouraged.

Floating the substrate or connecting it to the guard does ensure that the substrate capacitance is not accidentally measured. However, it does expose the measurement to more noise. On the other hand, grounding the substrate is less susceptible to noise, but there might be some inductive coupling between the ground and the Low terminal ground. For less than a perfect inductor, some high frequency signals from the substrate will leak to the Low terminal, which might affect the capacitance measurement. In practice, the difference between floating, guarding or grounding the substrate is small (about one percent), so all three methods are acceptable. From measurements at LSI Logic, grounding the substrate usually gives a slightly lower value than floating or guarding the substrate.

When measuring the field-oxide blanket capacitors, attaching the High terminal to M1 and the Low terminal to the substrate sometimes may not work on systems like the Keithley S400UX. Flipping the connections might make the measurement work.

One must ensure that the capacitance calculations account for the parasitic capacitance of the probe-card and wiring. This can be achieved by measuring the parasitic capacitance before the probe-tips connect to the pads. This parasitic capacitance can be subtracted from the measured capacitance to yield the correct device capacitance.

Bias between the High and Low terminals does not affect the measurement because the capacitors are metal - metal capacitors. A simple bias of one volt to coincide with the simulation values is suggested.

2.6.3 Interpolation of Critical Dimensions

In order to extract the ILD thickness from the simulation output in Figure 2.15, the measured capacitance and the critical dimension at the location of the desired ILD thickness must be known. The measured capacitance is obtained directly from the capacitor and is therefore at the location of the desired ILD thickness. However, the critical dimension is obtained from resistors which are relatively close-by, but nevertheless at different locations from the location of the ILD thickness of interest.

The critical dimension at the required location can be interpolated from similar nearby resistors within the same die. The critical dimensions are calculated from the resistances of both Kelvins and van der Pauws. For the probe layout in the L design, the Kelvins and van der Pauws are right next to each other. Thus, the X-Y coordinates for the critical dimensions can be approximated as the average of the X-Y coordinates for the Kelvins and van der Pauws.

The critical dimensions, their X-Y coordinates, and their die numbers, as well as the capacitor X-Y coordinates and die numbers, can be fed into a statistical analysis program such as SPLUS. Given this data, cubic interpolation [7] can be performed by the program to estimate the critical dimensions at the capacitor locations. It is important to make sure the program interpolates the critical dimensions for each capacitor using only the critical dimension locations within the capacitor's die. This is because critical dimension is typically affected by stepper variation, which varies die by die. Interpolating using other die's critical dimensions may be incorrect, especially for capacitors at the die edges. If the interpolation process takes too long, the program can use just critical dimensions from the

same die as the capacitor, but which are within a few millimeter radius for the interpolation.

2.6.4 Interpolation of ILD Thickness

Given the interpolated critical dimensions and measured capacitances, as well as the simulation output (capacitances for different ILD thicknesses and critical dimensions), SPLUS can again be used to interpolate the ILD thickness. Just as with the critical dimension interpolation, the ILD thickness can be cubic interpolated for the critical dimensions and measured capacitances using the simulation output. In this case, however, the interpolation is not limited to the data within each die. As before, if the interpolation takes too long, the data from which the interpolation is performed can be sized down according to the proximity of the data points.

2.7 Data Organization

Statistical metrology obviously generates a large amount of data. If not organized properly, the abundance of data will create a multitude of problems such as loss and mix-up of data, and difficulty in performing statistical analysis and signal processing. This section provides a few hints for preventing such havoc from happening.

2.7.1 Data Naming

Each measurement data point must have a unique identifier. For a particular experimental wafer lot, three levels of naming are typically needed. The highest in the hierarchy is wafer naming. It is recommended that wafers are named with numbers, since there is no distinguishing characteristic about each wafer. The second level is die naming. Again, there is no distinguishing characteristic about each die, therefore a numbering method is best. The order in numbering is most systematic when it follows the path the dies are measured, which is most efficient in a snake-like pattern.

The third and most complex stage of the hierarchy is device naming.⁷ Devices have their individual characteristics. For example, capacitors are different from resistors; regular L capacitors are different from Uni-edge capacitors, Block capacitors or Area capacitors; and L capacitors with neighborhood distance “A” are different from L capacitors with neighborhood distance “B” etc. These devices can be named differently based on what kind of devices they are. It is recommended that each kind of device has a similar prefix, for instance L capacitors have the prefix “C_”, Uni-edge capacitors have the prefix “D_”, Block capacitors have the prefix “E_”, resistors have the prefix “R_”, etc. When writing sorting program code as well as performing statistical analysis, such prefixes are beneficial for distinguishing devices.

Each kind of device can also have its own denominations. For instance, regular capacitors may have four different neighborhood distances, hence four L’s on each die. Each L can have its own denomination’s alphabetic descriptor such as “A”, “B”, “C”, and “D”. Each denomination will still contain a number of devices which can be numbered for simplicity. Of course, if the denomination contains more than a hundred devices, one might try finding another way of breaking down the denomination into smaller denominations. Another useful hint is when numbering more than ten devices, use “01” to represent “1”, “02” to represent “2”, and so on. It is most useful later when character matching in the sorting programs. Using this hierarchical naming scheme, the device name for L capacitors will be “C_A01” to “C_A32”, “C_B01” to “C_B32” and so on.

7. Sometimes, the third level is subdie or probe layout naming, and the device naming is the fourth level. However, this is not recommended when there are a large number of probe-layouts (as in the L die layout) since there is usually no distinguishing characteristic about probe-layouts, hence numbering them is the only naming method. If there are many probe-layouts, numbers can become confusing. Device naming is thus more appropriate than probe-layout naming since devices have individual characteristics.

2.7.2 Assigning Factor Identifiers

Each unreplicated device within a die has its own combination of factors which is sometimes not captured in its name. Assigning factor identifiers for each device makes the statistical analysis process easier because it gives the statistics program direct information on what factor levels the device is assigned. For example, L capacitors have six different factors, i.e. finger width, spacing, length, number of fingers, orientation and neighborhood distance. All except neighborhood distance and orientation have three levels (including centerpoint), whereas neighborhood distance has four levels, and orientation has two. When assigning factor identifiers, one can use different numbers for each factor, and use alphabetic characters for each level. Therefore, a small finger width can be assigned the identifier “1L” (low), a large finger width can be assigned “1H” (high) and a medium large finger width can be assigned “1C” (centerpoint). Finger spacings will be assigned “2L”, “2H”, and “2C”, and so on. When there are more than three levels (such as for neighborhood distance), consequent alphabets can be used such as “A”, “B”, “C”, “D” etc.

2.7.3 Data Filtering

After electrical characterization, the data set will usually contain a few bad data points. These data points include slightly high or low values, extremely high or low values, and out of bound values which are generated by the machine when an erroneous measurement is taken. The extremely high or low values, and out of bound values should be segregated immediately by the sorting programs into a separate “bad data” file before statistical analysis is performed. This follows the principle of not throwing data away. If the filtering process is later found to be erroneous, the filtered data is conveniently found in the “bad data” file, hence saving the need for retaking the data.

The slightly high or low values should be kept for statistical analysis. Using the statistical results, one can recheck the layouts and designs to see if there were flaws which may

have caused the inconsistencies in data. If there were flaws, then the data should also be segregated. Otherwise, one has no choice but to assume that the outliers are real phenomena.

2.8 Data Conversion, Sorting, and Calculation Procedure Flow

This section explains the steps for converting, sorting and calculating parameters for the data files before the ILD thickness can be extracted. Figure 2.22 shows a flow chart for the steps.

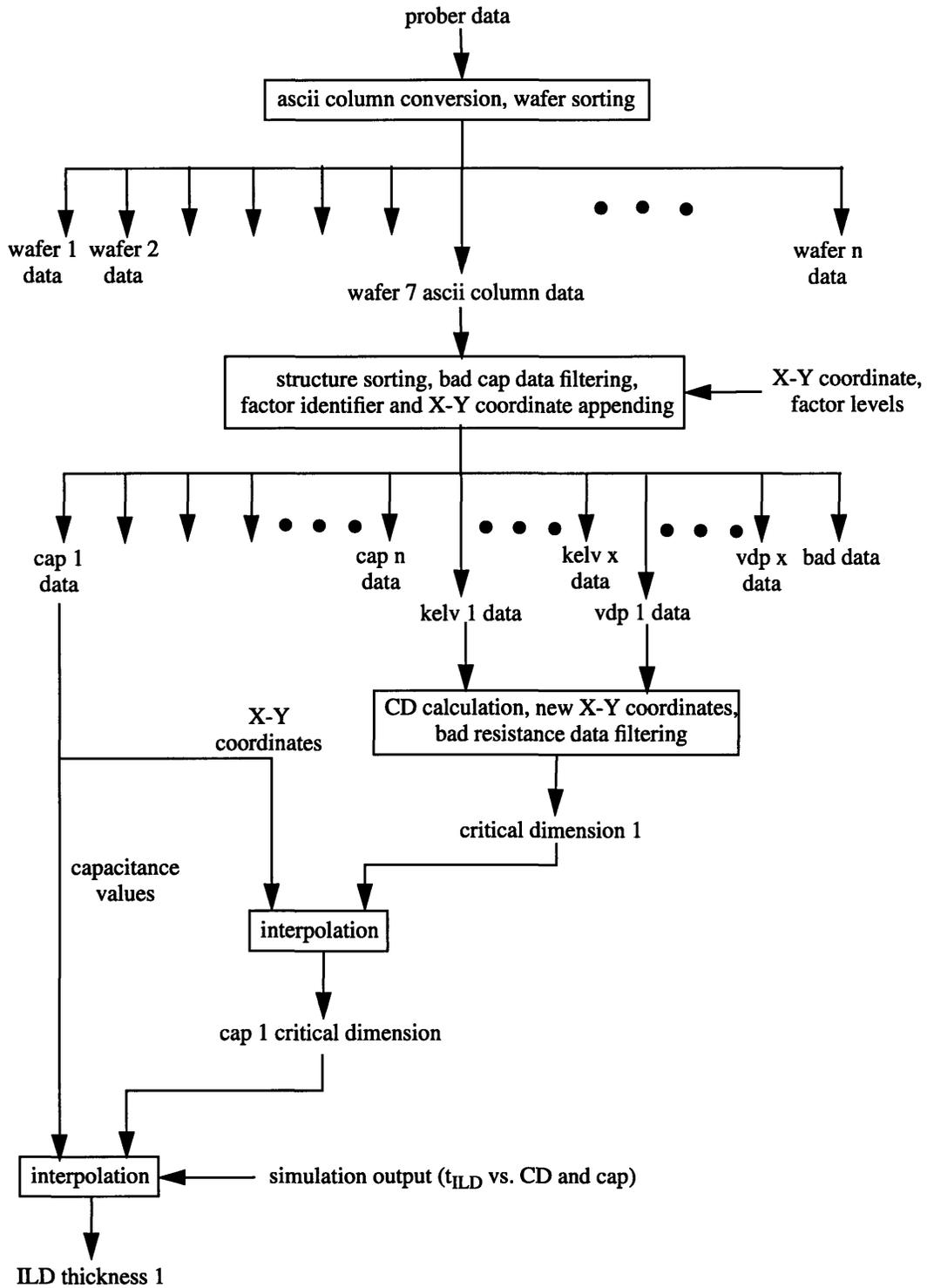


Figure 2.22: Data conversion, sorting, and calculation flow chart

Data from the automatic prober is typically not in ascii column format and thus must be converted before any sorting and calculations can be done. The columns should include wafer number, die number, device name, capacitance or resistance data, X coordinate and Y coordinate. The prober file may or may not include the X-Y coordinates, but a separate file with the locations can be referred to in the conversion or sorting programs. The conversion program can also filter any bad capacitance data points and place them in a “bad capacitance data” file.

Once the information is in ascii column format, a sorting program can separate the data into different files, whereby each file contains data for only one type of structure for each wafer. These files should be placed in directories which are distinguished by wafer number. This sorting program also appends the factor identifiers and X-Y coordinates (if not done so in previous steps).

After the data is sorted into the respective files, the resistance data in the resistor files can be used to calculate (using Equation 2.1) and output the critical dimensions to some new critical dimension files. At the same time, any bad resistance data is segregated into a “bad resistance data” file. Note that if either a Kelvin or a van der Pauw in a probe layout yields bad data, both the resistors must be discarded. This is the reason why the resistance data is filtered at this stage instead of during the file sorting. The new X-Y coordinates for the critical dimensions are also appended to those files after being calculated as the average of the Kelvin X-Y coordinate and the van der Pauw X-Y coordinate.

The simulation output files (described in subsection 2.6.1) and prober (critical dimension and capacitance) files are then read into a statistics program such as SPLUS. Interpolation is performed on the critical dimension files for the capacitor locations. Following this, interpolation for the ILD thickness can then be performed.

2.9 Data Analysis

This section briefly touches on portions of the data analysis which includes statistical analysis as well as signal processing and fitting for variation decomposition. The statistical analysis focuses on Analysis of Variance methods which models how much each factor contributes to the ILD thickness variation. The signal processing decomposes the variation into its constituent components.

2.9.1 Analysis of Variance

Analysis of Variance can be calculated by statistical programs such as SPLUS. Given the factor levels and data, the program can determine how much each factor contributes to the ILD thickness variation. Pareto charts or Main Effects plots can be used to display the extent of the factor contributions as seen in Chapter 3.

2.9.2 Variation Decomposition⁸

Variation decomposition uses spline-fits and signal processing. Wafer-scale variation is assumed to be low-frequency variation, hence a moving average of the data can approximate the wafer-scale variation rather well. After the wafer-scale variation is subtracted from the data, signal processing using a Fast Fourier Transform method exploits the periodicity of die locations to extract the die-scale variation. This is because periodic data in the spatial domain transforms to a periodic impulse train in the frequency domain which can be easily extracted. After the die-scale variation is subtracted, the wafer-die interaction variation can be removed via a spline-based fit. A flow chart of the analysis is shown in Figure 2.23.

8. The variation decomposition methods were developed by Brian Stine, a member of the MIT statistical metrology group.

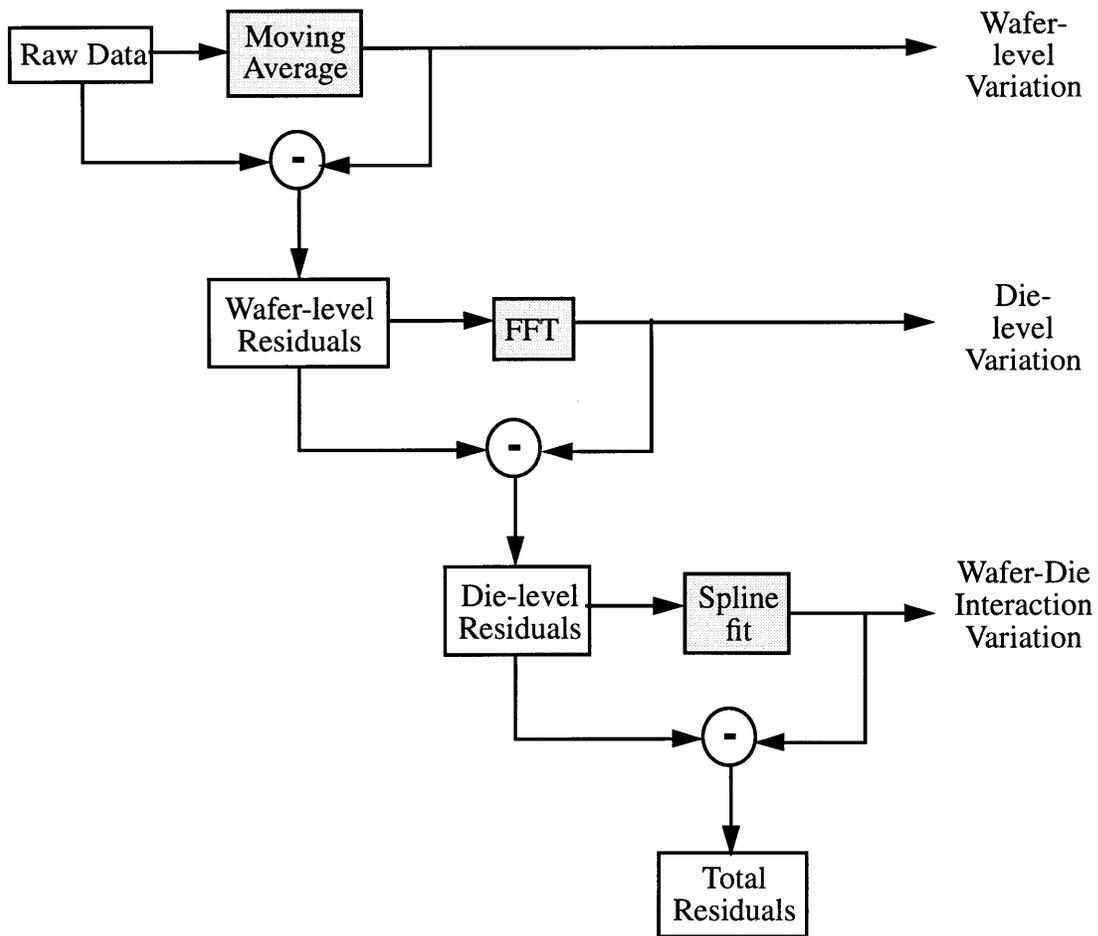


Figure 2.23: Variation decomposition flow chart

2.10 Validation of Assumptions

During the course of using statistical metrology for characterizing ILD thickness, there were several assumptions that were made. Some of these assumptions can be validated by performing extra measurements. The following details these assumptions and how they are verified:

2.10.1 Does Capacitor Area Affect ILD Thickness in a Dummy-line Environment?

When designing the regular capacitors in the L design, it was assumed that capacitor area in a dummy-line environment did not have a large effect on ILD thickness. This assumption evolved from the hypothesis that the CMP polishing pad does not distinguish

between small differences in areas which are below the planarization length. The Area test structures described in Section 2.4.3 try to validate this assumption by comparing if areas larger or smaller than the planarization length have an effect on the ILD thickness. Note that if the Area capacitors show an effect from the area, there is still no conclusion that the CMP polishing pad distinguishes between small differences in areas below the planarization length. Furthermore, Area capacitors have dummy-lines stretching all the way to the device, with a minimum neighborhood distance. L capacitors have dummy-lines stretching to a neighborhood distance from the device. The Area structures thus cannot prove that capacitor area separated by a large neighborhood distance to dummy-lines, does not affect ILD thickness. Due to lack of layout area and time in the LSI Logic experiment, these proofs are left to a future experiment.

2.10.2 Are Interpolated Critical Dimensions Representative of Capacitor Critical Dimensions?

Mathematical interpolations are used to estimate the critical dimensions at the capacitor locations. To verify if these interpolations are correct, top-down SEM critical dimension measurements (non-destructive) can be performed at both the Kelvin location, and at the capacitor location. SEM critical dimension measurements can usually only be done on thin interconnect lines. Fortunately, critical dimension variation is proportionally smaller for wide lines.

2.10.3 Is the Field Oxide and M1's Thickness Variation Small Enough to Neglect in Capacitance Simulations?

Most industrial processes' film deposition variation is very good - a few percent wafer-scale, and less than five to ten percent lot-scale. However, there is never any guarantee that these limits are kept. To ensure that statistical metrology's reliability does not fall victim to poor or abnormal processing, one can use additional measurements to character-

ize the field-oxide and M1 thickness variation. The mean of the measurement thicknesses can also be used as a more accurate simulation thickness than the designed thickness.

Field-oxide thickness is best measured by optical measurements. Measurements can be done on three or more wafers in the lot to monitor the thickness variation. The wafers should include the wafers at the edge and at the center of the boat. Five measurements per wafer (four at edges, with one at center) is a bare minimum.

M1 thickness can be measured using a surface profilometer. The throughput for this measurement is very low, so time may limit the number of measurements that can be performed. A minimum of two wafers should be measured, where the two are close to each edge of the boat. As for the field-oxide measurement, at least five measurements per wafer are needed. When performing the measurements, one must be careful to choose the edge of an area on the die which has a large neighborhood distance (M1 is absent). The profilometer can then use the empty M1 space and the M1 step to level the profile so that the thickness can be calculated.

2.10.4 Does the Electrically Extracted ILD Thickness Correlate with Optical and SEM Cross-section ILD Thicknesses?

Although the electrical (statistical metrology) method of extracting the ILD thickness has many advantages over other methods, it is still important to calibrate electrical results with results from the alternative methods. This is because statistical metrology is susceptible to error if not properly performed, so correlations with other methods will increase the level of confidence in statistical metrology.

Optical characterization is a reliable method for measuring ILD thickness if the interconnect width is much larger than the beam spot-size. Therefore, the only way of correlating electrical and optical ILD thickness measurements is using the Area capacitors which have wide interconnect lines. Note that the measurements must be done before M2 is

deposited. The throughput for optical measurements is high, so every die can be measured. Some systems such as the Prometrix 750 can only perform one site per die at a time, hence making multiple sites per die more inconvenient.

SEM cross-sections are cumbersome and destructive measurements because the wafer has to be cleaved at the cross-sections of interest. Throughput is therefore low, although the L die design does try to improve this. Several measurements should be done to yield a statistically significant amount of data which can be correlated with the electrical data. When performing the measurements, one must ensure that the cross-section is perpendicular to the SEM beam so that there are no parallax errors. In addition, one must beware of oxide charging which can create an impression of a larger ILD thickness. Oxide charging in non-environmental SEMs can be prevented by coating the sample with gold. Decorating the ILD with HF can increase the contrast of the SEM picture, however one must be careful not to over-etch the oxide because too much metal overhang will create an impression of a smaller ILD thickness. It is recommended that the cross-sectional surface is polished before SEM measurements to rid the cross-section of metal overhangs or residuals.

2.10.5 Does the Wafer-scale Centerpoint and Blanket Capacitor Data Correlate with the Wafer-scale Portion of the Signal Processing Analysis?

In the L die layout, there are many replicates of centerpoint and blanket capacitors per die which can be used to generate wafer-scale variation models. These wafer-scale models can thus be compared with the wafer-scale portion of the signal processing analysis. If the models are drastically different, this reveals that either statistical metrology is flawed, or the signal processing has bugs.

Chapter 3

Framework Application at LSI Logic

This section illustrates an application of the issues in Chapter 2 on a statistical metrology experiment at LSI Logic Corporation. Section 3.1 is organized similar to Chapter 2 except it contains additional details of how the experiment was performed at LSI Logic. Section 3.2 then shows some experimental data generated from the experiment. Finally, Section 3.3 describes the oversights which occurred during the LSI Logic experiment.

3.1 Experimental Procedure

In previous experiments, neighborhood distance was not characterized as a source of ILD thickness variation [2]. There were no dummy-lines on the chip, hence the test-chip did not emulate conditions on typical product chips. The LSI Logic experiment thus tries to gather data for a chip which better emulates a real-life chip, and which emphasizes the characterization of neighborhood distance effects. In addition, it investigates next-generation test structures and process monitors to aid in development of the methodology and test structure design.

The framework design described in Chapter 2 was applied in an experiment at LSI Logic. The experiment was targeted at characterizing the ILD thickness variation for one of LSI Logic's advanced sub-micron silicon processes. This section describes how the experiment was designed and carried out. For proprietary reasons, minimum interconnect dimensions are not described. Instead, α is defined as the minimum line width, and β is defined as the minimum line spacing for that particular process at LSI Logic. λ is defined as the target ILD thickness value.

3.1.1 Test Structures in Experiment

The main focus of the LSI Logic experiment was the L die design, and its ability to characterize neighborhood distance while emulating conditions on typical product chips. In the upper right quad of the L and in other empty sections of the die, there are also next-generation structures such as Block capacitors, Uni-edge capacitors, and Area capacitors. All of the capacitors except the blanket capacitors have M2 overlapping M1 by 0.4 micron on each side. The ILD blanket capacitor has the M1 overlapping the M2 by 0.4 micron on each side. The M1 overlap versus an M2 overlap for the ILD blanket capacitor was no longer advantageous when capacitance measurements were done without connecting the Low terminal to the substrate. Hence, an M2 overlap over M1 for the ILD blanket capacitor will work just as well.

3.1.1 a) L Capacitors and Resistors

The L capacitors were varied using six factors: line width, spacing, length, number of fingers, orientation, and neighborhood distance. Line width, spacing, length, and number of fingers have two-levels and a centerpoint, orientation has two-levels without a centerpoint, and neighborhood distance has four-levels (without centerpoint). For the full-factorial experiment, the five factors without the neighborhood distance generates 34 unique structures which include two centerpoints with different orientations. Therefore, for four-levels of neighborhood distance, there are a total of 136 unique structures. The two centerpoints with a minimum neighborhood distance are replicated another eight times each and are located in various parts of the die. The reason for the replication is so that a die-mapping of ILD thickness for this particular structure can be produced. The factor levels (H(igh), L(ow), C(enterpoint)), and device/structure numbering are shown in Table 3.1. Each factor is assigned a factor number, hence line width (lw), spacing (ls), number of fin-

gers (nof), finger length (fl), geometric orientation (go), and neighborhood distance (nd), are assigned numbers 1 to 6 respectively.

Structure #	Line width	Line spacing	# of fingers	Finger length	Orientation
	1H: $\alpha+8 \mu\text{m}$	2H: $\beta+8 \mu\text{m}$	3H: 62	4H: $685 \mu\text{m}$	5H: 90°
	1L: $\alpha \mu\text{m}$	2L: $\beta \mu\text{m}$	3L: 42	4L: $343 \mu\text{m}$	5L: 0°
	1C: $\alpha+4 \mu\text{m}$	2C: $\beta+4 \mu\text{m}$	3C: 52	4C: $514 \mu\text{m}$	
1	L	L	L	L	H
2	H	L	L	L	H
3	L	H	L	L	H
4	H	H	L	L	H
5	L	L	H	L	H
6	H	L	H	L	H
7	L	H	H	L	H
8	H	H	H	L	H
9	L	L	L	H	H
10	H	L	L	H	H
11	L	H	L	H	H
12	H	H	L	H	H
13	L	L	H	H	H
14	H	L	H	H	H
15	L	H	H	H	H
16	H	H	H	H	H
17	L	L	L	L	L
18	H	L	L	L	L
19	L	H	L	L	L
20	H	H	L	L	L
21	L	L	H	L	L
22	H	L	H	L	L
23	L	H	H	L	L

Table 3.1: Factor levels and numbering of devices

Structure #	Line width	Line spacing	# of fingers	Finger length	Orientation
24	H	H	H	L	L
25	L	L	L	H	L
26	H	L	L	H	L
27	L	H	L	H	L
28	H	H	L	H	L
29	L	L	H	H	L
30	H	L	H	H	L
31	L	H	H	H	L
32	H	H	H	H	L
33	C	C	C	C	H
34	C	C	C	C	L

Table 3.1: Factor levels and numbering of devices

The L capacitors are named as following. All the L capacitors have a “C_” prefix. Depending on their neighborhood distance, the capacitors are assigned a descriptor, “A”, “B”, “C”, or “D”, whereby “A” has a neighborhood distance of β micron (minimum spacing), “B” with 40 micron, “C” with 120 micron, and “D” with 400 micron. The “A” distance of α micron was chosen because it was the minimum line spacing. Numeric descriptors 01 to 32 are assigned to the non-centerpoint capacitors starting from the top of the “L” to the center, and ending at the right of the “L”. The factors for the “A” capacitors adhere to the structure numbering in Table 3.1. The factors for “B”, “C”, and “D” capacitors are randomized as shown in Figure 3.1. All groups of capacitors (“A” to “D”) have at least two centerpoints with numeric descriptors 33 and 34. There are also centerpoint replicates with a minimum neighborhood distance (“A”) that have the numeric descriptors 35 to 50. These geometric orientations of these replicates are as shown in Table 3.2. The L capacitors thus have the names “C_A01”, “C_A02”, ..., “C_A50”, “C_B01”, “C_B02”, ..., “C_B34”, “C_C01”, “C_C02”, ..., “C_C34”, “C_D01”, “C_D02”, ..., “C_D34”.

Each L capacitor has its corresponding Kelvin and van der Pauw resistors. The Kelvins and van der Pauws both have the prefix “R_”. Like the capacitors, the Kelvins have different alphabetic descriptors assigned to them for their corresponding capacitor’s different neighborhood distances. The minimum to maximum neighborhood distance will have the alphabetic descriptors “E”, “F”, “G”, and “H”. The van der Pauws have the alphabetic descriptors “J”, “K”, “L”, and “M”. The character “I” had been reserved for a row of extra and now unnecessary van der Pauws which are no longer measured. The numbering is similar to that of the capacitors. The resistors thus have the names “R_E01”, “R_E02”, ..., “R_E50”, “R_F01”, R_F02”, ..., “R_F34”, “R_G01”, “R_G02”, ..., “R_G34”, “R_H01”, “R_H02”, ..., “R_H34”, “R_J01”, “R_J02”, ..., “R_J50”, “R_K01”, “R_K02”, ..., “R_K34”, “R_L01”, “R_L02”, ..., “R_L34”, “R_M01”, “R_M02”, ..., “R_M34”.

The locations of the L capacitors can be seen in Figure 3.2. For sake of clarity in the figure, the locations of the corresponding resistors are not shown.

Struct #	Orientation	Struct #	Orientation
	5H: 90°		5L: 0°
33	H	34	L
35	H	39	L
36	H	40	L
37	H	41	L
38	H	42	L
45	H	43	L
46	H	44	L
47	H	48	L
50	H	49	L

Table 3.2: Replicated centerpoint geometric orientations

L Descriptors	Structure type
A (1-50)	capacitor with $nd = \alpha \mu\text{m}$
B (1-34)	capacitor with $nd = 40 \mu\text{m}$
C (1-34)	capacitor with $nd = 120 \mu\text{m}$
D (1-34)	capacitor with $nd = 400 \mu\text{m}$
E (1-50)	Kelvin in A's probe layout
F (1-34)	Kelvin in B's probe layout
G (1-34)	Kelvin in C's probe layout
H (1-34)	Kelvin in D's probe layout
I (1-34, some missing)	extra L of VDP (unnecessary)
J (1-50)	VDP in A's probe layout
K (1-34)	VDP in B's probe layout
L (1-34)	VDP in C's probe layout
M (1-34)	VDP in D's probe layout

Table 3.3: Descriptor types for L devices

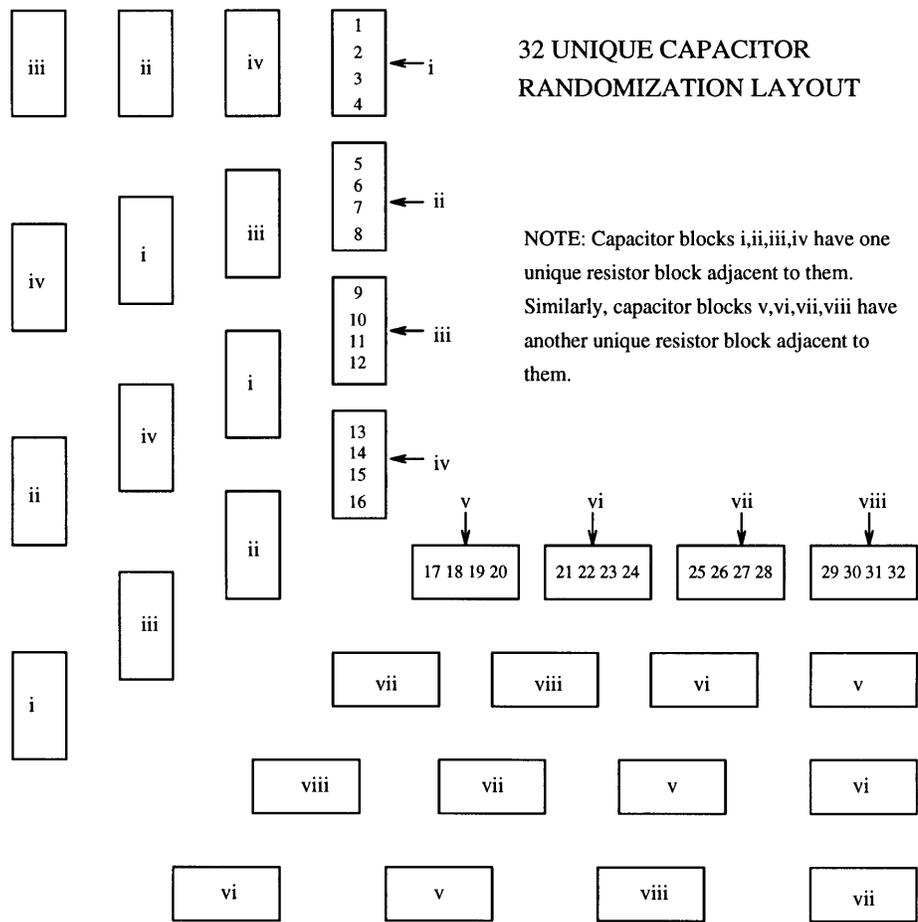


Figure 3.1: Partial randomization of L capacitor groups.

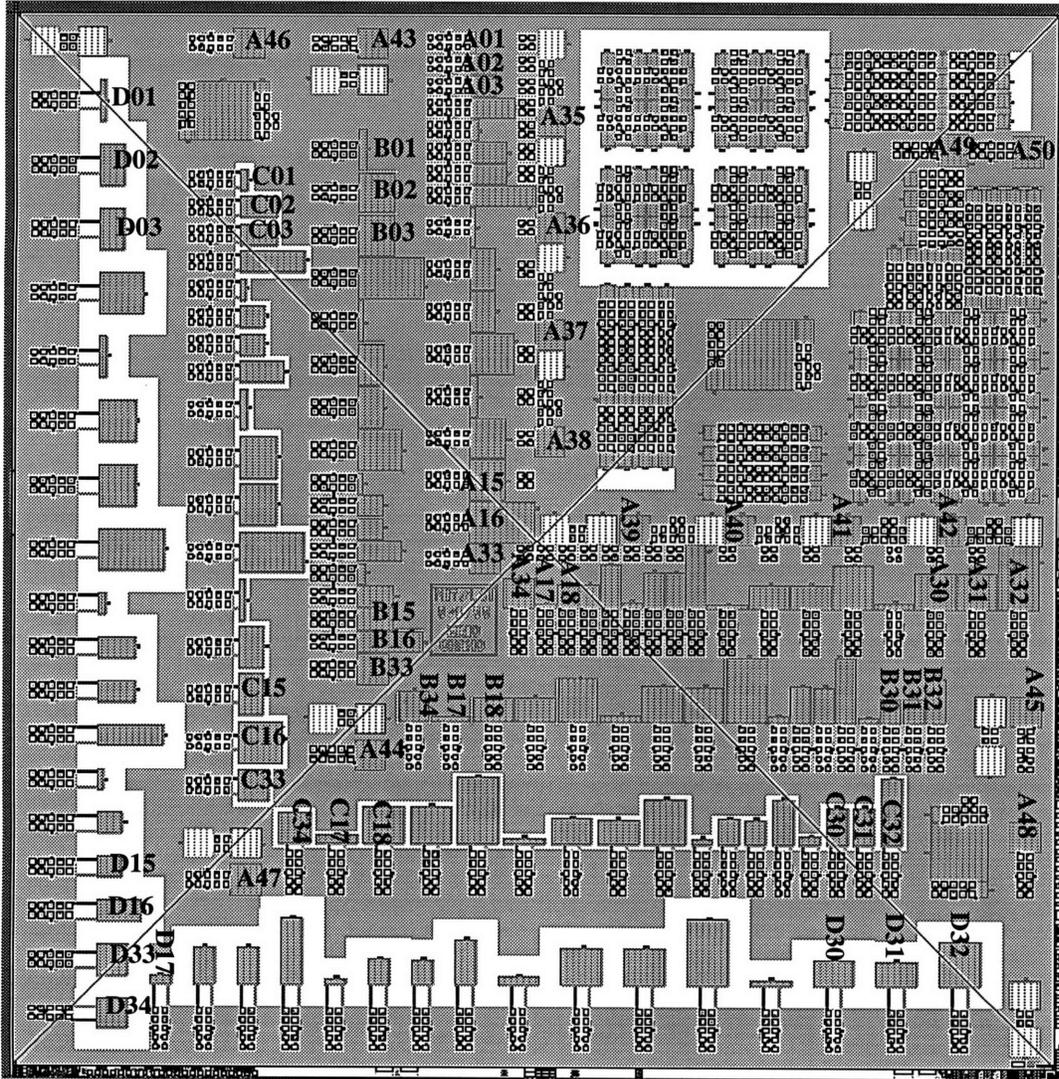


Figure 3.2: L capacitors' locations.

3.1.1 b) Block Capacitors and Resistors

Block capacitors are located in the top-right quad in the die. Each block of Block capacitors contain sixteen similarly pitched capacitors arranged in a 4 x 4 square. The capacitors along the edge have a defined neighborhood distance of either 40 micron or 400 micron, while the inside capacitors are closely packed to each other (minimum neighbor-

hood distance of β micron). There are eight blocks of Block capacitors on each die. Four of these blocks have an edge-capacitor neighborhood distance of 40 micron while the other four have an edge-capacitor neighborhood distance of 400 micron. The four blocks for both cases are for the four combinations of line width and spacing with two-levels each (as in L capacitors).

The Block capacitors have the prefix “E_”. Each block of sixteen capacitors have their own assigned alphabetic descriptors as described in Table 3.4. Note that since there are only 26 alphabetic characters, and hence not enough for all the different devices, some descriptors use two characters as in this case. The sixteen capacitors also have their own number from 01 to 16 which are arranged in a left to right fashion as shown in Figure 3.3. The Block resistors are exactly like the L resistors, hence their naming prefix is also “R_”. This is because critical dimension interpolation is performed on all similar resistors, irrespective of their type (L or Block). The resistors also have their own assigned alphabetic descriptors which are shown in Table 3.4. Since there are only four Kelvins and four van der Pauws for every block, the numeric descriptors range from 1 to 4 in a left to right fashion as seen in Figure 3.3. Figure 3.3 also shows how the Block devices are arranged in the top right quad of the die.

Since the number and direction of exposed capacitor sides to the neighborhood distance depend on where the capacitor is located in the block, a new factor is defined for the Block capacitor. This factor is called “exposed sides” (es), and it is assigned the factor number “7” with nine levels. Nine levels are needed because there are four sides and four diagonals for the block, as well as center capacitors which have zero exposed sides. The nine levels are named L(eft), R(ight), T(op), B(ottom), W (top left), X (top right), Y (bottom left), Z (bottom right), and N(one). The factor levels are related to the structure numbering by the mapping in Table 3.5.

Block Descriptors	Structure type	lw	ls	outer cap's nd
		1H: $\alpha+8 \mu\text{m}$	2H: $\beta+8 \mu\text{m}$	6B: $40 \mu\text{m}$
		1L: $\alpha \mu\text{m}$	2L: $\beta \mu\text{m}$	6D: $400 \mu\text{m}$
AA (1-16)	capacitor	H	H	B
AB (1-16)	capacitor	H	L	B
AC (1-16)	capacitor	L	H	B
AD (1-16)	capacitor	L	L	B
AE (1-4)	Kelvin in AA's probe layout	H	H	n/a
AF (1-4)	Kelvin in AB's probe layout	H	L	n/a
AG (1-4)	Kelvin in AC's probe layout	L	H	n/a
AH (1-4)	Kelvin in AD's probe layout	L	L	n/a
AI (1-4)	VDP in AA's probe layout	n/a	n/a	n/a
AJ (1-4)	VDP in AB's probe layout	n/a	n/a	n/a
AK (1-4)	VDP in AC's probe layout	n/a	n/a	n/a
AL (1-4)	VDP in AD's probe layout	n/a	n/a	n/a
AM (1-16)	capacitor	H	H	D
AN (1-16)	capacitor	H	L	D
AO (1-16)	capacitor	L	H	D
AP (1-16)	capacitor	L	L	D
AQ (1-4)	Kelvin in AM's probe layout	H	H	n/a
AR (1-4)	Kelvin in AN's probe layout	H	L	n/a
AS (1-4)	Kelvin in AO's probe layout	L	H	n/a
AT (1-4)	Kelvin in AP's probe layout	L	L	n/a
AU (1-4)	VDP in AM's probe layout	n/a	n/a	n/a
AV (1-4)	VDP in AN's probe layout	n/a	n/a	n/a
AW (1-4)	VDP in AO's probe layout	n/a	n/a	n/a
AX (1-4)	VDP in AP's probe layout	n/a	n/a	n/a

Table 3.4: Descriptor types for Block devices

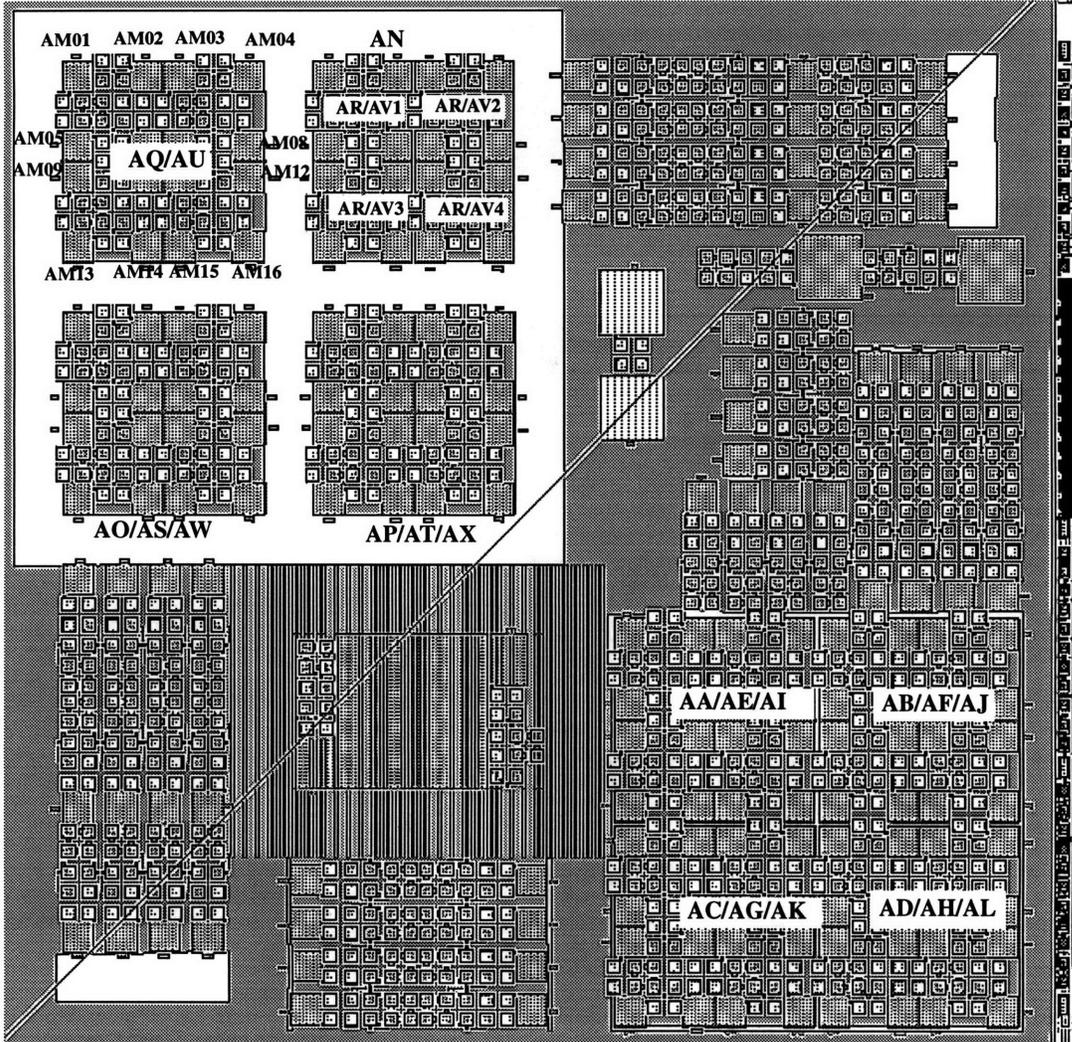


Figure 3.3: Block device numeric descriptors and locations.

Capacitor #	nd	es
	6A: $\alpha \mu\text{m}$	7?: refer to prev. paragraph
	6B: $40 \mu\text{m}$	
	6D: $400 \mu\text{m}$	
1	B or D	W
2	B or D	T

Table 3.5: Numeric types for Block capacitors

Capacitor #	nd	es
3	B or D	T
4	B or D	X
5	B or D	L
6	A	N
7	A	N
8	B or D	R
9	B or D	L
10	A	N
11	A	N
12	B or D	R
13	B or D	Y
14	B or D	B
15	B or D	B
16	B or D	Z

Table 3.5: Numeric types for Block capacitors

3.1.1 c) Uni-edge Capacitors and Resistors

Uni-edge capacitors are hybrid structures between L capacitors and Block capacitors. Since there are four unique combinations of line width and spacing, two neighborhood distances (outer capacitors), and nine exposed sides for the Block capacitors, Uni-edge capacitors also follow suit. The only difference is that Uni-edge capacitors do not have the four exposed sides for the diagonals as in the Block capacitors, hence Uni-edge capacitors only have five types of exposed sides: L(ef), R(igh), T(op), B(ottom), and N(one) (minimum neighborhood distance). Therefore, there are four capacitors per side of each block for the four combinations of line width and spacing. The four sides thus make a total of sixteen capacitors, which is tripled for the two non-minimum neighborhood distances and for exposed sides equal to “None”. There are hence 48 Uni-edge capacitors for each die.

The naming prefix for Uni-edge capacitors is “D_”. The alphabetic descriptors for the capacitors are summarized in Table 3.6. The capacitors are placed together in groups of four whereby the four capacitors have different combinations of line widths and spacings. Four of these groups will constitute the four exposed sides of a block, and have a unique neighborhood distance. These sixteen capacitors have numeric descriptors from 01 to 16 with a particular alphabetic descriptor. There are thus three of these macro-groups of sixteen capacitors, each with a different neighborhood distance and alphabetic descriptor. As for the L devices, there is a Kelvin and a van der Pauw for each Uni-edge capacitor. These capacitors and resistors have alphabetic descriptors which are summarized in Table 3.6 . The resistors have the same numeric descriptors as the capacitors. Table 3.7 shows the characteristics of each numeric descriptor. Figure 3.4 illustrates how the Uni-edge capacitors are located in the top right quad for every die.

Alphabetic Descriptor	Structure type
BA	Capacitor with $nd = \alpha \mu\text{m}$
BB	Capacitor with $nd = 40 \mu\text{m}$
BC	Capacitor with $nd = 400 \mu\text{m}$
BD	Kelvin in BA's probe layout
BE	Kelvin in BB's probe layout
BF	Kelvin in BC's probe layout
BG	VDP in BA's probe layout
BH	VDP in BB's probe layout
BI	VDP in BC's probe layout

Table 3.6: Uni-edge device alphabetic descriptors

Struct #	lw	ls	es	
	1H: $\alpha+8 \mu\text{m}$	2H: $\beta+8 \mu\text{m}$??: refer to prev. paragraph	
	1L: $\alpha \mu\text{m}$	2L: $\beta \mu\text{m}$	BA	BB or BC
1	H	H	N	R
2	H	L	N	T
3	L	H	N	L
4	L	L	N	B
5	H	H	N	R
6	H	L	N	T
7	L	H	N	L
8	L	L	N	B
9	H	H	N	R
10	H	L	N	T
11	L	H	N	L
12	L	L	N	B
13	H	H	N	R
14	H	L	N	T
15	L	H	N	L
16	L	L	N	B

Table 3.7: Uni-edge device numeric descriptors

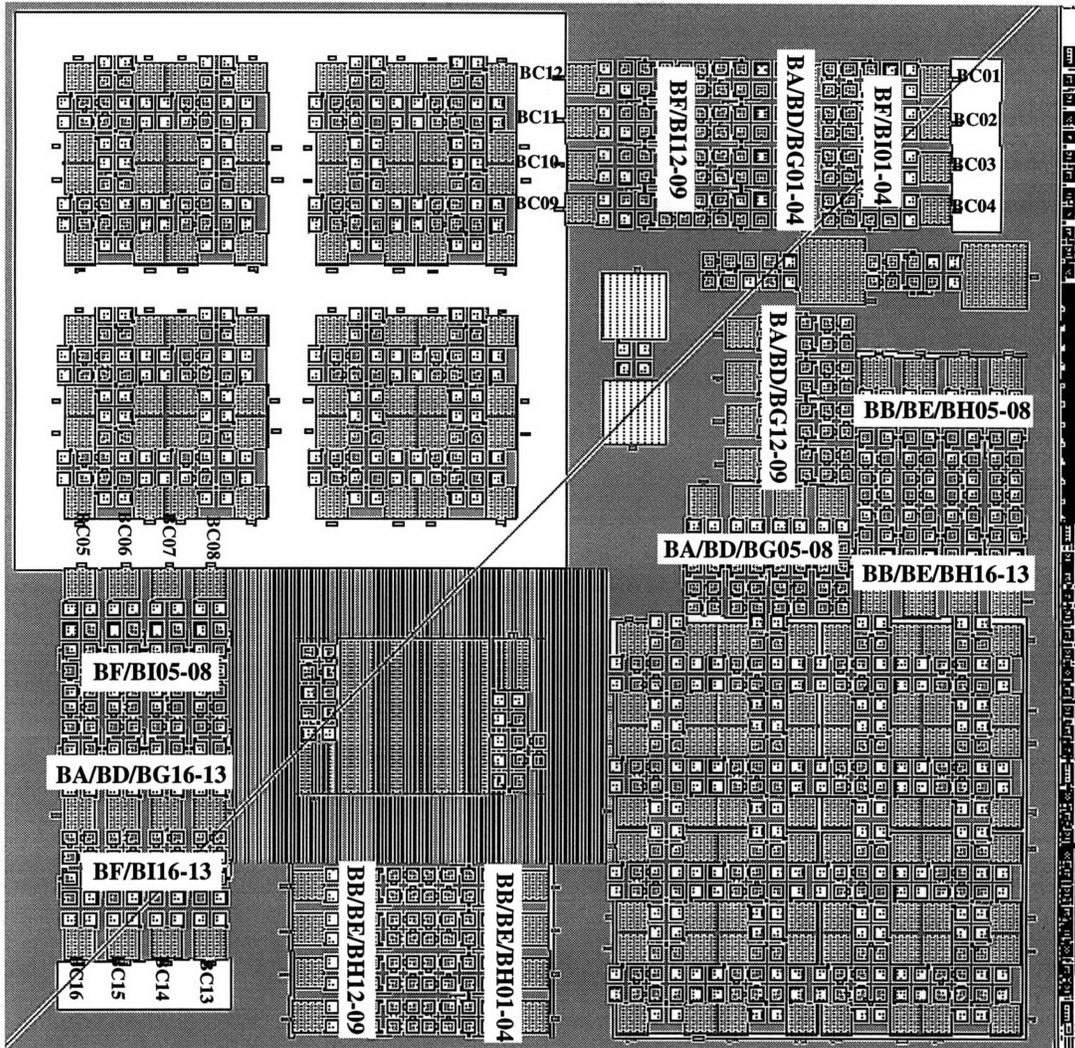


Figure 3.4: Uni-edge device locations in top-right quad.

3.1.1 d) Area Capacitors and Resistors

The Area capacitors are located in groups of three, whereby a large area capacitor is sandwiched by two smaller capacitors. There are three of these groups, two of which have a minimum line width of α micron, and the third with a line width of 18.4 micron. All three groups have a minimum line spacing of β micron. The areas for the capacitors are shown in Table 3.8.

Since there is now a new line width, a new factor level, W(ide) is defined for the 18.4 micron line width. In addition, a new factor is also defined as “size of capacitor” (sc). This factor is assigned the factor number “8” with two levels, H(igh) and L(ow) whereby the High level is the large area and the Low level is the small area.

The prefix for the Area capacitor is “F_”. The alphabetic descriptor for the capacitors is “CA”, while the descriptors for the Kelvin and van der Pauws are “CB” and “CC” respectively. Numeric descriptors 1 to 3 describe the capacitor group in the top-left corner of the die, 4 to 6 describe the group in the bottom-right corner of the die, and 7 to 9 describe the capacitor group in the top-right quad (Table 3.8). Note that there are no resistors for the center (large) capacitor, hence there is a lack of numeric descriptors 2, 5, and 8 for the resistors. The locations of the Area devices are shown in Figure 3.5.

Structure #	lw	go	sc	Capacitor area (μm^2)
	1W: 18.4 μm	5H: 90°	8H: large	
	1L: α μm	5L: 0°	8L: small	
1	L	H	L	52160
2	L	H	H	1000398.08
3	L	H	L	52160
4	W	L	L	52160
5	W	L	H	1000398.08
6	W	L	L	52160
7	L	H	L	117354.24
8	L	H	H	1471853.6
9	L	H	L	117354.24

Table 3.8: Area devices’ numeric descriptors

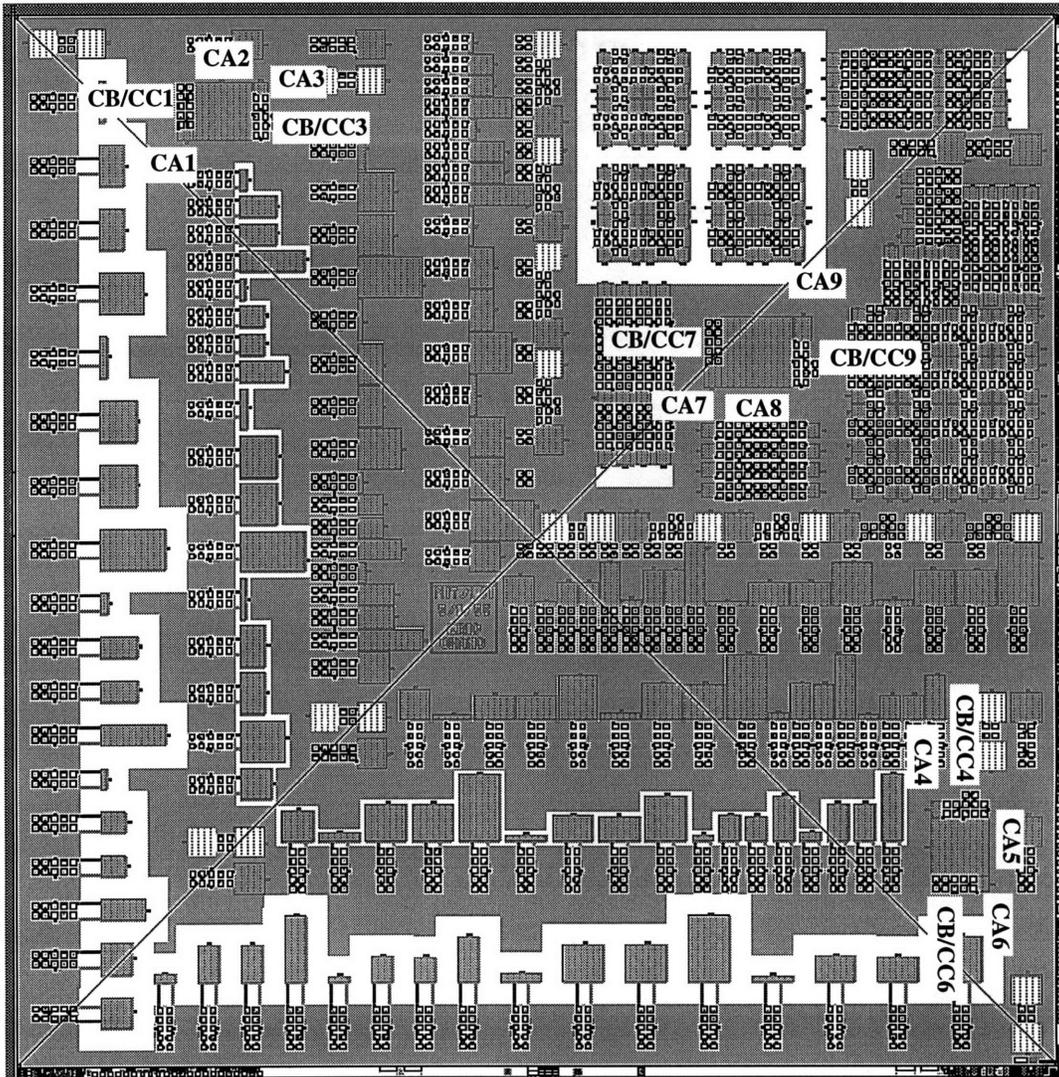


Figure 3.5: Area device locations.

3.1.1 e) Blanket Capacitors

There are ILD blanket capacitors as well as field-oxide blanket capacitors. Both these capacitors have the prefix, “G_”. The ILD blanket capacitor has the alphabetic descriptor, “O” while the field-oxide has the alphabetic descriptor, “N”. There are twelve ILD blanket capacitors and twelve field-oxide blanket capacitors placed in spread-out locations within the die. Therefore, the numeric descriptors range from 1 to 12. These blanket capacitors

do not have any factor identifiers. The location of the blanket capacitors are shown in Figure 3.6.

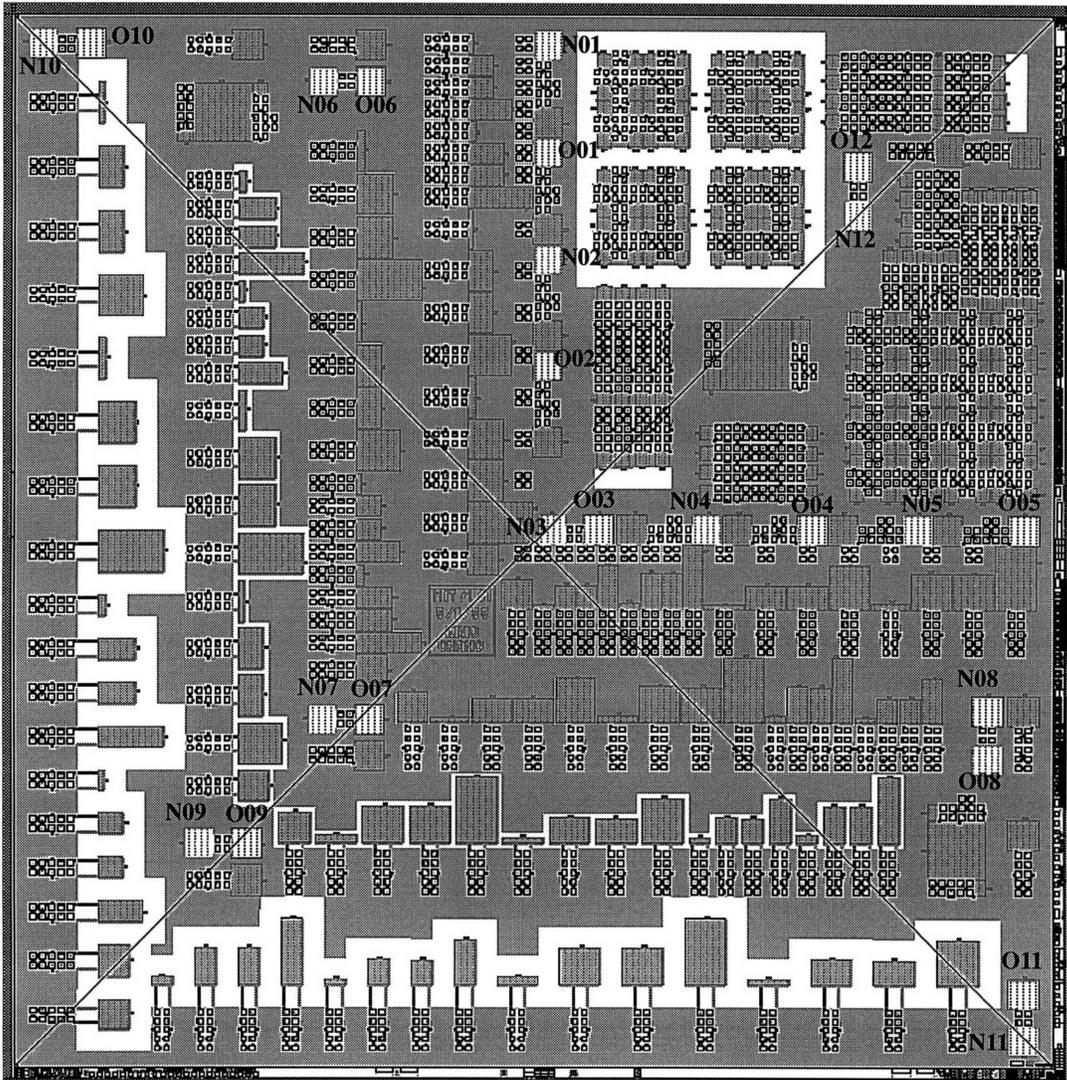


Figure 3.6: Blanket capacitors' locations.

3.1.2 Probe Layout

The LSI Logic experiment uses the T probe-card layout so that probe-pads of different orientations can be measured easily. Figure 3.7 shows the Keithley switching-matrix pin numbers for each of the sixteen pads in the T probe-card layout. These pin numbers are different from the pin numbers printed on the probe-card, however they are linked by the

mapping in Table 3.6. The size of each pad is 100 micron x 100 micron, and the spacing is sixty micron on each side. Following this, the subsection details how the T probe layout is used for different devices in the die.

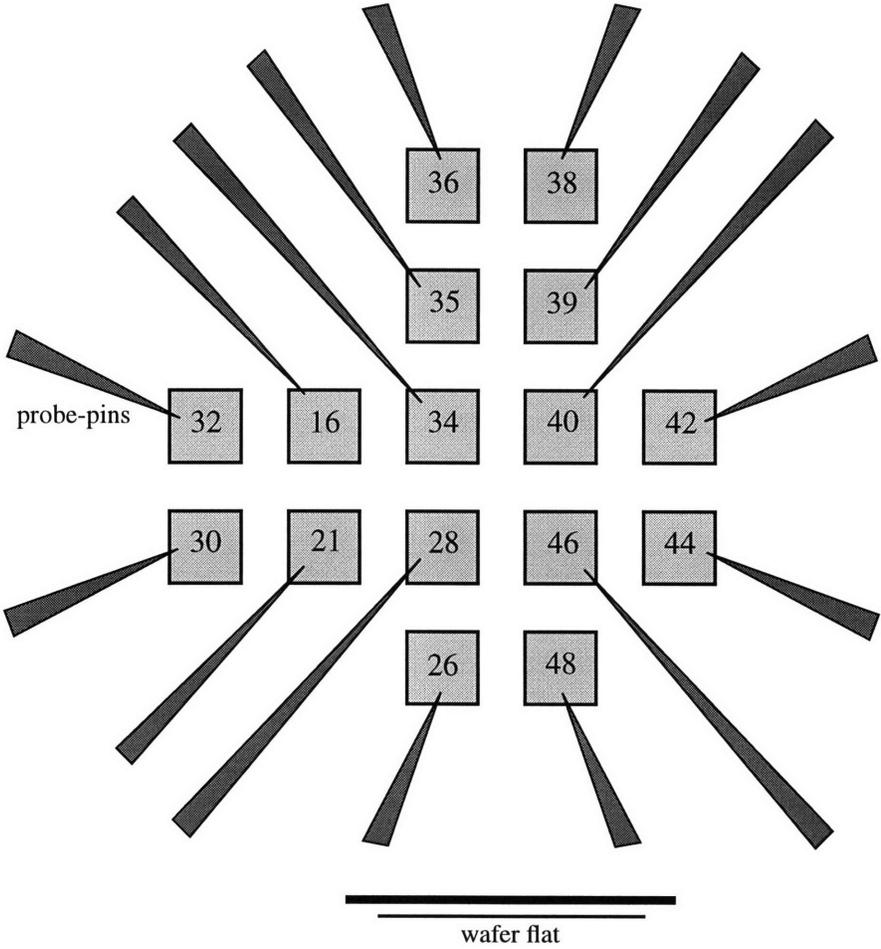


Figure 3.7: Switching-matrix probe pin numbers.

Probe-card numbers	Switching matrix numbers
A	47
C	46
E	44

Table 3.9: Switching matrix and probe-card pin numbers

Probe-card numbers	Switching matrix numbers
H	42
K	40
L	39
M	38
P	36
R	35
S	34
16	16
U	32
W	30
21	21
Y	28
AA	26

Table 3.9: Switching matrix and probe-card pin numbers

3.1.2 a) L Devices Probe Layout

The L devices probe layout has ten probe-pads, with a capacitor, a Kelvin structure, and a van der Pauw structure. The probe layout can either be horizontal or vertical as shown in Figure 3.8. Dummy-lines can either be horizontal or vertical for both the horizontal or vertical probe layouts. The difference is that for a particular probe layout orientation, the orientation of the dummy-lines makes the Kelvin structure use different probing pads as shown in Figure 3.9.

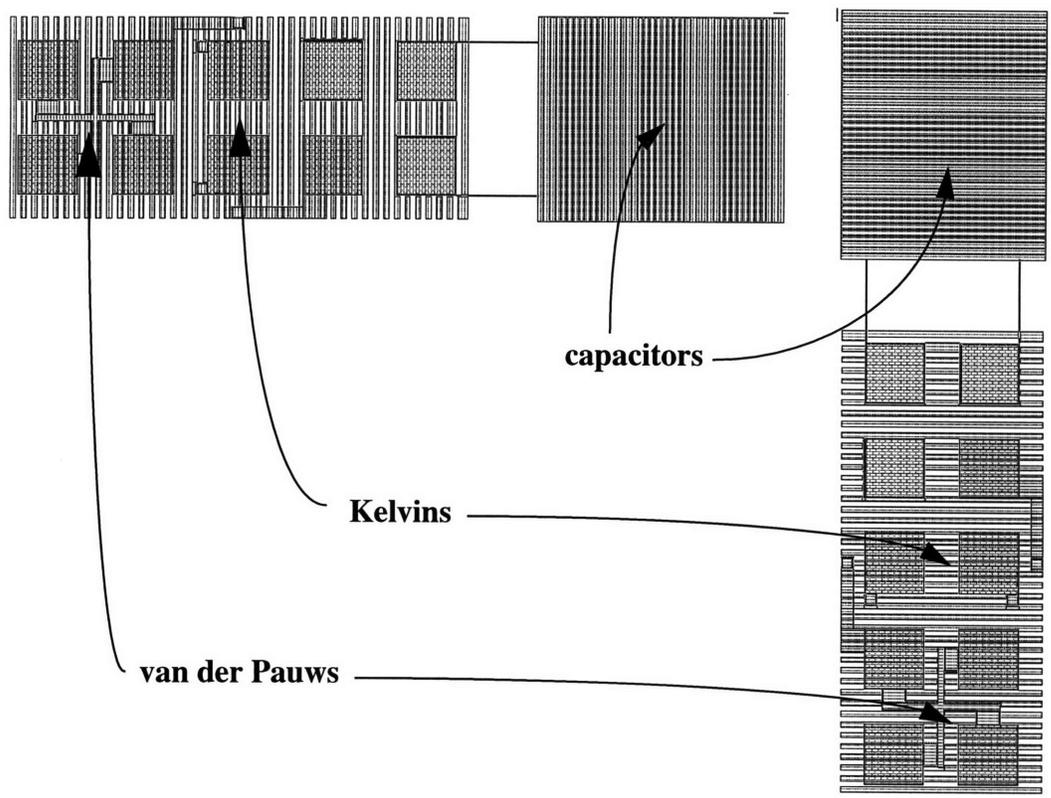


Figure 3.8: L device probe-layout.

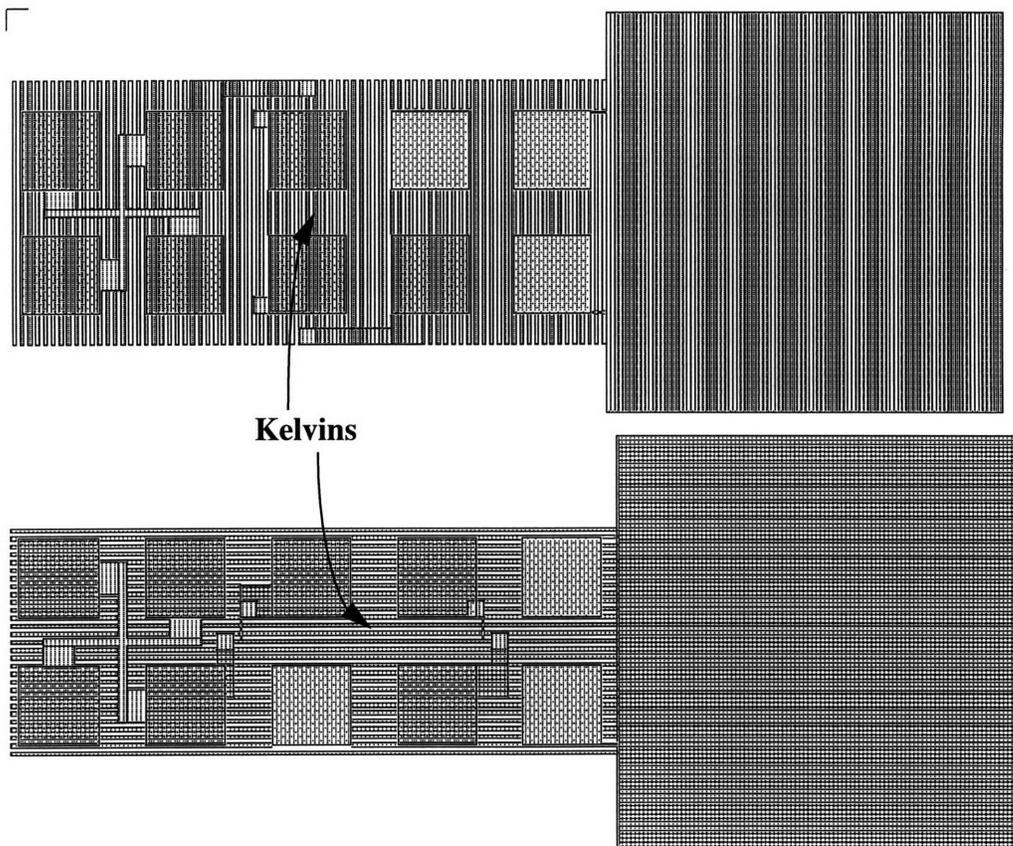


Figure 3.9: Different Kelvin pads for different dummy-line orientations.

3.1.2 b) Blanket Capacitor and Centerpoint Probe Layout

Blanket capacitors are connected to two different kinds of probe-layouts. The first kind is a 2 x 2 pad matrix which is connected to an ILD blanket capacitor and a field-oxide blanket capacitor. This probe-layout can be orientated vertically or horizontally as seen in Figure 3.10.

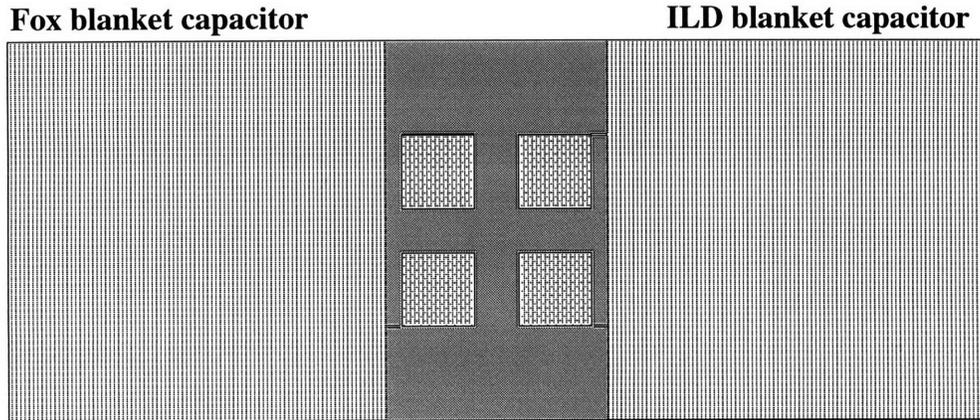


Figure 3.10: Blanket capacitor probe layout I.

A second probe layout for the blanket capacitor also probes the centerpoint capacitor structure. Again, this probe layout can be vertical or horizontal. The layout consists of a centerpoint capacitor, a Kelvin resistor, a van der Pauw resistor, and either an ILD blanket capacitor or a field-oxide blanket capacitor. The layouts for the ILD or field-oxide capacitors are shown in Figure 3.11.

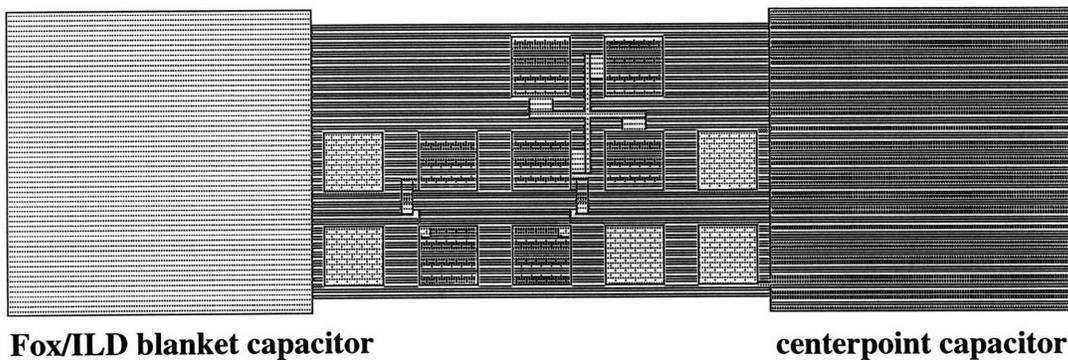


Figure 3.11: Blanket capacitor probe layout II with centerpoint capacitor.

3.1.2 c) Block Device Probe Layout

Each Block device probe layout connects to four capacitors, a Kelvin resistor, and a van der Pauw resistor as shown in Figure 3.12. The probe layout has sixteen pads, and

thus uses all sixteen of the probe-card pins. Four of these probe layouts are placed side by side in a 2 x 2 matrix to form a block of sixteen capacitors. Note that the spacing between each of these four probe layouts is also sixty micron, or the same as the spacing between pads in each probe layout.

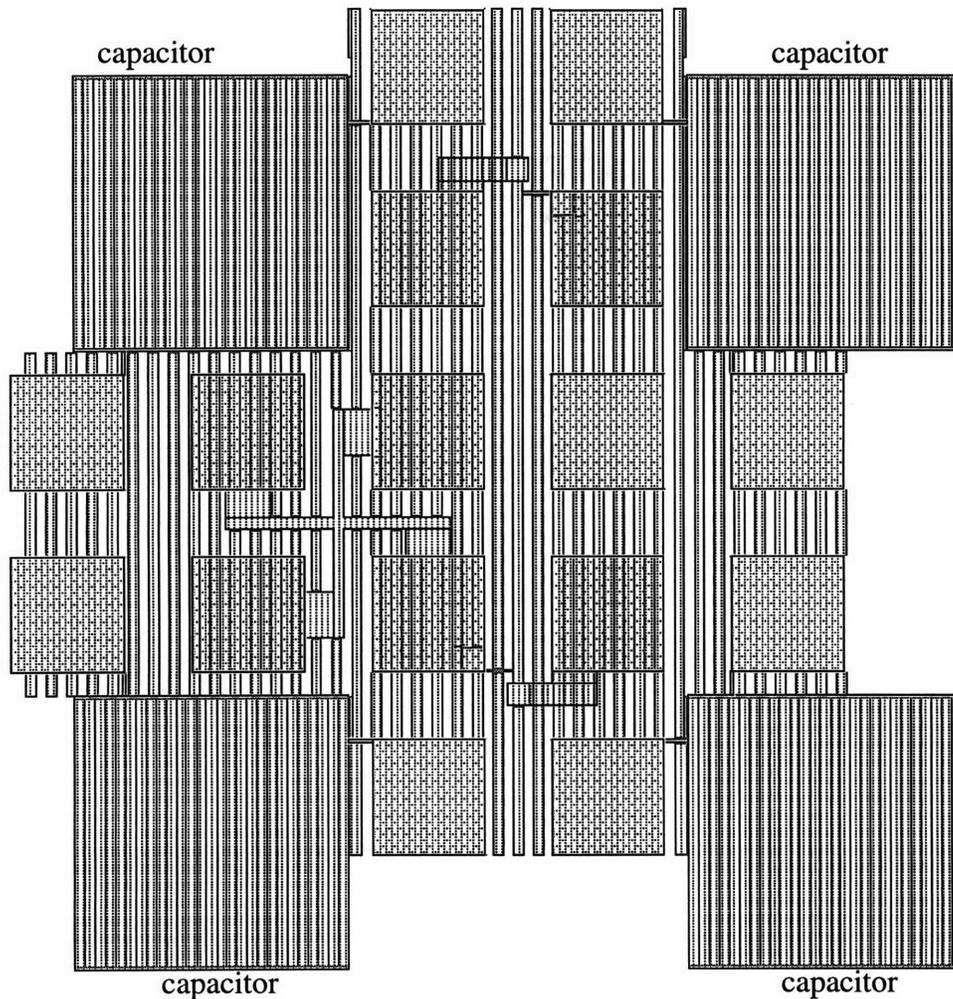


Figure 3.12: Block device probe layout.

3.1.2 d) Uni-edge Device Probe Layout

The Uni-edge probe layout is very similar to the L probe layouts with the minimum neighborhood distance. The only difference is that Uni-edge probe layouts can be orien-

tated in four ways so that they can simulate the four edges of the Block capacitors. This is illustrated in Figure 3.13.

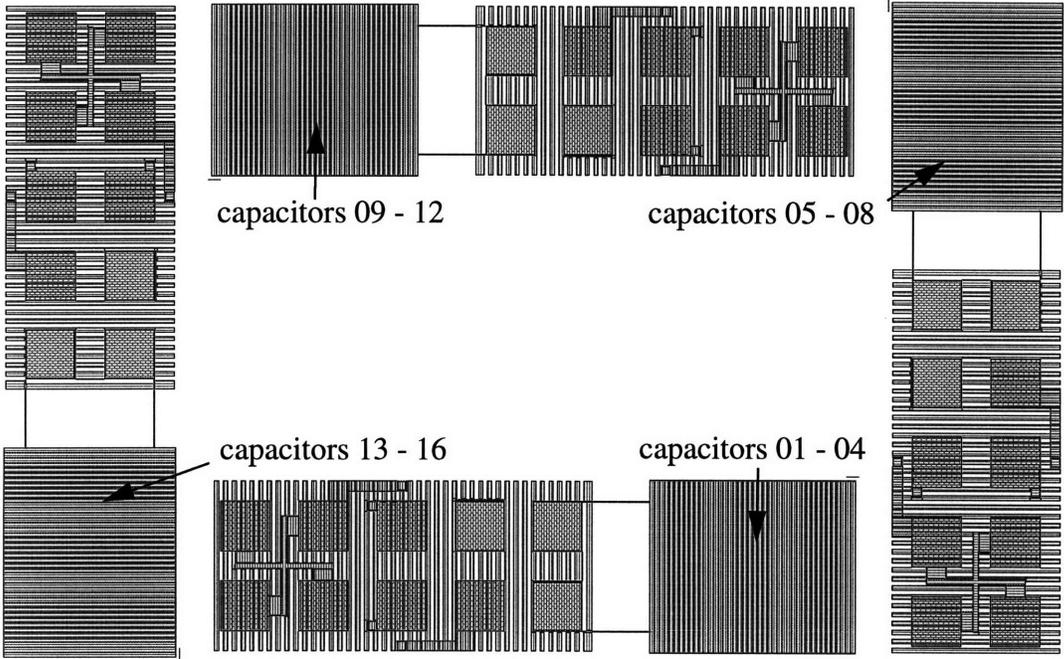


Figure 3.13: The four orientations of the Uni-edge probe layout.

3.1.2 e) Area Device Probe Layout

There are two kinds of Area probe layouts which can have two orientations. One kind has ten pads which connects to a capacitor with a small area, a Kelvin resistor, and a van der Pauw resistor. The second kind has twelve pads which connects to two capacitors (large and small area), a Kelvin resistor, and a van der Pauw resistor. These two layouts are shown in Figure 3.14. The figure has the capacitors outlined in black because the capacitors are camouflaged by the dummy-lines. Note also that the large capacitors shown are one and the same because only a portion of the large capacitor is shown for each layout.

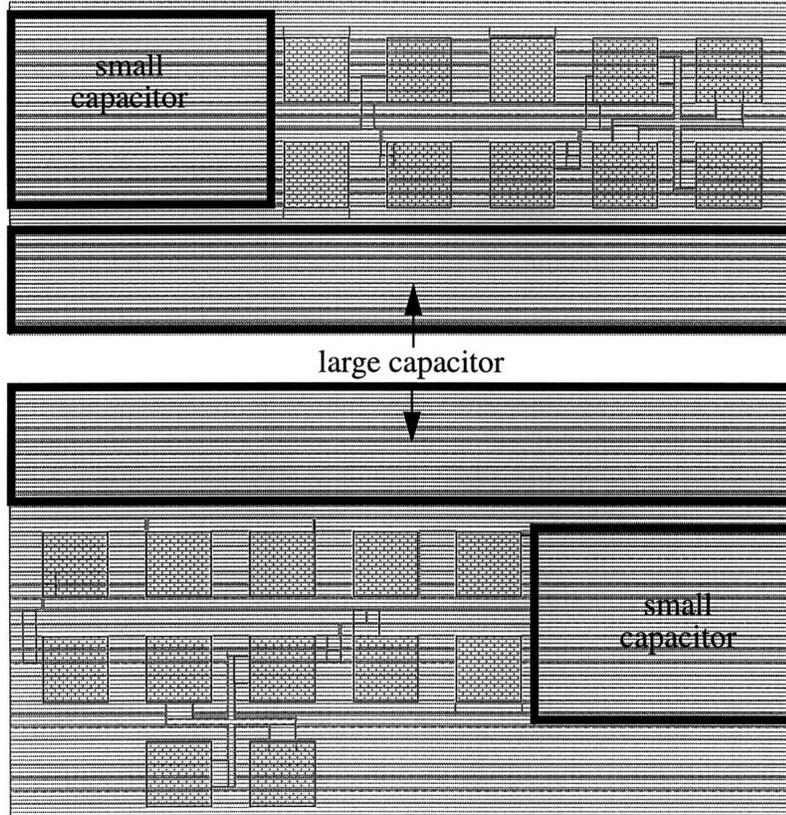


Figure 3.14: Area device probe layouts.

3.1.3 Die Layout

The LSI Logic die size was 18.11 mm x 18.11 mm, yielding 37 die per wafer. It was not recommended to have a die size which was too close to the maximum stepper field (20 mm x 20 mm). Furthermore, having too large a die would not yield at least 36 die per wafer as needed by the signal processing algorithms. Figure 3.15 shows a picture of the LSI Logic die. The names of the devices are as described in the previous subsections.

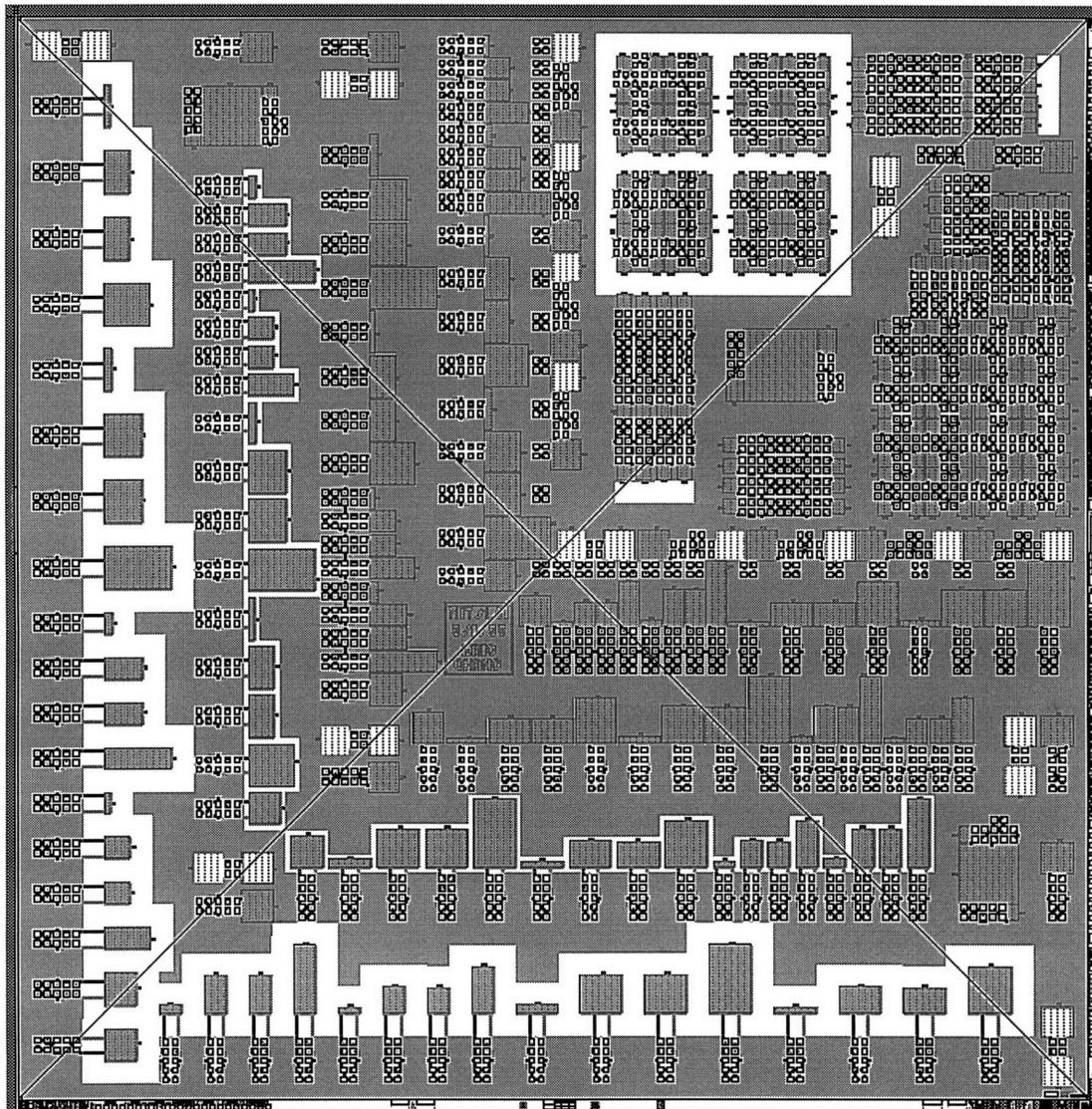


Figure 3.15: LSI Logic die layout.

3.1.4 Process Flow and Characterization

The LSI Logic statistical metrology wafers were fabricated in the Santa Clara fab facility. There were 24 p-type wafers in the lot. At various stages of the fabrication process, process measurements were performed such as SEM critical dimension measurements and optical oxide thickness measurements.

First, the wafers were field-implanted with boron so that the field-oxide will not deplete or invert and the substrate will be in accumulation when the capacitance bias is applied. This is only necessary for measuring the field-oxide blanket capacitor which has the Low capacitance probe connected to the substrate. After the implant, the wafers were annealed to repair any damage to the silicon. A thick TEOS (thickness equal to process field-oxide and ILD thicknesses combined) was then deposited on the silicon for the field-oxide. The field-oxide thickness was measured at five points per wafer for five wafers using the Prometrix 750 optical film thickness equipment. The five points/dies are shown in Figure 3.16. The wafers were chosen from wafers 1, 7, 13, 19, and 24 (wafers were sorted in increasing order).

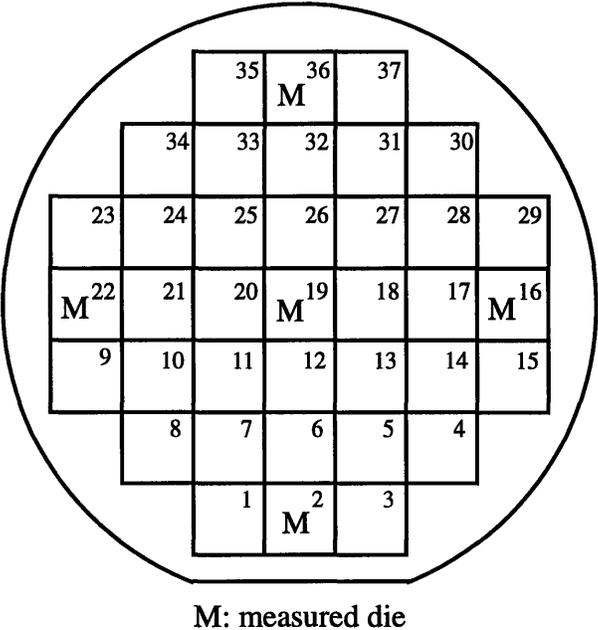


Figure 3.16: Five dies used for optical, SEM-cd, and profilometer measurements.

Next, AlCu was sputtered on the wafers. Patterning and etch was performed using the M1 reticle. SEM critical dimension measurements were done on wafers 5 and 20 for five points per wafer as shown in Figure 3.16. Profilometry measurements were then per-

formed to characterize the M1 thickness using the Tencor P2 system. These measurements were done for five points per wafer (Figure 3.16) for wafers 2, 13, and 23.

A thick TEOS was then deposited on the wafers for the ILD, and followed by CMP of the ILD down to a target CMP thickness. Following this, a layer of TEOS was redeposited over the ILD to make a final target ILD thickness of λ micron. The next step is to measure the ILD thickness using the Prometrix 750. This was done for three points per die for every die in wafers 13 and 21. The three points were the centers of the three Area capacitors with the 18.4 micron line width, located in the top right quad. The measurements were careful to place the optical beam on top of the metal lines using a spot size of about 4 micron x 4 micron.

After the Prometrix ILD measurement, vias were patterned and etched using the via 1 reticle. The vias were then filled with tungsten and CMP planarized before AlCu was resputtered for M2. After patterning and etching M2 using the M2 reticle, a thick passivation oxide was deposited to prevent accidental shorting of probe pins to the devices. Next, the passivation oxide was patterned and etched using the passivation oxide reticle. The wafers then undergo a final anneal to induce good contacts between the metal layers. Finally, the backside of the wafer was sputtered with aluminium to make the backside contact.

3.1.5 Capacitance Simulations

Batch two-dimensional capacitance simulations were performed using Raphael [10]. The simulations were run for various pitches and ILD thicknesses of the capacitors. In addition, simulations were also run for the connecting line structure using various ILD thicknesses.

Structural dimensions for the simulations were determined by process measurements, such as field-oxide thickness Prometrix measurements and M1 thickness Tencor measure-

ments. Since the field-oxide and M1 thickness variation was small, the mean of the measurements was used as a representative value.

The width range of the batch simulations was set to be $(\alpha - 0.6)$ micron to $(\alpha + 0.8)$ micron for the α micron line width, $(\alpha + 7.4)$ micron to $(\alpha + 8.8)$ micron for the $(\alpha + 8)$ micron line width, and 17.8 micron to 19.2 micron for the 18.4 micron line width. The spacing was derived by subtracting the line width from the pitch. The width steps were 0.02 micron for the α micron lines, and 0.05 micron for the $(\alpha + 0.8)$ micron lines. The ILD thickness range spanned $(\alpha - 0.6)$ micron to $(\alpha + 0.6)$ micron. The ILD thickness steps are 0.01 micron. For both the width and ILD thickness steps, the step size was increased at the extremes of the ranges.

3.1.6 Electrical Characterization

Capacitance and resistance measurements were carried out at LSI Logic using the Keithley S400UX parametric test system which controlled the Electro-Glass 2001 automatic prober. The Keithley system has a user interface program (Keithley Test Program (KTP)) which facilitates (though restricts) the writing of a C program to control the probing. This interface program allows the user to program individually the die and probe-site probing pattern (Wafer Definition Utility (WDU)), the order of measurements at each site (Keithley Interactive Tool (KITT)), and the definition of the measurement macros (Keithley User Library Tool (KULT)), then finally bring them together into a final program with the Keithley Test Program Builder (KTPB). After the probing, the output from the Keithley interface is an *outfile.kdf* file, which has the data stored in a hierarchical ascii format.

The WDU was programmed so that the probe-card stepped through all the probe-sites within the die in a snake-like fashion beginning from the top left probe-site in the die. After all the probe-sites were completed within the first die, this was repeated for all the dies in the wafer, and consequently everything was repeated for all the other wafers in the

lot. The die numbering was as previously shown in Figure 3.15. The wafers can be measured multiple times for a time-series analysis by running the same program.

The measurement order and probe-pin utilization was specified using KITT. Kelvin measurements were performed first, followed by van der Pauw measurements. Capacitance measurements were last because *metrocap.c*, the capacitance measurement macro, ends with the probe-pins not touching the pads so that parasitic capacitance measurements could be performed. It was thus more efficient to perform the capacitance measurements just before the prober had to step to another site.

metrocap.c was written using KULT because there were no existing measurement macros that accounted for parasitic measurements. Typically, the parasitic measurement is done while the probe-pins are not connected to the pads, then while the pins are connected to the pads the device capacitance is measured. The correct device capacitance is the parasitic capacitance subtracted from the measured device capacitance. However, due to the inflexibility of the interface, the stepping to each probe-site included contacting the pins to the pads. Instead of inefficiently disconnecting the pins from the pads, the parasitic measurement was performed after the device measurement in *metrocap.c*. *metrocap.c* uses a pre-defined *capg* macro which compensates for conductance errors during the capacitance measurement. The substrate (assigned pin 25) was grounded for all capacitance measurements except for the field-oxide blanket capacitor, when it was connected to the Low capacitance probe. The resistance measurements were performed using pre-defined macros, *res4* (Kelvin) and *rudp* (van der Pauw) which output Kelvin resistance and van der Pauw resistance respectively. A current of 50 mA was used for the Kelvin measurements while a current of -200 mA was used for the van der Pauw measurements. The van der Pauw current was negative in order to yield a positive voltage for the order of pads specified in the resistance algorithm.

3.1.7 Data Conversion

After the electrical probing, the Keithley output file (*outfile.kdf*) must be converted into ascii column format and binned into different files according to wafer number. This is achieved with a C program called *kthconv.c* which looks for end-of-wafer markers (<EOW>) and end-of-site markers (<EOS>), and formats and bins accordingly. A unix script, *sort_wafer*, then places each of these wafer files into its own directory which bears its own filename.

The next program, also written in unix, is called *runsplitup*. It calls a C program, *splitup.c* as well as moves files generated by *splitup.c* into new directories according to device type. For instance, the “R_” directory contains all resistors, and “C_” directory contains all L capacitors. *splitup.c* takes any one of the wafer files generated by *kthconv.c*, and splits the file into many smaller ones by device name. For example, all C_A01 devices are placed in a file called “C_A01”. *splitup.c* also generates twenty files with prefix “R_” to contain all the L, Block and Uni-edge resistors. The way the resistors are sorted into these files is shown in Table 3.10. There are also two files with prefix “T_” generated to contain the Area resistors which is also described in Table 3.10.

splitup.c also filters bad capacitor data into a *badcap* file, and appends factor levels and X-Y coordinates to the data. Since the prober does not have the device X-Y coordinates, the locations are supplied by a pre-written ascii file, *devxy2.txt*.

Resistor filename	Type	lw	ls	go
R_1HA	Kelvin	L	L	H
R_1HB	VDP	n/a	n/a	n/a
R_2HA	Kelvin	H	L	H
R_2HB	VDP	n/a	n/a	n/a

Table 3.10: Resistor files generated by *splitup.c*

Resistor filename	Type	lw	ls	go
R_3HA	Kelvin	L	H	H
R_3HB	VDP	n/a	n/a	n/a
R_4HA	Kelvin	H	H	H
R_4HB	VDP	n/a	n/a	n/a
R_5HA	Kelvin	C	C	H
R_5HB	VDP	n/a	n/a	n/a
R_1LA	Kelvin	L	L	L
R_1LB	VDP	n/a	n/a	n/a
R_2LA	Kelvin	H	L	L
R_2LB	VDP	n/a	n/a	n/a
R_3LA	Kelvin	L	H	L
R_3LB	VDP	n/a	n/a	n/a
R_4LA	Kelvin	H	H	L
R_4LB	VDP	n/a	n/a	n/a
R_5LA	Kelvin	C	C	L
R_5LB	VDP	n/a	n/a	n/a
T_CB	Kelvin	W/L	L	H/L
T_CC	VDP	n/a	n/a	n/a

Table 3.10: Resistor files generated by *splitup.c*

A C program, *calc_cd.c* then calculates critical dimension while filtering any bad resistance data. The Kelvins (R_??A) and van der Pauws (R_??B) are read by *calc_cd.c* to calculate the critical dimensions. *calc_cd.c* then generates a file called “R_??C” which contains the calculated critical dimensions. Likewise, the Area Kelvins (T_CB?) and Area van der Pauws (T_CC?) are also used by *calc_cd.c* to calculate critical dimensions which are output in “T_CD?”.

Several routines have been written in the SPLUS S Language to perform data reading (into SPLUS) and critical dimension and ILD thickness interpolations. These routines are called in batch mode by invoking the command, “splus BATCH batch-file log-file”. The

batch-files are *metroread.sim.bat*, *metroread.bat*, *metrointerp.cd.bat*, *metrointerp.ild.bat*, *metroappend.bat*, and *metrofilter.bat*. *metroread.sim.bat* is only run once to read in the simulation data. The other batch-files must be run once for each wafer. *metroread.bat* is used to read in the wafer data. *metrointerp.cd.bat* and *metrointerp.ild.bat* performs the CD and ILD thickness interpolations respectively. *metroappend.bat* generates a big SPLUS data frame which contains the ILD thickness, critical dimension, capacitance value, factor identifiers, and X-Y locations for all the measured capacitors in the wafer. Finally, *metrofilter.bat* filters out any bad ILD thickness data which may have been generated.

3.2 Experimental Results

This section presents some ILD thickness data extracted from the LSI Logic experiment. Note that the graph values presented have been arbitrarily normalized for company proprietary reasons. Due to time constraints, only data for one die is presented in this thesis.

There is considerable die-scale variation as can be seen in the histogram in Figure 3.17. This histogram was generated for all the capacitor test structures within one particular die. Figures 3.18 to 3.21 show die-maps of the capacitor structures sorted by type (i.e. L, Uni-edge, Block, and Area).

If the ILD thickness for one particular structure is die-mapped, one can also observe the die location dependence of the die-scale variation. This is illustrated in Figures 3.22 and 3.23 which plot the die-map for the vertical and horizontal centerpoint structures within one particular die. The die location dependence is again shown in Figure 3.24 which presents the die-map for the ILD blanket capacitor.

Finally, Figure 3.25 plots the die-map for the field-oxide blanket capacitor. Note that the range of thickness variation is considerably smaller than that of the ILD thickness capacitors because field-oxide thickness variation is usually well controlled.

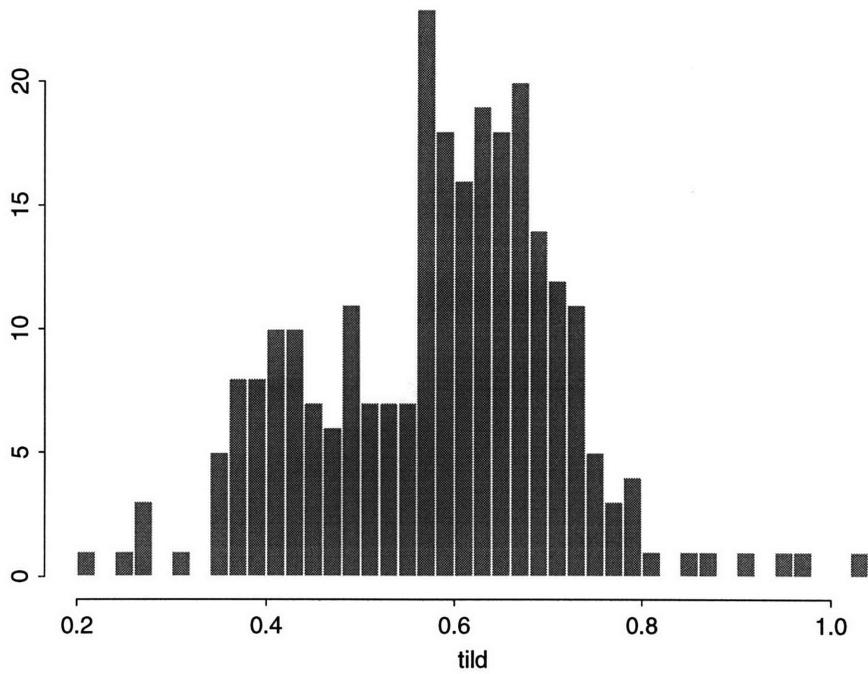


Figure 3.17: Histogram showing the ILD thickness variation in a particular die.

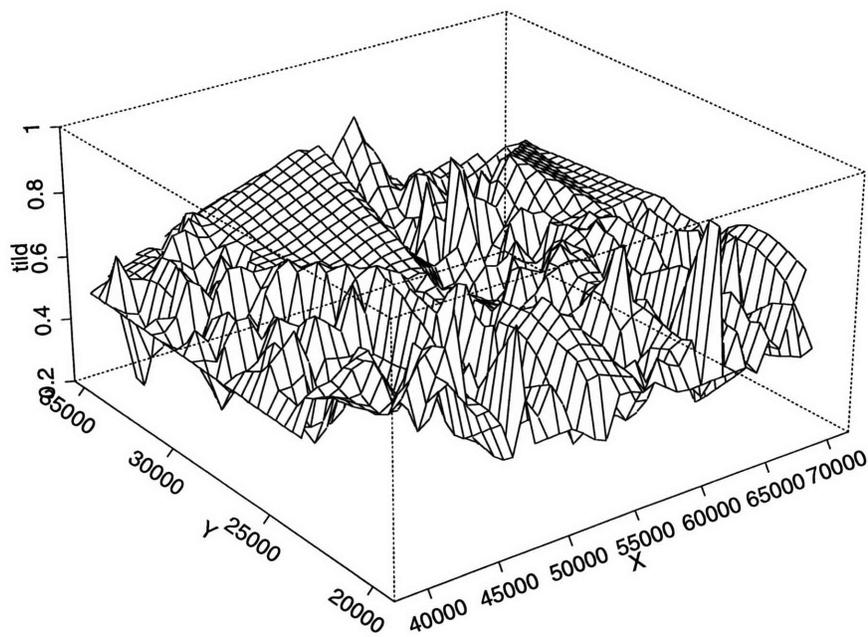


Figure 3.18: L capacitor ILD thickness in a particular die.

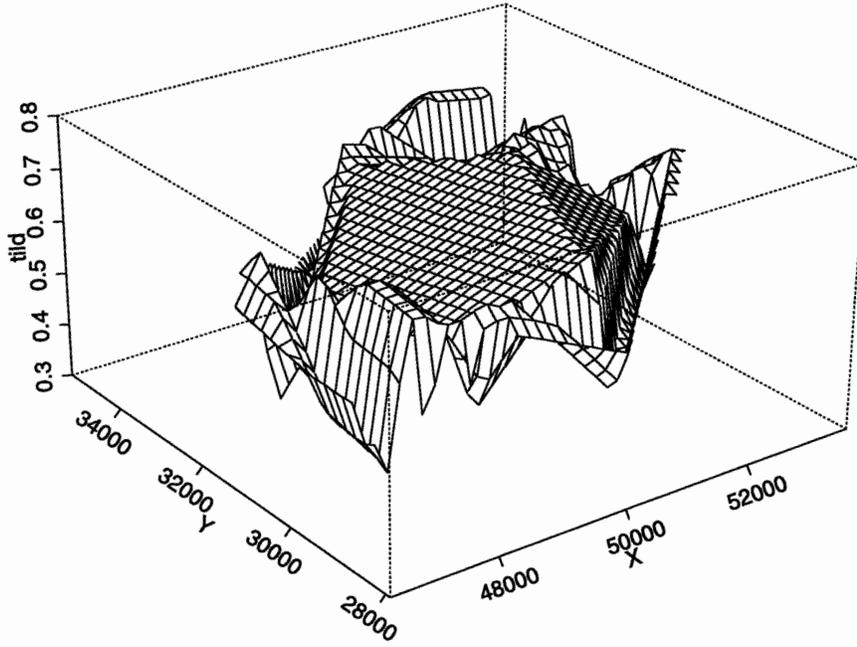


Figure 3.19: Uni-edge capacitor ILD thickness in a particular die.

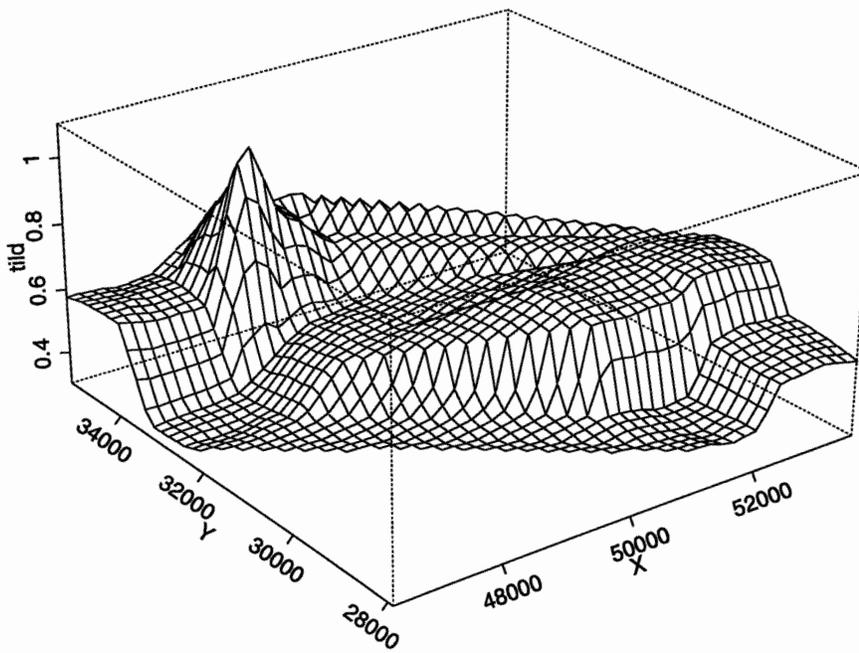


Figure 3.20: Block capacitor ILD thickness in a particular die.

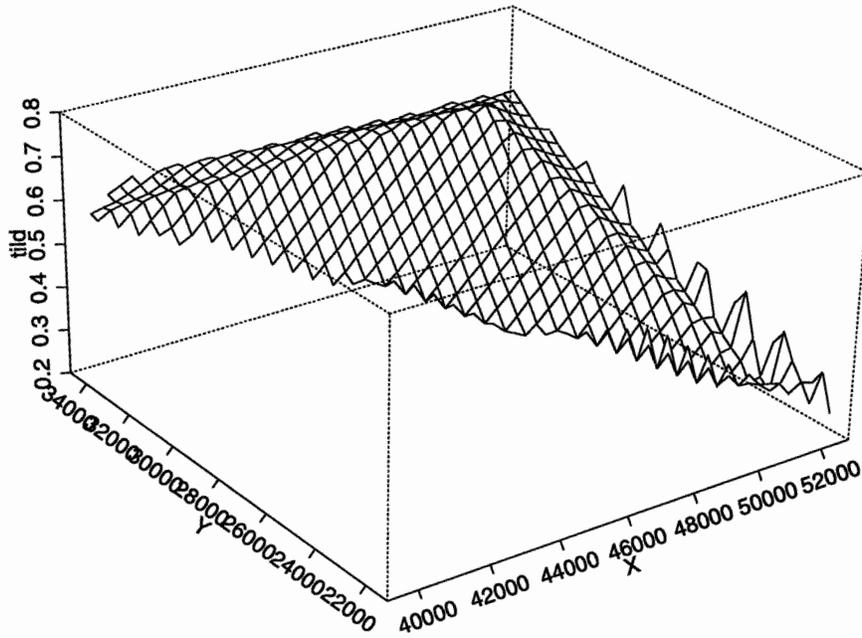


Figure 3.21: Area capacitor ILD thickness in a particular die.

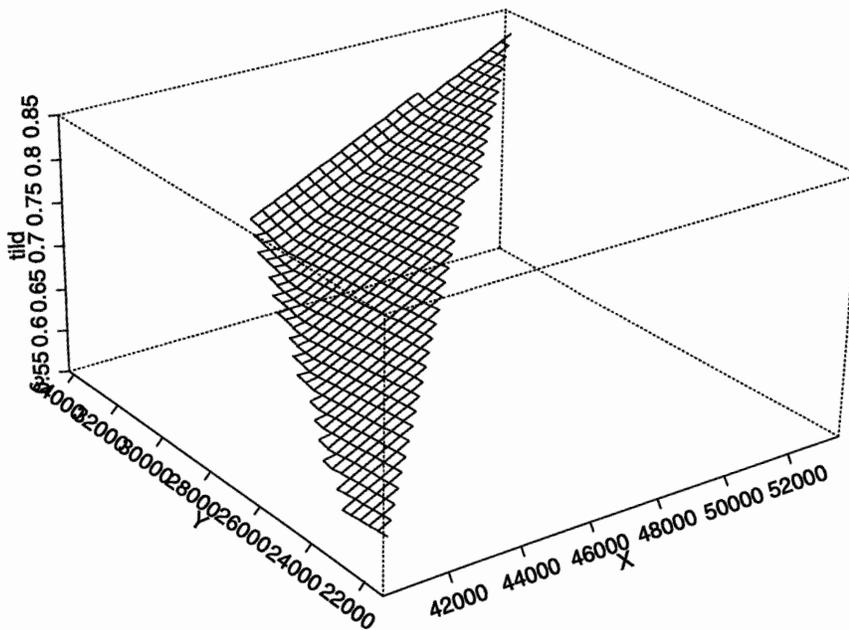


Figure 3.22: Vertical centerpoint ("5H") ILD thickness in a particular die.

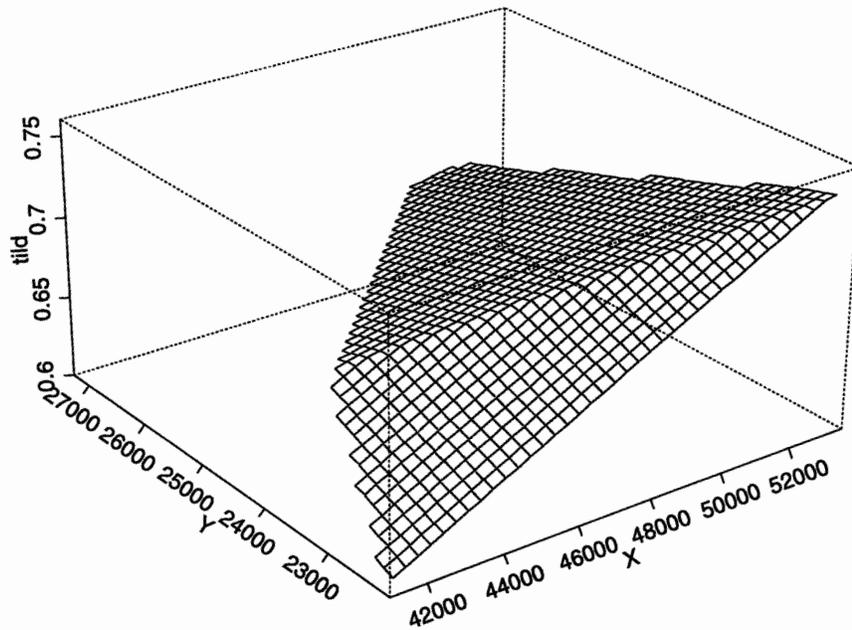


Figure 3.23: Horizontal centerpoint capacitor (“5L”) ILD thickness in a particular die.

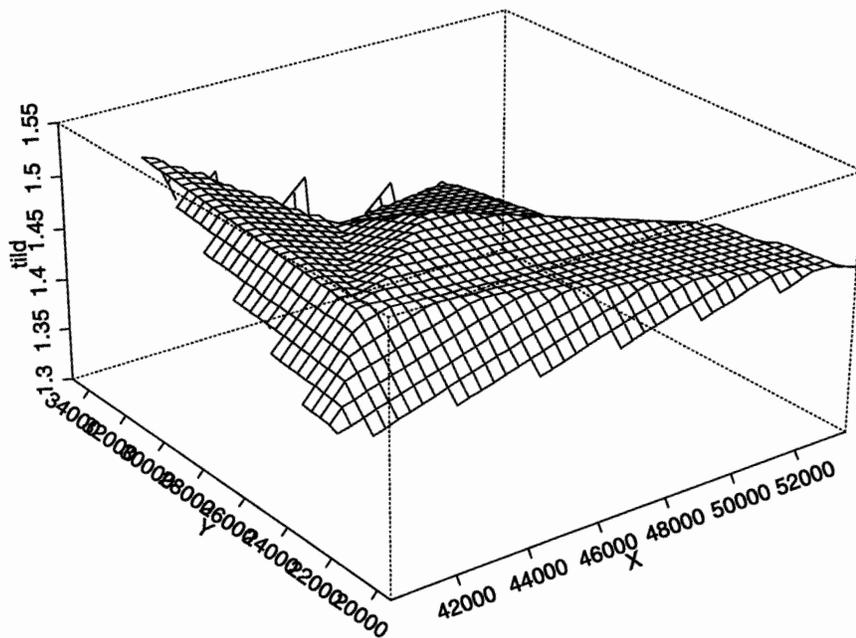


Figure 3.24: ILD blanket capacitor ILD thickness in a particular die.

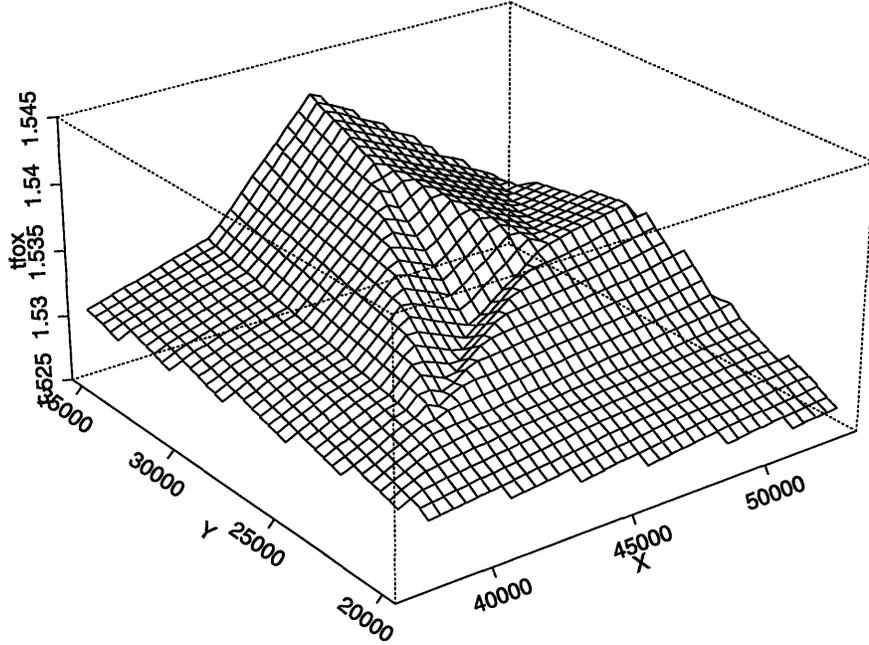


Figure 3.25: Field-oxide blanket capacitor field-oxide thickness in a particular die.

3.3 Experimental Oversights

Some oversights in the LSI Logic experiment are presented in this section. It is the hope of this author that the documentation of these oversights will help increase the effectiveness of future experiments.

3.3.1 Opposite Orientation of L Capacitors

One advantage of the L die design is that SEM cross-sectional measurements can be easily performed since the capacitors are lined up in “L”s. Unfortunately, the capacitor orientations was inadvertently flipped for the “L”s, hence making the L die design lose its easy SEM capability. However, since L capacitors are more densely packed than previous die designs [5, 6], it is still easier to generate SEM cross-sections for the LSI Logic test chip.

3.3.2 Pad for Measuring Pad Capacitance

In the initial stages of designing the experiment, it was assumed that the Low capacitance probe was connected to the substrate as well as to M1. Therefore, the pad capacitance was significant enough to warrant allocating an extra pad for measuring the pad capacitance. The two capacitor pads as well as this extra pad were also designed as a specialized pad [3]. The specialized pad minimizes the pad capacitance variation due to ILD thickness variation. Nevertheless, the effort was wasted because the Low capacitance probe is no longer connected to the substrate. Future experiments can utilize the extra pad as well as lay out dummy-lines more easily because there is no need for the specialized pads.

3.3.3 Unnecessary Row of van der Pauws

When designing the layout, it was assumed that the van der Pauw's sheet resistance will be interpolated for each of the Kelvins when calculating critical dimensions for the Kelvins. These critical dimensions can then be interpolated for the capacitor critical dimensions. This is why an extra row of van der Pauws was placed next to the inside/smallest L so that interpolation can be done more accurately. However, it was decided later that since the Kelvins are rather close to the van der Pauws, the error caused by not interpolating the sheet resistance can be neglected.

There are two outcomes from this oversight: first, some area was wasted on the die, and second, the path for stepping each probe-site became less efficient. This was because a stepping program had already been defined, and was too much effort to change.

3.3.4 Wrong Orientation of Uni-edge Capacitors

The Uni-edge capacitors were originally conceived as a replacement for the L capacitors because of their closeness to the Block capacitors (e.g. neighborhood distance defined

on one edge instead of all four). Therefore, the Uni-edge and the Block capacitor data will be compared to see if they correlate. Some of these correlations include the exposed sides, pitch, and neighborhood distance factors.

The mistake was that the Uni-edge capacitors had different orientations for the capacitors with different exposed sides. In other words, capacitors BA01-BA04, BA09-BA12, had orientation “5H” while capacitors BA05-BA08, BA13-BA16 have orientation “5L”. This is in contrast to the Block capacitors which only have one orientation “5H”. Thus, if orientation is a significant factor, then capacitors BA05-BA08, BA13-BA16 cannot be used to correlate with the Block capacitors.

3.3.5 Incorrect Neighborhood Distances

The neighborhood distances are defined to be either β , 40, 120, 400 micron. Unfortunately, when laying out a large chip, sometimes some instances are accidentally moved and thus they might have different neighborhood distances. The accidental moving occurs when one is not careful enough to unselect all instances when starting work on new parts of the die. Remember that since this is a test-structure chip, there is no available “neighborhood distance” rule-checker program and all checks must be made by hand. Some erroneous neighborhood distances are shown in Table 3.11.

Capacitor Name	Implemented nd	Correct nd
BB14	7.2	40
BB16	5.2	40
BB13	62	40
BB15	62	40
AA2	62	40
AA3	62	40

Table 3.11: Capacitors with incorrect neighborhood distances

Capacitor Name	Implemented nd	Correct nd
AA4	62	40
AB1	62	40
AB2	62	40
AB3	62	40
AB4	62	40

Table 3.11: Capacitors with incorrect neighborhood distances

3.3.6 “Disconnecting” Capacitor Connectors

Another common error when laying out a large number of test structures is that some layers do not connect when they should. This is due to accidental moving of instances and structures. Design rule checkers only catch these errors when the misconnection has a spacing smaller than that of the minimum allowed spacing. Electrical rule checkers can detect these errors, however, it is not an easy task to program the ERC to perform the detections. Capacitors F_CB1, F_CB6, and G_O10 have connectors which do not connect correctly, hence these devices do not work and must be discarded.

Chapter 4

Conclusion

4.1 Summary of Results

This thesis has described a framework for performing statistical metrology of ILD thickness variation on CMP processes. In addition, it has presented an implementation of the framework on a CMP process at LSI Logic.

The framework that is presented includes experimental details spanning test structure design, die-layout design, process characterization, simulations, electrical characterization, data conversion and organization. This thesis tries to expose the intricacies involved in designing and implementing a successful experiment for performing statistical metrology of ILD thickness variation.

Over a duration of six months at LSI Logic, the framework described in Chapter 2 was designed, modified, and implemented. The work at LSI Logic included design and layout of the test reticle, fabrication of the wafers, electrical characterization of the wafers, capacitance simulations, and building and applying the conversion program infrastructure to yield the desired ILD thickness values. The above mentioned effort was successfully performed, and yielded a large amount of ILD thickness data which will be used for statistical modeling and process control.

To understand the scope of the experiment, here are some statistics of the experiment. The experiment at LSI involved over 300 unique capacitors per die, or over 300 ILD thickness data points per die. There were over 800 devices (capacitors and resistors) per die. The 500 or so resistors yielded about 300 critical dimension data points per die. Therefore, the experiment needed over 250 probing sites per die for the 37 die per wafer. There was a total of eight factors varied for the different capacitors, in addition to the device X-

Y coordinates. The sheer magnitude of these numbers shows how generous statistical metrology can be in generating data for statistical analysis and modeling. This is a major advantage which sets apart statistical metrology from other metrology methods, and presents statistical metrology as the method of choice for understanding the details of spatial and pattern dependent variation.

4.2 Future Work

The LSI Logic work succeeded in obtaining the ILD thickness values using statistical metrology. The data thus gathered for a state of the art industrial process will be the basis for continuing research into statistical metrology and the analysis of sources of variation in CMP. Such analysis will be possible using analysis programs such as VarDAP and VarNOVA currently under development at MIT.

In addition, verification of the ILD thickness data must still be performed via SEM cross-sections. Some verification has been done using the Prometrix optical data measurements, however, that was only for wide metal lines.

Future experiments should also benefit from the results of the LSI Logic experiment. The advanced test structures in this experiment can be used as candidate test structures, and can stimulate new ideas for next generation test structures and layouts. If the advanced test structures are successful, in future experiments, they should replace the older structures, while more advanced test structures can be evaluated. If they are not successful, future experiments should try to build on the mistakes of the current advanced test structures to yield better test structures.

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