Investigating Packaging Effects on Bandgap References

by

Ravi Palakodety

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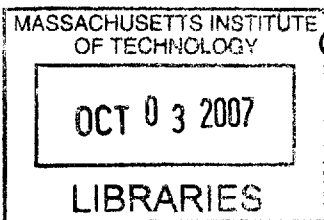
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Abstract

This thesis investigates packaging effects on precision bandgap voltage references used in LTC switching regulators. Packaging stress causes a mean offset and room temperature distribution widening of the bandgap reference output voltage, as well as inconsistent temperature characteristics. Bandgap references with and without a proprietary stress-relief mechanism were compared to determine the impact of packaging stress on reference performance. References without stress-relief showed a mean offset of -2.3mV and spread of 10mV, while references with stress-relief showed a mean offset of -2.0mV and spread of 3.6mV. References with stress relief exhibited more consistent temperature coefficients than references without stress relief. A test chip was fabricated to allow measurement of V_{BE} and ΔV_{BE} within the bandgap reference. Parts with stress-relief showed tighter V_{BE} and ΔV_{BE} distributions, as well as more favorable temperature characteristics. The experiments in this thesis show that stress-relief is effective at improving bandgap reference performance.

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Finally, I would like to thank my parents for their support throughout my life. In all aspects of life, they have ensured that I had the right aims and was capable of eventually achieving those goals.

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Chapter 1

Introduction

1.1 Overview

This M.Eng thesis explores packaging effects on a high performance bandgap reference used in a switching regulator produced by Linear Technologies (LTC). In recent years, competition has dictated that these references have an accuracy of $\pm 0.5\%$ over all operating conditions. For a reference voltage of 0.6V, the total error budget is ± 3mV. Since LTC requires some margin on this specification, the actual error budget is about ± 2mV, broken down into ± 1mV of room-temperature variation and ± 1mV of variation over the specified temperature range.

In past years, bandgap references on board LTC switching regulators were only trimmed during wafer-sort testing. The references were trimmed to a target voltage within a tight distribution and then assembled in plastic packages. Post-package testing showed a mean offset and considerable distribution widening. With the advent of stricter bandgap specifications, the stresses caused by plastic packaging warranted a second round of trimming and testing after packaging. In an effort to remove the wafer sort trim-and-test procedure, LTC has developed a proprietary stress relief mechanism to alleviate package-induced stress. This thesis characterizes the effectiveness of this stress relief mechanism and investigates the effects of stress on the fundamental NPN

transistors in the bandgap cell.

By characterizing the effectiveness of the stress relief, LTC may be able to eliminate the wafer-sort trim-and-test procedure. With very small die, the number of dice on a wafer can be very large. Since the yield is often greater than 95 percent, the sort time can be in excess of eight hours per wafer. If trimming is no longer necessary at wafer-sort, then testing can be done on a statistical sampling basis, increasing throughput and reducing cost. If the stress relief mechanism is effective, the untrimmed packaged parts will not experience any further distribution widening due to packaging stress, reducing the necessary number of post-package trim bits. More importantly, if the stress relief mechanism is effective, the untrimmed references will have consistent temperature characteristics. By using a single target voltage for the post-package trim, all of the references will be be forced to operate with minimum temperature coefficient. Without the stress relief mechanism, packaging stress might cause the untrimmed references to exhibit random variations in temperature characteristics. Since the post-package trim would have a single target voltage, trimming might result in references operating with a non-optimal temperature coefficient. By investigating the effects of stress on the NPN transistors within the bandgap cell, designers will be able to better compensate for packaging stress in their bandgap circuits. If the stress relief mechanism is effective, it can be added to many of LTC's products to tighten specifications and give these parts a competitive advantage.

1.2   Background

The bandgap voltage reference plays a significant role in switching regulators. Figure 1-1 shows a conceptual diagram of a voltage-mode buck converter.

A buck regulator converts an unregulated high voltage V_{IN} to a regulated lower voltage V_{OUT}. Switching regulators accomplish this by modulating the duty cycle of a switch. When the switch is closed, V_{IN} appears at the V_{SW}. When the switch

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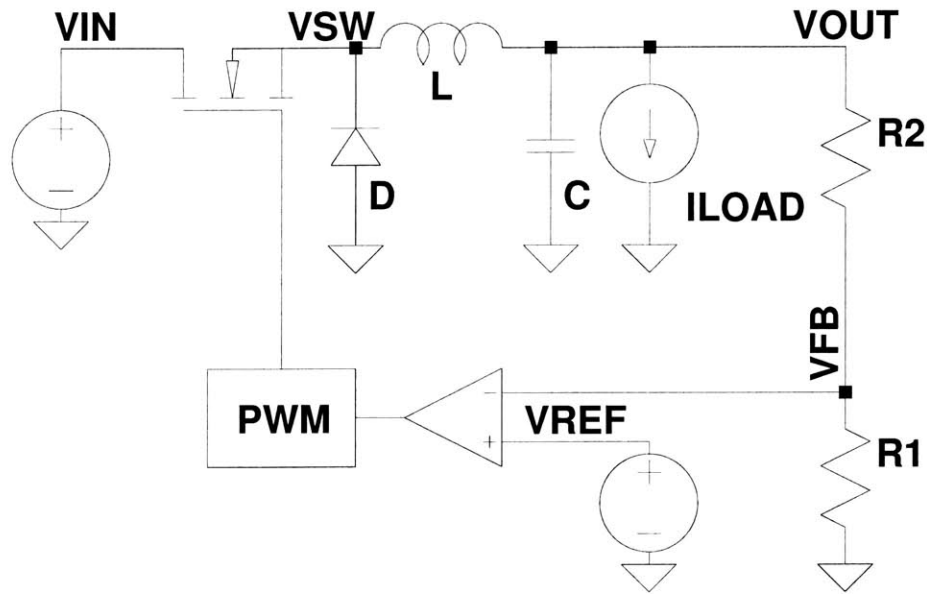
Figure 1-1: Buck Converter

is opened, the current through the inductor must remain continuous, so current circulates to turn on the diode and clamp V_{SW} to approximately -0.7V. The chopped waveform at V_{SW} is then low-pass filtered, resulting in an approximately DC voltage at V_{OUT}. This DC voltage is equal to the product of V_{IN} and the duty cycle of the chopped waveform at V_{SW}.

To regulate a certain output voltage, a buck converter must control the duty cycle of the switch. This is accomplished by using an op-amp to compare a portion of V_{OUT}, designated V_{FB}, to a voltage reference. The op-amp output is sent to a pulse-width-modulation (PWM) block that sets the duty cycle of the switch. When V_{OUT} (and therefore V_{FB}) is too high, the duty cycle is decreased, causing V_{OUT} and V_{FB} to drop. When V_{OUT} is too low, the duty cycle is increased, causing V_{OUT} to rise. Steady-state is achieved with V_{FB} equal to V_{REF}. Assuming an ideal op-amp with zero offset voltage and zero bias current over all temperatures, V_{OUT} will equal $V_{REF}(1 + R_2/R_1)$. Assuming perfect resistor matching between R_1 and R_2 over all temperatures, the accuracy of V_{OUT} equals the accuracy of the voltage reference.

A temperature-independent voltage reference is needed to ensure correct performance over a desired operating range. Bandgap voltage references are well suited for low voltage operation and are the reference of choice for buck converters. Bandgaps have a certain "magic" voltage for which they have minimum temperature dependence. Careful circuit design, layout, and trimming schemes are necessary to ensure that every bandgap is operating exactly at this magic voltage. Packaging stress is one of the major obstacles in the path of precision design - this thesis characterizes the effectiveness of stress relief in fixing this problem.

In this thesis, the room temperature distributions for the precision bandgap onboard an LTC switcher are compared with and without stress relief. The temperature characteristics of the bandgap are then compared with and without stress relief. After assessing the effectiveness of the stress relief mechanism, the changes to the fundamental characteristics of the NPNs within the same bandgap cell are investigated. By bonding out the terminals of the key transistors, and examining their properties, this thesis examines how the assembly process changes NPN transistor characteristics.

1.3 Organization

Chapter 2 describes the theory and operation of bandgap references. The temperature dependence of bipolar transistors is developed, followed by an explanation of first-order references. A simplified version of the curvature-corrected reference used in these experiments is described. Chapter 3 introduces the causes of physical stresses in plastic packages and the electrical effects of packaging stress. Chapter 4 presents the experimental setup and results for tests on the operating bandgap reference. Chapter 5 presents the experimental setup and results for tests on the fundamental NPN transistor characteristics within the bandgap cell. Finally, Chapter 6 presents conclusions and topics for future research.

Chapter 2

Theory of Bandgap References

2.1 Overview

Bandgap references create a temperature stable output voltage by temperature compensating a forward-biased diode. The temperature coefficient of the diode voltage (designated V_{BE}) is approximately linear with a slope of about -2mV/°C. A correction voltage V_C is added to V_{BE} to create an output V_{REF} with minimum temperature dependence. At room temperature, the optimum V_{REF} is approximately equal to the bandgap voltage of silicon extrapolated to 0 Kelvin.

In the following sections, the temperature dependence of the I_C-V_{BE} relation of a bipolar transistor will be developed in detail. A solid understanding of this theory is necessary when assessing the impact of packaging stress on bandgap references. An explanation of first-order voltage references will be given. Finally, a simplified version of the bandgap reference under test will be analyzed.

2.2 Temperature Dependence of I_C-V_{BE} Relation

The V_{BE} vs T relation is roughly linear as shown in Figure 2-1. The V_{BE} temperature dependence is affected by many factors such as the temperature dependence of

the bandgap voltage of silicon (E_G), the temperature dependence of mobility (μ), the temperature dependence of the intrinsic carrier concentration (n_i), and the temperature dependence of the current flowing through the transistor (I_C). Section 2.2.1 contains the detailed derivation of the V_{BE} vs T relation, with the key result presented as Equation 2.1.

$$
\begin{aligned}
V_{BE}\left(T\right) &= E_G\left(T\right) - \left(\frac{T}{T_r}\right) E_G\left(T_r\right) + \left(\frac{T}{T_r}\right) V_{BE}\left(T_r\right) \\
&\quad - \eta\left(\frac{kT}{q}\right) \ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right) \ln\left(\frac{I_C\left(T\right)}{I_C\left(T_r\right)}\right)
\end{aligned}
\tag{2.1}
$$

This equation expresses V_{BE} at an arbitrary temperature T as a function of V_{BE} at a reference temperature ($V_{BE}(T_r)$), the collector currents at T and T_r ($I_C(T)$ and $I_C(T_r)$), the bandgap energy of silicon at temperature T ($E_G(T)$), and the curvature factor (η). The curvature factor η depends on the temperature dependence of n_i and mobility μ. Important to note is that some of the parameters that appear in this temperature dependence, such as E_G and η, could be affected by packaging stress.

2.2.1 Derivation

This analysis follows the derivations given by Tsividis[1], starting with Equation 2.2.

$$
I_C\left(T\right) = I_S\left(T\right) \exp\left(\frac{qV_{BE}\left(T\right)}{kT}\right)
\tag{2.2}
$$

I_C is the collector current, I_S is the saturation current, k is Boltzmann's Constant, T is the absolute Kelvin temperature, and q is the charge of an electron. The saturation current I_S is given by Equation 2.3.

$$
I_S\left(T\right) = \frac{qAn_i^2\left(T\right)D\left(T\right)}{N_B}
\tag{2.3}
$$

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VBE vs Temperature
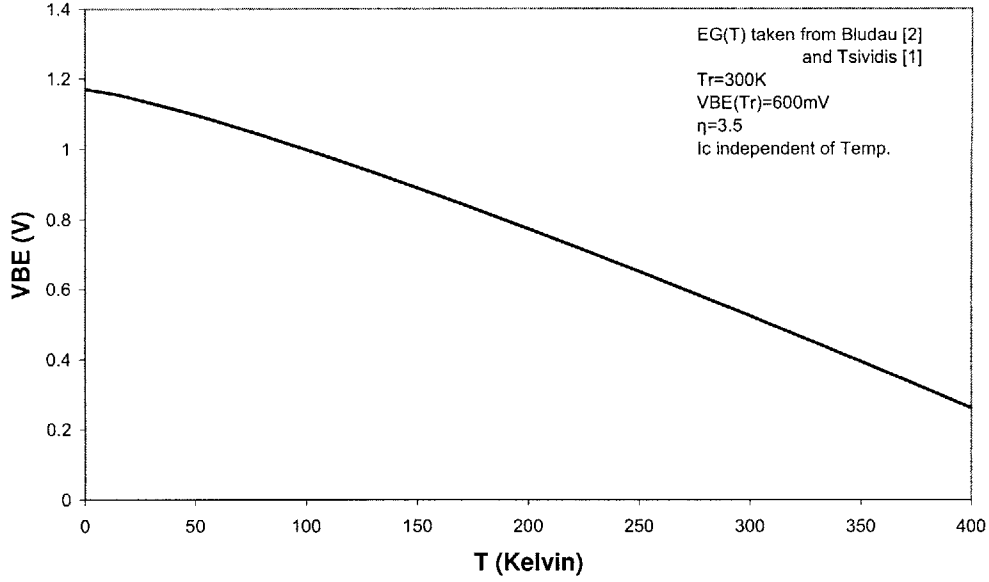
Figure 2-1: V_{BE} Temperature Dependence - Derived from Equation 2.1

A is the base-emitter junction area, n_i is the intrinsic carrier concentration, D is the effective minority carrier diffusion constant in the base, and N_B is the Gummel number, the total number of impurities per unit area in the base. n_i^2 is given by Equation 2.4

$$n_i^2 = BT^3 \exp\left[\frac{-qE_G(T)}{kT}\right] \tag{2.4}$$

E_G is the bandgap energy of silicon at temperature T and B is an empirical processing constant. The effective diffusion constant can be expressed in terms of mobility using the Einstein relation.

$$\frac{D}{\mu} = \frac{kT}{q} \tag{2.5}$$

$$\mu = CT^{-n} \tag{2.6}$$

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μ is the effective mobility and is further expressed in terms of processing constants C and n. This allows us to express I_S as Equation 2.7, where η replaces $(4 - n)$.

$$I_S(T) = \frac{ABCkT^{(4-n)} \exp\left[\frac{-qE_G(T)}{kT}\right]}{N_B} = \frac{ABCkT^{\eta} \exp\left[\frac{-qE_G(T)}{kT}\right]}{N_B} \tag{2.7}$$

We derive an expression for $V_{BE}(T)$ in terms of $V_{BE}(T_r)$, taken at a reference temperature (usually room temperature). Dividing $I_C(T)$ by $I_C(T_r)$, we obtain Equation 2.8.

$$V_{BE}(T) = \left(\frac{T}{T_r}\right)\left\{V_{BE}(T_r) + \left(\frac{kT_r}{q}\right)\ln\left[\frac{I_s(T_r)}{I_s(T)}\frac{I_C(T)}{I_C(T_r)}\right]\right\} \tag{2.8}$$

Further simplification using Equation 2.7 eventually yields Equation 2.9.

$$
\begin{aligned}
V_{BE}(T) &= E_G(T) - \left(\frac{T}{T_r}\right)E_G(T_r) + \left(\frac{T}{T_r}\right)V_{BE}(T_r) \\
&\quad - \eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right)\ln\left(\frac{I_C(T)}{I_C(T_r)}\right)
\end{aligned} \tag{2.9}
$$

At temperatures above room temperature, the E_G vs T curve is roughly linear. This allows for the following simplification

$$E_G(T) - \left(\frac{T}{T_r}\right)E_G(T_r) = E_{G0r} - \left(\frac{T}{T_r}\right)E_{G0r} \tag{2.10}$$

$$
\begin{aligned}
V_{BE}(T) &= E_{G0r} - \left(\frac{T}{T_r}\right)E_{G0r} + \left(\frac{T}{T_r}\right)V_{BE}(T_r) \\
&\quad - \eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right)\ln\left(\frac{I_C(T)}{I_C(T_r)}\right)
\end{aligned} \tag{2.11}
$$

E_{G0r} is the bandgap voltage extrapolated to 0K using a line tangent to the $E_G(T)$ curve at T_r. At temperatures below room temperature, this equation will not be accurate due to the parabolic temperature dependence of E_G at lower temperatures.

2.2.2 Details on Processing Parameters

The derivations above presented many process parameters and expressions describing their behavior; some of these parameters warrant further scrutiny. This section takes a closer look at the parameters E_G and μ.

The above derivation mentions the bandgap energy of silicon at temperature T, given as $E_G(T)$, and the bandgap energy of silicon extrapolated to 0K using a straight line, given as E_{G0r}. In the early 1970's, the $E_G(T)$ curve for unstressed, intrinsic silicon was found by Bludau, et al[2] using wavelength-modulation spectroscopy, and is given below.
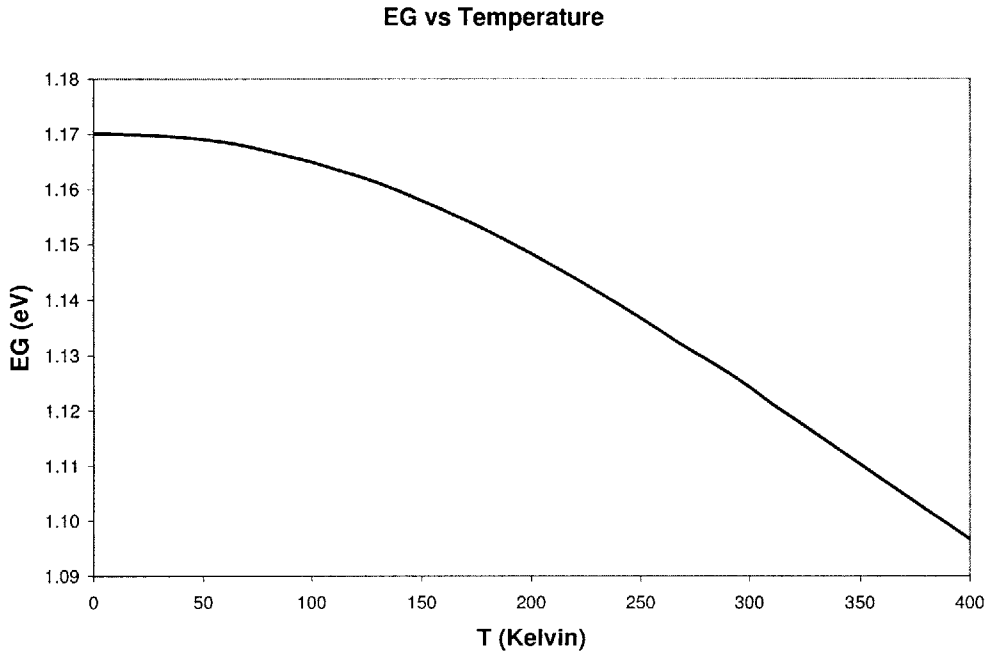
EG vs Temperature

Figure 2-2: E_G Temperature Dependence - Derived from Tsividis[1] and Bludau[2]

Tsividis[1] chooses the approximation that the $E_G(T)$ curve is linear at temperatures above 300K - this thesis also adopts that approximation. The subscript r in E_{G0r} is to remind the reader that the value of E_{G0r} depends on the temperature T_r where the extrapolation line is set tangent to the $E_G(T)$ curve. Using a lower value of T_r will lead to an inaccurate low value in the extrapolated E_{G0r} as the nonlinearity

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in $E_G(T)$ plays a larger role in the V_{BE} expression. Using the data for unstressed, intrinsic silicon, the extrapolated E_{G0r} from $T_r = 300\text{K}$ is 1.205V. Using $T_r = 273\text{K}$ yields an extrapolated E_{G0r} of 1.201V. Finally, as will be shown in the next section, the "magic" voltage of a first-order bandgap reference, defined as the voltage where the bandgap has 0 TC at T_r, is expressed in terms of E_{G0r}, not $E_G(0)$. The "magic" voltage depends on the bandgap voltage of silicon extrapolated to 0K, not the actual bandgap voltage at 0K. As will be explained in Chapter 3, stress can modify the bandgap energy of silicon. One of the experiments in this thesis compares the value of E_{G0r} for parts with and without stress relief.

The mobility dependence on temperature, given as $\mu(T)$, is another process parameter that deserves a second look. The value of the mobility is determined by the various scattering mechanisms present in silicon. These mechanisms cause free electrons and holes to lose their velocity, decreasing the mobility. The dominant scattering mechanism at higher temperatures is lattice scattering. As temperature increases, the thermal vibration of atoms in the crystal lattice disrupts the periodicity of the lattice, impeding the motion of the free electrons and holes. This mechanism causes the mobility to decrease at higher temperatures.[4]

Lattice scattering dominates at higher temperatures and accounts for the CT^{-n} behavior assumed in the above derivation. As explained in Chapter 3, stress can break the periodicity of the crystal lattice. If this causes the exponent in the μ vs T relation to change, the value of η will change. One of the experiments in this thesis compares the value of η for parts with and without stress relief.

2.3 First-Order V_{BE} Temperature Compensation

First-order references add a PTAT correction voltage V_C to V_{BE}, creating a V_{REF} with low temperature dependence. V_C is chosen such that at some reference temperature T_r, the sum of V_{BE} and V_C has zero temperature dependence, or an incremental slope of 0. This reference temperature is usually chosen as room temperature, and value of

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V_{REF} at the reference temperature is called the "magic" voltage.

To determine the appropriate correction voltage, we first perform a Taylor expansion of V_{BE}, around T_r, resulting in Equation 2.12.[1]

$$V_{BE}(T) = V_r + \gamma_r T + f_r(T) \tag{2.12}$$

$$V_r = E_{G0r} + (\eta - \theta_r)\left(\frac{kT_r}{q}\right) \tag{2.13}$$

$$\theta_r = \left.\frac{I_C'(T)}{I_C/T}\right|_{T=T_r} \tag{2.14}$$

$$\gamma_r = V_{BE}'(T) = -\left[\frac{V_r - V_{BE}(T_r)}{T_r}\right] \tag{2.15}$$

$$
\begin{aligned}
f_r(T) =\ & E_G(T) - E_{G0r} + \frac{T}{T_r}[E_{G0r} - E_G(T_r)] \\
& - (\eta - \theta_r)\left(\frac{kT_r}{q}\right) + (\eta - \theta_r)\left(\frac{kT}{q}\right) \\
& - \eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right)\ln\left[\frac{I_C(T)}{I_C(T_r)}\right]
\end{aligned}
\tag{2.16}
$$

To perform first order compensation, we choose the PTAT correction voltage such that its slope is equal and opposite to γ_r. This cancels the linear term in the Taylor expansion, leaving only the higher order terms designated $f_r(T)$. Since these expressions were derived by a Taylor expansion about T_r, f_r and its derivatives equal 0 at T_r. This means that V_{REF} has 0 temperature coefficient at T_R. A typical temperature characteristic for a first order reference is shown in Figure 2-3.

Common practice is to bias V_{BE} with a PTAT current, derived off the PTAT correction voltage generated. This gives θ_r as 1, and reduces the curvature in V_{BE} by one unit. In practice, the correction voltage is chosen by increasing the value of V_C until $V_{REF} = V_R$.

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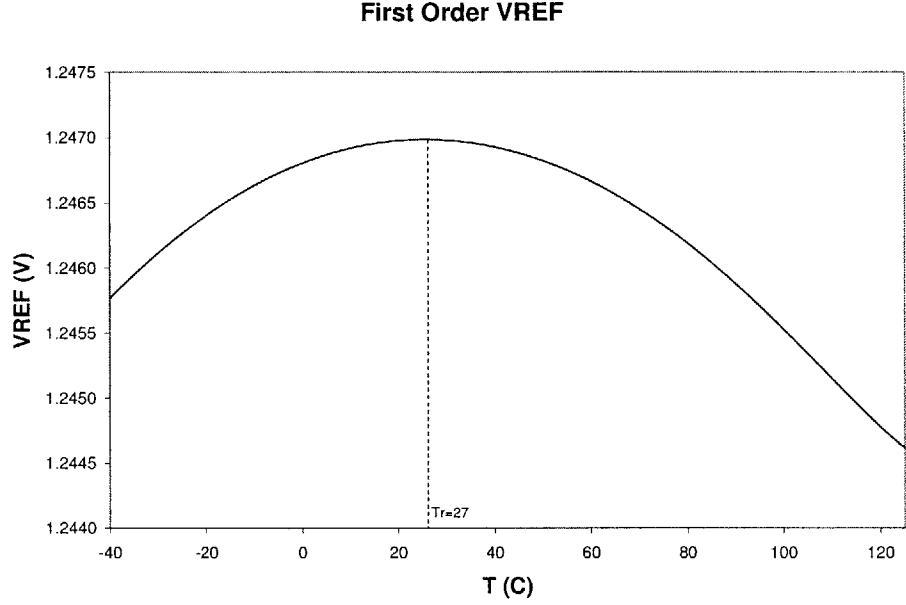
First Order VREF

Figure 2-3: First Order V_{REF} TC

2.4 Simplified Bandgap Schematic

In this thesis, we used an LTC bandgap reference as a test structure for our packaging stress tests. The bandgap reference used is a derivation of the Brokaw cell.[5][6] A precision op-amp is used to drive equal collector currents into the 2T cell. To meet the accuracy specifications, pre-package and post-package trim networks are used. Finally, curvature correction is added, turning the parabolic temperature characteristic of a first order cell into the S-shape of a higher-order bandgap.

The simplified schematic for the bandgap used in these experiments is shown in Figure 2-4. In equilibrium, equal PTAT currents flow through Q1 and Q2. Since the emitter area of Q2 is N times larger than Q1, the current densities will differ by a factor of N causing a ΔV_{BE} to occur across R_{SET}. Assuming that the resistors are zero TC, the ΔV_{BE} will be PTAT and the current through R_{SET} will also be PTAT. A V_{BE} adds to the voltage created by the PTAT current flowing through R_{TRIM}, R_{SET} and R_{CURVE}, creating V_{REF}. Ignoring the I_{CURVE} current source, this achieves a first order bandgap reference.

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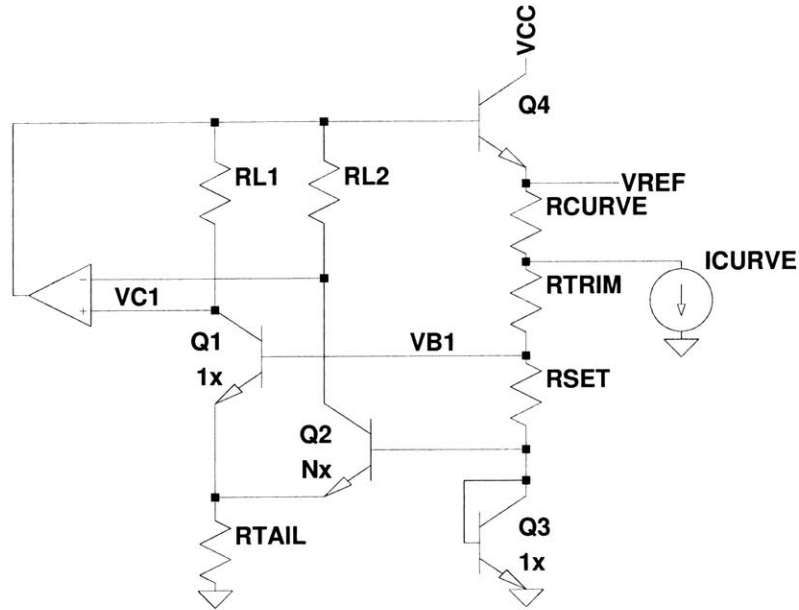
Figure 2-4: Bandgap Under Test

The op-amp functions to drive equal currents through Q1 and Q2, regulating the voltage across R_{SET} to $kT/q * ln(N)$. To see the operation, suppose that the currents are initially equal and V_{B1} drops slightly. This will cause slightly less current to flow in Q1, causing V_{C1} to rise. Since the voltage at the positive terminal of the op-amp is rising, the op-amp output at the base of Q4 will rise. This means more current will run through the resistor string, causing the V_{B1} to rise slightly, restoring equilibrium.

As mentioned before, the op-amp functions to force equal currents through Q1 and Q2, regulating the voltage across R_{SET} to $kT/q * ln(N)$. At higher temperatures, the curvature correction current source I_{CURVE} begins to draw more current, as shown in Figure 2-5. Since the voltage across R_{SET} is regulated, the PTAT current through R_{SET} and R_{TRIM} remains unchanged. The curvature correction current source causes an additional current to flow across R_{CURVE}, creating a voltage drop that increases V_{REF}. As a result, the drop in V_{REF} at higher temperatures for first order bandgaps is averted. Figure 2-6 shows the temperature characteristic for this curvature corrected bandgap reference.

ICURVE vs Temperature
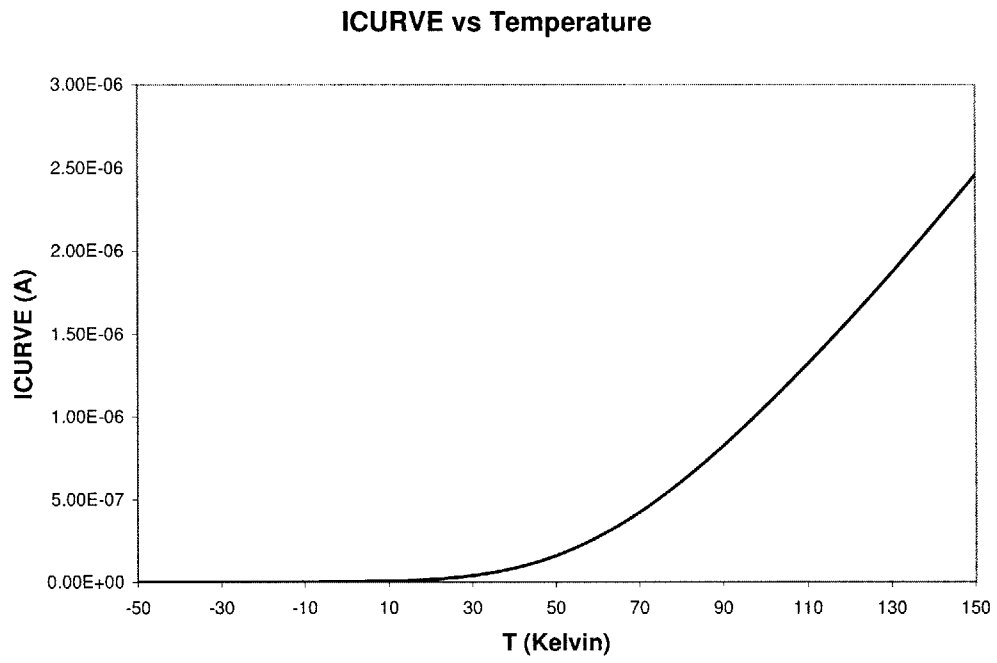
Figure 2-5: Curvature Correction Current vs. Temperature

Curvature Corrected VREF
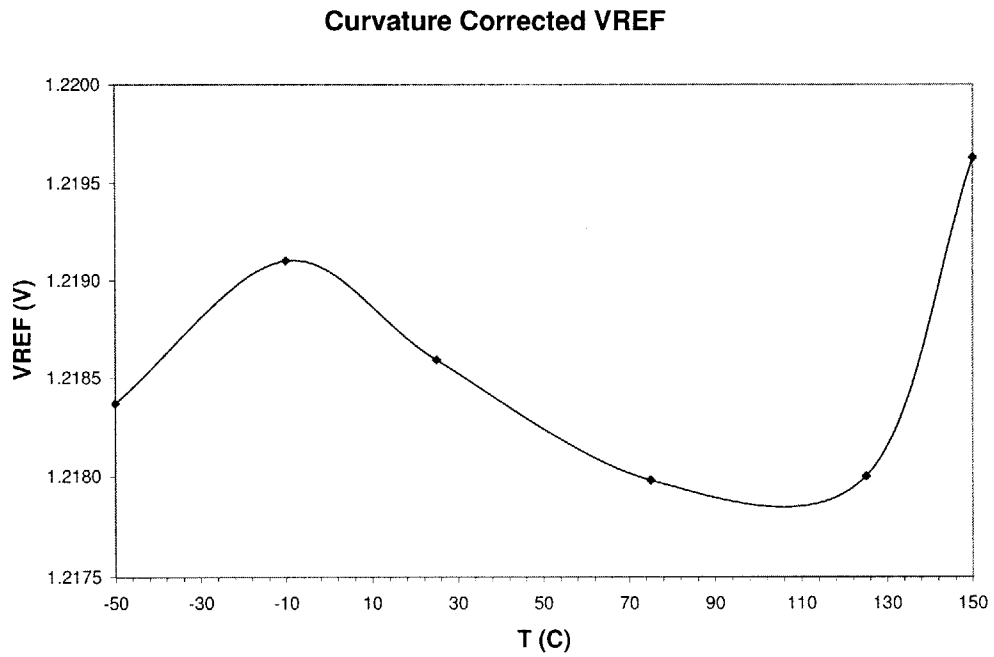
Figure 2-6: Curvature Corrected V_{REF} TC

Chapter 3

Theory of Packaging Stress

3.1 Overview

A major challenge in precision IC design is dealing with the stress induced by the assembly process. After using simulations to design circuits that meet tight specifications and trimming wafers to meet these specifications, the designer often finds that offsets have crept into the product after plastic packaging. One solution is to turn to post-package trimming, allowing all of the parts to re-enter the specification. Even after this trim, problems can arise when customers mount these parts onto PCBs, inducing additional stresses from soldering.

This chapter introduces some of the sources of mechanical stress in plastic packaged ICs. Some current solutions to the packaging stress issue are presented. Finally, the chapter discusses the electrical effects of stress on bipolar transistors and the specific bandgap reference under test.

3.2 Origins of Mechanical Stress

This section covers how the processing steps in plastic packaging apply stress to the silicon die. A cross-section of a typical plastic package is given as Figure 3-1.

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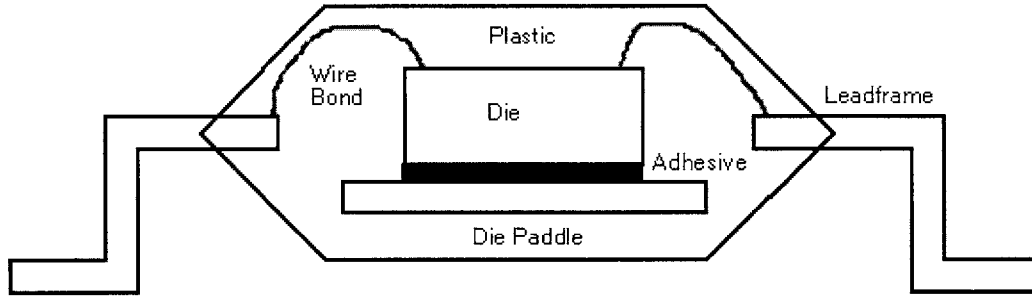
Figure 3-1: Cross-section of Plastic Package

After a wafer is tested at wafer-sort, it is diced to produce the individual die. The die is then mounted on the die paddle using a silver-filled epoxy adhesive paste called die attach. The adhesive is cured by baking the package in an oven, typically at 150°C. Gold wire bonds are attached to bond pads on the die, connecting these pads to the package leads. The parts are then loaded into mold cavities. Liquid molding compound is forced into the mold cavities encapsulating the parts in plastic. Finally, the individual leads are isolated from each other and shaped into a profile.[7]

In this process, stress is introduced by the differing temperature coefficients of expansion (TCE) of the various materials. Silicon has a low TCE compared to the die attach and plastic molding compounds. For example, the die attach is cured by baking the package in an oven. As the package cools, the die attach will contract at a different rate then the silicon die, inducing a stress that increases as the die approaches room temperature. Similarly, the plastic encapsulation is typically done around 175°C. Again, the plastic has a TCE greater than the silicon, and the plastic exerts an increasing stress from above as the part cools to room temperature. Vertical, compressive stresses are highest near the center of the die, but are consistent from package to package. Horizontal, shear stresses are highest near corners and edges, and are more random from unit to unit. The plastic mold contains silica fillers that vary in size and shape. These reduce the coefficient of thermal expansion in order to prevent destructive events like corner and passivation layer cracking and metal-line shifts. Since these fillers have somewhat random size, shape, and orientation,

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they exert unpredictable stresses on localized areas of the die. Finally, the metal lines result in humps and troughs in the silicon surface that will lead to non-uniform stresses on the die[8]. The stress relief mechanism under investigation is only effective for stress sources above the die, such as plastic encapsulation.

A customer can introduce additional package stress when they mount the IC on a PCB. Soldering the IC brings portions of the IC to elevated temperatures and the subsequent cooling can cause a change to the stress field on the silicon. In addition, the leads are now fixed, which causes an unrelieved stress on the leadframe. If the board containing the IC is flexed, an additional stress is introduced to the IC. Since LTC tests packaged parts using mechanical contactors that impart little stress, stresses induced by the customer may bring an LTC-tested part out of specification.[9]

Thermal hysteresis is the room temperature voltage change when a part is cycled between hot and cold temperatures. When the part is heated, the plastic and silicon die will expand at different rates. When the part is cooled back to room temperature, the plastic and silicon will contract at different rates again, except there is no guarantee that the stress will return to the exact same amount in the exact same location. As a result, a reference voltage sensitive to package stress may deviate slightly in room temperature measurements. The same phenomenon will occur on a room temperature-cold-room temperature cycle.[10]

3.2.1 Current Solutions

The best solution to most stress problems is proper layout. Symmetrical layouts should be used. For example in a 10x-1x bandgap cell, the 10x transistor should be broken into two parts of 5, and surround the 1x transistor. Common centroid layouts should be used for differential pairs. The bandgap cell should be kept away from corners of the IC, where the stresses are most extreme. In this particular chip, the bandgap cell appears at the left-center edge of the IC with the key transistors located towards the center of the chip.

Beyond proper layout, IC designers have used coatings to alleviate stress shifts. Some coatings consist of inserting a drop of a gel inside the plastic before the plastic molding procedure. However, the gel provides less stress relief at the edges of the die, where the coating is the thinnest.

3.3 Electrical Effect

The change in electrical characteristics of a transistor as a result of mechanical stress can be traced back to the electronic band structure of silicon. Stress, the effect of the applied force to an area of the silicon, is first converted into a strain, the resulting deformation of the silicon. This strain changes the interatomic distances within the lattice, and if the strain is not a pure dilation, destroys the cubic symmetry. The induced strain changes the band structure of silicon, and thus modifies the electrical properties.

The band structure of silicon is represented by plotting a quantity called the wave-vector (denoted $\mathbf{k}$) versus energy of the electrons. The wave-vector is defined as the inverse of the wavelength associated with a particle of a particular momentum. Here the de Broglie wavelength is defined as h/p, where h is Planck's constant, and p is momentum. Since momentum is effective mass times velocity, $\mathbf{k}$ is a representation of effective mass. The band structures for unstressed (left) and stressed silicon are given in Figure 3-2.

In the absence of strain, the forbidden bandgap between the valence band and conduction band is a single quantity. In addition, the symmetry of the crystal leads to the valence band $\mathbf{k}$-vectors tangent at $\mathbf{k}$=0. The addition of strain changes the wave-vectors and thus changes the effective mass. As seen in Figure 3-2b, the forbidden bandgap is no longer a single quantity. If the strain changes the symmetry, the valence band curves are no longer tangent at $\mathbf{k}$=0. When the effective masses of the carriers change, the mobility changes. This causes a change in saturation current, leading to a change in V_{BE}.[3]
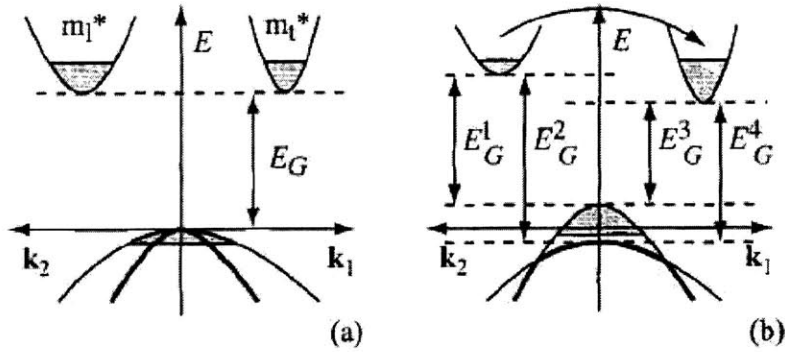
Figure 3-2: Bandstructure for Unstressed and Stressed Silicon - From Creemer[3]

Researchers at the Delft University of Technology[3][11][12] have investigated the change in I_S as a result of stress, termed the piezojunction effect. In their research, they applied a uniform, precisely measured stress to a chip, and measured the changes in V_{BE} and ΔV_{BE}. This thesis does not measure the stress applied; rather, we measure the electrical changes to a large distribution of plastic packaged parts. While this is less precise than the Delft Researchers, it takes into account real-world packaging stress issues, such as localized random points of high stress within a uniform stress field. In addition we attempted to find the change in "magic" voltage (defined in Chapter 2) and changes to the bandgap energy of silicon extrapolated to 0K and curvature factor, E_{G0r} and η. Finally, we measured the temperature linearity of the ΔV_{BE} cell.

3.4   Impact of Stress on Bandgap Under Test

This section poses some possible stress scenarios, and hypothesizes their possible impact on bandgap performance. The bandgap under test is repeated below for convenience.

33
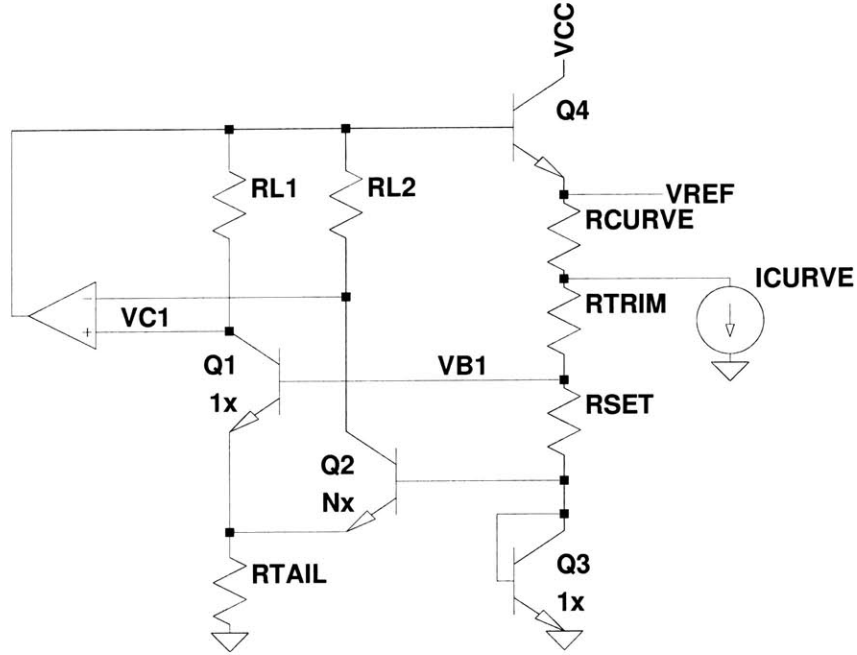
Figure 3-3: Bandgap Under Test

3.4.1 Uniform Stress Field

One possible stress scenario is uniform stress on all components of the bandgap cell. Given a uniform stress field, R_{L1} and R_{L2} will remain matched. Assuming a post-stress ideal op amp, the collector currents for Q1 and Q2 will remain equal. Also, the ratio $(R_{CURVE} + R_{TRIM} + R_{SET})/R_{SET}$ will remain at its pre-stressed value. Next, we examine the effect of a uniform stress on the ΔV_{BE}. From Chapter 2, I_S is given as

$$I_S(T) = \frac{ABCkT^\eta \exp\left[\frac{-qE_G(T)}{kT}\right]}{N_B} \qquad (3.1)$$

If a uniform stress field scales parameters such as η and E_G by an amount independent of transistor size, the I_S ratio will not change, and the ΔV_{BE} will remain $kT/q*ln(N)$. The correction voltage V_C is given by $\Delta V_{BE}(1 + (R_{TRIM} + R_{CURVE})/R_{SET})$, so V_C remains unchanged. Finally, we examine the effect of stress on transistor Q3. Previous

research has shown that stress lowers the bandgap energy of silicon. The effect of stress on the curvature factor η is unknown to the author's knowledge and will be investigated later in this thesis. A reduction in E_{G0r} will cause an increase in I_S. This causes a reduction in V_{BE}. Since V_C is unchanged by stress, the reduction in E_{G0r} results in a decrease in V_{REF}. An increase in η causes a increase in I_S and a decrease in V_{BE}. Since V_C is unchanged, the reduction in V_{BE} results in a reduction in V_{REF}.

By comparing the post-package shift in room temperature V_{REF} to the post-package shift in room temperature V_{MAGIC}, we can deduce whether packaging stress causes a change in the temperature coefficient. The temperature characteristic for a first-order V_{REF} is a parabola opening downwards. Assume that the bandgap is correctly operating such that the room temperature V_{REF} is close to the room temperature V_{MAGIC}. If the room temperature V_{REF} is below V_{MAGIC}, the bandgap does not have enough positive TC correction voltage and V_{REF} will appear with a net negative temperature coefficient. Similarly, if the room temperature V_{REF} is above V_{MAGIC}, the bandgap has too much correction voltage and V_{REF} will appear with a net positive temperature coefficient.

We examine the impact of E_{G0r} and η stress variations on the bandgap reference temperature coefficient independently. First, we assume that packaging stress modifies the bandgap energy of silicon extrapolated to 0 Kelvin from E_{G0r} to E_{G0rs}. In addition, we assume that packaging stress does not change the curvature factor η, derived from the temperature dependences of the intrinsic carrier concentration and mobility. We use equations from Section 2.3 to determine how the room temperature values of V_{MAGIC} and V_{REF} shift with packaging stress.

From Chapter 2, the room temperature pre-stress and post-stress values of the magic voltage, designated as V_{MAGIC} and V_{MAGICs} respectively, can be written as Equations 3.2 and 3.3.

$$V_{MAGIC} = E_{G0r} + (\eta - 1)\frac{kT_r}{q} \qquad (3.2)$$

$$V_{MAGICs} = E_{G0rs} + (\eta - 1)\frac{kT_r}{q} \qquad (3.3)$$

$$V_{MAGICs} - V_{MAGIC} = E_{G0rs} - E_{G0r} \qquad (3.4)$$

Next, we derive the room temperature pre-stress and post-stress values of V_{REF}, designated as V_{REF} and V_{REFs} respectively. From Chapter 2, V_{REF} is formed by adding a PTAT correction voltage V_C to a base-emitter voltage V_{BE}. As previously shown, a uniform stress field does not modify the correction voltage V_C. Then the stress-induced change in V_{REF} equals the stress-induced change in V_{BE}, as shown by Equation 3.7.

$$V_{REF} = V_C + V_{BE} \qquad (3.5)$$

$$V_{REFs} = V_C + V_{BEs} \qquad (3.6)$$

$$V_{REFs} - V_{REF} = V_{BEs} - V_{BE} \qquad (3.7)$$

The next step is to find the stress-induced change in V_{BE}. To do this, we use Equations 3.8 and 3.9 (taken from Chapter 2) to derive Equations 3.10 and 3.11, which express V_{BE} at room temperature in terms of I_C at room temperature, E_G at room temperature, η, and processing parameters.

$$V_{BE} = \frac{kT_r}{q}\ln\left(\frac{I_C(T_r)}{I_s}\right) \qquad (3.8)$$

$$I_s = \frac{ABCkT_r^\eta \exp\left[\frac{-qE_G(T_r)}{kT_r}\right]}{N_B} \qquad (3.9)$$

$$V_{BE} = \frac{kT_r}{q}\ln\left(\frac{I_C(T_r)N_B}{ABCkT_r^\eta \exp\left[\frac{-qE_G(T_r)}{kT_r}\right]}\right) \qquad (3.10)$$

$$V_{BE} = \frac{kT_r}{q} \ln\left(I_C\left(T_r\right)\right) - \frac{kT_r}{q}\left(\eta\right)\ln\left(T_r\right) + \frac{kT_r}{q}\ln\left(\frac{N_B}{ABCk}\right) + E_G\left(T_r\right) \quad (3.11)$$

For this portion of the analysis, we assumed that stress did not modify η. Furthermore, since I_C is derived from V_C for our particular reference, stress does not modify I_C. Finally, we assume that stress does not change the processing parameters A, B, C, nor the Gummel number N_B. This means that the change in V_{BE} is due totally to the change in $E_G\left(T_r\right)$. Comparing the pre-stress and post-stress values of V_{BE}, designated V_{BE} and V_{BEs} respectively, we arrive at Equation 3.13.

$$V_{BEs} = \frac{kT_r}{q} \ln\left(I_C\left(T_r\right)\right) - \frac{kT_r}{q}\left(\eta\right)\ln\left(T_r\right) + \frac{kT_r}{q}\ln\left(\frac{N_B}{ABCk}\right) + E_{Gs}\left(T_r\right) \quad (3.12)$$

$$V_{BEs} - V_{BE} = E_{Gs}\left(T_r\right) - E_G\left(T_r\right) = E_{G0rs} - E_{G0r} \quad (3.13)$$

Equation 3.13 is derived by assuming that stress shifts the $E_G\left(T\right)$ curve, but does not alter its shape. Equations 3.4 and 3.13 show that change in V_{REF} is compensated by an equal change in V_{MAGIC}. This means that if the effect of packaging stress is to change only E_{G0r}, the reference will still be operating at its optimum room temperature value after stress.

We now examine the impact of a stress modification on the curvature factor η with no change in the bandgap energy. Again, we chart the change in room temperature V_{REF} versus the room temperature V_{MAGIC}.

$$V_{MAGIC} = E_{G0r} + \left(\eta - 1\right)\frac{kT_r}{q} \quad (3.14)$$

$$V_{MAGICs} = E_{G0r} + \left(\eta_s - 1\right)\frac{kT_r}{q} \quad (3.15)$$

$$V_{MAGICs} - V_{MAGIC} = \left(\eta_s - \eta\right)\frac{kT_r}{q} \quad (3.16)$$

Once again, in the presence of a uniform stress field, the stress variation on

V_{REF} equals the stress variation on V_{BE}. The stress variation on V_{BE} due to stress modification of η is given as Equation 3.19.

$$V_{BE} = \frac{kT_r}{q} \ln\left(I_C\right) - \frac{kT_r}{q}\left(\eta\right)\ln\left(T_r\right) + \frac{kT_r}{q}\ln\left(\frac{N_B}{ABCk}\right) + E_G\left(T_r\right) \quad (3.17)$$

$$V_{BEs} = \frac{kT_r}{q} \ln\left(I_C\right) - \frac{kT_r}{q}\left(\eta_s\right)\ln\left(T_r\right) + \frac{kT_r}{q}\ln\left(\frac{N_B}{ABCk}\right) + E_G\left(T_r\right) \quad (3.18)$$

$$V_{BEs} - V_{BE} = -\frac{kT_r}{q}\left(\eta_s\right)\ln\left(T_r\right) + \frac{kT_r}{q}\left(\eta\right)\ln\left(T_r\right) = \frac{kT_r}{q}\ln\left(T_r\right)\left(\eta - \eta_s\right) \quad (3.19)$$

Comparison of equations 3.16 and 3.19 show that the stress induced change in V_{REF} does not equal the stress-induced change in V_{MAGIC}. Specifically, if the value of η increases, V_{MAGIC} will increase. However, I_S also increases causing V_{BE} to decrease. This means that V_{REF} decreases. Since V_{REF} is lower than V_{MAGIC}, negative TC behavior will be observed.

3.4.2 Large Stress on Q2

Another possible scenario is an isolated region of stress affects Q2 but not Q1, while all transistors are in the presence of an otherwise uniform stress field. This is plausible since Q2 is larger than Q1 and may be more likely to be hit by an isolated random stress point.

If stress causes a decrease in E_{G0r}, then ΔV_{BE} will increase. This is because I_{S2} increases due to the uniform stress field and the large isolated stress point while I_{S1} only increases due to the uniform stress field. This results in a higher I_S ratio in the ΔV_{BE} cell. The sign of the room temperature V_{REF} change is uncertain since V_{BE3} has dropped, but the the correction voltage V_C has increased. From the previous derivations, we stated that V_{MAGIC} dropped by the same amount as V_{BE3}. Since V_C has increased, V_{REF} will show a net positive temperature coefficient.

If stress causes an increase in η, then ΔV_{BE} will increase. This is because I_{S2} increases due to the uniform stress field and the large isolated stress point while I_{S1}

only increases due to the uniform stress field. This results in a higher I_S ratio in the ΔV_{BE} cell. The sign of the room temperature V_{REF} is uncertain since V_{BE3} has decreased, but the the correction voltage V_C has increased. In addition, the sign of the temperature coefficient is uncertain, since the increase in η induces negative TC behavior due to Q3, but the isolated stress point increased V_C, inducing positive TC behavior due to the ΔV_{BE} cell.

While the package shift induced by a uniform stress field is a systematic shift, resulting in a mean offset in the V_{REF} distribution, scenarios such as large isolated stresses on Q2 are random effects and result in distribution widening. If larger transistors truly are more susceptible to isolated stresses, then an isolated stress on Q2 will contribute both to the mean offset and distribution widening.

Chapter 4

Impact of Packaging Stress on Bandgap References

4.1 Overview

Our first set of experiments assesses the effectiveness of the stress relief mechanism in improving the performance of a precision bandgap reference onboard an LTC switching regulator. Two wafers of the switching regulator were fabricated, identical except for the presence or absence of the stress relief mechanism. The units without stress relief will be designated the control group, while the units with stress relief will serve as the experimental group. After testing the die at wafer-sort, the die were sent for plastic packaging with the bandgap reference output brought out to a pin.

This set of experiments has three main parts. First, we compare the room temperature V_{REF} distributions for the control and experimental groups. Since both wafers are identical after wafer-sort, this experiment will examine the impact of plastic packaging stress on the room temperature distributions. In the second part of this experiment, we compare the temperature characteristics of V_{REF} for the representative parts in the control and experimental groups. The third part of this experiment measures the thermal hysteresis, as parts are cycled between room

temperature, high temperature, and low temperature.

4.2   Experimental Setup

To generate an effective comparison of the control and experimental groups, the groups need to be identical before introducing packaging stress. This is achieved at wafer sort by trimming all the die to the same target voltage, within the resolution of the trim scheme. Trimming turns a wide Gaussian distribution to a tight rectangular distribution. Figures 4-1 and 4-2 show the pre-trim and post-trim V_{REF} distributions at wafer sort for the two wafers used in these experiments. The bandgap reference trim achieves a resolution of $\pm1mV$ about a specified 1.216V trim target. The mean pre-trim V_{REF} is not the same for both wafers due to random variations in the wafer processing.
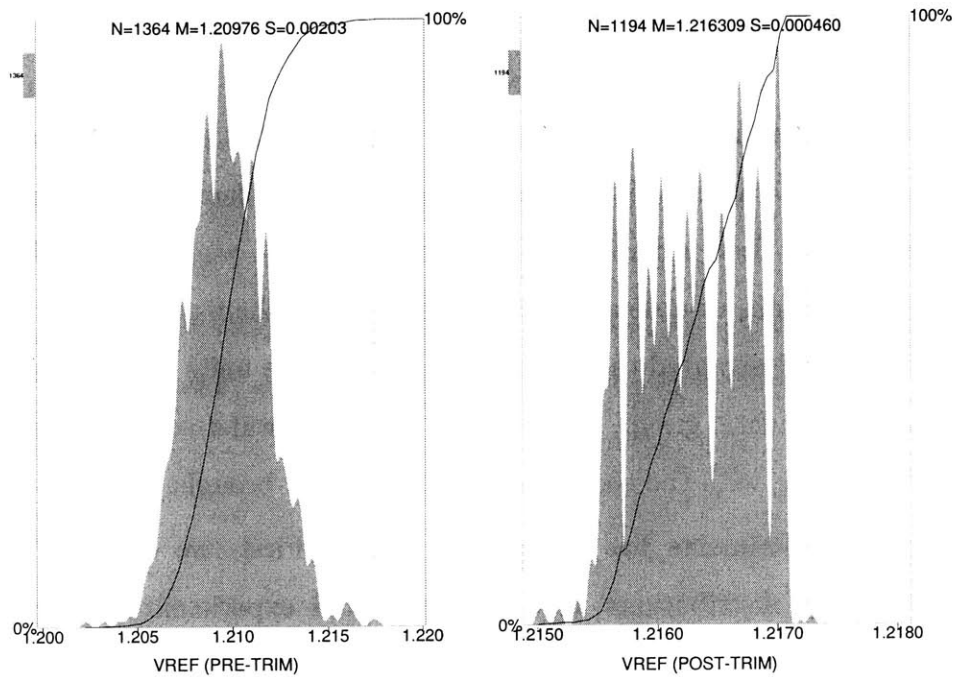
Figure 4-1: Wafer Sort Distribution - No Stress Relief

After the wafer-sort trim, the parts were packaged in 36 lead SSOP plastic packages. Figure 4-3 shows the package type used for these experiments.

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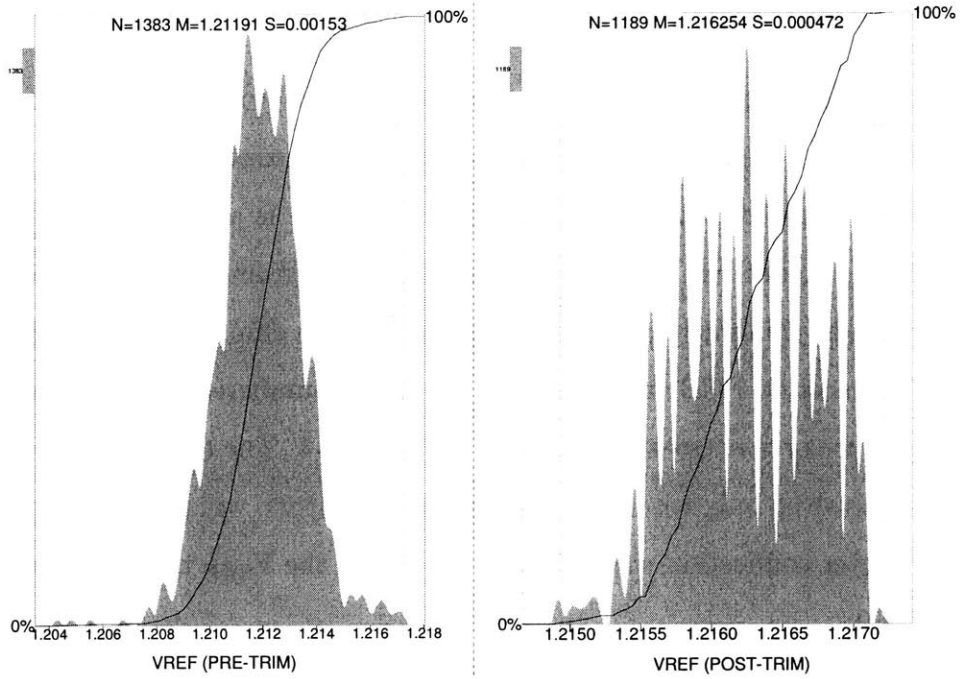
Figure 4-2: Wafer Sort Distribution - Stress Relief
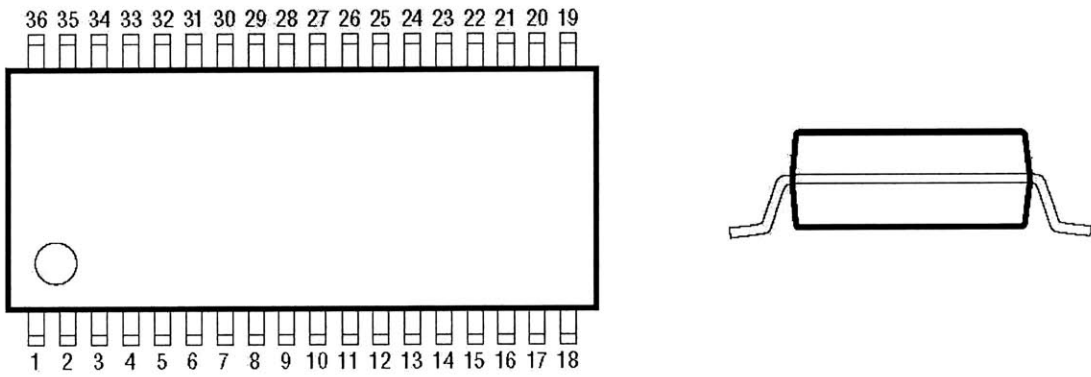
Figure 4-3: SSOP Package Diagram

4.3 Room Temperature Characterization

4.3.1 Experimental Setup

After plastic packaging, both groups were tested by hand at room temperature. Room temperature tests were performed using sockets, which exert very little stress on the package. When the lid of the socket is closed, pressure is applied to the top of the pins of the chip under test. These pins are contacted from below by spring-loaded gold socket leads, minimizing the stress applied to the chip under test. These gold leads then connect to PCB traces which run to the numbered vias surrounding the socket. A picture of the test-setup is given in Figure 4-4. The test schematic for these experiments involved only wires and decoupling capacitors, which are not shown here. The GND meter connection was taken at Via 8 and the V_{REF} meter connection was taken at Via 9.
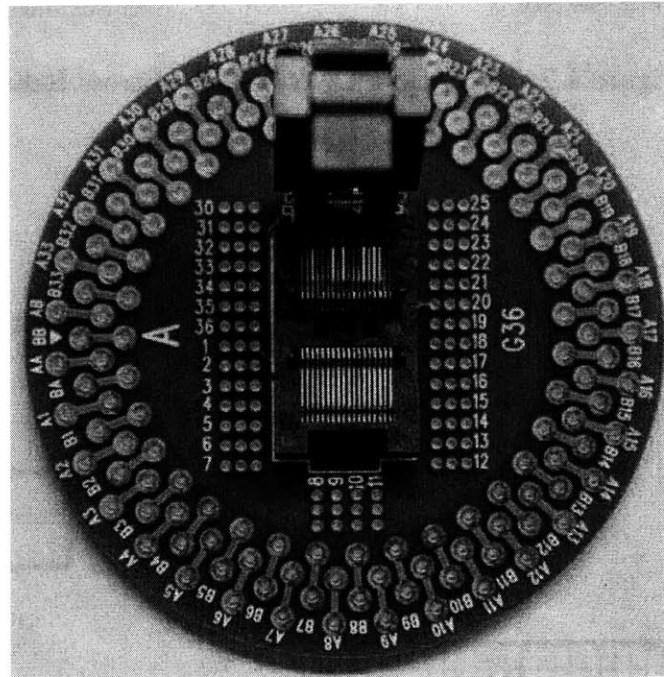
Figure 4-4: Socket-Based Test Setup

Since the reference is only part of the larger switching regulator system, we must ensure that other parts of the switcher do not interfere with measurements of V_{REF}.

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For example, suppose the current drawn from the supply is modulated by an amplifier in the chip. There is a finite resistance from the GND pad on the die through the bond wire, to the GND pin on the plastic package. If the supply current is modulated, the voltage across this bond wire will also be modulated. As a result, the measured value of V_{REF}-GND, will differ from its true value. To prevent this from happening, the gate drivers, onboard oscillator, and all other circuit blocks were switched off.

The HP34401A multimeter is used for these measurements. This particular multimeter has a very high input impedance greater than $10G\Omega$. However, it also has a large input capacitance of about 100pF. Room temperature was between 21°C and 23°C for these experiments. Since V_{REF} is temperature stable, the slight variations in actual die temperature do not impact V_{REF} significantly.

Three hundred and fifty parts were tested in the experimental group with stress relief and the control group without stress relief. Figure 4-5 and 4-6 shows the the post-package room temperature V_{REF} distributions for the two package technologies. These distributions will be compared on the basis of a σ change and μ shift from the pre-package mean.

4.3.2 Analysis

Packaging stress typically introduces a mean shift and a increase in standard deviation as compared to the wafer-sort distributions. These two plots clearly show that the addition of stress relief dramatically tightens the V_{REF} distribution, but does not alleviate the mean package shift issues completely. Consider first that the trimmed wafers had a rectangular distribution of ±1mV about a mean of 1.216V. The control group without stress-relief exhibited a distribution widening with measured values spanning from 1.210V to 1.220V with a standard deviation of 1.6mV. On the other hand, the experimental group with stress-relief had values spanning from 1.2127V to 1.2163V with a standard deviation of 580μV - almost a factor of three improvement. The 2mV pre-package spread increases to a 3.6mV post-package spread with stress

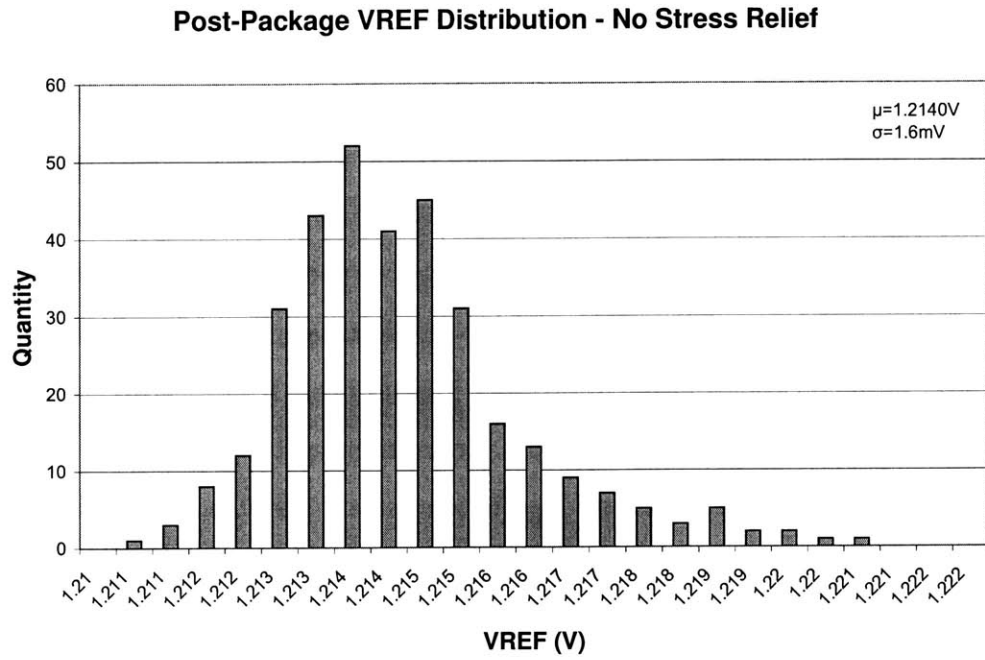**Post-Package VREF Distribution - No Stress Relief**

μ=1.2140V
σ=1.6mV

Quantity

VREF (V)

Figure 4-5: Room Temperature Post-Package V_{REF} Distribution - No Stress Relief

Post-Package VREF Distribution - Stress Relief
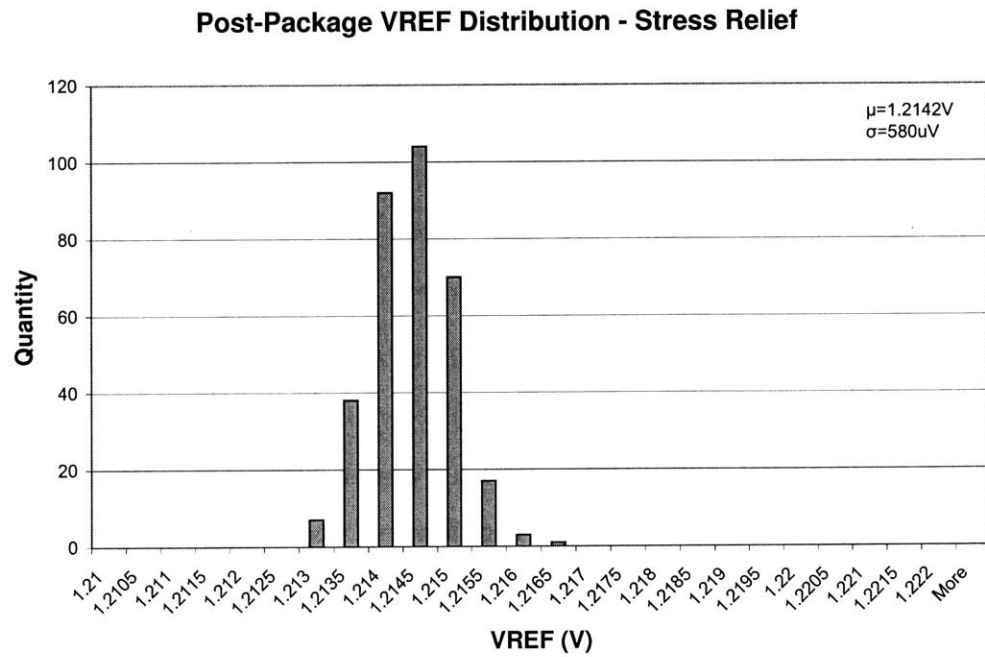
μ=1.2142V
σ=580uV

Quantity

VREF (V)

Figure 4-6: Room Temperature Post-Package V_{REF} Distribution - Stress Relief

relief and a 10mV post-package spread without stress relief. This data suggest that most of the random stress effects that widen a V_{REF} distribution originate from plastic stresses on the top of the die, where the stress relief mechanism is effective.

While the spread of the distribution was greatly improved, both control and experimental groups showed approximately the same mean offset. The control group experienced a mean package shift of about -2.3mV, changing from 1.2163V at wafer sort to 1.2140V post-package. The experimental group also experienced a mean package shift of about -2.0mV, changing from 1.2162V at wafer sort to 1.2142V post-package. This data suggests that the mean offset is due more to the effects of die attach and other stress mechanisms, as opposed to plastic compressive stress from the top.

If the package shift is consistent, the package shift and post-package V_{REF} temperature curves can be characterized. In the switcher, the actual V_{REF} voltage is only used to create a smaller 600mV reference via a resistive divider. This 600mV reference feeds into the positive input of the error amplifier. Once the the room temperature V_{REF} with the best temperature coefficient is found and the package shift is characterized, the divider to create this 600mV reference can be modified. No additional post-package trimming would be needed given tight distribution of the post-package V_{REF} distribution.

The distribution widening of the parts without stress relief is more problematic. For this circuit, post-package trimming is a one-time modification of the resistive divider after packaging to create a tight distribution for the 600mV reference. However, changing this resistive divider cannot change the temperature coefficient of the 600mV reference from that of the 1.2V bandgap reference. If stress causes some of the bandgaps to have unusual TCs, these uncorrectable unusual TCs will appear at the 600mV reference, and therefore at the output of the switcher.

4.3.3 Experimental Justification

When performing these experiments, it was important that both the control and experimental groups received the exact same treatments. That is, measurements for both groups were taken in the same way, such that no factors other than the presence or absence of stress relief differentiate the two groups. Beyond the apples-to-apples comparison between post-package control and experimental groups, there is also the comparison between wafer-sort and post-package data for the two groups. This means that absolute accuracy is required in addition to relative accuracy.

An important specification for justifying the absolute accuracy is the contact resistance between the pins of the package and the spring-loaded leads of the socket. This contact resistance, denoted $R_{CONTACT}$, depends on the area of the pin-to-socket-lead junction and the stress applied to the pins. The major factor altering the contact resistance is the position of the IC within the socket. There is a small amount of wiggle-room in how the IC is placed within the socket. For example, the bottom pins (1-18) can be aligned with the bottom edge of their corresponding socket leads. Similarly, the top pins (19-36) can be aligned with the top edge of their corresponding socket leads. Finally, the IC can be centered within the socket, so that neither set of pins are aligned with any edges. These three configurations are shown in Figure 4-7, where the gold stripes represent the width of the socket leads.

The impact of contact resistances on the measured V_{REF} is shown as Figure 4-8. The quiescent current in these parts is about 5mA. This current flows into the part from the unregulated high voltage V_{IN}. From here, the 5mA splits up to power the op-amps, support circuitry, and bandgap reference, recombining at the ground node. From the GND node to the GND meter connection is a finite resistance that can cause an error in the V_{REF} reading. Since, the quiescent current in these parts is 5mA, a 0.5Ω resistance from the the GND pin to GND meter connection at via 8 translates to a 2.5mV error in the V_{REF} reading. Since the multimeter's input resistance is $10G\Omega$, negligible current will flow out of the V_{REF} node through the

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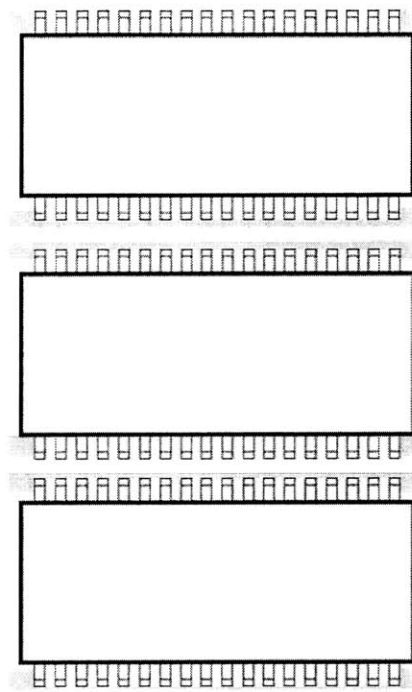
Figure 4-7: Three configurations of IC within socket
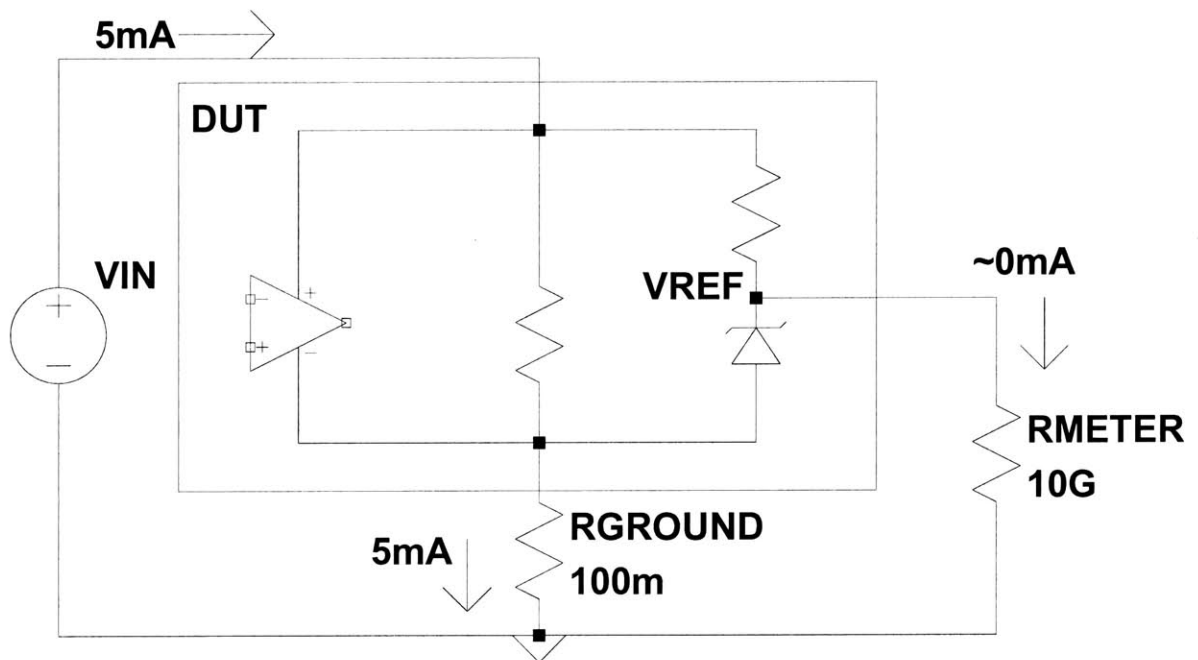
Figure 4-8: Current Flow in the Device-Under-Test

meter connections.

The parasitic resistances that form R_{GROUND} in Figure 4-8 were measured using the circuit in Figure 4-9. There are 4 major drops in the path from the GND pin to the GND measurement point at Via 8. First, there is a nonzero contact resistance ($R_{CONTACT}$) that can be modulated by the placement of the IC within the socket. There is also the resistance of the gold socket leads ($R_{SOCKETLEAD}$) that connect the IC pins to the PCB board trace. Next, there is the resistance of the PCB board trace ($R_{PCBTRACE}$) to Via 8. Finally, there is the resistance of the wire from Via 8 to the multimeter. The following experiment measured the contact resistance, socket lead resistance, and PCB board trace resistance, assuming that the wire resistance from the via to meter was negligible.
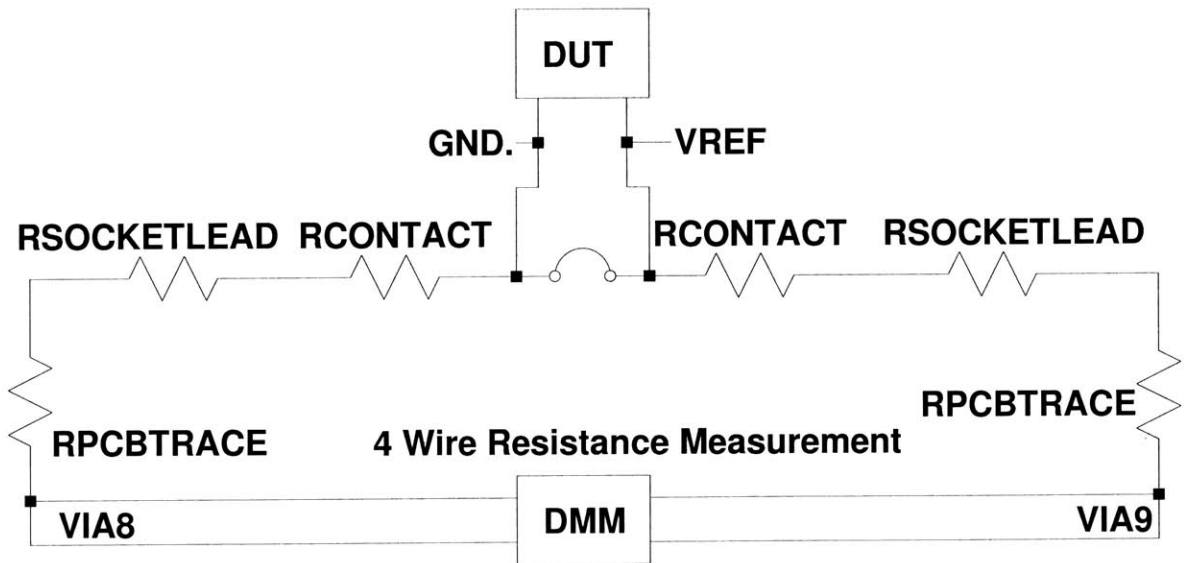
Figure 4-9: Experimental Setup to Measure Contact Resistance

To measure the contact resistance, the adjacent V_{REF} and GND pins were shorted together with a tiny wire at the lead frame, represented by the jumper from the GND to V_{REF} nodes. The socket had an opening at its top, so this wire did not introduce any additional stress factors. A 4-wire resistance measurement was taken from Via 8 to Via 9. Since the only external load on V_{REF} is the multimeter with a $10G\Omega$

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Alignment	Total Resistance	GND Pin-Meter Resistance	Error
Top	145mΩ	72.5mΩ	362μV
Center	188mΩ	94.0mΩ	470μV
Bottom	111mΩ	55.5mΩ	278μV

Table 4.1: Contact and Wiring Resistances in Socket Setup

input impedance, a negligible current flows through the resistance from V_{REF} to Via 9. However, the return path for the part's 5mA quiescent current is through the resistances from GND to Via 8. Thus, these resistances have the potential to cause an error in the V_{REF} reading.

The resistances measured are given in the table of Table 4-1. This shows that the best contact is made when the IC leads are either lined up with the bottom or top of the socket, with the worst contact being made when the IC is centered in the socket. The resistance from GND pin to Via 8 is half the resistance measured in this experiment. This implies that when the IC pins make good contact within the socket, the series resistance between the GND pin and GND meter connection is about 55mΩ. 5mA flows through this resistance, corresponding to an error of about 275μV in V_{REF}.

The alternative to the socket-based measurements is soldering the plastic parts to special boards. However, this has two major consequences. First, soldering adds an additional component of stress that is not induced by the assembly process. In addition, hand soldering 700 parts for room temperature testing was not practical for this thesis. Thus the error source of contact resistance was characterized, but not eliminated.

Since these tests are taken at room temperature, the assumption that the lid exerts a constant stress independent of package alignment is valid. However, as a part is measured over temperature, the stress exerted by the socket lid changes as the plastic socket contracts and expands. Therefore for the temperature testing of the bandgaps, a selection of parts spanning the room temperature distribution were

soldered to special boards. This introduces solder stress to the measurements.

The solder shift was measured by using probe needles to measure $V_{REF} - GND$ directly at the pins while the IC was still in the socket (through the opening in the socket lid), and also when the IC was soldered to one of the special boards. The solder shift was found to be about $+100\mu$V.

4.4 Temperature Characterization

4.4.1 Experimental Setup

Once we have determined the effectiveness of stress relief at room temperature, we compared the temperature coefficients (TC) of the two groups. Analysis of this experiment depends in part on the results of the previous experiment, since there is no temperature characterization data on the wafer before packaging. Since both groups showed the same mean offset, we enter this experiment knowing that there is a stress impact even on the parts with stress-relief. However, the tight post-package distribution of the parts with stress-relief suggests that these parts will exhibit a consistent temperature coefficient. The parts without stress-relief are much more susceptible to random stresses, and we may see some parts that show behavior deviating from expected theory.

In this experiment, parts that spanned the room temperature V_{REF} distribution were soldered to special boards and placed in an oven. The value of V_{REF} is measured at various temperatures over the operating range of -50 to 150°C. As shown in Chapter 2, measuring V_{REF} for various parts will generate a family curves where those parts that are below the optimum magic voltage at room temperature will exhibit overall negative TC behavior, and those that are above the optimum voltage will show overall positive TC behavior. These theoretical curves were verified by testing side-brazed, hermetically sealed ceramic parts. Sidebrazed parts have no compressive stress from the top. In addition, the die can be exposed by lifting a lid, and thus the part

can be trimmed at a probe station (similar to at wafer sort). A family of curves, shown in Figure 4-10, was generated by trimming parts. Since this data was taken on sidebrazed parts, we might expect a different set of curves from plastic packaging as the magic voltage and temperature coefficient might change due to differing packaging stresses.

Temperature Characterization - Sidebrazed
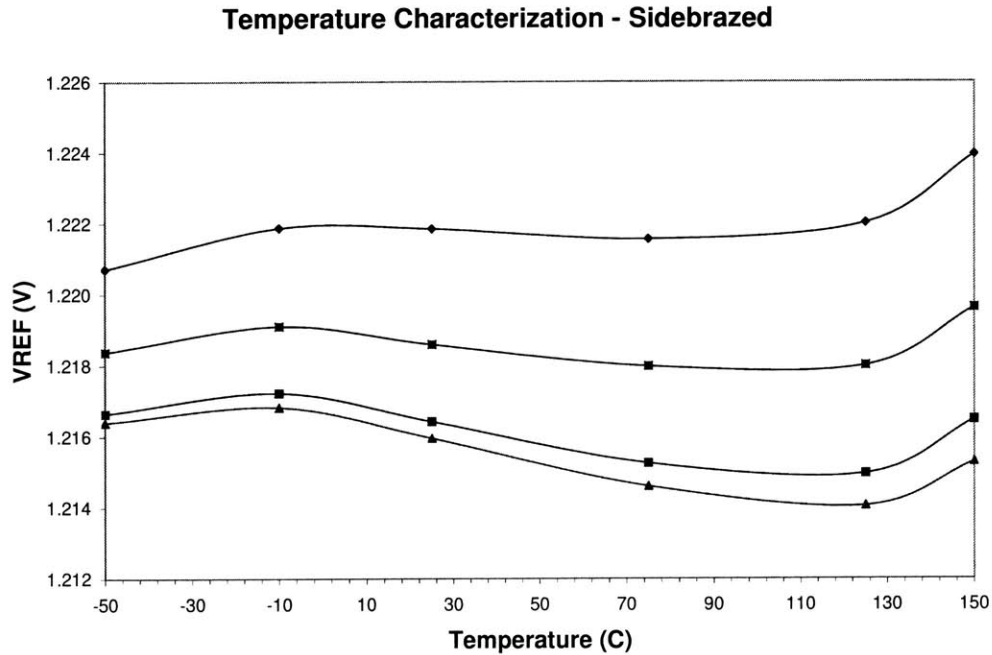
Figure 4-10: Temperature Characterization - Sidebrazed Parts

To insure that all parts taken over temperature received the same thermal stresses, 18 parts were mounted on a large copper board which was placed in an oven. 8 parts with stress relief and 10 parts without stress relief were chosen to span the respective room temperature distributions. An automated test setup took measurements of V_{REF} by first measuring V_{REF} at 25°C, and then heating the oven to 150°C. Measurements were then taken at 15°C increments as the parts were cooled from 150 to -45°C. Finally, the parts were heated back to 25°C and V_{REF} was measured. The TCs obtained are given in Figures 4-11 and 4-12.

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Temperature Characterization (No Stress-Relief)
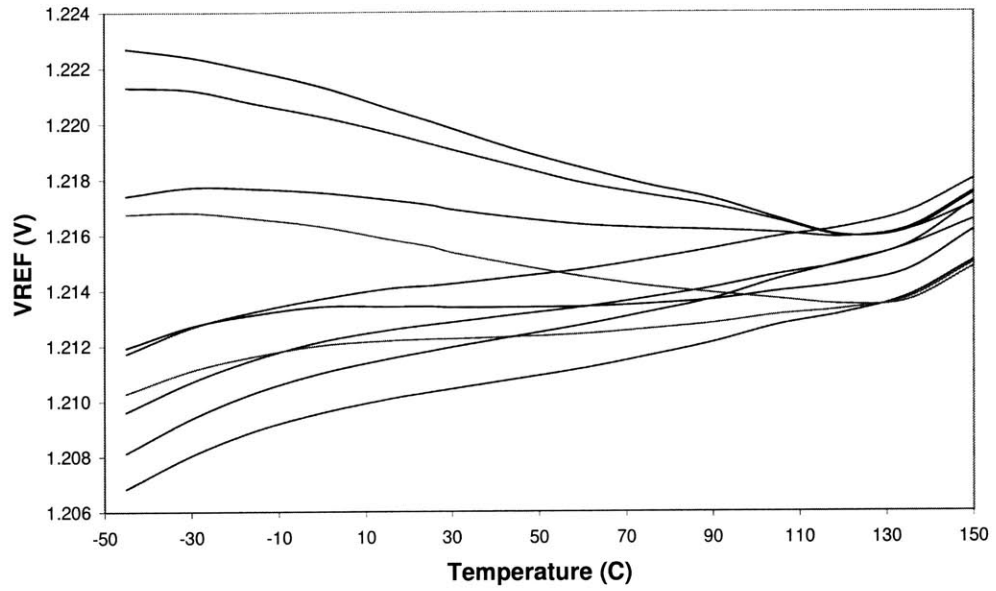
Figure 4-11: Temperature Characterization - No Stress Relief

Temperature Characterization (Stress-Relief)
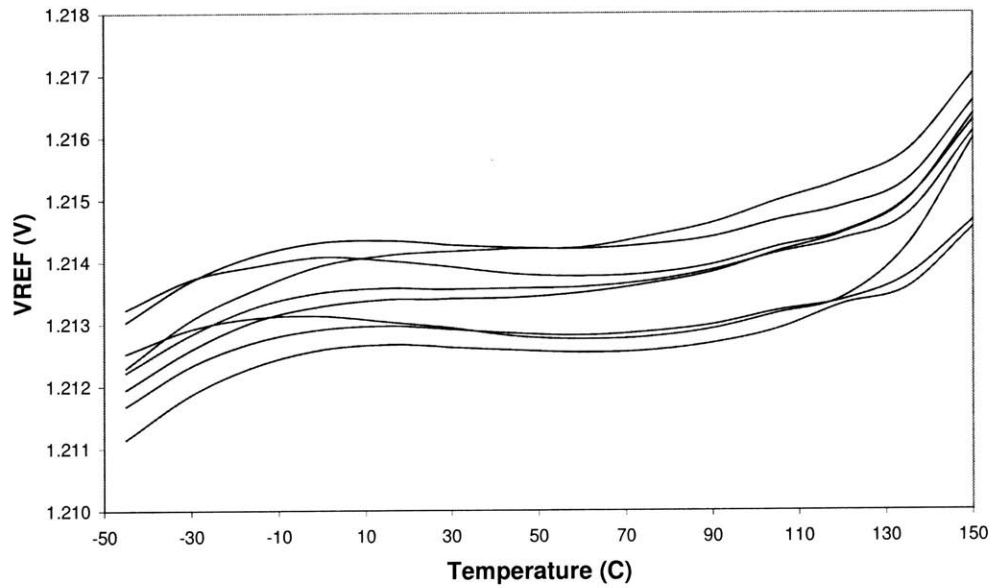
Figure 4-12: Temperature Characterization - Stress Relief

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4.4.2 Analysis

As expected, the TC for the parts with stress relief is very consistent. In particular, both the lowest and highest parts tested, which differ by 2mV at room temperature appear to have almost exactly parallel temperature curves (Figure 4-13). In addition, these parts have much lower room temperature values than the sidebrazed parts tested earlier, but show more positive TC behavior over the temperature range. The data for the parts with stress relief suggest that the magic voltage for these parts is slightly below 1.214V, while the data for the sidebrazed parts suggests that the magic voltage for those parts was around 1.218V.

Temperature Characterization (Stress-Relief)
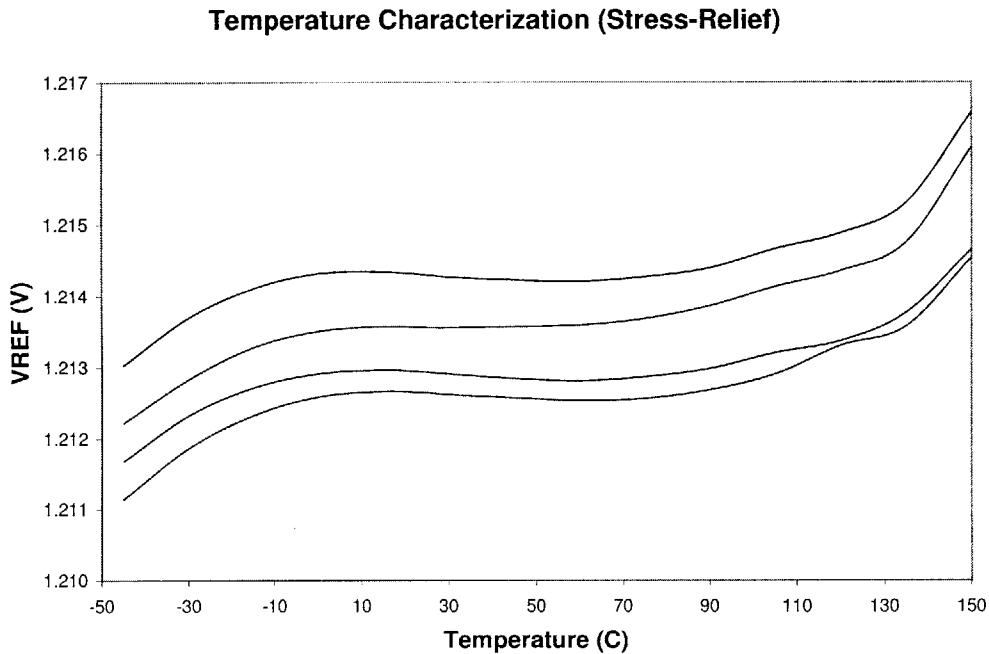
Figure 4-13: Temperature Characterization - Stress Relief

One explanation for the parallel TCs shown by the parts in Figure 4-13 is that a uniform stress field causes drops in the value of E_{G0r} for the various parts. If the value of η was the same for the parts shown, then variation in E_{G0r} will shift the room temperature value, but keep the TC unmodified. The first order curvature of the bandgap does not depend on E_{G0r}, and the curvature correction inflection points

do not move substantially for small changes to E_{G0r}.

One possible explanation for the more pronounced positive TC is a reduction in the value of η. This would have the effect of flattening the first order portion of the bandgap TC. Thus, V_{REF} will not have dropped as low by the time the curvature correction begins at 75°C, pulling V_{REF} up. However, a reduction in η will also flatten the left half (cold half) of the first order portion of the bandgap TC. To test this theory, we can compare one of these stress-relief parts with a room temperature value around 1.214V to a sidebrazed part with a room temperature value around 1.220V. We look at the ΔV_{REF} from 0 to -45°C for both parts. Both parts show a similar 1.2mV ΔV_{REF}, suggesting that both parts have similar values of η.

A final explanation for the more pronounced positive TC is a shift left in the inflection points of the curvature correction. Such a shift would cause the right half of the first order portion to appear flattened while leaving the left half of the first order portion unchanged. If the inflection points move left, the bandgap would have too much curvature correction, and would exhibit strongly positive TC behavior. However, the curvature correction inflection points are fairly insensitive to changes in E_{G0r} and η. To cause a 10°C shift in the inflection point, stress would have to cause V_{BE} to drop by 20mV, which is not supported by this data.

The TCs for parts without stress-relief are rather unusual. First, parts that are extremely low at room temperature show strongly positive TC behavior. Figure 4-14 shows three parts below the post-package mean that have parallel positive TCs even though they differ by roughly 4mV at room temperature.

As with the parts with stress relief, an explanation for the parallel TCs is that these parts experience different drops in E_{G0r}, but have similar values of η. This would imply that the E_{G0r} distribution widens considerably as a result of packaging stress. However, such an explanation would imply that these parts were initially positive TC before introducing packaging stress - a claim that does not seem plausible in light of the TCs of those parts with stress relief.

Temperature Characterization (No Stress-Relief)
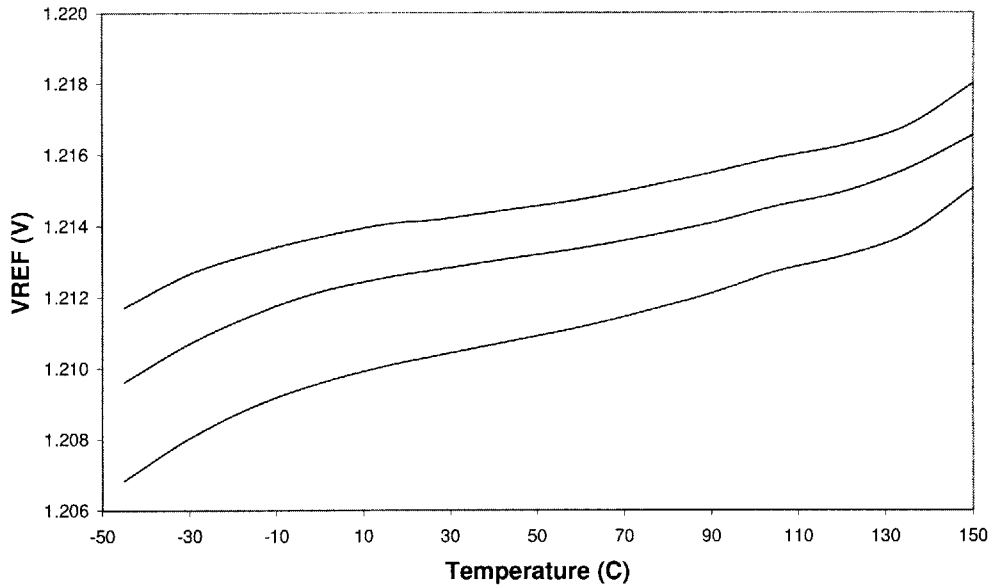
Figure 4-14: Temperature Characterization - No Stress Relief

More troubling is the fact that parts that are extremely high at room temperature show strongly negative TC behavior. Assuming that the die attach yields a uniform stress that shifts the bandgap downwards by approximately 2mV, parts that are high at room temperature would require a stress that acts strongly in the opposite direction to raise V_{REF}. Traditional bandgap theory would imply that these references have too much PTAT voltage added to the V_{BE}, resulting in a strongly positive TC. These parts imply that their magic voltage is much higher than 1.220V, while the other parts imply that the magic voltage may be lower than 1.216V. Efforts to explain these discrepancies are covered in the next section.

Finally, there are two curves within this family of curves that do behave as theoretically expected. These two curves are shown in Figure 4-15, and have room temperature values of 1.216 and 1.217V. These two values are suspiciously close to the pre-package values, and these curves would fit very well with the sidebrazed temperature characteristics presented earlier. These parts may have received similar stresses as the sidebrazed parts, as they fit very well within their family of curves.

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Temperature Characterization (No Stress-Relief)
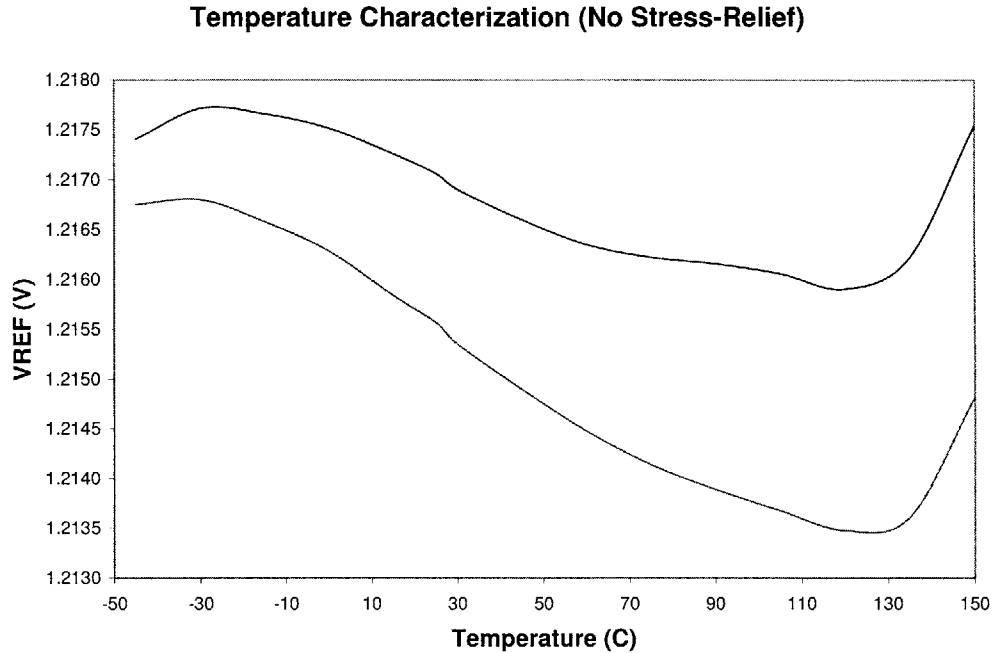
Figure 4-15: Temperature Characterization - No Stress Relief

The temperature characteristics for the parts without stress-relief are at odds with the theory of bandgap references. Packaging stress explanations can be given for the parts that are low at room temperature but yield positive TC temperature curves. However, these explanations imply that the stress within this package is quite extreme - a claim partially supported by the room temperature distributions. Parts that were high at room temperature and yield negative TC temperature curves are more difficult to explain. This data suggests either extreme packaging stress or an unseen error in the test setup. The following section charts attempts to find potential errors in the test setup.

The final verification of this data will be the automated testers used when LTC puts parts into production. These testers look at the V_{FB} voltage, the negative input to the error amplifier. This node is forced almost equal to the internal 600mV reference by the switcher feedback loop. If this TC data correlates with the bandgap data taken, then this particular package is unsuitable for precision bandgaps without stress-relief.

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4.4.3 Experimental Justification

In light of the odd temperature characterization of the uncoated parts, some level of experimental justification is required.

First, similar to the room temperature measurements, care must be taken in how the GND node is sensed by the DMM. Since this experiment involves multiple parts running on the same board, with the same power supply and ground, the voltage drop across the copper ground plane could interfere with accurate measurements. Thus the kelvin ground connections were used, and measurements were taken between the V_{REF} to GND of each individual part.

A second problem was the possibility of oscillations on V_{REF}. The setup presents the reference with a much larger capacitive and/or inductive load than it is used to seeing. The reference was not designed to be pinned out, and is not particularly equipped to see a large capacitive load.

$$ Z_o \Big|_{\omega=0} \approx \frac{1}{g_m} + \frac{r_b}{\beta} $$

$$ Z_o \Big|_{\omega=\infty} \approx r_b $$
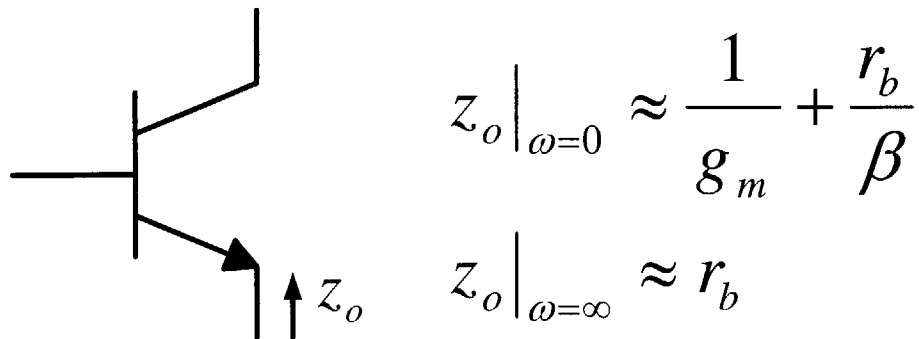
Figure 4-16: Output Impedance of Emitter Follower

As shown in the schematic presented in Chapter 2, the reference output looks into the emitter of an NPN connected as an emitter follower. This particular output stage is vulnerable to oscillations when faced with a large capacitive load because at moderate current levels, the output impedance can look inductive. To see this, we look at the value of the output impedance at low and high frequencies, given as equations 4.1 and 4.2.

$$z_o\big|_{\omega=0} \approx \frac{r_\pi + r_b}{\beta} \tag{4.1}$$

$$z_o\big|_{\omega=\infty} \approx r_b \tag{4.2}$$

At low frequencies, c_π is an open circuit, so the output impedance simplifies to $1/g_m + r_b/\beta$. At high frequencies, c_π becomes a short circuit, and β approaches 1, so the output impedance simplifies to r_b. At moderate current levels, $1/g_m + r_b/\beta < r_b$, meaning the output impedance is rising with frequency (inductive behavior).

Oscillations were initially seen on these parts at temperatures above 125°C, but disappeared at lower temperatures, suggesting that the phase margin of the circuit had a temperature dependence. However, an easy fix is available, by adding a damping resistor of 5.6kΩ in series between the reference and meter. Since the input impedance of the DMM is 10GΩ, this causes a negligible error in the V_{REF} reading, and provides damping for the LC tank formed by the reference output impedance and the capacitive load. This approach eliminated oscillations at high temperatures.

Another possible problem is the internal linear regulator may be oscillating. While this internal regulator does not serve as the supply for the bandgap, they do share a common ground. The impact of these oscillations would be a modulation of the quiescent current, possibly causing a DC error voltage developed between the GND pin and GND meter connection. This was tested by choosing a part that had this problem, and quelling the oscillations with additional capacitance between the internal regulator and GND. No change in the room temperature V_{REF} was found to 100μV accuracy. In addition, the shape of the temperature characteristic remained unchanged.

Finally, the input pins to a current sense amplifier were initially left floating. It was found that this was causing a slight oscillation in V_{REF} at cold temperatures. To solve this problem, the input pins of the sense amplifier were grounded such that noise could not couple into the amplifier. This reduced the quiescent current of the

parts by about 1mA and brought about a related decrease in V_{REF}. This removed the oscillations seen at V_{REF} at cold temperatures, but did not change the shape of the temperature coefficient.

The temperature coefficients for the parts without stress relief are fairly odd, and not particularly believable at first glance. Before assigning the blame to extreme packaging stress, the above error sources were examined. However, removing these error sources did not modify the observed temperature characteristics, suggesting that these temperature characteristics were indeed real, and caused by a combination of packaging stress and pinning out the V_{REF} node. One possibility is that the stress events that caused V_{REF} to shift upwards are different in nature than those that caused V_{REF} to shift downwards, with one set of stress events causing V_{MAGIC} to rise with stress, and the other causing V_{MAGIC} to fall with stress.

4.5 Thermal Hysteresis

The thermal hysteresis test was done as part of the last experiment. The part was initially measured at 25°C, and then heated to 150°C. While cooling, the temperature characterization of the last section was taken. At 25°C, V_{REF} was measured again, and then cooled to -45°C, with the temperature characterization continuing. Finally, after the last cold temperature was taken, the parts were heated back to 25°C, and V_{REF} was measured one last time.

The thermal hysteresis of the bandgap references is shown in Figures 4-17 and 4-18. Figure 4-17 represents the change from initial V_{REF} at 25°C to the value of V_{REF} after being heated to 150°C and cooled to 25°C. Figure 4-18 represents the change from initial V_{REF} at 25°C to the value after being heated to 150°C, cooled to -45°C, and heated to 25°C. For the 18 parts seen, the parts without stress relief have a higher spread in the full hysteresis cycle. Both groups have about the same absolute value worst-case hysteresis for the limited selection of parts tested. With most references exhibiting a hysteresis of 100 to 200μV, we conclude that thermal

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hysteresis is not a substantial problem for these parts with or without stress relief.

Thermal Hysteresis - RT-Hot-RT
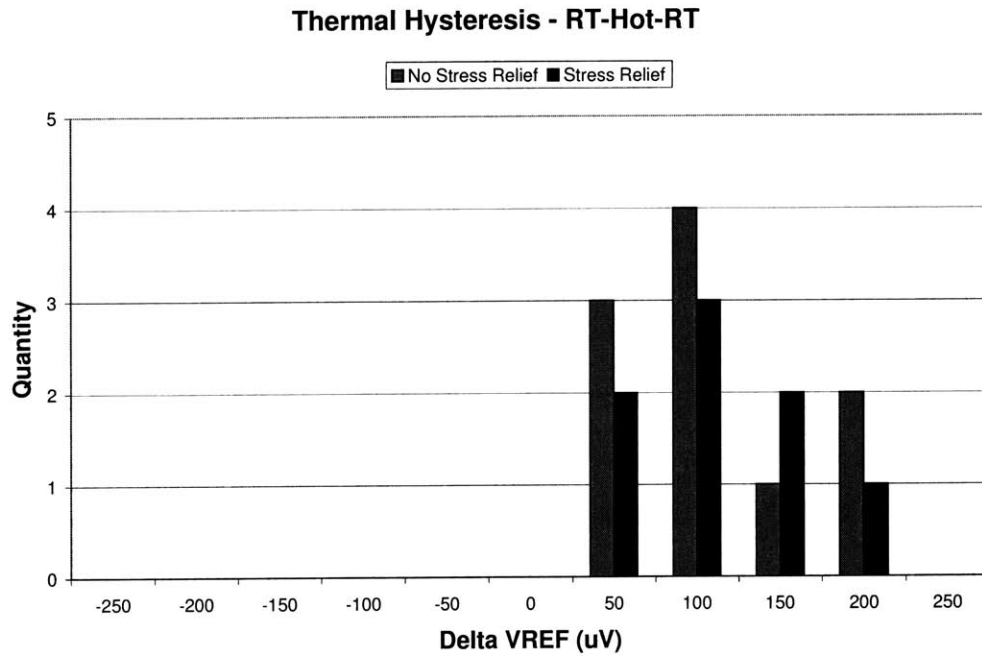
Figure 4-17: Thermal Hysteresis - RT-HOT-RT

4.6 Conclusions

These experiments show that stress-relief mechanism was very effective in improving the performance of bandgap references. A 3x room temperature distribution tightening was found as compared to parts without stress relief. In addition the temperature coefficient of these bandgaps with stress-relief was extremely consistent, in contrast to the parts without stress-relief. The stress-relief mechanism was able to turn a package that had very poor stress performance both at room temperature and over the operating temperature range, and turn it into a viable package option for products containing precision voltage references.
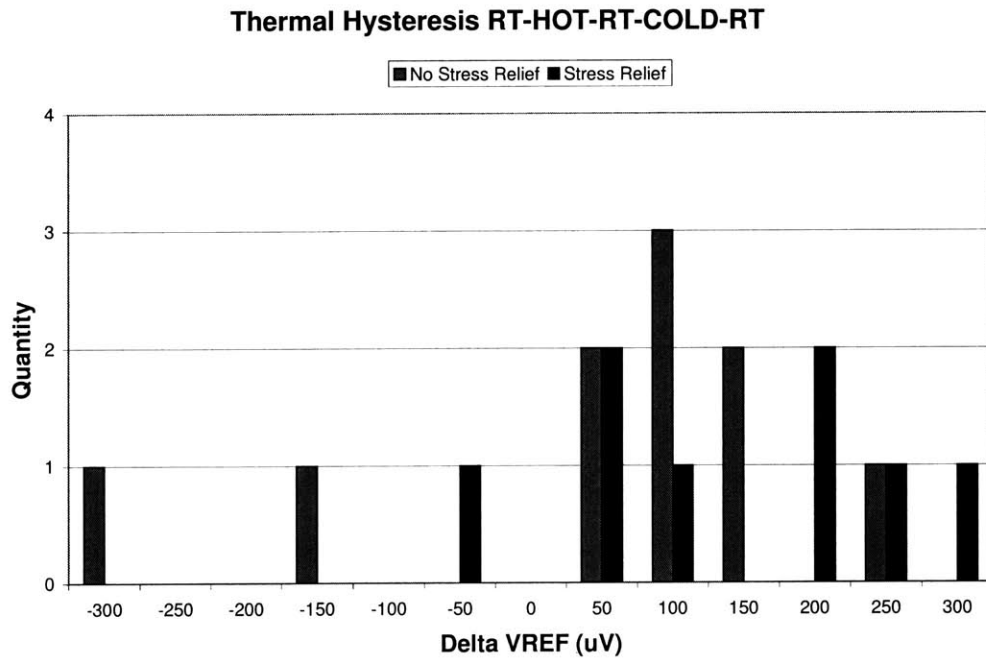
Figure 4-18: Thermal Hysteresis - RT-HOT-RT-COLD-RT

Chapter 5

Impact of Packaging Stress on NPN Transistors

5.1 Overview

This chapter covers a series of experiments investigating the impact of packaging stress on the NPN transistors in the bandgap cell. A new metal mask was created that pins out the terminals of the emitter-coupled 12x-1x NPN transistors in the bandgap core. This allows us to examine these transistors in the same stress configuration as they receive in the functioning bandgap reference. Two wafers were fabricated, with and without stress relief, and the die were assembled in the same SSOP package as the previous experiments.

The previous chapter showed that the addition of stress relief significantly tightened the V_{REF} distribution and resulted in parts with a more consistent temperature characteristic. The first experiment in this chapter examines the V_{BE} and ΔV_{BE} distributions at room temperature. This experiment should help determine if V_{BE} or ΔV_{BE} variation is more responsible for room temperature V_{REF} distribution widening. In the second experiment we examine the V_{BE} and ΔV_{BE} temperature characteristics to see if packaging stress significantly modifies these temperature

dependencies.

5.2   Experimental Setup

The experiments in this chapter were performed using the test circuit shown in Figure 5-1.
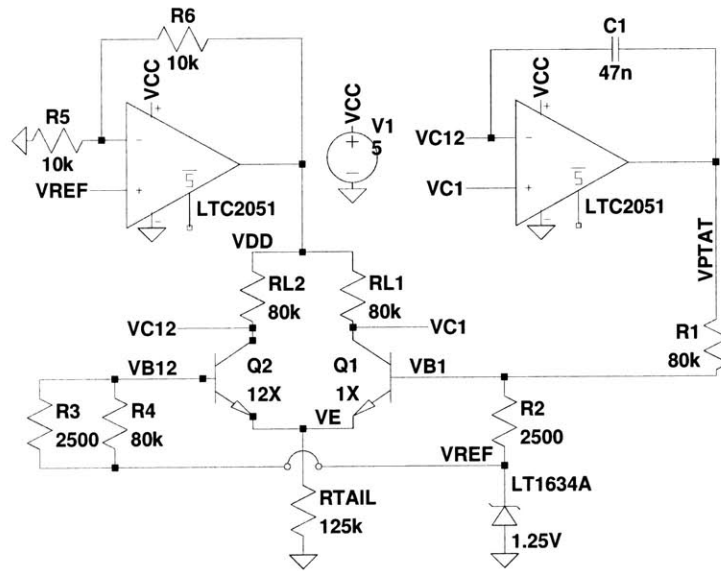
Figure 5-1: Circuit for Evaluating Characteristics of NPN Transistors

This test circuit was created by rewiring components that existed in the bandgap reference. The emitter-coupled 12x-1x pair was used with the same 80kΩ load resistors as in the bandgap cell. An internal 125kΩ resistor was used for the tail resistor of the differential pair, which results in a tail current of 5μA. R_1 and R_4 were formed from a series connection of four identical 20kΩ resistors, while R_2 and R_3 were formed from the parallel combinations of eight 20kΩ resistors. Since these resistors were formed from identical blocks, the resistor matching will be excellent. V_{REF} is realized using the LT1634[13], a precision 1.25V bandgap reference with excellent initial accuracy, low temperature drift and a small minimum operating current. The two op-amps are realized using the LTC2051[14], a precision dual op-amp with low offset voltage, low

offset voltage temperature drift, and low input bias current. Finally, R_5 and R_6 are external resistors used to create the common mode bias point for the differential pair, designated V_{DD}.

This circuit operates in a similar fashion as the bandgap cell presented in Chapter 2. The op-amp outputs a voltage V_{PTAT} such that its input terminals (V_{C1} and V_{C12}) are forced equal. This means that Q1 and Q2 must run at equal collector currents in equilibrium, where Q2 is 12 times larger than Q1. Neglecting R_3 and R_4, this would force a ΔV_{BE} to occur across R_2, where $\Delta V_{BE} = kT/q * ln(12)$. Neglecting base currents, $(V_{PTAT} - V_{REF})$ would yield $\Delta V_{BE}(1 + R_1/R_2)$. R_3 and R_4 are added to eliminate the error in V_{PTAT} due to finite β. ΔV_{BE} no longer appears across R_2, but the amplified version of ΔV_{BE} appearing at V_{PTAT} now has no β dependence. This is important because β has its own temperature dependence, which would interfere in accurate characterization of V_{PTAT}. In addition, β varies from part to part, so mathematical compensation for its influence would be difficult.

To ensure power supply rejection, the common mode bias point for the differential pair, designated V_{DD}, is derived off the external reference. For the room temperature measurements, this V_{DD} is set at 2.5V, leading to approximately 1.25V of base-collector voltage. In the temperature characterization, R_6 is replaced with a potentiometer such that Q1 operates at approximately 0V of base-collector voltage at all temperatures, eliminating the Early effect for this experiment.

V_{REF} is nominally zero TC due to its low temperature drift. The voltage drop across R_2 is approximately equal to ΔV_{BE}, with a slope of $k/q * ln(12)$ which equals $214\mu V/°C$. V_{BE} has a slope of approximately -2mV/°C. Writing KVL around the loop consisting of the bandgap, R_2, Q1, and R_{TAIL}, we find that V_E rises by approximately 2.2mV/°C. The tail resistor has a low TC, measured to be -240ppm/°C, which means the tail current is approximately PTAT and positive TC. Thus, the differential pair runs with approximately the same PTAT current as in the functioning bandgap cell.

The circuit as presented has two stable states. The desired state is described

above, with the external bandgap reference on at 1.25V and approximately 5μA of tail current at room temperature. The undesired state is given when the op-amp is powered, but the bandgap reference is off and there is 0μA of tail current in the differential pair. This state corresponds to 0V at V_{REF}, V_{PTAT}, V_{B1}, V_{B12} and V_E. Since V_{REF} is at 0V, V_{DD} will also be at 0V. With no tail current, V_{C1} and V_{C12} will be at 0V. Since the inputs to the op-amp are 0, the op-amp will output 0V, and the circuit will stay in this state. Now suppose a disturbance causes V_{C1} to rise slightly above V_{C12}. This will cause the op-amp to raise V_{PTAT}, and current will flow into the bandgap reference. The minimum operating current for this particular bandgap is 7uA, which means V_{PTAT} must rise approximately 578mV above V_{REF}. Since the typical open-loop voltage gain is 140db and there is a capacitor in the feedback path, a disturbance of 57nV will be enough to cause this series of events and turn the bandgap reference on.

Once the bandgap reference is on, the lower end of R_2 is pinned to 1.25V. Thus, the op-amp output can be seen as driving the base of Q1 up or down to ensure equal collector currents in the differential pair. If Q1 is drawing too much current, V_{C1} will drop relative to V_{C12}, and the op-amp will lower V_{BE1}. If Q2 is not drawing enough current, V_{C12} will drop relative to V_{C1}, and the op-amp will raise V_{BE1}. As mentioned before, equilibrium is found when the ΔV_{BE} between Q1 and Q2 is exactly equal to $kT/q * ln(12)$.

5.3   Room Temperature Characterization

5.3.1   Experimental Setup

After plastic packaging, both groups (with and without stress relief) were tested at room temperature. As in the previous chapter, room temperature testing was done using sockets which add negligible additional stress and are well-suited for hand-testing a large population of parts.

Since V_{BE} and ΔV_{BE} are very temperature sensitive voltages, a precision thermistor was mounted directly over the socket opening to measure the ambient temperature. We used the Yellow Springs Instruments (YSI) 44100 thermistor - a thermistor that has a resistance of 100kΩ at room temperature and 0.1% initial accuracy. The thermistor resistance has a negative temperature coefficient, and the resistance changes by three orders of magnitude over a 150°C range, allowing accurate measurement of very small temperature variations. Thermistors are much more sensitive than thermocouples and platinum RTD sensors. For example, to measure a 0.01°C temperature deviation about room temperature, one must be able to measure resistance to 45Ω resolution - a manageable proposition. The thermistors are accompanied by a R vs T table listing resistance for every degree in the thermistor's operating range. Using this table, we can interpolate between adjacent (R, T) pairs to obtain temperature accuracy to within 0.01°C.[15]

In this room temperature characterization, we try to find the variation in V_{BE} and ΔV_{BE} for parts with and without stress relief. This means we need to either eliminate or compensate for sources of variation other than packaging stress. One source of V_{BE} variation is due to variation in I_{TAIL} caused by variation in the absolute value of R_{TAIL}. V_E and R_{TAIL} were measured to allow for a post-testing normalization. Temperature variation is another potential source of V_{BE} and ΔV_{BE} variation, and will be covered in detail in the next section.

The HP34401A multimeter was used for these measurements. Since all of the currents in the circuit are in the μA range, the meter must be used with 10GΩ input impedance. While meter connections were still taken as close to the IC pins as possible, the low quiescent current of the test circuit means that errors are not likely to be induced by resistive paths between the IC pins and the meter connections.

250 parts were tested in the experimental and control groups. Figure 5-2 and 5-3 show the V_{BE} distributions for the two groups after normalizing for I_{TAIL} and temperature. Figure 5-4 and 5-5 show the ΔV_{BE} distributions for the two groups

after normalizing for tail current and temperature variations.

Post-Package VBE Distribution - No Stress Relief
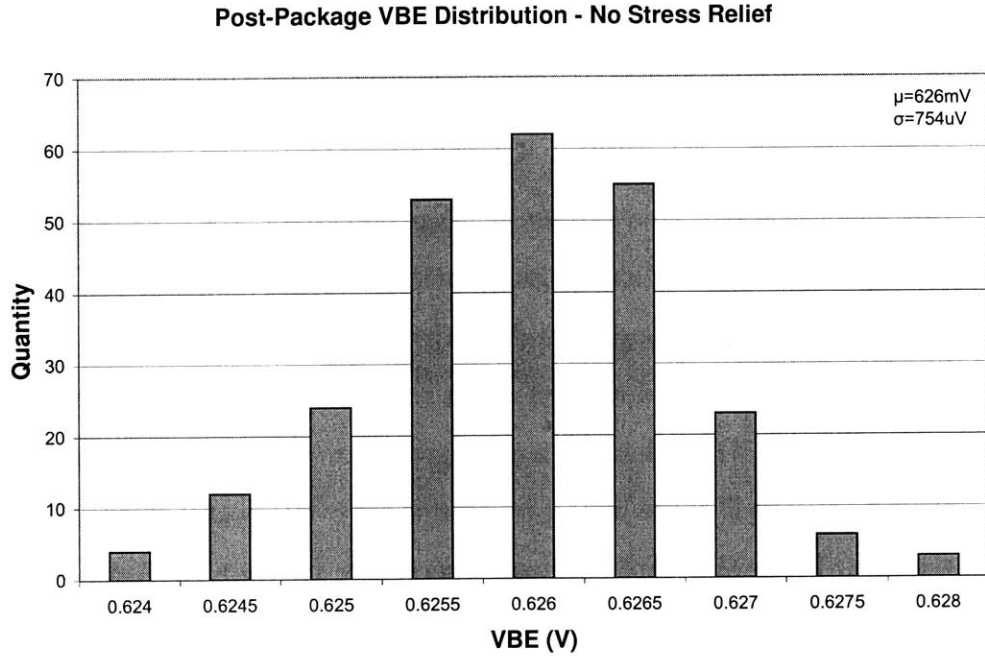
Figure 5-2: Room Temperature Post-Package V_{BE} Distribution - No Stress Relief

5.3.2 Analysis

These four plots show that stress relief tightens both the V_{BE} and ΔV_{BE} distributions, but not nearly as much as was expected from the V_{REF} experiments. The V_{BE} distribution without stress relief has a minimum value of 623.6mV and a maximum of 627.9mV with a standard deviation of 754uV. The V_{BE} distribution with stress relief has a minimum value of 624.9mV and a maximum of 628mV, with a standard deviation of 485μV.

The ΔV_{BE} showed less change with and without stress relief. The ΔV_{BE} distribution without stress relief had a minimum of 63.05mV and a maximum of 63.94mV with a standard deviation of 186μV. The ΔV_{BE} distribution with stress relief has a minimum value of 63.25mV and a maximum of 64.16mV with a standard deviation of 168μV.

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Post-Package VBE Distribution - Stress Relief
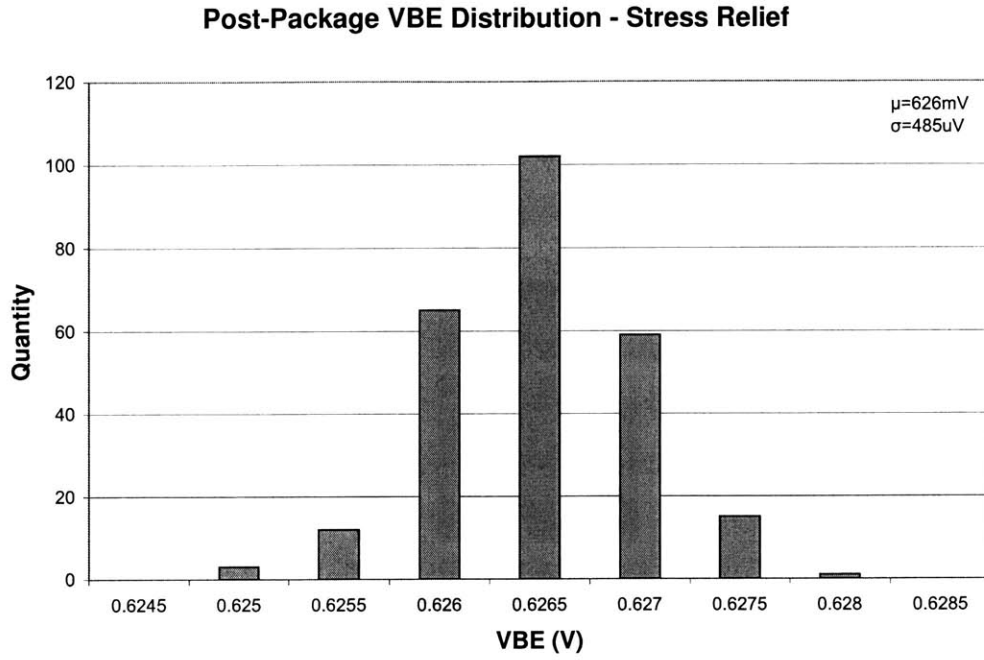
Figure 5-3: Room Temperature Post-Package V_{BE} Distribution - Stress Relief

Post-Package DeltaVBE Distribution - No Stress Relief
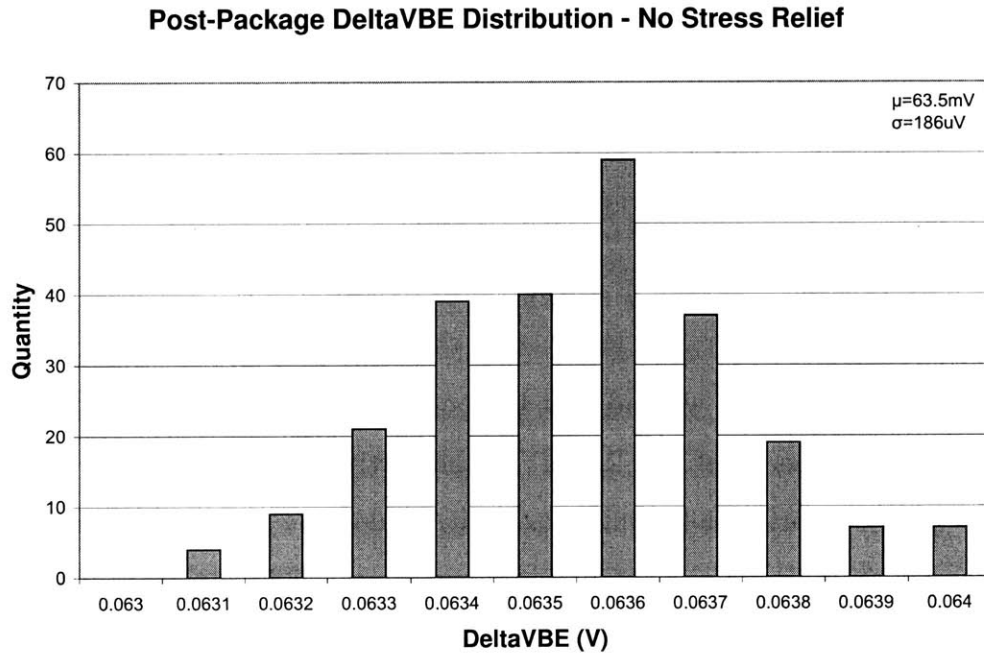
Figure 5-4: Room Temperature Post-Package ΔV_{BE} Distribution - No Stress Relief

Post-Package DeltaVBE Distribution - Stress Relief
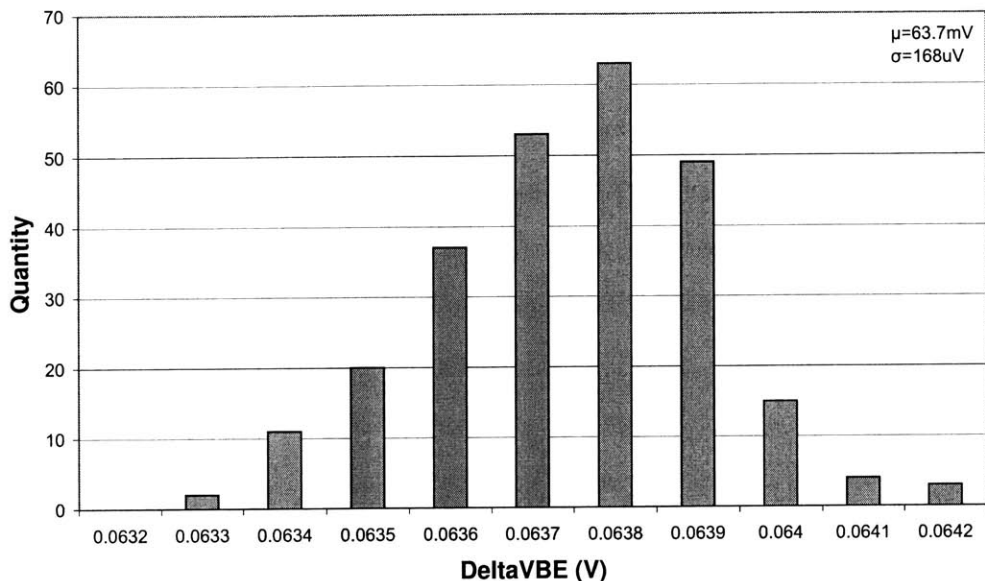
Figure 5-5: Room Temperature Post-Package ΔV_{BE} Distribution - Stress Relief

While the ΔV_{BE} results in less absolute variation, its variation is more important when analyzing the bandgap cell. The ΔV_{BE} is amplified by a factor of 10 to form the 1.2V V_{REF}. To find the standard deviation that would be seen in V_{REF}, we need to add the variances - the square of the standard deviation.

$$\sigma^2_{VREF} = \sigma^2_{VBE} + 10^2\sigma^2_{\Delta VBE} \tag{5.1}$$

Using this calculation, we find that the post-package standard deviation in V_{REF} is 1.75mV with stress relief and 2.01mV without stress relief. While we do not have pre-package wafer sort data for our test circuit, we do have pre-trim pre-package wafer sort data for the references of the previous experiment. These plots suggest that the standard deviation in V_{REF} before trimming or adding packaging stress is between 1.5 and 2mV.

This information suggests that while stress relief does tighten a V_{REF} distribution,

it *should not* yield major improvement in this particular cell. ΔV_{BE} variation dominates the V_{REF} variation; however, stress relief yielded only mild improvements to the ΔV_{BE} distribution. Nonetheless, this information does provide design insight. Suppose that instead of a 12x-1x bandgap core, we used a 48x-1x core or a 99x-1x core. With a 48x-1x core, the amplification needed to create a 1.2V V_{REF} is 6, and with a 99x-1x core, this necessary amplification is 5. With a 48x-1x core, the extrapolated post-package standard deviation with and without stress relief will be 1.11mV compared to 1.34mV variation without stress relief. Similarly, with a 99x-1x core, the extrapolated post-package standard deviation with and without stress relief will be 0.97mV compared to 1.20mV without stress relief. These extrapolations do not take into consideration second-order effects such as bond wire resistance variation. A 5mA quiescent current flows through the GND bond wire, causing an extra V_{REF} variation equal to $I_Q \Delta R$.

This experiment suggests that while stress-relief tightens the V_{BE} and ΔV_{BE} distributions, these distribution changes are not sufficient to explain the 3x V_{REF} distribution tightening. Furthermore, this data suggests that the fundamental bandgap core is fairly stress-resistant, and the parts without stress relief should not have shown the extreme distribution widening seen in the previous chapter.

5.3.3 Experimental Justification

Through this thesis, we assumed that the resistors are stress-resistant. However, any mismatch in the load resistors will cause errors in both the measured V_{BE} and ΔV_{BE}. A mismatch in the load resistors will lead to one transistor getting more than half of the tail current, modifying the current ratio I_{C1}/I_{C2} and therefore ΔV_{BE}. Since the total tail current is constant, the amount of current through the 1x transistor is guaranteed to change, again causing an erroneous V_{BE} measurement.

The temperature sensitivity of the parameters under test (V_{BE} and ΔV_{BE}) complicated the measurements in this chapter. V_{BE} varies by about -2mV/°C

or -200μV/0.1°C. For the 12x-1x bandgap core, ΔV_{BE} varies by 214μV/°C or 21.4μV/0.1°C. Controlling the temperature to 0.1°C was not possible within the oven, let alone in room temperature tests. Rather than controlling the temperature to such a resolution, efforts were made to ensure that the temperature variation was slow, and an accurate temperature measurement accompanied V_{BE} and ΔV_{BE} measurements.

To generate an effective comparison between parts with and without stress relief, the testing procedure needed to collect data in a manner such that an appropriate normalization could be performed after the test. However, since this portion of the experiment involved hand-testing 500 parts, the testing procedure could not be too time-intensive. This ruled out taking the measurements inside a oven regulating temperature to 27°C. The oven itself only is able to regulate temperature to ±0.1°C, and this strategy would require the parts to be soaked in the oven setting for some time.

Instead of using the oven to regulate temperature, we used the air-conditioning system and two temperature sensors to gather enough data for a post-testing normalization. First, the precision thermistor was used to measure the temperature of the ambient air directly above the IC. The thermistor suggested that the ambient temperature was surprisingly well-controlled, varying slowly by ±1°C. Such a change would cause a negligible change in V_{REF} measurements of last chapter, but would cause a ∓2mV change in V_{BE} and a $\pm214\mu$V change in ΔV_{BE}.

While the thermistor provided an excellent measure of the instantaneous ambient temperature, it proved to be a poor measure of the instantaneous die temperature. This could be easily seen by noting a quick increase in the thermistor resistance when the air conditioning unit audibly turned on. Only after a few minutes later would the IC under test show a related rise in V_{BE} and fall in ΔV_{BE}. This is directly attributable to the small amount of air flow across the chip. The chip itself is encapsulated within the plastic socket with only a small air hole near the top. By contrast, an oven with a fan circulating air within the chamber would heat the IC under test much differently.

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Despite these difficulties, we can use the fact that the ambient temperature and die temperature varied only slowly to our advantage. This experiment was broken into 14 testing groups of approximately 35 parts each, which we will designate as *blocks*. Using the thermistor to track ambient temperature showed that the temperature during each block of testing did not vary too greatly (usually 1°C or less). By making the assumption that the die temperature variation is smaller than the ambient temperature variation, because of the thermal capacitance associated with the package-socket apparatus, we can say that each block of 35 parts was tested at nominally the same die temperature. This cannot be found from the thermistor which tracks the ambient temperature variation. Instead, the mean ΔV_{BE} for each block of 35 parts is used as a temperature sensor showing the die temperature for the particular group of tests. Afterwards, the 14 blocks can be normalized in relation to each other, to take into account the differing mean temperature. This normalization procedure makes a assumption that the mean I_S ratio for each set of 35 parts is equal. This assumption is valid considering the small standard deviation in ΔV_{BE} for each individual rail.

5.3.4   Normalization Procedure

The V_{BE} measurements required two normalizations. First, the tail current of the differential pair was determined by a single on-chip resistor. The absolute value of this resistance varied from part to part, causing the I_C to vary from part to part. We normalized all V_{BE} to a tail current of $5\mu A$ as shown below.

$$V_{BEN} = V_{BEM} + V_C \tag{5.2}$$

$$V_{BEN} = V_T \ln\left(\frac{5\mu A}{I_S}\right) \tag{5.3}$$

$$V_{BEM} = V_T \ln\left(\frac{I_{CM}}{I_S}\right) \tag{5.4}$$

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$$V_C = V_{BEN} - V_{BEM} = V_T \ln\left(\frac{5\mu A}{I_S}\frac{I_S}{I_{CM}}\right) = V_T \ln\left(\frac{5\mu A}{I_{CM}}\right) \tag{5.5}$$

Here, V_{BEM} represents the measured V_{BE} and V_C is the correction voltage we will add to account for part-to-part I_C variation to determine a normalized V_{BEN}. I_{CM} is the measured tail current, derived from measurements of V_E and R_{TAIL}.

After normalizing for V_{BE} collector current differences, we normalize for the block-to-block temperature differences. As explained in the previous section, the temperature variation within the block is not particularly significant, but the block-to-block temperature differences are significant. The average temperature within a block is found by finding the average ΔV_{BE}, and back-extracting the temperature using the relation

$$\Delta V_{BE} = \frac{kT}{q}\ln(12) \tag{5.6}$$

After finding the mean temperature for each block, the normalization center for the distribution is chosen as the average of these mean block temperatures. Using the difference between the block temperature and normalization center, we can choose a correction factor to add to all the parts within the block. The correction factor must be chosen such that it does not overwhelm the distribution shape. V_{BE} shows an approximately linear relationship of -2mV/°C. We formulated a correction factor

$$V_{BEN2} = V_{BEN} + \kappa V_C \tag{5.7}$$

$$V_C = (-.002)(T_M - T_C) \tag{5.8}$$

$$\kappa = 0.5 \tag{5.9}$$

Here, V_{BEN} is the value of V_{BEM} after being normalized for tail current variation. V_{BEN2} is the value of V_{BE} after normalizing for temperature. V_C represents the error

caused by a temperature variation from the mean. This temperature variation is given by $T_M - T_C$ where T_M is the measured block temperature, and T_C is the normalization center. Finally, κ is the fitting parameter, chosen such that the correction voltage does not alter the distribution disproportionately.

ΔV_{BE} data does not need to be normalized for tail current, since the value depends on the ratio of currents through Q1 and Q2, not the total current through these transistors. However, ΔV_{BE} also should be normalized for temperature, just like the V_{BE} data. We again assume that the block temperature did not significantly change during the testing of each block, and that the mean ΔV_{BE} for each block can accurately represent the temperature. Put another way, we are assuming that the mean I_S ratio of Q1 and Q2 is the same for every block. Considering that the ratio of standard deviation to mean is about 0.25% for every block, this seems to be a good approximation. Again, we add an attenuated correction factor, such that the correction voltage does not overwhelm the distribution shape. ΔV_{BE} shows a very linear relationship of 214uV/°C. We formulated a correction factor as

$$\Delta V_{BEN} = \Delta V_{BEM} + \kappa V_C \tag{5.10}$$

$$V_C = (.000214)\,(T_M - T_C) \tag{5.11}$$

$$\kappa = 0.5 \tag{5.12}$$

Repeated for comparison are the original V_{BE} and ΔV_{BE} distributions and the distributions with temperature normalization. As can be seen, the temperature correction serves to slightly tighten the distributions, but does not disturb the overall shape.

Post-Package VBE Distribution - No Stress Relief

Figure 5-6: Room Temperature V_{BE} Distributions With and Without Temperature Correction - No Stress Relief

Post-Package DeltaVBE Distribution - No Stress Relief

Figure 5-7: Room Temperature ΔV_{BE} Distributions With and Without Temperature Correction - No Stress Relief

Post-Package VBE Distribution - Stress Relief
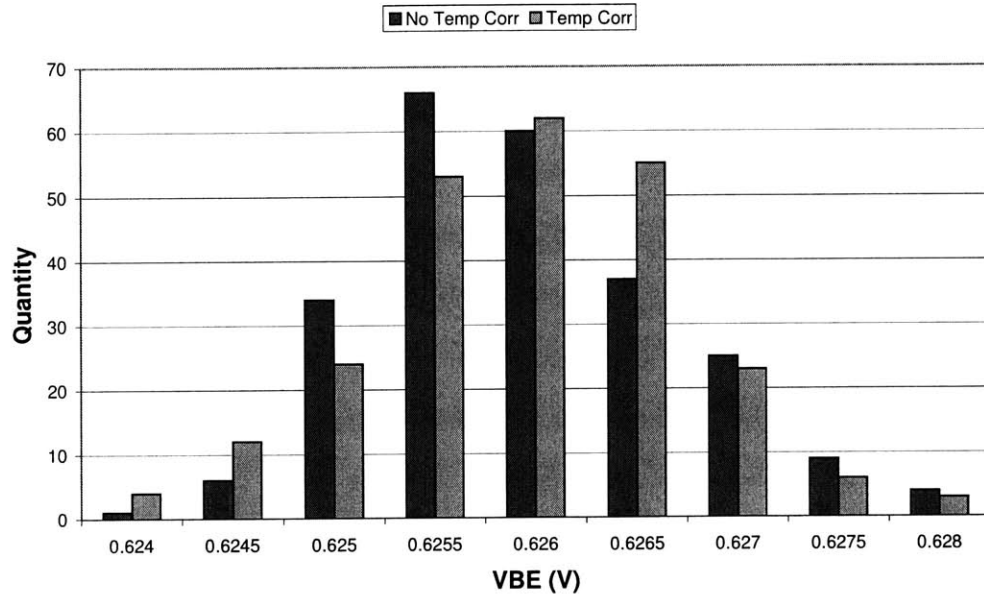
Figure 5-8: Room Temperature V_{BE} Distributions With and Without Temperature Correction - Stress Relief
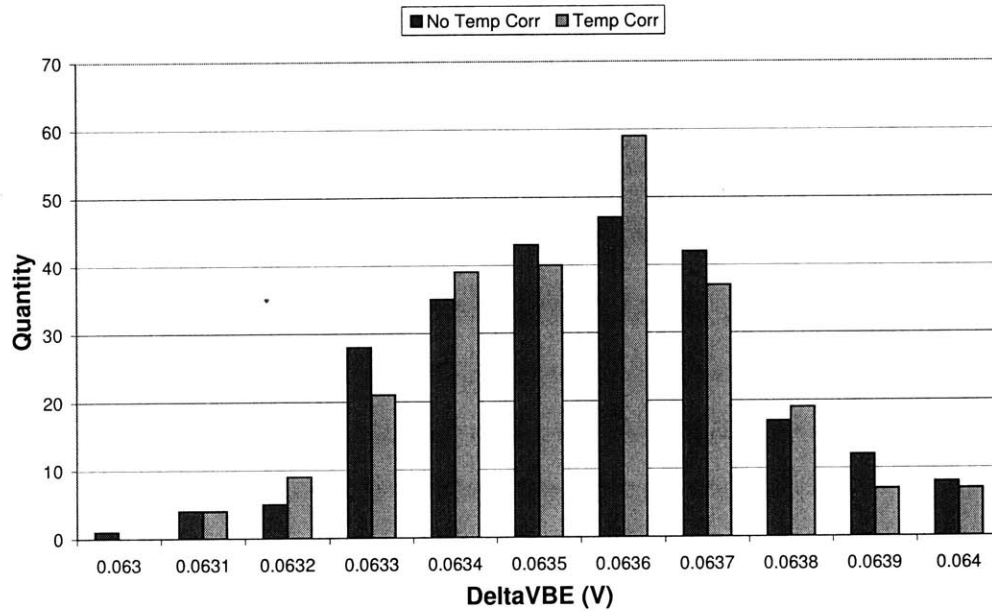
Post-Package DeltaVBE Distribution - Stress Relief

Figure 5-9: Room Temperature ΔV_{BE} Distributions With and Without Temperature Correction - Stress Relief
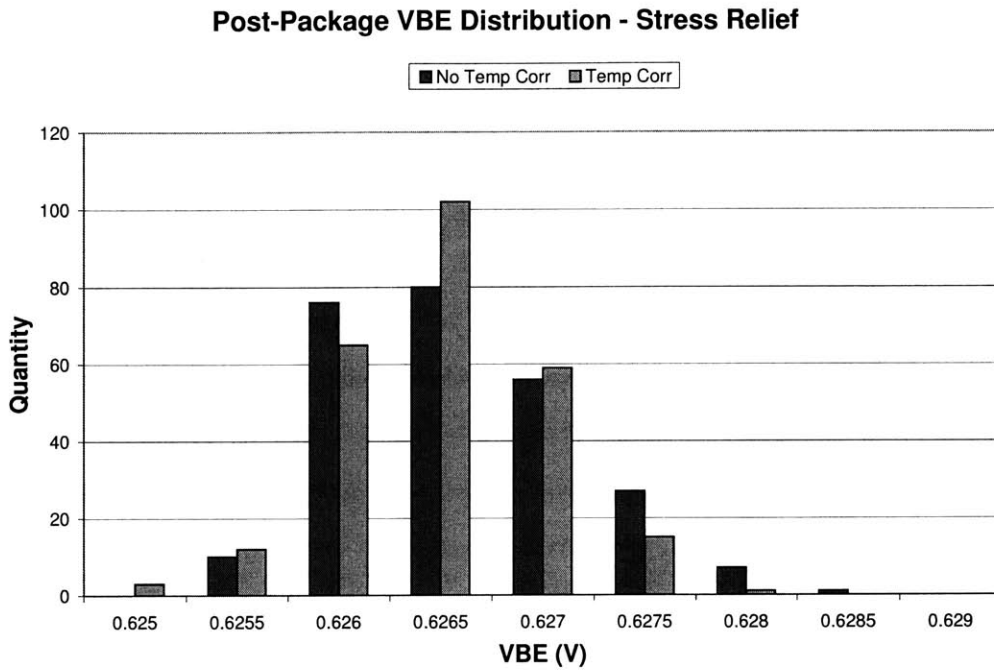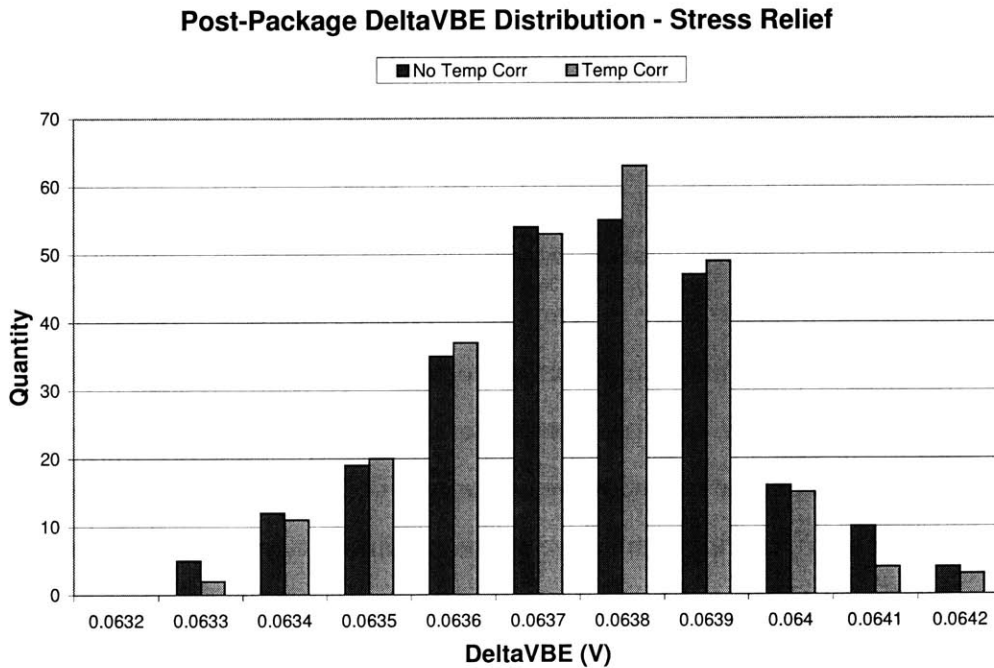
5.4 Temperature Characterization

After generating the room temperature V_{BE} and ΔV_{BE} distributions for parts with and without stress relief, we measured the temperature characteristics of a representative part in each group. In this experiment, we can qualitatively compare the V_{BE} temperature curvature for parts with and without stress relief. In addition, we can extract the optimum magic voltage of a first-order reference and the bandgap parameters E_{G0r} and η. Finally, we examine the linearity of the ΔV_{BE} vs T relation.

5.4.1 Experimental Setup

For the temperature characterization, the IC under test was soldered to one side of a PCB board. The support circuitry (op-amp, external bandgap, etc) were mounted on the reverse side of the PCB board. This setup is shown in Figures 5-10 and 5-11. A precision thermistor, shown at the right side of Figure 5-10, was suspended directly over the IC during testing. Finally, the entire setup was wrapped tightly in bubble wrap before being placed in the oven.

Due to the sensitivity of the parameters under test, the temperature characterization of V_{BE} and ΔV_{BE} was more difficult than the similar characterization performed on a completed bandgap cell. V_{BE} in particular is very temperature sensitive, dropping by approximately $200\mu V$ per $0.1°C$ change in temperature. Stated another way, a $0.1°C$ uncertainty in temperature leads to a $200\mu V$ uncertainty in V_{BE}, which translates to a 3% uncertainty in a room temperature V_{BE} value of 650mV.

While this uncertainty does not preclude a qualitative picture of the V_{BE} vs T relation, it does complicate quantitative extraction of E_{G0r} and η. By extracting these parameters, we are obtaining a measure of the nonlinearity of V_{BE} - a parameter that is known to be fairly linear. Indeed, first-order bandgap references operate on the premise that the nonlinearities present in V_{BE} are small enough to enable a low temperature coefficient over a broad operating range.

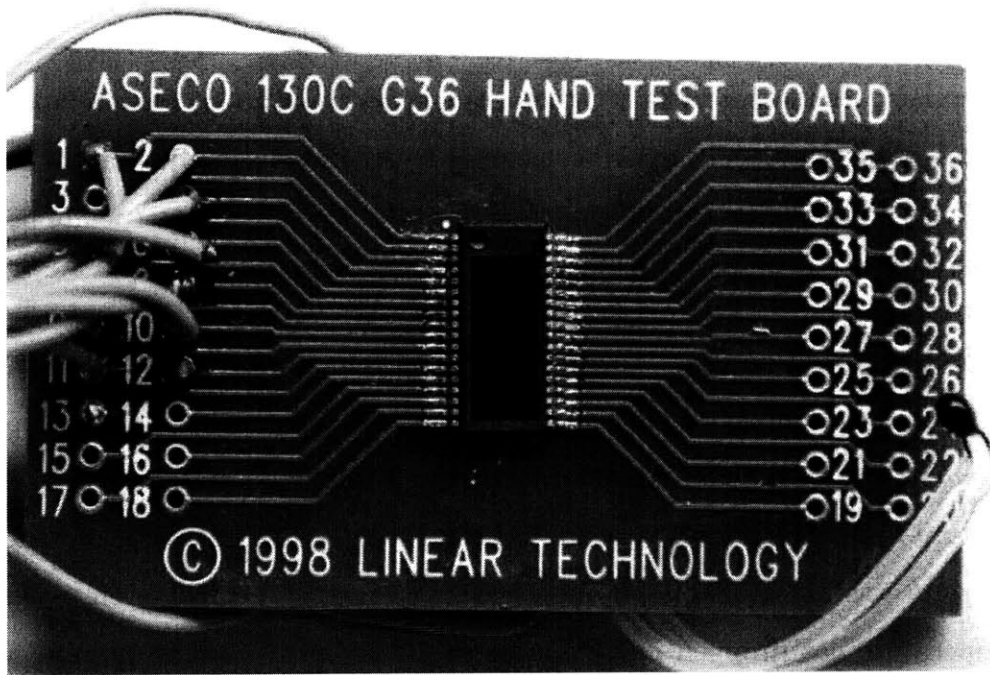The temperature sensitivity of V_{BE} and ΔV_{BE} demanded a thermometer capable

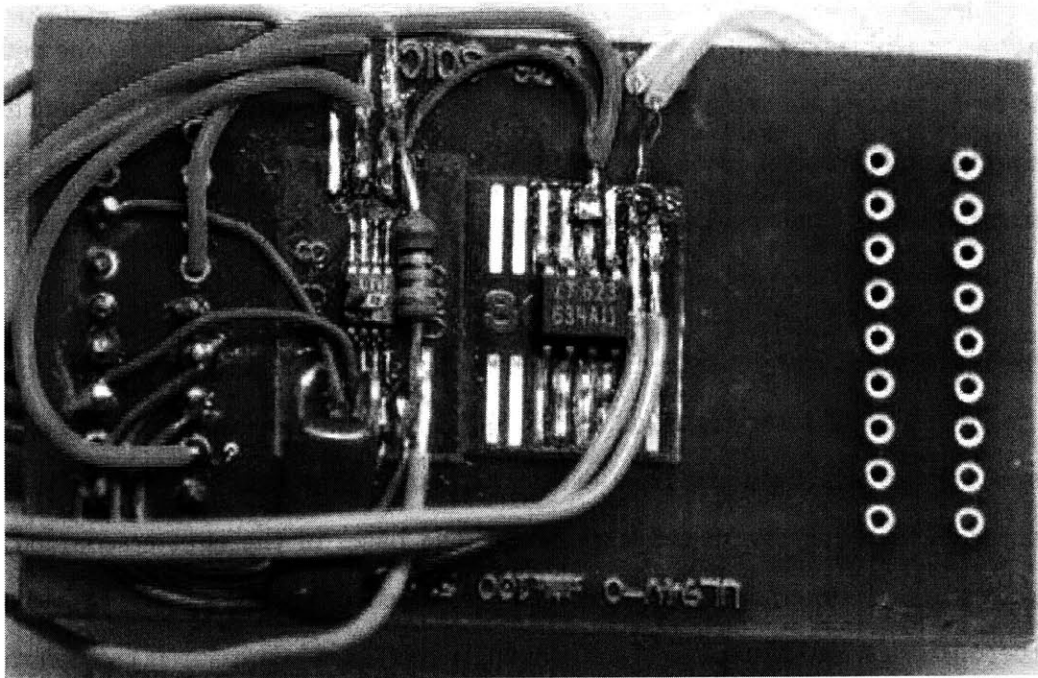Figure 5-10: Test Board for Temperature Characterization

Figure 5-11: Test Board for Temperature Characterization - Support Circuitry

of extremely fine resolution. Again, we used the Yellow Springs Instruments (YSI) 44100 thermistor, which has a resistance of 100kΩ at room temperature and 0.1% initial accuracy. To measure a 0.01°C temperature deviation about room temperature, our resistance measurements must be accurate to 45Ω resolution, making the wiring resistance negligble. Using this thermistor's R vs T table, we can interpolate between adjacent (R, T) pairs to obtain temperature accuracy to within 0.01°C.

In addition to an accurate thermometer, the temperature characterization attempted in this experiment requires an extremely precise oven. If the oven is not able to regulate temperature to a fine resolution, there will be a mismatch between the die temperature and ambient temperature measured by the thermistor. Unfortunately, such an oven was not available for these measurements. When the oven senses that the temperature has dropped below its set-point, the heater turns on, and hot air circulates through the chamber. When the oven senses that the temperature has risen above its set-point, the heater turns off, and the temperature in the chamber begins to drop. In a sense, the oven is analogous to a switching regulator, providing temperature ripple instead of voltage ripple. In a switching regulator, one reduces ripple by increasing the output capacitor. In an oven, we added thermal capacitance by wrapping the circuit in bubble wrap. By adding bubble wrap and giving the parts a 30 minute settling time to adjust to temperature steps, V_{BE} and ΔV_{BE} measurements were stable to 10uV resolution.

Each part was individually measured from -30° to 100°C, using 20° intervals from -30° to 10°, and 15° intervals from 10° to 100°C. V_{BE} was measured by hooking the meter leads directly from the base of the 1x transistor to the emitter. ΔV_{BE} was measured by hooking the meter leads across the bases of the emitter coupled 12x-1x transistors. Temperature measurements consisted of measuring the resistance of the thermistor on the test board. A HP34401A multimeter measured the thermistor resistance. The range of the multimeter was set to use a small excitation current to avoid self-heating effects while still achieving reasonable resolution.

The tail current in the differential pair is approximately PTAT and positive TC. In the data below, V_{BE} was normalized for a tail current of 5μA. The normalized V_{BE} and ΔV_{BE} temperature curves are presented as Figures 5-12 and 5-13. Since the temperature accuracy is 0.01°C, and V_{BE} changes -2mV/°C, the error in the V_{BE} measurements is at most 20uV. Since ΔV_{BE} only changes 214uV/°C, the error in the ΔV_{BE} measurements is set by the minimum resolution of 10uV.

Temperature Characterization - VBE
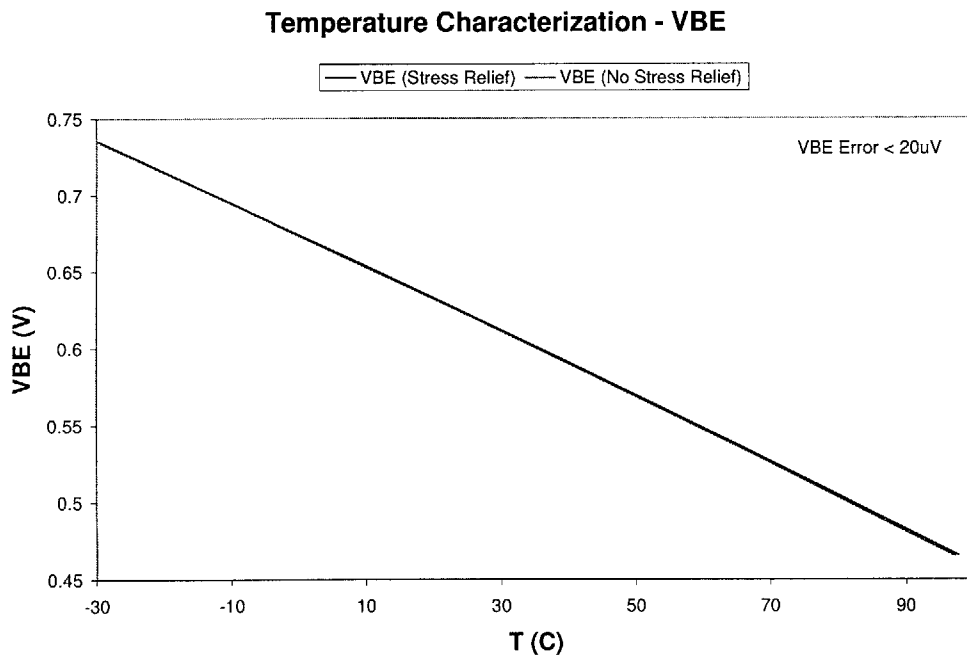
Figure 5-12: V_{BE} vs T

5.4.2 Analysis

As Figure 5-12 shows, both parts (with and without stress relief) have fairly linear V_{BE} temperature characteristics. The part without stress relief shows more curvature at higher temperatures, suggesting a higher value of η. Figure 5-14 plots the incremental slopes between each data point. This plot shows that both parts have similar slopes at lower temperatures, but at higher temperatures, the absolute value incremental slope is higher in parts without stress relief. This suggests a higher value of η in parts

Temperature Characterization - DeltaVBE
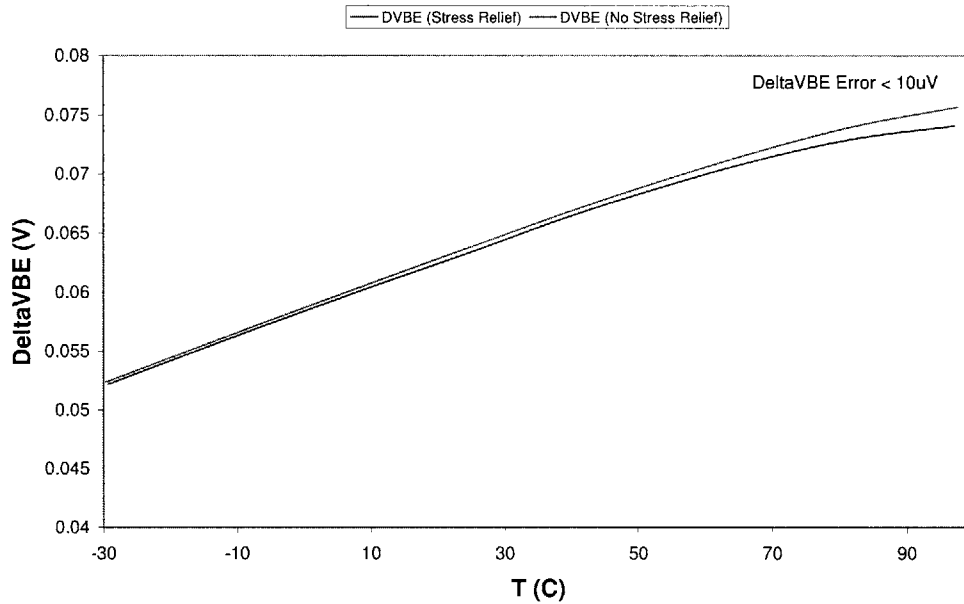
Figure 5-13: ΔV_{BE} vs T

without stress relief.

The optimum "magic" voltage for a first order reference can be found by extrapolating the V_{BE} vs T relation to absolute zero using a line tangent to the room temperature value. The slope of the tangent line is chosen as the average of the incremental slope from -10° to 25°C and 25° to 40°C. This calculation gives a magic voltage of 1.246V for parts with stress relief and 1.248V for parts without stress relief. This is much higher than expected. For the bandgap under test, the first-order trim target was 1.220V, experimentally verified to have the best temperature coefficient. The curvature-corrected bandgap circuit has a slightly lower trim target of 1.216V leading to a negative TC first-order portion. Because the curvature correction pulls up V_{REF} at higher temperatures, the final curvature corrected bandgap has an optimal TC. Again, this trim target for the curvature corrected bandgap was experimentally verified to have the best TC performance.

Figure 5-13 shows that the slope of the ΔV_{BE} vs T relation drops at higher temperatures, and with this drop being more significant in the part without stress

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Incremental VBE Slope
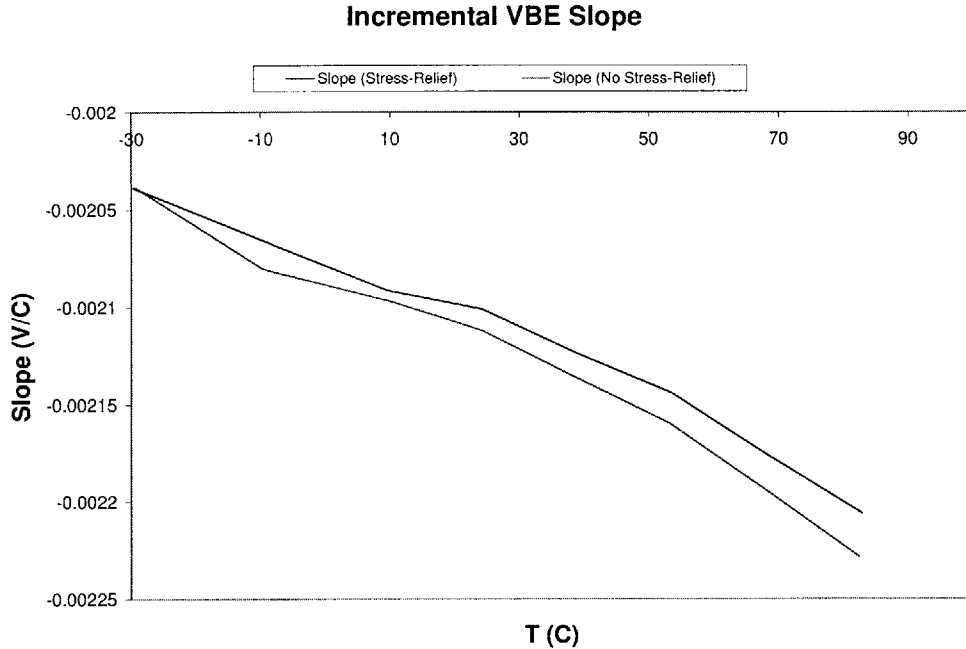
Figure 5-14: Incremental Slope of V_{BE} vs T

relief. This drop was unexpected and did not appear in simulations of the test circuit.

5.4.3 Extraction of E_{G0r} and η

We extracted E_{G0r} and η using two different temperature ranges: 40°C to 100°C and -30°C to 40°C. As mentioned before, the temperature characteristic of the bandgap energy of unstressed intrinsic silicon is parabolic at lower temperatures, as shown in Figure 2-2. Tsividis[1] references certain coefficients to describe parabolic temperature dependence below room temperature, and a linear temperature dependence above room temperature. Rather than use these coefficients in an E_{G0r} characterization derived from V_{BE} data, we assume that stress does not change the linearity of the E_G vs T curve at higher temperatures. By only using V_{BE} data taken at these higher temperatures, we can continue to assume that the E_G characteristic is linear in the region of interest. From this point, we can use equation 2.13 to solve for E_G and η.

$$V_{BE}(T) = E_{G0r} - \left(\frac{T}{T_r}\right)E_{G0r} + \left(\frac{T}{T_r}\right)V_{BE}(T_r) \tag{5.13}$$
$$- \eta\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right)\ln\left(\frac{I_C(T)}{I_C(T_r)}\right)$$

This equation can be solved for E_{G0r} and η by measuring V_{BE} and I_C at three temperatures. Designating the middle temperature as T_r, this results in two equations and two unknowns and can be solved analytically. Solving for E_{G0r} and η in this fashion will give the value of E_G extrapolated to absolute zero from T_r, which is not room temperature in this experiment. However, since we have assumed that stress does not change the linearity of the E_G vs T curve at higher temperatures, the value of E_{G0r} found will be the same as if it had been extrapolated from room temperature.

The odd behavior of ΔV_{BE} at higher temperatures brings into doubt the validity of these data points. For comparison, we also extracted E_{G0r} and η using the lower temperature values from -30°C to 40°C. Using these data points will mean that a slight error due to the curvature of $E_G(T)$ will enter into derived E_{G0r} and η. However, if the higher temperature data points are compromised, this E_{G0r} will be more reliable.

For our experiment, we have already normalized V_{BE} for collector current, so the term related to I_C will equal zero. We now express this equation in a form that will lead us to a multivariable regression.

$$y = \beta_1 x_1 + \beta_2 x_2 \tag{5.14}$$
$$T_r V_{BE}(T) - T V_{BE}(T_r) = (T_r - T)E_{G0r} - \eta\left(\frac{kTT_r}{q}\right)\ln\left(\frac{T}{T_r}\right) \tag{5.15}$$
$$y = T_r V_{BE}(T) - T V_{BE}(T_r) \tag{5.16}$$
$$x_1 = (T_r - T) \tag{5.17}$$
$$x_2 = -\left(\frac{kTT_r}{q}\right)\ln\left(\frac{T}{T_r}\right) \tag{5.18}$$
$$\beta_1 = E_{G0r} \tag{5.19}$$

	E_{G0r}	η	Adjusted R^2
No Stress Relief	1.02V	8.46	1
Stress Relief	1.05V	7.54	1

Table 5.1: Extracted E_{G0r} and η using 40° to 100°C

	E_{G0r}	η	Adjusted R^2
No Stress Relief	1.13V	4.55	1
Stress Relief	1.14V	4.08	1

Table 5.2: Extracted E_{G0r} and η using -30° to 40°C

$$\beta_2 = \eta \qquad (5.20)$$

A multivariable regression was performed using Microsoft Excel. The values of y, x_1, and x_2 are created using the measured V_{BE} and T values. T_r is chosen to be 70°C when analyzing the experimental range from 40°C to 100°C. T_r was chosen to be 10°C when analyzing the experimental range from -30°C to 40°C. The coefficients are then found using a least-squares regression in Excel. The extracted values of E_{G0r} and η for each temperature range are given in tables 5-1 and 5-2.

When using the higher temperature data points, the extracted value of E_{G0r} is much lower than the commonly assumed values around 1.18V, while the extracted value of η is much higher than the commonly assumed values around 3.5. This may be because these parameters are extremely sensitive to small variations in the measured temperature and V_{BE}. For example, assume that instead of using a multivariate regression, we measured V_{BE} at three temperatures (40, 70, 100°C) to extract the parameters E_{G0r} and η. Designate the V_{BE} error in the measurement at 40°C as ΔV_{BE1}. The ΔE_{G0r} and $\Delta \eta$ as a function of ΔV_{BE1} are given below.

$$\frac{\Delta E_{G0r}}{\Delta V_{BE1}} = \frac{T_1 T_3 \ln\left(T_3/T_1\right)}{T_3 \ln T_3 \left(T_2 - T_1\right) + T_2 \ln T_2 \left(T_1 - T_3\right) + T_1 \ln T_1 \left(T_3 - T_2\right)} \qquad (5.21)$$

$$\frac{\Delta\eta}{\Delta V_{BE1}} = \frac{q}{k} \frac{T_3 - T_1}{T_3 \ln T_3 (T_2 - T_1) + T_2 \ln T_2 (T_1 - T_3) + T_1 \ln T_1 (T_3 - T_2)} \quad (5.22)$$

Similar equations can be derived for the error terms due to V_{BE2} and V_{BE3}. The V_{BE} error terms are directly related to the uncertainty in the temperature measurements, and the sensitivity can only be reduced by using a larger temperature range. For example, a 50μV uncertainty in V_{BE} measurements induces a 25mV uncertainty in E_{G0r}. Similarly, a 50μV uncertainty in V_{BE} measurements leads to an uncertainty of 1.0 (units) in η.

The ΔV_{BE} of the 1x-12x pair may also play a role in the increased curvature shown by this bandgap. The decrease in the ΔV_{BE} could be explained by an imbalance in the differential pair that caused the 12x transistor to draw a larger share of the tail current than the 1x transistor. This would mean the drop in the V_{BE} at higher temperatures was not only due to the natural curvature of V_{BE}, but also a less than 50% share of the 5μA tail current. The op-amp used has a low offset voltage drift of 30nV/C, which is not enough to induce a appreciable imbalance in collector currents. In addition, although the op-amp's input bias current increases with temperature, it should not rise above 100pA at 100°C, again suggesting that this is not enough to unbalance the differential pair.

The data points using the cold temperature range show extracted values of E_{G0r} and η closer to accepted values. While these values include an error due to the curvature of $E_G(T)$, they do not include errors due to potentially-compromised high temperature data points. These extracted values suggest that the effect of packaging stress is to decrease E_{G0r} and increase η. Using the formula for magic voltage given by $V_{MAGIC} = E_{G0r} + kT_r/q * \eta$, we find that the magic voltage for parts with stress relief is 1.222V, while the magic voltage for parts without stress relief is 1.224V. Furthermore, a decrease in E_{G0r} and an increase in η both serve to decrease V_{BE}. Using this information, we would predict that parts without stress relief would see a mean negative shift in room temperature distributions and a net negative TC.

While the room temperature distributions of the operating bandgap did show that the parts without stress relief had more of a mean negative shift, the temperature characteristics of these parts were inconclusive with some parts showing net negative TCs and others showing net positive TCs. This may imply that stress is impacting some other portion of the circuit that is not appearing in the fundamental 2T cell.

5.5 Conclusions

These experiments offer a prediction into the behavior of a bandgap reference that is untrimmed at wafer sort and packaged in the SSOP package used in this thesis. First, the core transistors are fairly stress-resistant with and without stress relief. Stress relief offered almost a 2x room temperature distribution tightening in V_{BE}, but less clear gains in the ΔV_{BE} distribution. Furthermore, it was shown that the ΔV_{BE} variation was actually the dominant factor in the extrapolated V_{REF} performance. Finally, it was shown that parts without stress relief have a lower E_{G0r} and higher η. Previous researchers also found that stress reduced the bandgap voltage of silicon. The change in η could mean that the intrinsic carrier concentration temperature dependence or the mobility temperature dependence changed. Since stress breaks the periodicity of the silicon lattice, we might expect a change in the mobility temperature dependence due to the lattice scattering effect.

Chapter 6

Conclusion

6.1 Summary

In this thesis, we investigated the packaging effects on precision bandgap references used in an LTC switcher. In addition, by pinning out the transistor terminals, we investigated the packaging effects on the fundamental NPN transistor characteristics in the bandgap core. By comparing the performance of a control group that used the normal manufacturing cycle with the performance of the experimental group with a proprietary stress relief mechanism, we were able to characterize both the effectiveness of stress relief and the magnitude of stress-induced performance decrease.

The first experiment investigated the room temperature performance of a functioning precision reference used in the LTC switcher under test. In this experiment, it was found that the addition of stress relief tightened the room temperature distribution by a factor of three. Since the stress relief mechanism only alleviates stress from above the die, and the mean package shift was approximately the same for the both groups, this experiment concluded that the die attach was mainly responsible for the mean offset of -2mV. Finally, the fact that stress relief dramatically tightened the room temperature distribution suggests that stress from above the die play a major role in the random stress events that cause distribution

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widening.

The second experiment investigated the temperature characteristics of the functioning precision reference under test. In this experiment, it was found that the addition of stress relief led to more predictable and consistent temperature coefficients. Furthermore, it was found that the random stress events that caused the distribution widening had a somewhat chaotic effect on the temperature coefficients of parts without stress relief. Specifically, some parts that had low room temperature values showed positive TC behavior suggesting that random stress events caused a drop in the magic voltage for these parts. In addition, some parts that had high room temperature values showed negative TC behavior, suggesting that random stress events caused an increase in the magic voltage for these parts. Efforts to find interfering factors turned up no suspects, leading to the conclusion that these temperature coefficients were a result of random extreme stress events.

After the first and second experiments, we concluded that the stress relief mechanism was very effective in reducing the random stress events. The third experiment investigated the room temperature distributions of the fundamental NPN transistors in the 2T core of the bandgap reference. Specifically, the V_{BE} and ΔV_{BE} of the 2T core was examined in a configuration similar to that of the functioning reference. While the V_{BE} distribution for the control group without stress relief was wider than the for the experimental group with stress relief, this widening was not sufficient to explain the widening in the functioning precision reference. Furthermore, while the absolute ΔV_{BE} distribution widening was only slightly larger in the control group without stress relief, ΔV_{BE} distribution widening was found to have a larger impact on the functioning precision reference due to the fact that ΔV_{BE} was scaled by 10 in the functioning reference. This experiment suggests that precision references with larger ΔV_{BE} will be more stress resistant, due to the smaller scaling factor required.

Finally, the fourth experiment investigated the temperature characteristics of the

NPN transistors. In this experiment, it was found that parts without stress relief had lower E_{G0r} and higher η than parts with stress relief. This made intuitive sense since prior experiments have established that stress decreases E_{G0r} of an NPN. In addition, the higher η value suggests that stress is breaking the periodicity of the lattice and changing the temperature dependence of mobility. The higher value of η means that even after a post-package trim to a new "sweet-spot", a first order reference without stress relief will always have a worse TC than one with stress relief. In addition, in this experiment, it was found that the magic voltages for parts with and without stress relief were similar to within 2mV.

6.2   Further Research

There are many avenues for further research in this field. For example, the lateral and vertical PNP transistors can be examined in identical fashion to the experiments in Chapter 5. Since holes are the important carriers in these devices, the results may not be identical. Furthermore, lateral PNPs are known to be less stress resistant than vertical PNPs. Quantifying this difference would yield design knowledge that designers could use when designing various analog building blocks such as references and op-amps.

Throughout this thesis, we assumed that the resistors were stress-resistant. Using the test chip, we could prove or disprove this assumption, again measuring the room-temperature and temperature coefficients of resistors with and without stress relief. Finally, the stress resistance of NMOS and PMOS could be examined, again in a similar manner as the experiments in Chapter 5.

In this thesis, packaging effects were examined by packaging the die and then examining distributions. An alternative scheme, used by researchers at Delft[3][11][12], is to precisely apply stress to a silicon beam and measure the characteristics. One possible experiment would be to measure NPN characteristics using both the packaging method used in this thesis and using the precise application

of stress to the silicon beam. Comparison of these characteristics would yield an estimate of the magnitude of the stress induced by the packaging process.

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