Effects of Mechanical Properties on the Reliability of Cu/low-*k* Metallization Systems

by

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ABSTRACT

Cu and low-dielectric-constant (k) metallization schemes are critical for improved performance of integrated circuits. However, low elastic moduli, a characteristic of the low-k materials, lead to significant reliability degradation in Cu-interconnects. A thorough understanding of the effects of mechanical properties on electromigration-induced failures is required for accurate reliability assessments.

During electromigration inside Cu-interconnects, a change in atomic concentration correlates with a change in stress through the effective bulk modulus of the materials system, B, which decreases as the moduli of low-k materials used as inter-level dielectrics (ILDs) decrease. This property is at the core of discussions on electromigration-induced failures by all mechanisms. B is computed using finite element modeling analyses, using experimentally determined mechanical properties of the individual constituents. Characterization techniques include nanoindentation, cantilever deflection, and pressurized membrane deflection for elastic properties measurements, and chevron-notched double-cantilever pull structures for adhesion measurements.

The dominant diffusion path in Cu-interconnects is the interface between Cu and the capping layer, which is currently a Si_3N_4-based film. We performed experiments on Cu-interconnect segments to investigate the kinetics of electromigration. A steady resistance increase over time prior to open-circuit failure, a result of void growth, correlates with the electromigration drift velocity. Diffusive measurements made in this fashion are more fundamental than lifetime measurements alone, and correlate with the combined effects of the electron wind and the back stress forces during electromigration-induced void growth. Using this method, the electromigration activation energy was determined to be 0.80 ± 0.06eV.

We conducted experiments using Cu-interconnects with different lengths to study line length effects. Although a reliability improvement is observed as the segment length decreases, there is no deterministic current-density line-length product, jL, for which all segments are immortal. This is because small, slit-like voids forming directly below vias will cause open-failures in Cu-interconnects. Therefore, the probabilistic jL_{crit} values

obtained from via-above type interconnects approximate the thresholds for void nucleation. The fact that $jL_{crit,nuc}$ monotonically decreases with B results from an energy balance between the strain energy released and surface energy cost for void nucleation and the critical stress required for void nucleation is proportional to $\sqrt{B}$.

We also performed electromigration experiments using Cu/low-k interconnect trees to investigate the effects of active atomic sinks and reservoirs on interconnect reliability. In all cases, failures were due to void growth. Kinetic parameters were extracted to be $(Dz^*)_{0,eff} = 3.9 \times 10^{-10} m^2/\sec$ and $z^* = 0.40 \pm 0.12$, where $D_{0,eff}$ is the pre-factor for the effective diffusivity, and z^* is the effective valence. Quantitative analysis demonstrates that the reliability of the failing segments is modulated by the evolution of stress in the whole interconnect tree. During this process, not only the diffusive parameters but also B play critical roles. However, as B decreases, the positive effects of reservoirs on reliability are diminished, while the negative effects of sinks on reliability are amplified.

Through comprehensive failure analyses, we also successfully identified the mechanism of electromigration-induced extrusions in Cu/low-k interconnects to be near-mode-I interfacial fracture between the Si_3N_4-based capping layer and the metallization/ILD layer below. The critical stress required for extrusion is found to depend not only on $\sqrt{B}$ but also on the layout and dimensions of the interconnects. As B decreases, sparsely packed, wide interconnects are most prone to extrusion-induced failures.

Altogether, this research accounts for the effects of mechanical properties on all mechanisms of failure due to electromigration. The results provide an improved experimental basis for accurate circuit-level, layout-specific reliability assessments.

Thesis Supervisor: Carl V. Thompson
Title: Stavros Salapatas Professor of Materials Science and Engineering

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Chapter 1

Introduction

The integrated circuit (IC) is one of the fundamental technological building blocks of our modern society. The lineage of this engineering marvel can be traced to the first planarized and transistorized semiconductor chip made by Robert Noyce and Gordon Moore of Fairchild Semiconductor Corp. in 1960. Ever since the IC industry's genesis, rapid growth and stringent demands for performance have become the benchmarks for success. This progress has rigorously followed the predictions of the Moore's law [Moo 65]: the packing density of the ICs has doubled in every two years or less (see Figure 1.1).

Si is the semiconductor of choice for IC fabrication. As a result of the advancements in front-end IC processes, such as, photolithography, ion implantation, oxidation, and dopant diffusion, hundreds of millions of transistors, resistors, and junctions can be packed into a one square inch area in a state-of-the-art microprocessor or a non-volatile memory device. The topological challenge of wiring these circuit elements together is enormous. Fortunately, engineers have established various multi-level metallization schemes in the back-end of the line (BEOL) area to meet such challenges. Some of the important BEOL unit operations include chemical mechanical polishing (CMP), electroplating, physical vapor deposition (PVD), and plasma-enhanced chemical

vapor deposition (PECVD). Today, a high-performance IC chip contains several kilometers of metallic wiring used for electrical signal and power distribution [ITR 06], called interconnects, which are tens of nanometers to a few microns wide, stacked into 9 to 11 layers (see Figure 1.2).
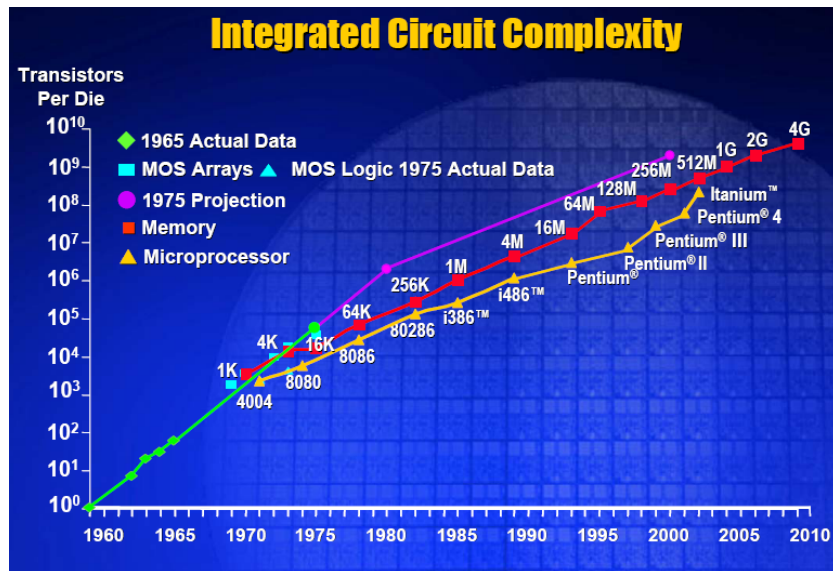
Figure 1.1 Moore's Law [Moo 03] – the exponential increase of IC packing density over time since the 1960's. The packing density is doubled in every two years or less.
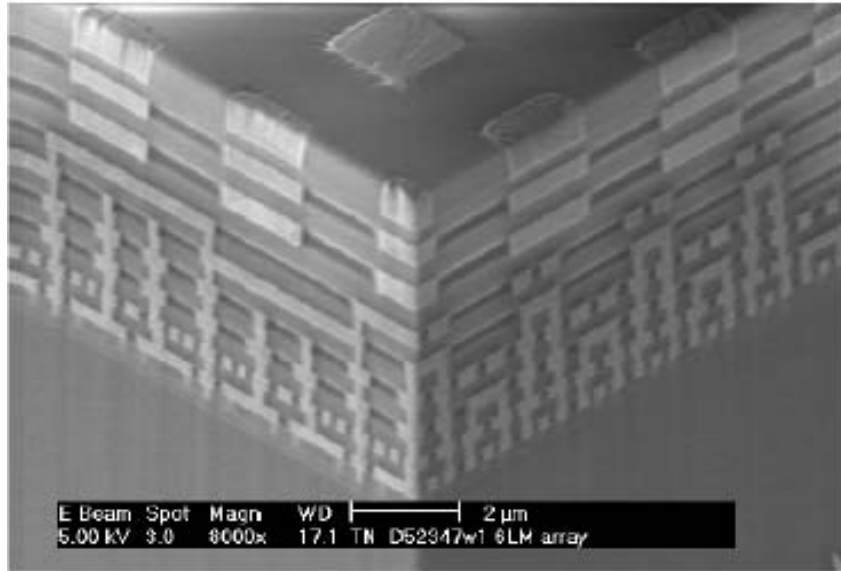
Figure 1.2 A cross-sectional view of a fully integrated chip from the 130nm technology node with 9-level dual-damascene Cu/low k interconnects [San 03].

Scientists have predicted that as the packing efficiency increases in an IC chip, the delay associated with the transistors, the gate delay, will continuously decrease, while the delay associated with the interconnects, the parasitic resistance-capacitance (RC) delay, will continuously increase and become dominant in performance budgeting [Boh 95] (see Figure 1.3). In order to minimize the RC delay, Cu and low-dielectric constant (k) inter-level dielectric (ILD) metallization schemes are becoming the preferred choice in fabrication of high-performance ICs, because the electrical resistivity of Cu is one of the lowest among metals, and low-k ILDs means low capacitances.
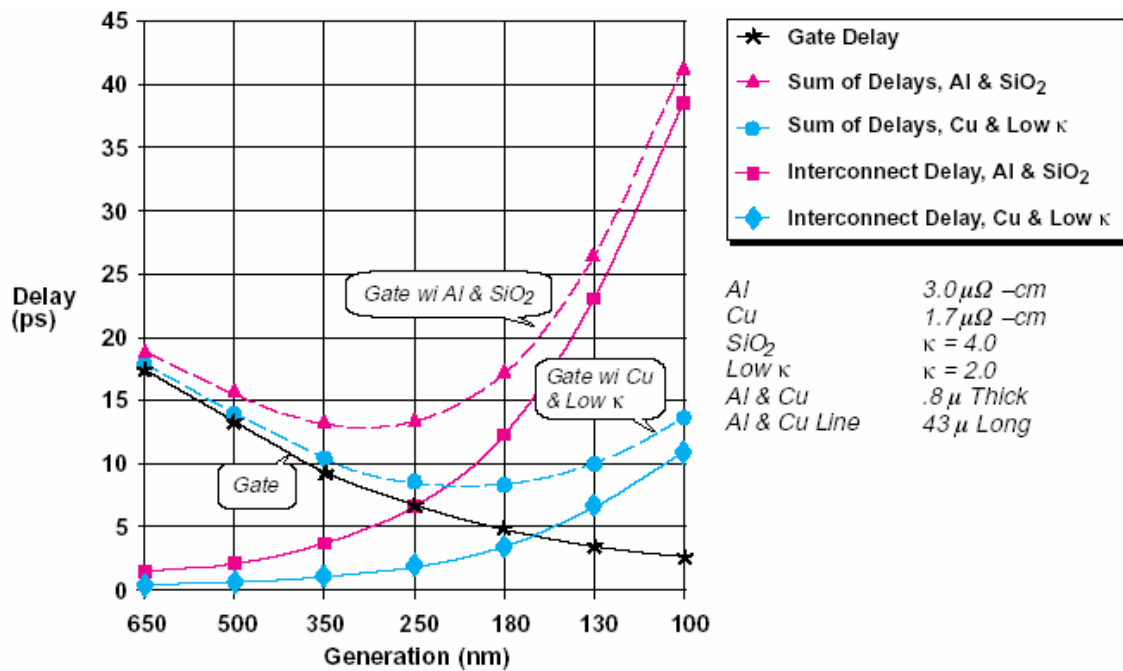
Figure 1.3 Calculated gate and interconnect delay versus technology generation [Boh 95]. Despite of the introduction of copper and the low-*k* ILD interconnect, the *RC* delay, rather than gate delay, will dominate for 130nm technology node and beyond.

Though the obvious reduction to the *RC* delays drives this change, current Cu/low-*k* technologies are facing reliability challenges with unknown solutions for future generations of ICs [ITR 06]. The operational current density inside the interconnects is ever increasing. Figure 1(a) shows that the maximum current density predicted in the *International Technology Roadmap for Semiconductors* (ITRS) in the year 2020 is close to 30MA/cm^2 [ITR 06], about 10 to 20 times the present day *accelerated* testing current density! Such a requirement for current density is due to the fact that while the interconnect dimensions need to decrease to accommodate the shrinkage of circuit elements, voltage levels will not drop accordingly. As more devices are packed together, the total length of the interconnects on a chip will also increase (see Figure 1(b)). Consequently, the reliability of a chip needs to improve at an exponential rate over time to ensure a tolerable failure rates, measured in FITs (see Figure 1.4(b)). By definition, 1FIT, a unit in failure rate, equals to 1 part per million per 1000 hours, or,

$1 \times 10^{-9} \dfrac{failure}{hour}$.
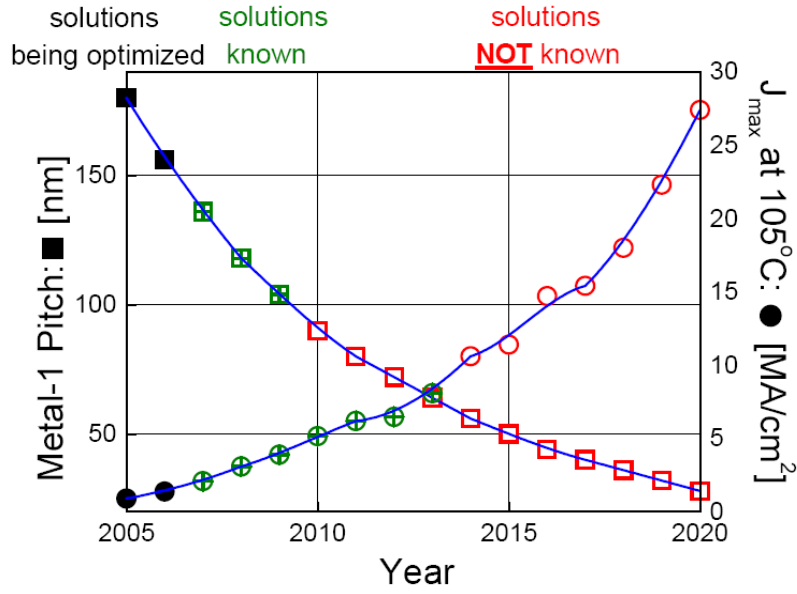
(a)
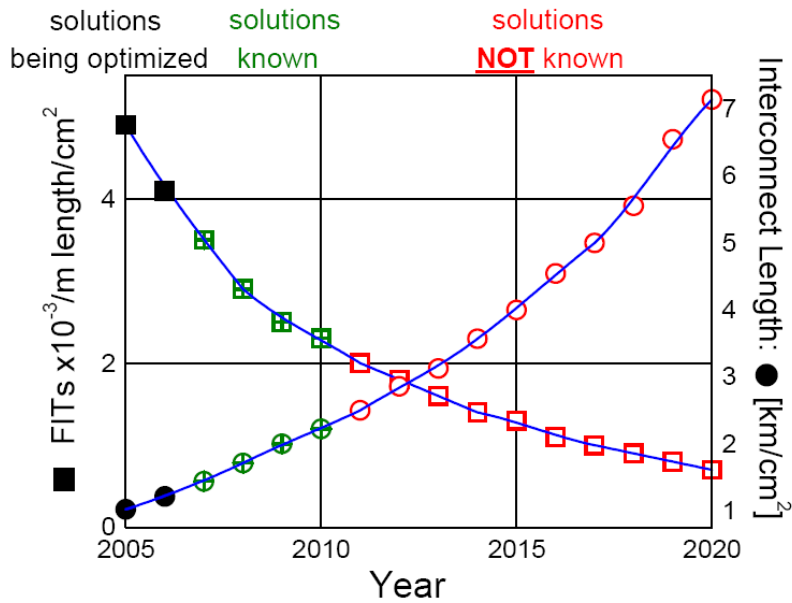
International Technology
Roadmap for Semiconductors, 2006 Update

(b)

Figure 1.4 Projections from the *2006 Update of ITRS* Interconnect Chapter [ITR 06].
(a) The interconnect dimension and maximum current density vs. future year; (b) the
tolerable failure rate and total interconnect length vs. future year. As indicated on the
figures, manufacturable solutions for many of the projected targets are still currently
unknown.

Such taxing operating conditions not only limit the degrees of freedom in circuit designs as well as the semiconductor processing widows, but also exacerbate the risks and rates for physical failures. One of the many major reliability concerns for interconnects has persisted in the past, and will remain for the future, is electromigration, which refers to current-induced atomic diffusion via a vacancy exchange mechanism due to momentum transfer from conducting electrons. This dissertation presents observations and discussions on electromigration-induced failures in Cu/low-k metallizations. This chapter reviews the basic concepts provide a background to the discussions in other chapters.

1.1 Electromigration and Korhonen Equation

1.1.1 Overview

The first scientific observation of electromigration is dated as early as 1861 [Ger 61]. However, this topic did not receive much attention from the engineering community until about a century later when small dimensions and high current densities inside chips would become synonymous with high-performance. Prior to the introduction of ICs, bulk wires were used for electrical contacts, in which less than 1% of $1MA/cm^2$ current density would produce sufficient Joule-heating to melt the metal. The dimensions of thin-film metallizations, however, provide a high enough surface-to-volume ratio to conduct the heat away through the Si substrate, an excellent thermal conductor. This enables 2 to 3 orders of magnitude increase in current densities to be carried. As a result, the copious flow of conducting electrons scatters frequently with metal atoms vibrating around lattice positions. (The room temperature phonon frequencies for metals are on the

order of 10^{13} Hz.) In turn, momentum is transferred from the electrons to the atoms. If vacancies are present, the atoms diffuse along the electron wind direction by exchanging with vacancy positions. Therefore, the most prevalent diffusion paths for electromigration are those with the highest free volume and/or the weakest bonding amongst the atoms, such as grain boundaries in Al-based interconnects, or interfaces in Cu-based interconnects.

I.A. Blech pioneered the physical observations, by using scanning electron microscopy (SEM) as well as transmission electron microscopy (TEM), and the mathematical descriptions of electromigration inside Al thin film strips in the 1960's [Ble 67a, Ble 67b, Ble 69]. Over the decades that followed, other investigations contributed to the library of knowledge on electromigration. Two observations are still relevant to the state-of-the-art Cu/low-k interconnects: the Blech length effect [Ble 76] and Black's equation [Bla 67]. The Blech length effect refers to a critical jL product exists, where j is the current density, and L is the interconnect segment length, below which electromigration would not induce damage (reasons are shown later). Black's equation is,

$$ttf = Aj^{-n} \exp(\frac{E_a}{kT}),$$
(1.1)

where A is a pre-exponential factor, E_a is the activation energy required for diffusion, k is Boltzmann's constant, T is temeperature, and n is the current density exponent. Though empirical in nature, not only Black's equation is useful in extrapolating lifetimes from accelerated testing conditions to service conditions, but also can give insights into the

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physics of the failures. When *n* is 1, failures are void growth limited; and when *n* is 2, failures are void nucleation limited [Llo 91c, Kir 91, Kor 93].

1.1.2 Mathematical Description

In the early 1990's, a thorough mathematical description of electromigration began to emerge, which was first proposed by M.A. Korhonen *et al.* [Kor 93], along with J.J. Clement and C.V. Thompson [Cle 95]. The derivations of the relevant concepts are summarized below.

In an elastically confined interconnect segment, the conducting electrons exert an electron wind force on the atoms, $z*q\rho j$, where ρ is the electrical resistivity, q is the fundamental charge, and $z*$ refers to an effective valence. The expression for the electron wind force stems from the classical expression for an electrical force on a point charge, $\vec{F} = q \cdot \vec{E}$. However, electromigrating metal atoms are electrically neutral. Here, $z*q$ is only a fictitious factor. Fundamentally, $z*$ has been suggested to be related to $n_e \cdot l_e \cdot \sigma_e$, where n, l, and σ represent the electron density, electron mean free path, and electron scattering cross-section, respectively, in the diffusion medium [Fik 59]. Estimates of $z*$ inside Al-based interconnects using quantum mechanical calculations have been reported by many [e.g. Doi 03, Sor 98]. However, first-principle-like computations are impossible for Cu interconnects due to the random nature of the diffusion path in Cu interconnects. For Cu/low-*k* metallizations, $z*$ can only be determined through experiments.

Under the electron wind force, metal atoms deplete near the cathode end, and accumulate toward the anode end. The changes in atomic concentration, C_a, at different positions inside the interconnect segment generate changes in the chemical potential.

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Since the diffusion is by a vacancy exchange mechanism, the chemical potential function can be expressed as $(\mu_0 + \Omega\sigma)$ [Her 50], where μ_0 is a reference potential, Ω is the atomic volume, and σ is the stress. Thermodynamically, the gradient of chemical potential, $\nabla\mu$, equaling to a force. A good approximation for an interconnect segment in 1–dimension is,

$$\nabla\mu = \Omega\frac{\partial\sigma}{\partial x}. \tag{1.2}$$

This force acts in the opposite direction to the electron wind force, therefore, is called the back stress force caused by the surrounding confinement. The more rigid the surroundings, the higher the back stress force would be generated inside an interconnect segment.

By recognizing the Nernst-Einstein relationship for drift velocity,

$$v_d = \frac{D}{kT}(F_{electron} + F_{back}) = \frac{D_{eff}}{kT}(qz*\rho j + \Omega\frac{\partial\sigma}{\partial x}), \tag{1.3}$$

the atomic flux can be written as

$$J_a = C_a \cdot v_d = \frac{D_{eff}C_a}{kT}\rho j z*q + \frac{D_{eff}C_a}{kT}\Omega\frac{\partial\sigma}{\partial x}. \tag{1.4}$$

C_a can be expressed as the difference between the lattice site concentration and the vacancy concentration [Cle 95] with appropriate stress dependencies,

$$C_a = C_l - C_v = C_{lo} \exp\left(-\frac{\sigma}{B}\right) - C_{vo} \exp\left(\frac{\Omega\sigma}{kT}\right), \qquad (1.5)$$

where and C_{lo} and C_{vo} are stress independent constants, and B, the effective bulk modulus of the interconnect system, relates a relative atomic concentration change, $\dfrac{dC_a}{C_a}$, to a change in stress, $\partial\sigma$ [Kor 93],

$$\frac{dC_a}{C_a} = -\frac{\partial\sigma}{B}. \qquad (1.6)$$

B is a function of the modulus and the dimensions of all the materials surrounding the metal, including the liner, the ILD, and the etch-stop capping layers, and can be determined using finite-element-method modeling (FEM) [Hau 00a]. Similar to Equation (1.5), D_{eff}, the effective diffusivity, which also depends on the stress, can be expressed as [Kor 93, Cle 95],

$$D_{eff} = D_0 \cdot \exp(-\frac{\Delta H}{kT}) \cdot \exp[(\frac{\Omega}{kT} + \frac{1}{B})\sigma], \qquad (1.7)$$

where D_o is the temperature independent pre-factor and ΔH is the electromigration activation energy. Finally, combing and substituting Equations (1.4) to (1.7) into the continuity equation for material transport,

$$\frac{\partial C_a}{\partial t} + \frac{\partial J_a}{\partial x} = 0, \tag{1.8}$$

a differential equation expressing the transient stress evolution in an interconnect segment is reached [Cle 95],

$$\frac{\partial \sigma}{\partial t} = \frac{\dfrac{\Omega}{kT} \dfrac{\partial}{\partial x}\left[D_v C_v \left(\dfrac{z^* q \rho j}{\Omega} + \dfrac{\partial \sigma}{\partial x} \right) \right]}{\dfrac{C}{B}\left(1 + \dfrac{B\Omega}{kT}\dfrac{C_v}{C} \right)}. \tag{1.9}$$

Due to its non-linearity, and the stress-dependence of D_{eff}, Equation (1.9) can only be solved numerically. We have developed a MatLab-based solver, XSim, at MIT, using the Backward Euler finite-discretization method to obtain numerically stable solutions for Equation (1.9) [Cho 04, Cho 07].

1.1.3 Definitions of Immortality

Figure 1.5 shows typical solutions to Equation (1.9) in a straight segment with zero-atomic flux boundary conditions. As time advances, the stresses eventually evolve toward a steady state, in which the electron wind force and the back stress force completely balance each other ($J_a = 0$), and the stress profile is linear, so that,

$$\Omega \frac{\Delta \sigma_{\max}}{L} = z^* q \rho j .$$

$$(1.10)$$

If neither the critical stress required for void nucleation, $\sigma_{crit.,nuc}$, nor the critical stress for metal extrusion, σ_{ext}, were reached before a force balance develops, the segment is immune to electromigration-induced damage and 'immortal.' Generally, $\sigma_{ext} > \sigma_{crit.,nuc}$, so that if the initial stress is zero everywhere in the metal line, the immortality condition relevant to void nucleation is,

$$jL < (jL)_{crit,nucleation} \equiv \frac{2\Omega \sigma_{crit,nuc}}{z^* q \rho} ,$$

$$(1.11)$$

which is often referred to as the Blech immortality condition, hence, the aforementioned Blech length effect [Ble 67b, Kor 93, Cle 95] (see Figure 1.5(a)).

If a void nucleates, it must grow to cause failure, and, depending on the robustness of the diffusion barrier, which can shunt the electron flow inside interconnects, and the location of the void, it may reach a relatively large size without

causing an open-circuit failure.   In this case, the resistance will increase as the void

grows.   Growth will eventually stop when an open failure occurs *or* when the

electromigration wind force is balanced by the back stress (see Figure 1.5(b)), whichever

happens first.   If a force balance develops before the resistance reaches an unacceptably

high value, the segment is still immortal.   This immortality criterion can also be

quantified in terms of a critical *jL* product [Fil 95] for dual-damascene Cu interconnects:

$$\left(jL\right)_{crit,saturation} < \frac{\rho/A}{\rho_l/A_l}\frac{\Delta R_{fail}}{R}\frac{2\Omega}{q}\frac{B}{\rho z^*}, \tag{1.12}$$

where ρ and ρ_l are the resistivity of the Cu and the diffusion barrier, respectively, and A

and A_l are the cross-sectional areas normal to the direction of electron flow of the Cu and

the refractory metal diffusion barrier, respectively. ΔR_{fail} is the maximum tolerable

change in resistance.
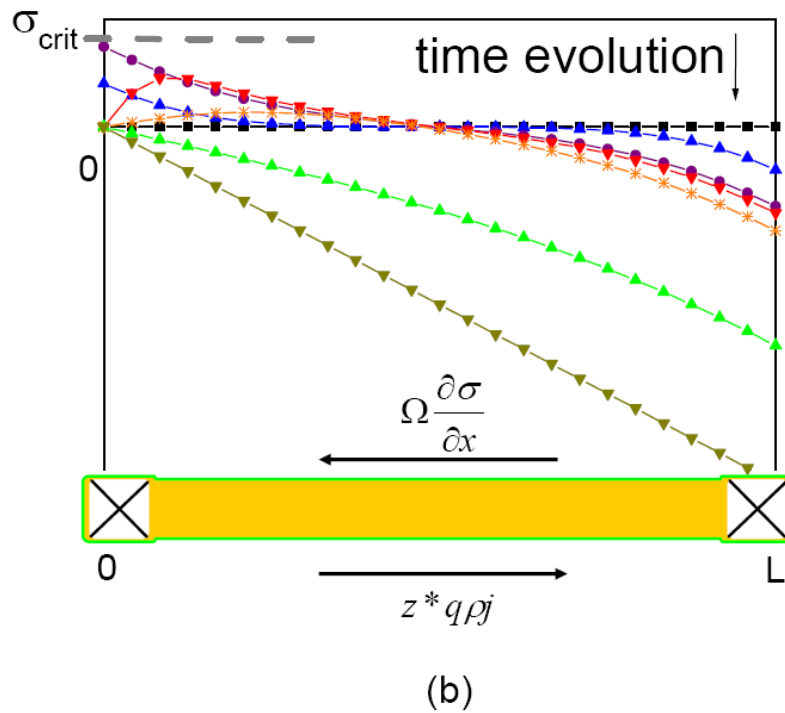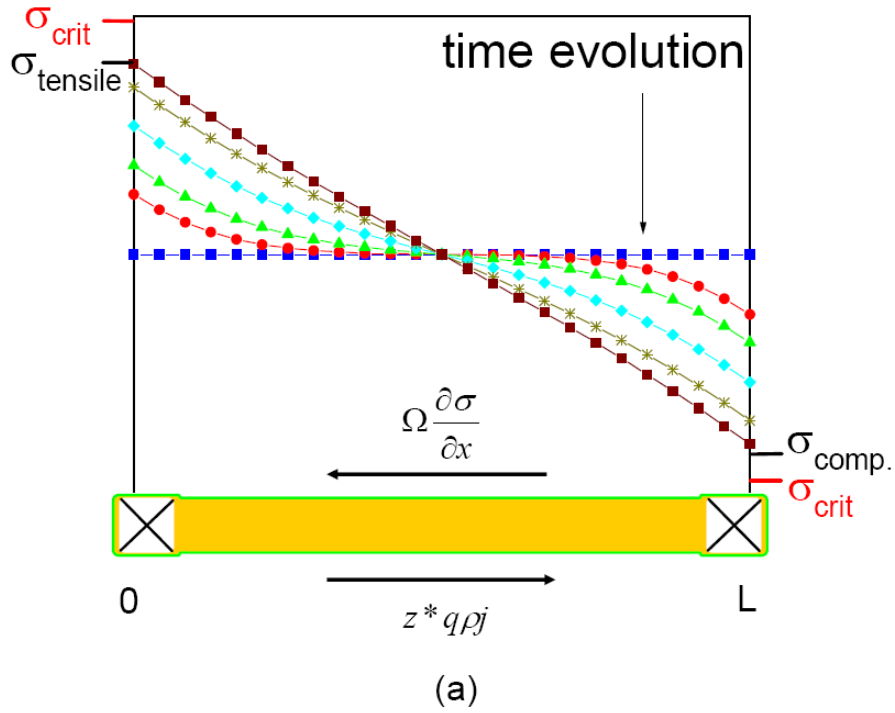
Figure 1.5 Typical solutions of the Korhonen equation for electromigration-induced stress development inside a straight segment (a) $\sigma_{crit.,nuc}$ when is not reached, and (b) when $\sigma_{crit.,nuc}$ is reached at the cathode end.

1.2 Cu/low-*k* Interconnect Architecture

In 1998, IBM fabricated the first commercially available IC chips containing Cu interconnects. Since then, Cu/low-*k* technologies have gradually replaced Al-based interconnects in high-performance ICs. Cu-based interconnects not only offer great reductions to the *RC* delay, but also hold the potential to be much more resistant to electromigration than Al-interconnects, due to the much higher melting temperature of Cu, which implies lower self-diffusion rates. However, this promise has not yet been fulfilled, because the dominant diffusion path in Cu-interconnects is the interface between Cu and the capping layer, currently, silicon nitride (usually the composition for this film is not stoichiometric, therefore, it is abbreviated as SiN) or SiN-based films, where the diffusivity is large, rather than the inside of the metal (such as the grain boundaries or the lattice), where the diffusivity is appreciably smaller. In order to further discuss this phenomenon, we must first become familiar with how Cu-based interconnects are fabricated.

1.2.1 Fabrication Procedures

Historically, damascening is the art of inlaying different metals into one another for decorative purposes. The English term comes from a perceived resemblance to the rich tapestry patterns of damask silk. The Cu-interconnect fabrication process earned this title, because Cu must be deposited and polished to remain isolated in pre-defined trenches. The results are inlay-like. Unlike the direct patterning process for Al interconnects, no known chemicals are able to etch Cu blanket films in an anisotropic

fashion to form the fine interconnect features that are required. Figure 1.6 illustrates the sequences of the dual-damascene process.

Low-k Film Deposition

First, a SiN/ILD/SiN film stack is deposited on Si substrate. SiN and SiO_2 films are deposited using PECVD at temperatures of 400°C or less in order to preserve the dopant concentrations inside the device layer in the Si substrate. However, deposition methods for low-k films can vary depending on the material and the manufacturer. ILDs deposited by PECVD are most commonly encountered in the IC industry because of good film thickness uniformity and coverage conformity. Some PECVD ILD examples include the '*Black Diamond*' family of ILDs (trade marked by Applied Materials, Inc.), the '*Coral*' family of ILDs (trade marked by Novellus), '*Z3MS*' (trade marked by Dow Corning), which are all variations of C-doped low-density SiO_2-based films with k ranging from 2.4 to 3.4, and the F-TEOS film, F-doped SiO_2 film using tetraethoxysilane as the PECVD precursor with k of >3.2. In the quest to further reduce k, one of the current research topics for PECVD low-k ILDs is to create nm-scaled pores by introducing organic pore-agents in the precursor, which are usually activated by heat and/or UV light curing after the deposition. Spin-on deposited ILDs are less favored in the IC industry production fabs due to less control over the film quality. Nevertheless, methyl-silsesquioxane (MSQ, trade marked by JSR Micro), which is a porous SiO_2 film incorporating methyl-groups with k of 2.2 to 2.4, an example of organic silicate glass, and 'SiLK' (trade marked by Dow Corning), which is an entirely C-based organic ILD with k of 2.6, are spin-on deposited films commonly encountered in the literature. Nearly all

low-*k* materials lower the *k* value by changing the density and/or the polarizability of the rigid Si-O covalent bond. However, all the efforts on reducing *k* also result in decreasing Young's moduli of the low-*k* films (see Figure 1.7). As later chapters will show, such changes also decrease the thresholds required for failure.
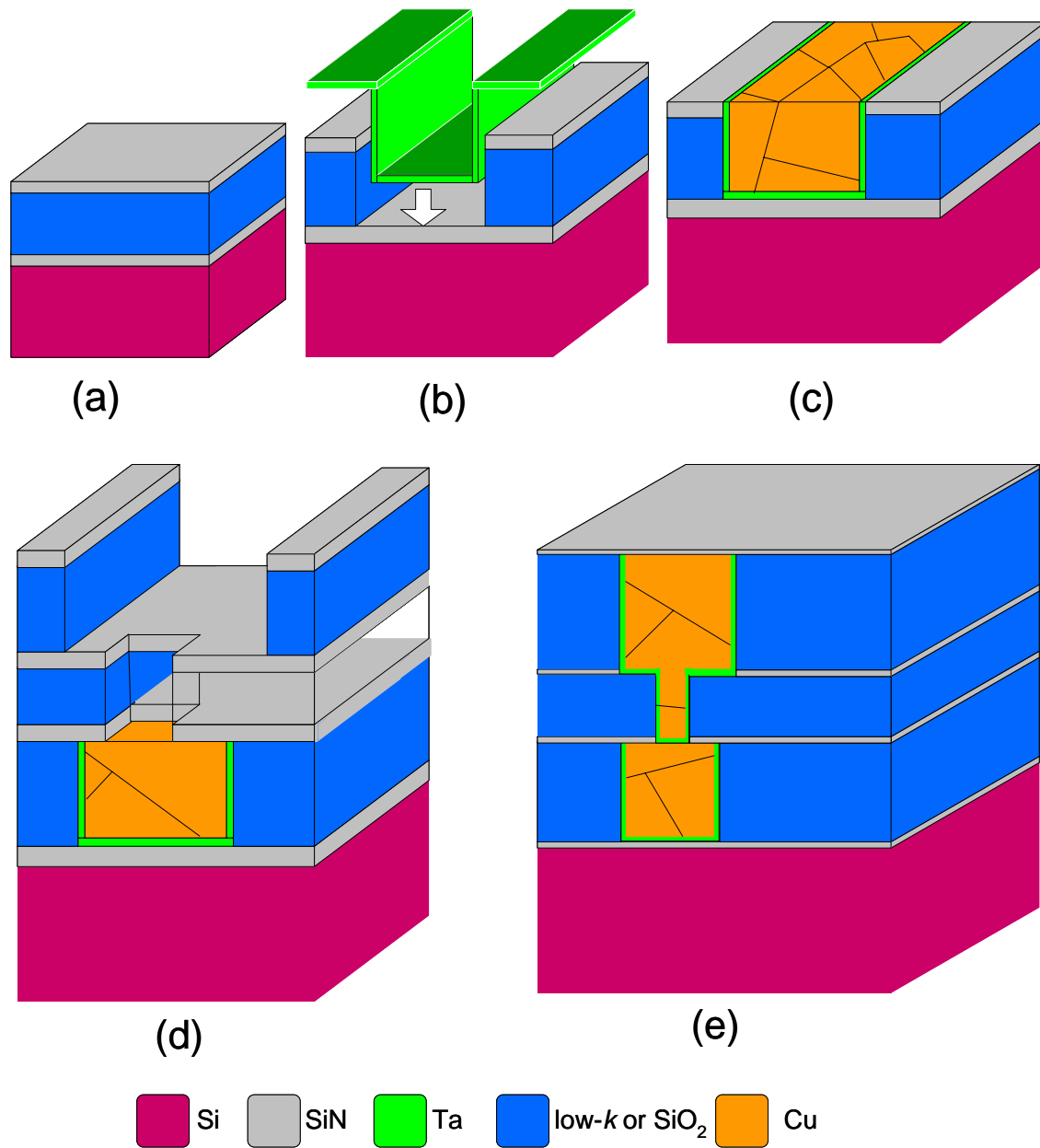
Figure 1.6 The dual damascene fabrication process for Cu interconnects. (a) deposition of SiN/ILD/SiN stack; (b) patterning and etching of the first level trenches, and sputter deposition of the Ta diffusion barrier as well as the Cu seed layer; (c) electrodeposition of Cu into the trenches, followed by CMP planarization of the top surface; (d) deposition of SiN/ILD stacks and etching for vias and second level trenches; (e) passivation of the top surface and fabrication of the second level Cu metallization.
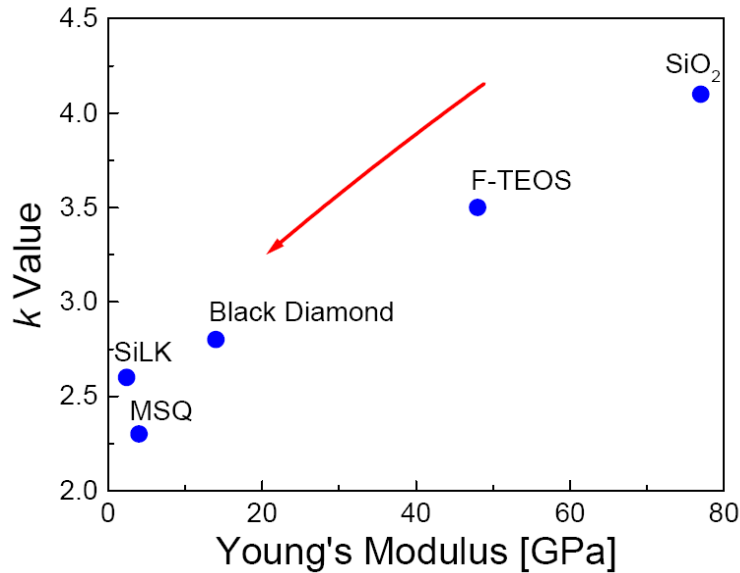
Figure 1.7 *k* vs. Young's modulus for commonly available low-*k* ILDs. As the value of *k* decreases, a nearly monotonically decreasing trend in the Young's moduli is seen.

<u>Patterning and Etching of Trenches</u>

After the SiN/ILD/SiN film stack deposition, the tri-layer film is patterned and etched using photolithography and reactive ion etching (RIE) methods to produce high-aspect-ratio trenches that define the interconnect layout. Presently, the IC industry requires a critical dimension of 45 to 90nm for the trenches. However, this dimension is projected to decrease according to Moore's law. Today, photolithography tools employ noble gas halides excimer laser sources that are in the ultraviolet (UV) range: ArF (λ=193nm) and KrF (λ=248nm). In order to decrease the dimensions of the exposed features, multiple beams of the coherent light are manipulated to interfere with each other to form patterns that are smaller than the wavelengths of the light sources (interference lithography). Furthermore, in order to increase the resolution, i.e., to decrease the numerical aperture, near-future IC lithography tools will employ liquid exposure mediums, with the index of refraction greater than 1, rather than air. However, photo-

lithography for the 22 to 16nm technology nodes and beyond will likely require extreme UV or X-ray sources, which can only be focused by using defect-free multilayer mirrors placed in high vacuum chambers. When such techniques become economically feasible, a fundamental change in lithography should be expected. As the dimensions get even closer to the quantum limit, new physical failure mechanisms may become important to affect reliability assessments of ICs.

After photo-developing, the RIE process uses the remaining photoresist film as a hard mask to etch the trenches. The plasma is generated under a low pressure, and ions are accelerated by electromagnetic fields toward the wafer surface to remove the material. Since the plasma is also chemically reactive, the sidewalls of the trenches are coated with its products as a protection during etching to achieve the anisotropic result.

Ta/TaN Diffusion Liner and Cu Seed Layer Deposition

Next, a film of 10-20nm thick Ta and/or TaN, serving as a diffusion barrier, followed by a thin layer of Cu (Cu seed layer) is sputter- or physical vapor-deposited. Depending on the deposition conditions, the residual stress in the barriers can be different. The ramifications of the intrinsic film stresses are explored in Chapter 3. Future ICs may require extremely high aspect-ratio trenches. The atomic layer deposition method (a form of CVD) is also being investigated as an alternative deposition method [Moo 05].

Cu Electroplating

Cu is subsequently electrodeposited onto the wafer surface. The main ingredients in commercially available electroplating baths consist of sulfuric and hydrochloric acids, and copper sulfate. However, the solutions also include proprietary inorganic and organic chemicals, known as levelers, brighteners, and accelerators, that inhibit dentridic surface morphologies, therefore promote uniform film growth and decreases surface roughness, and increase wetting properties. Consequently, less grain boundary grooving and micro-voids occur at the top surface. The overall advantages of electroplating deposition of Cu are the cost effectiveness and the uniform trench filling characteristics. Although the Cu/SiN interface is the dominant void nucleation site and fastest diffusion path inside Cu interconnects, understanding the Cu film microstructure is important in analyzing void growth and electromigration kinetics [Cho 07]. Furthermore, methods of suppression of the diffusion along Cu/SiN interface have been introduced [Lan 03]. Therefore, characterizing grain boundary diffusions, which is influenced by the microstructure, inside Cu-interconnects is also important for reliability assessment.

The microstructures of electroplated Cu films are found to have the following properties: the electroplating process produces extremely fine initial grain structures, less than 100nm in dimension [Lin 98]. However, over a period of hours to days, the Cu films transform to larger-grained structures via recrystallization and abnormal grain growth (see Figure 1.8). Thermodynamically, the driving force for recrystallization is the energy stored in grains due to defects. The high impurity concentration of the electroplating bath result in readily forming defects. Incoherent twin boundaries seem to be especially important. Experimentally, Walther *et al.* [Wal 00] presented observations

of much higher concentrations of (511) grains in (111) textured (the preferred texture for *fcc* metal films) electroplated Cu films prior to recrystallization than after, using X-ray analyses. In *fcc* structures, (511) grains result from twinning around a (111) plane. Having low stacking fault energies, Cu twins easily. Here, the strain energy associated with the two possible twin boundaries, incoherent (498mJ/m^2) and coherent (21mJ/m^2), is large. Therefore, the incoherent twin boundaries are the most likely driving force for recrystallization.

Kinetically, during and after recrystallization, some grains may grow at the expense of their neighbors. However, in electroplated Cu, this growth process is abnormal: a few grains grow extremely fast while other ones grow very little, and the statistical distribution of the grain sizes changes with time. To date, this behavior is not well-characterized. However, the main cause of abnormal grain growth is due to the additives, i.e., impurities, in the electroplating solution. During the growth, the impurities are segregated into the grain boundaries, and they impede grain boundary motion by exerting a solute drag. The grain boundary pinning forces are so great that further annealing after abnormal grain growth does not change the Cu films' microstructure [Hau 00b, Lin 98]. Empirically, the abnormal grain growth kinetics of Cu films can be fitted to the Johnson-Mehl-Avrami-Kolmogorov (JMAK) expression for phase transformations,

$$\xi(t) = 1 - \exp[-(\frac{t}{t_R})^{\alpha}], \qquad\qquad\qquad (1.13)$$

where, where ξ is the fraction of Cu that has transformed at time t, t_R is the characteristic recrystallization time, and α is the Avrami exponent. However, reports of α varies considerably from 1 by S.P. Hau-Riege *et al.* [Hau 00b], corresponding to a 2D diffusion-limited growth with a fixed number of sites (close to that suggested by *in-situ* TEM observations), up to >7.0 by Walther *et al.* [Wal 00], which has no physical correlation except to indicate a break-down of the JMAK theory in the presence of impurities. (α of 4 implies a 3D growth with a constant nucleation rate [Por 92].) Nevertheless, all studies show that the initial small grain size along with the strong pinning of grain boundaries by impurities, making it impossible to achieve a columnar grain structure in films or a true bamboo-like structure in interconnect trenches with electrodeposited Cu.
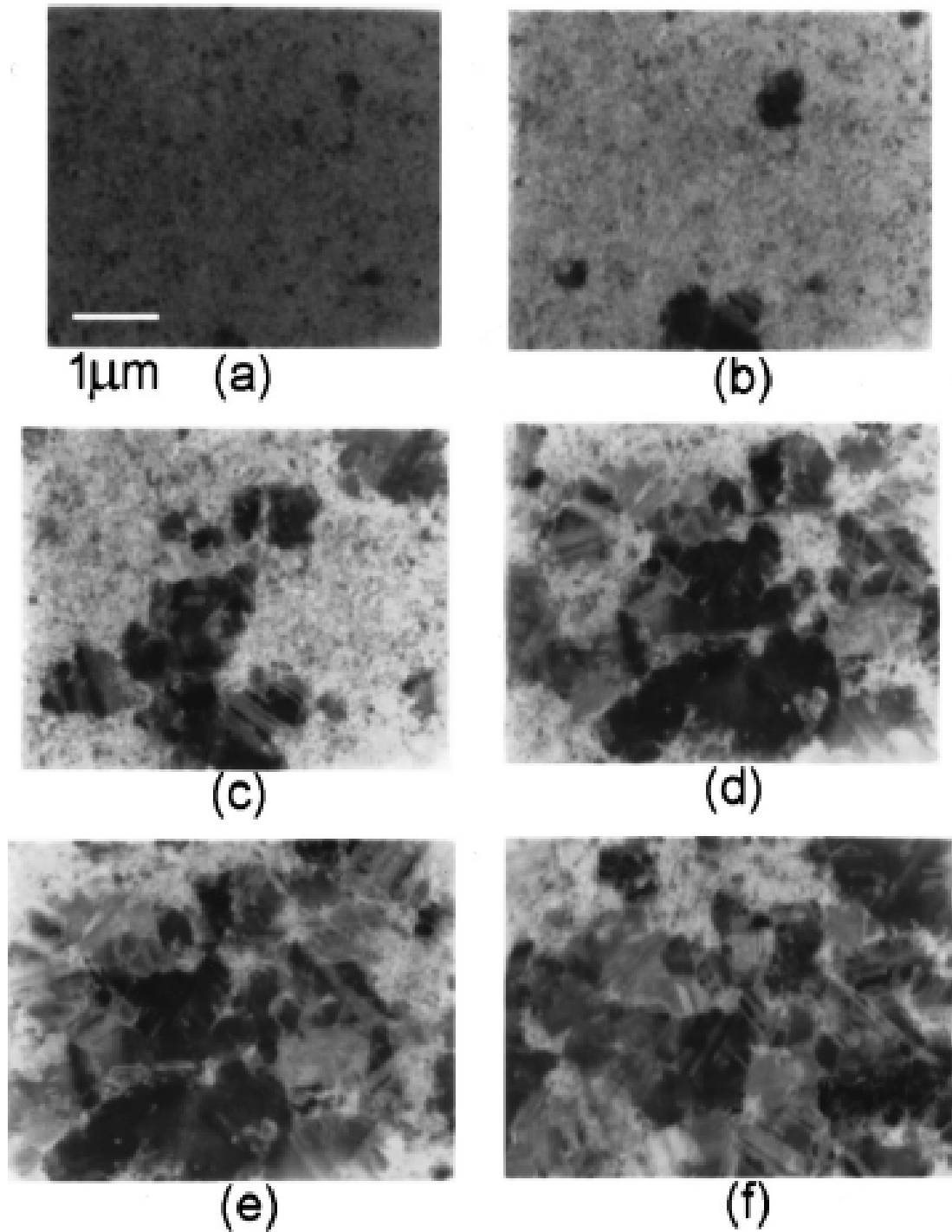
Figure 1.8 Series of TEM micrographs reported by S.P. Hau-Riege *et al.* for a 0.3μm thick electroplated Cu film transforming at room temperature (a) *t*=11min, (b) *t*=1hr, (c) *t*=2.5hr, (d) *t*=8hr, (e) *t*=23.5hr, and (f) *t*=80hr. After 80hr, no further transformation took place [Hau 00b].

Lastly, following Cu electroplating, excess materials outside the trenches are removed by CMP, which also planarizes the top surface. The chemicals in the slurry react with and weaken the films to be removed. The abrasive components accelerate the weakening process. The polishing pad helps wipe the reacted materials away from the wafer surface. Different slurries are used to target Cu, Ta, or TaN. Nearly all the aforementioned fabrication steps are repeated to passivate the Cu-filled trenches with a SiN-based film on the top, to create Cu-filled vias connecting to the metallization level above, and to produce the next level of metallization (see Figure 1.6).

1.2.2 Diffusion Paths in Cu/low-*k* Interconnects

As explained in the previous section, the Cu metallization scheme consists of polygranular Cu-interconnects encapsulated by Ta-based barriers on the side and bottom, and a SiN-based capping layer on the top. This architecture presents 4 diffusion pathways for electromigration: the interface along Cu/capping layer (SiN), the interface along Cu/liner barrier, the Cu grain boundary (g.b.), and the Cu bulk (see Figure 1.9). Following the formulism by Hu *et al.* [Hu 99], the overall diffusivity can be written as:

$$(Dz^*)_{eff} = (D_0z^*\delta)_{Cu/SiN}\left(\frac{1}{h}\right)\exp\left(\frac{-\Delta H_{Cu/SiN}}{kT}\right)$$

$$+ (D_0z^*\delta)_{Cu/Ta}\left(\frac{2}{w}+\frac{1}{h}\right)\exp\left(\frac{-\Delta H_{Cu/Ta}}{kT}\right)$$

$$+ (D_0z^*)_{g.b.}\frac{\delta_{g.b.}}{d}\left(1-\frac{d}{w}\right)\exp\left(\frac{-\Delta H_{g.b.}}{kT}\right) \qquad (1.14)$$

$$+ (D_0z^*)_{bulk}\exp\left(\frac{-\Delta H_{bulk}}{kT}\right)$$

where δ is the diffusion interface depth, and d, h, and w, are the grain size, line thickness, and line width, respectively. As will be discussed later, the most dominant diffusion path in Cu-interconnects is the Cu/SiN interface, whose kinetic properties are characterized through experiments that are presented in this dissertation.
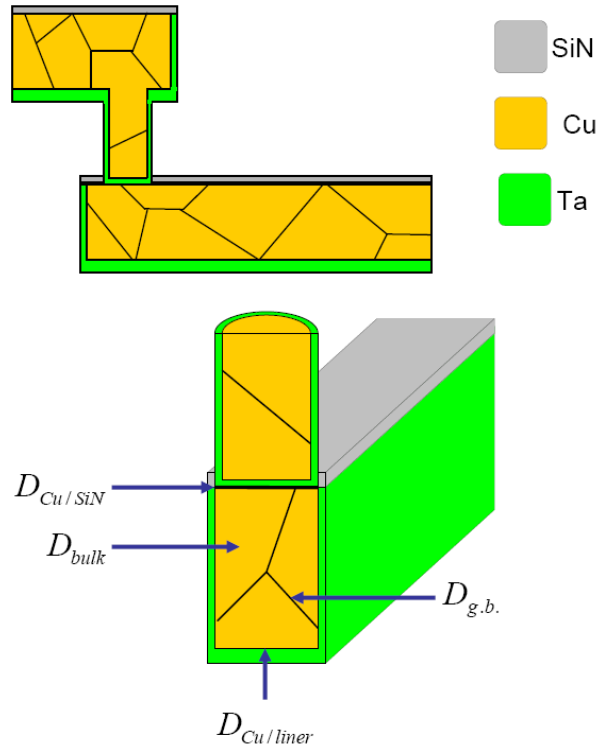
Figure 1.9 Four pathways for electromigration in Cu/low-*k* interconnects are illustrated: the Cu/SiN interface, the Cu/Ta liner interface, the Cu grain boundary, and the Cu bulk.

1.3 Interconnect Trees

Reliability testing is most often carried out using simple via-terminated segments; where we define a segment as a length of interconnect carrying a fixed current. However, in actual circuits, multiple segments can join together in a wide variety of ways. A via-terminated interconnect line with a third via in the middle is really two segments, in that different currents can be carried in the segments on either side of the central via. Also, segments can meet in junctions, to form simple 'T-shaped' junctions for example, for which each segment meeting at the junction can carry different currents. It has been shown in experiments on both Al and Cu-based multi-segment interconnect structures, that the reliability of any given segment depends on the current or stress-induced migration in connected segments [Hau 00c, Hau 01, Gan 03, Cha 06]. Therefore, for circuit-level reliability analyses, it is important to identify fundamental reliability units (FRUs) for which the reliability is not a function of stress conditions in other units. Such a unit is an interconnect tree, defined as any set of interconnect segments that are connected without a diffusion barrier between them, but that are connected to the rest of the circuit through a diffusion barrier. For technology in which refractory-metal liners are at the base of vias, a tree would be a set of segments that are connected within one layer of metallization.

The overall circuit-level reliability is the cumulative reliability of each FRU, which is evaluated on an individual basis. In order to accomplish this goal, one needs to establish both systematic approaches to evaluate the reliability of Cu-interconnect circuit layouts [Ala 05] but also physical understandings of electromigration behaviors in individual interconnect trees. The former has been developed by Alam *et al.* [Ala 04, Ala

05], who have developed a layout-specific, circuit-level reliability assessment tool, *SysRel*, employing a hierarchical approach to analyze Cu-based circuits. Experimentally, using Al-based interconnects, the jL_{crit} immortality concepts are extended to individual trees of arbitrary complexity by S.P. Hau-Riege *et al.* [Hau 00c, Hau 01] through the investigations of an effective value, $jL_{crit,eff}$. However, the experimental understanding of Cu/low-*k* interconnects is not yet complete. This dissertation presents experiments and analyses carried out toward this goal.

1.4 Reliability Statistics

Despite accurate experimental characterizations of the kinetic parameters, electromigration-induced failures are stochastic in nature. As a result, the times-to-failure (TTFs) for any given population of interconnects are not deterministic, but are governed by statistics instead. Nearly all reliability literature pervasively use the mono-modal lognormal distribution to describe the scatter of electromigration lifetime data, although the justifications are mostly empirical. Alternative fitting methods using Weibull-like distributions [Llo 91a], multi-lognormal distributions [Llo 91b, Cho 89, Kit 91], and 3-parameter lognormal distributions [Li 06] have been proposed. However, due to the simplicity of the expression and the ease for data comparisons, the mono-modal lognormal distribution fit remains as the convention among the reliability community. Similar to actual lifetimes, the lognormal distribution is only defined for time being positive. The versatile shape of the distribution covers a great range of data. The lognormal fit excels over other forms especially when the range of data cover different orders of magnitude [Kin 71, Ait 57], which is commonly achieved during

electromigration experiments. Most of the experimental data shown in this dissertation are also well fit by the mono-modal lognormal distribution. However, exceptional cases were observed and will be discussed.

1.4.1 Basic Definitions

Regardless of the distribution of the TTFs, four mathematical concepts are essential to aid the discussions of reliability: the cumulative distribution function (CDF), $F(t)$, the probability density function (PDF), $f(t)$, the reliability function, $R(t)$, and the failure rate, $\lambda(t)$. In the context of electromigration testing, if N identical interconnect structures were used in an experiment, $F(t)$ is defined to be the probability of any single sample failing at time t. If N is sufficiently large, $F(t)$ is also the fraction of samples that failed up to time t,

$$F(t) = \frac{N_f(t)}{N},\tag{1.15}$$

where $N_f(t)$ equals to the number of failed samples at time t. $f(t)$ is defined as the rate of change for the probability of failure,

$$f(t) = \frac{dF(t)}{dt},\tag{1.16}$$

or,

$$F(t) = \int_0^t f(t')dt' . \qquad (1.17)$$

$R(t)$, representing the surviving fraction of the population at time t, and $\lambda(t)$, representing the instantaneous rate of failure at time t, are computed as,

$$R(t) = 1 - F(t), \qquad (1.18)$$

and,

$$\lambda(t) = \frac{1}{1 - F(t)} = \frac{1}{R(t)} . \qquad (1.19)$$

Generally, the $\lambda(t)$ of IC components follows a bath-tub-shaped curve with three different regions (see Figure 1.10): early failure or infant mortality, steady state, and wear out regimes. Early failures are usually due to manufacturing defects, which have the highest rates for failure near $t=0$. Over time, the failure rate falls to a steady state value. During the steady state period, failures are sparse and almost constant in time, and are usually due to a combination of numerous independent causes. Toward the end of the IC components' lifetime, however, the number of failures monotonically increases because of specific physical mechanisms, like electromigration, leading to the wearing out of the components.
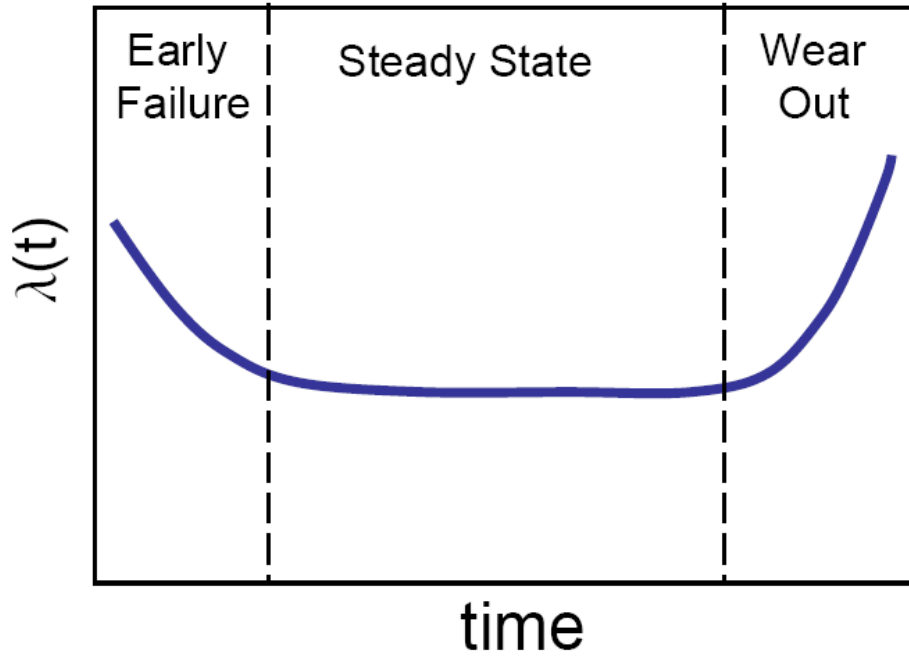
Figure 1.10 Failure rates vs. time for typical IC components (the-bathtub-shaped curve).

1.4.2 Lognormal Distribution and Lifetime Extrapolation

As introduced above, electromigration lifetimes are seemingly best fit with the lognormal distribution,

$$f(t) = \frac{1}{t\sigma\sqrt{2\pi}} \exp\left[-\frac{1}{2\sigma^2}\left(\ln\frac{t}{t_{50}}\right)^2\right], \qquad (1.20)$$

where t_{50} is the medium time to failure (MTTF), and σ, the shape parameter, corresponds to the standard deviation of the natural log of the failure times. $\ln(f(t))$ is normally distributed with mean of $ln(t_{50})$ and variance σ^2. This yields:

$$F(t) = \int_0^t f(t')dt' = \Phi\left[\frac{1}{\sigma}\left(\ln\frac{t}{t_{50}}\right)\right], \tag{1.21}$$

and

$$\Phi(z) = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^z \exp\left(-\frac{u^2}{2}\right)\cdot du = \frac{1}{2}(1 + Erf(\frac{Z}{\sqrt{2}})), \tag{1.22}$$

where Φ is the normal cumulative distribution function, and Erf is the error function. Lastly, the translation between any arbitrary time, t, and t_{50} can be expressed as,

$$\ln t = \ln t_{50} + \sigma\Phi^{-1}(F(t)), \tag{1.23}$$

for example,

$$\ln t_{1FIT-hr} = \ln t_{1\times10^{-9}} = \ln t_{50} + \sigma\Phi^{-1}(1\times10^{-9}). \tag{1.24}$$

Using Equations (1.20) to (1.24) along with the Black's equation (Equation (1.1)), the lifetimes at any probability density, under any operating conditions – different

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combination of j and T values, can be extrapolated using a few experimentally determined parameters, namely, ΔH, n, t_{50}, and σ.

However, generalizations based on such extrapolations are often scientifically unsound. First, statistically significant electromigration data can rarely be acquired under operating conditions. The scientific bases for using the lognormal fit over the early failure regimes, such as near $t_{1\times10^{-9}}$, under the normal operating conditions, are not well established. Second, an implicit assumption for this extrapolation is that σ does not change for different testing or operating conditions. This assumption can be either overly conservative or optimistic, depending on the physical failure mechanism at play. Currently, investigations on σ using Cu/low-k interconnects do not exist. Lastly, when the experimental data shows multi-modal failures, only the portion of the data corresponding to the appropriate failure mechanism (usually, this is difficult to determine) should be used in extrapolation. If possible, mechanistic comparisons through physical analyses of failures that occur in the field and under accelerated conditions, as well as those between early and late failures, may establish validations for the extrapolation method mentioned above, on a case-by-case basis. However, such analyses are rare, and generalizations for extrapolations are potentially disastrous.

1.5 Thesis Objectives

The aim of the work described in this dissertation is address the effects of the mechanical properties on electromigration-induced failures. As reviewed above, in order to continuously reduce the RC delay, Cu/low-k metallizations will be required to have ever decreasing ILD, liner, and capping layer thicknesses and ever decreasing k values

for the ILDs (i.e., decreasing Young's moduli). These facts lead to an ever decreasing B.

Experiments have shown that the dominant electromigration diffusion path and the site

for void nucleation, the Cu/capping-layer interface, is not changed for different ILDs

[Hau 04]. However, changes in the mechanical properties of the Cu-interconnects *do*

reduce the elastic response of the surrounding confinement on the Cu wiring, which, in

turn, affects the thresholds required for electromigration-induced failures by void

nucleation, void growth to a critical size, and Cu extrusion. In order to understand such

effects, a method is first developed to determine the elastic response of a Cu-interconnect

material system, i.e., B. Second, the physical nature of the mechanism for each type of

electromigration-induced failure must be explored through experiments. Such

characterizations and observations reveal relationships between the mechanical properties

of the material system and the corresponding failure mechanisms. Hence, the effects of

the mechanical properties on the reliability of Cu/low-k interconnect systems can be

explored.

1.6 Thesis Organization

In order to discuss the work carried out to achieve the goals outlined above, this

thesis is divided into 7 chapters. First, a quantitative understanding of the relevant

mechanical properties is established. Chapter 2 and 3 describe investigations of the

mechanical properties of the Cu/low-k materials system. A suite of experimental

characterization techniques that can be used to determine various mechanical properties

of the constituent materials, including low-k ILD films, are described in Chapter 2.

Chapter 3 presents FEM simulations that determine the overall elastic response of Cu/low-*k* interconnect material systems using the properties determined in Chapter 2.

Chapter 4 discusses investigations pertaining to the diffusive properties of Cu/low-*k* interconnects. First, experimental determination of the dominant diffusion path in Cu-interconnects, the interface between Cu and the capping layer, is reviewed. Second, methods for characterizing the kinetic parameters for electromigration are presented through correlating the resistance increase rate during electromigration experiments to the drift velocity using both via-above and via-below type of interconnects. Lastly, investigations of the thresholds of void nucleation at the Cu/capping layer interface show that the jL_{crit} values obtained from via-above type of interconnects approximate the thresholds for void nucleation. Hau-Riege *et al.* found that the critical stress required for void nucleation is proportional to $\sqrt{B}$.

Under commonly used testing conditions, failures in Cu/low-*k* interconnects are due to void growth, instead of void nucleation. Chapter 5 presents investigations of electromigration-induced void growth failures through experiments and modeling using Cu/low-*k* interconnect trees. It is found that during electromigration, the rate of void growth in the failing segment quantitatively depends on the magnitude of the back stress force, which is modulated by both the electromigration activities of the neighboring segments that serve as active atomic sinks and reservoirs as well as *B*. Simulation predictions on the reliability of the interconnect tree structures as a function of *B* show that as *B* decreases, the positive effects of reservoirs on reliability are diminished, while the negative effects of sinks on reliability are amplified.

In electromigration experiments that large compressive stresses developed inside Cu/low-*k* interconnects, Cu extrusions near the anode end are observed during failure analysis. In Chapter 6, the mechanism for electromgration-induced failures is identified as mode-I crack propagation at the interface between the capping layer and the metallization layer below. Quantitative analyses of the critical stress required for extrusion failures are presented. Failure-analysis-based estimation and critical stress intensity factor-based calculations show consistent results, which indicate that the threshold required for extrusion failure is proportional to $\sqrt{\dfrac{G_{I,crit} \cdot M}{a}}$, where $G_{I,crit}$ is the mode-I critical energy release rate of the failing interface, M is the effective plane-strain modulus of the Cu/low-*k* material system, and *a* is the half-width of the interconnect segment. Therefore, as *B* decreases, sparsely packed, wide interconnects are most prone to extrusion-induced failures.

Lastly, Chapter 7 gives a comprehensive summary of the results and suggests future directions for research in this area.

The appendix pertains to test wafers fabricated by International Sematech. Currently, International Sematech terminates interconnect fabrication with unpassivated Cu bondpads, which can oxidize during electromigration experiments rendering the results useless. Appendix A describes a procedure to passivate the exposed Cu bondpads with Al film using a lift-off process at the Microsystems Technology Laboratories (MTL) at MIT. Appendix A also includes a library of interconnect structures on the 465AZ Sematech test module mask designated for the Sematech-MIT collaboration.

Chapter 2

Characterizations of the Mechanical Properties of Low-*k* Dielectric Thin Films

As mentioned in Chapter 1, usually, low-*k* materials lower the *k* value by changing the density and/or the polarizability of the rigid Si-O covalent bond. Consequently, as the dielectric constant, *k*, decreases, the ILD become less stiff, and the modulus decreases. Knowledge about the mechanical properties, most importantly, the elastic properties of the low-*k* films is required in order to perform reliability assessment on electromigration-induced failures in Cu/low-*k* interconnects. Therefore, accurate experimental characterizations of the mechanical properties of the low-*k* films are needed. This chapter mainly presents investigations of the mechanical properties of two films, fluorine-doped SiO_2 films made using tetraethoxysilane PECVD precursor (F-TEOS) (*k*=3.5), a widely used low-*k* material, and methyl-silsesquioxane (MSQ) (*k*=2.3), a low-*k* ILD used in interconnect structures fabricated by International Sematech. A suite of analytical techniques were used to characterize the modulus, namely, wafer curvature, nanoindentation, micro-cantilever fabrication and deflection, and membrane bulge measurements. Self-consistent results were obtained using these various techniques. The mode-I adhesion property between Ta and SiN thin films were also performed.

2.1 Wafer Curvature Measurement

2.1.1 Experimental Procedure

9500Å- and 10335Å-thick F-TEOS films deposited using the PECVD method on 200mm diameter Si(100) and Si(111) substrates were obtained from Chartered Semiconductor in Singapore. 12000Å-thick MSQ films (JSR-LKD5109) deposited by spin-on method on Si(100) substrates were obtained from JSR Mirco in Japan. Wafer curvature measurements using laser scanning technique were conducted on these samples using a commercially available apparatus, Tencor FLX-2320. In the testing system, a laser beam (either 670 or 750nm in wavelength) is directed at the sample, and a position-sensitive photodetector is used to measure the angle between the incident and the reflected beams (see Figure 2.1). Such measurements produce the position-dependent slope of the sample surface, whose derivative with respect to the scanning position is the curvature of the wafer in the limit of small deflections. The stage, on top of which the sample wafer is placed, can be heated and cooled in a controlled manner so that laser scans at various temperatures can be carried out. Due to the difference in thermal expansion between the film material and the substrate, the sample bows when heated. Since the substrate thickness (~750μm) is more than two orders of magnitude larger than the film thickness, the *thin-film approximation* can be applied. The measured curvature changes can then be translated into changes in stress following the form of Stoney's relation [Sto 09],

$$\Delta\sigma_f = \Delta\alpha\, \tilde{E}_f\, \Delta T = \frac{1}{6}\frac{E_S}{(1-v_S)}\frac{h_S^2}{h_f}\left(\frac{1}{R_1}-\frac{1}{R_2}\right),$$ (2.1)

where σ is stress, $\tilde{E}$ is the biaxial modulus, α is coefficient of thermal expansion, T is temperature, E is Young's modulus, υ is Poisson's ratio, h is thickness, R is the radius of curvature of the wafer, and the subscripts s and f denote the substrate and film, respectively.
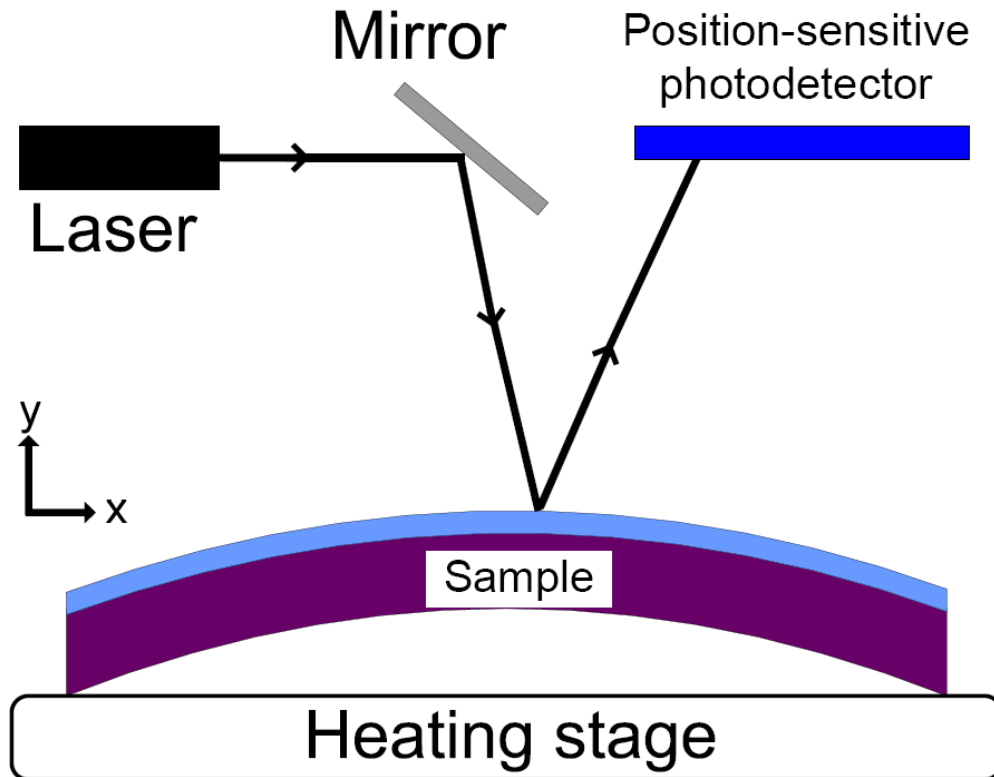
Figure 2.1 Schematics of the Tencor laser scanning equipment used to measure the curvature of samples, from which the product of the biaxial modulus of the film and the difference in the coefficient of thermal expansion between the film and the substrate, $E_f\Delta\alpha$, can be calculated.

2.1.2 Results and Discussion

Temperature cycles shown in Figure 2.2 were used in the wafer curvature experiments. In several instances, the cycles were repeated on the same sample and at a fixed orientation to ensure the repeatability of the measurements. No differences were observed between the different numbers of cycles. This indicates that no plastic deformation was induced by the applied thermal loads, which was expected for the temperature ranges used in the experiments. It was seen from the room temperature laser scans that nearly all the wafers are not initially flat, or have a well-defined dome shapes (see Figure 2.3(a) for an example). The exact shape of the wafers varies case-by-case, described by some, with the likeness of potato chips. Since the moduli of the low-k films are small, the film stress induced by heating is small as well. The large magnitudes of the initial random curvature of the 200mm wafers would introduce substantial error to the Tencor stress measurements if not accounted for. Therefore, in the cases of laser scanning using low-k blanket films, accurate measurements require the subtraction of an initial reference profile on a measurement-by-measurement basis. Figure 2.3(a) shows an example of the wafer profile obtained on a F-TEOS film on a Si(111) wafer at different temperatures. It is demonstrated that the initial surface variance is on the order of the curvature induced by the thermal load, which means that the uncertainty would be on the order of the measurement itself. However, accurate calculations could be performed after the initial surface profile being subtracted from the subsequent measurements, as seen in Figure 2.3(b). Such normalization produces curvature profiles resembling well-behaved dome-like shapes.
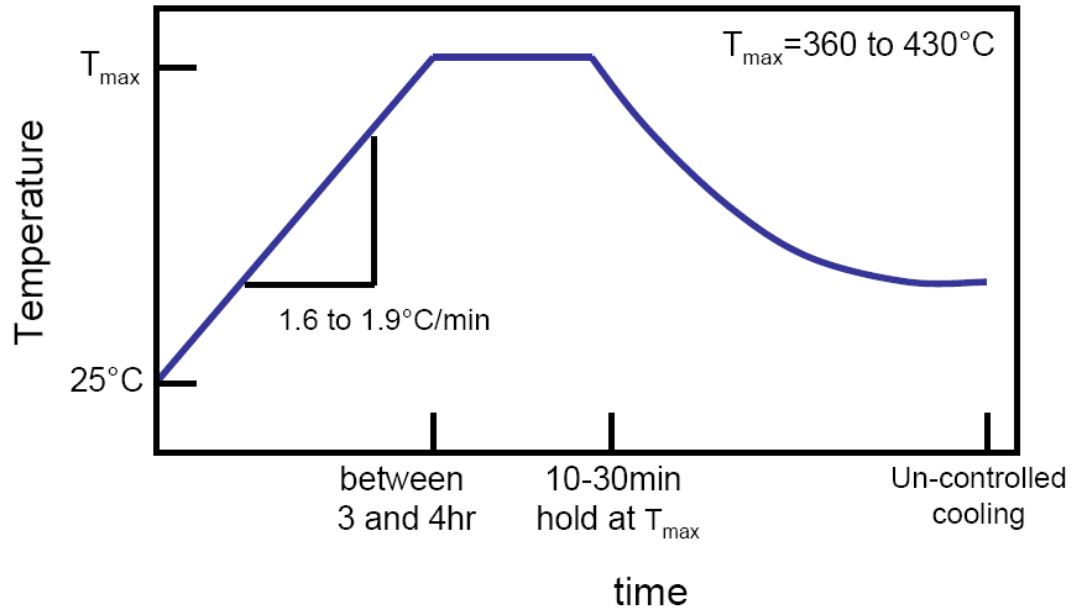
Figure 2.2 Illustrative profile of temperature cycles used during wafer curvature measurements performed using the Tencor system.
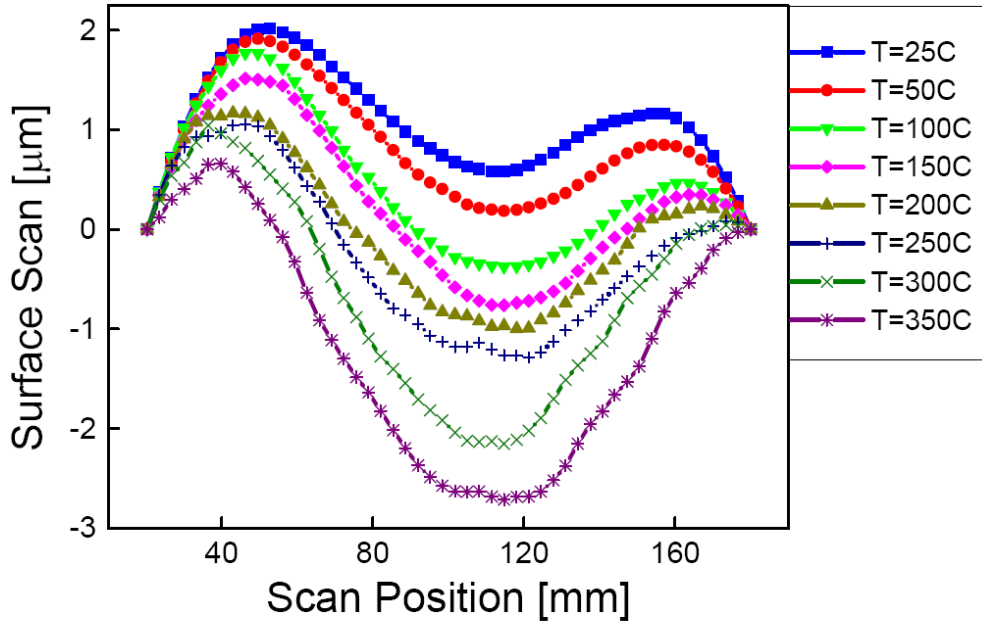
(a)
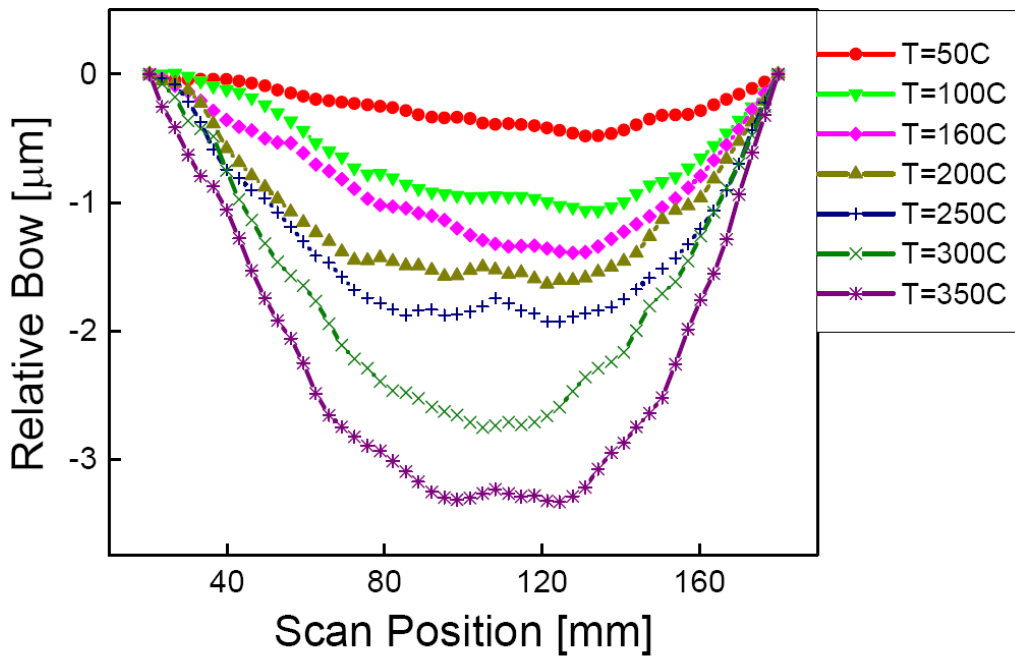
(b)

Figure 2.3 (a) Laser scan profiles of an F-TEOS film on a Si(111) wafer as a function of temperature. The initial variance in the surface profile is on the order the amount of bow induced by the thermal loading. (b) The normalized surface scans, in which the initial scan, the surface profile at 25°C, is subtracted from the results for each of the subsequent scans.

Using the method described above, the change in stress induced by heating can be calculated for all the samples according to Equation (2.1). The results obtained from F-TEOS films on Si(111) substrates are plotted in Figure 2.4. From Stoney's relation, the slope of $\Delta\sigma_f$ vs. T is $\Delta\alpha \cdot \tilde{E}_f$. For F-TEOS films, $\Delta\alpha \cdot \tilde{E}_f$ was obtained using two different substrates, Si(100) with bi-axial modulus 180.5GPa, and Si(111) with bi-axial modulus 229.0GPa. Therefore, a system of two equations can be established, in which the two unknowns, $\tilde{E}_f$ and α_f, can be independently calculated by assuming a υ of 0.16 (similar to that of SiO$_2$) to give $E_{F-TEOS} = 47GPa$ and $\alpha_{F-TEOS} = 0.88\,ppm/^\circ C$. These values are similar to those presented in [Che 00]. Similarly, experiments using MSQ films on Si(100) samples produced $\Delta\alpha \cdot \tilde{E}_f = 0.00845MPa/^\circ C$. By assuming similar values of υ and α as those for F-TEOS, the Young's modulus is determined to be 4.2GPa, which is consistent with that determined using nanoindentation and cantilever deflection techniques (see sections below).
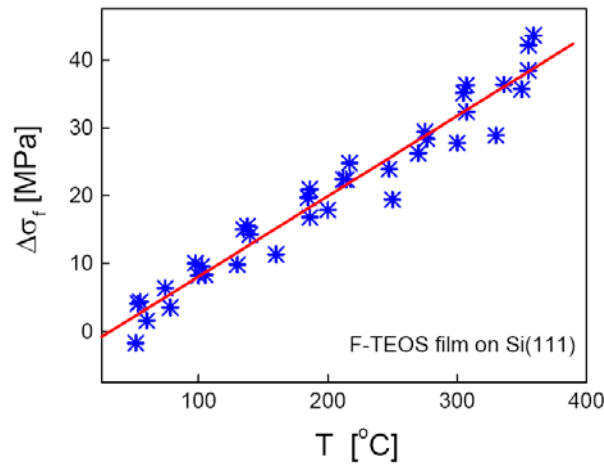
Figure 2.4 Stress-temperature curve for an F-TEOS film on a Si(111) substrate. The stresses were calculated using normalized surface scans for multiple temperature cycles.

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2.2 Nanoindentation

As discussions in the previous section show, the wafer curvature measurements on pre-fabricated blanket low-k film samples enable the determination of the product $E_f \Delta \alpha$. As demonstrated by the case of F-TEOS films, only when two different substrates with different moduli were used, Si(100) and Si(111), could the two properties, E_f and α_f be de-coupled. On the other hand, the nanoindentation technique, low-load and depth-sensing vertical indentation [Doe 86, Oli 92], can produce direct measurement of the modulus of a thin film on a substrate.

2.2.1 Experimental Procedure

Nanoindentation experiments were performed using the commercially available Hysitron TriboIndenter, which has fully automated controls with a computer user interface (see Figure 2.5), at the MIT Nanomechanics Lab. In this system, the nanoindentation experiments were performed in open atmosphere. An area on a sample that was fixed to the stage could be selected from the optical view before the nanoindentation experiments were to be performed. The system is also equipped with an atomic force microscope (AFM), which can be used to further analyze the surface. The nanoindenter unit is capable of applying a load in the range of about 5-10μN up to 10mN and a maximum displacement of 5μm while performing indentations. A variety of different indenter tips with different geometries are available for the TriboIndenter. However, the experiments described in this chapter were carried out using the Berkovich

diamond indenter tip, with the shape of an inverted pyramid. See [Fis 02] for detailed descriptions of indenter tip geometries.

The samples used in the indentation experiments consisted of not only the 9500Å-thick F-TEOS films and the 12000Å-thick MSQ films (JSR-LKD5109) on Si(100) substrates, similar to those used for the wafer curvature experiments, but also large exposed Cu thin film patterns without any passivation on top, such as, extrusion monitor plates (200μmX1000μm) and bondpads (85μmX85μm), on Cu/SiO_2 interconnect sample wafers fabricated by International Sematech that had been processed through the CMP step of the second metallization (top) level.

Illustrations of the force loading cycles used in the experiments are shown in Figure 2.6. First, the indenter tip is allowed to settle on the surface without any load to ensure a reference surface height is sensed. Then, a ramp-up in force occurs up to a maximum pre-defined value, F_{max}, ranging from 10 to 800μN for the experiments described here, accompanied by elastic and often plastic deformation of the samples under the tip. Lastly, the indenter tip is either withdrawn from the film immediately, or after a 5 to 60sec delay (see Figure 2.6). The applied force, the depth traveled by the indenter tip, and time were simultaneously recorded. The rates of loading and unloading were varied for the same F_{max}. However, no differences in the depth measurement were seen for different rates. During most measurements, the holding periods at F_{max} (see Figure 2.6) did not produce any changes in the maximum depths the indenter tip reached, because the materials studied here are elastic, rather than visco-elastic. However, on occasion, it was observed that the transducer of the nanoindenter (containing piezoelectric circuit elements) produced significant 'drifts' in the measurements. Self-

consistent results, similar depths at F_{max} obtained from both types of loading cycles and

without any 'drifts' during the holding periods, were used in the analyses.
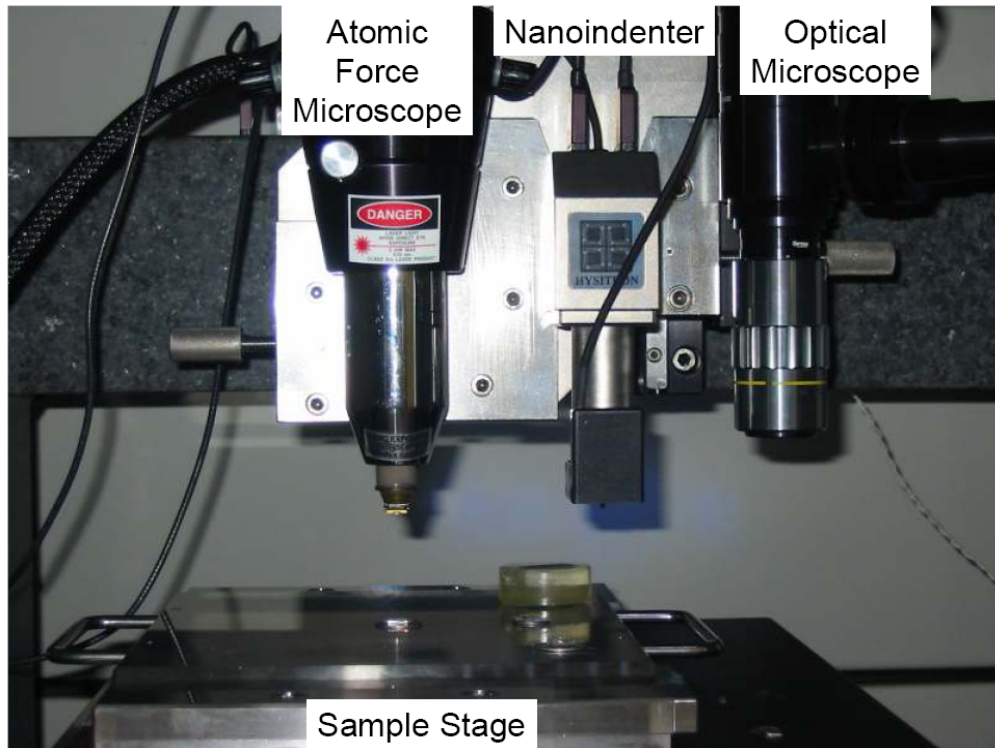
Figure 2.5 The TriboIndenter by Hysitron at the Nanomechanics Lab at MIT. The testing apparatus is fully automated with a computer user interface for the controls.
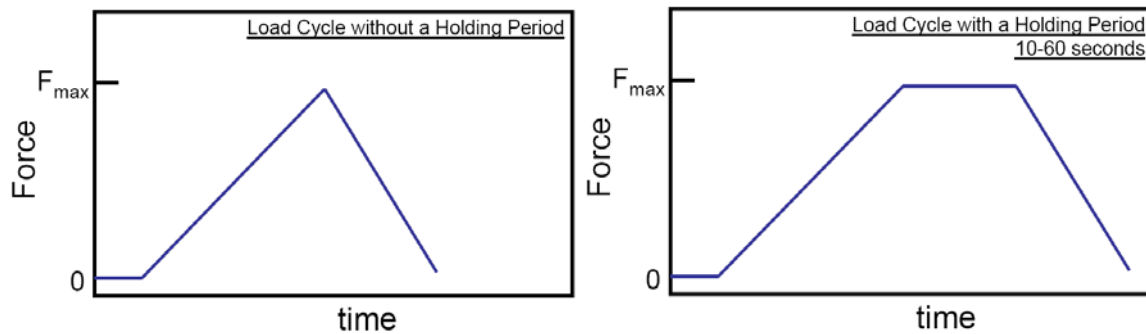
Figure 2.6 Two types of force loading cycles were used in nanoindentaion experiments: with and without a holding period at F_{max}.

2.2.2 Reduced Modulus, E_r

The force vs. depth curves were analyzed for the indentation experiments (see Figure 2.7). The unloading portion of the data corresponds only to the elastic response by the sample, while plasticity may occur during loading. By considering the known geometry of indenter tips, analytical models that correlate the slopes of the unloading portion of the curves to the mechanical properties of the materials were derived in references [Doe 86] and [Oli 92]. The hardness, H, and the reduced modulus, E_r, a measure of the overall elastic response by the sample combined with that of the indenter tip can be expressed as

$$H = \frac{dF}{dA} = c_b \sigma_y, \tag{2.2}$$

and

$$S = \frac{dF}{d\delta} = \beta \frac{2}{\sqrt{\pi}} E_r \sqrt{A}, \tag{2.3}$$

where F is the applied force, A is the projected contact area, c_b is called a constraint factor (which depends on the indenter geometry and materials properties), σ_y is the sample's yield strength, δ is the indentation depth, S is referred to as the contact stiffness, and β is a correction factor for a given indenter tip geometry. When the tip is conical, i.e., axially symmetric, $\beta=1$. For the Berkovich shape, $\beta \approx 1.03$ [Vla 94, Fis 02, Kin 87]. A is calculated as

$$A = \pi a^2 = \pi \cdot (\tan \alpha)^2 \cdot \delta^2,$$ (2.4)

where a is the contact radius and α is referred to as the apex angle, such that A associated with the inverted pyramid shape of the Berkovich indenter can be described by and equivalent conic shape of angle α at its tip (70.3° for Berkovich tips). However, indenter tips in general are not atomically sharp, but instead have a finite radius at the tip, $R_i = 80 - 120nm$ for the Hysitron TriboIndenter. Therefore, for extremely shallow indentations, a is approximated using the tip radius, instead of using Equation (2.4). Under these assumptions, E_r from the different experiments were calculated and are plotted in Figure 2.8.

Under ideal conditions, the contribution to E_r from the sample would only arise from the film. Therefore, for isotropic materials, the plane-strain modulus intrinsic to the film can be determined using [Fis 02],

$$\frac{1}{E_r} = \frac{1 - v_i^2}{E_i} + \frac{1 - v_f^2}{E_f},$$ (2.5)

where the subscripts i and f denote the indenter and film, respectively. The general rule-of-thumb ensuring such ideal conditions are met is that the contact depths during indentations should not exceed 10% of the film thickness, in order to avoid influences by the substrate [AST 87]. However, this rule is extremely rough, and for soft films on hard substrates, such as low-k films on Si, the 10% rule can be overly optimistic and incorrect: substrate contribution may become significant even when the indentation depth is less

than 10% of film thickness. Figure 2.8 shows that in the case of F-TEOS films, a discernable increase in E_r is observed as δ is increased to about 10% of the film thickness (by increase F_{max} during the experiment). Clearly, the depth at which substrate-independent measurements could be carried out varies depending on the particular substrate and film system. Therefore, accurate treatment of the substrate effects is needed in determining the moduli of low-k films by nanoindentation.

(a)

Nanoindentation on Cu Bondpad
Hertzian contact model

(b)
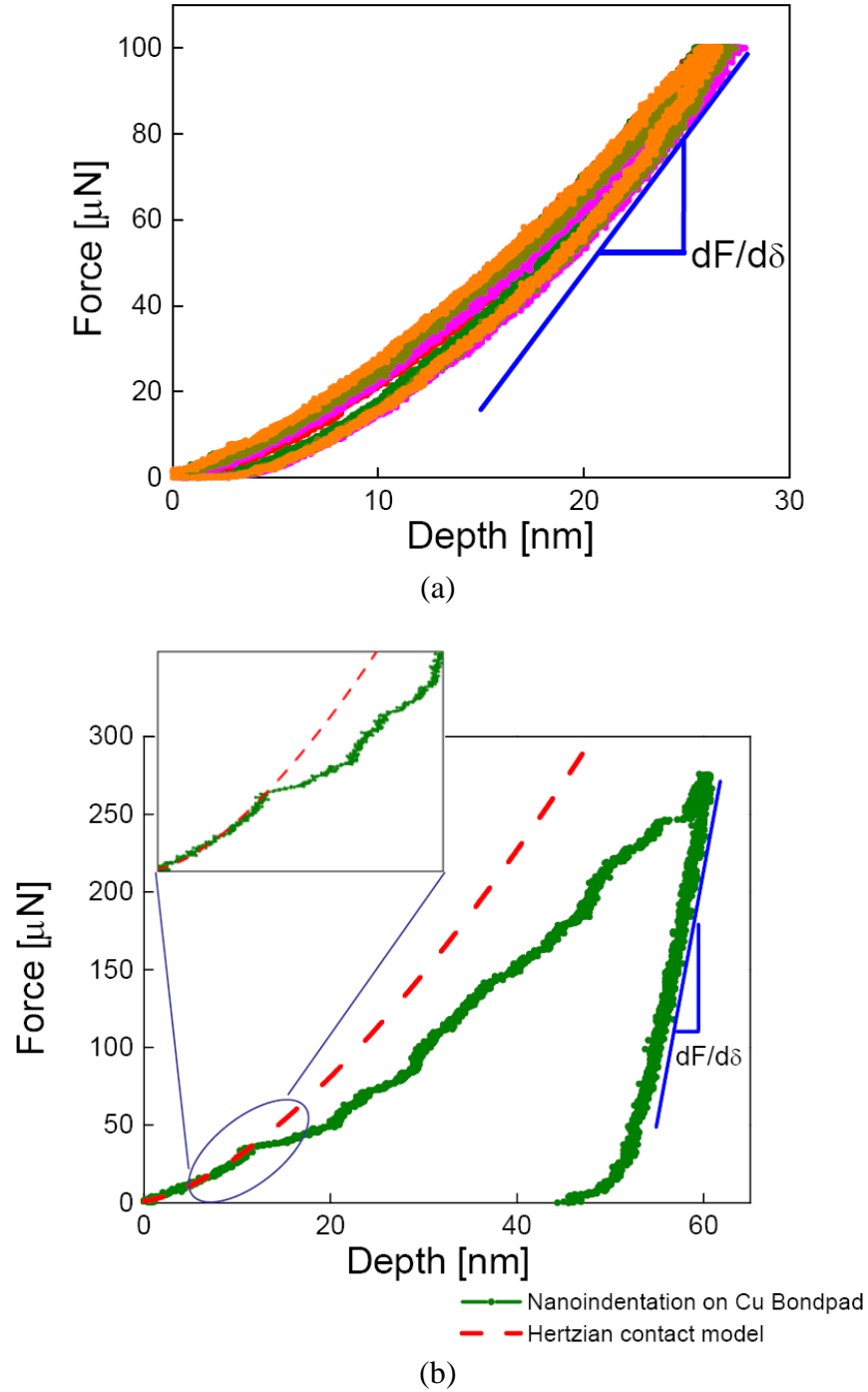
Figure 2.7 Example force vs. depth profiles of (a) several nanoindentations of an F-TEOS film on Si(100), and (b) one nanoindentation on an exposed dual-damascene Cu bondpad on a wafer of Cu/SiO$_2$ interconnects processed up until CMP. E_r is extracted from the initial slope of the unloading portion in both plots, and can also be obtained by applying the Hertzian contact model prior to 'pop-in' events for the crystalline Cu sample shown in (b).
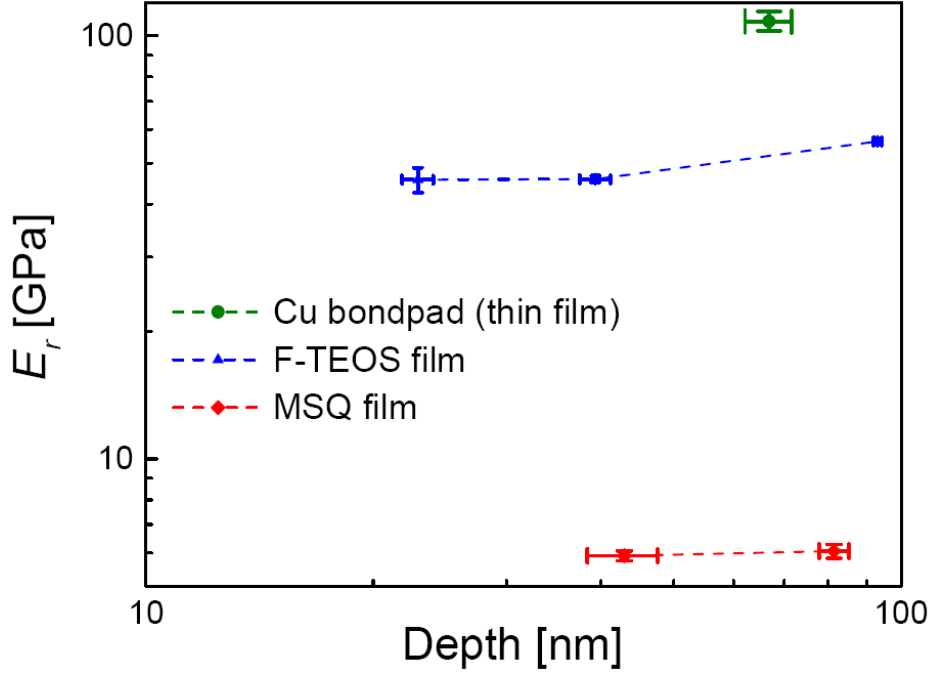
Figure 2.8 Measured reduced modulus, E_r, vs. the indentation depth, δ, for an exposed Cu bondpad on dual-damascene Cu/SiO$_2$ interconnect wafers, a 9500Å-thick F-TEOS film, and a 12000Å-thick MSQ film on Si(100) substrates. In the case of the F-TEOS film, a discernable increase in E_r is seen as the indentation depth is increased to 10% of the film thickness, due to contributions from the substrate.

2.2.3 Substrate Contributions to E_r

Several investigations, based both on theory as well as FEM analyses, address the effects of the substrate on modulus measurements of a film [Yu 90, Gao 92, and Che 01]. In the theoretical analysis presented by Gao *et al.* [Gao 92], the substrate contributions are weighted into the indentation measurements by using two weighting functions I_0 and I_1,

$$I_0(\frac{h}{a}) = \frac{2}{\pi}\tan^{-1}(\frac{h}{a}) + \frac{1}{2\pi(1-v)}[(1-2v)\cdot\frac{h}{a}\cdot\ln\frac{1+(\frac{h}{a})^2}{(\frac{h}{a})^2} - \frac{\frac{h}{a}}{1-(\frac{h}{a})^2}], (2.6)$$

and

$$I_1(\frac{h}{a}) = \frac{2}{\pi}\tan^{-1}(\frac{h}{a}) + \frac{1}{\pi}\cdot\frac{h}{a}\cdot\ln\frac{1+(\frac{h}{a})^2}{(\frac{h}{a})^2},$$ (2.7)

where h is the film thickness, in calculations of E_r,

$$E_r = \frac{2\mu_{eff}}{1-\nu_{eff}},$$ (2.8)

where μ is the shear modulus, such that

$$\mu_{eff} = \mu_s + (\mu_f - \mu_s)\cdot I_0(\frac{h}{a}),$$ (2.9)

and

$$\nu_{eff} = \nu_s + (\nu_f - \nu_s)\cdot I_1(\frac{h}{a}),$$ (2.10)

In the FEM analysis presented by X. Chen and J.J. Vlassak [Che 01], additional corrections to δ during the indentation process are considered. When the modulus ratio

between the film and substrate, $\dfrac{E_f}{E_s}$, is large, a 'sink-in' effect of the film material

around the tip results in a decrease of A, corresponding to a negative correction to δ. On

the other hand, when $\dfrac{E_f}{E_s}$ is small, a 'pile-up' effect results in an increase of A,

corresponding to a positive correction to δ. Consequently, when $\dfrac{h}{a}$ is in its medium

range (between 1 and 10), the FEM analysis mentioned above [Che 01] demonstrates that

the analytic model by Gao *et al.* [Gao 92] overestimates the substrate effect when 'sink-

in' is present, and underestimates the substrate effect when 'pile-up' is present.

However, the two different analyses converge when $\dfrac{h}{a}$ becomes large (>10), when I_0 and

I_1 approaches 1.

In all the nanoindentation measurements on F-TEOS and MSQ films, $\dfrac{h}{a}$ was

estimated to be ~10 and larger. The analytical treatment of E_r presented by Gao *et al.*

was applied in the analysis. In the depth range of the indentation experiments on MSQ

films, I_0 and I_1 were found to be between 0.980 and 0.990. By applying the measured E_r

in Equation (2.6), the Young's modulus of MSQ is found to be equal to 4.4GPa.

Similarly, for nanoindentations performed on F-TEOS film, I_0 and I_1 were found to be

between 0.987 and 0.992 for the shallow-depth indents. In the measurement where δ was

10% of film thickness, I_0 and I_1 both were calculated to be about 0.968. Thus, the

increase in the contribution by the substrate was quantified and isolated, and results for

the modulus of F-TEOS, 48GPa, were obtained, which is consistent with that determined

using the wafer curvature measurement.

2.2.4 Hertzian Contact Model

The substrate of the Cu thin-film features, such as an exposed Cu bondpad, is more complicated than that for the low-k dielectric films, Si(100). As mentioned above, the Cu film features, on top of which nanoindentations were performed, are parts of the dual-damascene metallization levels. In the Cu/SiO$_2$ wafers fabricated by International Sematech, two metallization layers exist. The samples used here were terminated at the second level after the CMP processing step. Recalling from the review on dual-damascene processing in Chapter 1, the substrate in this case, consists of multiple-layer film stacks, Cu-filled vias embedded in the dielectric film, the layer of dual-damascene Cu in the lower level of metallization, all having their respective SiN and Ta diffusion barrier layers. Additionally, all these layers are also stacked on top of more dielectric materials, which were grown on top of Si(100). The top dual-damascene layer in Cu/SiO$_2$ wafers fabricated by International Sematech has a thickness of 0.40μm. Therefore, δ in such experiments was more than 20% of the film thickness. However, due to the complexity of the substrate, an analysis on the substrate contribution similar to that shown in previous section cannot be performed.

However, since Cu is crystalline, well-defined mechanisms, like dislocation motion, are responsible for the plasticity induced during the loading portions of nano-indentation. Therefore, before the initiation of any plastic deformation, the strain is purely elastic. Furthermore, when the onset of plastic deformation occurs, an abrupt change in the slope of the force vs. depth curve, a 'pop-in' event, occurs [Gou 01]. For Cu thin films, Suresh *et al.* [Sur 99] have reported that 'pop-in' events usually occur below 50μN, which was also observed in the nanoindentations on exposed Cu bondpads

reported here (see Figure 2.7(b)). The portion of the indentation results prior to the first 'pop-in' event, truly elastic response of the Cu film, can be analyzed using Hertzian contact mechanics [Joh 85]. It was demonstrated in [Lar 96] that the following expression for Hertzian contact deformation should be used for the Berkovich indenter geometry at the depths described here,

$$F = 2.189 \cdot E_r \cdot \delta^2 \cdot (1.00 - 0.21 v_f - 0.01 v_f^2 - 0.41 v_f^3). \qquad (2.11)$$

At the shallow depths prior to the beginning of 'pop-in' events, Equation (2.5) can be used to extract the modulus of the film. As shown in Figure 2.7(b), by fitting Equation (2.11) to the shape of the indentation result prior to 'pop-in,' a modulus of 120GPa is obtained for the Cu bondpad, which is in excellent agreement with that reported in [Sur 99].

2.3 Micro-Cantilever Beams

Substrate-independent measurement of the film modulus can also be obtained using deflections of micro-cantilevers, a commonly employed technique in characterizations of materials used in the field of microelectromechanical systems (MEMS). Furthermore, analyses of the curvature of the cantilever and the buckling of doubly-supported beams can also give insights into other mechanical properties of the film, such as the stress gradient through the film thickness and the residual stress of the film.

2.3.1 Micro-fabrication of Beams Using Low-k Films

Micro-fabrication of cantilevers can be easily achieved via an anisotropic wet etch from the front-side of a patterned dielectric film on a Si(100) substrate. The pre-fabricated 9500Å-thick F-TEOS and 12000Å-thick MSQ samples on Si(100) mentioned in previous sections were used to fabricate the cantilever samples. The mask used for patterning and the processing steps used during micro-fabrication are illustrated in Figure 2.9 (a) and (b), respectively. The target dimensions of the beams on the mask are shown in Table 2.1. The processing steps (see Figure 2.9(b)), which were completed at the Exploratory Materials Laboratory (EML) at MIT, were first, deposition of a 1.5μm-thick photoresist layer, second, exposure and development of the photoresist layer, leaving a hard mask on top of the low-k film, third, plasma dry etch (CFH$_3$:Ar:O) to remove the remaining photoresist while removing the exposed areas of the low-k materials as well, and lastly, anisotripic wet etch using a 25% volumetric concentration of ethylammonium hydroxide (TMAH) solution at 87°C to etch away the Si under the film and to release the beam features. It was found that potassium hydroxide (KOH) solution would dissolve both the F-TEOS and MSQ films, and cross-sectional SEM confirms that TMAH solutions could also dissolve the MSQ films (at a slower rate), but would not attack the F-TEOS films. Therefore, only F-TEOS beam structures were produced using this fabrication technique.

The mask design takes advantage of the drastically different etching rates of Si<100> and <111> planes by the TMAH solution. The recipe above results in a ratio of approximately 1:100 in the etch rates of the two types of planes (<100> to <111>). When the die edges of the mask are aligned with the Si(100) substrate in-plane directions during

the photoresist development and exposure, beams in the shapes shown in the mask would be produced. However, despite the fact that the etch rate of Si<111> planes in TMAH solution is extremely fast, the etch rate of Si<100> planes is still finite. Therefore, in the process of releasing the beam structures, a small amount of undercutting at the support, approximately 15μm, in all the structures was produced (see Figure 2.10). Furthermore, any mis-alignment between the die edges of the mask with the in-plane (100) directions of the substrate would further exacerbate the undercutting at the support. The treatments of non-ideal supports in various cases are discussed in the following sections.
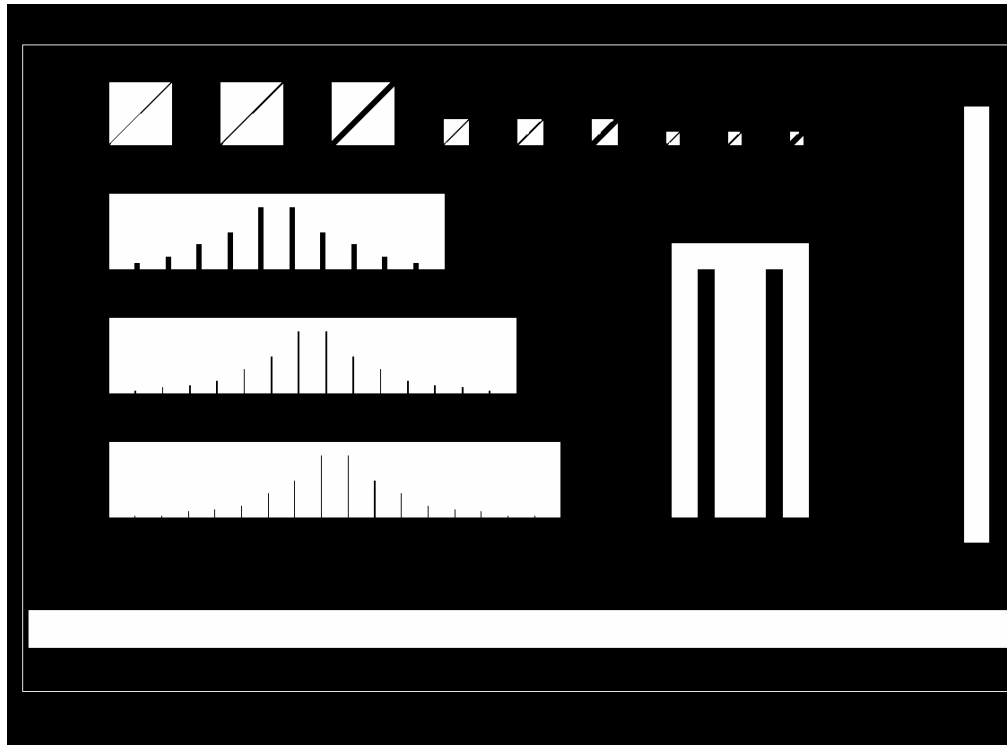
(a)
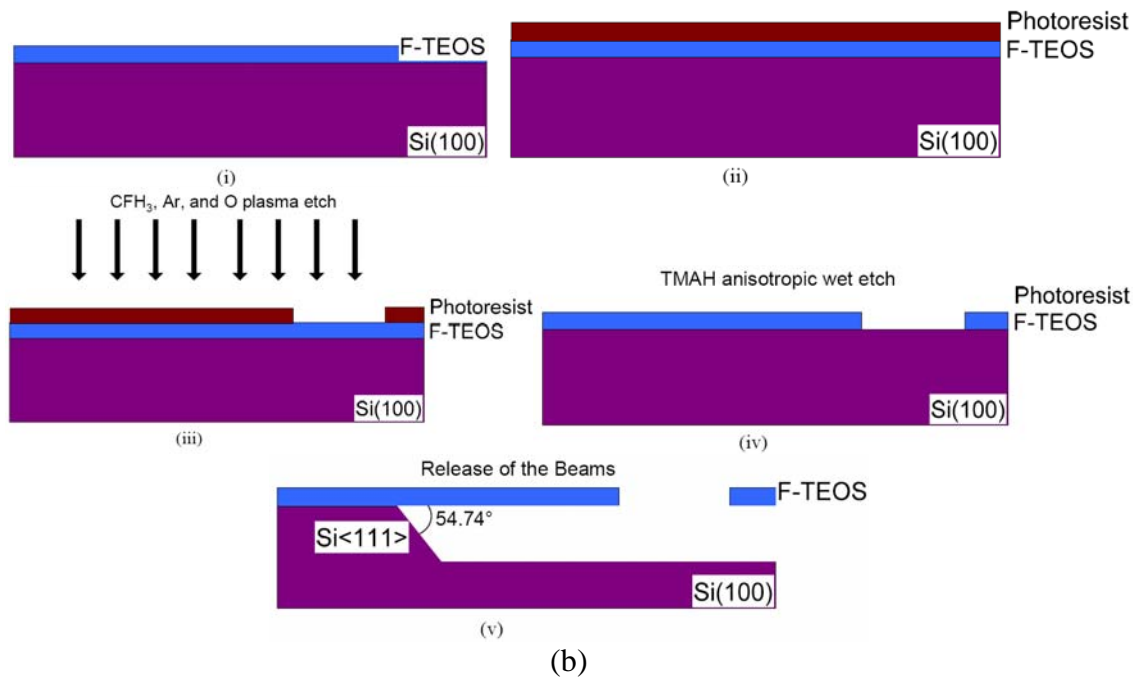
(b)

Figure 2.9 (a) Mask of one die used for developing the photoresist prior to plasma etch. A combination of micro-scale singly- and doubly-supported beams can be fabricated, as shown. (b) Illustration of the process flow employed to micro-fabricate the F-TEOS free-standing beams.

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Table 2.1 Dimensions of the F-TEOS beam structures fabricated for the cantilever deflections study. All units are in [μm].

Width (W)	Target Lengths of Singly-supported Beams (L)	Target Lengths of Doubly-supported Beams (L)
15	15, 20, 50, 70, 100, 200, 300, 500	140, 280, 700
20	15, 20, 50, 70, 100, 200, 300, 500	140, 280, 700
50	15, 20, 50, 70, 100, 200, 300, 500	140, 280, 700

(a)

(b)
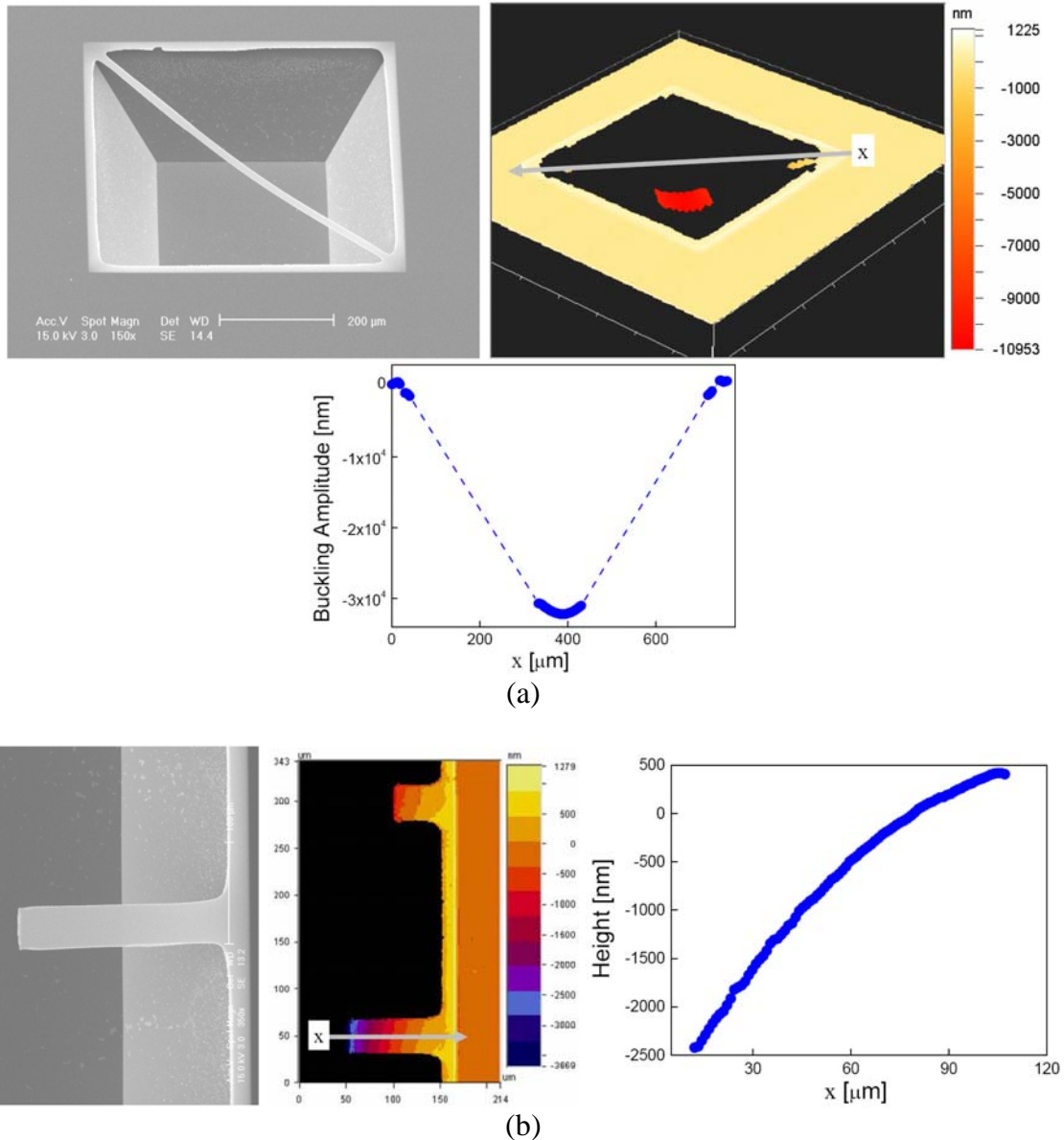
Figure 2.10 Scanning electron micrographs and surface profile measured using Wyko optical profilometer for (a) a doubly-supported beam showing buckling and (b) a singly-supported beam showing a downward curvature profile. Both micrographs show a non-ideality at the support resulting from the TMAH wet etch process.

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A Wyko NT2000 non-contact optical profilometer was used to measure the deflections of beams (Veeco Instruments Inc., Tucson, AZ), similar to those shown in Figure 2.10. A very basic description of the interferometric principles used by Wyko is shown in Figure 2.11. A beam of light is split into an incident beam shining on to the sample surface and a reference beam. Interference fringes form when the two beams recombine. A position-sensitive CCD array records such fringes, sharp increases in light intensity, which indicates the relative height of one pixel vs. another. Furthermore, the system is capable of measurements in two modes: Phase Shifting Interferometry (PSI) and Vertical Scanning Interferometry (VSI). PSI has sub-nanometer resolution, ideal for measurements of smooth surfaces, with the depth-of-scan less than 160nm. On the other hand, VSI is ideal for measuring rougher surfaces, and has depths of scans up to *mm* in range. Depending on the magnitudes of deflections, both modes were employed in mechanical characterizations of low-*k* films.
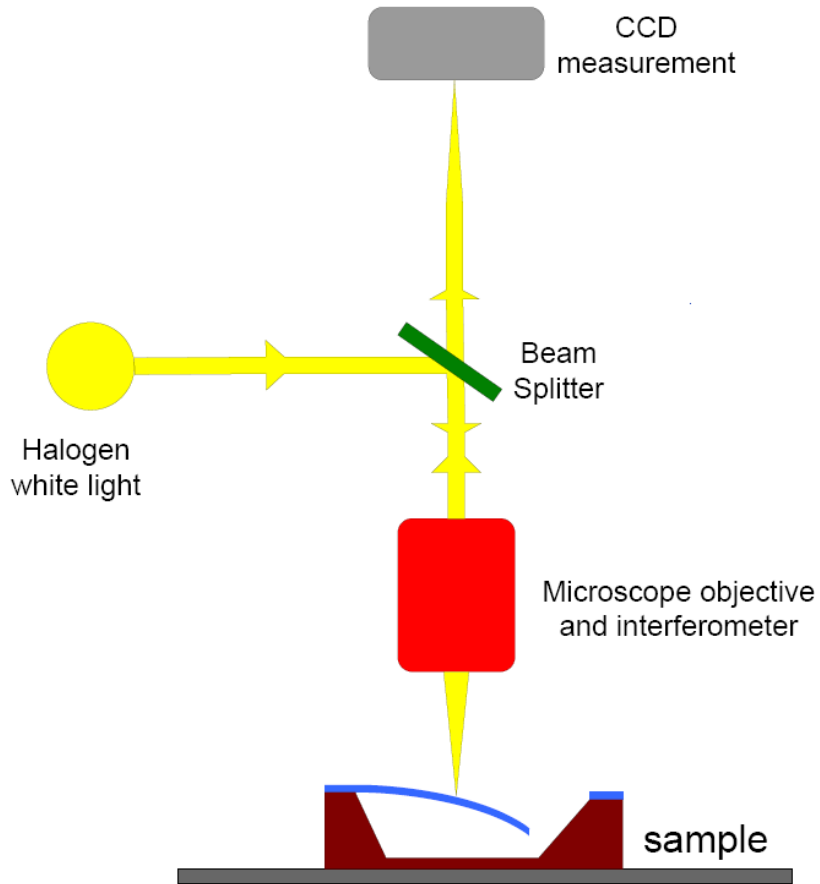
Figure 2.11 Interferometric principles of the Wyko optical profilometer. Various optical elements are omitted here.

2.3.2 Stress Gradient in F-TEOS Film

The curvature in the free-standing singly-supported beam implies the residual stress of the film changes as a function of its thickness [Sen 01, Tim 59]. In the case of the F-TEOS film, a downward curvature of the cantilever (see Figure 2.10(b)) indicates the top surface is under a higher compressive stress than the bottom. The average stress gradient is shown to be [Sen 01, Tim 59],

$$\frac{\Delta\sigma}{H} = \frac{1}{2} \cdot \frac{E}{1-\upsilon} \cdot \frac{1}{\rho}, \tag{2.12}$$

where ρ is the radius of curvature, which can be determined from the surface profiles by

$$\frac{1}{\rho} = \frac{\omega''}{[1+(\omega')^2]^{\frac{3}{2}}} , \qquad\qquad (2.13)$$

where ω is the vertical displacement as defined in Figure 2.12. This procedure is repeated for a number of beams with various dimensions. Applying the Young's modulus found from the nanoindentation experiments, 48GPa, and assuming a υ of 0.16 (similar to that of SiO$_2$), $\frac{\Delta\sigma}{H}$ for F-TEOS film is found to be $16.7 \pm 5.0 MPa/\mu m$.
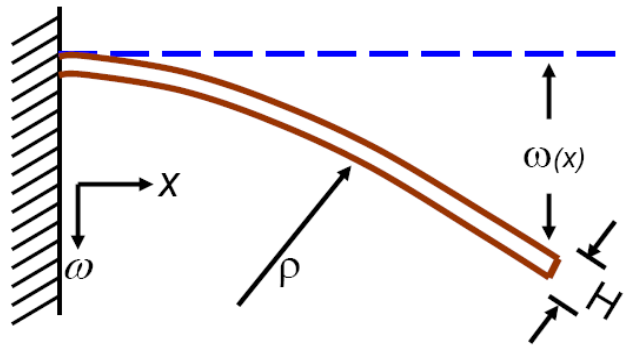
Figure 2.12 Definition of variables in Equation (2.12) and (2.13).

2.3.3 Residual Stress in F-TEOS Film

The profiles of the doubly-supported beams clearly indicate that these beams buckled upon being released from the substrate, due to a residual compressive stress. Both theoretical-based and FEM-based analyses of the residual stress present in F-TEOS film were performed.

Theoretical Analysis of Buckling

The critical stress required for a beam with length L to buckle can be derived by solving the Euler beam equation,

$$\tilde{E} \cdot I \cdot \frac{d^4 \omega}{dx^4} + (\sigma_0 HW) \cdot \frac{d^2 \omega}{dx^2} = 0, \qquad (2.14)$$

where $\tilde{E}$ is the bi-axial modulus, I is the moment of inertia of a beam, $\dfrac{WH^3}{12}$, W is the width of the beam, and σ_0 is the residual stress [Tim 59]. It is found that the critical stress required for buckling, the *Euler stress* is,

$$\sigma_{Euler} = -\frac{\pi^2}{3} \cdot \frac{\tilde{E} H^2}{L^2}. \qquad (2.15)$$

However, this solution does not relate the amount of buckling to the magnitude σ_0 beyond σ_{Euler}. An energy balance method, proposed by L. Nicu *et al.*, can be used to

address this problem [Nic 99]. The buckled beam's shape can generally be assumed to have the following form [Tim 63],

$$\omega(x) = \frac{A}{2}(1 + \cos\frac{2\pi x}{L}) = \frac{A}{2} \cdot u(x), \qquad (2.16)$$

where A is the amplitude of the buckled beam. L. Nicu *et al.* argued that the buckled beam shape is a result of contributions from both the in-plane elastic energy as well as the out-of-plane flexural strain energy [Nic 99]:

$$\varepsilon_{Total} = \varepsilon_{Elastic} + \varepsilon_{Flexdural}, \qquad (2.17)$$

where energy is denoted by ε. Upon reaching equilibrium, $\dfrac{\partial \varepsilon_{Total}}{\partial A} = 0$. It was further derived that this equilibrium condition produces the following formula relating A to σ_0 [Nic 99]:

$$\frac{H^2}{12}\int_{-\frac{L}{2}}^{\frac{L}{2}} u''^2(x)dx - [1 - (1 + \frac{\sigma_0}{\tilde{E}})\frac{1}{L}\int_{-\frac{L}{2}}^{\frac{L}{2}}(1 + A^2 u'^2(x))^{\frac{1}{2}}dx] \cdot \int_{-\frac{L}{2}}^{\frac{L}{2}} \frac{u'^2(x)}{(1 + A^2 u'^2(x))^{\frac{1}{2}}}dx = 0, \quad (2.18)$$

which can only be solved numerically. L. Nicu *et al.* also provided a MatLab-based numerical solver that could be used to accurately solve Equation (2.18). For doubly-supported F-TEOS beams with final dimensions fabricated in this study, Equation (2.18) can be solved to obtain Figure 2.13. Similar to the analysis of the stress gradient, the

Young's modulus found from the nanoindentation experiments, 48GPa, and υ of 0.16 (similar to that of SiO_2) were used here.

As Figure 2.13 shows, when the measured A, using the Wyko profilometer, at different beam lengths is correlated with the solution of Equation (2.18), almost consistent values of σ_0 were obtained. The differences are because of the geometrical contribution from the non-ideal support of the fabricated doubly-supported F-TEOS beam structures (see Figure 2.10(a)). Effectively, the undercuts added lengths to the beams, and widened the beams near the ends. This results in an increase of measured A than the model predicts. The non-ideal support in the case of long beams ($L=705\mu m$) has less contributions to the measurements than in the case of short beams ($L=140\mu m$). Therefore, a decrease in the correlated σ_0 is seen here as L increases.
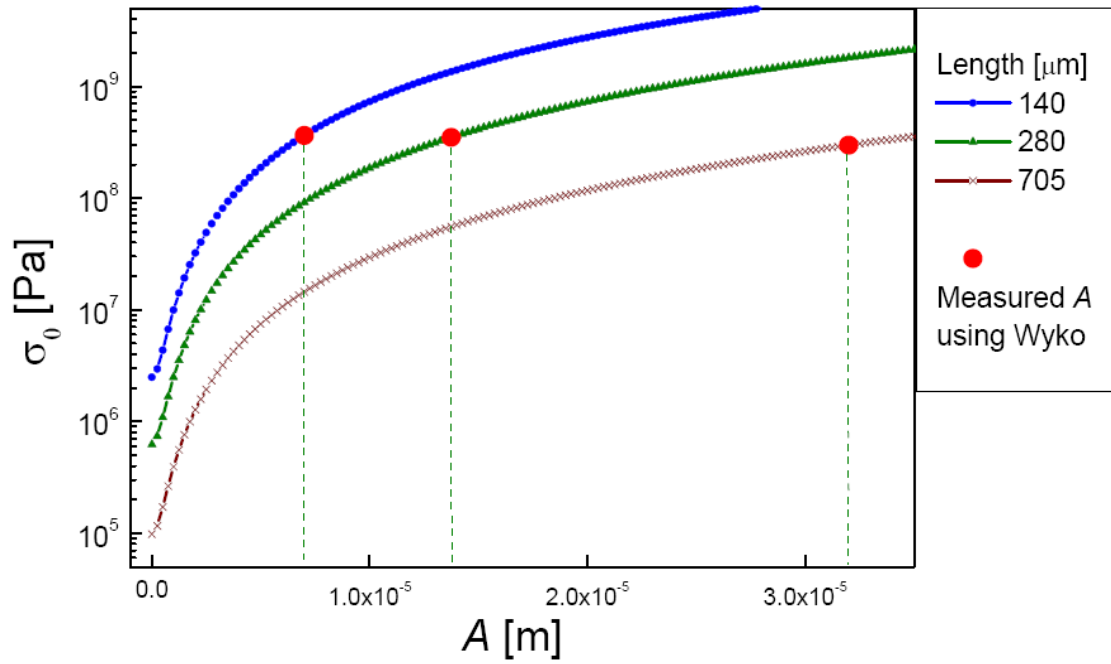
Figure 2.13 Numerical solution to Equation (2.18) for the three different lengths of doubly-supported F-TEOS beams. The measured buckling amplitudes by Wyko at different beams lengths correlate to different values of σ_0. This is due to non-ideal support contributions.

FEM Analysis of Buckling

In order to correctly address the geometrical effects of the non-ideal support, FEM analyses of the buckled shapes of F-TEOS beams were performed. The commercially available FEM software package available from ABAQUS Inc. (now Simulia, Providence, RI) was used to carry out these calculations. As shown in Figure 2.14(a), geometries similar to those observed using an SEM (Figure 2.10(a), for example) were created. Trials of various magnitudes of compressive stresses were induced in the elements created, and a small perturbation force was introduced to cause the FEM element to undergo buckling. For each trial, solutions of the spatial profiles (similar to that shown in Figure 2.14(b)) of the buckled beams were extracted and compared to actual measurements of F-TEOS beam buckling obtain using the Wyko system. It is worth noting in Figure 2.14(b) that the non-ideality of the support is manifested in the solution through the 'ripples' in the beam profile near the ends. It was found that a σ_0 of 233MPa (compressive) would produce an A value consistent with those experimentally observed for all three lengths of F-TEOS beams. This is close to the value of σ_0 correlating with the longest beam (L=705µm) in the theoretical solutions shown above. Similar to the analyses discussed above, the Young's modulus found from the nanoindentation experiments, 48GPa, and a υ of 0.16 (similar to that of SiO_2) were applied here.

(a)

(b)

(c)
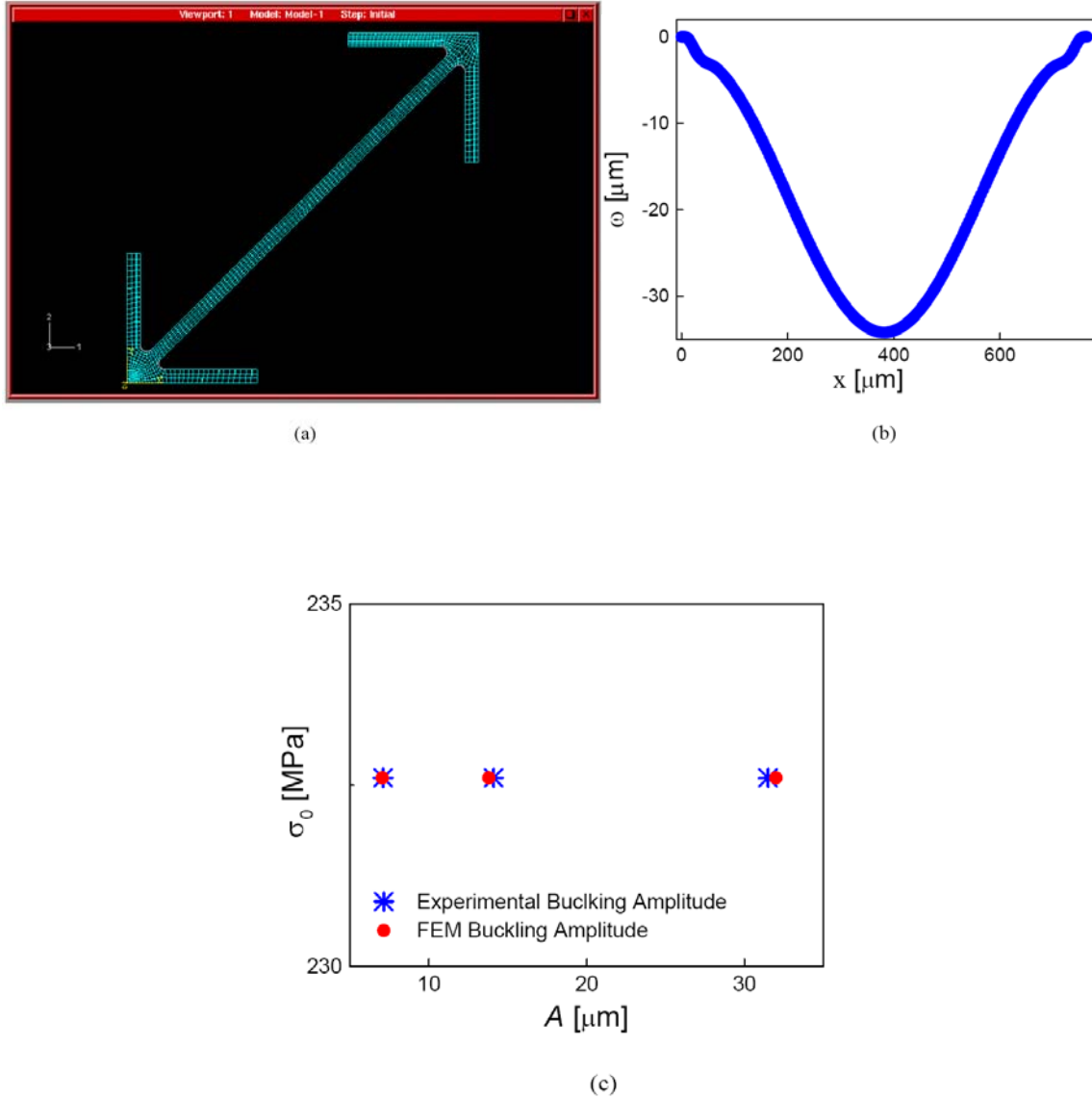
Figure 2.14 (a) Example drawing of a doubly-supported F-TEOS beam with non-ideal supports at the ends, similar to those shown by SEM observations. (b) Example solutions of the buckling of the F-TEOS beams with non-ideal supports. Note the 'ripples' near the ends of the buckling solution, which is a result of the particular non-ideal support. (c) Through trials of various magnitudes of σ_0 in the FEM analysis, a compressive stress of 233MPa produces beam buckling amplitudes similar to those observed using the Wyko system on the actual structures.

2.3.4 Modulus of F-TEOS Film

As shown above, upon releasing of the beams made of the F-TEOS film, substrate-independent properties can be extracted from measurements of the beam profiles. When such micro-cantilevers undergo deflections, the spring constants, correlated with the elastic modulus of the F-TEOS film only, without any substrate contributions, could also be determined. The deflection of the cantilever beams was induced using a modified AFM tip on a cantilever of a known length, which was attached to a Newport AD-100 (Newport Corporation, Irvine, CA) electrostrictively-driven actuation device (see Figure 2.15(a) for an illustration).

The commercially micro-fabricated Si-based AFM actuator tip used in this experiment has a well characterized length and ideal support. Therefore, the applied force during such experiments can be precisely calculated by applying the beam bending equation [Sen 01, Tim 59] to the bending profiles of the actuating beams,

$$F = (\frac{E_{Si}WH^3}{4L^3})\omega_{max}, \qquad\qquad (2.19)$$

where W, H, and L are 35, 1, and 350μm, respectively, for the MikroMasch CSC38/no Al/15 AFM cantilever beams used (MikroMasch USA, Portland, OR).

On the other hand, the analysis of the deflection data of the F-TEOS cantilevers is not as straight-forward as that of the actuator Si beam. The contributions by the non-ideal support should be corrected for. Following the analyses of J. Mencik *et al.* [Men 99], the following modified beam equation is valid for characterizing the non-ideality in the support through a correction length, L_C,

$$\omega = \frac{FL}{2\tilde{E}_C I}(x-L_C)^2(1-\frac{x-L_C}{3L}), \tag{2.20}$$

where $\tilde{E}_C$ is the corrected bi-axial modulus independent of any effects by non-ideal supports, i.e., the true intrinsic bi-axial modulus of the film. Figure 2.15(b) shows the values of uncorrected and corrected bi-axial moduli from deflection experiments using various lengths of F-TEOS cantilevers. Using this analysis, it is determined that $\tilde{E}_C = 53.1GPa$, which gives the Young's modulus of F-TEOS to be 44.6GPa when assuming υ of 0.16. It should be noted here that for the dimension of the beams used here, it is shown through FEM analysis that bi-axial modulus, rather than bulk modulus, should be used to characterize the beams, and anticlastic stiffening of by the beams during the deflections can be neglected also [Ber 04].
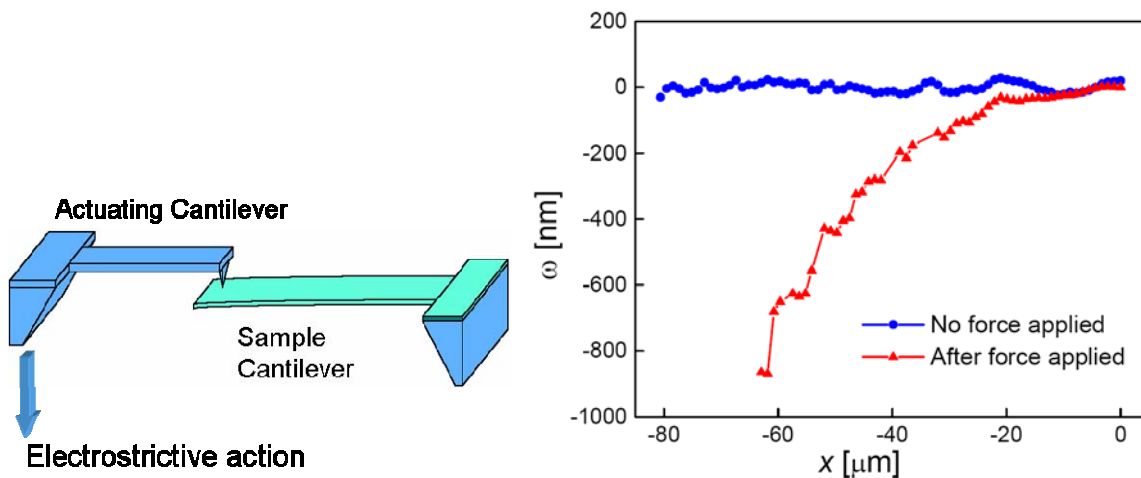
(a)
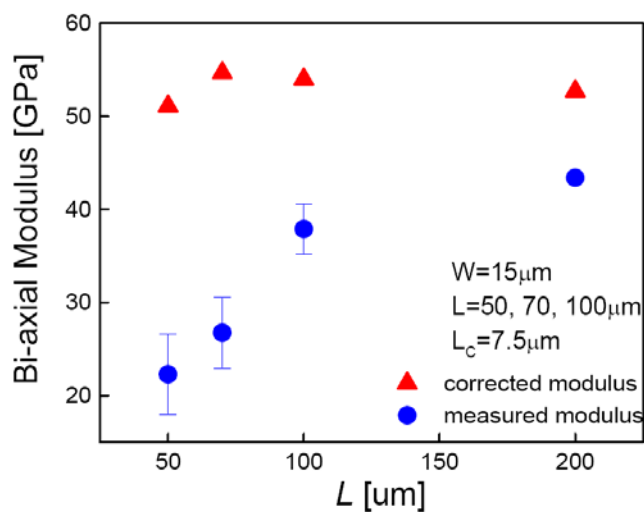
(b)

Figure 2.15 (a) Deflection of a singly-supported cantilever by an actuating cantilever. The deflection amount is measured using the Wyko system. (b) Experimentally determined bi-axial modulus from deflections of beams with various L and the corrected bi-axial modulus of F-TEOS film, after treatment of non-ideal supports.

2.4 Membrane Bulge Experiment

Since both KOH and TMAH solutions dissolve the blanket MSQ film, the membrane bulge test (with protective layers above and below the MSQ film) was explored as a characterization method in this case.

2.4.1 Experimental Procedure

The resin pre-cursor of JSR-LKD5109 was obtained form JSR Micro, Japan, to fabricate the film used in this experiment. Unlike the processes used for cantilever micro-fabrication, an anisotropic etch from the back side of the wafer is usually the most convenient way to produce membrane structures. A fabrication process and a mask design consisting of both square and rectangle features were devised (see Figure 2.16).

First, 5000Å of SiN was grown on both sides of the wafer using low pressure chemical vapor deposition method in the Integrated Circuits Laboratory (ICL) at MIT. Then, the back-side of the wafer was patterned using the MSQ membrane mask (Figure 2.16(a)) via photolithography and plasma etching at the Technology Research Laboratory (TRL). This was followed by anisotropic wet etching of the Si(100) wafer from the back side using KOH to create the membrane features. Lastly, spin-on deposition of 7100Å of MSQ and PECVD of 2000Å SiN was done at the EML. Using the wafer curvature technique described in Section 2.1, the residual stress of each layer was independently determined to be 50MPa tensile for the LPCVD SiN, 15MPa tensile for the MSQ film, and 75MPa tensile for the PECVD SiN.
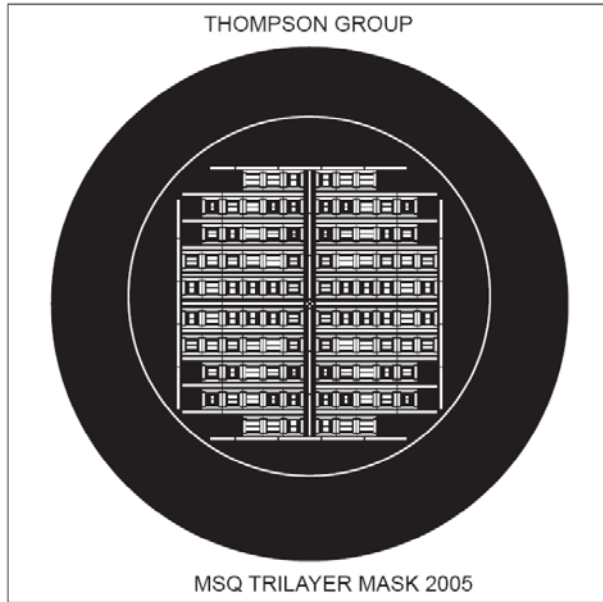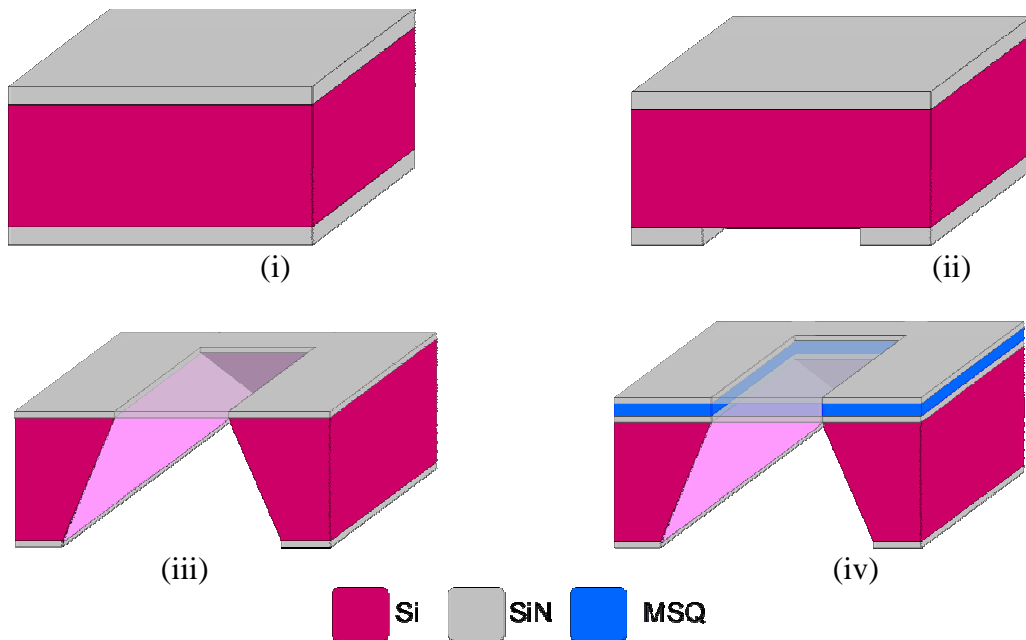
Figure 2.16 (a) Mask layout used in the MSQ membrane bulge experiment. (b) Schematic process flow of the fabrication process: (i) low pressure chemical vapor deposition of SiN on both sides of the wafer; (ii) patterning of the back-side using photolithography and plasma etching; (iii) anisotropic wet etch of the back-side; (iv) spin-on deposition of MSQ immediately followed by PECVD deposition of SiN.

Membrane structures consisted of different combinations of the layers described above were fabricated: (1) only the LPCVD SiN, (2) the LPCVD and the PECVD SiN, and (3) the complete MSQ-trilayer membrane structures. All membranes were made using 4-inch Si(100) substrates. The fabricated membrane structures were subjected to pressurized bulge tests using an apparatus similar to that used by Y. Li [Li 05]. The schematics are shown below in Figure 2.17. The pressure was produced using compressed air, and monitored by a pressure sensor. The over-pressure was maintained by sealing off the cavity below the membrane with a silicone gasket. The bulge deflection, h, as a function of the applied pressures, P, was recorded using the Wyko optical profilometer. Figure 2.17(b) shows example bulge measurements using square and long rectangular MSQ-trilayer membranes.
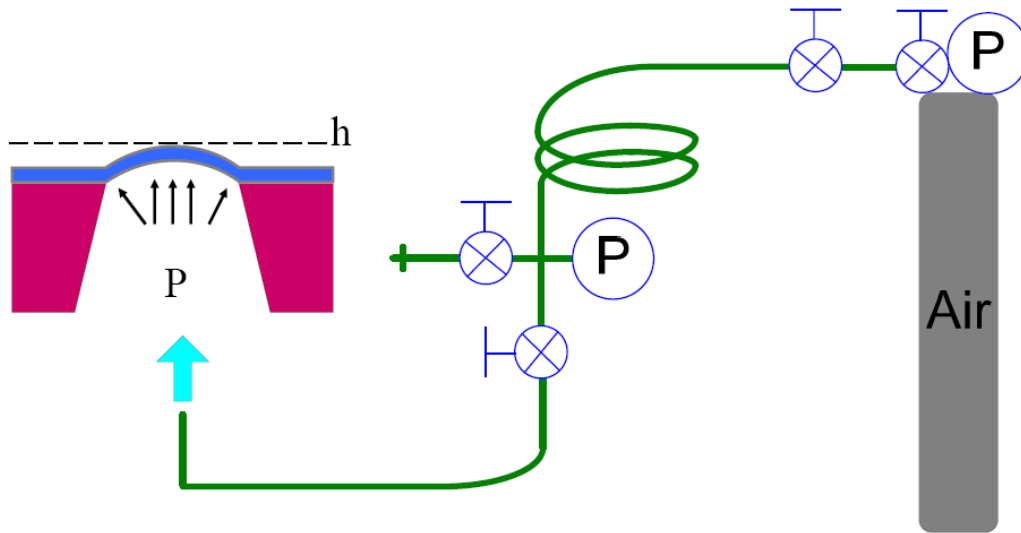
(a)
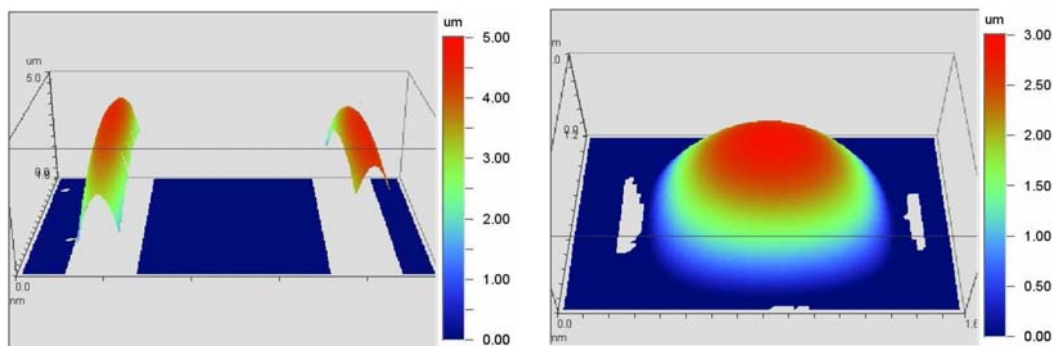
(b)

Figure 2.17 (a) Schematic diagram of the membrane bulge apparatus. (b) Examples of bulge measurements using long rectangular and square MSQ-trilayer membranes.

2.4.2 Results and Discussion

Since the amount of deflection induced during the bulge experiments were much smaller than the characteristic lengths of the membranes, the *small deflection approximation* can be used, such that [Hoh 99],

$$P = c_1 \cdot \frac{(\sigma_0 t)_{\textit{eff}}}{a^2} \cdot h + c_2 \cdot \frac{(\tilde{E} t)_{\textit{eff}}}{a^4} \cdot h^3 , \qquad (2.21)$$

where a is the characteristic length of the membrane, c_1 and c_2 are constants related to geometry, and the effective properties of the multi-layers are obtained according to

$$(\sigma_0 t)_{\textit{eff}} = \sum_i (\sigma_0 t)_i , \qquad (2.22)$$

and

$$(\tilde{E} t)_{\textit{eff}} = \sum_i \frac{(E t)_i}{1 - \upsilon_i} . \qquad (2.23)$$

For square geometries, c_1 and c_2 have the values of 3.393 and (1.966-0.613υ) [Hoh 99], respectively, while for long rectangular geometries (aspect ratio>4), c_1 and c_2 have the values of 2 and $\frac{4}{3(1+v)}$.

Figure 2.18 shows an example of a P vs. h plot for a 100μm wide long rectangular-geometry membrane with the three different combinations of film layers. It was observed that in general, since the film thicknesses of SiN layers were comparable to that of MSQ, the discernable contributions to the measurement by MSQ is nearly negligible prior to sample rupture. The expected elastic modulus of MSQ is only about 2% of that of the SiN films. Overall, very few data points could be generated in all sets

of tests. No curve-fitting was performed to extract the MSQ film modulus. However, when the theoretical predictions of made using Equations (2.21) to (2.23) were plotted along with the data obtained experimentally, like those in Figure 2.18, it is seen that the data broadly agrees with the model predictions when using a Young's modulus for MSQ films in the range of 4 to 6GPa. This agrees with the values obtained using nanoindentation technique.
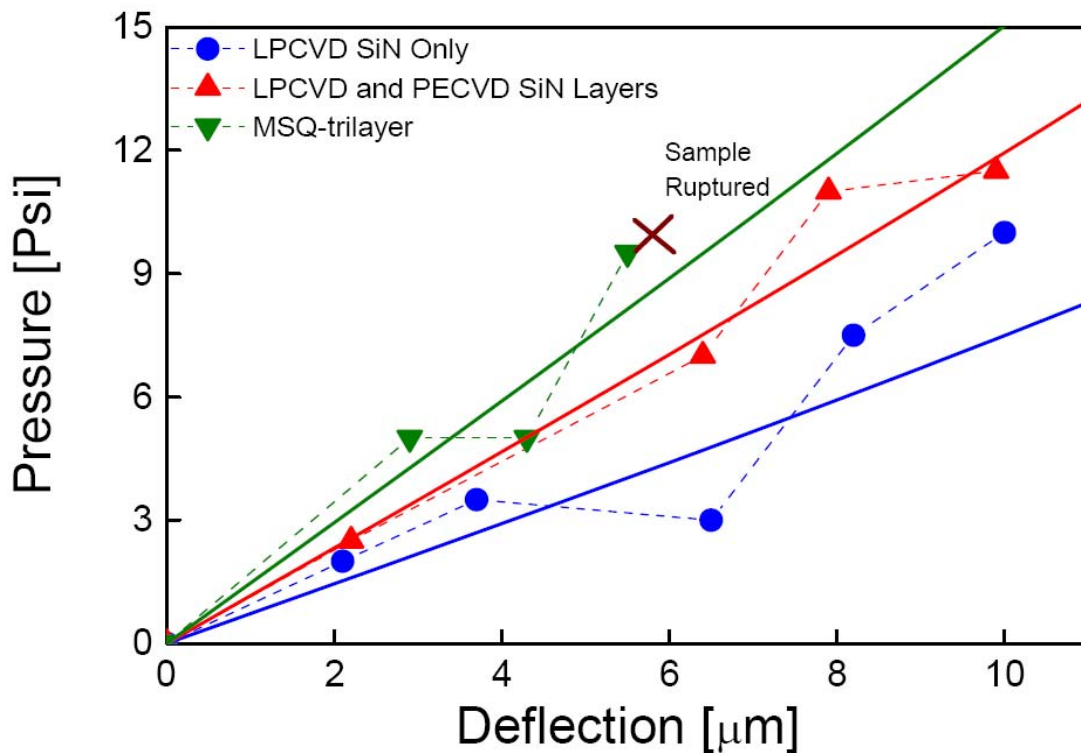
Figure 2.18 Example plot of membrane bulge vs. applied pressure in a 100μm-wide long rectangular geometry. It was seen that inconclusive results were generated due to the high thickness and modulus of the SiN layers. However, the data obtained broadly agrees with theoretical predictions when using a Young's modulus of 4 to 6GPa for the MSQ layer.

2.5 Chevron Notch Double-Cantilever Pull

The mode-I critical energy release rate for the Ta/SiN interface will be shown to be an important parameter in the analysis of extrusion failures induced by electromigration presented in Chapter 6, is studied here. Chevron-shaped notch structures illustrated in Figure 2.19 were produced at the TRL at MIT. Thermal compression bonding procedures similar to those presented by R. Tadepalli [Tad 07] were used. A 3500Å SiN film was deposited using the PECVD method, and the film was found to have a nearly zero intrinsic film stress. The thickness of the Ta film was close to 1100Å. Here, Cu films were used as 'glue' between the two bonded wafers, such that the weakest interface available for fracture was expected to be the Ta/SiN interface. All other layers were deposited using e-beam evaporation. Identical layers were deposited on both the wafer with the chevron notch patterns and the wafer without any patterns. The bonded wafers were then di-sawed into double cantilever samples, which were pulled apart using a Instron Microtensile Tester 8848 (Instron, Norwood, MA) at the Nanomechanics Lab at MIT. Force vs. pulling distance was recorded for each sample. See Figure 2.19 for an example curve.

The analysis of the measurements follows closely those presented by J. Bagdahn *et al.* [Bag 01] and R. Tadepalli [Tad 07]. The sample dimensions were $W = B = 1.0cm$ and $a_0 = 3mm$. The critical energy release rate of a mode-I crack at the Ta/SiN interface is found from,

$$G_{C,I} = \frac{(1-\nu^2)}{E} \cdot K_{C,I}^2 ,$$
(2.24)

and the mode-I critical stress intensity factor, $K_{C,I}$ is

$$K_{C,I} = \frac{F_{max} \cdot Y_{min}}{B\sqrt{W}},$$

(2.25)

where F_{max} is experimentally determined, and Y_{min}, a geometry factor, is [Bag 01]

$$Y_{min} = \frac{(5.805 \cdot \frac{a_0}{W} + 0.725)}{H^{\frac{3}{2}}},$$

(2.26)

where H is the thickness of two 4-inch wafers (the two substrates which were bonded). It

was determined that $G_{C,I} \cong 1.1 J/m^2$ for the Ta/SiN interface.
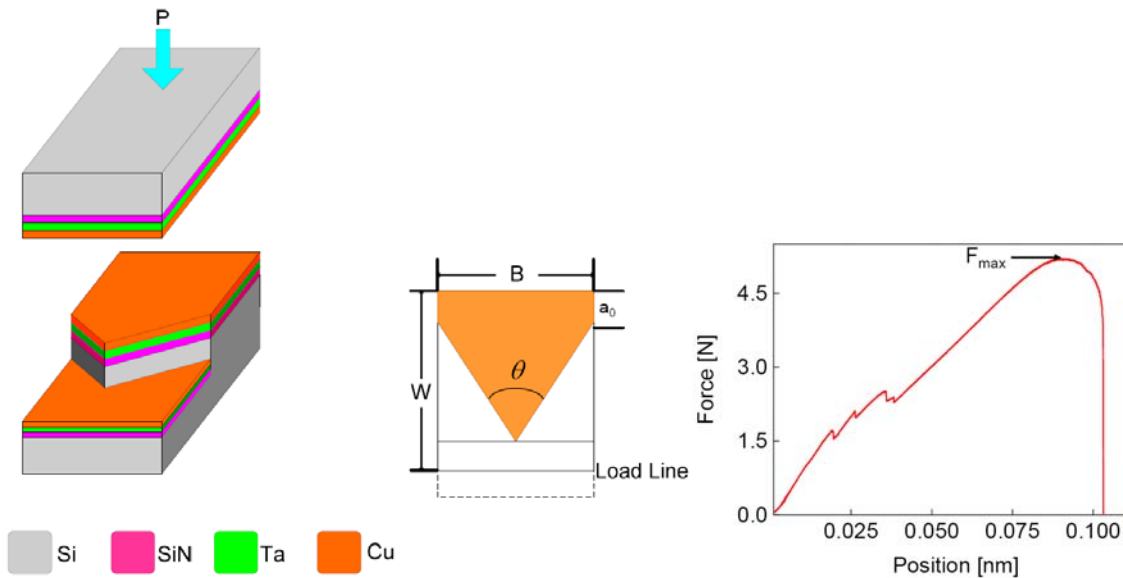
Figure 2.19 Illustration of the wafers bonded with a chevron notch of known geometry, along with an example pulling curve.

2.6 Summary

A suite of experimental characterization techniques, wafer curvature measurements, nanoindentation, micro-cantilever fabrication and deflections, and membrane bulge tests, related to the determination of Young's modulus of thin films, including low-k dielectric films, and chevron-shaped notch double-cantilever pull tests for characterization of the Ta/SiN interfaces were undertaken. For the two films in majority of the studies, F-TEOS and MSQ film, relatively consistent mechanical properties were extracted, most notably, $E_{F-TEOS} = 48 GPa$ and $E_{MSQ} = 4.5 GPa$. Since the low-k films studied here are so soft compared to many other commonly studied materials, such as, metallic thin films, in many cases, the limitations of the characterization techniques have became the limiting factor for accuracy. This calls for improvement in the characterization capabilities for low-k films for future IC generations, as their elastic moduli are expected to decrease even further. Nevertheless, characterization results obtained here were applied to FEM analyses in order to characterize the elastic response of Cu/low-k interconnect systems during the electromigration process. This is presented in the next chapter.

Chapter 3

FEM Studies of the Elastic Properties of Cu/Low-*k* Interconnect Systems

When electromigration occurs inside interconnects, metal atoms are displaced from the cathode towards the anode by the electron wind force. Macroscopically, however, it is the stress generated due to the changes in the atomic concentration that cause failure. Reiterating from Chapter 1, a change in the atomic concentration, $\dfrac{dC_a}{C_a}$, is related to a change in stress, $\partial\sigma$, through B, the effective bulk modulus of the Cu/low-*k* interconnect system [Kor 93]:

$$\frac{dC_a}{C_a} = -\frac{\partial\sigma}{B}\;.$$

<div align="right">(3.1)</div>

In this chapter, the elastic properties of all constituent parts, similar to those characterized by the experimental techniques reviewed in Chapter 2, are applied in FEM based analyses in which the elastic response of the Cu/low-*k* interconnect material system under hydrostatic loading is characterized. The dependencies of B on the mechanical properties of the constituent films are thereby explored.

3.1 Simulation Procedure

FEM analyses, similar to those carried out by S.P. Hau-Riege *et al.* [Hau 00a], were performed for a variety of interconnect geometries. The FEM code used was the commercially available ADINA software package (ADINA R. & D., Inc., Watertown, MA). In the FEM simulations to obtain B, a 3-dimensional space was constructed in which an interconnect structure consisted of the ILD, a Cu line bound by a Ta liner on the sides and bottom, and a SiN capping layer, along with the SiN etch stop layer on the top and bottom of the Cu line was modeled (see Figure 3.1). The thicknesses of the Ta and SiN layers were set to those in the interconnect structures fabricated by International Sematech. (In the FEM calculations relevant to the investigations shown in Chapter 5 and 6, geometries and dimensions appropriate for the Cu/low-k interconnect structures fabricated by AMD were used.) Due to the mirror symmetry with respect to the middle xz-plane, only half of the interconnect is actually needed to complete the calculations. However, full structures were created in this study. During data analysis, the half- and full-space-based calculations showed no difference for the calculations of B, as expected. The region where occupied by the ILD were assigned the properties of the various low-k ILDs considered, in order to observe the effect of the Young's modulus of the ILD on B. All material properties used in this investigation are listed in Table 3.1. A fixed boundary condition is applied to the xy-plane on the bottom of the interconnect structure (see Figure 3.1(a)) to approximate the extremely thick Si substrate (a 200 or 300mm-diameter Si(100) wafer). While all other boundary surfaces were allowed to move and bow under the applied loads, no rotation or twisting was allowed, which is expected for hydrostatic loading conditions. 3-D meshes with aspect ratios of 3 or less, generally

considered a good quality for meshing, were obtained using the procedures intrinsic to the ADINA software. A higher density of nodes and meshes were generated for the thinner layers in the material system, for example, the Ta liner.
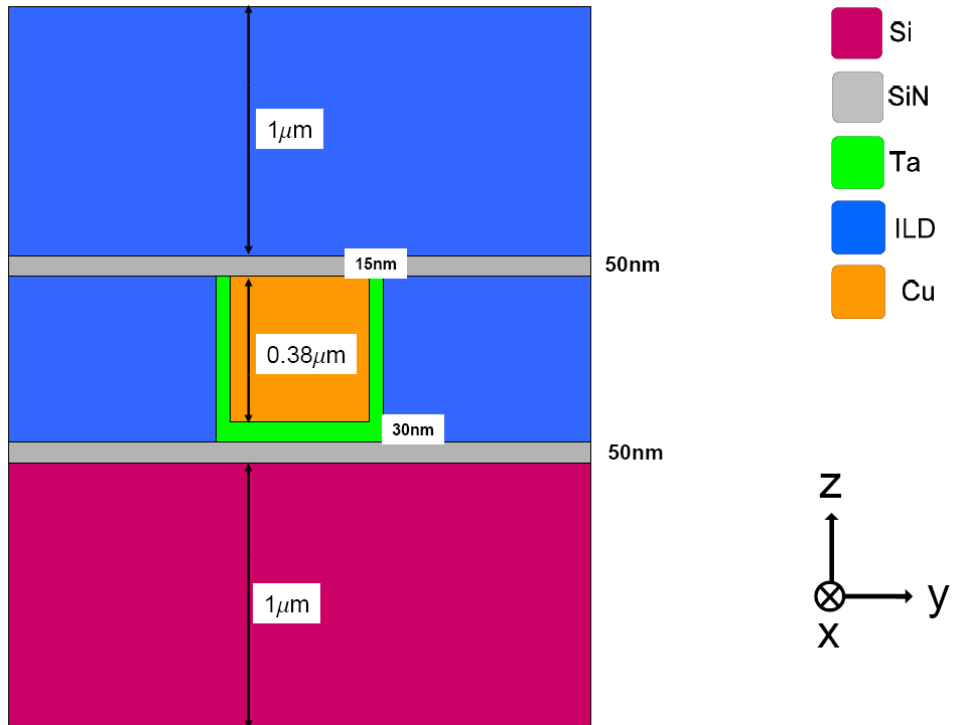
(a)
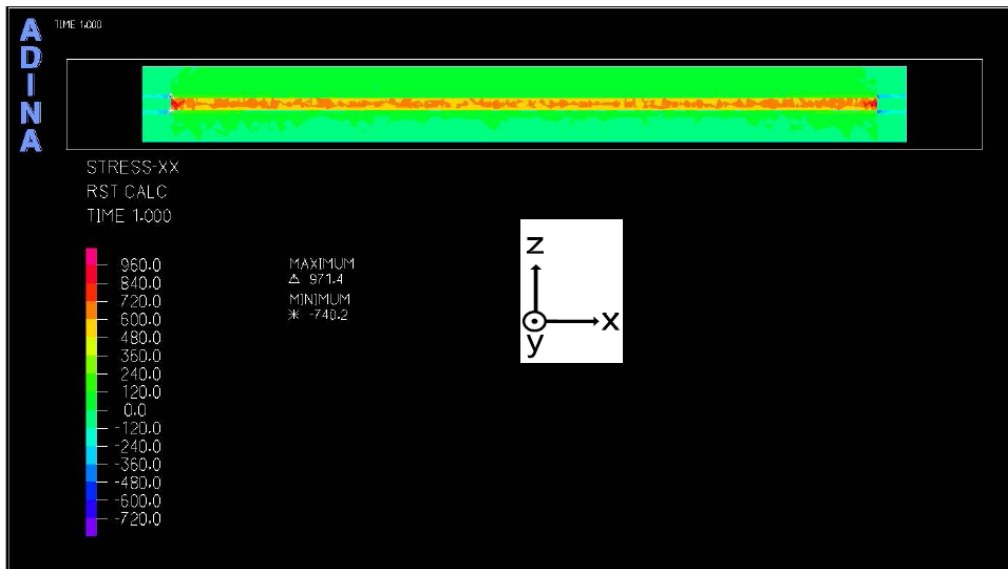
(b)

Figure 3.1 (a) Illustrative *yz*-plane view of the cross-section of the interconnect structures created in ADINA, with appropriate dimensions labeled. The length and width of the interconnect segment were varied. (b) *xz*-plane view of a 25μm-long interconnect segment underwent a 600MPa applied load.

Table 3.1 Elastic materials properties used in FEM analyses.

	Young's Modulus [GPa]	υ
Cu	120	0.33
Ta	186	0.34
SiN	221	0.27
Si(100)	180.5	0.215
SiO$_2$	77	0.16
F-TEOS	48	0.16
Black Diamond	14	0.16
SiLK	2.4	0.34

Following the formulism set forth by S.P. Hau-Riege *et al.* [Hau 00a], *B* is calculated as an averaged value, such that [Noy 87],

$$\Delta \equiv \frac{dC}{C} = \varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}, \tag{3.2}$$

and,

$$B = \frac{\Delta}{\sigma_{applied}}, \tag{3.3}$$

where ε_{ii} is the dilatational strain [Noy 87] and $\sigma_{applied}$ is a defined hydrostatic load applied to the region representing Cu in the FEM. Thus, the overall elastic response of the material system is characterized.
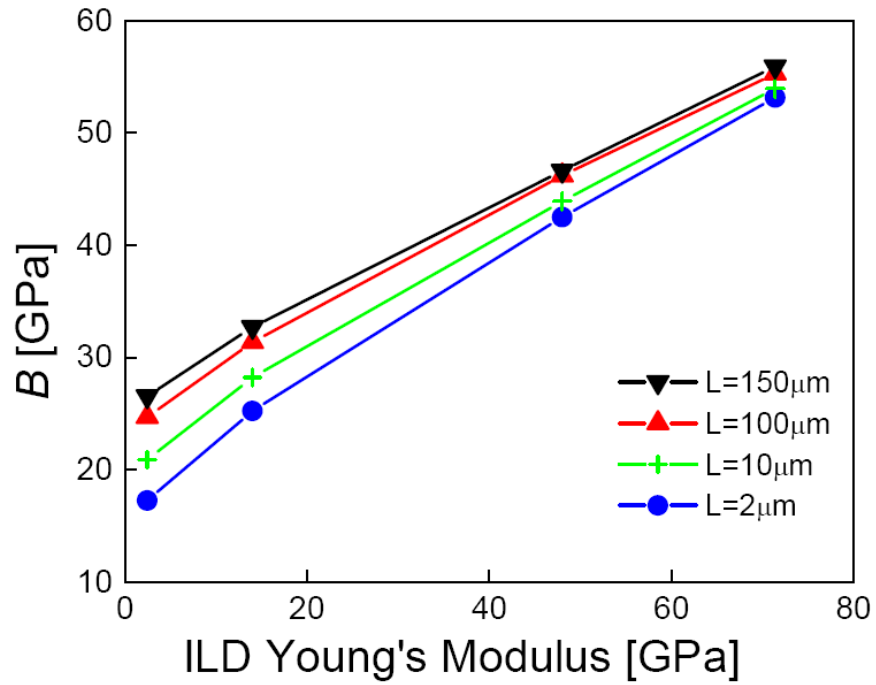
(a)
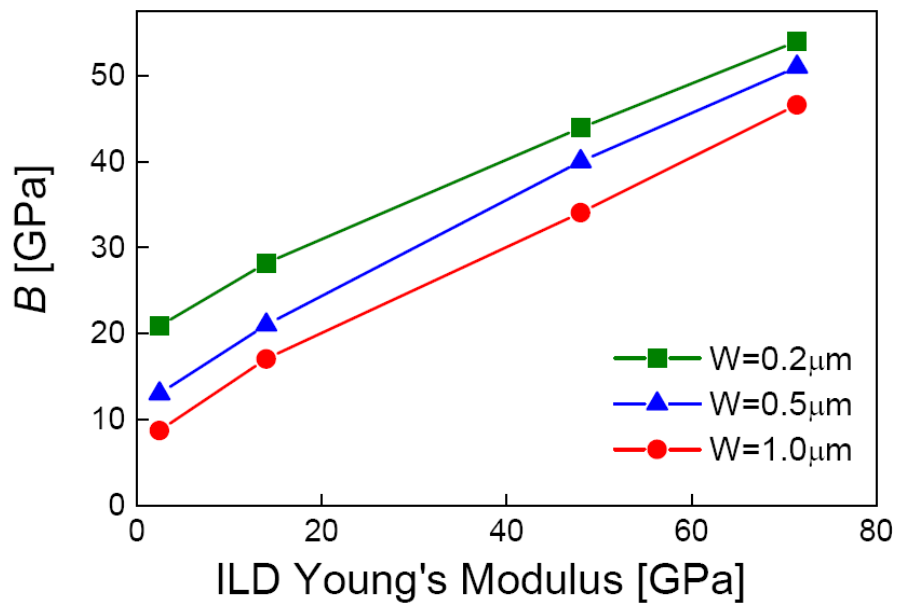
(b)

Figure 3.2 *B* calculated using various ILDs, (a) for a width of 0.2μm with different lengths and (b) for a length of 10μm with different widths.

3.2 Effects of Interconnect Dimensions on *B*

Both plots in Figure 3.2 show that, when the Young's modulus of the ILD decreases, *B* decreases as well. This is consistent with findings presented in [Hau 00a]. Ultimately, this results in a decrease in the thresholds required for failure for all failure mechanisms.

Figure 3.2(a) shows that *B* slightly increases with increasing line length. This is because, as the line length approaches infinity, the loading conditions transition from being hydrostatic to being plane-strain, and more low-*k* materials are replaced with much stiffer Cu in the axial direction. For elastically isotropic materials, the bulk and the plane-strain moduli are $\dfrac{E}{3(1-2\nu)}$ and $\dfrac{E}{1-\nu^2}$, respectively. For all the constituent films used in the Cu-based metallization system, υ is between 0.16 and 0.34, for each of the homogeneous materials, the plane-strain modulus is expected to be slightly larger than the bulk modulus. Therefore, it is also plausible that the effective plane-strain modulus is slightly larger than the effective bulk modulus in a multi-layer structure.

Regardless of the intermediate trends, as line length is increased toward infinity, the aspect ratio for the interconnect line becomes large. The modulus determined through the FEM method would be an effective plane-strain modulus, instead of an effective bulk modulus. However, the particular ratio of the two moduli depends on the particular geometry and material properties of the interconnect system. In Chapter 6, an effective plane-strain modulus, *M*, is accurately calculated using 2-D shell meshes, which enables the modeling of true plane-strain conditions, for the AMD interconnect structures and used in the analyses of Cu extrusions in Cu/low-*k* interconnects.

As the width of the interconnect increases, the interface area (covered with stiff Ta) of the Cu line per volume decreases. Therefore, less restraint by the Ta liner is exerted, resulting in a decrease in *B*. Figure 3.2(b) shows this trend with respect to line width.
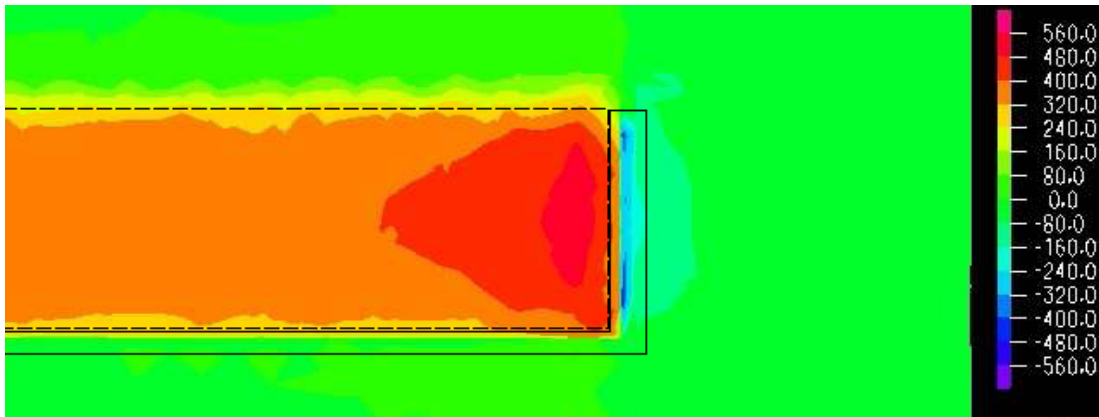
Figure 3.3 Local stress fields near the edge of the interconnect. The highest stress is generated in the region of the Ta liner.
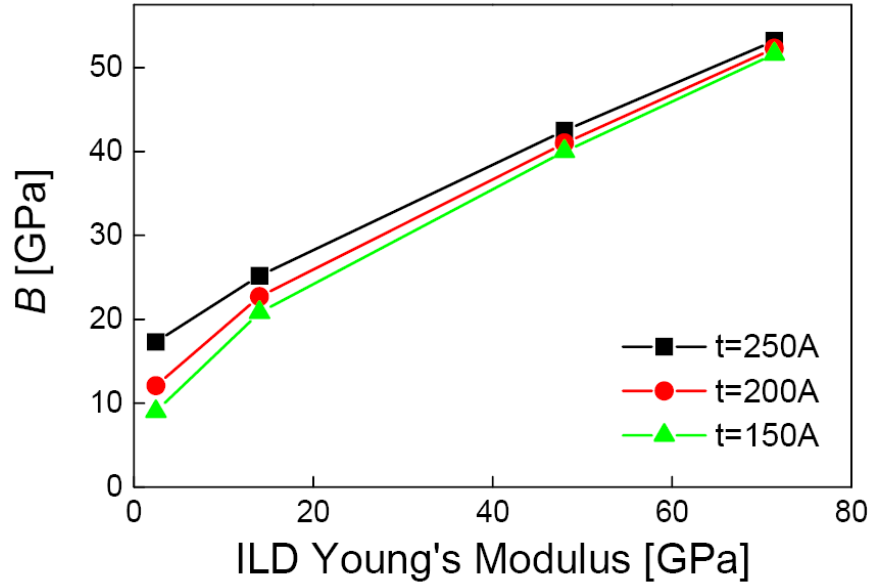
(a)
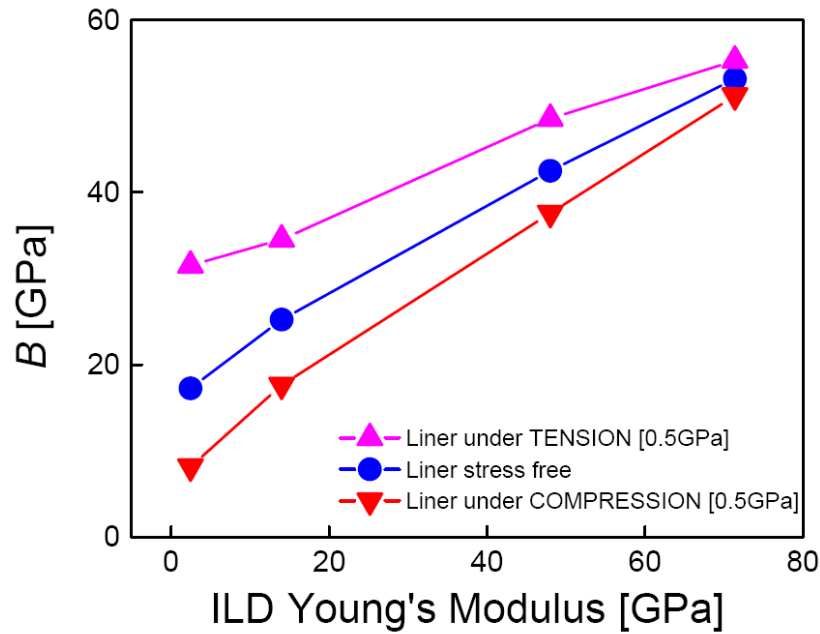
(b)

Figure 3.4 The effects of the Ta liner properties on B. (a) B for different ILDs with different Ta liner thickness. (b) B for different ILDs with different Ta liner residual stress. A compressive residual stress degrades B, while a tensile residual stress improves B.

3.3 Effects of the Ta Liner Properties on *B*

During the FEM analyses of *B*, it was observed that, because the refractory diffusion barrier, Ta in this case, has a high value of Young's modulus compared to that of the surrounding ILD, a large fraction of the stress generated in the surrounding material is concentrated near the Ta liner (see Figure 3.3). Therefore, even a small change in the liner could result in significant changes to *B*.

In future generations of interconnect technology, the thicknesses of diffusion barrier layers, including the Ta liner, is expected to decrease. FEM calculations using three different liner thicknesses, 150, 200, and 250Å, show that when the thickness of the liner decreases, *B* decreases also (see Figure 3.4(a)). This is because, as the Ta barrier thickness decreases, the side walls become less stiff. Similar trends in *B* as a function of the Ta barrier thickness have also been reported by K.-D. Lee *et al.* [Lee 03].

However, because Ta is usually deposited using sputtering techniques, a Ta film's intrinsic stress can vary over a wide range. D.W. Hoffman *et al.* [Hof 82] demonstrated that sputter deposited Ta films can have up to 1GPa of intrinsic stress, tensile or compressive, depending solely on the Ar pressure at which the film was sputter deposited. From the understanding about the elastic behavior of membranes, it is reasonable to imagine that an intrinsic tensile stress could have a positive effect on *B*. FEM studies were carried out on interconnect structures with the same dimensions, 0.2μm wide, 0.38μm thick, and 2μm long, but with only the stress state of the Ta barrier film varied. It is seen that, as expected, the interconnect structure having a Ta barrier under tension (0.5GPa) has a much stiffer elastic response than the one with zero-stress Ta barriers. On the other hand, when the liner has a compressive intrinsic stress, it

affects B negatively (see Figure 3.4(b)). Furthermore, as the divergence in the trends shown in Figure 3.4(b) indicate, the effect of the intrinsic stress of the liner on the overall elastic response of the Cu/low-k interconnect system becomes more pronounced when ILDs with decreasing k, decreasing moduli, are introduced.

3.4 Summary

Through FEM calculations, the overall elastic parameter, B, for Cu/low-k interconnects can be accurately determined by inputting experimentally well-characterized elastic properties of the constituent films. Also, such FEM investigations on interconnect structures with various geometries, and with the Ta liner barriers in various stress states, indicate that, first, when lower-k, lower-modulus, ILD films are introduced to Cu-based metallizations, the elastic properties will monotonically degrade. Second, such negative effects can be compensated for, to a small degree, by having a Ta barrier liner with a tensile intrinsic stress, and therefore a stiffer membrane confining the Cu interconnect segment. However, a compressive intrinsic stress in the Ta liner would further exacerbate the negative effects. B is also geometry dependent, such that interconnect line lengths and widths can change its value. In the case that the aspect ratio of the interconnect line becomes extremely large, it approaches plane-strain loading conditions, and the effective plane-strain modulus, M, can be calculated using FEM techniques.

Chapter 4

Electromigration Diffusive Properties of Cu/low-*k* Interconnects

As reviewed in Chapter 1, the dual-damascene fabrication process creates four possible diffusion paths for electromigration inside the Cu interconnects: the interface along Cu/capping-layer, the interface along Cu/Ta liner barrier, the Cu grain boundary, and within the Cu lattice. Among the four paths, the Cu/capping-layer interface is the most dominant. This chapter presents discussions relevant to this diffusion characteristic.

4.1 Dominant Diffusion Path for Electromigration

Several experimental studies have identified the Cu/SiN interface as being both the dominant diffusion path and the primary site for void nucleation in Cu-based interconnects, e.g., [Gan 01] and [Hau 02].

In experiments performed by Gan *et al.* [Gan 01], similar dimensions of via-to-via Cu/SiO$_2$ interconnect segments that only differed in whether the via was located above or below the test segment were subjected to electromigration experiments (see Figure 4.1(a)). An asymmetry in lifetimes was observed in that the t_{50}'s for structures with vias located below the test segments were consistently longer than those for structures with vias above the test segments (see Figure 4.1(b)). During failure analysis, it was reported

that voids forming along the Cu/SiN capping-layer interface had contributed to failure. During the experiments performed by Gan *et al.*, the Ta liners at the bottom of the vias were found to be fully blocking, so that the regions of the cathode-end vias were under highest tensile stresses. Smaller void volumes observed in via-above type interconnects compared to those in via-below type structures were consistent with the behavior seen in lifetime measurements. Therefore, the Cu/SiN capping layer interface was concluded to be the dominant diffusion path for electromigration and the primary sites for void nucleation.
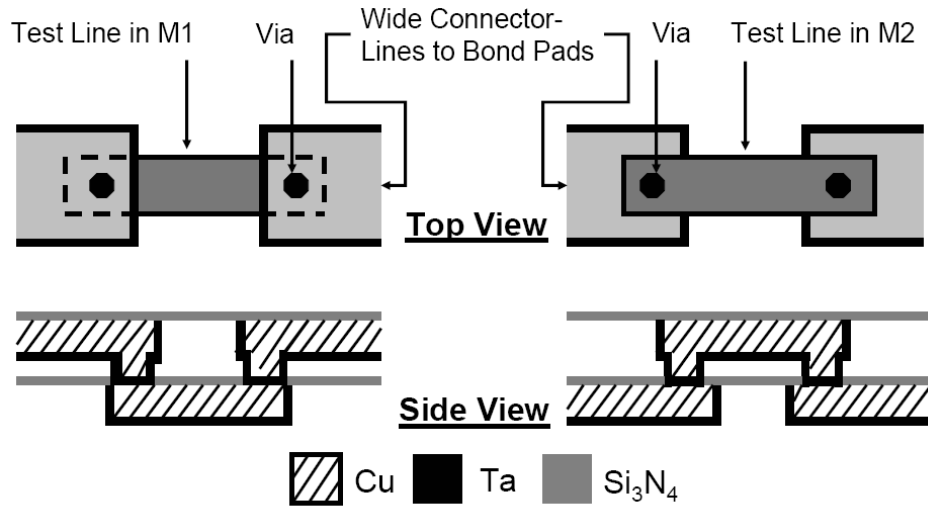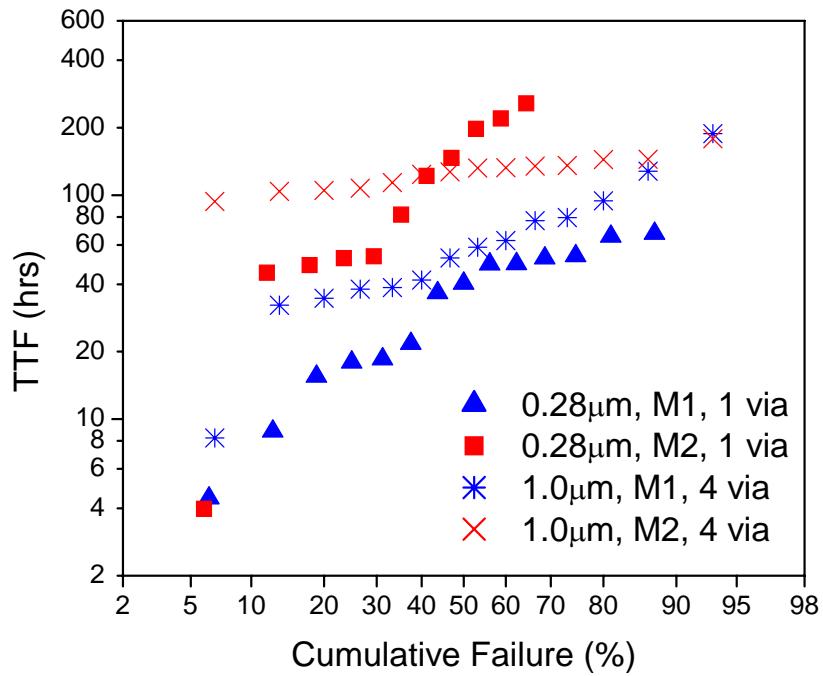
Figure 4.1 (a) Schematic illustrations of the via-above and via-below types of interconnect structures. (b) Time-to-failure for 800µm-long, 0.28µm-wide single via and 1.0µm-wide 4-via, M1 and M2 test structures stressed at 350°C and 2.5 MA/cm^2. Failure was defined as a 30% increase in resistance [Gan 01].

4.2 Critical jL Product Measurements

The conclusions provided by Gan *et al.* point to the fact that among the experiments reporting the critical jL products, such as, $jL_{crit} = 3700 A/cm$ in [Oga 01] and [Lee 01] for Cu/SiO$_2$ interconnects, $jL_{crit} \leq 2100 A/cm$ in [Hau 01] for Cu/SiO$_2$ interconnects, $jL_{crit} \leq 1500 A/cm$ in [Hau 03] for Cu/SiO$_2$ interconnects, and $jL_{crit} \leq 375 A/cm$ in [Hau 04] for Cu/low-k interconnects, where the low-k material was a carbon-doped SiO$_2$ material grown by PECVD, with a Young's modulus of about 10 GPa, the jL_{crit} obtained using via-above type interconnects was a result of much a smaller void volume than those determined using via-above type interconnects (see Figure 4.2). An extremely small, slit-like void forming underneath the cathode via will result in an open-circuit failure in via-above structures. On the other hand, a much larger void volume is required to cause resistance increase in via-below structures, because a small void forming at the Cu/capping-layer interface does not block the path for conduction. During the jL_{crit} electromigration experiments, the current density is kept at mildly low, resulting in a relatively low electron wind force and low amounts of stress development. A force balance easily occurs inside the interconnect over long periods of testing, producing very few or no failures. With the exception of [Oga 01] and [Lee 01], all other jL_{crit} studies were carried out using via-above type test structures in which the contribution from void growth is minimized due to the small void volume required for failure. Therefore, the reported jL_{crit} values using via-above interconnects closely approximate those for void nucleation, or the Blech immortality condition. In contrast, the jL_{crit} obtained using the via-below type of structure is that for void growth saturation.
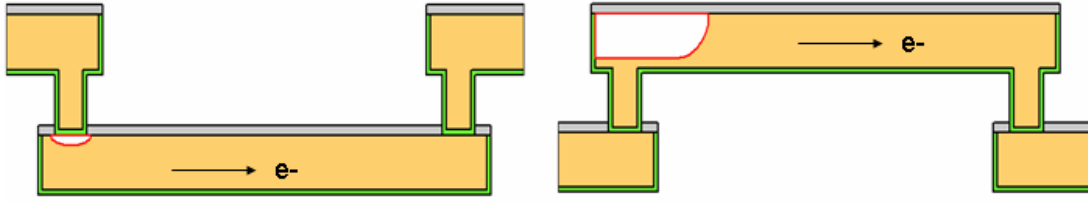
Figure 4.2 Illustration of the size difference in the void volume required for failure in via-above compared to via-below types of interconnects.

4.3 Critical Stress Required for Void Nucleation

Under the steady state of Blech immortality, $jL_{crit,nuc}$ is directly proportional to the stress required for void nucleation. Therefore, using the measured jL_{crit} obtained from via-above structures, $\sigma_{crit.,nuc}$ is estimated to be less than 41MPa in Cu/SiO_2 [Hau 02] and less than 25MPa in Cu/low-k interconnects [Hau 04]. Moreover, the failure analysis performed in [Hau 04] indicates that small voids still formed at the Cu/SiN interface despite the ILD being other than SiO_2. This fact indicates that changes in the mechanical properties of the interconnect system do not change the dominant diffusion path or the preferred site for void nucleation, the Cu/SiN interface. The decrease in measured $jL_{crit.,nuc}$ is explained through an energy balance argument, for which the strain energy released must be equal to the surface energy cost for void nucleation. Such an argument has been presented by Hau-Riege *et al.* [Hau 04], who find that

$$(jL)_{crit,nuc} \propto \sqrt{B \cdot \Delta\gamma} \,, \tag{4.1}$$

115

where B is the effective bulk modulus and $\Delta\gamma$ is the change in surface energy as a result of void nucleation. Therefore, as the ILD modulus is reduced in low-k dielectrics, $\sigma_{crit,nuc}$ is reduced [Hau 04].

Equation (4.1) also explains the fact that when the Cu/SiN interfacial adhesion is increased, such as, by the use of a layer like CoWP [Lan 03], which adheres better to Cu than SiN does, the reliability of the interconnect dramatically improves. Such processes, though, have not been proven to be manufacturable solutions to suppress electromigration. Therefore, Cu/SiN is the preferred site for void nucleation and growth for the foreseeable future.

4.4 Line Length Effects

As was reported in [Wei 02], package-level electromigration experiments were performed using via-above type interconnect structures fabricated by International Sematech and the Institute for Microelectronics (IME), Singapore. The test temperature was 350°C for all the experiments. The failure criterion was a 30% change of the initial resistance. The results are listed in Table 4.1. In this table, j is the current density, σ is the deviation in the log of the failure times, and '% unfailed' is the percentage of structures that did not fail.

Table 4.1   Lifetime data from electromigration experiments using via-above type interconnects at different lengths.

Structure	Length (μm)	Width (μm)	j (MA/cm^2)	t_{50} (min)	σ	% unfailed	Test time (min)
M1 (Sematech)	1000	0.3	2.0	2430	$\geq$1.22	7.7	16631
M1 (Sematech)	100	0.3	2.0	996	0.48	0	2373
M1 (Sematech)	50	0.3	2.0	4356	$\geq$1.01	25.0	9691
M1 (IME)	800	0.28	2.5	1720	$\geq$1.07	6.7	28731
M1 (IME)	100	0.28	2.5	1230	$\geq$0.85	6.3	11541
M1 (IME)	50	0.28	2.5	1262	0.62	0	23189
M1 (IME)	20	0.28	2.5	9820	$\geq$1.74	37.5	23189

It was found that at short lengths, the reliability of Cu-based interconnects improves. Also, some short Cu segments do not form voids that cause failure before back-stresses prevent the further growth of voids (see Figure 4.3). However, there is no apparent deterministic current-density line-length product jL for which all lines are immortal, similar to that was reported by S.P. Hau-Riege [Hau 02]. This is related to the absence of a conducting refractory-metal overlayer in Cu-technology that can shunt current around small voids. Secondly, it was found that at long lengths, a sub-population of Cu lines is immortal. Wei *et al.* postulated that this may be the result of rupture of the thin refractory metal liner at the base of the dual-damascene Cu vias. As a consequence of this complex behavior, median times to failure and lifetime variations are minimum at intermediate line lengths.

4.4.1 Short Length Effects in Cu Technology

Similar to the length effect study in [Wei 02], the investigations mentioned above in determining jL_{crit} also did not find deterministic values, despite the use of lower currents, and therefore lower jL than in [Wei 02]. In today's Cu-technology, SiN, an electrical insulator, is used as an inter-level diffusion barrier and as a capping layer for interconnects. Therefore, in test structures with a cathode via located above the test line, even when a small-volume void forms below a via, it can cause an open circuit failure if it spans the bottom of the via, as illustrated in Figure 4.2. As mentioned above, S.P. Hau-Riege reported $\sigma_{nuc.}$ to be less than 41MPa [Hau 02]. Thus, in via-above-type interconnects, true immortality requires that the conditions for void nucleation are not reached.

However, in via-below type interconnect structures, voids that nucleate and grow at the Cu/SiN interface must grow to span the entire line and the refractory metal liner must fail for an open circuit failure to occur. Therefore, in this type of structure, true immortality requires that the electron wind force not exceed the back stress, which is equivalent to the resistance saturation scenario in Al interconnects. However, actual resistance saturation is not observed experimentally, as the non-fatal voids that partially span the cross-section of the structure do not significantly increase the resistance of the line.

Wei *et al.* [Wei 02] found that for via-above structures, as the line length is decreased, the median-times-to-failure are highest at a jL product of 10000A/cm for the Sematech samples (L = 50μm), and 5000A/cm for the IME samples (L = 20μm). These line lengths were the minimum available on the fabricated structures. The jL products

suggest that void nucleation is highly probable inside the line, because they are higher than the $jL_{nuc.}$ reported by S.P. Hau-Riege [Hau 02]. Therefore, it is not surprising that the majority of the structures failed, as shown in Table 4.1. However, the jL products are in the range of the jL_{AR} values reported by Ho *et al.* [Oga 01, Lee 01]. This fact suggests that non-fatal voids could also exist in the M1-type interconnect segments, so long as the voids do not span the Cu cross-sectional area. An example is shown in Figure 4.3. Therefore, in the range of short lines investigated here, all lines are expected to have voids, but whether or not these voids lead to failure depends on their location and shape.
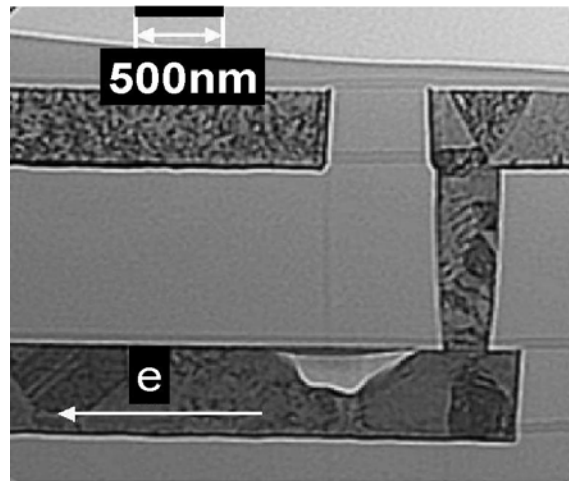
Figure 4.3 TEM image of a non-fatal void in an via-above test segment. Sample is from IME, L = 50μm; tested at j = 2.5MA/cm^2, 350°C.

4.4.2 Long Length Effects in Cu Technology

For the very long interconnect segments considered in [Wei 02], (1000μm and 800μm lines fabricated by Sematech and IME, respectively) high values of the lognormal variance, σ, were observed, and some lines never failed (see Figure 4.4). The stress difference, $\Delta\sigma$, that should develop in 1000μm-long lines tested at 2.0MA/cm^2, and 800μm-long lines tested at 2.5MA/cm^2, should both be approximately 5200MPa (taking a $z^*=1$ and $\rho=4.0\mu\Omega$-cm at 350^{0}C [Hau 02, Hu 99]). This stress is expected to cause void nucleation. However, the presence of a sub-population of immortal lines suggests that the refractory metal liners in one or both of the vias, in fact, did not block electromigration. It was proposed that the apparent immortality of a sub-population of long lines is the result of electromigration-stress-induced rupture of the Ta liners at the vias. Rupture of the liners would allow continuous flow of Cu to and from the connector lines and contact pads, which serve as large sinks and reservoirs for Cu [Hu 01]. It should be pointed out that while liner rupture can lead to an improved reliability in these and similar test structures, the presence of reservoirs and sinks would contribute to a reduced reliability in connecting lines on a circuit-level.
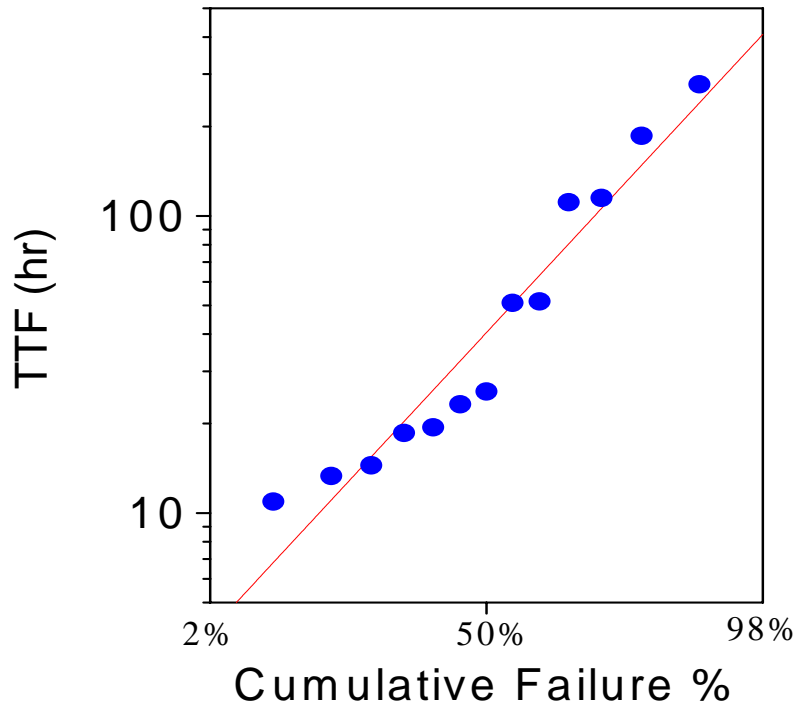
Figure 4.4 Example lognormal plot showing a high value of the lognormal variance, $\sigma > 1.5$, and a failure distribution suggests multiple modes of failures. This experiment was performed at 350°C and 2.0MA/cm^2, using 1000μm long via-above lines.

The results from these experiments using straight-line structures demonstrate two major characteristics of the reliability of Cu interconnects. First, the Cu/SiN interface degrades the reliability of Cu by providing a site for easy void nucleation and fast electromigration. Second, the Cu-filled vias may not be fully blocking in these particular samples. (Chapter 6 reports on the formation of extrusions induced by electromigration, and include the observations of fully blocking vias in samples from a more mature technology generation of interconnects.) The combination of the two aspects gives rise to the multiple failure mechanisms summarized in this chapter. This also suggests that characterization and improvements of Cu reliability should revolve around these two

issues. These results further suggest that different reliability models should be applied to via-above and via-below type of structures, and that, if vias do not form blocking boundaries, interconnect trees are no longer fundamental reliability units whose reliabilities are independent. Both of these results constitute profound differences from Al, and call for significant revision of circuit-level reliability assessment methodologies.

4.4.3 Joule Heating Experiment

At accelerated stress conditions during electromigration experiments, the amount of Joule heating must be quantified to ensure that testing conditions are valid. Since diffusivity is highly temperature dependent, Joule heating-induced thermal gradients are not desired during electromigration tests. A commonly acceptable level is 2 to 4°C increase.

The temperature coefficient of resistivity, TCR, or α, is defined by the following [Sch 94]:

$$R(T) = R_0(1 + \alpha \Delta T) \ , \tag{4.2}$$

where R_0 is the resistivity at a reference temperature. Solving for ΔT, the amount of Joule heating during an electromigration experiment, gives

$$\Delta T = \frac{\frac{R}{R_0} - 1}{\alpha} \quad .$$
(4.3)

α and Joule heating measurements were completed at wafer-level using a via-above interconnect structure with L=1000μm and W=0.3μm, fabricated by Sematech, similar to those used in the length-effect experiments in [Wei 02]. First, a nominal current density ($j=1.1 \times 10^5 A/cm^2$) was passed through the structure in order to obtain the resistance values at temperatures from 25 to 350°C. Using Equation (4.2), $\alpha = 3.1 \times 10^{-3} K^{-1}$ was obtained (see Figure 4.5(a)). Subsequently, while the temperature was fixed at 350°C, the current density was ramped from 1.1×10^5 up to $1.0 \times 10^7 A/cm^2$ in a short amount of time. The resistance values were recorded at current density increments (see Figure 4.5(b)). As shown in Figure 2.4, the results suggest that at a test temperature of 350°C and a current density up to $4.0 \times 10^6 A/cm^2$, Joule heating is not significant for Cu interconnects. (It should be noted that the experimental conditions, under which extremely long voids and extrusions were observed, as described in Chapter 6, was still below this limit.
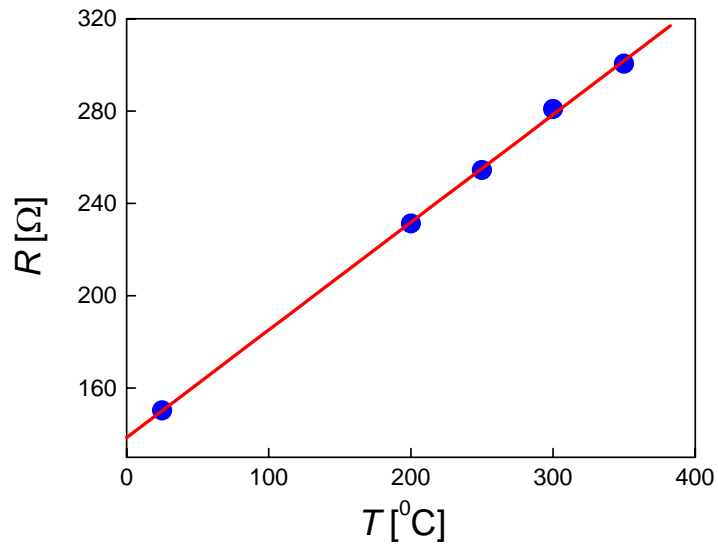
(a)
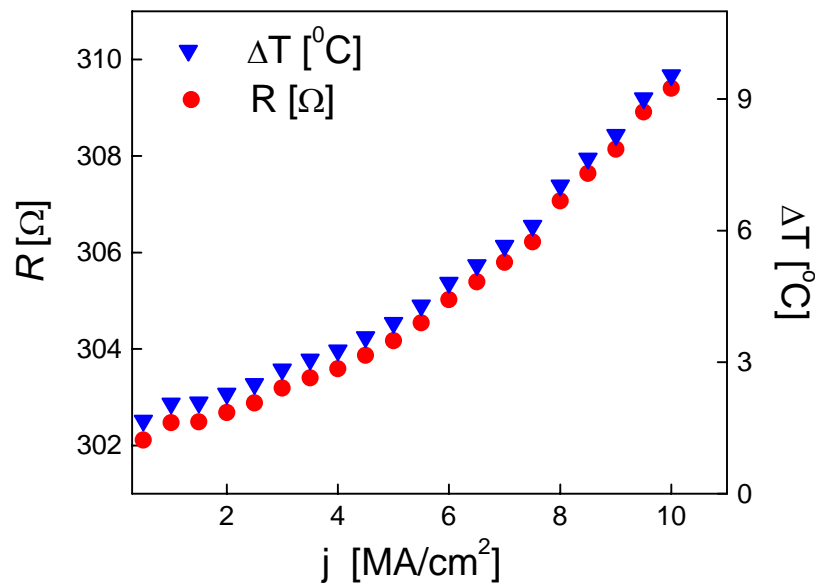
(b)

Figure 4.5 Joule heating measurement for a Cu-based interconnect, (a) R vs. T at nominal current density, (b) rises in T and R as j is increased to an extreme value at elevated T over a short amount of time. It is seen that even at 4.0MA/cm^2, there is negligible Joule heating.

4.5 Determination of Kinetic Properties of the Cu/capping-layer Interface

As shown in Chapter 5 and 6, accurate determination of the kinetic parameters for the electromigration process is crucial in reliability analyses. Several ways of quantifying the electromigration kinetics are discussed here.

Package-level electromigration experiments on both via-above and via-below type of Cu/SiO_2 dual-damascene interconnect lines were carried out. The structures were fabricated by Intel Corp., International Sematech, and IME Singapore. 16-18 samples were used per test. The failure criterion was a 100% change of the initial resistance. A number of combinations of test conditions were applied to the via-above-type interconnects as summarized in Table 4.2. Via-below type interconnects were tested with j= 2.0 and 2.5MA/cm^2 at 350ºC at two different lengths, 500 and 1000μm.

Table 4.2 Values of v_d [x10^{-4}µm/hr]; values of ΔH [eV]; and values of *j*-exponent. ΔH was obtained from a linear fitting of lnv_d vs $1/T$ at the same current densities. The *j-exponent* was obtained from linear fitting of logv_d vs log$j$ at the same temperatures.

*, **   The M2 structures used at the two different current densities shown here were fabricated by two different companies. All of the M1 structures were fabricated at the same third location.

*** This v_d value was extrapolated using *j*-exponent=1.0, at T=350ºC.

T [ºC] *j* [MA/cm²]	250	(via-above) 300	350	(via-below) 350	ΔH [eV]
1.0	5.6±3.0		88±16		0.82±0.05
1.5	6.4±1.8	18.1±3.6	106±41		0.78±0.06
2.0	11.8±4.7	26.4±6.4	213±108	300±56*	0.81±0.08
2.5	18.8±7.1		191***	250±150**	
j-exponent	1.2±0.3	1.3±0.4	0.9±0.3		

(a)

(b)

(c)

(d)
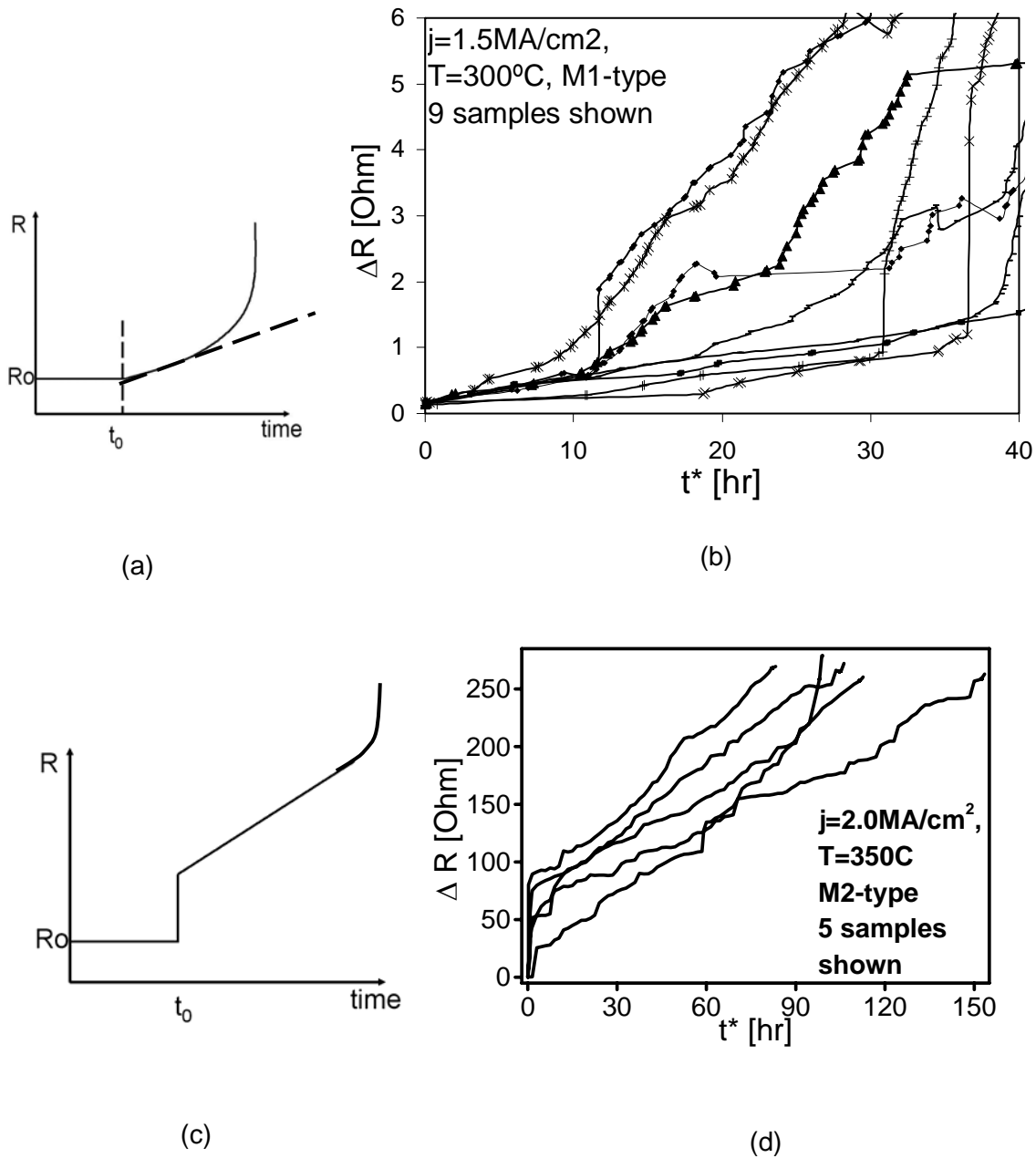
Figigure 4.6 Schematic Resistance versus time trends observed for (a) via-above-type and (c) Via-below interconnects. (b) and (d) are examples of normalized R vs t plots showing a regime of steady resistance increase. The ordinates are the resistance increase, $\Delta R = R - R_0$. On the abscissa, t^*, designates the difference between the actual test time and the incubation period, t_0.

For both via-above and below structures, regimes in which the resistance of the structures increased linearly with time, were observed (see Figure 4.6). For the experiments performed using via-above-type interconnects, the lowest value of the jL product was 7000A/cm. This value is larger than the $(jL)_{crit.,nucleation}$ reported by Hau-Riege [Hau 02, Hau 03]. This fact suggests that voids are expected to form inside the Cu. We postulate that the resistance increase observed was due to void growth in the interconnects. It was postulated that during void growth here, the contact area between the via and the line would decrease. The via resistance of the structure increases inversely proportional to a decrease of the contact area. Open failure occurs when the slit-like void spans the entire contact area. A uniform void growth was assumed, corresponding to a steady state resistance increase.
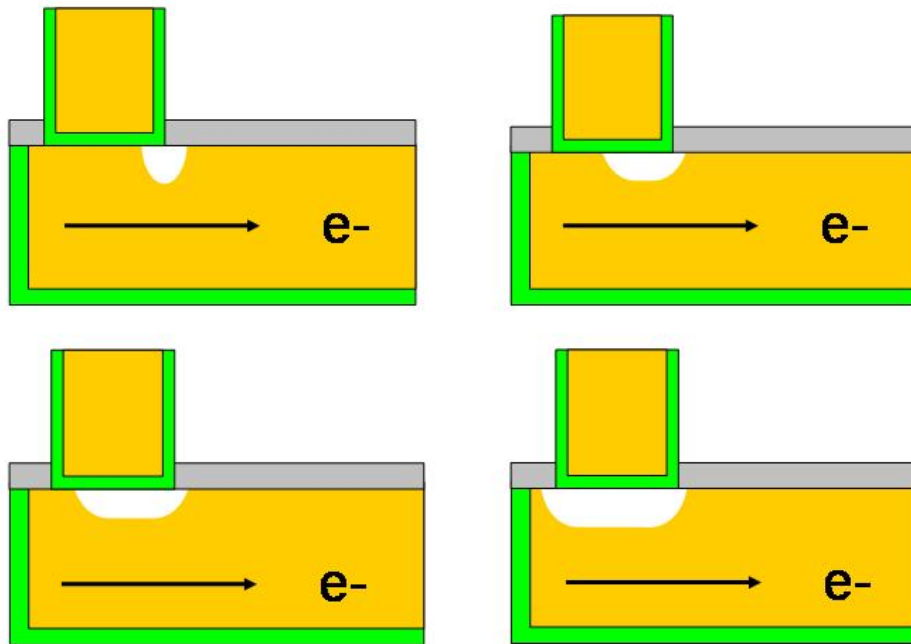
Figure 4.7   Cross-sectional view of a slit-like void growth process in via-above interconnects during electromigration.

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Under such assumptions,

$$\frac{dA}{dt} = (-L)\frac{dx}{dt}, \tag{4.4}$$

where A is contact area, and L is the size of the via $\frac{dx}{dt}$, i.e., v_d, was calculated using,

$$v_d = \frac{dx}{dt} = \frac{(\frac{dR}{dt}) \cdot L}{R_{via,0}}, \tag{4.5}$$

where $R_{via,0}$ is the initial via resistance at the testing temperature.

The slopes of the normalized R vs. t plots at $t^*=0$ were used to estimate v_d using Equation 4.5. As the results in Table 4.2 show, the activation energy is 0.80 ± 0.06eV. This value is consistent with that obtained using the failure lifetimes of the same structures (0.8 ± 0.1eV). Furthermore, this value of the activation energy is also in close agreement with literature values, which range from 0.7 to 0.9eV [Hu 99, Lin 02, Lan 03].

The analyses of the drift behavior of via-below structures are identical to that shown in later chapters. Therefore, the calculations are not repeated here. However, it is important to note that v_d results were similar for both via-above and via-below structures, and the values were also similar among the different sample suppliers (see Table 4.2).

4.6 Circuit-level Reliability Assessment Tool, *SysRel*

The accurate understanding and characterization of the electromigration phenomena in dual-damascene Cu interconnects prompted the development of an circuit-level reliability assessment approach appropriate to Cu metallizations. Consequently, an interconnect reliability assessment tool, *SysRel*, that is capable of characterizing the reliability of full-chip layouts has been developed [Ala 04, Ala 05]. *SysRel* incorporates many concepts that are applicable to Al-based as well as Cu-based interconnect circuits reliability analyses, namely, interconnect tree extraction from the circuit, determination of the highest-stressed path in a tree, jL_{max}, which was first conceptualized by S.P. Hau-Riege *et al.* [Hau 00c, Hau 01], as well as the general default model for estimating the time required for failure for an interconnect tree declared to be 'mortal.' Additionally, through experimentations on Cu/SiO_2 interconnect tress, Gan *et al.* [Gan 03] validated the conservative estimations of the default model for Cu interconnect trees.

However, stemming from the experimental understanding about the difference in void volume required for failure with respect to the direction of the electron flow in a via, *SysRel* adopted a filtering algorithm appropriate for Cu interconnects (see Figure 4.8). Different jL_{crit} filters are used for jL_{max} in trees that are classified as via-above or below. Default models with appropriately determined kinetic parameters, and stochastically distributed non-blocking vias, which result in trees with much longer L_{max}, are also among the features appropriate for Cu-based circuit analyses. Lastly, full-chip reliability analysis through the accumulations of the FRUs from any given circuit is communicated through a computer interface (see an example screen-shot in Figure 4.9) [Ala 04, Ala 05].
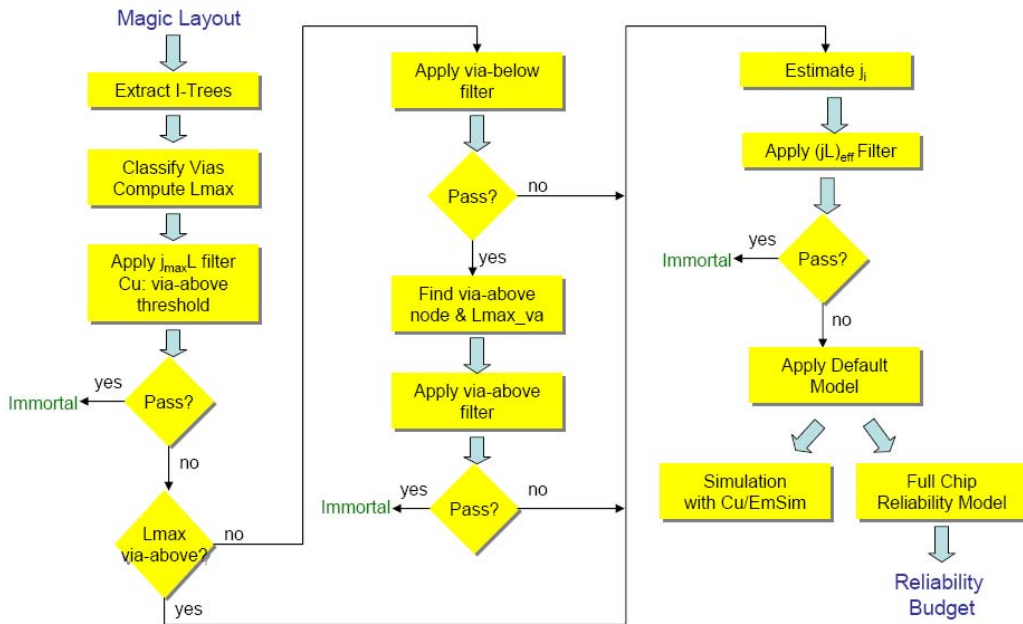
Figure 4.8 Flow diagram for Cu-interconnect circuit-level reliability analyses using *SysRel* [Ala 04, Ala05].
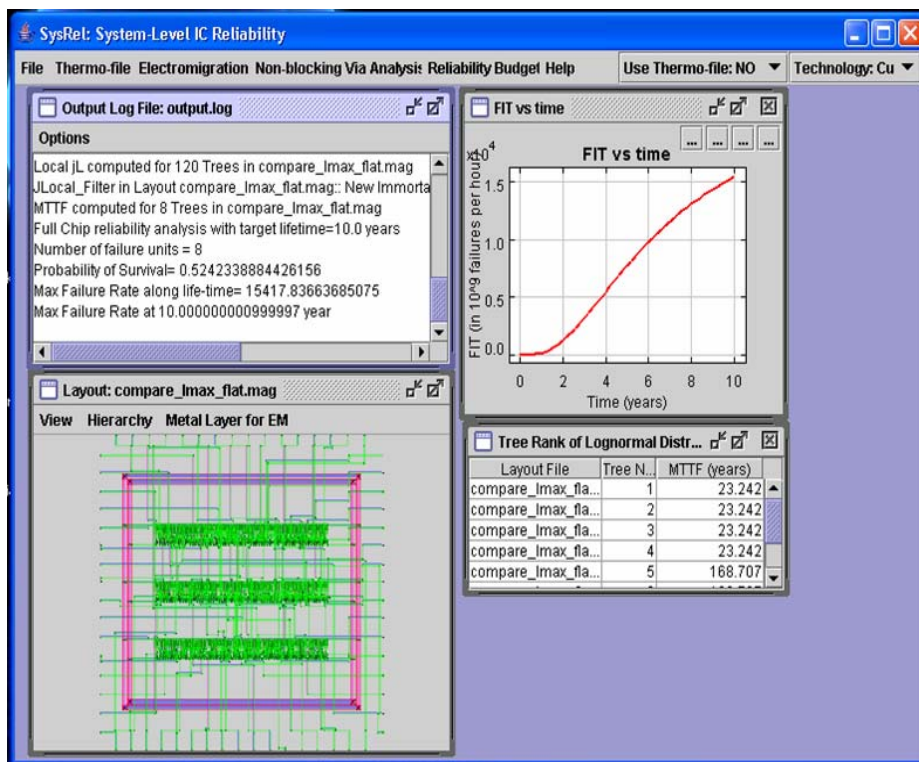
Figure 4.9 Screen-shot of *SysRel* performing reliability analyses on a 32-bit comparator circuit layout.

When the appropriate materials properties were changed in *SysRel*, from those of the stiffer SiO_2 to those of the softer low-*k* dielectrics, namely, *B* and *jL$_{crit}$*, it was demonstrated that the overall circuit-level reliability monotonically decreases [Ala 04a, Ala 05a, Ala 05b]. Therefore, a continued effort in the understanding of the failure mechanisms in Cu-low-*k* interconnects is required. An improved experimentally-based understanding of failures due to electromigration-induced void growth and extrusion is the focus of discussion in the next two chapters of this dissertation.

4.7 Summary

Due to the low threshold required for failures by void nucleation in Cu interconnects at the Cu/SiN capping layer interface, Blech immortality is not observed. This impacts not only the design of circuits, such as, new via redundancy schemes, but also led to a requirement for new characterization techniques for electromigration kinetics as well as a new hierarchical methodology and a new circuit-level reliability assessment tool, *SysRel*, for Cu/low-*k* interconnects.

Chapter 5

Effects of Active Atomic Sinks and Reservoirs on the Reliability of Cu/low-*k* Interconnects

Electromigration experiments using Cu/low-*k* interconnect tree structures were carried out in order to study the effects of active atomic sinks and reservoirs on interconnect reliability. In all cases, failures occurred after a long period of void growth. Kinetic parameters were extracted from resistance versus time data, giving $(Dz^*)_{0,eff} = 3.9 \times 10^{-10} \, m^2 / \sec$ and $z^* = 0.40 \pm 0.12$. Using these values, the evolution of stress in each of the interconnect tree segments could be calculated and correlated with the rate of void growth and failure times for all test configurations. It is demonstrated that segments that serve as atomic sinks and reservoirs for the failing segments affect the lifetime by modifying the conditions for stress induced migration. Reservoirs can lead to increased lifetimes, while sinks can lead to reduced lifetimes. Quantitative predictions of the times required for failure for Cu/low-*k* interconnect trees as a function of the effective bulk elastic modulus of the interconnect system, *B,* are made. As the Young's modulus of the inter-level dielectric (ILD) films decreases, *B* decreases, and the positive effects of reservoirs are diminished and the negative effects of sinks are amplified.

5.1 Introduction

As reviewed in Chapter 1, Korhonen equation [Kor 93, Cle 95] models all electromigration phenomena. Recall from Chapter 1,

$$\frac{\partial \sigma}{\partial t} = \frac{\frac{\Omega}{kT} \frac{\partial}{\partial x}\left[D_v C_v \left(\frac{z^* q \rho j}{\Omega} + \frac{\partial \sigma}{\partial x} \right) \right]}{\frac{C}{B}\left(1 + \frac{B\Omega}{kT} \frac{C_v}{C} \right)}. \tag{5.1}$$

This differential equation can be correctly solved using XSim, a MatLab-based numerical solver developed at MIT [Cho 04, Cho 07]. Applying accurately determined mechanical and diffusive properties, solutions of the Korhonen equation provide great insights to the reliability behaviors of via-to-via segments and interconnect trees alike.

The reliability of simple interconnect trees implemented in Cu/SiO$_2$ technology has been evaluated in earlier studies [Gan 03, Cha 06]. It was found that, because connected segments act as atomic sinks and reservoirs, even inactive segments (segments without current) can affect the reliability of connected segments. The purpose of the study reported here was to investigate the effects of both active and inactive segments on the reliability of other segments in a tree in Cu/low-k interconnects, in order to quantify the effects of changes in the ILD modulus on the reliability of Cu-based interconnect trees. As will be shown in later sections, the solutions to the Korhonen equation under different experimental conditions established the basis of the analyses.

5.2 Experiments and Results

We performed package-level electromigration experiments using interconnect tree structures fabricated by Advanced Micro Devices, Inc (AMD). The low-*k* ILD consisted of a form of carbon-doped SiO_2-based material deposited using PECVD, with a Young's modulus of 10GPa, and a Poisson's ratio of 0.16. The capping layer was a 50nm-thick layer of SiN-based film and a Ta-based diffusion barrier with a thickness of 15nm at the bottom and 10nm on the sides of the Cu lines was used. The test structures had an approximate 0.10μm-wide by 0.16μm-deep cross-section, with 0.13μm-wide vias located above the test lines, resulting in via-landing areas slightly wider than the interconnect width. Figure 5.1 shows the dimensions and layout of the test structures. We refer to the two interconnect tree structures in this diagram as 'asymmetric-dotted-I' and 'asymmetric-T' structures. Using the FEM formalism developed by S.P. Hau-Riege [Hau 00a], we calculated an effective modulus B of 17GPa for these interconnect tree structures.
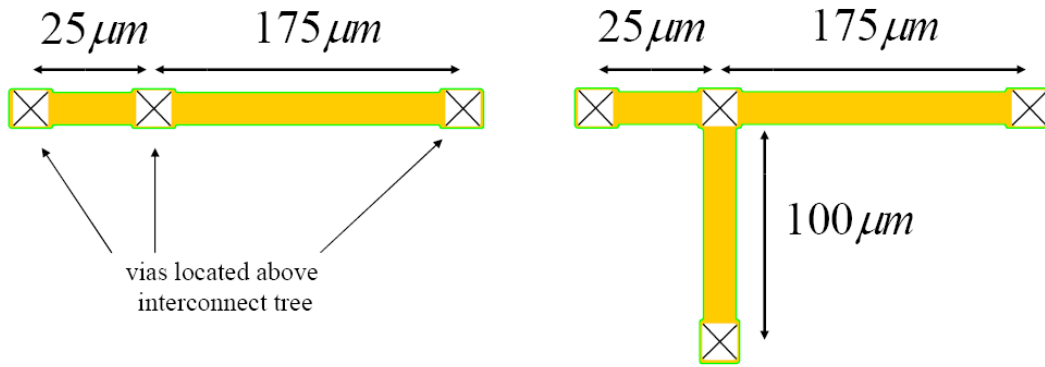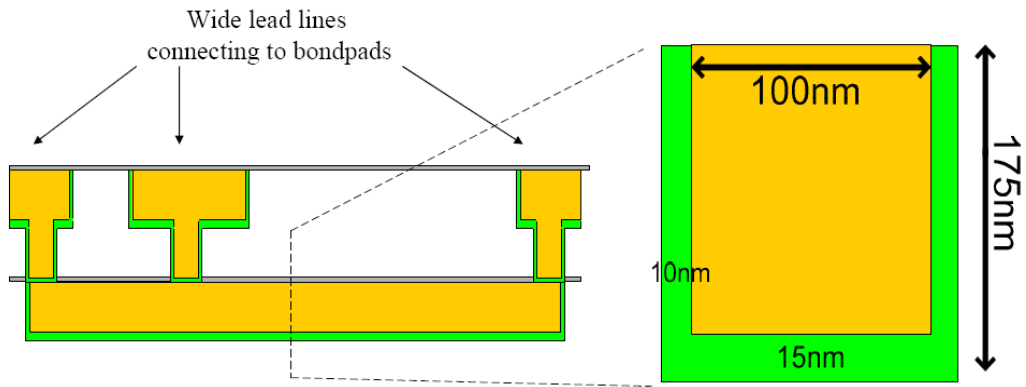
Figure 5.1 (a) Top-view illustrations of the asymmetric-dotted-I and asymmetric-T interconnect tree structures. (b) Side and cross-sectional views of the Cu/low-*k* interconnect tree structures.

5.2.1 Failure Times

Figures 5.2 and 5.3 show the testing configurations and time-to-failure (TTF) results graphed on lognormal plots with linear fits. The absolute scale and unit for the ordinates in Figure 5.2(b) and 3(b) have been replaced by arbitrary units (A.U.). Qualitau MIRA electromigration testing systems that support the use of multiple power supplies per package were used. Each interconnect tree structure was wire-bonded to one ceramic package. Two or three independently-controlled power sources and resistance monitors (one power source or monitor per segment in the interconnect tree) were assigned to one asymmetric-dotted-I or asymmetric-T tree structure, respectively. All tests were performed at 325°C. The failure criterion for the results shown in Figures 5.2 and 5.3 was a 10% increase of the initial resistances (10% ΔR_0), a commonly used convention.

In the first set of experiments (Figure 5.2), both an isolated via-terminated 25μm segment and two-segment trees (asymmetric-dotted-I) with a 25μm-long segment connected to a 175μm-long segment were tested. In all cases, the 25μm-long limb was stressed at a current density of 1.25MA/cm^2, while the current density in the 175μm-long segment was varied as indicated. The lifetimes shown in Figure 5.2(b) are those of the 25μm-long segment. No failures were recorded for the 175μm-long segment in this set of experiments. As electrons flowed toward the middle via in the 25μm-long segments, and away from the middle via in the 175μm-long segments, the 175μm-long segments functioned as *sinks* for the Cu atoms electromigrating from the short segments. Therefore, the five test conditions consist of:

(i) no sink,

(ii) an inactive sink,

(iii) an active sink at 10% current (compared to the 25µm-long test segment),

(iv) an active sink at 50% current, and

(v) an active sink at 100% current.

In a second set of experiments (Figure 5.3), both two-segment (asymmetric-dotted-I) and three-segment structures (asymmetric-T) were tested. Again, the current density in a 25µm-long segment was fixed at 1.25MA/cm^2 and the current densities in the other segments were varied. However, in this case, the lifetimes shown in the figure are those of the 175µm-long segments, because no failures were recorded for the 25µm-long segment. Here, the directions of the electron fluxes were from the central via to the terminating via in the 25µm-long segments, and from the terminating vias toward the central via in the longer segments. The other segments therefore served as atom *reservoirs* for the 25µm-long test segment, providing a source of atoms that might replace atoms electromigrating away from the middle via in the 25µm-long segment. The test configurations were therefore:

(1) an inactive reservoir,

(2) two 10% active reservoirs,

(3) two 50% active reservoirs,

(4) one 50% active reservoir, and

(5) one 100% active reservoir.

In addition, the last configuration was also carried out with an electron flux of 4.0MA/cm^2 – configuration (6), one 100% active reservoir. As mentioned above, a 10% ΔR_0 failure criterion was applied to all the tests. No failures were observed after about 1000hours of testing for configurations (1) and (2).
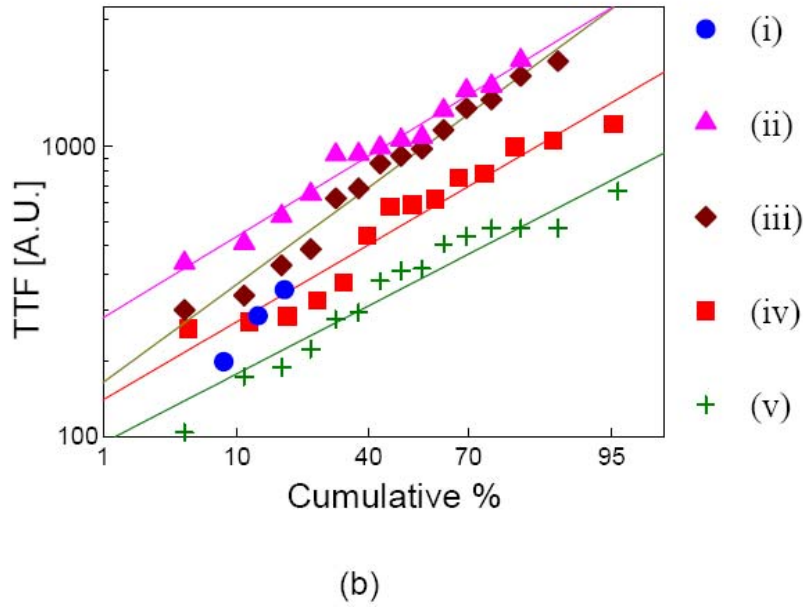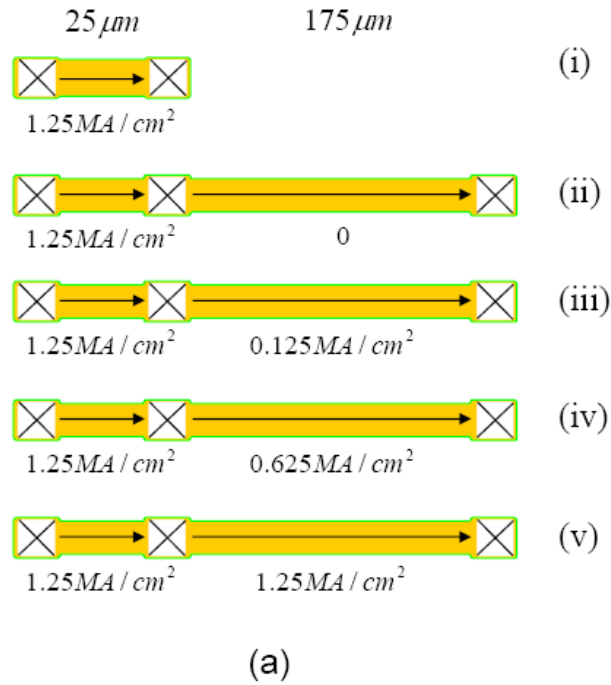
Figure 5.2 Experiments involving active atomic sink effects. (a) Schematic diagrams showing the direction of electron flow and the current densities for test configurations (i) to (v). (b) Times to failure determined using a $10\%\Delta R_0$ failure criterion and plotted on a lognormal graph with linear fits to the data. The ordinate is normalized to arbitrary time units (A.U.). All tests were carried out at 325°C.
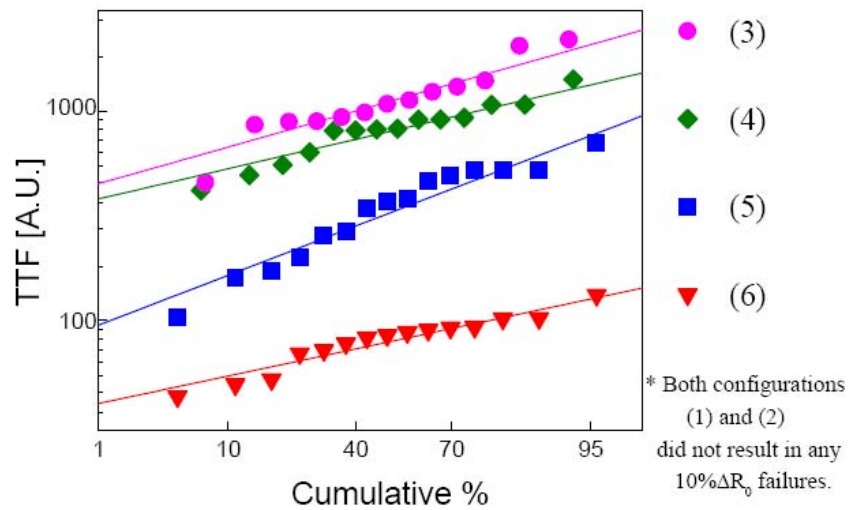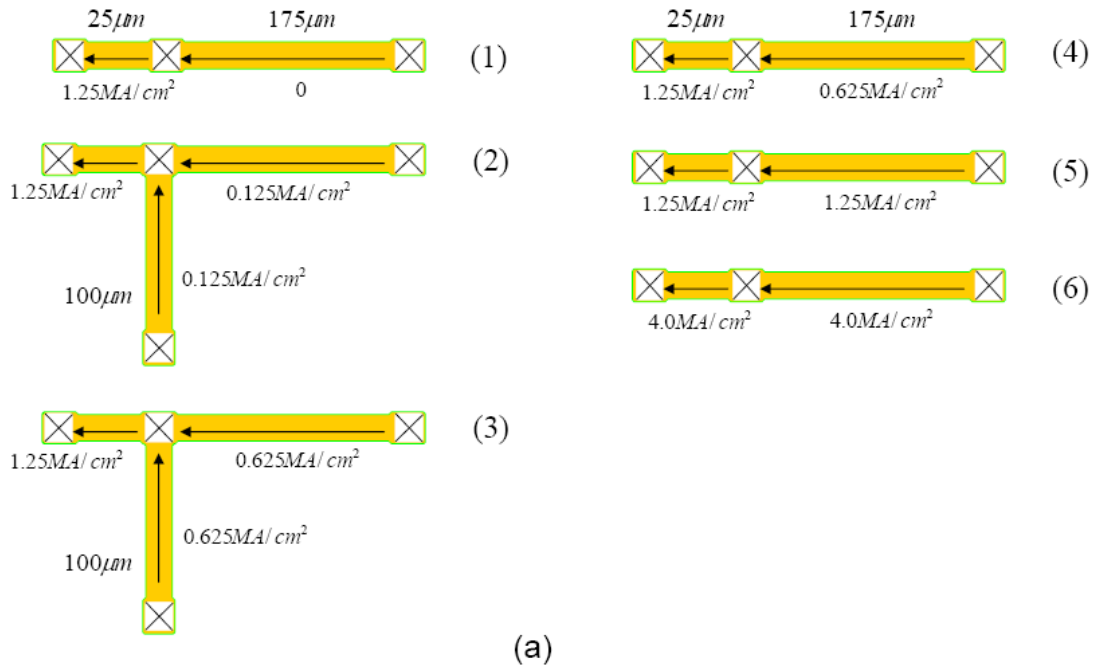
Figure 5.3 Experiments involving active atomic reservoirs. (a) Schematic diagrams showing the directions of electron flow and the current densities for test configurations (1) to (6). (b) Times to failure determined using a $10\%\,\Delta R_0$ failure criterion, plotted on lognormal graph with linear fits to the data. The ordinate is normalized to arbitrary time units (A.U.). All tests were carried out at 325°C.

5.2.2 Resistance vs. Time

Figure 5.4(a) shows resistance vs. time (R vs. t) traces for the 14 samples tested in configuration (iv). These traces are characteristic of all experimental configurations for which failure was observed. Figure 5.4(b) shows a single schematic R vs. t curve. The initial resistance of the interconnect segment remained almost constant R_0 until time t_0, at which a virtually instantaneous increase in resistance of 50 to $100\,\Omega$ occurred. This sudden resistance increase was almost always large enough to satisfy the 10% ΔR_0 failure criterion. The resistance 'jump' is followed by a period of steady increase in resistance characterized by a constant slope, $\dfrac{dR}{dt}$. All electromigration experiments were continued long after the 10% ΔR_0 failure criterion had been reached: a few hundred to more than a thousand hours after t_0. Despite of the extremely large final resistance values of some of the test samples (up to about $10\mathrm{k}\Omega$ in some instances); there were not *any* abrupt open-circuit failures in all of the experiments. Also, in many cases, $\dfrac{dR}{dt}$ decreased over a long time after t_0.

As discussed in Chapter 4, behavior like that described above is usually associated with void growth in Cu-based interconnects and has been observed in other investigations [Gan 03, Lee 06, Li 04]. However, it is very unusual for void growth to not lead to open-failure in such long segments. Also, while a decreasing $\dfrac{dR}{dt}$ is sometimes observed in experiments on short lines that are approaching a force balance, this is not expected for lines of the length studied here.
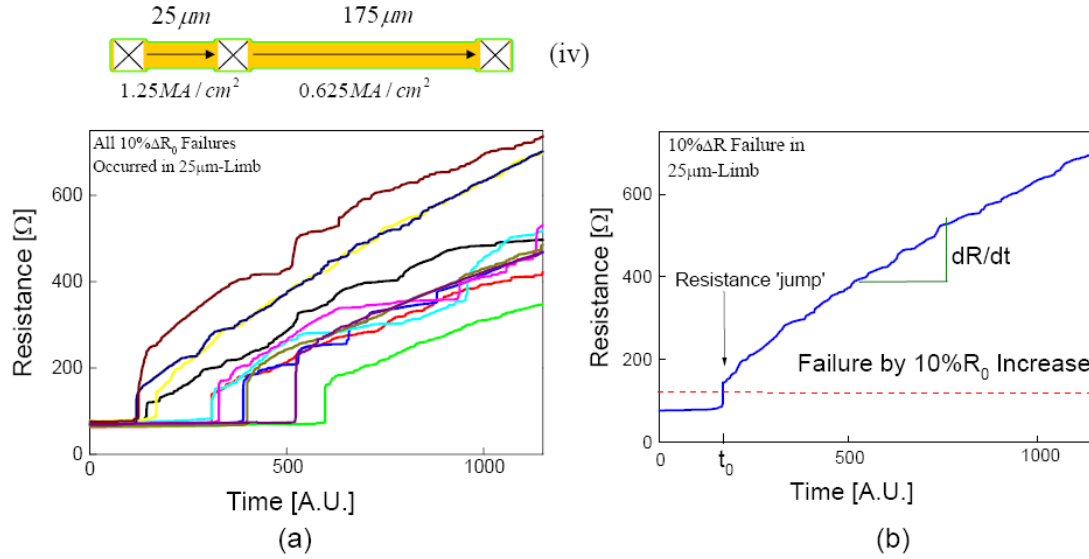
Figure 5.4 In all experiments, the *R* vs. *t* plots for segments that produced failures had similar features. All 14 results for tests in configuration (iv) are shown as example in (a). (b) shows *R* vs. *t* plot for a single sample, along with labels of the key features.

5.2.3 Failure Analysis of the Cathode End

We performed failure analyses on nearly half of the populations of the asymmetric-dotted-I structures tested under various configurations. In all the cases that showed a large resistance increase, very large voids were observed near the cathode, as shown in Figure 5.5. However, we did not observe slit-like voids forming directly below the cathode via. The final resistances increase in the samples correlate well with the observed void lengths (see Figure 5.5, the normalized-*R* vs. *t* plots, as examples). The resistance per void length ratio for the cross-sectional geometry is consistent among all samples subjected to failure analysis, and also agrees with the reported electrical resistivity value for Ta-based thin films $\rho_{liner} = 350 \mu\Omega - cm$ at 25°C with $TCR = 0.00382°C^{-1}$ [Kim 04].

$\Delta R = 2650 \ \Omega$

$void \ length \ \cong 4.0 \ \mu m$

$25 \ \mu m$ $175 \ \mu m$

$1.25 \ MA \ / \ cm^2$ $1.25 \ MA \ / \ cm^2$ cathode via

(a)

$\Delta R = 3300 \ \Omega$

$void \ length \ \cong 4.8 \ \mu m$

$25 \ \mu m$ $175 \ \mu m$

$1.25 \ MA \ / \ cm^2$ $1.25 \ MA \ / \ cm^2$

cathode via

(b)

$\Delta R = 5900\ \Omega$

$void\ \ length\ \ \cong 9.5\,\mu m$

$25\,\mu m$ $175\,\mu m$

$4.0\,MA\,/\,cm^{2}$ $4.0\,MA\,/\,cm^{2}$

cathode via

R-R$_0$ [Ω]

6000

4000

2000

0

t-t$_0$ [A.U.]

e-

E-Beam	Spot	Mag	Tilt	Det	FWD	10/01/06		2 µm
5.00 kV	3	25.0 kX	52.0°	SED	4.740	15:27:54		

(c)

$\Delta R = 7500\ \Omega$

$void\ \ length\ \ \cong 11\,\mu m$

$25\,\mu m$ $175\,\mu m$

$4.0\,MA\,/\,cm^{2}$ $4.0\,MA\,/\,cm^{2}$

cathode via

R-R$_0$ [Ω]

6000

4000

2000

0

t-t$_0$ [A.U.]

e-

HV	curr	det	mag	tilt	WD	4 µm
5.00 kV	0.27 nA	ETD	10000 x	53 °	5.0 mm	label

(d)

Figure 5.5 Scanning electron micrographs near the cathode end of tested interconnect segments sectioned using a focused ion beam (FIB). All parts show images of large voids, along with measured void lengths, the overall resistance increase, and the corresponding normalized resistance traces. In all cases, as in the cases for all other samples subjected to failure analysis, no damage to the Ta-based liner was observed. (a) and (b) show Cu in the void region in the form of de-wetted particles or 'chains' of particles, respectively. (c) and (d) show two voids that are >10µm in length and that fully spanning the cross-section of the line.

The unusually high resistances and correlated large void sizes attained here suggest that the electron flux has shunted over long lengths of liner without causing failure. We did not observe any damage to the Ta-based liner, such as evidence of melting, deformation, or fracture, during failure analysis, even when extremely large voids had formed. However, on occasion, we observed evidence of high temperatures being achieved inside the interconnects, presumably due to resistive heating of the liner around long voids. Figure 5.5(a) shows such a case, in which some of the Cu in the voided region formed a nano-particle 'chain.' This morphology suggests that the Cu wire was beading through a Rayleigh-like instability [Jir 92, Mcc85], which requires high atomic mobilities, i.e., high temperatures.

5.3 Discussion

The lifetime results described above demonstrate that the reliability of a test segment depends on whether it is connected to another segment that can act as an atomic sink or reservoir. Specifically, connection to an atomic sink degrades reliability, by an amount that depends on the electron flux in the sink, while connection to a reservoir improves reliability, analogously, by an amount that also depends on the current in the reservoir.

In general, the shunting behavior of Ta-based liners is independent of the ILD. The unusual robustness of the liners of the Cu/low-k interconnects studied here allows continued electromigration well after the 10% ΔR_0 increase used to define failure. More comprehensive presentation of the failure analysis, shown in Chapter 6, indicates that electromigration-induced voiding was confined within the test structures. The Ta-based

barriers of the test structure around the voids as well as the liner of both cathode and anode vias were still continuous and intact. Also, no damages were seen to the lead lines that connect the test structures to the bond pads during failure analysis. Therefore, the R vs. t traces can provide data which can be analyzed to extract values for the drift velocity, the effective diffusivity, and the effective charge. The determination of these values, in turn, allows quantitative analysis of the effects of the sink and reservoir, and analysis of the effects of the modulus of the ILD on both.

5.3.1 Kinetic Parameters and Numerical Calculations on TTF

Before a void spans the width and thickness of an interconnect, its effect on the resistance is small, as discussed in Chapter 4. The sudden resistance increase seen in Figures 5.4(a) and 5.4(b) corresponds the time t_0 when a void first spans the cross-section of the line. Given the resistivities and dimensions of the Cu and the refractory liner, the total volume of the void at t_0 can be estimated from the magnitude of the resistance increase. Assuming that the void fully spans the width and thickness of the interconnect everywhere along the void's length, we estimate void volumes at t_0 to be 1.12×10^{-3} to 1.6×10^{-3} μm^3, corresponding to fully-spanning void lengths 0.07 to 0.1μm, respectively.

After a void spans the line, it continues to grow due to continued electromigration of Cu out of the void. This subsequent void growth rate can correlates with the rate of change of the resistance, $\dfrac{dR}{dt}$. Using the relationships for fully spanning void growth shown in Chapter 4, the drift velocity for each experiment shown in Table5.1. Configurations (v), (5), and (6) are equivalent to testing a via-terminated segment of length 200μm under the respective current densities, for which no effects of a back stress

are expected at t_0. The reduced drift velocities determined for configurations (ii) to (iv), (3), and (4) are the result of contributions from the back stress force, with the drift velocity decreasing with decreasing electron flux in the atomic sinks and with increasing electron flux in the atomic reservoirs, as qualitatively expected.

Table 5.1 Tabulated results for the drift velocity, v_d, obtained from R vs. t data for configurations (ii) to (v) and (3) to (6). $\dfrac{\partial \sigma}{\partial x}$ values were calculated from stress profiles generated using XSim.

Experiment Number	j [MA/cm^2] in the limb of void growth	v_d [x 10^{-9} m/hr] experimental results	v_d/j	$\partial \sigma / \partial x$ [x 100 MPa/µm] XSim calculation using $z^*=0.40\pm0.12$
(ii)	1.25	0.30±0.10	0.24	-0.017
(iii)	1.25	0.51±0.14	0.41	-0.014
(iv)	1.25	0.79±0.18	0.63	-0.0078
(v)	1.25	2.0±0.8	1.6	0
(3)	0.625	0.95±0.25	1.4	0.00028
(4)	0.625	1.1±0.4	1.7	0.00027
(5)	1.25	2.0±0.8	1.6	0
(6)	4.0	6.6±1.3	1.5	0

Table 5.2 Experimental and calculated median times to failure for configurations (i) to (v) and (1) to (6). t_N is the calculated time required for void nucleation in each configuration, and t_G is the subsequent time required for void growth to reach the critical size required for a $10\%\Delta R_0$ failure.

Experiment Number	j [MA/cm^2] in the limb of void growth	t_{50} [A.U.] experimental results	$t_{0,calc}$ [A.U.] XSim calculation	t_N [A.U.] XSim calculation	$t_G=t_0-t_N$ [A.U.]
(i)	1.25	>39100	immortal	44	void growth saturates prior to critical volume
(ii)	1.25	1130	983	45	1038
(iii)	1.25	863	767	47	720
(iv)	1.25	532	486	44	442
(v)	1.25	322	353	45	308
(1)	0	No failures recorded	immortal	$\sigma_{nucl.}$ is not reached even at steady state	N/A
(2)	0.125	No failures recorded	8892	4167	4725
(3)	0.625	1100	1033	162	873
(4)	0.625	793	854	157	686
(5)	1.25	322	353	45	308
(6)	4.0	79	122	4.7	117

The results from configurations (v), (5) and (6), for which the back stress force is negligible, are used to estimate the $(Dz^*)_{eff}$. Recall the Nernst-Einstein relationship [Ble 67b],

$$v_d = \frac{D}{kT}(F_{electron} + F_{back}) = \frac{D_{eff}}{kT}(qz^* \rho_{Cu} j + \Omega \frac{\partial \sigma}{\partial x}). \quad (5.2)$$

Using the data from Table 5.1, when $F_{back} \sim 0$, $(Dz^*)_{eff} = 7.4 \times 10^{-17} m^2 / \sec$. Also recall the expression for the effective diffusivity [Cle 95],

$$D_{eff} = D_0 \cdot \exp(-\frac{\Delta H}{kT}) \cdot \exp[(\frac{\Omega}{kT} + \frac{1}{B})\sigma]. \quad (5.3)$$

ΔH was experimentally determined to be between 0.80 and 0.84eV [Pri 06]. σ is zero right next to the void, and should not exceed the critical stress for void nucleation near the void ($\sigma_{crit.,nuc} = 25$MPa [Hau 04]), so that we can determine that $(Dz^*)_{0,eff}$ to be $\sim 3.9 \times 10^{-10} m^2 \sec$.

Voids that fully span the cross-section of the line must have grown from smaller volumes, so the failure time includes both the time required for void nucleation, t_N, and the time required for the void to grow to span the line, t_G, such that $t_0 = t_N + t_G$. Using the experimental values of $(Dz^*)_{0,eff}$, ΔH and $\sigma_{crit.,nuc}$, Equation (5.1) can be solved using XSim [Cho 04] to predict values for t_0, t_N, and t_G. (In cases where the back stress force strongly influences the void growth process, $D_{0,eff}$ and z^* must be separately determined

in order to calculate t_0. This is described in the following section.) Here, t_G is the time required for growth of a void from negligibly small dimensions, to the volumes implied by the observed ΔR at t_0. These calculated values are shown with measured values of t_{50} in Table5.2, both in the same A.U. It should first be noted that the values of the calculated t_0 ($t_{0,calc}$) and t_{50} are in good agreement, both in magnitude and trend. It should also be noted that, with the exception of Experiment (2), t_N is only 10 to 20% of t_G. In Experiment (2), the electron flux in the limb where voiding occurs, 0.125MA/cm^2, is so mild that t_N becomes a significant fraction of t_0, and both t_0 and t_N are extremely long. However, the void nucleation process in Experiment (2) is not influenced by the back stress force. As seen in Table5.2, the t_N values for all experimental configurations, i.e., the time required to reach $\sigma_{crit.,nuc} = 25$MPa, scale well with j^{-2}, where j is the current density in the limbs where a void was able to nucleate. This indicates that in these experiments, void nucleation was not impeded by the back stress force despite having different stress conditions in the atomic sinks or reservoirs. Furthermore, if $t_N << t_G$, t_0 (and t_{50}) should scale with j^{-1} [Bla 67]. Table5.2 shows that generally $t_N \sim 10$ to 20% of t_0. Therefore, the scaling factor should be close to, but slightly greater than 1. This is consistent with the lifetime results obtained for Experiments (5) and (6).

5.3.2 Back Stress Force and z * Calculations

As mentioned above, in Experiments (v), (5) and (6), the back stress force impeding void growth up to the volume required for the 10% ΔR_0 failure is negligible. In these cases, it can be seen from Equation (5.2) that in the absence of any back stress force, v_d/j becomes a constant proportional to $(Dz*)_{eff}$. In the other experiments, during

the void growth process the back stress force in the void region became appreciable in magnitude and competed with the electron wind force. This is evident in the decrease in the v_d/j values shown in Table5.1. In these cases, D_{eff} and z^*_{eff} must be separately determined. In order to de-couple these two kinetic parameters, simultaneous calculations using Equation (5.1), to calculate the transient stress profiles to determine

$F_{back} = \Omega \dfrac{\partial \sigma}{\partial x}$, and Equation (5.2), to calculate the impeded v_d, were carried out. In this

process, z^* becomes a parameter that can be adjusted in order to match the calculated v_d values to those determined experimentally (summarized in Table5.1) for each of the testing configurations. Additionally, the calculated t_0 values are also matched to the t_{50}'s as z^* is adjusted.

z^* of 0.40 ± 0.12 is found to give the best match to cover the range of experimentally determined v_d values while closely matching $t_{0,calc}$ to t_{50}. z^* equaling to 0.40 falls in the previously reported range of values [Hu 99]. As a result, Figure 5.6 and 5.7 show the time-dependent stress profiles for the atomic sink and reservoir experiments, respectively, at $t_{0,calc}$'s. As Table5.1 shows, $\dfrac{\partial \sigma}{\partial x}$ is negative if a compressive stress is present, and is positive if a tensile stress is present in the void growth region. Notably, test configurations (ii), (iii), and (iv) generate the highest values of F_{back}. In most other

cases, $\dfrac{\partial \sigma}{\partial x}$ is close to zero.
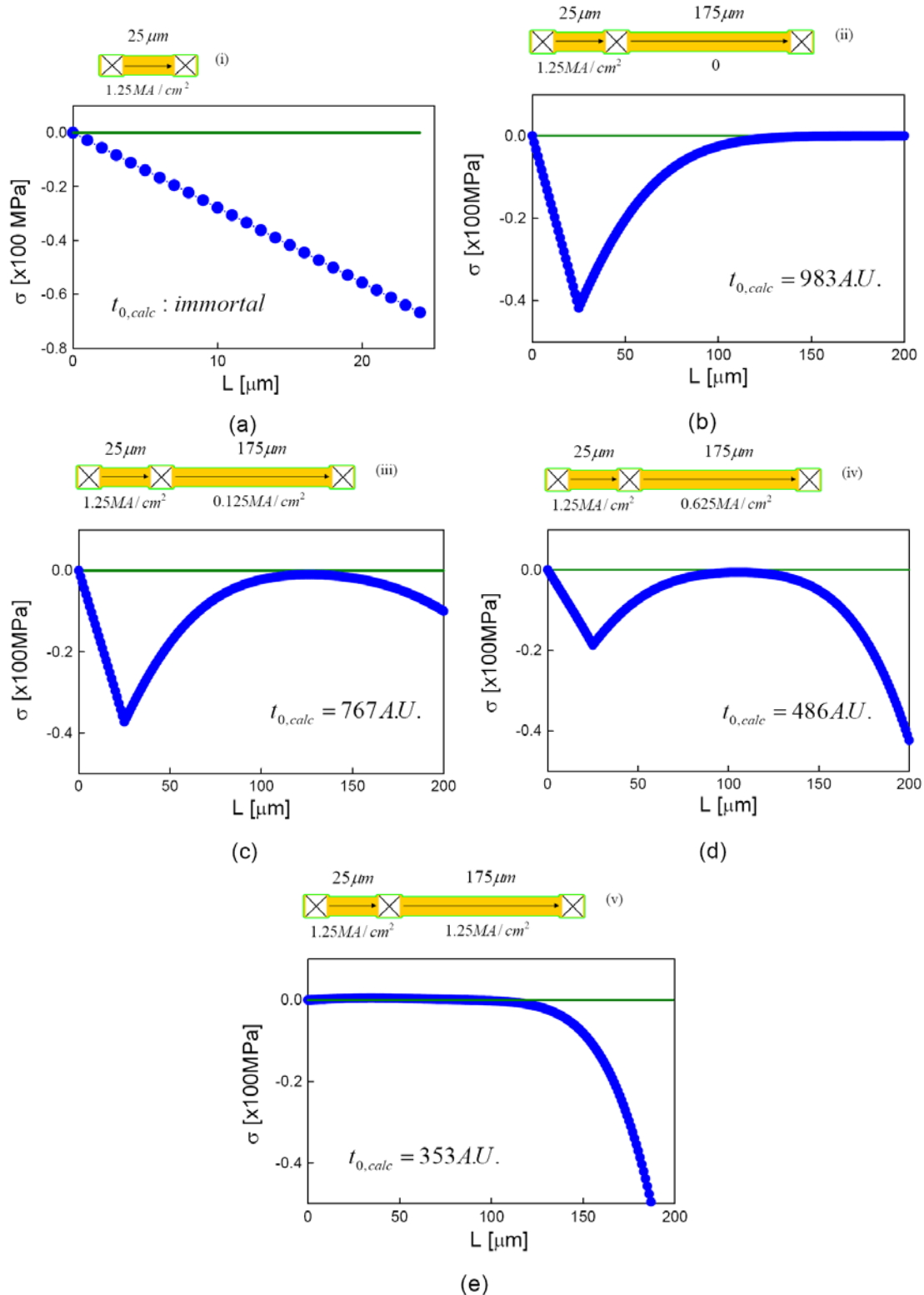
Figure 5.6 Calculated stress profiles at the calculated failure times for tests in configurations (i) to (v), shown in (a) to (e), respectively.
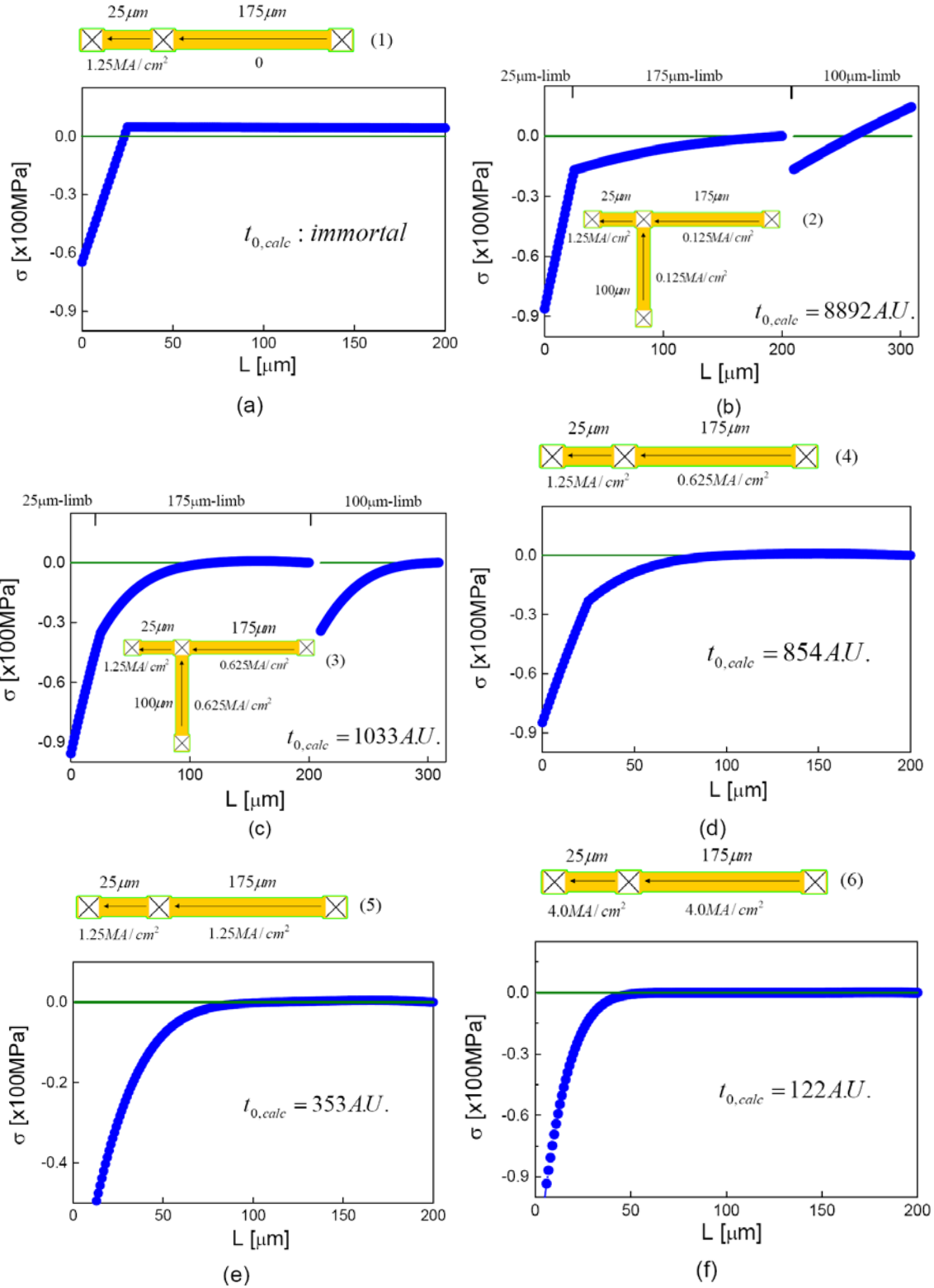
Figure 5.7 Calculated stress profiles at the calculated failure times for tests in configurations (1) to (6), shown in (a) to (f), respectively.

5.3.3 Failures in the Atomic Sink Experiments

We can explain the trend seen in the lifetime data for the atomic sink experiments in the following way. In case (i), no atomic sink is present at the anode. All the electromigrated Cu atoms are confined near the anode end of the 25μm-long segment. This results in a sharp increase in the compressive stress, i.e., a high back stress force. In the course of void growth up to the size required for failure, the back stress force became large enough that the void growth immortality condition was satisfied. This is consistent with the fact that only 25% of the samples failed during testing in this configuration. In case (ii), there is a passive segment at the anode end of the 25μm-long limb, so the accumulated Cu atoms can be passively 'pushed' into the atomic sink. The added volume for accommodation of drifting Cu means a reduction in the maximum compressive stress at the middle via, and therefore, a smaller back stress force compared to configuration (i). For configurations (iii) and (iv), the atomic sinks are active: in addition to Cu atoms being passively pushed to the middle via, the atomic-sink segments can also actively redistribute atoms toward the right-most via, resulting in a compressive stresses at the right-most via. A stronger active sink means more Cu atoms are transported (see Figure 5.6(c) and (d)). Thus, even less accumulation of Cu occurs at the middle via. This translates to a lower back stress force to impede the void growth near the left-most via. In experiment (v), a 100% atomic sink exists. Here, just about all electromigrated Cu atoms accumulate near the right-most via. The lack of a change in C_a near the middle via means that no back stress force develops inside the 25μm-long limb to restrain void growth at the left-most via. Therefore, ranging from configuration (i) to (v), the void growth process at the left-most via is impeded less and less by the

compressive stress build-up at the middle via, resulting in a decreasing trend in the t_{50} values.

5.3.4 Failures in the Atomic Reservoir Experiments

The back stress force plays an equally important role in analyzing the atomic reservoir experiments as well. First, recall that in all cases, when failure occurred, it occurred through voiding in the reservoir, and not in the 25μm-long segment. Our calculations for configuration (1) show that a force balance is achieved before $\sigma_{crit.,nuc}$ can be reached. This result suggests that the stress gradient that develops in the reservoir due to depletion of Cu at the central via is sufficient to drive diffusion of Cu from the inactive segment to lower the stress at the central via, further suppressing void nucleation at the central via [Cha 04, Vai 05]. The experimental results also support this conclusion. Simulations for configurations (2), (3), and (4) show an initial depletion of Cu atoms at the middle via, which leads to the development of a tensile stress. (This process happens for a much shorter period of time in configuration (3) than in (2) and (4).) The 1.25MA/cm^2 current density in the 25μm-long segment initially 'drains' Cu faster than it can be replaced by electromigration from the reservoir. However, as a stress gradient develops in the reservoir near the central via, it contributes a purely diffusive flux in addition to the electromigration flux, and the tensile stress at the central via is suppressed before void nucleation occurs. When this happens, the Cu that electromigrates in the 25μm-long segment ultimately contributes to void nucleation and growth at the end of the reservoir segment. Calculations showed that the time needed for void growth to reach the critical volume require for failure in configuration (2) is much longer than the

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electromigration testing duration. Therefore, no failures seen for Experiment (2) is consistent with this analysis as well.

In configurations (3) and (4), the current densities in the atomic reservoir segments are equal, $0.625MA/cm^2$. However, two reservoirs are present in asymmetric-T structures (configuration (3)), while only one reservoir is present in asymmetric-dotted-I structures (configuration (4)). As reasoned above, having two atomic sources would cause a faster diffusive flux to suppress development of tensile stress at the middle via. Therefore, as both the experimental data as well as XSim calculations demonstrate, the asymmetric-T structures are more reliable than the asymmetric-dotted-I structures.

5.4 Effects of Mechanical Properties on t_{50}'s

From the preceding discussions, it should be clear that in general, the back stress force, i.e., the stress gradients, play critical roles in governing the lifetimes of multi-segment interconnect trees. The relationship between the back stress and the amount of Cu that is transported is governed by the effective elastic modulus B, which is a function of the elastic modulus of the ILD. When B is small, a large amount of Cu must be transported to achieve a high back stress. When a high back-stress is beneficial, a low B value is problematic.

Though direct experimental comparisons between Cu/low-k and Cu/SiO$_2$ results cannot be made, in earlier studies of the reliability of two-segment Cu/SiO$_2$ interconnect trees, phenomenology broadly similar to that outlined above was observed [Gan 03]. For these studies, $(Dz^*)_{0,eff}$ and $\sigma_{crit.,nuc}$ were estimated to be $3.0\times10^{-10}\,m^2/\sec$ and 41MPa,

respectively. Similar to this study, using XSim, $t_{0,calc}$ values were also found to be consistent with experimentally determined values of t_{50}.

Furthermore, the results discussed in earlier sections allow us to use XSim to estimate the effects expected for test segments with the same geometries, but implemented in technologies leading to different B values. The value of B does not affect the kinetic parameters determined in this study; e.g., the values of $(z*D)_{eff,0}$ or ΔH. As discussed in Chapter 4, $\sigma_{nuc,crit}$ is expected to roughly scale with $\sqrt{B}$. With these assumptions, we have calculated the times required for $10\%\Delta R_0$ failures for different B values, shown in Figure 5.8. A B of 49GPa corresponds to the ILD being SiO_2, and a B of 7GPa corresponds to an ILD with Young's modulus of 3GPa. For the Cu/low-k experiments discussed above, B is 17GPa. Similar to the other plots, Figure 5.9(a) and (b) is normalized to arbitrary time units.
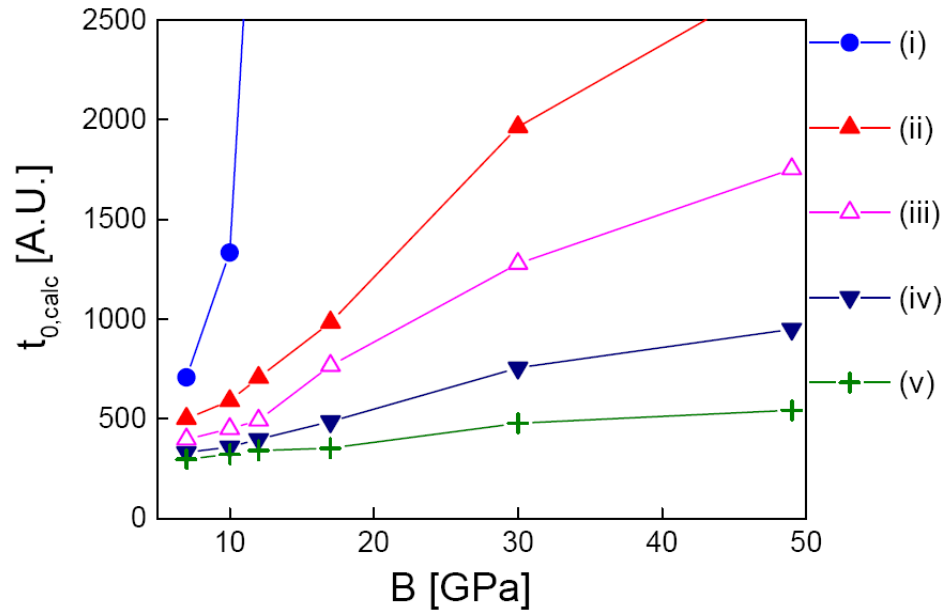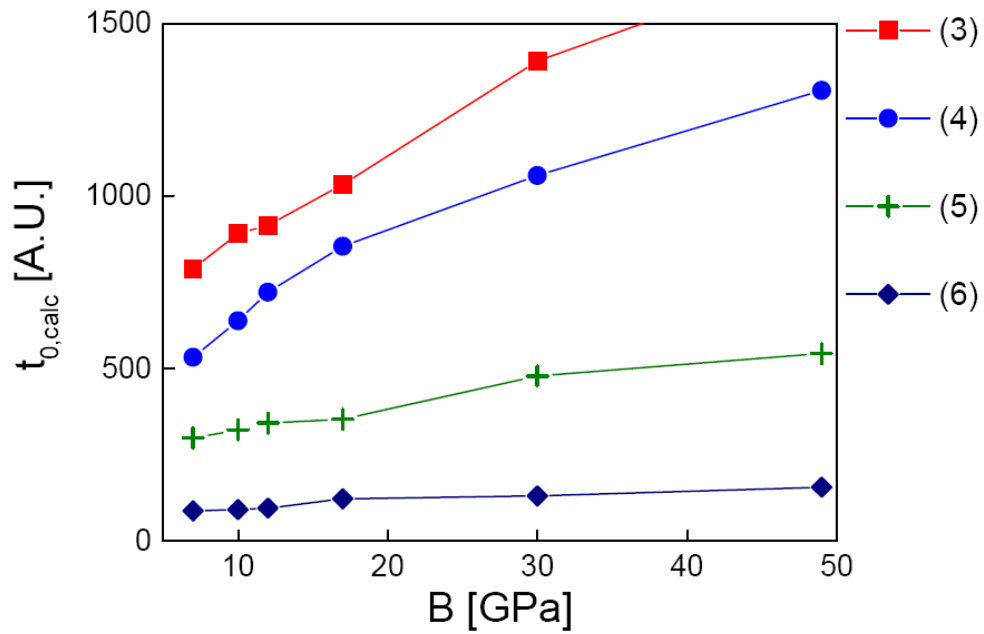
Figure 5.8 Predicted failure times as a function of the effective bulk elastic modulus, *B*, for (a) the atomic sink experimental configurations, (i) to (v), and (b) the atomic reservoir configurations, (3) to (6).

Recall from the discussions in previous sections, the presence of an active sink degrades reliability (Experiments (ii) through (v)), and the presence of an active reservoir improves reliability (Experiments (1) through (6)), with the magnitude of the degradation or improvement depending on the level of activity (current density) in the adjacent segment. The results shown in Figure 5.8 indicate that the reliability degradation associated with atomic sinks becomes rapidly more severe with decreasing B. This is because the stress gradient that develops in the sink segment, near the middle via and resists 'draining' of the 25μm-long segment, is reduced when B is reduced. In order to demonstrate this point, Figure 5.9 compares the time-dependent stress profiles for configurations similar to experimental configurations (iii) and (iv) with different values of B. In both sets of illustrations, as B diminishes, both the compressive stress and the stress gradient decrease in the 25μm-long segment. Consequently, as B decreases, t_0 also decreases. The results shown in Figure 5.8 also indicate that the positive effects of reservoirs are reduced as B is reduced. In this case, the stress gradient in the sink segment near the middle via that helps drive diffusion of Cu from the reservoir to replace Cu in the 25μm-lomng segment is reduced as B is reduced. Lower values of the ILD moduli are therefore seen to amplify the negative effects of sinks, and reduce the positive effects of reservoirs.

(iii)

(a)

(iv)
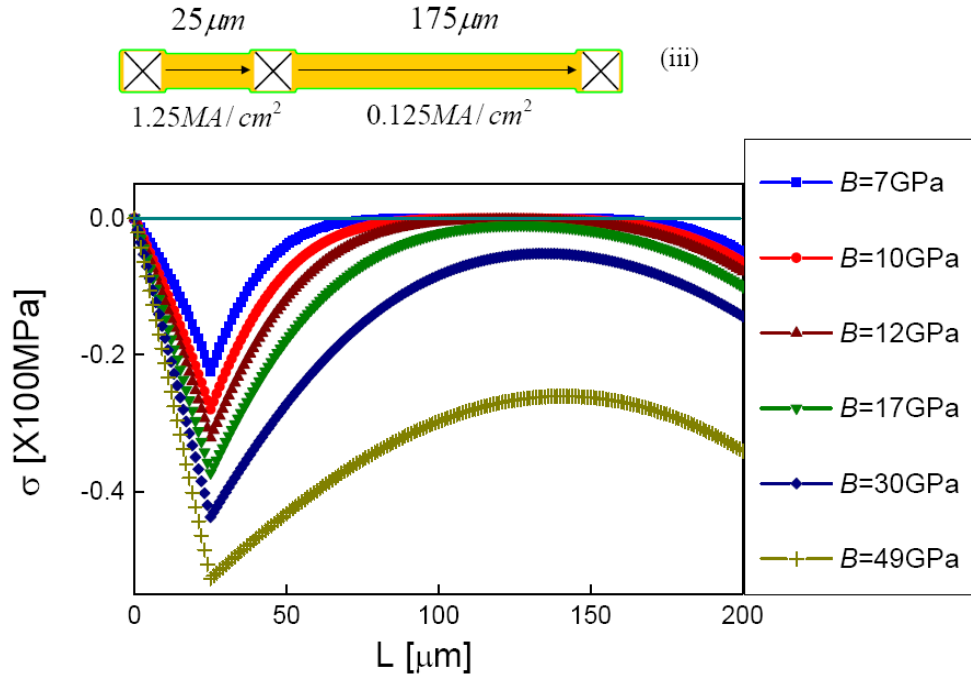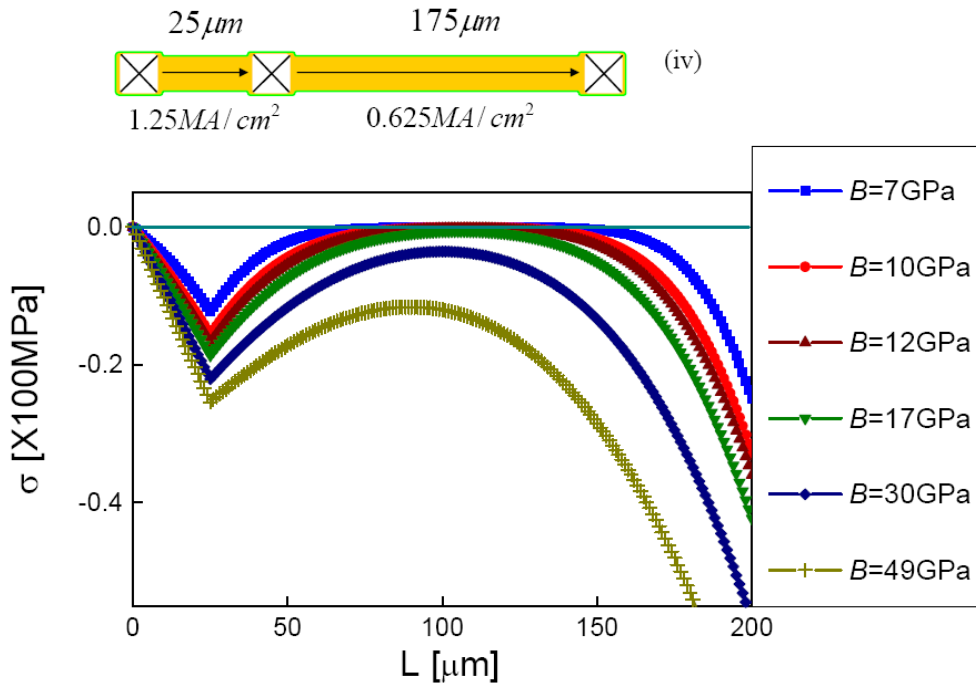
(b)

Figure 5.9 Calculated stress profiles at the calculated failure times for (a) configuration (iii) and (b) configuration (iv) with *B*=7, 10, 12, 17, 30, and 49GPa

5.5 Conclusions

We performed electromigration experiments using asymmetric-dotted-I and asymmetric-T Cu/low-k interconnect structures to investigate the effects of active atomic reservoirs and sinks on reliability, and to investigate the effects of the low stiffness of low-k dielectrics on these sink and reservoir effects. Current conditions were kept constant in a relatively short segment (25μm) while currents were varied in a longer (175μm) connected segment. Analyses of the data show that, first, the time required to reach the $10\%\Delta R_0$ failure criterion was dominated by the time required for void growth (and not void nucleation) and, second, in many cases the void growth rates depended on a balance between the electron wind force and the back stress force associated with stress gradients.

The presence of an atomic sink degraded the reliability of the 25μm-long test segment, with the magnitude of the degradation increasing with increasing current in the sink. This results in a decrease of the stress gradients (F_{back}) that oppose the 'draining' of Cu from the short segments, and therefore assist in void growth. The presence of an atomic reservoir leads to Blech-like immortality of the 25μm-long segment, even when the longer reservoir segment was not activated with current. Failure, if it occurred at all, always occurred in the longer segment, even when the longer segment had a lower current density than the shorter segment. The lifetime of the long segment (reservoir) decreased as the current density in it was increased. The lifetime improvement in the short segment is associated with stress gradients that develop in the reservoir near the central via and that drive diffusion of Cu from the reservoir into the short segment, replacing Cu electromigrating away from the central via in the short segment. Stress

gradients are seen to lead to the beneficial effects of reservoirs and the detrimental effects of sinks.

The Cu/low-k interconnects studied here have unusually robust liners, so that electromigration continued well after the *10%ΔR₀* failure criterion was reached. This allowed determination of the kinetic parameters required, specifically, $(Dz^*)_{0,eff} = 3.9 \times 10^{-10} m^2 / \sec$ and $z^* = 0.40 \pm 0.12$, to predict the effects of the bulk elastic modulus of the ILD (and the corresponding effects of the effective modulus *B*) on the sink and reservoir effects. Use of low-k materials with low stiffness (low elastic modulus) amplifies the negative effects of sinks, and reduces the positive effects of reservoirs. As a consequence, use of low-modulus materials is seen to always degrade the reliability of interconnect trees.

Chapter 6

Electromigration-Induced Extrusion Failures in Cu/low-*k* Interconnects

Electromigration experiments were conducted to investigate the thresholds required for electromigration-induced extrusion failures in Cu/low-*k* interconnect structures. Extrusions at the anode end were observed after long periods of void growth. Characterization of failure sites was carried out using scanning and transmission electron microscopy, and showed that failure occurred through delamination at the interface between the silicon nitride-based capping-layer/diffusion-barrier, and the underlying Cu, Ta liner, and inter-level dielectric (ILD) materials. This interface is subjected to near tensile (mode I) loading with a mode mixity angle between 4 and 7 degrees, estimated using FEM analysis, as electromigration leads to a compressive stress in the underlying Cu. Comparisons of the fracture toughness for interfaces between the capping layer and individual underlayer materials indicate that the extrusion process initially involves plane-strain crack propagation. As Cu continues to extrude, the crack geometry evolves to become elliptical. An analysis of the critical stress required for extrusions based on these observations leads to a value of approximately 710MPa, which agrees well with the value determined through estimation of the volume of material extruded and the required stress to accomplish this extrusion. The critical stress analysis also indicates that sparsely-packed, intermediate to wide interconnect lines are most susceptible to

electromigration-induced extrusion damage, and that extrusion failures are favored by ILDs with low stiffness (low elastic moduli) and thin liners, both of which are needed in future interconnect systems.

6.1 Review of Void Growth in Cu/low-*k* Interconnect Trees

As presented in Chapter 5, package-level electromigration experiments using Cu/low-*k* interconnects fabricated by Advanced Micro Devices, Inc (AMD) were performed at 325°C. This chapter focuses on the results from two particular experiments from this set of experiments, named (A) and (B). Figure 6.1 shows the time-to-failure (TTF) results plotted on a lognormal graph with linear fits. Here, the criterion for failure was a 10% increase of the initial resistances ($10\% \Delta R_0$). The absolute time scale and units for the ordinate in Figure 6.1 has been converted to arbitrary units (A.U.). While these test structures are interconnect trees with three vias, including one located 25μm from the anode, only the vias at the ends of the lines were used in the experiments to be discussed in this study. Experiments (A) and (B) were equivalent to testing of via-terminated segments of length 200μm, at either an electron current density of 1.25 and 4.0MA/cm^2.
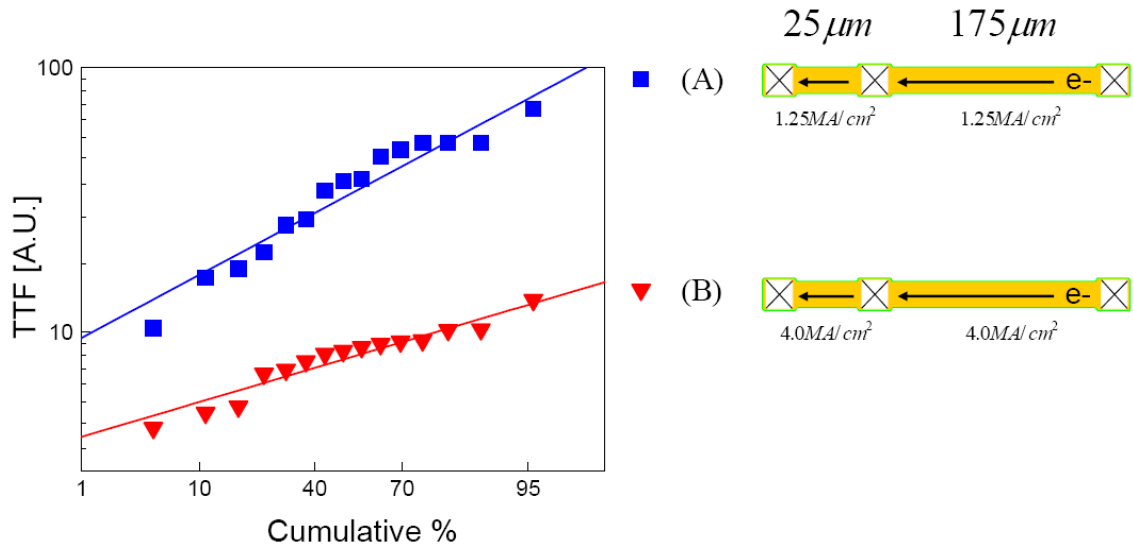
Figure 6.1 Times to failure determined using a $10\%\Delta R_0$ failure criterion for Experiments (A) and (B), plotted on a lognormal graph with linear fits to the data. The ordinate is normalized to arbitrary time units (A.U.). Both tests were carried out at 325°C.
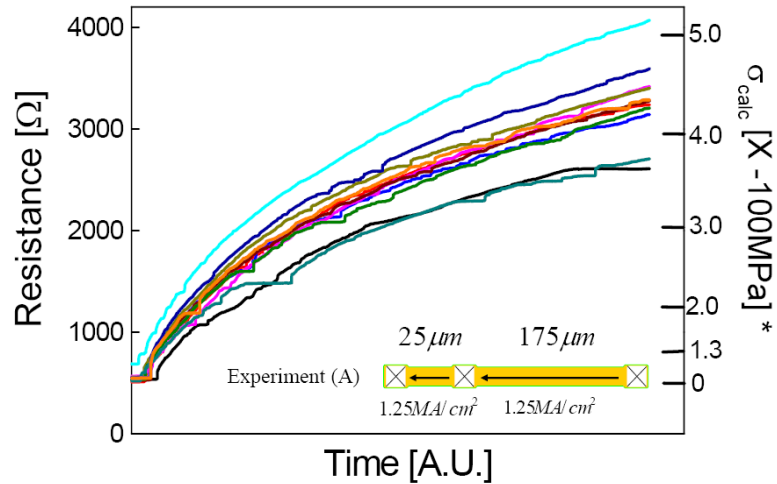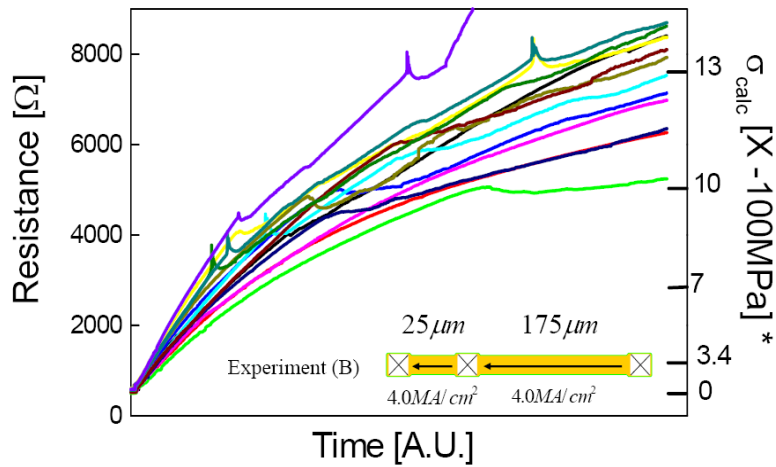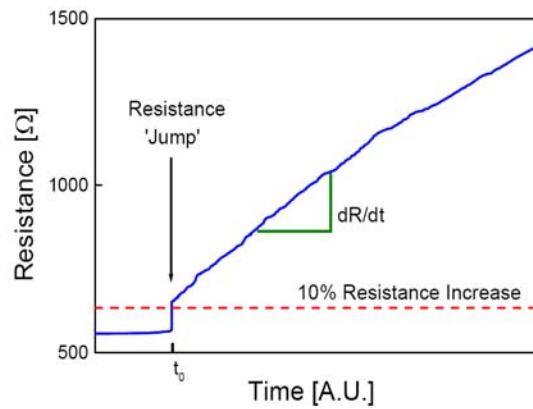
Figure 6.2 In all experiments associated with the interconnect structure used, including those presented in Chapter 5, the *R* vs. *t* plots had similar features. (a) and (b) are the *R* vs. *t* plots for Experiment (A) and (B), respectively. (c) shows a single representative *R* vs. *t* plot, along with labels of its key features.

Figure 6.2(a) and (b) show the resistance vs. time (R vs. t) traces for all the samples in Experiment (A) and (B), respectively. The resistances were measured over the entire lengths of the 200μm-long lines. Figure 6.2(c) shows a single typical R vs. t curve from Experiment (B). As discussed in previous chapters, the R vs. t behavior discussed above is associated with void growth. Also, a decreasing $\dfrac{dR}{dt}$, indication of lines approaching force balance, is not expected for lines of 200μm length.

As shown in Chapter 5, through failure analysis of the cathode, it was found that extremely long voids were able to grow near the cathode, while the flow of electrons was shunted around the void through the Ta-based liner. No damage was observed to the liner, despite evidence of large amount of Joule heating was seen, on occasion. The unusual robustness of the Ta-based liners used in these experiments allowed continued electromigration well beyond the 10% ΔR_0 failure criterion. The steady rates of resistance increase, $\dfrac{dR}{dt}$, observed following the resistance jumps can be used to determine kinetic parameters for the electromigration process, $(Dz^*)_{0,eff} = 3.9 \times 10^{-10} \, m^2 / \sec$ and $z^* = 0.40 \pm 0.12$ [Wei 07].

Using these kinetic parameters in obtaining the numerical solutions of Korhonen equation, using XSim [Cho 04, Cho 07], the amount of Cu transported toward the anode, and the corresponding stress increase at the anode can be calculated, based on the assumption that no extrusion of Cu occurred. The time-dependent changes in C_a near the cathode can be correlated with a void volume, which can be translated to an increase in resistance of the test structure by assuming that the void fully spans the width and thickness of the line (not including the Ta liner). Under these assumptions, a steady state

stress of 0.51 and 1.64GPa at the anode in Experiments (A) and (B), respectively, is predicted. While the decreasing R vs. t curves in Figure 6.2 (a) and (b) suggest that a steady state is being approached, it is unreasonable to expect that the liner and ILD could resist compressive stresses with these magnitudes without failure. Under a high compressive stress, the anode end of Cu interconnects is likely to fail by one of the following four mechanisms:

(i) – liner rupture at the base of either the cathode or anode via;

(ii) – volumetric expansion at the anode of the interconnect segment;

(iii) – stress-induced Cu seepage through the thin refractory liner into the ILD;

(iv) – decohesion and Cu extrusion along the capping layer/ILD interface.

6.2 Failure Analysis of the Anode End

Mechanism (i)

Transmission electron microscopy (TEM) was used to determine if the liner membranes at the bottom of the vias had ruptured. Several samples containing very long voids (about 10µm long) were selected based on either direct observation of the voids during failure analysis of the cathode end or through correlation with a large resistance increase during testing. Figure 6.3 shows the cathode and anode vias in a sample in which a 10µm-long void was expected. Here, the viewing plane of the TEM micrographs is perpendicular to the length-axis of the test line. In addition to showing the vias located above the test structure, Figure 6.3 also shows Cu dummy interconnect lines on either side of the test structure. There are ten, closely spaced, isolated dummy Cu lines total (five on either side of the test line, see Figure (6.4)) that do not have any lead lines connecting to the surface of the wafer. These lines have the same dimensions as those of the test segment, and are included to emulate the packing density encountered in an actual IC at lower metallization levels. Figure 6.3 shows that underneath the cathode via, the side walls of the test structure buckled during the electromigration experiment. This may be due to the vacuum created when the void formed. The TEM micrographs show that, despite this buckling, the Ta-based barriers of the test structure around the void as well as the liner at the base of both vias are still continuous and intact. Since the magnitudes of the stresses are the highest at the terminal vias, and no damage to the liner was seen, these results suggest that mechanism (i) is not responsible for the transport of large amounts of Cu.

$\Delta R = 7000 \ \Omega$

$expect \ void \ length \ \cong 10 \ \mu m$

$25 \ \mu m$ $175 \ \mu m$

$4.0 \, MA \ / \ cm^2$ $4.0 \, MA \ / \ cm^2$

100nm   100nm

Anode via   Cathode via
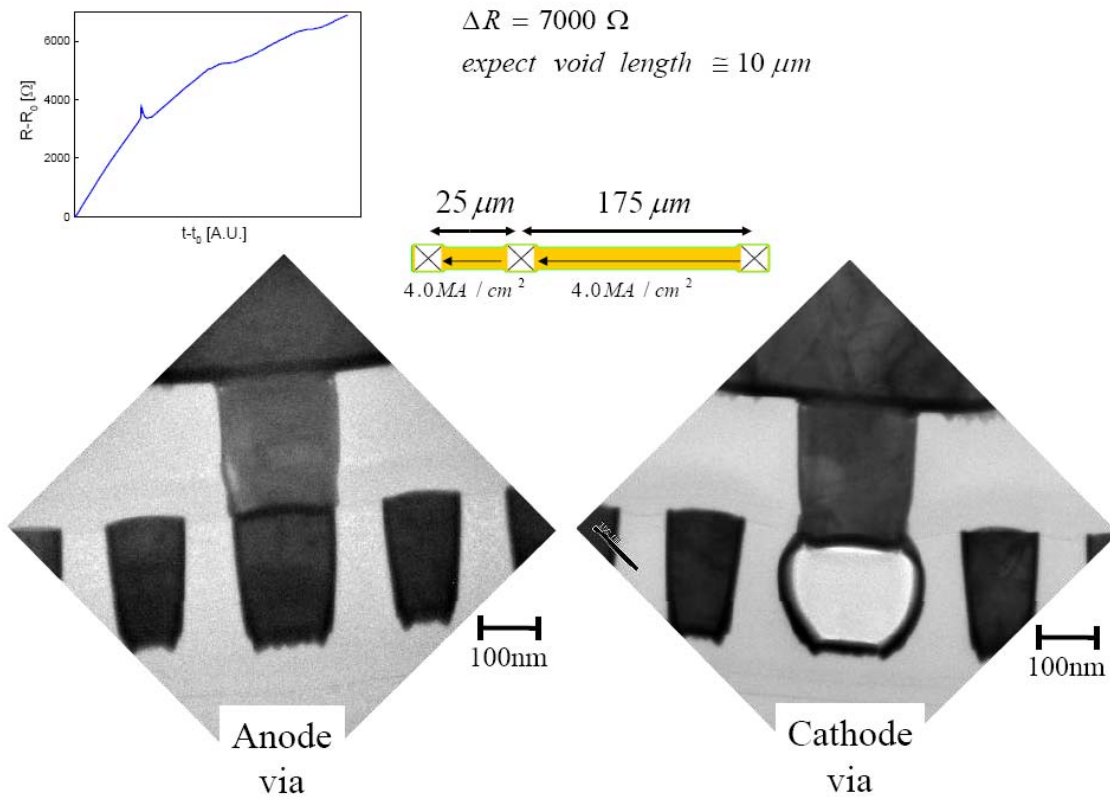
Figure 6.3 Transmission electron micrographs of cross-sections perpendicular to length-axis of the line, at both the cathode and anode vias in a tested structure in which a 10μm-long is expected from the observed resistance increase. The cathode via micrograph shows a fully voided region in the test line below the via, where the side walls have buckled, presumably due the vacuum created when the void formed. Both micrographs show the liner to be continuous and intact at the base of the vias.

Mechanism (ii)

Though unlikely, due to the brittleness of the ILD and the Ta-based liner, the large amount of electromigrated Cu could, in principle, be accommodated by an increase in interconnect volume near the anode end. In order to determine if this behavior occurred, cross-sectional micrographs of the test structure under the same magnification were obtained at various length intervals (1-2μm steps) approaching the anode via. No volumetric expansion was detected: as the cross-section viewing plane approached closer to the anode end, the cross-sectional areas of the test structure remained unchanged with respect to position along the length-axis, as well as with respect to the dummy lines, on either side of the test line, that were not subjected to electromigration. Examples of these observations are shown in Figure 6.4, for a sample in which a void with length >10μm was expected. Therefore, mechanism (ii) also cannot account for the electromigrated Cu.
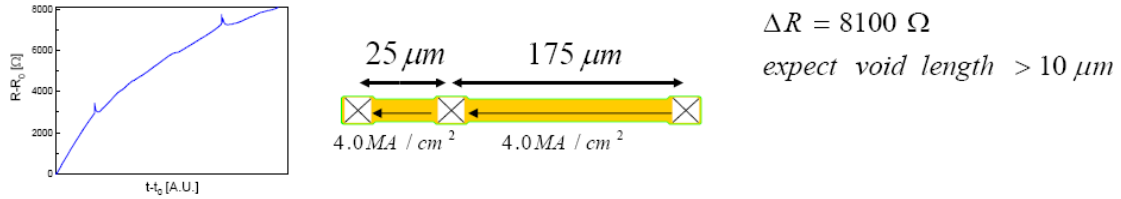
$$\Delta R = 8100 \ \Omega$$
$$expect \ void \ length \ > 10 \ \mu m$$

Cross-section 11μm away from anode via

Test line

| E-Beam | Spot | Mag | FWD | 12/05/06 | Tilt | Det | 500 nm |
| 5.00 kV | 3 | 99.9 kX | 4.796 | 07:54:46 | 52.0° | TLD-B | |

Cross-section 7μm away from anode via

Test line

| E-Beam | Spot | Mag | FWD | 12/05/06 | Tilt | Det | 500 nm |
| 5.00 kV | 3 | 100 kX | 4.795 | 08:34:59 | 52.0° | TLD-B | |

Cross-section 2μm away from anode via

5 dummy lines on either side of test line

Test line

| E-Beam | Mag | FWD | Tilt | 02/08/07 | Det | 500 nm |
| 5.00 kV | 100 kX | 4.794 | 52.0° | 05:51:24 | TLD-B | |
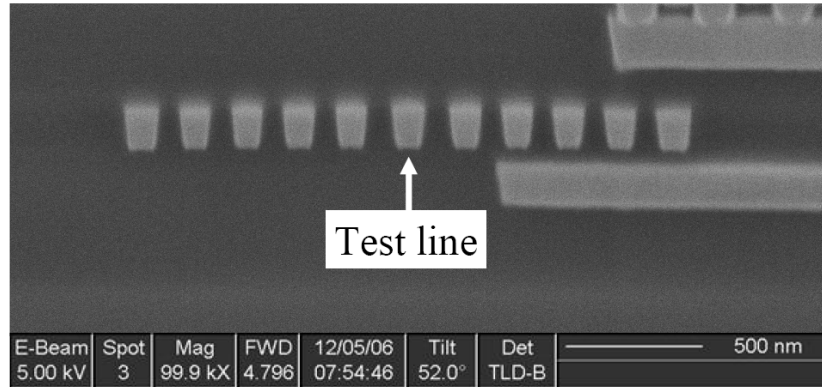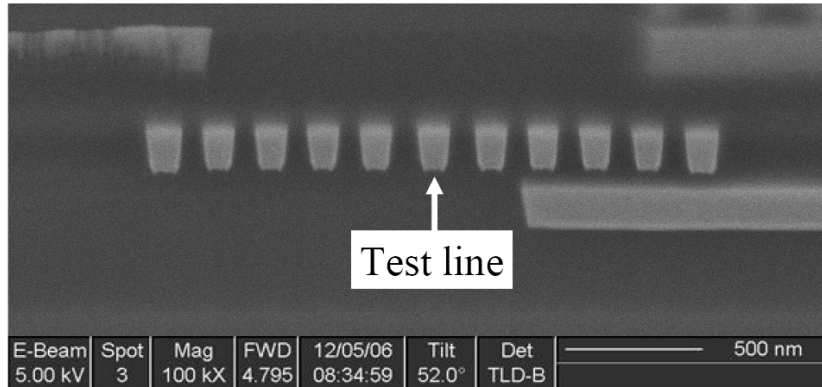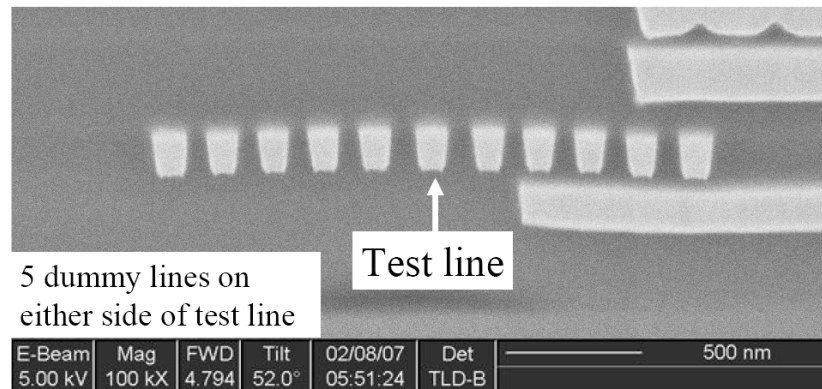
Figure 6.4 Scanning electron micrographs, at the same magnification, viewing FIB-sectioned surfaces normal to the length axis of a test line, at different distances from the anode via. The cross-sectional area of the tested interconnect is similar to those of the dummy Cu lines on either side, and does not change with distance from the anode via.

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<u>Mechanism (iii)</u>

For all the samples subjected to the analysis of mechanism (ii), at each sectioning plane, chemical analyses at various locations in the ILD were performed using energy dispersive X-ray technique (SEM/EDX). The spectra from different locations relative to the test structure, on the same sectioning plane, as well as the locations with the same relative distances to the test structure, on different section planes, were compared. The observed EDX spectra remained the same at all sampling locations. Figure 6.5(a) shows examples of two of the sampling locations in the ILD, '1' and '2,' on two different FIB sectioning planes, 11 and 2μm away from an anode via. Figures 6.5(b) and (c) show corresponding EDX spectra for the respective axial locations and cutting planes. Comparisons show that the size of the Cu spectral peaks generated at various positions remained unchanged in relation to those of Si, which is constant at all locations in the ILD. Additionally, the magnitudes of the Cu spectral peaks are similar to those of Ga peaks, the ion source of the FIB system. Therefore, the spectra are consistent with Cu being a minor impurity on the cross-sectional plane, as a result of either minute amounts of Cu leakage into the ILD, or, more likely, due to redistribution during the FIB sectioning process. Therefore, it does not seem likely that mechanism (iii) can account for the missing Cu.
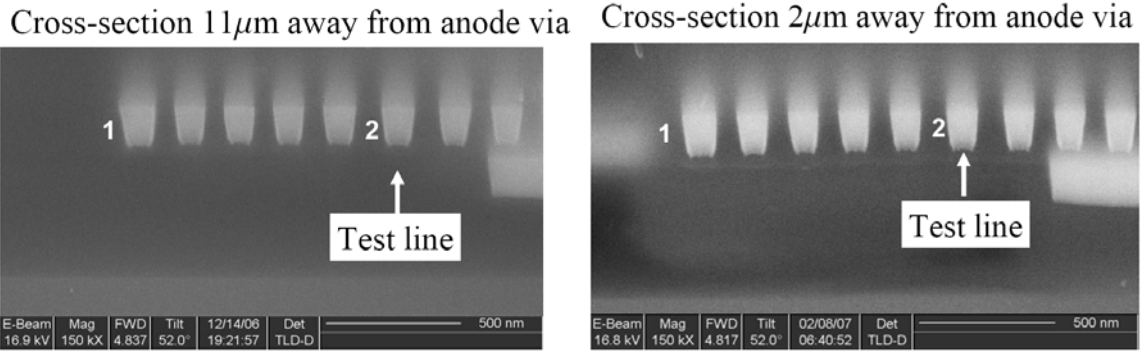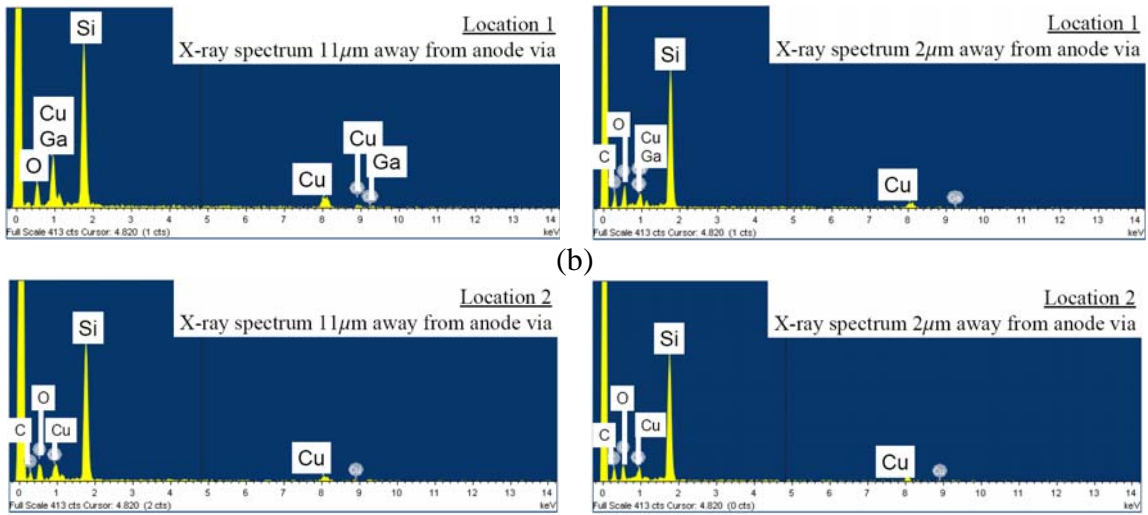
Figure 6.5 (a) Scanning electron micrographs at 11 and 2μm away from the anode via in the same sample shown in Figure 6.4, sectioned using an FIB. The sectioned plane contains two locations, '1' and '2,' where energy dispersive X-ray (EDX) analyses were made. (b) and (c) contrast the EDX spectra generated at locations '1' and '2' on the two different section planes shown in (a).

<u>Mechanism (iv)</u>

Cu extrusions consistent with mechanism (iv) *were* observed in samples from Experiment (B) (see Figure 6.6), but not in samples from Experiment (A) The SiN-based capping layer decohered from the layer below, and Cu extruded from the test segment to occupy the interfacial crack. This resulted in a thin patch of extruded Cu near the anode end, just below the capping layer. Cross-sectional TEM observations (see Figure 6.6(b)) show that the Cu extrusions have a characteristic thickness of 30nm. Also, by examining the cross-sectional SEM micrographs that contain the extruded Cu patch, while tracking the respective axial positions of the cross-section planes along the length of the test segment, the shape and area of the extruded patch could be estimated (see Figure 6.6(c)). The shape of the extrusion shown in Figure 6.6 is approximated as an ellipse with a major axis of 2.5 to 3.0µm and a minor axis of 1.0µm. Therefore, the volume of extruded Cu in this sample is estimated to be 0.058 to $0.071 \mu m^3$.

(a)

Test line

25 μm 175 μm

4.0 MA/cm^2 4.0 MA/cm^2

anode end

100nm
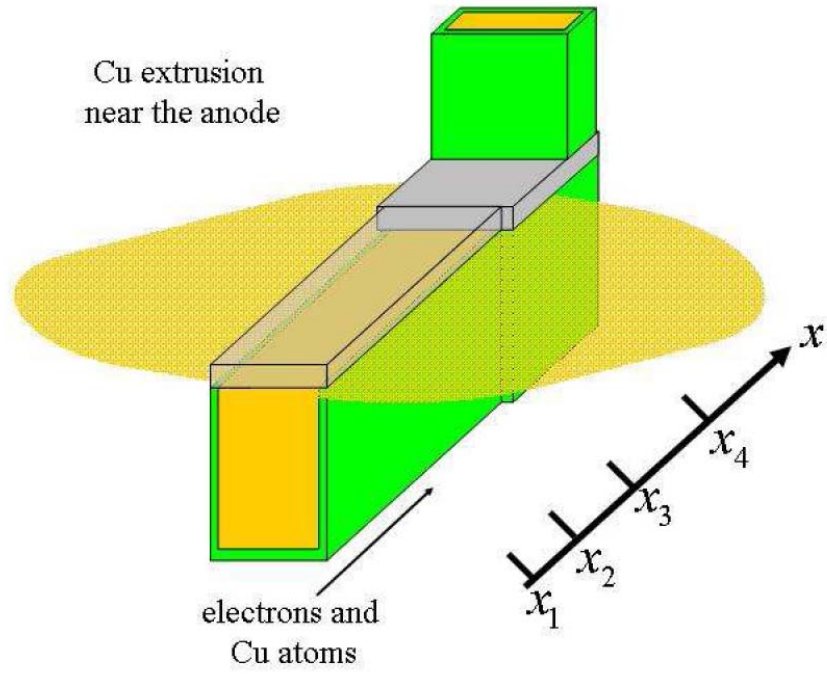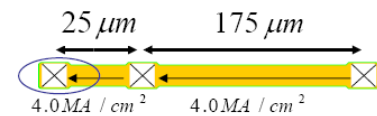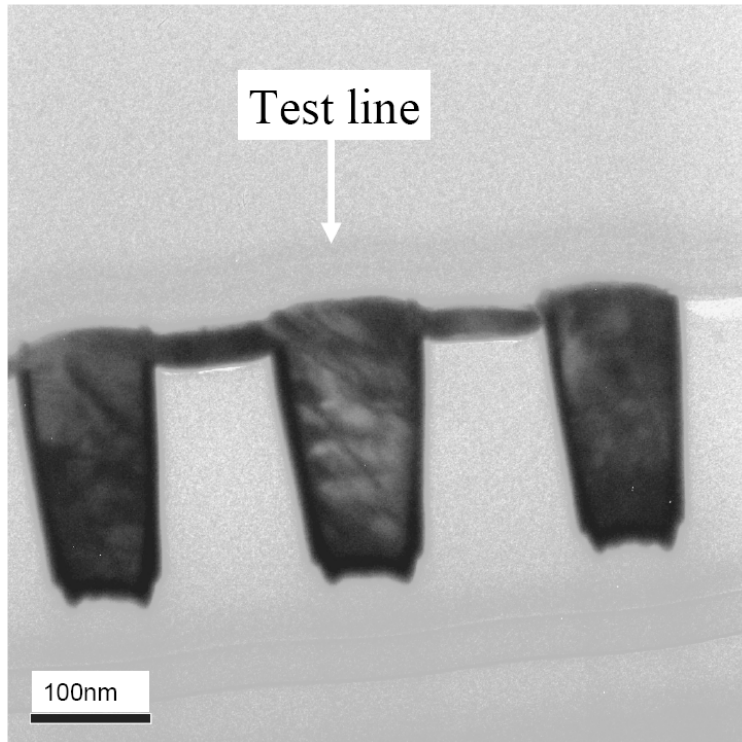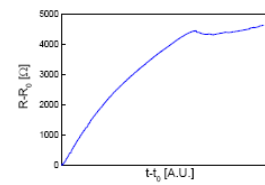
$\Delta R = 4630\ \Omega$

$expect\ void\ length \cong 6-7\ \mu m$

(b)

176

(c)
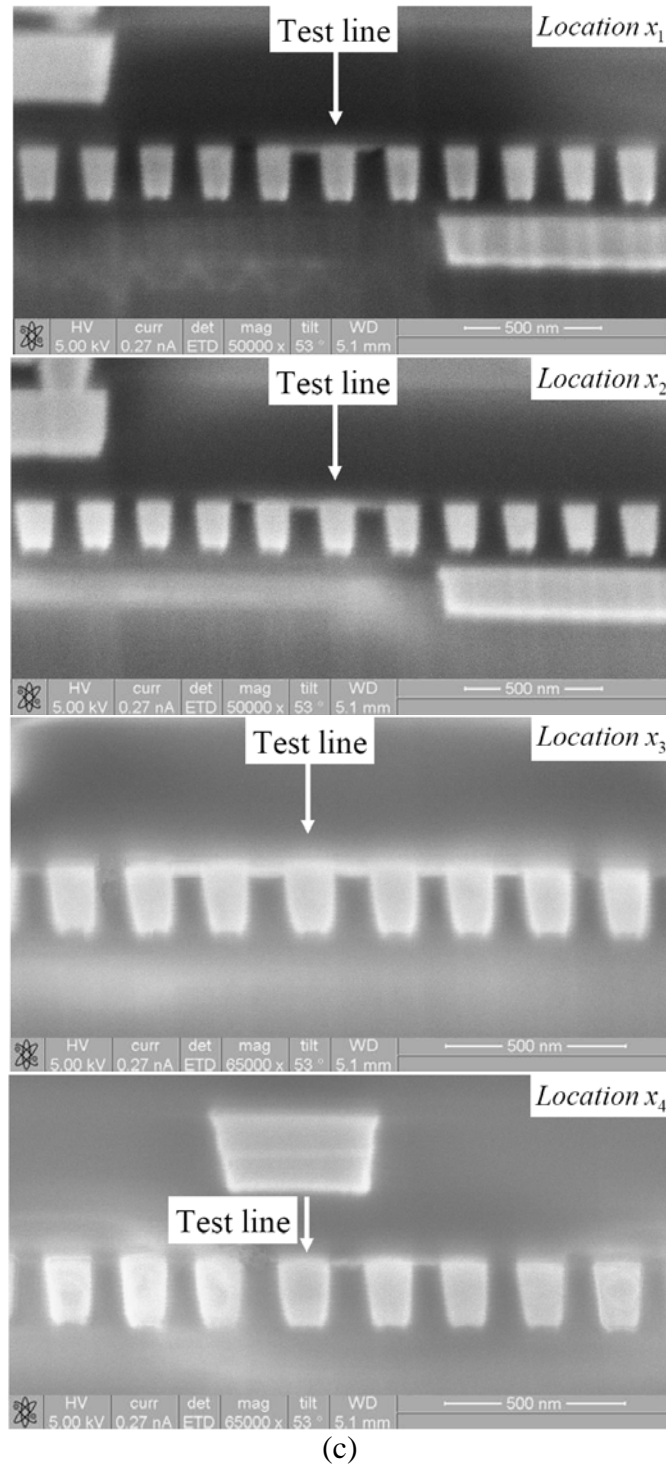
Figure 6.6 (a) Schematic illustration of the Cu extrusion observed in a test line from Experiment (B). (b) Transmission electron micrograph of the Cu extrusion formed in a structure where a 6.6μm long void was expected. (c) Cross-sectional scanning electron micrographs, each showing the extrusion at one of four different locations sequentially closer to the anode via. The measurements of the width of the extrusion at the four locations enabled the determination of the shape of the extruded patch.

6.3 Failure-Analysis-Based Assessment of $\sigma_{crit,ext}$

As mentioned previously, the changes in resistance recorded during the experiments correlate well with the sizes of the voids observed in failure analysis. By comparing the volume of the observed extrusions at the anode with the void volume at the cathode, a difference in volume can be calculated and used to estimate the stress in the Cu inside the interconnect at the anode. Using XSim, we calculated the compressive stress, $\sigma_{crit,ext}$, corresponding to the observed volumetric difference and estimate the stress at the anode, and therefore the critical stress for extrusion, $\sigma_{crit,ext} = 630MPa$. This result is consistent with the fact that no extrusions were observed on samples from Experiment (A), in which the testing conditions produced an expected steady state compressive stress less than 630MPa.

6.4 Effects of Mechanical Properties on $\sigma_{crit,ext}$

Failure analysis of the extrusions suggests that they result from near tensile (mode-I) loading of the capping/layer interface with the underlying materials. (As to be shown in later sections, the mode mixity angle is determined to be 4 to 7 degrees.) Once the loading leads to fracture at this interface, Cu extrudes into the crack. The effects of the mechanical properties of the medium on the critical stress for fracture, in this case on $\sigma_{crit,ext}$, are accounted for in the critical stress intensity factor, $K_{I,C}$. However, the appropriate expression for evaluation of $K_{I,C}$ depends on the geometry of the flaw at which the crack initiates.

6.4.1 The Incipient Crack Flaw

Using chevron-notch double cantilever pull test [Tad 07], the pure mode-I critical energy release rate for the interface between Ta and SiN films was determined (reviewed in Chapter 2). The critical strain energy release rate for the liner/SiN interface is estimated to be $G_{I,crit}(SiN/Ta) = 1.1 J/m^2$. The critical energy release rate for the interface between carbon doped SiO_2 (COD) low-k blanket films, with various values of k, with SiN films has been reported to be $3.0 J/m^2$ [Sch 06, Vla 05], when determined using the four-point bending technique. Empirically, for mix-mode interfacial cracking, like that produced in four-point bend tests, the critical energy release rate can be expressed by [Hut 92]

$$\Gamma = G_{I,C} \cdot [1 + \tan^2((1-\lambda) \cdot \psi)], \qquad\qquad (6.1)$$

where ψ is the mode mixity angle and λ is an adjustable fitting parameter, usually between 0 and 1. For the four-point bending test-specimen geometry similar to that in [Sch 06], $\psi = 40 - 45°$ [Hut 92, Eva 90, Cha 90]. The limit $\lambda=1$ represents an 'ideally brittle' interface with crack initiation occurring when $\Gamma = G_{I,C}$ for all mode combinations. This gives the possible range of $1.5 J/m^2 \leq G_{I,crit}(SiN/ILD) \leq 3.0 J/m^2$, which is larger than the mode-I critical energy release rate for the capping layer and Ta-liner interface. This comparison implies that the liner-capping layer interface does not serve as a barrier to crack propagation rather, decoheres prior to the threshold for capping layer/ILD interfacial cracking is reached. Therefore, the load-bearing Cu/capping-layer

interface and the short liner/capping-layer interface on either side of the interconnect near

the anode can be considered as the incipient crack (see Figure 6.7). An assumption of

plane-strain is most appropriate for such crack flaw geometry. Therefore,

$$\sigma_{crit,ext} = \sqrt{\frac{G_{I,crit} \cdot M}{\pi \cdot a}} \; ,$$

(6.2)

where a is half of the line width, and M is the effective plane-strain modulus of the

Cu/low-k interconnect system.
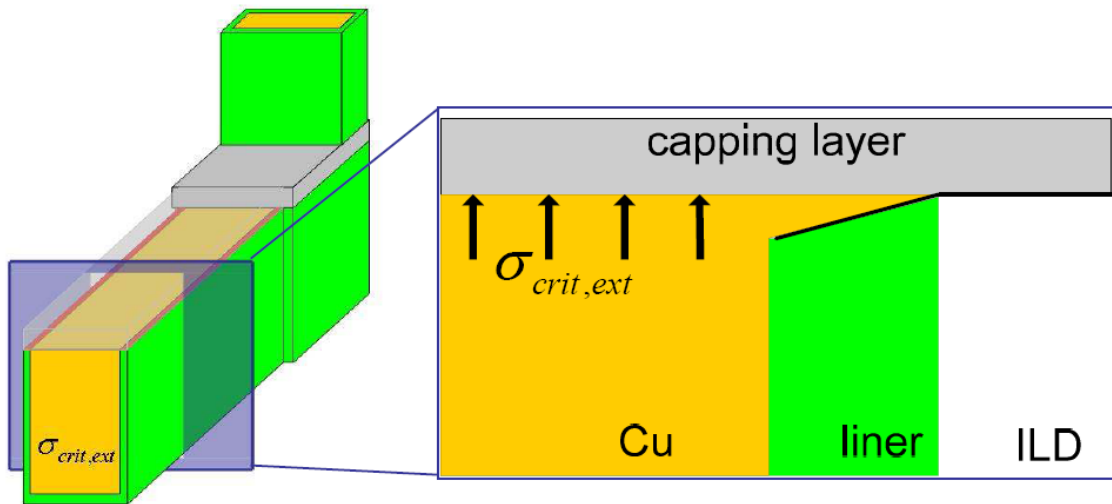
Figure 6.7 Illustration of the incipient crack flaw, debonding of the sidewall liner from the capping layer.

6.4.2 $\sigma_{crit,ext}$ Calculation

The critical energy release rate of the interface between SiN and parallel patterned Cu lines has been estimated to be 8.0*J/m²* for orthogonally propagating cracks [Sch 06, Lit 03], with measurements made using the four-point bending technique. Compared to the much lower fracture toughness of the SiN/ILD interface, the increase in adhesion energy is due to the substantial strain energy dissipation required for crack propagation across the ductile Cu lines. It should also be noted that this value of the adhesion energy is a strong function of the patterned line spacing and orientation [Sch 06, Lit 03]. When lines are more sparsely packed, the adhesion energy of the interface will decrease. Nevertheless, λ is clearly less than 1 for the interface of interest in the structures studied here, and $4.0 J/m^2 \leq G_{I,crit}(cap/lines) < 8.0 J/m^2$.

We performed FEM calculations using a commercial software package (ADINA) to obtain the effective plane-strain modulus of the Cu/low-*k* system. We used shell elements to construct the cross-sectional areas of the interconnects (see Figure 6.8(a)), and mirror symmetry with respect to the middle plane of the interconnects was applied. In this model, the elements corresponding to Cu were subjected to known amounts of pressure loading, *P*, while the deflection of the of Cu/capping layer interface, *GH* in Figure 6.8(a), was tracked as a function of *P*. Under applied pressures, the shell elements ensured that the out-of-plane strain was zero, so that the plane-strain loading condition was maintained. For plane-strain cracks, the crack opening displacement must follow the following form [Bar 02],

$$u_y = \frac{4}{M} \cdot \sqrt{a^2 - x^2} \cdot P.$$

(6.3)

Therefore, the effective plane-strain modulus, M, could be used as a fitting parameter in describing the shape of GH as a function of P, and was determined to be 20GPa. For the Cu/low-k geometries studied here, B and M are contrasted in Figure 6.8(b) as a function of the Young's modulus of the ILD. The magnitudes of B and M are similar, because the interconnect lines in this study have an extremely large aspect ratio, the line length (200μm) is much larger than the dimensions of the cross-section (0.1μm). Therefore, the conditions used in the FEM calculations that were used to calculate B, following [Hau 00a], were also nearly plane-strain. As expected, both moduli decrease as Young's modulus of the ILD decreases.

Using the value of M appropriate for the lines investigated in this study in Equation (6.2) yields $\sigma_{crit,ext} \approx 710MPa$, which is in agreement with the value determined in the preceding section (630MPa).

The FEM calculations can also help to estimate the mode mixity angle, ψ, for the extrusion process,

$$\psi = \tan^{-1} \frac{K_{II}}{K_I} = \tan^{-1} \frac{\sigma_{xy}}{\sigma_{yy}},$$

(6.4)

where σ_{xy} and σ_{yy} are the in-plane shear and normal tensile components of the stress at the edge of the incipient crack, H in Figure 6.8. In the stress range for the extrusion process, ψ is determined to be between 4 and 7 degrees, which corresponds to the liner/capping-layer decohesion process being nearly mode-I.
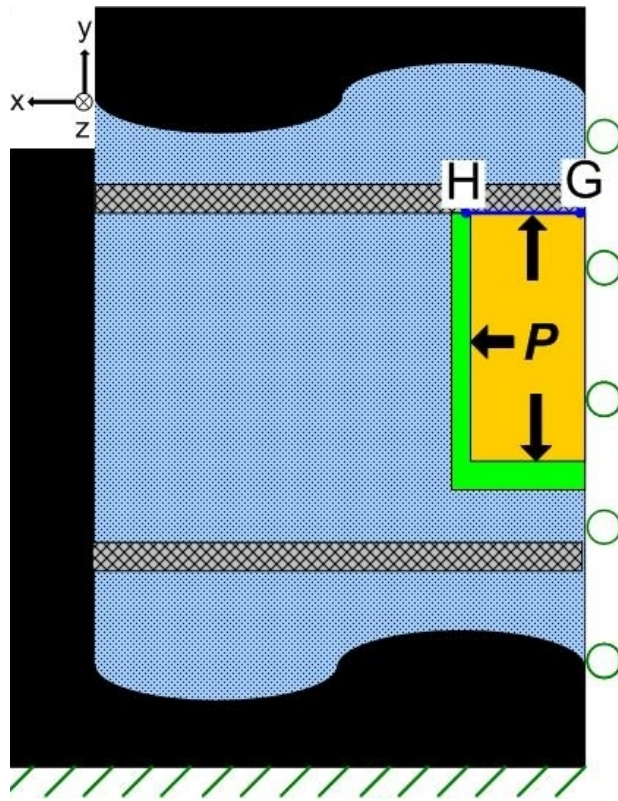
(a)
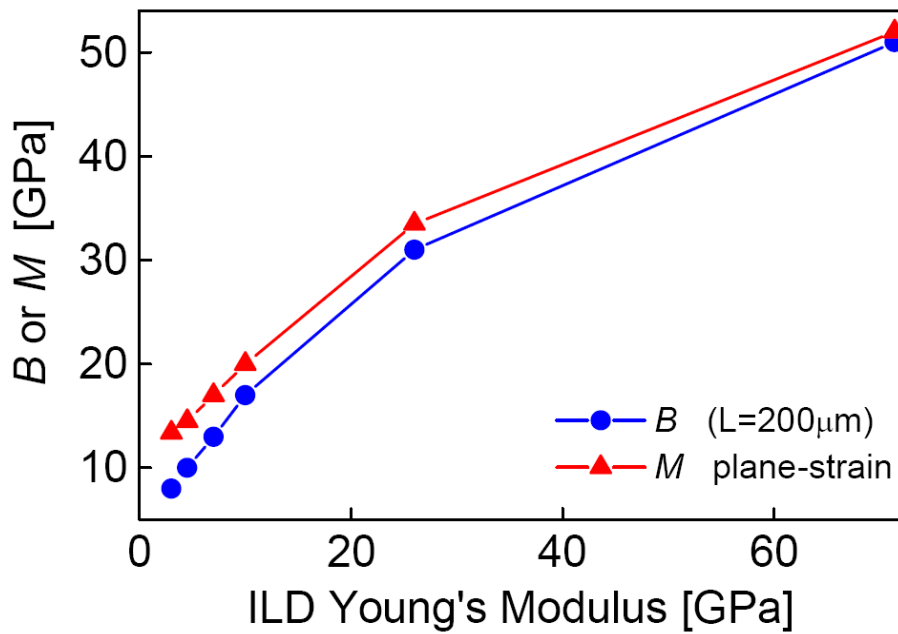
(b)

Figure 6.8 (a) Schematic of the interconnect cross-section generated in FEM modeling. (b) The calculated effective plane-strain modulus is compared with the effective bulk modulus, both as a function of the Young's modulus of the ILD.

6.4.3 $\sigma_{crit,ext}$: Post-extrusion Stress Relaxation

As failure analysis revealed, the continuously extruded Cu patch generally takes on an oval shape (see Figure 6.6(c)). Presumably, the extrusion would ultimately evolve toward a circular shape to achieve a uniform stress field and a minimum surface energy. Through the processes of Cu patch expansion, the characteristic length of the crack flaw, a, also increases. Thus, the compressive stress near the anode continuously relaxes. However, it is worth noting that, unlike the stress relaxations associated with void nucleation, Cu extrusions do not instantaneously relax all the stress that has built up before the extrusion initiates. The crack volume merely accommodates the Cu atoms that can not be elastically contained within the interconnect. Consequently, extrusion failures are not 'catastrophic,' and do not have a clear 'signature' in R vs. t traces.

The relaxed stress associated with an ellipse is [Sih 73]:

$$\sigma_{relax} \cong \frac{\sqrt{\pi}}{2} \cdot \sqrt{\frac{c}{a}} \cdot \sqrt{\frac{G_{I,crit} \cdot M}{a}} , \qquad (6.5)$$

where $2a$ and $2c$ are the minor and major axis lengths of the elliptical crack, respectively. By the end of the electromigration experiments in this study, $2a$ and $2c$ reached approximately 1.0 and 2.5-3.0μm, respectively. As a result, σ at the anode decreases from $\sim 710 MPa$ to $\sim 610 MPa$.

6.4.4 Stress Development Accounting for $\sigma_{crit,ext}$

The post-extrusion evolution of the resistance of a segment can be simulated by using σ_{relax} and $\sigma_{crit,ext}$ with XSim to analyze conditions corresponding to Experiment (B). The fully blocking boundary condition is replaced at the anode once $\sigma_{crit,ext}$ is reached. Instead, atomic concentrations were held at values corresponding to $\sigma_{crit,ext}$ and σ_{relax}. This leads to an increase in the stress gradient near the anode (see Figure 6.9(a)) and an associated increase in the back stress force. Consequently, void growth slows down, which is manifested experimentally in the decrease in $\frac{dR}{dt}$. Due to the lack of a blocking boundary at the anode, a linear spatial profile is not a stable solution for the stress inside the interconnect. Instead, a concave-up spatial profile in stress develops, as seen in Figure 6.9(a).

XSim calculations can also be used to track the amount of Cu that has electromigrated away form the cathode, both before and after Cu extrusion is initiated. Assuming that the corresponding Cu volume is present in the form of a void that fully spans both the width and thickness of the line, the corresponding resistance change can also be calculated, as shown in Figure 6.9(b). Also shown in Figure 6.9(b) are two experimental R vs. t curves, which are the upper and lower bonds. The good agreement between the calculated and experimental R vs. t traces further validates the analysis of $\sigma_{crit,ext}$ described above.
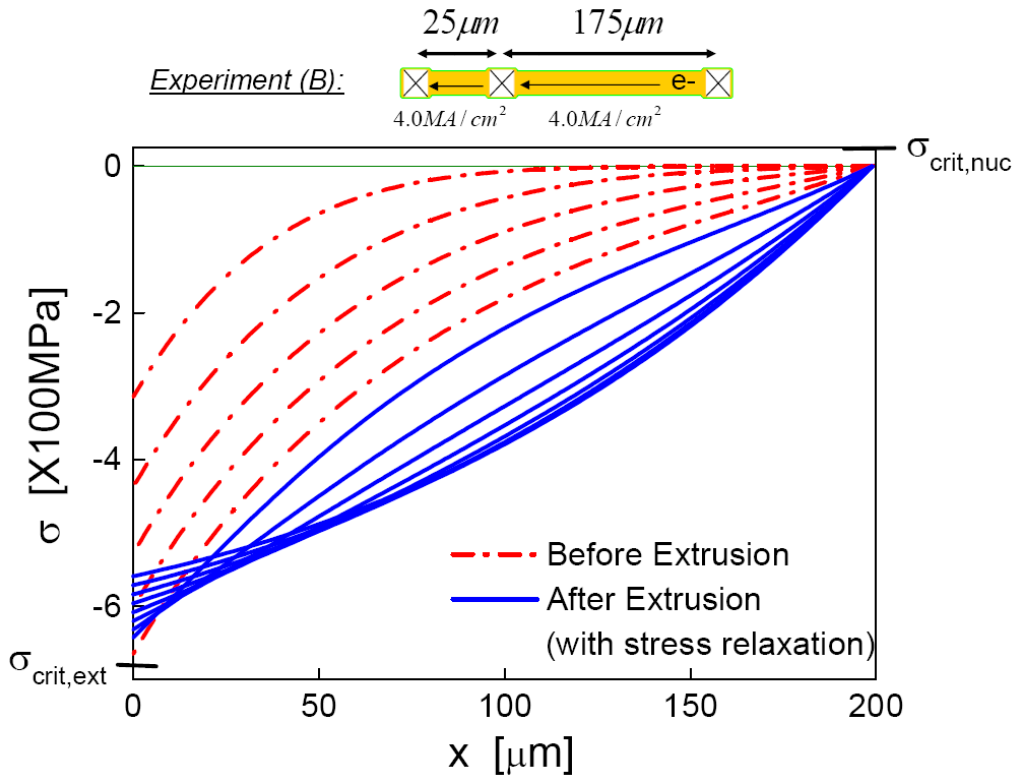
(a)
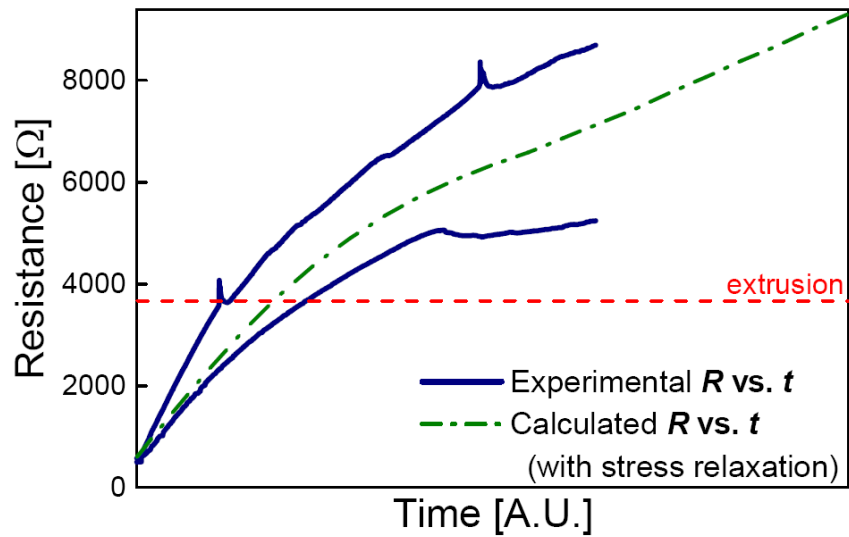
(b)

Figure 6.9 (a) Calculated time-dependent spatial stress profiles for Experiment (B), both before and after $\sigma_{crit,ext}$ is reached, calculated using XSim. (b) Calculated R vs. t traces for Experiment (B), along with two experimental R vs. t curves, which are the upper and lower bonds in the results of Experiment (B).

6.4.5 Surface Energy Contributions

The aforementioned analysis uses critical energy release rates determined through fracture toughness experiments. However, in the Cu extrusion process studied here, the newly formed crack surfaces are covered by the extruded Cu patch instead of being free surfaces, as in the case of fracture toughness tests. Therefore, the different interfaces present in the two cases may, in theory, lead to a difference in surface energy contributions to the fracture process.

Generally, fracturing processes are expected to have work contributions from both the energies of the newly created surfaces and the plasticity required for fracture [Irw 49],

$$G_C = 2 \cdot (\gamma_{Surf} + \gamma_{Plastic}) . \tag{6.6}$$

The effect on γ_{Surf} is accounted for in the following way for the case of fracture toughness tests:

$$\Delta \gamma_{Surf}(fracture\ test) = -\gamma_{SiN/Cu} - \gamma_{SiN/SiO_2} + \gamma_{vac/Cu} + \gamma_{SiN/vac} + \gamma_{SiO_2/vac} , \tag{6.7}$$

and for the Cu extrusion process,

$$\Delta \gamma_{Surf}'(extrusion) = -\gamma_{SiN/SiO_2} + \gamma_{SiN/Cu} + \gamma_{SiO_2/Cu} , \tag{6.8}$$

where the capping layer is approximated as SiN, and the ILD is approximated as SiO$_2$. The difference between Equation (6.7) and (6.8) is the correction needed for comparisons between the analysis shown here and the referenced experimental results,

$$correction = (-\gamma_{SiN/Cu} + \gamma_{vac/Cu}) + (\gamma_{SiN/vac} - \gamma_{SiN/Cu}) + (\gamma_{SiO_2/vac} - \gamma_{SiO_2/Cu}). \quad (6.9)$$

However, because Cu, SiN, and SiO$_2$ are virtually inert in reactions with each other, most of the interface energies are equivalent to those free surfaces, about 1J/m^2. $\gamma_{Cu/Vac} = 1.2 J/m^2$ [Smi 92], $\gamma_{SiN/Cu} \leq 0.9 J/m^2$ [Pan 04], $\gamma_{SiN/Vac} = 1.1 J/m^2$ [Ste 02], $\gamma_{SiO_2/Vac} = 1.0 J/m^2$ [Ile 79], and $\gamma_{SiO_2/Cu} = 0.84 J/m^2$ [Gad 03]. Therefore, the surface energy correction can be ignored for the $G_{I,C}$ used in the analysis presented above.

6.4.6 Implication of Results

In the analysis presented here, both σ_{relax} and $\sigma_{crit,ext}$ depend on not only M, which depends on the Young's modulus of the ILD, but also $G_{I,crit}(cap/lines)$, which is a strong function of the patterned line spacing and orientations, and the line width (a is one half of line width when the crack initiates). This result implies that sparsely-packed, intermediate to wide interconnect lines could be more susceptible to electromigration-induced extrusion damage. For example, consider a 0.8µm-wide, 0.5µm-thick, and 200µm-long Cu/low-k interconnect segment embedded in an ILD with a Young's modulus of 3GPa (corresponding to $M = 8GPa$), which is far enough away from other interconnect segments that $G_{I,crit}(SiN/ILD)$ could be used to approximate its capping

layer adhesion. These conditions give , $\sigma_{crit,ext} \cong 100MPa$, which corresponds to growth

of a fully spanning void of length 0.4μm. Using common via redundancy schemes at the

cathode, it is plausible that such an interconnect segment could fail due to extrusions

before failing due to void growth. Electromigration-induced extrusion, in this case, is a

competing failure mechanism with void growth.

6.5 Conclusions

We performed electromigration experiments using 200μm-long Cu/low-*k*

interconnects embedded bound by a Ta-based diffusion-barrier liner on three sides, and

embedded in an ILD consisting of a form of carbon-doped SiO_2-based material deposited

by PECVD. The unusual robustness of the Ta-based diffusion barrier allowed continued

testing and void growth well after observation of 10%R_0 resistance increases without any

occurrence of open-circuit failures. Voids that fully spanned the width and thickness of

the lines, and with lengths of 10μm or more were observed during microscopic analysis

at the cathode end. Through thorough microscopic analyses of the anode end of these

test structures, it was also found that the Cu transported from the cathode end contributed

to formations of extrusions of Cu along the ILD/SiN-capping-layer interface. This

extrusion failure mode was modeled as near mode I (tensile) fracture with a mode mixity

angle of 4 to 7 degrees. The incipient crack flaw geometry corresponds to a plane strain

condition, and the effective plane strain modulus was determined using FEM analyses.

The critical stress required for extrusion, $\sigma_{crit,ext}$, calculated in this way (~710MPa) agrees

well with the value estimated through comparison of the volumes of the extrusion and the

corresponding void. This analysis further suggests that sparsely-packed, intermediate to wide interconnect lines could be more susceptible to electromigration-induced extrusion damage, especially as low-k ILDs with lower stiffness and thinner liners are deployed.

Chapter 7

Conclusions and Future Work

In this thesis, the effects of the mechanical properties on the mechanisms of failures induced by electromigration were examined. Three regimes of interest can be defined; void nucleation, void growth to a critical volume, and Cu extrusions. Key dependencies for each process were determined. In all cases, it is found that a decrease in the elastic response of the Cu-interconnect system, i.e., B, leads to a degradation in reliability. Techniques for characterization of the relevant mechanical properties and diffusive parameters for electromigration have been developed and demonstrated. Stemming from these results, future directions for related research can be identified.

7.1 Conclusions

The Korhonen model [Kor 93, Cle 95] provides an accurate framework for all electromigration phenomena, including those in Cu/low-k interconnects. Calculations using this model can be carried out using XSim, a MatLab-based numerical solver developed at MIT [Cho 04, Cho 07]. However, experimentally-based knowledge in two areas is essential in order to complete the description of electromigration in Cu/low-k interconnects: mechanical and diffusive properties.

The elastic response of an interconnect system depends on the elastic properties of its constituent materials. A suite of characterization techniques was investigated, using mainly two low-k films, F-TEOS and MSQ, as case studies. Self-consistent measurements of Young's modulus of the low-k films were made using nanoindentation, cantilever deflection, and membrane bulge tests. However, it was found that during nanoindentation of low-k films, the substrate contribution to the measured modulus can be significant, even when the indentation depth as less than10% film thickness [AST 87]. Accurate subtraction of the substrate contribution should be made based on either analytical [Gao 92] or FEM [Che 01] methods. Substrate-free measurements can be accomplished using cantilever deflection techniques. The inaccuracies introduced by the non-ideal supports resulting from the micro-fabrication can be reduced by applying a modified beam equation with a fitting parameter, L_C, a correction length [Men 99], in the analysis. Cantilevers cannot be readily made for characterization of MSQ films, but, in principle, a membrane bulge test can be used, if over- and under-layers are used to environmentally protect the MSQ layer during wet etching. However, the protective SiN layers used in the current study were much stiffer than MSQ. Consequently, the elastic properties of MSQ could not be accurately extracted. Other material properties, such as, residual stress, stress gradients, mode-I fracture toughness, and coefficient of thermal expansion, were also investigated using micro-beams, chevron-notch double cantilever pull, and wafer curvature measurements.

Using FEM analyses similar to those presented by S.P. Hau-Riege *et al.* [Hau 00a], B was calculated for a combination of Cu and ILD interconnects. It was determined that B decreases monotonically with the Young's modulus of the ILD. It was also found

that a tensile residual stress in the Ta liner can have a positive effect on *B*, while a compressive residual stress has a negative effect on *B*. Geometrically, *B* changes with respect to the liner thickness, line width, and line length. As the interconnect line length increases, *B* approaches *M*, the effective plane-strain modulus.

The dominant diffusion path in Cu-interconnects is the interface between Cu and the capping-layer. The kinetics of electromigration can be characterized by correlating gradual resistance increases over time, a result of steady void growth, with the drift velocity. In the case of experiments using Cu/low-*k* interconnect trees discussed in Chapter 5, it is evident that such kinetic measurements directly correspond to the combined effects of the electron wind and back stress forces. Therefore, such measurements are more fundamental than lifetime measurements alone and can allow separate extraction of the effective diffusivity and the effective valance.

Investigations of Blech length effects using Cu-interconnect segments point to a probabilistic, rather than, deterministic critical *jL* value due to the possibilities of pre-existing voids and the low tensile stresses required for void nucleation, which have been estimated to be in the range of few tens of MPa [Hau 02, Hau 04]. A small, slit-like void will cause open-failure, if it occurs directly under a via in Cu-metallizations. The void nucleation process is viewed as stored strain energy relief processes, which occur at the cost of increased surface energy. C.S. Hau-Riege *et al.* [Hau 04] argued that the resistance to void nucleation should scale with $\sqrt{B}$.

In actual circuits, interconnect trees are the fundamental reliability units, because connected interconnect segments can serve as active atomic sinks and reservoirs for linked segments, so that the reliabilities of the segments are coupled. The degree of the

coupling becomes more significant as the stress inside interconnects evolves beyond the point of void nucleation and into the void growth regime, in which case the maximum compressive stress is usually expected to be in the range of about 100 MPa for interconnects with typical dimensions. Using Cu/low-*k* interconnect tree structures, in which failures occurred due to void growth, it was demonstrated that atomic reservoirs improve the reliability of the failing segment, and atomic sinks degrades the reliability of the failing segment. The amount by which the reliability is altered quantitatively depends on the stress development, which is a function of both the mechanical properties as well as the diffusive parameters. The analyses shown in Chapter 5 demonstrate the accuracy of the Korhonen model, when used with correct inputs based on experiments. Predictive reliability calculations for interconnect trees with similar atomic reservoir and sink conditions, but with ILDs of different Young's modulus, were also made. As *B* decreases, it is seen that the benefits of the atomic reservoirs will decrease, while the disadvantages of the atomic sinks will increase.

Unusually robust liners allowed the experiments on Cu/low-*k* interconnect trees to continue well after void nucleation, to conditions under which compressive stresses greater than several hundreds of MPa were reached, and electromigration-induced Cu extrusions were seen at the anode. Failure analysis identifies near mode-I interfacial cracking to be the mechanism for this failure mode. The condition under which the crack propagates closely resembles plane-strain loading. Therefore, the critical stress required for extrusion failures is found to be proportional to $\sqrt{\dfrac{G_{I,crit} \cdot M}{a}}$, where $G_{I,crit}$ is the critical energy release rate of the fracture interface (between the capping layer and the metallization/ILD layer below), and *a* is one half of the interconnect width. This result

implies that sparsely packed, wide interconnects are most prone to electromigration failures due to extrusions. The risk of such failure can be alleviated during circuit design by replacing a wide interconnect segment that is susceptible to electromigration with several parallel narrower segments (see Figure 7.1). This way, a is decreased while $G_{I,crit}$ is increased to improve the threshold for extrusion.
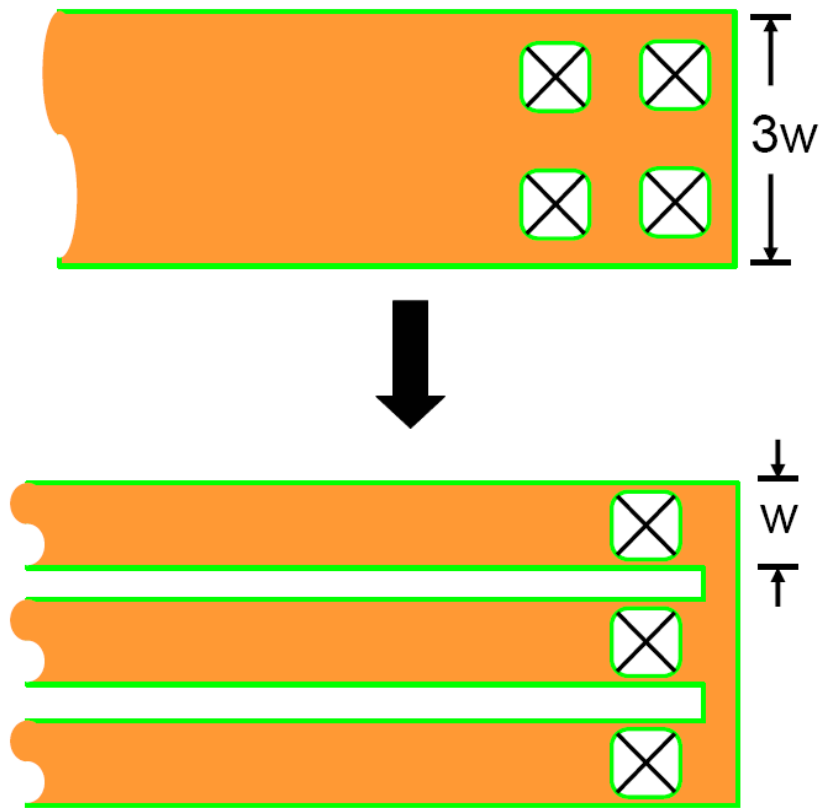
Figure 7.1   An example of an alternate design to reduce the risk of failure by electromigration-induced extrusion in Cu/low-k interconnects. The proposal illustrated here is to divide a wide interconnect segment into equal-width narrower segments, to promote the decohesion toughness.

7.2 Future Work

7.2.1 Improvements for *SysRel*

The experimental findings of this thesis can be incorporated into *SysRel* to improve the existing methods for circuit-level reliability assessments. Gan C.L. *et al.* [Gan 03] demonstrated that the void growth default model in *SysRel* for estimating the lifetime is overly conservative. Improved experimental understanding of the effects of atomic reservoirs and sinks could lead to the development of a more accurate default models.

A criteria for electomigration-induced extrusion can now also be implemented in *SysRel*. Potentially problematic interconnect trees can be analyzed using XSim to determine if extrusions could be possible failure mechanisms.

7.2.2 Investigations of Via-landing Shape on Reliability

In the experiments on Cu/low-*k* interconnect tress, no open-failures, or slit-like voids under the cathode via, were observed. The *R* vs. *t* traces indicate formation of voids that fully spanned the cross-section of the interconnects. In many instances during failure analysis, such voids were observed at a distance away from the cathode via. Z.-S. Choi [Cho 07] reported that, based on XSim calculations, pre-existing voids that are sufficiently close to the cathode end via could lead to void pinning and subsequent growth at locations other than directly below the via. Li *et al.* [Li 04] reported that when the bottom of the via overlaps with the sidewalls of the interconnect segment below, voids that fully span the cross-section of a line could be achieved, on occasion, at a

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distance away from the via location, similar to that observed in the Cu/low-*k* interconnect tree studies. However, there have not been any experimental characterizations of the effects of the geometry via-landings on the preferential site for void nucleation. The implication of such investigations could be enormous: detrimental slit-like voids under the via could be eliminated in Cu-interconnects through the design of an appropriate via landing geometry. All electromigration failures would occur through void growth to a critical volume corresponding to an unacceptable resistance increase, or due to extrusions, both of which require much longer times than void nucleation.

7.2.3 Electromigration-induced Cu Leakage through the Liner

Failure analysis on Cu/low-*k* interconnects indicated that electromigration-induced Cu leakage through the thin refractory metal liner is smaller than the detection limit of chemical analysis using SEM/EDX. However, the results are inconclusive in showing whether a minute amount of Cu could leak into the ILD through the Ta-based liner, driven by electromigration or line-to-line voltage drops. The potential damage to the breakdown threshold of a low-*k* film by a small amount of Cu is tremendous [Llo 06]. Therefore, we can devise a simultaneous electromigration and time-dependent dielectric breakdown (TDDB) experiments to determine if electromigration can trigger other physical failures in Cu/low-*k* metallizations.

7.2.4 Mechanical Characterization

The Korhonen-model-based investigative approach presented in this thesis can be applied to the study of Cu-interconnects with many different low-k ILDs, as long as accurate diffusive and elastic materials parameters are obtained. However, during the mechanical characterization studies, it was found that, on several occasions, due to the low stiffness of the low-k films, the detection limit of the experimental technique was similar in magnitude as the materials property to be determined. The membrane bulge test holds a great potential for improvement. The current experimental setup uses SiN protective layers with thicknesses of similar magnitude to the thickness of the low-k film of interest. A possible future investigation could include evaporative deposited Au or other thin films as protective layers. Such films with thickness on the order of several hundred Å could have lower residual stresses and resist chemical etching. Thus, the mechanical response of a much thicker low-k film in a multi-layer membrane could be maximized.

Currently, research on adhesion properties mainly focuses on the use of the four-point bending technique, which produces results with both mode-I and -II contributions. It has been shown that by varying the specimen geometry, the range of mode mixity angles that can be achieved is between 35 to 60 degrees [Even 90]. In the analysis of Cu extrusions, the interfacial fracture was seen to be close to mode-I. The ensuing analysis extrapolated quantities from the fracture toughness from four-point bending results. In the future, adhesion characterizations involving SiN films and Cu/ILD metallization layers employing pure mode-I or to low mode mixity loading would be more appropriate. The chevron-notch double cantilever pull technique can be used for such experiments.

Appendix

International Sematech Cu/low-*k* Interconnects

A.1 Cu/low-*k* Interconnects Fabricated by International Sematech

The Cu/low-*k* interconnect structures fabricated by International Sematech in collaboration with MIT currently uses 300mm-diameter Si(100) substrates and an ultra-low-*k* porous ILD, with a *k* of 2.3 and a Young's modulus of about 5.5 to 6 GPa, that is deposited using PECVD methods. MSQ, deposited using spin-on methods, was used as the low-*k* ILD prior to year 2005, and is no longer being pursued as a candidate ILD material for Cu/low-*k* studies by International Sematech. Through physical analysis using an FIB/SEM on untested samples, it is observed that the Cu/PECVD-low-*k* structures fabricated by International Sematech show the following characteristics.

In order to prevent environmental degradation of the Cu/low-*k* structures, presumably assisted by moisture from the atmosphere, two through-thickness metal guard-rings were designed to surround all test structures in a fashion shown in Figure A.1(a). A cross-sectional micrograph of a fabricated Cu guard-ring in the MIT/Sematech structures is shown in Figure A.1(b). It is seen that the guard-ring extends through both layers of metallization (M1 and M2 levels), the via level in between M1 and M2, and the passivation layer on top of M2, which terminates with exposed Cu at the surface. At each level, Cu is confined by Ta liner on the sides and bottom, though there is not a via level

between the Cu metallization in M2 and in the passivation level. The guard-rings are 10µm wide at M1 and M2 levels, and are 5µm wide at the exposed passivation level (see Figure A.1(b)).

(a)

E-Beam	Spot	Mag	Tilt	Det	FWD	10/15/06		2 µm
5.00 kV	3	25.0 kX	52.0°	SED	4.729	19:22:49		
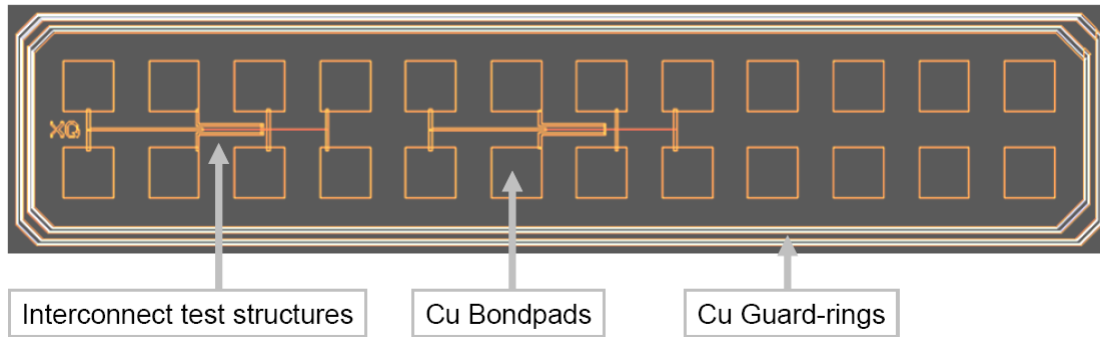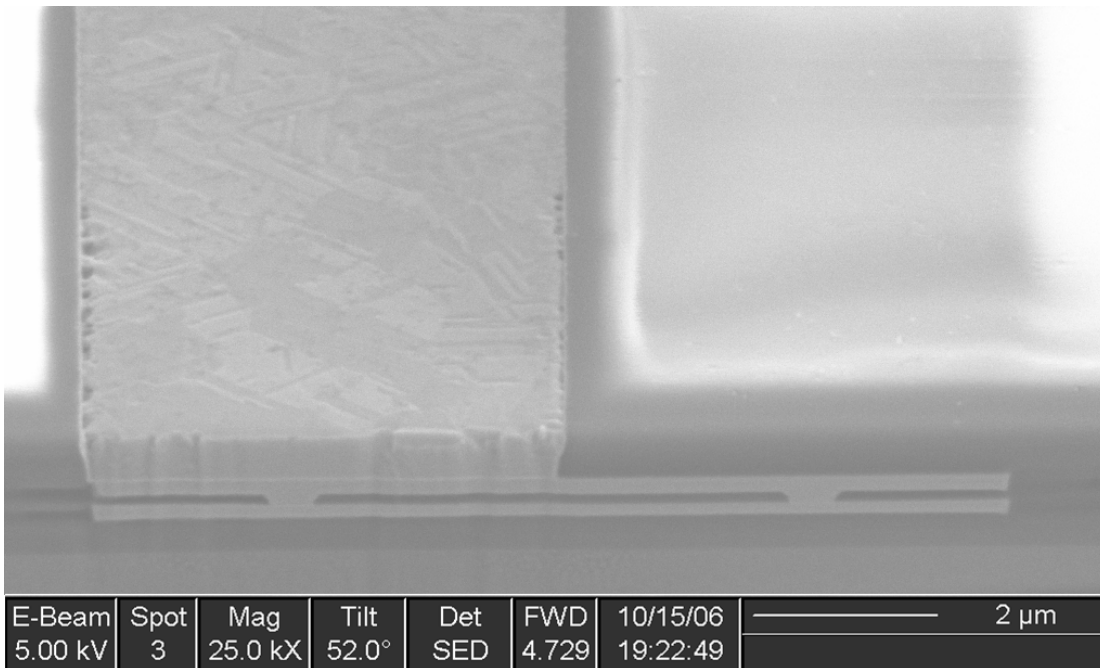
(b)

Figure A.1 (a) International Sematech mask design for the Cu/low-*k* test structures with metal guard-rings to prevent environmental degradation of the interconnects. (b) Cross-sectional SEM micrograph of the through-thickness Cu guard-rings in Sematech Cu/low-*k* structures.

In addition to showing the geometry of the Cu guard-rings of the Cu/low-k structures, Figure A.1(b) also shows micro-voids forming along the edge interfaces between the Cu and the Ta liner. Similar voids along the Cu/Ta liner edges were observed throughout large surface features of the Sematech interconnects, including both the Cu guard-rings and the exposed Cu bondpads. The origin of such voids is unknown, since no stress voiding was observed at other interfaces. However, it may be reasonable to suspect the edge voids are caused by a CMP process during which one of the slurry component etches or delaminates Cu from this particular edge interface.

Cross-sectional SEM micrographs of untested interconnect test features show that the spacing between the test lines and the extrusion monitor rings is not well-controlled in the current Sematech Cu/low-k structures (see Figure A.2). Observations were made using several dies from different locations on the wafer. Consistently, lines with narrow width (0.15μm) are separated from the extrusion monitor rings at a distance corresponding to the designed spacing. However, for lines with wide width (1.4μm), it was seen that the spacing between the test line and the extrusion monitor ring is much smaller than the designed spacing. On several occasions, shorting between the line and extrusion monitor ring was observed (see Figure A.2(b)).
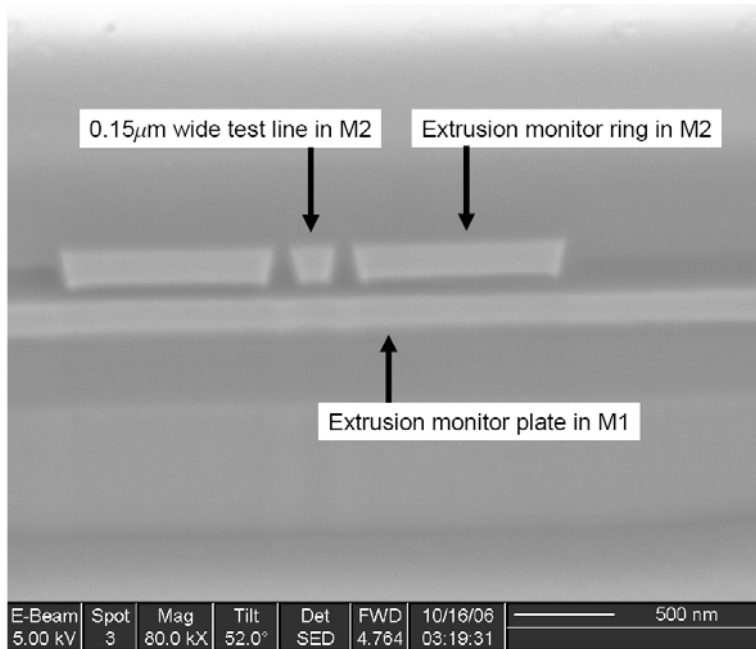
(a)
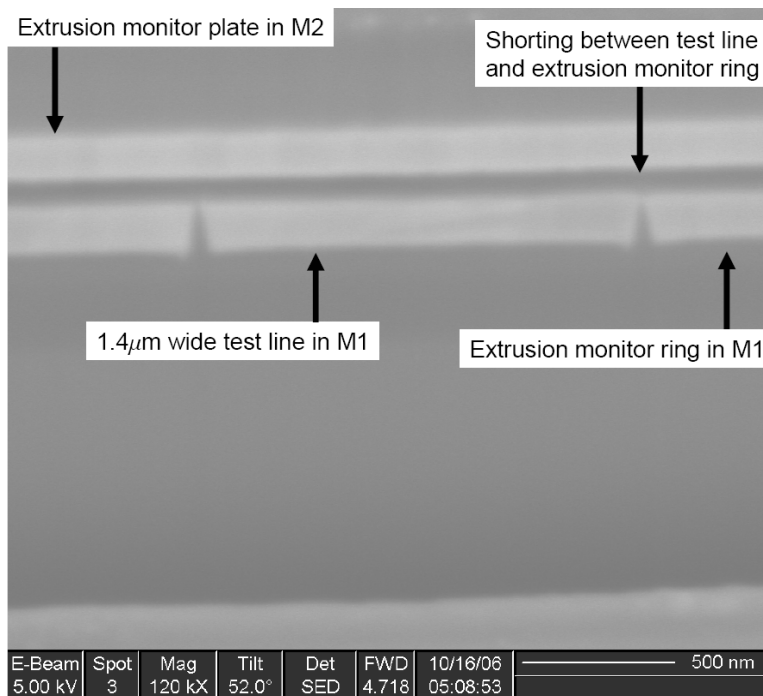
(b)

Figure A.2 Cross-sectional SEM micrographs of untested structures: (a) a 0.15μm-wide test line with designed spacing away from its extrusion monitor ring, (b) a 1.4μm-wide test line shorting with its extrusion monitor ring.

A.2 Al Passivation of Exposed Cu Bondpads

Similar to the construction of the Cu guard rings, the metallization in the Cu bondpads in Sematech structures also includes M1 and M2 layers, the via layer between M1 and M2, and the exposed Cu features in the passivation layer (see Figure A.3). Since electromigration tests require elevated temperatures, the exposed Cu bondpads would readily oxidize during experiments. A process was developed in which Al film passivation layers were deposited and patterned at MIT after receiving the fabricated Cu/low-k interconnect structures from International Sematech.
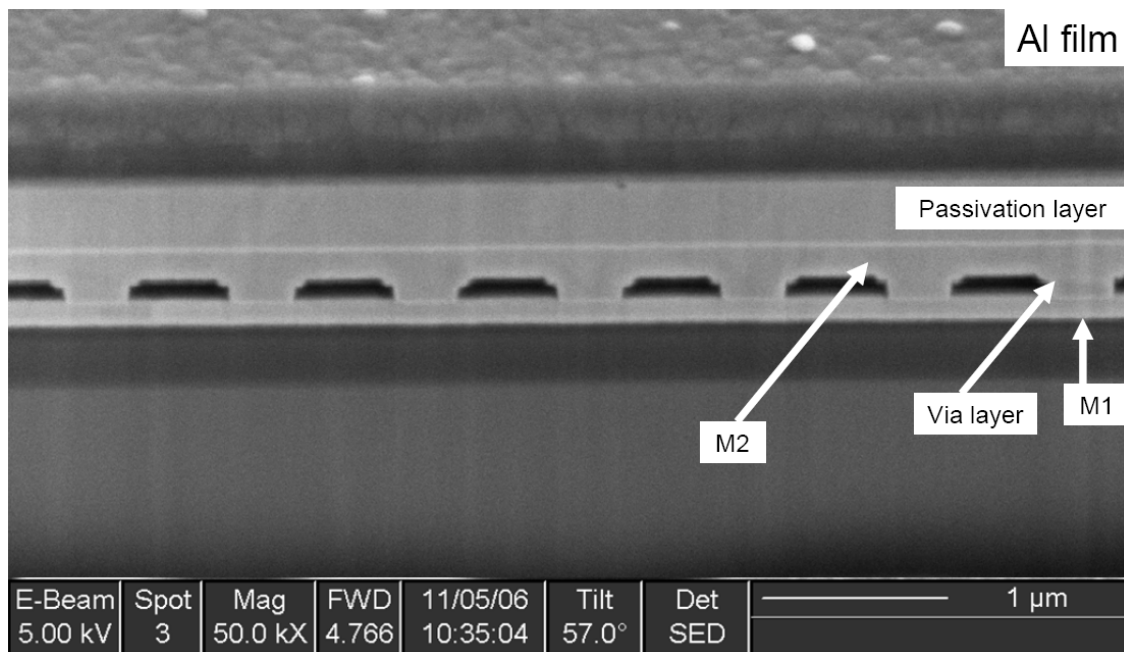
Figure A.3 Cross-sectional SEM micrograph of a Cu bondpad covered with an Al film deposited at TRL at MIT, using the ebeam evaporation method.

An Al ebeam lift-off process using negative photoresist was devised using deposition tools available at the Technology Research Laboratory (TRL) at MIT. A mask was created using the coordinates and the stepping distances used in the Sematech 465AZ mask design. In order to make the 300mm-diameter pre-fabricated wafer from Sematech compatible with the 100 or 150mm tools available at TRL, the Sematech wafer was first cleaved into individual strips containing 3 to 8 dies in a row (see Figure A.4(a)). Second, a negative photoresist was spun on each wafer strip and developed using the aforementioned mask to expose windows above the Cu bondpads (see Figure A.4(b)). The wafer strips were then transferred into a Temescal VES2550 (BOC Edwards, Inc., England) ebeam evaporator. In order to promote adhesion, a 400Å-thick Ti layer was deposited before a 4000Å-thick Al film was evaporated on top. The deposition was carried out under high vacuum conditions at a rate of 2Å per second. Lastly, the remaining photoresist on the surface of the wafer strips was dissolved using acetone, leaving the Cu bondpads covered with Al passivation (see Figure A.4(c)).
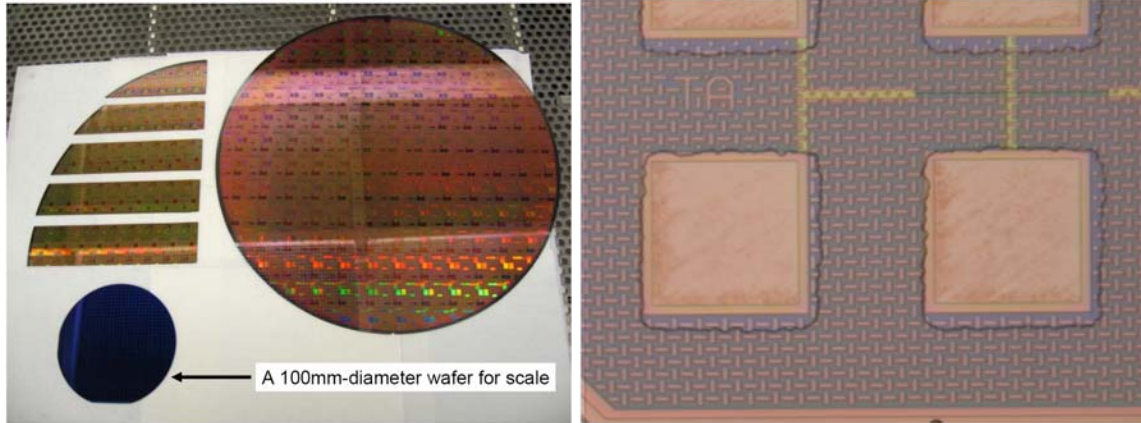
(a)   (b)
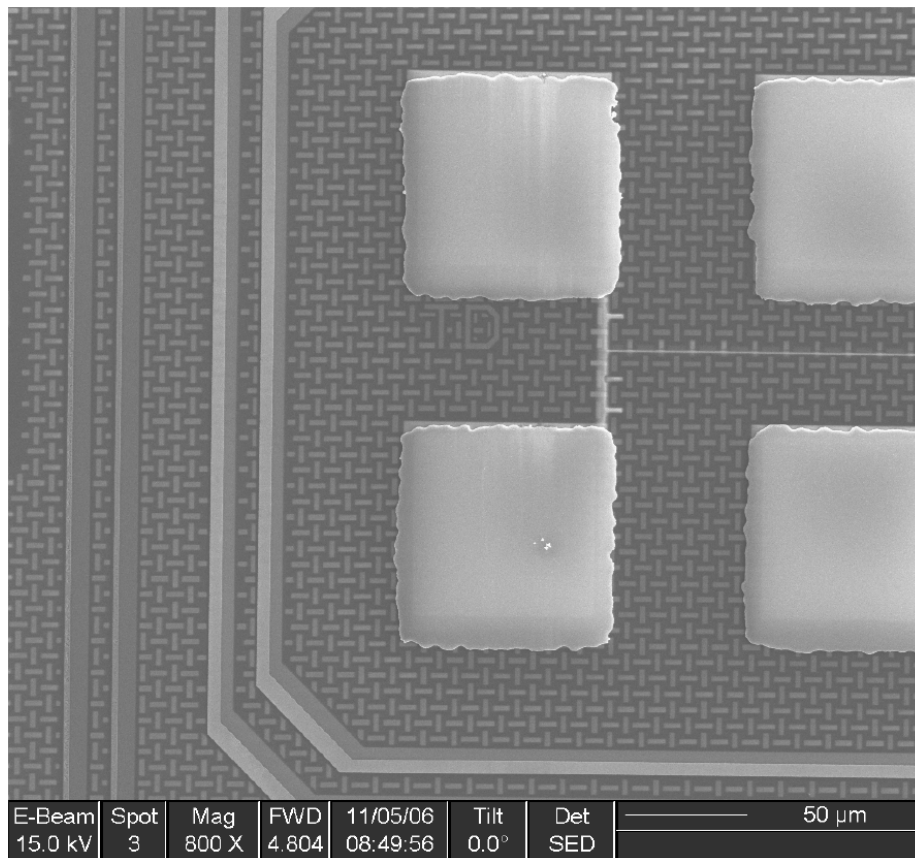
(c)

Figure A.4 Lift-off process used to deposit Al passivation on top of exposed Cu bondpads. (a) Cleave 300mm-diameter wafer into single-die-row wafer strips, (b) expose and develop negative photoresist to create windows for bond pad areas, and (c) lift-off the ebeam evaporated Al film, with a Ti underlayer film as an adhesion-promoting layer.

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A.3 Library of Interconnect Structures

This section describes all the interconnect test structures designed on the 465AZ mask at International Sematech in collaboration with MIT.

Straight line test segments:

Table A.1 Straight line test segments on the International Sematech 465AZ mask design. The alpha-numeric designation outside the parenthesis corresponds to the bondpad lane in the die, and the designations between the parentheses correspond to the structure's metallization level.

L [μm]	W [μm] 0.15	0.23	0.5	0.8	1.4
10	Z2(M1) Z6(M2)	Z2(M1) Z4(M1) Z6(M2) Z8(M2)	-----------------------	----------------------	Z2(M1) Z6(M2)
20	TI(M2) TP(M2) TO(M1) TJ(M1)	----------------------	TH(M2) TN(M1)	----------------------	----------------------
25	Z2(M1) Z6(M2)	----------------------	-----------------------	----------------------	Z2(M1) Z6(M2)
50	TI(M2) TP(M2) TO(M1) TJ(M1)	Z4(M1) Z8(M2)	TH(M2) TN(M1)	Z1(M1) Z5(M2)	Z1(M1) Z5(M2)
100	TD(M2) TM(M1)	Z3(M1) Z7(M2)	Z3(M1) Z7(M2)	Z3(M1) Z7(M2)	Z1(M1) Z5(M2)
250	Z3(M1) Z7(M2)	----------------------	-----------------------	----------------------	----------------------
1000	TH(M2) TJ(M1) TN(M1) TP(M2)	Z4(M1) Z8(M2)	TI(M2) TP(M2) TJ(M1) TO(M1)	TH(M2) TN(M1) Z4(M1) Z8(M2)	TD(M2) TI(M2) TM(M1) TO(M1)

Interconnect Tree Structures:
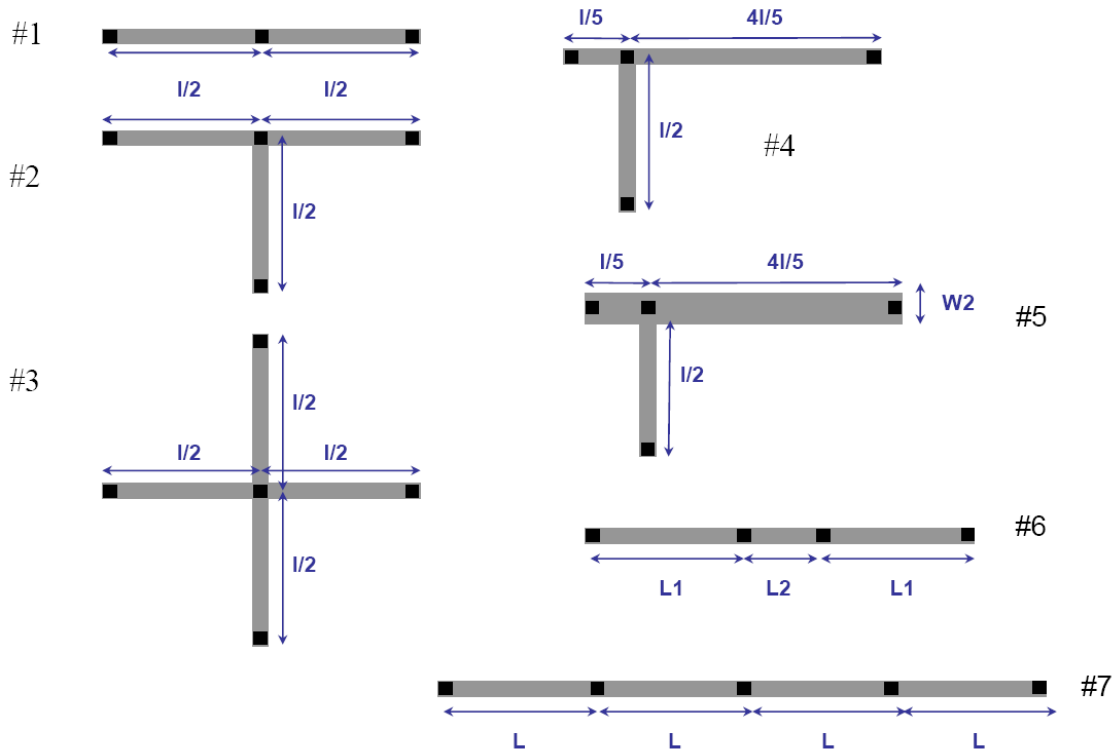
Figure A.5 Interconnect tree structure identifier.

Table A.2 Interconnect tree structures on the International Sematech 465AZ mask according to the identifiers shown in Figure A.5. The alpha-numeric designation outside the parentheses corresponds to the bond pad lane in the die, and the designation between the parentheses corresponds to the structure's metallization level. The unit for length is μm, while the width is 0.15μm in all cases.

Tree 1	Tree 2
L=10 TM(M2) XB(M2) X1(M1)	L=10 X3(M1) XB(M2)
20 TA(M2) X1(M1)	20 X2(M1) TB(M2)
50 TA(M2) X1(M1)	50 X2(M1) TB(M2)
100 TA(M2) X1(M1)	100 X2(M1) TB(M2)
500 TA(M2)	500 TC(M2)
Tree 3	**Tree 4**
L=10 X5(M1) XB(M2)	L=10 X6(M1) X7(M1) XD(M2)
20 X4(M1) XC(M2)	20 X6(M1) X7(M1) TC(M2)
50 X4(M1) XC(M2)	50 X6(M1) X7(M1) TE(M2)
100 X3(M1) XD(M2)	100 X5(M1) TE(M2)
500 TD(M2)	500 TE(M2)
Tree 5	**Tree 7**
L=10 X9(M1) XE(M2)	L=5 XA(M1) XF(M2)
20 X9(M1) TF(M2)	10 XA(M1) XF(M2)
50 X9(M1) TF(M2)	
100 X8(M1) TB(M2)	
500 TF(M2)	
Tree 6	**Tree 6**
(L1:L2:L1)	(L1:L2:L1)
5:1:5 XK(M1) XR(M2)	50:1:50 XO(M1) XV(M2)
5:2:5 XK(M1) XR(M2)	50:2:50 XO(M1) XV(M2) TG(2)
5:10:5 XK(M1) XR(M2)	50:10:50 XO(M1) XV(M2) TG(2)
5:20:5 XL(M1) XS(M2)	50:20:50 XP(M1) XW(M2) TG(2)
10:1:10 XL(M1) XS(M2)	100:1:100 XP(M1) XW(M2)
10:2:10 XL(M1) XS(M2)	100:2:100 XP(M1) XW(M2)
10:10:10 XM(M1) XT(M2)	100:10:100 XQ(M1) XX(M2)
10:20:10 XM(M1) XT(M2)	100:20:100 XQ(M1) XX(M2)
25:1:25 XM(M1) XT(M2)	
25:2:25 XN(M1) XU(M2)	
25:10:25 XN(M1) XU(M2)	
25:20:25 XN(M1) XU(M2)	

Width-transition Structures:
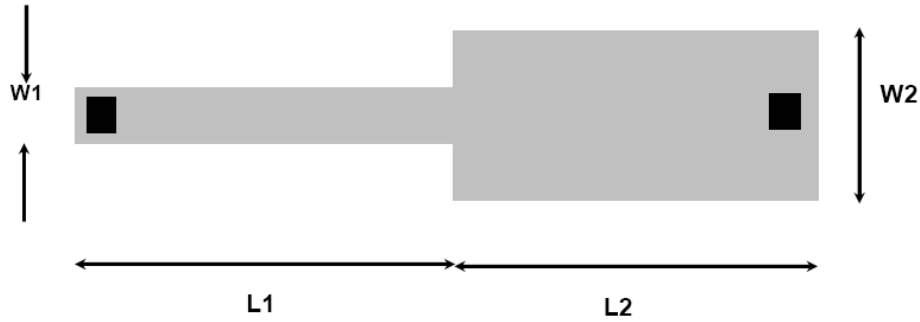
Figure A.6 Width-transition structure identifier.

Table A.3 Width-transition structures on the International Sematech 465AZ mask according to the identifier shown in Figure A.6. The alpha-numeric designation corresponds to the bond pad lane in the die. All width-transition structures are in the M2 level. The units are in μm.

|			
TK (M2)	(left top) L1=20, W1=0.15 L2=280, W2=0.3	(middle top) L1=150, W1=0.15 L2=150, W2=0.3	(right top) L1=20, W1=0.15 L2=280, W2=2.5
	(left bottom) L1=10, W1=0.15 L2=290, W2=0.3	(middle bottom) L1=280, W1=0.15 L2=20, W2=0.3	(right bottom) L1=10, W1=0.15 L2=290, W2=2.5
TL (M2)	(left top) L1=20, W1=0.15 L2=280, W2=1.4	(middle top) L1=150, W1=0.15 L2=150, W2=1.4	(right top) L1=50, W1=0.15 L2=250, W2=0.30
	(left bottom) L1=10, W1=0.15 L2=290, W2=1.4	(middle bottom) L1=50, W1=0.15 L2=250, W2=1.4	(right bottom) L1=280, W1=0.15 L2=20, W2=1.4

Serpentine Structures:
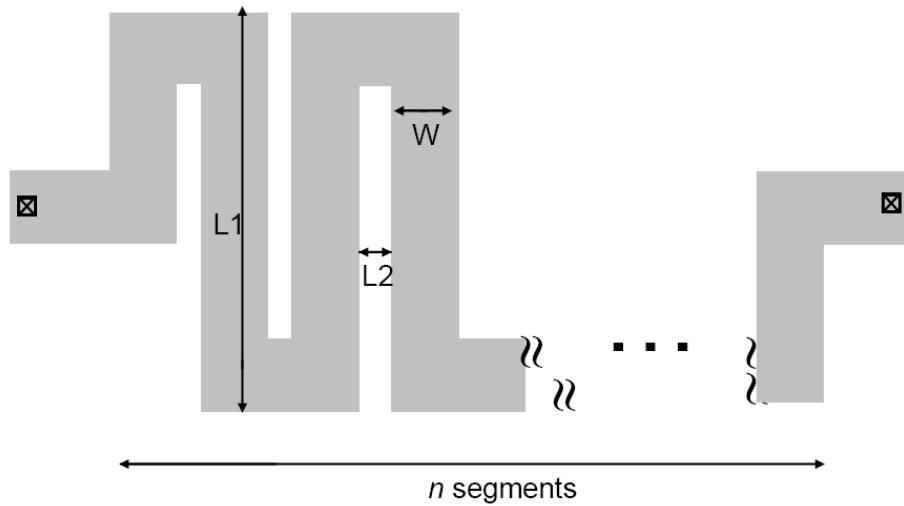
Figure A.7 Serpentine structure identifier.

Table A.4 Serpentine structures on the International Sematech 465AZ mask according to the identifier shown in Figure A.7. The alpha-numeric designation corresponds to the bond pad lane in the die. All serpentine structures are in the M2 level. The units are μm.

XG	L1=L2=60, W=0.15, n=25 (left top), 18 (left bottom), 13 (right)
XH	L1=L2=60, W=1.25, n=25 (left top), 18 (left bottom), 13 (right)
XI	L1=L2=60, W=2.5, n=25 (left top), 18 (left bottom), 13 (right)
XJ	n=25, L1=60 L2=30, W=0.15 (left top), L2=30, W=2.5 (middle top), L2=15, W=0.15 (right top), L2=30, W=1.25 (left bottom), L2=15, W=1.25 (middle bottom), L2=15, W=2.5 (right bottom)

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