Low Threshold Vertical Cavity Surface Emitting Lasers Integrated onto Si-CMOS ICs Using Novel Hybrid Assembly Techniques

by

James Michael Perkins

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of

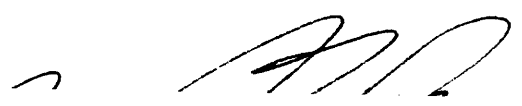
Doctorate of Philosophy in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

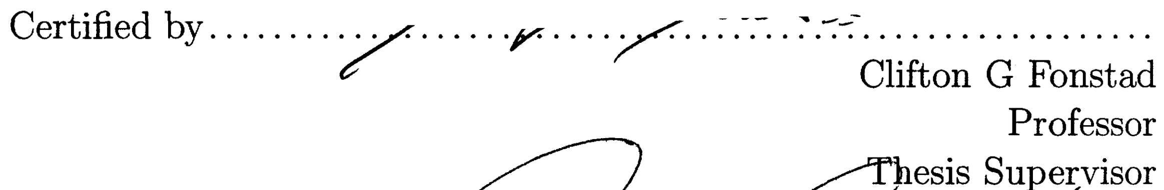
August 2007
[September 2007]

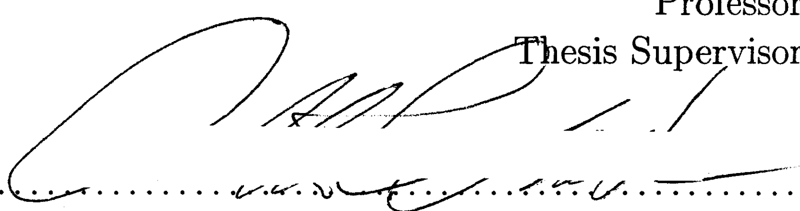
© Massachusetts Institute of Technology 2007. All rights reserved.



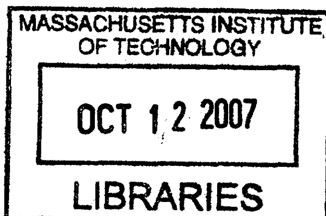
Author ....
Department of Electrical Engineering and Computer Science
August 31, 2007

Certified by ....
Clifton G Fonstad
Professor
Thesis Supervisor





Accepted by ....
Arthur C. Smith
Chairman, Department Committee on Graduate Students


MASSACHUSETTS INSTITUTE OF TECHNOLOGY
OCT 1 2 2007
LIBRARIES

ARCHIVES

Low Threshold Vertical Cavity Surface Emitting Lasers Integrated onto Si-CMOS ICs Using Novel Hybrid Assembly Techniques

by

James Michael Perkins

Submitted to the Department of Electrical Engineering and Computer Science
on August 31, 2007, in partial fulfillment of the
requirements for the degree of
Doctorate of Philosophy in Electrical Engineering

Abstract

A new heterogeneous integration technique has been developed and demonstrated to integrate vertical cavity surface emitting lasers (VCSELs) on silicon CMOS integrated circuits for optical interconnect applications. Individual oxide-apertured 850 nm AlGaAs VCSEL micro-devices discs, 8 μm tall and 55 μm in diameter (pills), have been both bonded and electrically contacted within the dielectric stack of a commercially-fabricated silicon integrated circuit. To accomplish this, fully processed VCSEL device pills are assembled within dielectric recesses using a vacuum pick up tool, and solder bonded in place using a method developed at M.I.T.. VCSELs device characteristic show threshold currents of 1 to 2.5 mA and thermal impedances as low as 1.6 $^oC/mW$, similar to native substrate device impedances. This technique intimately connects devices within the dielectric stack, allowing for size independent, wafer scale monolithic processing of heterogeneous circuits. The size and placement of these devices prevent the stress build up that occurs in growth on non-native substrates due to thermal expansion mismatches. These same devices can be used in more parallel assembly techniques such as fluidic self-assembly and magnetically-assisted statistical assembly.

Thermal modeling of these devices has also been preformed, investigating the impact of integration on VCSEL device operation. The results show potential thermal impedance improvements for both single and arrayed devices due to integration on silicon. This model also investigates the impact of integration on a dielectric stack, as well as the impact of the current aperture of the VCSEL device.

This work also investigated the forces associated with magnetically-assisted statistical assembly. A cantilever measurement tool was fabricated and utilized to measure the stiction force on patterned samarium cobalt thin films. The measurements revealed a force range that agreed with modeling results from previous work, while also showing the variation in force due to non-ideal films.

Thesis Supervisor: Clifton G Fonstad
Title: Professor

Acknowledgments

This is the acknowledgements section. You should replace this with your own acknowledgements.

Words to be headed. I stood there fatigued staring at my thesis believing beneath those hard cardboard covers lay hundreds of typos, suggesting I had failed at my final task. And if that was all that bothered me, nothing was new; nothing had change, and that itself would be comforting. But there was something was amiss. I to attributed this unease to my new title of shiftless vagabond, with only friends' couches to call home. But no, this was not the realization. The unease could have been the remaining jittery fatigue from the 30-hour day, or my near break down in public when the thesis printer refused to print this document; you now have the privilege of reading. The above words then rattled from my skull down to my stomach. I failed to write this page, my note to the ether, my chance to be a published writer.

I'd like to thank my thesis advisor Professor Fonstad for his help, mentorship, encouragement, and advice throughout my years at M.I.T., having a seemingly unending belief in my abilities. I'd also like to thank Prof. Bulovic for his friendship and mentorship. He always had a smile and several words encouragement, and his help with my academic growth and sanity has been truly immeasurable. I'd like to thank professor Kolodziejski for being on my thesis committee and helping to refine the work presented. I'd also like to thanks her for the use of the oxidation chamber, without which this research would be impossible. I would also like to thank Gale Petrich for his invaluable help with the VCSEL oxidation results.

I like to thank the members of the Fonstad group past and present. I'd like to thank Henry for his advise throughout the process for his guidance and his seemingly unlimited knowledge. I'd like to thank Joe for his friendship. I would also like to thank him for being a good lifting partner, when he actually went to the Gym, and thank him for his collaboration on many of my projects at M.I.T. I would like to thank Ed for being a great office mate, and for showing me the ropes in the lab and starting me on my fitness kick. I would like to thank Wojciech for his crazy Canadian

advice and opinions. Shelia, thanks for your encouragement, and your office coffee breaks. Mindy, thanks for putting up with me and Joe, and the bonding work you did enable this project to be feasible. I'd also like to thank the rest of the crew Shaya, Vivian, and Diana.

I would like to thank Seth and Connor for being great friends and helping me get through this process. Of course, I'd like to thank Jen for being Jen. Also Debbie, Alexi, Leeann, John Ho, Jakov, and the whole Bulovic crew for including me in the Bulovic fun. I'll try to live up to my title as the Bulovic group mascot. Oh, and I'd like to thank Ivan "Drago" for his Brewer perspective, his unending knowledge of warcraft, and his opinions on everything. I'd also like to thank my IM tennis, volleyball, and softball teammates.

I'd like to thank Kurt Broderick for all his help and technical expertise. I will miss the banter and the fun in EML.

I like to mention my friends Tom, George, Sang, Kate and all the others that I mentioned before and go unmentioned, for help making this experience fun-filled at times, and bearable at others. I'd also like to thank Dr. Christine McElroy for her advice over the past five years.

Lastly I like to thank my family for their support in getting me this far. Their love and encouragement has been a great source of energy, that has helped me become the person I am today.

Contents

1 Introduction **23**

1.1 Thesis Overview 24

1.2 Motivation for Optoelectronic Integration 25

1.3 Integration Obstacles 27

1.4 Integration Techniques 28

2 Assembly Integration **33**

2.1 Micro-scale Pick and Place Assembly (MAPA) 34

2.2 Fluidic Assembly Techniques 35

2.2.1 Simple Fluidic Self-Assembly 35

2.2.2 Electric Field Directed Assembly 36

2.2.3 Capillary Force Assembly 36

2.3 Magnetically-Assisted Statistical Assembly 37

2.3.1 MASA 37

2.3.2 Advantages of MASA 39

2.3.3 MASA Theory 40

2.4 Pill Bonding 42

3 Magnetic Measurements **45**

3.1 Cantilever Design 46

3.2 Cantilever Simulation 48

3.3 Cantilever Fabrication 50

3.3.1 Metalization 52

3.3.2 Backside Window 53
3.3.3 Semiconductor Etch 55
3.3.4 Selective Oxide Vapor Etch Trials 56
3.4 Cantilever Measurements 57
3.4.1 Spring Constant Measurement 58
3.4.2 Magnetic Film Measurements 61
3.5 Future Work 64

4 VCSEL Pill Development 65

4.1 Procedure 65
4.2 VCSEL Growth Material 66
4.3 Pillar Etch Techniques 68
4.3.1 Two Tier Mesa Etch 70
4.3.2 Single Tier Mesa Etch 70
4.4 Aperture Oxidation 73
4.4.1 Oxidation Theory and Practice 74
4.4.2 Oxidation Set Up 76
4.4.3 Oxidation Trials 80
4.5 Metal Deposition and Patterning 82
4.6 Pill Release and Collection 83
4.7 Backside Metalization 85
4.8 WaferBOND^{tm} Testing and Results 88
4.8.1 Backside Metalization using WaferBOND^{tm} 94
4.8.2 WaferBOND^{tm} Polymer Cleaning 94
4.9 Clumping 95
4.10 VCSEL Pill Results 96
4.11 Pill Processing Improvements 99

5 Device Integration Implementation 101

5.1 Recesses on Integrated Circuits 101
5.2 Device Assembly using Pick and Place 104

5.2.1 Pick and Place Apparatus 105
5.2.2 Pick and Place Assembly 107
5.3 Bonding 109
5.3.1 Bonding Apparatus 110
5.3.2 Bonding Experiments 114
5.3.3 Bonding Improvements 116
5.4 Post Integration Processing 118
5.5 Post Integration Processing Results 123
5.5.1 Low Temperature Dielectric 123
5.5.2 Metal deposition 124
5.5.3 AuSn Bonded Devices 125
5.5.4 AuCr Top Contact Results 128

6 VCSEL Micro-pill Electrical and Optical Characteristics 129
6.1 Measurement Apparatus 129
6.2 Early Devices 130
6.3 Two Tier Devices 132
6.4 Single Tier Devices 137
6.5 Transistor Driven Devices 141

7 VCSEL Heating Simulations 149
7.1 Simple Thermodynamics Model 151
7.2 Gauss-Seidel Iteration 152
7.2.1 The Model 153
7.2.2 Thermal Analysis of Aperture Dependence 154
7.2.3 Thermal Simulation of Integrated Devices 158
7.2.4 Integration on Oxide films Simulations 160
7.3 Thermal Impedance Measurement 161
7.4 Experimental Thermal Impedance Results 165
7.4.1 Measured Aperture Dependence 165
7.4.2 Oxide Dependence 166

7.4.3 Bonded Interface Dependence 169
7.4.4 Summary of Results 170

8 Conclusion **177**
8.1 Summary of Results 178
8.2 Future Work 180

A Thermal C++ Code **183**

B Recipes **201**

C Single-tier VCSEL Process Flow **205**

D Cantilever Process Flow **207**

List of Figures

1-1 Cartoon depicting a single tier device pill and a two tier device pill, with approximate dimensions 24

1-2 Schematic in which pill VCSELs are integrated into recesses on silicon ICs. 24

1-3 Cartoon of multichip module showing the ability to communicate interchip and intrachip with both electrical and optical signals. Optical signals are represented by arrows. 25

1-4 Free-space optical interconnect 26

1-5 Epitaxy on electronics: growth is preformed directly within a silicon IC recess. 27

1-6 Left: Device chip being handled for flip chip bonding. Right: Micrograph of a 16X16 array VCSELs. 29

1-7 Illustration of aligned pillar bonding. 30

1-8 Device assembly of recesses on target substrates. 31

2-1 Left: Diagram of the pick and place technique. Right: Micrograph of an integrated inplane device on a silicon substrate 34

2-2 Left: Cartoon depicting fluidic assembly of silicon trapezoids. Right: LED devices assembled in a study at MIT by Joe Rumpler and James Perkins 36

2-3 A cartoon illustrating a two-tiered VCSEL pill. The mirror layers, active region, and laser cavity are identified. 38

2-4 Schematic detailing the retention force parameters. In equation 2.1, d is the thickness of the hard magnetic material, g is the distance between the recess bottom and the magnetic thin film on the pill, and t is the thickness of the magnetic thin film on the pill. 41

2-5 Calculated decay rate of the magnetic force for different period stripe patterns. 41

3-1 Schematic showing the dimensions of the designed cantilevers. 46

3-2 100 X 100 μm cantilever head with 200 nm thick Ni layer covered by gold 47

3-3 Schematic of the cantilever simplified as parallel plate capacitor on spring. A is the area of the capacitive structure, V is the voltage applied across the structure, K is the spring constant, and g_o is the initial gap distance (i.e. with V=0) 49

3-4 Schematic of the fabrication steps for the cantilever device. A) Head metal is deposited. B) Substrate window is etched. C) Oxide etch stop is removed just below the silicond device membrane. D) Cantilever shape is patterned. E) Silicon is etched into cantilever shape using RIE. 51

3-5 The substrate window etched out, revealing the oxide etch stop layer below. The edges of the patterned window area can be seen in the top left, top right, and bottom right corners. Residual roughened under-etched silicon can be seen outlining the smooth center, comprising the oxide surface. 54

3-6 Released cantilever devices observed through the backside substrate window. The contact supports are seen below the two legs. 55

3-7 Micrograph of fully processed cantilever arms, as seen through the backside window. 57

3-8 Schematic of measurement techniques using these cantilevers. Pull in a) cantilever with initial separation of 15 μm. b) Voltage measured when cantilever pulls in during voltage potential ramp. Pull up c) Cantilever head is placed on the surface of the sample. d) Cantilever is slowly pulled up, with stiction force keeping the head down. e) The cantilever pulls up because the due to bending of the cantilever overcomes the stiction force, resulting in a 15 μm separation between the head and the surface of the sample. 58

3-9 Cantilever pull down measurement setup. One probe contacts and actuates the cantilever devices, while the second probe contacts the aluminum layer. An oxide layer is situated between the cantilever and the aluminum layer to prevent electrical conduction through cantilever legs, which could damage the cantilever device 59

3-10 Modeled cantilever spring constants as a function of separation along with measured data from device heads. 60

3-11 Micrograph of a cantilever above a magnetic substrate. The two squares in the background are patterned samarium cobalt.(a) The cantilever device in its full down position. (b) The device is sticking with flexed arms. (c) The device shown after stiction force released the cantilever. The device head is no longer within the microscopes depth of field. . 62

3-12 Modeled force measurements as a function of distance from Rumpler et. al. Force data range found in cantilever measurement shown within (separation $\leq$ 1 μm). 63

4-1 A cartoon illustrating a partially-processed two-tiered VCSEL pill after mesa etching and upper ohmic contact formation, and prior to substrate removal and back-side metalization. At this stage the first tests of VCSEL performance can be made. 66

4-2 A schematic depicting the basic processing needed to obtain pill devices: a) AlGaAs growth material (p-type mirror dark, n-type mirror light), b) first tier etch removing p-type mirror material, c) second tier etch removing n-type mirror material and revealing InGaP layer, d) oxide aperture formation, e) n-type and p-type metalization (light circles), f) front surface embedded & handle wafer bond (silicon substrate is dark and embedding polymer is clear), g) substrate removal, h) backside metalization(light regions), i) pill release, j) integration onto integrated circuit. 67

4-3 Etch profile of first tier wet etch showing undercut. The first tier reaches into the n-type layer 69

4-4 Cartoon depicting a single tier device and a two tier device, with approximate dimensions. 69

4-5 Array of single tier etched mesas produced using a hard mask (30-35μm diameter). 71

4-6 Single tier etch with hard mask seen(30-35μm diameter) 71

4-7 Backside of VCSELs showing the bottom of a single tier device. The oval shape of the tier due to non-uniform etching is evident. 72

4-8 A visible ring can appear through the top of the mesa due to etching or oxidation of the $Al_{.92}Ga_{.08}$ layers 73

4-9 Current aperture design 73

4-10 Schematic of wet oxidation process 74

4-11 84 nm thick film oxidation rate a) as a function of temperature b) as a function of Al concentration. 75

4-12 Oxidation rate as a function of layer thickness for $Al_{.98}Ga_{.02}As$. . . . 76

4-13 Schematic of Prof. Kolodziejski's wet oxidation furnace. 78

4-14 Wet Oxidation trials at 440 °C for 2 hours. Cleaved SEM (a), IR imaging (b), and luminescence techniques (c) are used to characterize oxidation. 80

4-15 TLM measurement of P-type and N-type metal stacks used for ohmic metal contacts. The TLMs were not confined but showed the metals had decent contact resistances (p-type: 1.8610-4 ohm-cm^2; n-type: 3.7510-5 ohm-cm^2). The contacts also displayed good ohmic linearity. 83
4-16 Pill release process flow. a) Devices protected in wax and attached to dummy substrate. b) Expose backside of substrate. c) Selectively etch to InGaP layer. d) Selectively remove InGaP layer. e) Dissolve polymer in solvent and store devices in IPA. 84
4-17 Released pills with polymer conglomeration 85
4-18 a) Black wax encases devices and fixes them onto a dummy wafer. b) Native substrate etch back. c) Photo patterning on thin film. d) InGaP wet etch removal. e) metal deposition. f) liftoff. g) pill release. 86
4-19 Pills embedded in black wax with metal on their backside 87
4-20 Semiconductor remain after InGaP etch, due to unetched GaAs during tier etch. 88
4-21 Black wax burnt residue producing a carbonized connective film between devices. 88
4-22 Pills Surrounded by WaferBOND^{tm}, with intermittent bubbles. 90
4-23 Schematic of Bonding chamber with pump stage 91
4-24 micropraphs of fissures in the WaferBOND^{tm}. Over etch pills are seen, and misalignment developed 92
4-25 GaAs remaining after backside InGaP etch. This thin layer remains after being unetched during the tier etch. 93
4-26 LI curve of two tier VCSEL integrated on Si with threshold currents of 1ma. 96
4-27 LI curve of single tier VCSEL integrated on chip with threshold current of 2 ma. 98

5-1 Etched well in an IC down to an aluminum pad using SF_6 and Silox Vapox. 102

5-2 Silox Vapox can remove the last remained of material. Above are the last stage of recess opening. Color changes until etch is stopped just above the Al layer, seen in above figure. 103
5-3 Brown film Silox vapox etch stops on. open recesses, Al layer revealed. 103
5-4 500 nm of indium on aluminum within the chip recess. 103
5-5 Schematic of recess dimensions 104
5-6 Pick and place apparatus, showing microscope, probe tip, wafer chuck, tip manipulator, and vacuum line. 105
5-7 Schematic and picture of pick and place setup. The micro-pipette, vacuum lines,and micro-manipulator are shown 106
5-8 Bonding Force 109
5-9 Bonding chamber 110
5-10 Picture showing inner chamber of bonding apparatus with thermal polymer cover. 111
5-11 GaAs pills bonded in oxide recesses using pressure bonding system. . 116
5-12 Schematic of post integration process flow. (a) Device is bonded within the recess. (b) Spin-on dielectric over coating planarizes recess. (c) Vias are etched through the spin on dielectric. (d) Vias are etched through the IC dielectric. (e)Metal is deposited and patterned, connecting the device contacts to the chip. 118
5-13 Lift off Al via mask revealing the yellow contact pads bellow. Circular center vias are also made and need to be covered during etch steps. . 121
5-14 Via metal on AuSn substrate (S-Au-500). Contours of dielectric show underlying metal layers. Etched out side vias to contacts 126
5-15 Top contact, connecting the P-side of the VCSEL to the side contact of the S-Au-500 chip. 127
5-16 Resistance from contact pad to top of VCSEL Pill 128

6-1 Electrical probe station with affixed silicon photodetector, and HP4145B 131

6-2 Spectral light output of non-current confined device at 10 ma and 25 ma input current. Spectral width is indicative of a LED device with spectral filter, ... 132
6-3 Unapertured device on its native substrate with a 35 μm diameter, and a 25 ma threshold current. 133
6-4 LI curves of several nominally identical devices on native substrates displaying various threshold currents. Each are apertured using oxidation, and display relatively high threshold currents 134
6-5 LI curve of integrated on Si VCSELS with threshold currents of 1ma. 135
6-6 LI curves of two VCSELS, one on a native substrate and the second bonded to a Si substrate. Both show current thresholds of 2.5 ma . . 136
6-7 LI curves for fully integrated Device 11. The P-type contact is probed using both the top contact and side contact. 138
6-8 Array of devices showing gold connecting top contact. 138
6-9 LI curves for fully integrated Device 21. The P-type contact is probed using both the top contact and side contact. 140
6-10 Transistors on chip, designed to power the VCSEL devices. Design by Simpkins, made by MOSIS. on the right a diagram showing the drive transistor diode circuit layout. 141
6-11 Transistors on chip after processing, Vdd = 5 volts. Design by Simpkins, made by MOSIS 142
6-12 Two tier VCSEL lasers driven by the gate of on chip transistors. Devices bonded using thin Au/Sn on Chip T-Au-100. The devices shown have their top contact probed and are not fully integrated 143
6-13 LI curves of Two tier VCSEL lasers driven by the gate of on chip transistors. Devices were bonded using 400 nm of indium on Chip T-In-400. The devices shown have their top contact probed 144
6-14 Integrated VCSEL lasers bonded using 400 nm of In on Sample S-In-400b. The devices shown has been probed from the top device contact to bottom aluminum pad. 145

6-15 Fully integrated VCSEL lasers (Device 11) driven by the gate of on chip transistors. Devices were bonded using 500 nm of Au/Sn. The device shown has been probed from the side bond pad of the IC. . . . 146

6-16 Fully integrated VCSEL lasers (device 21) driven by the gate of on chip transistors. Devices were bonded using 500 nm of Au/Sn. The device shown have been probed from the side bond pad of the IC. 147

7-1 LI curve of integrated on Si VCSELS with threshold currents of 1ma. 150

7-2 Schematic of the simple model for thermal behavior of a VCSEL device 151

7-3 (a) A schematic of the simulation space, showing specific aspects of assumptions inherent in the radial thermal isolation boundary, the changeable surface contact layer, and the isotherm 65 μm below the surface. (b) Resulting simulated temperature gradients within of 10 μm diameter aperture with a 50 μm radial isolation for 1 mW power dissipation at the aperture. The peak temperature of 1.6 ^oC seen at the aperture. The thermal isolation boundary is seen as a sudden dip in temperature, outlining the pill and substrate. 155

7-4 Thermal impedance and threshold current dependence on aperture size. 156

7-5 Operating temperature of devices as a function of aperture diameter both at threshold, and at 10 ma current bias 157

7-6 (a) Device on its native substrate,(b) Device bonded on Si,(c) Device bonded on oxide,(d) Device freed and unbonded 158

7-7 Thermal impedance as a function of simulation confinement. The results are confirmed by the simple model at large confinement lengths. 160

7-8 Thermal impedance dependence on interface oxide layer thickness . . 161

7-9 Peak emission shift of a bonded device on a heated substrate, biased at 4 mA 163

7-10 Normalized output frequency of a device driven with increasing current. A shift of 10 nm is observed 164

7-11 Modeled impact of device threshold current on thermal impedance. The measured data confirms the modeled trend. An exponential fit to the modeled data is also shown as a continuous line. 166

7-12 Measured devices confirm the affects of oxide film on thermal impedance. 167

7-13 LI curves of the devices on the oxide study. High threshold devices were chosen for Figure 7-12 to minimize aperture dominance of the thermal impedance. Top: devices on 5 μm oxide. Bottom: devices on 3 μm oxide. 168

7-14 LI curves of two 2 ma threshold VCSELS, one on a native substrate, one integrated using 30 nm AuSN 169

7-15 (a) LI curves of a device before and after indium bonding. Drive current range is significantly increased due to bonding. (b) Power vs. peak emission data from device before and after bonding. The increase in slope indicates a decrease in thermal impedance. 171

7-16 (a) an increase in threshold current is seen in the LI curve after the device is bonded. (b) The threshold current is returned to its previous state by heating the device, suggesting the DBR is out of tune for low temperature operation. 172

7-17 (a) Thermal impedance data from a variety of devices integrated differently. A larger slope suggest a smaller thermal impedance. (b) Schematic depicting device integration states 173

7-18 Thermal impedance data from 3 devices integrated onto ICs , demonstrating the input power attainable from these devices. Device 33 was a 2 tier device, while devices 11 and 21 were single tier fully integrated devices. 174

List of Tables

2.1 Force term definitions 40

3.1 Spring Constant 61

5.1 Bonding experiment samples 115

5.2 Bonding Results 117

6.1 Samples used in characterization experiments 130

7.1 Thermal Impedance Results 175

B.1 NR7 3000, 3 micron negative resist 201

B.2 NR7 1000, 1 micron negative resist 201

B.3 OCG, 1 micron positive resist 201

B.4 Thick resist, 5 micron positive resist 202

B.5 WaferBOND, 15 microns bonding agent 202

B.6 BCB cyclotene 3000 series, 1.5 microns BCB 202

B.7 AlGaAs wet etch 202

B.8 InGaP wet etch 202

B.9 Silicon wet etch 202

B.10 SiO_2 BOE wet etch 203

B.11 PECVD oxide 203

B.12 PECVD nitride 203

B.13 Si dioxide etch 203

B.14 Silicon etch (fast with undercut) 203

B.15 Silicon etch (minimal undercut) 203
B.16 BCB, minimal undercut 203
B.17 Silicon dioxide etch 204
B.18 GaAs etch (inconsitant, use for small etch depths) 204
B.19 photo etch 204

Chapter 1

Introduction

Opto-electronic devices integrated on silicon integrated circuits have been sought for over 20 years, to enable optical interconnect applications, providing improved data transfer rates in high performance silicon integrated circuit applications. Currently, electrical interconnects use lossy copper lines to provide system buses, on which data is transfered within a chip and between chips. The next generation copper interconnect bus (PCI Express 3) aims at transfer rate of 8 Gbits/sec. Interconnects based on copper interconnects are expected to hit their maximum at around 15 Gbits/sec however. By replacing these lossy electrical copper lines with wave guided optical signals, this roadblock can be avoided. A single vertical cavity surface emitting laser can be used to transmit beyond 8 Gbits/s. By placing these devices in an array, a bus that is significantly faster than current electrical buses can be produced. This study demonstrates new heterogeneous integration techniques that have been developed for these hybrid applications. Using heterogeneous integration techniques, vertical cavity surface emitting lasers (VCSELs) have been fully integrated into standard silicon IC technology.

In this study small AlGaAs VCSEL heterostructure discs referred to as ̈pills ̈(40-90 μm in diameter and 8μm high, shown in Figure 1-1) have been placed within the dielectric stack using pick and place assembly [1], allowing for wafer-size independent, wafer scale, monolithic processing of heterogeneous circuits. The recess integration process is schematically shown in Figure 1-2. The micro-pill devices are processed on

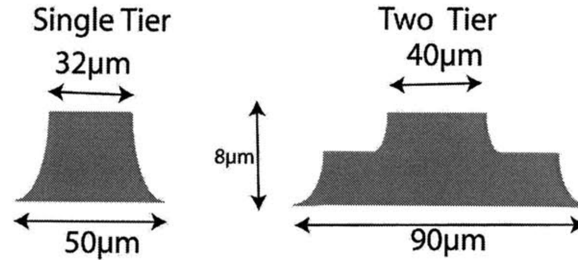


Figure 1-1: Cartoon depicting a single tier device pill and a two tier device pill, with approximate dimensions

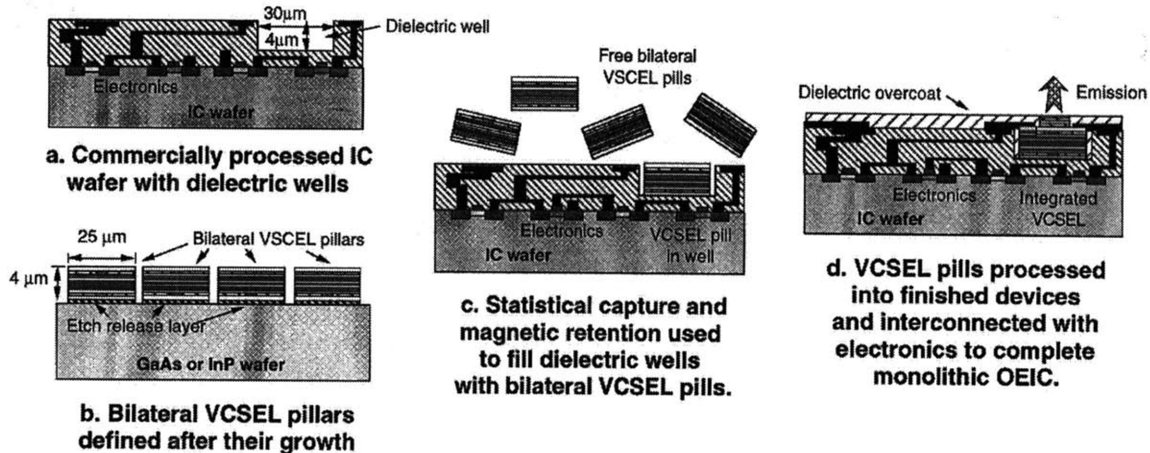


Figure 1-2: Schematic in which pill VCSELs are integrated into recesses on silicon ICs.

their native substrate, then removed from their native substrate. After removal, the micro-pill devices are placed, bonded, and connected to the silicon integrated circuit (IC). The individual optoelectronic devices produced in this work can be used in pick and place assembly or other recess integration techniques such as fluidic self-assembly [2] and magnetically-assisted statistical assembly (MASA [3]), techniques which can assemble hundreds of devices without individual device alignment.

1.1 Thesis Overview

This thesis will begin by motivating and discussing current heterogeneous integration techniques. Chapter 2 will discuss assembly techniques, focusing on pick and place assembly and discussing MASA theory and practice. Chapter 3 will present measurement of the stiction forces used MASA assembly. Chapter 4 discusses the

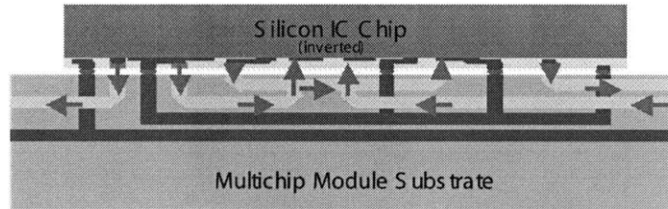


Figure 1-3: Cartoon of multichip module showing the ability to communicate interchip and intrachip with both electrical and optical signals. Optical signals are represented by arrows.

design, fabrication, and properties of the micro-pill VCSEL devices. The electrical and optical device characteristics of the VCSEL micro-pills are presented in Chapter 6. The heating that occurs during operation of integrated VCSELs will be simulated, and experimentally measured thermal impedances of these integrated devices are reported in Chapter 7. Chapter 8 will summarize this work and discuss how to further advance this technology.

1.2 Motivation for Optoelectronic Integration

For most applications silicon CMOS IC technology holds several advantages over III-V IC technologies. Complimentary circuit design, a native oxide (SiO_2), and years of industrial investment and experience provide silicon's advantage in integrated circuit applications. However, III-V direct band gap semiconductor devices are necessary for many optoelectronic applications. Tuning of the elemental composition in III-V materials resulting in adjustments in the energy band of the material provides a large amount of flexibility in these systems, producing tailored light emission and quantum well confinement. Heterogeneous integration of these materials enables flexible, efficient system design, and potentially allows for high speed ICs with fast data links using optical interconnects.

Hybrid chips produced by integrating silicon ICs and III-V optoelectronics can be used to improve the data comunication bandwidth on chip. Optical signals can be used to transmit data via wave-guided light. A single VCSEL can transmit beyond 10 Gbits/sec, while electrical lines have limited bandwidth. Currently parallel opti-

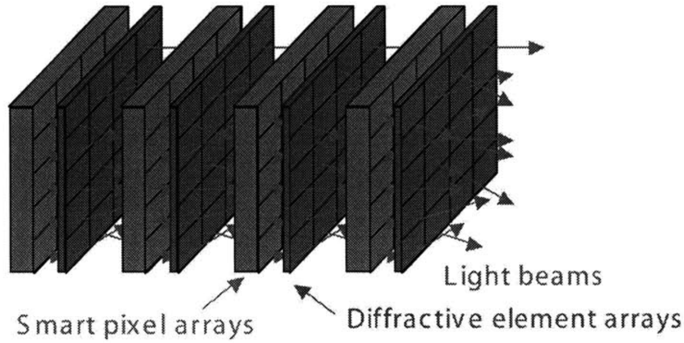


Figure 1-4: Free-space optical interconnect

cal interconnect schemes are being used for rack-to-rack application, providing data transfer rates up to 10 Gb/s, while replacing bulky electrical cables with thin fiber optic cables. IBM is currently investigating on-board interconnects with their Terabus project [4]. The Terabus project places a 4X12 array of VCSELs onto Optocard, which transmits the signals from the VCSELs using waveguides, to allow high speed chip to chip communication. A conceptual cartoon of what a hybrid chip might look like is seen in Figure 1-3. The hybrid chip transmits signals to the board below both optically and electrically. The interconnect board has waveguides directing optical signals to different regions on the same source chip or these optical signals are directed to other chips on the same multichip board. Intel Corporation has also investigated hybrid silicon / III-V technology with their hybrid silicon laser project, work done in conjunction with University of California Santa Barbara[5]. The hybrid silicon laser technology aims to integrate in-plane laser onto a silicon platform, by using an InP optical gain region bonded above a silicon waveguide to pump light into the silicon device.

Hybrid VCSEL IC technology can also be used in free space optical interconnect applications. In one such scheme, depicted in Figure 1-4, several hybrid chips are stacked face to back, with a light steering element between each stacked chip. The left most chip, shown in Figure 1-4, sends a signal to the adjacent chip, which processes the signal information, and optically communicates with the next chip. The research reported within this thesis will implement a hybrid integration technique and demonstrate it by producing a 3X3 array of VCSELs integrated on a Si IC circuit.

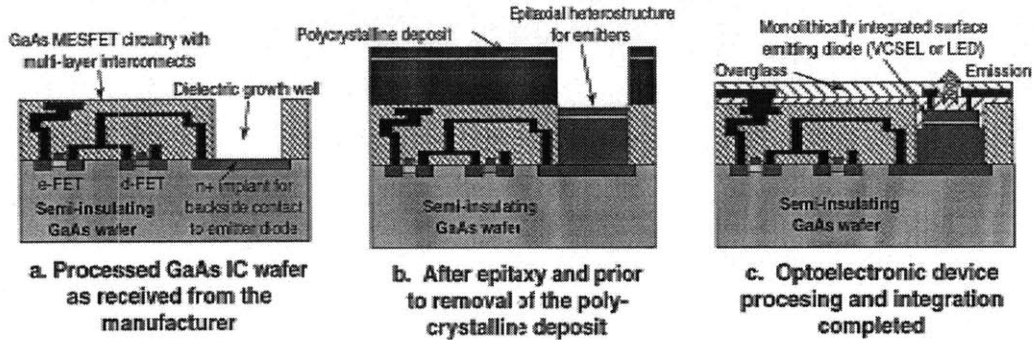


Figure 1-5: Epitaxy on electronics: growth is preformed directly within a silicon IC recess.

The target silicon IC is designed for a free-space optical interconnect application. Specifically, the target CMOS chip was designed for a neural network application by Travis Simpkins (2005 MIT Ph.D. graduate) in his Ph.D. thesis work [6].

1.3 Integration Obstacles

The integration of Si and III-V semiconductors has long been recognized as an important goal. Heterogeneous integration would allow for cheap, low power silicon ICs driving efficient optical devices. Many integration techniques have been researched, including direct MBE growth on Si substrates [7] as seen in Figure 1-5 [8] . There are two main issues with this technique. Although most III-V semiconductors and silicon have compatible crystal structures, the size of their unit cell differs, creating stresses in the grown crystal, ultimately producing defects in the grown material. Such defects limit the optical and electrical characteristics of devices produced. Graded buffers have been used to over-come this problem, however the thermal expansion coefficient mismatch between these materials compounds can become the mains source of defects in grown material and has become an obstacle in III-V Si integration [3]. The difference between the thermal expansion coefficient of GaAs and Si, for example, is more than $4 \cdot 10^{-6}\ ^{o}C^{-1}$. For six-inch wafers, a temperature increase of 100 ^{o}C would result in a difference in diameters of 70 microns [3]. Compounding this issue, growth of III-V materials using MBE techniques is usually done at temperatures well above

550 ^oC. Though high purity, low stress material can be grown on Si at these temperatures, sample cooling produces defects to release the stress build up in the grown material. Even if quality III-V materials can eventually be grown on a Si substrate, further processing must be limited to low temperatures in order to prevent thermal stresses in the material.

1.4 Integration Techniques

Integration techniques that bond two different materials together after processing avoid crystalline mismatch problems by allowing growth to take place on native substrates and at optimal temperatures. After growth, the two different materials can be bonded together and processed further. Flip chip bonding is one such technique. The chips are fully processed and diced separately allowing for CMOS circuitry on one chip and optoelectronic devices on the other. Solder bumps are placed on contact pads of the chips for interconnects. The chips are then aligned and bonded together. This is the industry standard for III-V Si integration. Figure 1-6 [9] shows a die being aligned and integrated. Krishnamoorthy et. al. demonstrated a 16 X 16 array of III-V VCSELs integrated using this technique [9]. The VCSEL devices bonded had bandwidths in excess of 4 Ghz, and thermal impedances of about 1 ^{o}C/mW.

Full wafer bonding integrates two independent preprocessed full wafers [10]. Instead of bonding through metal pads as with flip chip, wafer bonding attaches the two wafers by chemically bonding their surfaces. This process allows integration of full wafers. Wafer bonding studies have been done at MIT, but have shown some limitation [11]. Alignment is necessary and wafer sizes are restricted to those of common III-Vs growth substrates. Good control of surface quality, and roughness is needed for surface bonding to occur, especially with preprocessed wafers. Low temperature bonds are also needed, to avoid thermal expansion problems.

Aligned pillar bonding (APB) [12] uses optoelectronic material that is again grown on a native substrate. The optical device material is etched into pillars, while the silicon ICs have recesses etched into them, providing areas where the III-V devices are

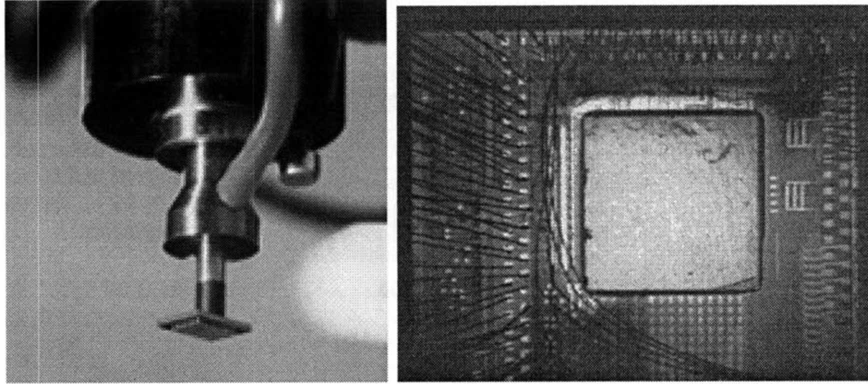


Figure 1-6: Left: Device chip being handled for flip chip bonding. Right: Micrograph of a 16X16 array VCSELs.

to be placed. These pillars are aligned to the recesses and the pillars are bonded into place on the silicon wafer. The optoelectronic substrate is then etched off to produce a silicon IC with III-V optical components. The small size of these pillar components allows for further temperature cycling without defect formation. Figure 1-7 [8] shows the steps needed for aligned pillar bonding. A similar integration technique called epitaxial lift-off (ELO) was used to place VCSEL arrays onto silicon substrates [13]. The VCSEL arrays are bonded to silicon with their native substrate still attached. The integrated devices are then oxidized, which simultaneously produces a current aperture while also freeing the individual devices from their native substrate. Pillar bonding techniques are pseudo-monolithic and allow for integration of complex heterostructures grown on native substrates, however there are still disadvantages. Due to direct wafer-to-wafer bonding, a significant amount of growth material is wasted. This technique also requires both wafers to be the same size and requires meticulous alignment. Furthermore, aligned pillar bonding integrates full device dies or wafers regardless of whether all the devices on the integrated substrate are functioning.

Techniques involving assembly of small individual devices avoid the problems associated with APB, yet use the same general integration principles. In contrast to aligned pillar bonding, the integrated optoelectronic material is fully removed from its native substrate before integration, as shown in Figure 1-8 [8]. Assembly involves integrating small pieces of processed material onto a substrate. Thousands of these pieces must be integrated on a wafer. In order for such a technique to be practical

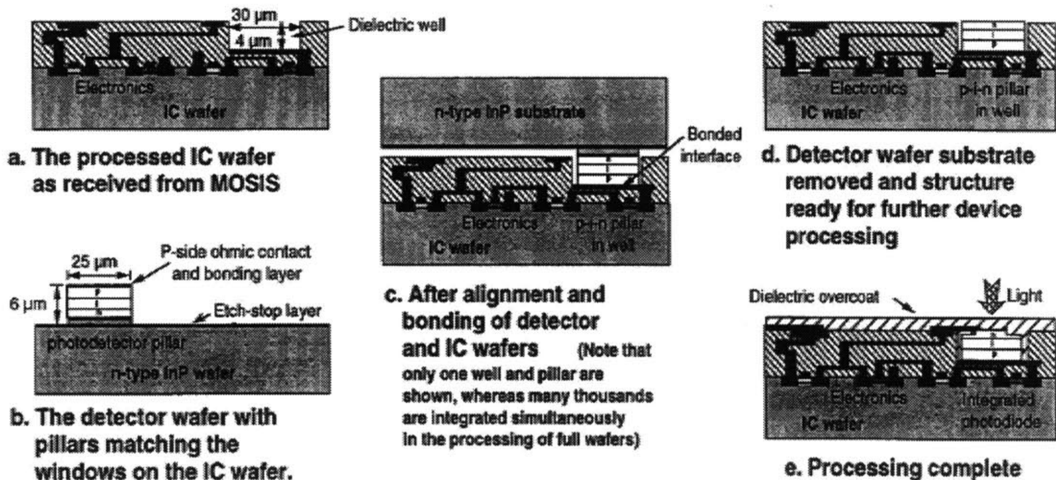


Figure 1-7: Illustration of aligned pillar bonding.

for a large number of devices, individual piece alignment is not an option. There are various assembly techniques for integrating these pieces (whose widths can range from millimeter to microns), some of which will be discussed in Chapter 2. In many techniques, pieces are moved in solution over the target wafer, where they fall into recesses. Recesses can be patterned wherever device structures are needed. The substrate independence of the two material sets allows the use of standard wafer sizes. More efficient use of III-V material can be obtained using assembly techniques, while also avoiding tedious and costly alignment processes, and pre-selection of only working devices for integration. While the concept of integrating individual devices as small as pills has been around for about 15 years, its impact on heterogeneous integration has been relatively limited. With results like those presented in this thesis, and the growing sophistication and needs of the optoelectronic industry, this situation seems poised to change and the impact of micro-scale assembly technique can be expected to increase significantly.

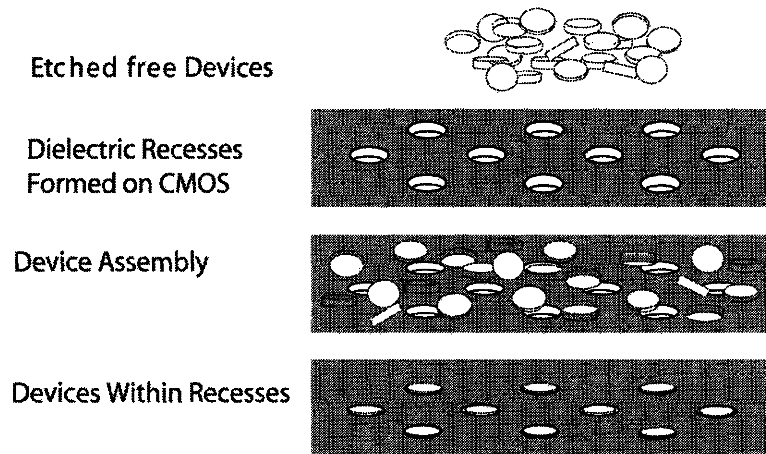


Figure 1-8: Device assembly of recesses on target substrates.

Chapter 2

Assembly Integration

As discussed in Chapter 1 Section 1.4, microscale hybrid device assembly uses small area devices that can be placed and bonded onto substrates for further processing, enabling truly independent material mixing, i.e. heterogeneous integration. The size of these devices can range from microns to millimeters. Each assembly technique varies in their placement procedure.

Using recess assembly techniques like those introduced in this thesis, devices can be selectively placed in recesses within the dielectric stack throughout a processed wafer, while allowing further monolithic post integration processing, allowing array pitch for VCSEL devices to be limited by the size of the device rather than the bonding accuracy and pad size as seen with techniques like flip-chip bonding. Flip-chip bonding requires each device to have its own bond pads on the substrate. These bond pads need to be large for alignment, bonding, and heat dissipation purposes. This increases the area needed per pixel, and decreases the possible density of the array. State-of-the-art flip chip bonding techniques have minimum array pitches of 125 μm. The devices integrated within the recesses, using assembly techniques such as pick and place assembly and MASA, are bonded below the device. The recess integrated devices are connected to the IC using metal lines within the dielectric stack of the IC. The limiting factors for array pitch become device size and thermal constraints due to thermal cross talk, which are dependent on the aperture size of the VCSELs. 55 μm devices have been integrated in the present study, enabling pitch

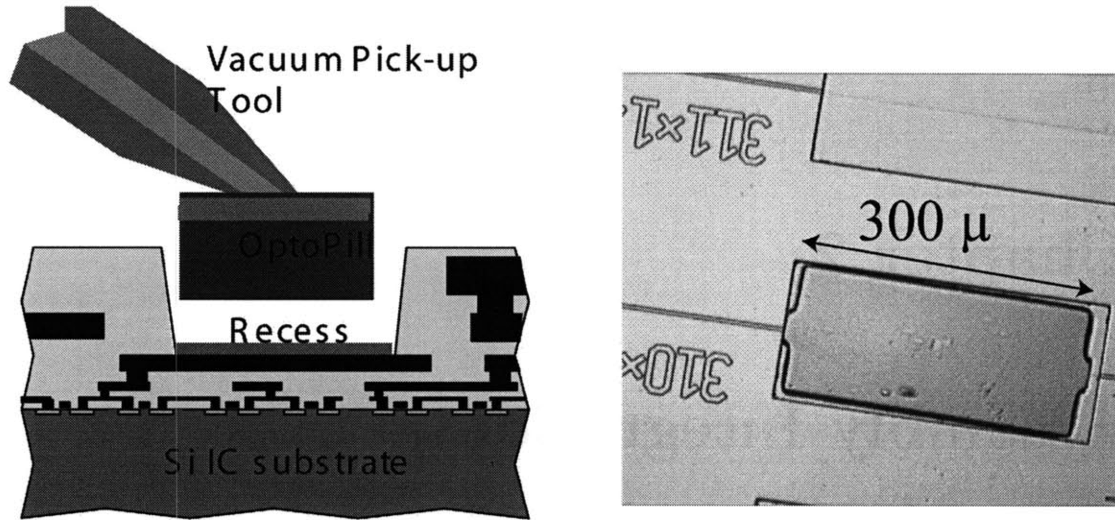


Figure 2-1: Left: Diagram of the pick and place technique. Right: Micrograph of an integrated inplane device on a silicon substrate

arrays on the order of 70 μm. The size of the device are limited by the size of the contact on the top of the device and the aperture size of the VCSEL device.

2.1 Micro-scale Pick and Place Assembly (MAPA)

Micro-scale pick and place assembly is a new technique developed at MIT by Prof. Fonstad and Mindy Teo [1]. MAPA takes optoelectronic pills and individually assembles them. Using a fine micro-pipette each device is picked up via suction and placed in the desired recesses. This technique requires the alignment of each device, but enables reliable, precise, and selective integration. The specifics of the implementation of this technique can be found in Chapter 5 Section 5.2.1. A similar technique was used by S. Daryanani et. al. to place a stand alone VCSEL device with a 7mA threshold on an inverter circuit [14].

A diagram depicting this technique can be found in Figure 2-1. The vacuum micro-pipette has a flat surface with an inner diameter smaller that the pill top. The pipette tip can be maneuvered to place the devices in a IC recess directly on the target bonding film within. Figure 2-1 also shows a large device assembled for in-plane laser studies. These devices can be accurately placed with small tolerances.

2.2 Fluidic Assembly Techniques

Fluidic assembly is a relatively new integration process. Fluidic Self-Assembly (FSA) [2] was first investigated in the mid 90's with other similar techniques soon following. Generic fluidic self-assembly places devices into recess by flowing them within a fluid over the target substrate. Many assembly techniques use fluid flow to direct individual devices to the target substrate, while introducing techniques designed to improve recess-filling probabilities. Recess filling can be increased by introducing attractive forces between the recess and the assembled pieces. The attractive retention force can potentially prevent devices from falling out during further processing steps. Assembled devices are often lost, for example, during removal from solution, and a retaining force has the potential to prevent such losses.

2.2.1 Simple Fluidic Self-Assembly

As stated above fluidic self-assembly, FSA, uses the flow of solution along the surface of the substrate to place individual devices into specific recesses on the Si substrate. A recirculating pump is often used to re-flow the solution and the devices back over the target substrate, reusing devices that were not assembled in the first pass. In the process introduced by Prof. Smith and his group at Berkeley, who invented FSA [2], both the pills and holes are etched into trapezoids, allowing these devices to orient by sliding to the bottom of the holes. This technique has been used for a variety of applications from placing millimeter size chips to 40 μm x 40 μm square optical devices. InGaAs VCSELs have been successfully integrated using FSA [15]. Close to 100 % of the holes are filled using this technique with devices larger than 150 μm in width, however this yield gets worse when used with smaller devices [16, 17]. Figure 2-2 [2] depicts this type of assembly and shows the result of some FSA studies done at MIT by Joe Rumpler and James Perkins.

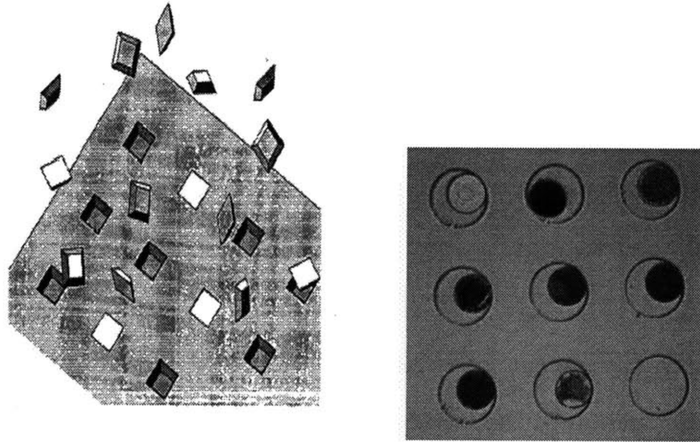


Figure 2-2: Left: Cartoon depicting fluidic assembly of silicon trapezoids. Right: LED devices assembled in a study at MIT by Joe Rumpler and James Perkins

2.2.2 Electric Field Directed Assembly

Electric field directed assembly (EFDA) has been used to improve assembly yields for small devices [18]. In this technique, solution flows to the unoccupied holes using electroosmosis. The holes are negatively biased using contacts on the substrate while an anode is place in solution. A voltage differential across a charged solution produces a flow to each recesses. The devices are dragged along the surface of the substrate to negatively biased holes. Once all holes are filled, the solution is removed. The substrate is then heated to fuse the contacts between the substrate and the placed device. 20 μm InGaAs light emitting diodes have been integrated using this technique. EDFA requires separate biasing wires added to the circuitry for the purpose of assembly, creating added complexity.

2.2.3 Capillary Force Assembly

Capillary force assembly [19] is a relatively new fluidic self-assembly inspired technique in which epoxy is used to selectively attach pieces onto substrates. Self-assembled monolayers (SAM) of thiols attach preferentially to gold. This layer is hydrophobic, allowing epoxy to selectively stick to these areas within an aqueous solution. When pieces with this same hydrophobic SAM flowed in solution across the

target substrate, they stick and align to the epoxy due to the capillary forces at the interface. The epoxy is then hardened, affixing the pieces to the substrate permanently. U. Srinivasan et. al. attached Si micro-mirrors 450 microns in diamter to a substrate using this method [19], producing good fill rates.

2.3 Magnetically-Assisted Statistical Assembly

Magnetically-assisted statistical assembly (MASA) [3, 20] is a technique similar to the above self-assembly techniques, but provides better scaling and retention properties. Specifically a magnetic retention force is used to keep properly oriented devices within target recesses. MASA uses a spatially varying magnetic field is used to induce a force on a soft magnetic film included on the assembled device. This section will discuss the details of this assembly technique, while Chapter 3 will discuss work done to measure the interaction between these spatially varying fields and the assembled devices.

2.3.1 MASA

In this technique, individual optical devices are etched into cylindrical pills. These pills are processed with a soft magnetic film, such as nickel, on the bottom of the device. Recesses are etched into the target substrate. These recesses act as the target location for the pill devices. At the bottom of these recesses, strips of a high coercivity magnetic film are patterned. The patterned magnetic film creates an exponentially decreasing short-range magnetic field that will attract the soft magnetic pill layer, retaining the entire pill in these wells [3]. During the assembly process a high density of pills is introduced to the surface of the substrate, producing a high probability of each hole being filled. As with most fluidic techniques, a vibrating stage can aid in the movement of the pills as they flow across the substrate. To ensure this pill density, the pills out-number the holes by an order of magnitude or more. Pills with their magnetic layer away from the substrate do not experience the same attractive force as those with metal layer touching the bottom of the recess, enabling selectivity for proper orientation. Once the pills are in place, the soft magnetic metal layer acts

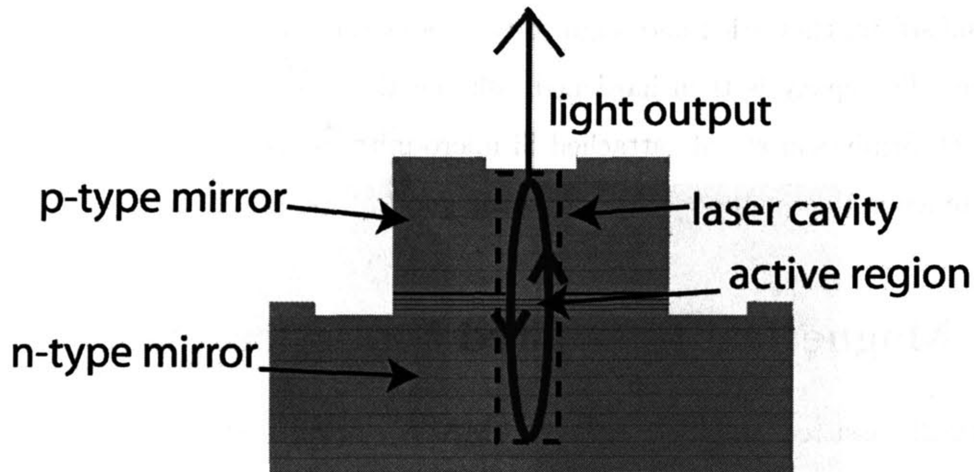


Figure 2-3: A cartoon illustrating a two-tiered VCSEL pill. The mirror layers, active region, and laser cavity are identified.

as a contact for the backside of the device. The devices are then bonded in place and a polymer fills the residual empty area of the well. Once the recesses are filled, processing of the substrate can proceed normally.

Pill devices are not restricted to one particular kind of device or material. Recess integration technique has the potential to be used with a wide variety of devices including optoelectronics, heterostructure electronics, and micro-electro-mechanical systems (MEMS) devices. In this study a VCSEL structure was used for integration. Figure 2-3 diagrams the heterostructure of the two tier VCSEL pill developed. A VCSEL laser is produced by growing Bragg refracting mirrors above and below a quantum well active region in which the light is produced. The VCSEL mirrors create the resonant cavity for the laser. The top mirror allows a small amount of light transmission, creating a device that emits in the out-of-plane direction, with respect to the growth substrate. In this work, an oxide aperture was used to confine the current in the lateral direction. An InGaP layer was used as an etch stop layer at the bottom of the growth stack, allowing the removal of the device from the host substrate. Further discussion of the device materials and their processing can be found ins Chapter 4.

2.3.2 Advantages of MASA

There are several integration advantages that make MASA an interesting alternative to current techniques. The following is a summary of these advantages.

1. The short range magnetic field produces an attracting and retaining force during assembly, enabling a higher yield of filled wells compared to simple fluidic assembly

2. Normal device patterning and processing can be done after the pills are in place, making the process pseudo-monolithic.

3. The heights of the pills are made co-planar with that of the surrounding surface of the substrate, allowing for further high resolution photolithographic processing after assembly.

4. Assembly can be used to place pill devices above existing substrate devices, allowing for 3-D circuit capability.

5. MASA can be repeated, allowing for the integration of multiple device types.

6. Pill materials and device functionality can be tested prior to integration, ensuring the placement of working devices.

7. Cylindrical pills are highly symmetric and can be produced in many material systems.

8. The process is compatible with full-wafer processing technology and can be done with multiple wafers at a time, achieving economics of scale similar to monolithic integration.

9. Substrate wafer size is not limited by the wafer size of the pill material, allowing the use of standard wafer sizes.

10. Pills are etched out in a close packed array, ensuring efficient use of grown material.

11. Pill material can be grown under optimum conditions.

2.3.3 MASA Theory

Calculations have been done to determine the forces associated with the magnetic field produced during magnetic assembly [20, 21]. Equation 2.1 shows the equation relating the force per area to the parameters of the pills and the magnetic substrate. Since the sum falls off as $1/n^2$ only the n=1 term is important. The simplified relationship is described in Equation 2.3, with the quantities defined in Table 2.1.

$$F_z/Area = \frac{\mu_o M_r^2}{\pi^2} \sum_{n_{odd}}^{\infty} \{ \frac{1}{n^2} [(e^{kd} - 1)^2 e^{-2kd}] [\frac{(e^{2kd} - 1)(\mu_s^2 - 1)}{e^{2kt}(\mu_s + 1)^2 - (\mu_s - 1)^2}] [e^{-2kg}] \} \quad (2.1)$$

where

$$k = \frac{2n\pi}{L} \quad (2.2)$$

$$F_z/Area = \frac{\mu_o M_r^2}{\pi^2} [(e^{\frac{2\pi d}{L}} - 1)^2 e^{-\frac{4\pi d}{L}}] [\frac{(e^{\frac{4\pi d}{L}} - 1)(\mu_s^2 - 1)}{e^{\frac{4\pi t}{L}}(\mu_s + 1)^2 - (\mu_s - 1)^2}] [e^{-\frac{4\pi g}{L}}] \quad (2.3)$$

Table 2.1: Force term definitions

Term	Definition
μ_o	permeability of free space
M_r	Magnetization of hard film in recess
d	hard magnetic material thickness
L	period of stripe pattern
μ_s	magnetic permeability of magnetic film on pill
g	gap between pill and recess
t	thickness of magnetic material on pill

The formula given in Equation 2.1 analyzes the magnetic attractive force of a striped pattern. Figure 2-4 schematically shows how these parameters relate to the dimensions in the system. The formula, Equation 2.3 can be broken down into four parts. The first term is dependent on the magnetic saturation of the permanent magnet. The second term shows the dependence on the ratio of hard magnetic film

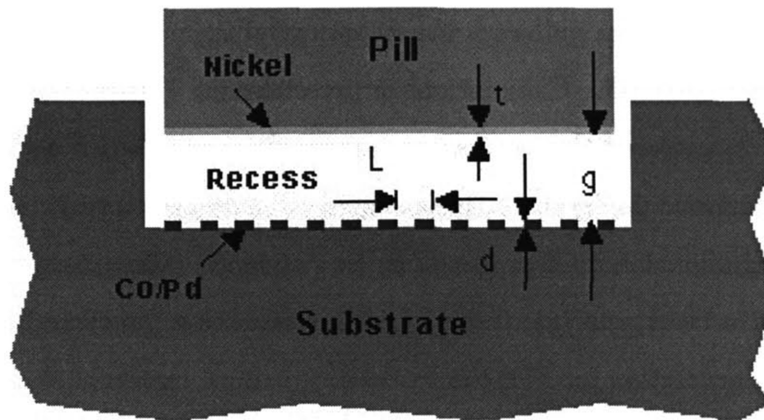


Figure 2-4: Schematic detailing the retention force parameters. In equation 2.1, d is the thickness of the hard magnetic material, g is the distance between the recess bottom and the magnetic thin film on the pill, and t is the thickness of the magnetic thin film on the pill.

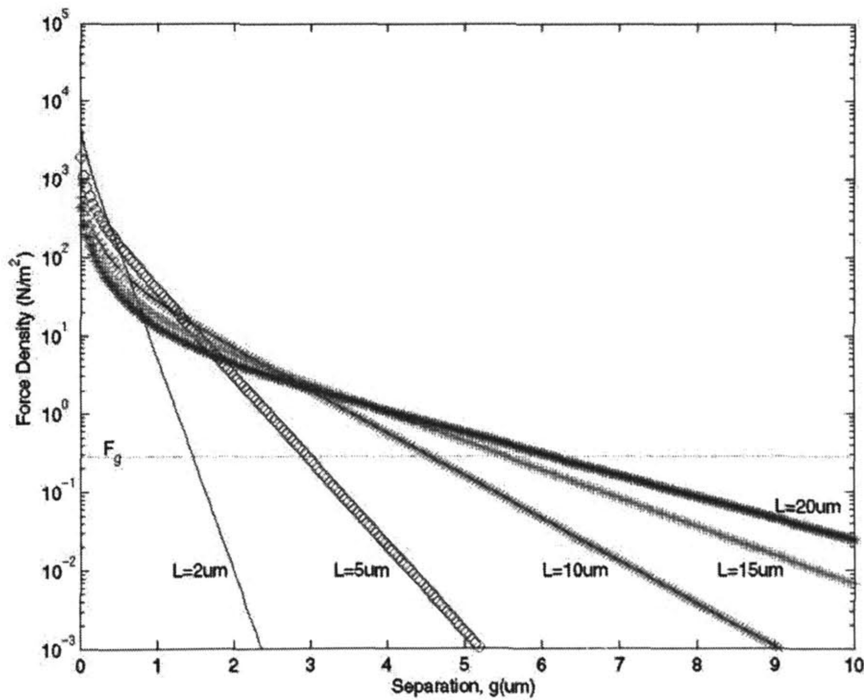


Figure 2-5: Calculated decay rate of the magnetic force for different period stripe patterns.

thickness and its lithography period. The third term shows its dependence on Ni film thickness. The fourth term indicates the exponential decreasing force with distance between substrate and pill. Calculations represented in Figure 2-5 show the force magnitude as a function of the separation between the pill device and the recess for different hard magnetic patterned stripe periods. The model represented by Equation 2.3 predicts a significant retention force can be produced (three orders of magnitude greater than the force of gravity). Using MASA, a retention force can be implemented and reasonable parameters for film thicknesses, spacings, and field magnitude can be determined with the help of this model.

The magnetic attractive force exponentially decays with distance from the bottom of the recess. Since the purpose of this field is to retain pills in the recess, the field should be strong within a micron of the recess bottom. The period should be about the height of the recess or larger, which is typically around 4 μm. The derivation of Equation 2.1 assumes the period L is much smaller than the width of the recess, thus if larger period were to be used the resulting force would be smaller than the above equation predicts. A stripe pattern was used to simplify the derivation, however many different patterns might be used. Different patterns could offer advantages in attractive forces or alignment. However the stripe pattern simplifies processing and allows quantitative analysis leading to an understanding of the feasibility of this assembly technique.

2.4 Pill Bonding

Assembly techniques locate individual devices en mass at particular places on a target substrate. However, forces used in assembly are often not strong enough to permanently attach the devices there, and a second step is required to produce a mechanical bond and insure electrical contact to the target substrate. This thesis work will use a metal-to-metal solder bond which is often used to fix these types of devices to a substrate. Though solder bonds are commonly used in flip chip bonding and aligned pillar bonding, bonding individual 50-micron diameter pill devices onto a substrate

poses an interesting problem.

Techniques such as APB, flip chip, and wafer bonding apply pressure to the wafers while heating the bonding interface to obtain a reliable bond using either a metal to metal bond or a metal to semiconductor bond. The bonding pressure is evenly distributed over the substrate and in the case of align pillar bonding, the substrate can be removed after the bonding step. The magnetic force in MASA could be used as a bonding force, however the magnetic force may not be large enough to provide the needed pressure especially at temperatures approaching the Currie point of the magnetic materials. Mindy Teo has addressed this issue with a mechanical approach [1]. Using a flexible temperature resistant membrane pressed against the pill devices, an adequate force can be produced and has successfully bonded pick and place assembled devices. The membrane bonding technique is explained further in Chapter 5 Section 5.3. This thesis represents the first successful application of the membrane bonding technique to bond and integrate actual device pills on an IC wafer.

Chapter 3

Magnetic Measurements

A numerical simulation of the magnetic attractive force in MASA was developed by Prof. Fonstad, Joe Rumpler , et.al. [21] and was discussed in Chapter 2 Section 2.3. The calculations suggested that the force could be significant, however several assumptions were made within this model and no experimental verification was attempted. Non-ideal material properties and finite boundaries could reduce the potential retention force associated with MASA. To determine experimentally whether these magnetic forces are suitable for assembly, a way to physically measure these forces is needed. Such a technique would also give insight into how different types of magnetic materials and their patterning affect the force exerted on the pills during assembly. A micro-cantilever was developed to measure the MASA force. A schematic of this cantilever can be seen in Figure 3-1. The cantilever arms extend to a head that is designed to simulate the bottom surface of a pill device in MASA. The head of the cantilever was designed to be either 2,500 μm^2 or 10,000 μm^2 in area and have a 200 nm thick Ni film. Both the area and film are similar to those of a real pill device. The Ni film on the head interacts with the spatially varying magnetic force, exerting a force that pulls the head to the hard magnetic substrate that is producing the magnetic field. By measuring the deflection caused by the magnetic force, a measurement of the magnetic force can be made. The spring constant of cantilever must also be known to determine the correspondence between the applied force and the cantilever deflection . This detection system has to measure a force as low as

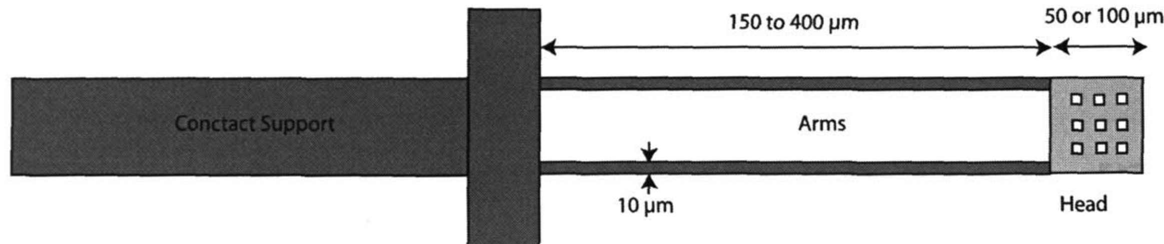


Figure 3-1: Schematic showing the dimensions of the designed cantilevers.

$5 \cdot 10^{-7}$nt, so these cantilever devices must be designed to this level of sensitivity. The cantilever devices made in this work used Microsystems Technology Laboratory (MTL) facilities at Massachusetts Institute of Technology (MIT). In this Chapter a design for this cantilever device will be discussed in Section 3.1 and simulations of the cantilever devices will be discussed in Section 3.2. Section 3.3 is a detailed discussion of the fabrication process, while measurements using these cantilevers will be presented in Section 3.4. Finally suggested improvements and future work are discussed in Section 3.5

3.1 Cantilever Design

The cantilever is designed to have a head with dimensions similar to those of a VCSEL pill; one set of cantilevers had 50 by 50 μm^2 heads and a thickness of 4 μm, and a second set has 100 by 100 μm^2 heads. The larger size is used to achieve greater sensitivity. Two arms, 10 μm wide, and 4 μm high extend to the base of the cantilever. The distance from the base to the head varies in length. Figure 3-1 is a plan view schematic showing the dimensions of the cantilevers. Most of the bending was designed to occur in the arms, their thin dimension producing a small spring constant. The two arms are placed on the left and right sides of the head to prevent axial tilting of the devices. The cantilever was fabricated using n-type silicon allowing electrical conduction through the arms to the head, enabling a voltage to be applied for pull down measurements. On the head, a 200 nm Ni film is deposited and patterned,

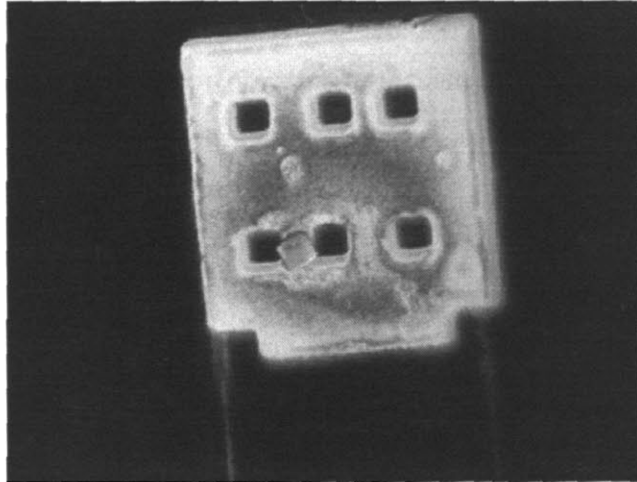


Figure 3-2: 100 X 100 μm cantilever head with 200 nm thick Ni layer covered by gold

providing the force interaction needed between the cantilever head and the magnetic field. Figure 3-2 shows the head of one such cantilever, with the two arms of the devices stretching downward and out of the field of the micrograph.

As detailed in the following section of this chapter, a set of cantilevers was designed to be placed on a variety of substrates to sense their magnetic force. These cantilevers require a spacing of 2 μm or less between the head of the cantilever and the hard magnetic film substrate in order to sense the magnetic force. However placing substrates face-to-face, while obtaining a consistent cantilever spacing was found to be problematic. A large window opening can be placed in the cantilever substrate to view the devices from the back side, and a probe tip can be used to flex the cantilevers into contact with the opposing substrate. The focal plane of the microscope above the sample can be used to adjust and determine the spacing between the cantilever head and the substrate. Placing a voltage across the capacitor, formed by the cantilever and the substrate, produces a deflection in the cantilever due to the the attraction of the charges across the capacitor. As the voltage increases this deflection increases until the system is no longer stable and the cantilever is suddenly pulled down to the substrate. The voltage at which the system becomes unstable is called the pull in voltage. By determining the pull in characteristics of the cantilevers, a spring

constant estimate can be made. From this spring constant, measured forces can be determined. schematics of this measurement can be found in Figure 3-3 and Figure 3-8. The measurement techniques used in this study are described fully in Section 3.4.

Film stresses that arise during processing can dominate cantilever structures and must be taken in account when designing a cantilever. These stresses can induce curvature within the cantilever devices after they are freed from their substrate. Slight curvatures will change the contact angle between the cantilever device and the magnetic substrate. The cantilevers are fabricated using single crystal silicon, which is essentially a strain-free material, but almost all deposited films will induce stresses, so these films must be used with caution and removed from the device if possible. However, it is essential to have a Ni film on the head of the device to induce an interaction with the applied field. Fortunately the film thickness is 4μm and is relatively rigid due to its relatively large width of 50 μm. Figure 3-2 shows the head of one cantilever produced. The 200 nm of Ni deposited on the device has little detrimental affect on the planarity of the device since little or no curvature of the heads were seen in observation.

3.2 Cantilever Simulation

There are some basic equations associated with cantilever devices, which can help predict and reveal the basic properties of the device. The most important device property associated with a cantilever device is its spring constant K_s. This constant relates the deflection (x_s) of the device to the force (F_s) applied to it ($F_s = K_s x_s$). One potential way of determining this constant K_s is to apply a known force F_s, and measure this deflectionx_s. As suggested in the previous section a known voltage can be applied across the cantilever and the measuring substrate. This system can be reduced to a voltage V being applied across a two parallel plates with area A, one of which is attached to a spring with a spring constant value K_s. The parallel plates have an initial separation of g_o, which can be measured. A schematic of this

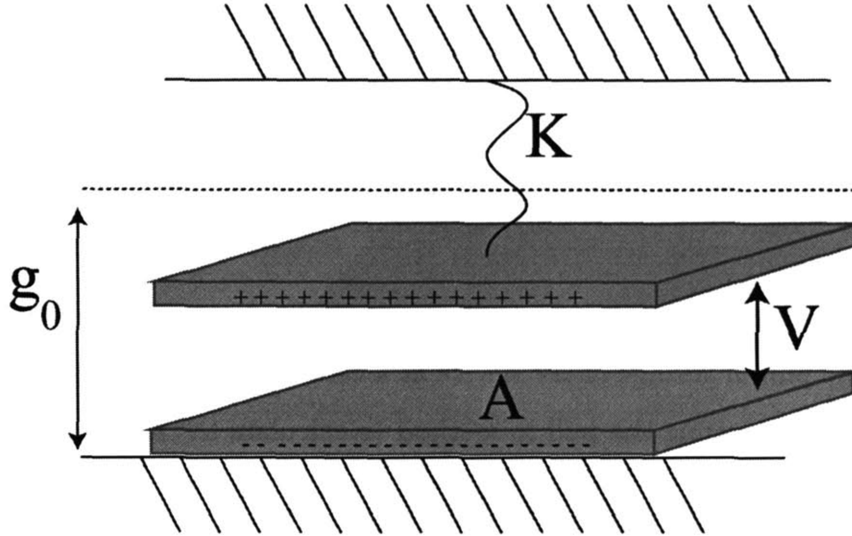


Figure 3-3: Schematic of the cantilever simplified as parallel plate capacitor on spring. A is the area of the capacitive structure, V is the voltage applied across the structure, K is the spring constant, and g_o is the initial gap distance (i.e. with V=0)

system can be found in Figure 3-3. The voltage across these parallel plates is slowly increased causing the separation between the two plates to decrease, resulting in an increased capacitance between the plates. The voltage can be increased, decreasing the separation until a critical voltage and separation is reached, at which time the cantilever pulls in (i.e. the separation between the plates is 0). The voltage and the separation at which this instability occurs are defined as the pull in voltage and pull in separation respectively.

The value of this pull in voltage and the corresponding pull in separation has a well known solution [22]. The pull in separation has been shown to be 2/3 the initial separation as given in Equation 3.1, where g_o is the initial separation, and g_{pi} is the distance just before pull in.

$$g_{pi} = 2/3 \cdot g_o \tag{3.1}$$

The pull in voltage can be solved in terms of initial separation (g_o), the area (A), the permitivity of free space (ϵ), and the spring constant of the device (K). The resulting relation is given in Equation 3.2[22], which can be solved for K, resulting in Equation 3.3[22].

$$V_{pi} = \sqrt{\frac{8Kg_o^3}{27\epsilon A}} \tag{3.2}$$

$$K = \frac{17\epsilon A V_{pi}^2}{3g_o^3} \tag{3.3}$$

Using this relationship, the spring constant of the device can be determined by measuring the pull in voltage of the device at a certain initial spacing. One source of error resulting from using the pull in method to calculate the spring constant of the cantilever is in determining the value of the initial distance g_o between the parallel plates. The accuracy of this distance measurement will determine the accuracy of the spring constant obtained. The results from the pull in measurements can be compared to the theoretical spring constant of the cantilever determined using the device's geometry (width W, height H, length L)and the Young's modulus of the material (E) the device is fabricated with. This geometrical relationship is given by Equation 3.4[22].

$$K = \frac{EWH^3}{4L^3} \tag{3.4}$$

3.3 Cantilever Fabrication

To fabricate cantilevers, a silicon-on-insulator (SOI) wafer was used. The top n-type silicon device layer was 4 μm thick. This layer dimension determines the thickness of the cantilevers. As mentioned in Section 3.1, once the silicon device layer is etched free from the oxide layer below the single crystal device layer is stress-free, preventing curling of the cantilevers. The oxide layer below the silicon film was 1 μ thick, which is relatively large for an SOI wafer, however this thickness provides a good etch stop layer during the backside window etch. Using a die saw, the SOI wafer was cut into 1.1 cm x 1.1 cm dies before processing.

MEMS device fabrication differ from normal semiconductor fabrication. Free floating devices such as cantilevers are very fragile and vulnerable, especially to wet pro-

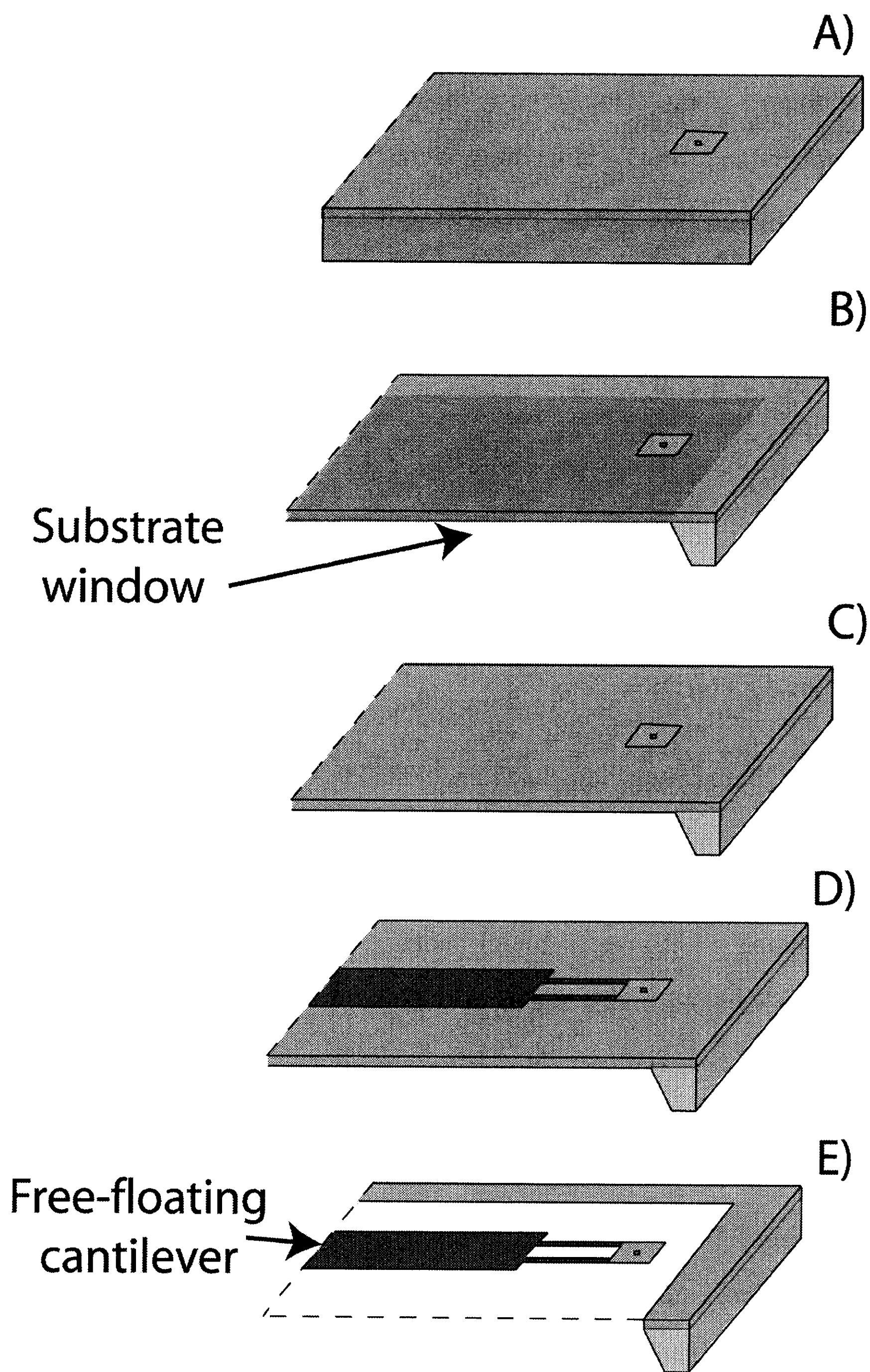


Figure 3-4: Schematic of the fabrication steps for the cantilever device. A) Head metal is deposited. B) Substrate window is etched. C) Oxide etch stop is removed just below the silicond device membrane. D) Cantilever shape is patterned. E) Silicon is etched into cantilever shape using RIE.

cessing. During drying, solutions used in wet processing (i.e. wet etches and solvent cleans) tend bead between adjacent exposed surfaces. As the solution dries the surface tension of the liquid pulls free floating surfaces to their adjacent surfaces, causing these surfaces to touch and stick to each other. The cantilevers can either break during evaporation or become stuck permanently to an adjacent surface. Avoiding wet etches and cleaning solvents during processing is essential when processing these fragile cantilever devices. The next Section will discuss metal deposition for these devices, followed by backside window etching, the semiconductor etch, and a brief section on vapor-phase oxide etching.

3.3.1 Metalization

The first step in the process, which is shown in Figure 3-4, is to pattern the Ni layer on the silicon film to form the head of the device. A Ni metal layer is deposited and patterned using photo-resist lift-off with e-beam metal deposition. Stiction of the metal to the silicon device surface can be an issue, an oxygen plasma of the silicon surface is needed to clean the surface. Buffered oxide etch (BOE) is not used because a thin surface oxide layer between the silicon surface and the metal layers can aide in stiction, and a electrical contact from the silicon to the metal layer. A metal layer sequence of Cr (20nm) Ni (200nm) Au (20nm), in order of deposition, was deposited and lifted off using negative NR7 3000P photoresist [23]. The resist remover specifically made for the NR7 series (RR7) was used. In order to prevent the metal layers from unsticking from the silicon surface care must be taken if agitation is used to aide lift-off. A solvent flow, induced by pipetting solvent in and out over the surface of the sample, was used to promote metal removal in these experiments. Occasional problems with metal adhesion to the silicon surface were observed, however it is likely that using a thicker Cr layer (100nm) could be used to resolve this issue.

3.3.2 Backside Window

Several techniques were used to try to free the cantilever devices from the substrate. Initial work focused on selective wet etching of the oxide layer, undercutting the cantilever. However this involved using an HF wet etchant, which upon drying, as mentioned in the previous section, induced the cantilevers to permanently stick to the surface of the silicon substrate below. A backside window avoids such problems. This window is etched from non-device side of the SOI wafer down to the oxide layer protecting the Silicon device layer. A thin 4 μm device membrane was formed using this etch. The wafer surrounding the window remains to provide structural support during further processing and testing. This window is around 6 mm by 4 mm in dimensions. This widow etch step can be seen in Figure 3-4 B).

Using the tools in Experimental Materials Laboratory (EML), it is not easy to produce such window. It is hard to pattern such a window with a wet etch, while also maintaining protection of the front of the wafer. Black wax was used in several experiments as a masking agent, but potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) required elevated temperatures for etching (80 ^{0}C) and the wax would soften at those temperatures. When teflon or glass slides were used to mask the area, bubbles prevented the etching of the substrate. A dry reactive ion etch avoided these problems. SF_6 was used to etch a depth of 500 μm of the substrate window, using two pieces of glass cover slide as the etch mask, adhered on the silicon substrate with black wax to keep the two slides in place. Water soluble tape was used to mask the shorter sides of the window rectangle. It was found that the SF_6 reactive ion etch (RIE) oxide etch rate was slow enough to allow a 30 minute over etch, eliminating all the silicon remaining in the window cause by uneven silicon etching. The entire window could be cleanly etched using this single RIE technique. Figure 3-5 shows this window after the RIE. The oxide layer can be seen preserved, protecting the Si material below. The RIE etch conditions can be found in Appendix B.

Using the RIE in EML, the substrate window etch was a long process. Due to the

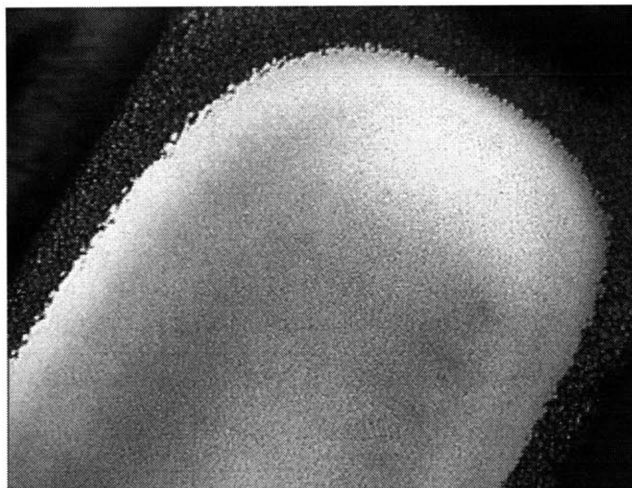


Figure 3-5: The substrate window etched out, revealing the oxide etch stop layer below. The edges of the patterned window area can be seen in the top left, top right, and bottom right corners. Residual roughened under-etched silicon can be seen outlining the smooth center, comprising the oxide surface.

possibility of overheating the power cables in the RIE, all etch lengths were restricted to a 30 minute maximum, with a 15 minute pause to allow the cables to cool down. After each 30 minute etch and during the cool, each substrate was removed and a nitrogen gun was used to spray off the window area. This nitrogen flow would clean off redeposits that collected in the window, decreasing the speed of etch. The etch and nitrogen spray off procedure was repeated about 20 times, for a total of about 10 hours of RIE. This machine was not ideal for deep trench etching, however devices could be produced reliably this way. Once the RIE is finished, the oxide layer can be removed so that only a silicon membrane remains. BOE is used for this for this oxide removal step.

Caution must be used while preforming further processing steps now that the cantilever is released and the sample is fragile. All spin coating must be done with a glass slide attached to the bottom of the sample, providing a flat suction surface for the spinner's vacuum chuck to attach to. Black wax can be used to adhere the sample to the glass slide. When placing the sample under vacuum during subsequent deposition processes and etching steps, an unobstructed air path must be made to the back of the substrate. This air path prevents the membrane from fracturing under

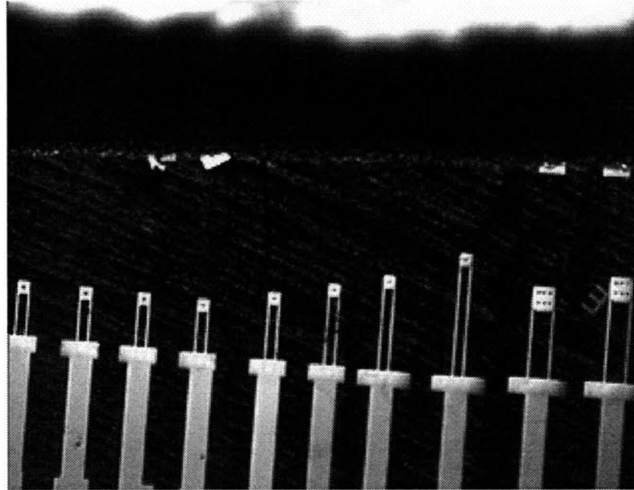


Figure 3-6: Released cantilever devices observed through the backside substrate window. The contact supports are seen below the two legs.

the differential pressure created during evacuation of the process chamber.

The window etch should be done as late as possible in the process. To delay this step, the window must be aligned to the front side's features. However the window does not have to be exact and the alignment of the glass slide for patterning can be done by eye. 3 mm was below the cantilever, allowing the contact supports to add flexibility, such that these devices can be bent down to the target substrate. These contact supports also proved a valuable way to decreases the spring constant of the device, increasing its sensitivity. These contact supports can be seen in Figure 3-6. These contact supports suspend the arms and structurally support the device to what remains of the substrate. The length of these contact supports are determined by the size of the window opening.

3.3.3 Semiconductor Etch

The legs and contact pads of the cantilever device need to be patterned. Ideally this could be done before the backside window etch to reduce the chance of breaking the device membrane during the lithography step. A mask patterning the device film into cantilevers was required. If this mask was deposited and patterned prior to the backside window etch, the mask needed to be resilient to a solvent clean, ruling out a

photo-resist mask. Plasma enhanced chemical vapor deposition (PECVD) oxide was tried as a mask material, however a lot of strain is introduced into the devices due to this thin film. This film could be selectively removed after the device membrane etch, however a wet BOE etch would damage the cantilever devices. Vapor phase hydrofluoric acid etch was tried and showed decent results, but due to the complexity of this process and the vulnerability of the highly stress cantilevers it was deemed unsatisfactory.

A very thin Aluminum mask was tried. 20 nm of aluminum was deposited and used as an etch mask. This thin film still induce enough strain in the cantilever structures to produce curling in the devices. Masking the device membrane for the cantilever etch prior to the backside window etch was abandoned. In the end, 1 μm of photoresist was spun and patterned into cantilevers on the freed device membrane. The photoresist was used as the RIE mask .

The device membrane surface was patterned into the cantilever using 1μm thick photo-resist. The silicon can then be etched using an SF_6 RIE etch for 8 minutes. The processing parameters can be found in Appendix B. The RIE removes most of the Si membrane, resulting in cantilevers have a 4 μm height. Care must be taken with this etch to avoid undercutting of the mask. To prevent this, the etch must take place at low pressures, 15 mTorr or below for the EML RIE. In order to obtain a plasma at these pressures, the plasma must be first struck at a minimum of 18 mTorr. The chamber pressure can then be reduced, while still maintaining a plasma. This etch must be done in intervals 3 minute steps or less, in order to prevent over etching, inducing undercutting. Figure 3-7 shows the long thin arms of the cantilevers resulting from the device membrane RIE processing.

3.3.4 Selective Oxide Vapor Etch Trials

Though a selective oxide vapor etch processing step was not used to process the cantilever devices used in this work, vapor-phase etching can be a useful tool. 50% HF is placed in a beaker and the sample is taped within beaker but not immersed in the liquid. A fiber light illuminated the surface of the sample to raise the sample tem-

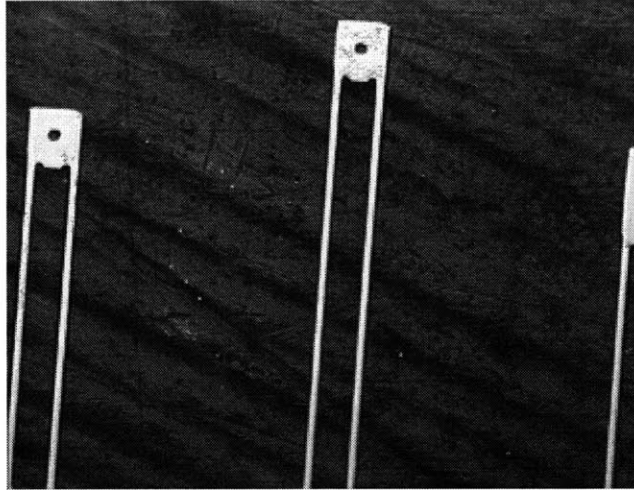


Figure 3-7: Micrograph of fully processed cantilever arms, as seen through the backside window.

perature while preventing condensation on the sample. The beaker is then covered, allowing HF vapor to fill the closed beaker and etch the SiO_2. The clear cover allows the light to illuminate the sample. 1 μm of SiO_2 was etched in 30 minutes using this technique. This vapor-phase etch could be used to remove the oxide selective etch layer in the SOI wafer. This dry removal of the oxide layer would allow full cantilever device layer processing before the backside window was etched through.

3.4 Cantilever Measurements

There are two types measurements that need to be done using the cantilevers for the magnetic attractive study. First, the cantilevers need to be characterized. The spring constant of these devices must be obtained to determine the force values associated with their deflection. As discussed in Section 3.2, a pull in measurement can be used to estimate this spring constant of each cantilever. Once K_s is determined, the cantilevers can be used to measure the attractive force associated with the varying magnetic field interaction. A pull up measurement can be used to achieve this magnetic force measurement. These measurement techniques are schematically represented in Figure 3-8. The next subsection will discuss spring constant measurements,

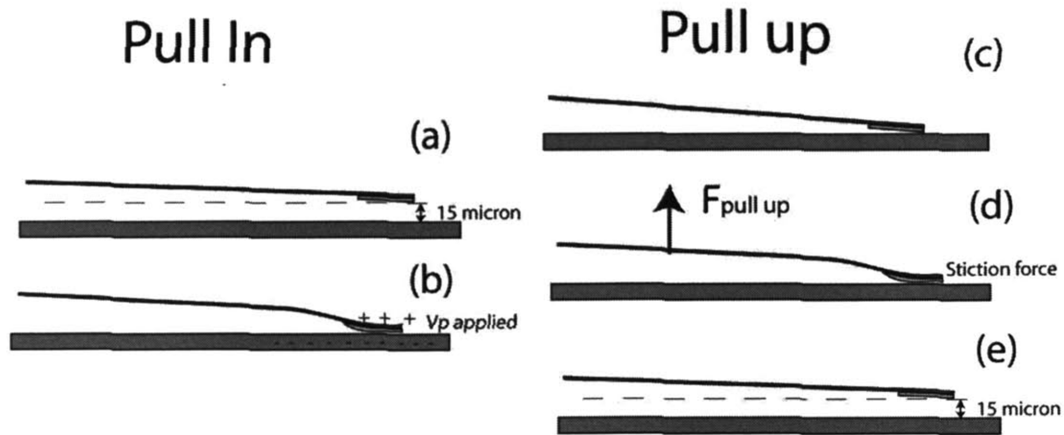


Figure 3-8: Schematic of measurement techniques using these cantilevers. Pull in a) cantilever with initial separation of 15 μm. b) Voltage measured when cantilever pulls in during voltage potential ramp. Pull up c) Cantilever head is placed on the surface of the sample. d) Cantilever is slowly pulled up, with stiction force keeping the head down. e) The cantilever pulls up because the due to bending of the cantilever overcomes the stiction force, resulting in a 15 μm separation between the head and the surface of the sample.

and a discussion of the magnetic film measurements will follow.

An electrical probe station, and HP4145B parameter analyzer were used as the measurement setup in this study. The probes manipulated and electrically contacted the cantilevers. Using the microscope on the probe station, the user could to align, manipulate, and observe the cantilever device through the substrate window on the cantilever chip.

3.4.1 Spring Constant Measurement

To measure the spring constant of these cantilever devices, a voltage pull in method was used as described in Section 3.2 and depicted Figure 3-3 and Figure 3-8. These measurements are made by placing the face of the cantilever substrate on top of the test substrate. The cantilever is deflected to a certain spacing above the test substrate. This spacing is set and measured using the depth of field of the microscope objective on the probe station. A second probe is placed on the conducting part of the substrate and a bias voltage is applied. The microscope views the head to detect when the device pulls down to the test substrate surface.

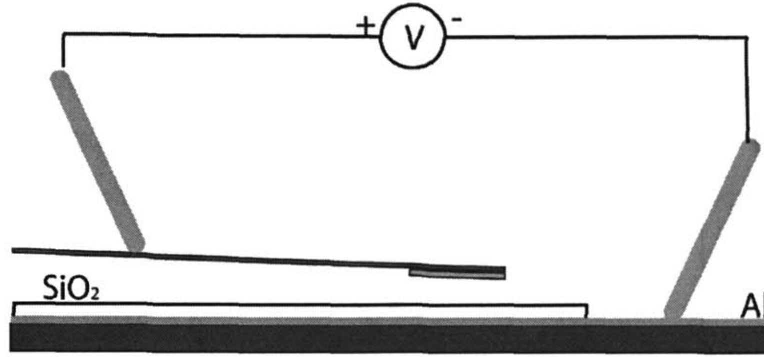


Figure 3-9: Cantilever pull down measurement setup. One probe contacts and actuates the cantilever devices, while the second probe contacts the aluminum layer. An oxide layer is situated between the cantilever and the aluminum layer to prevent electrical conduction through cantilever legs, which could damage the cantilever device .

These pull in measurements were carried out for each cantilever at varying initial separations, and the corresponding voltage at which the cantilever is pulled in was recorded. Even small amounts of current can damage the cantilever legs. Though the amount of current can be constrained by the HP4145B parameter analyzer, a large unconstrained pulse of current can flow. To prevent this flow the substrate, above which the cantilevers are suspended, has an oxide layer on top to prevent a conducting path through the cantilever during pull down. A schematic of this substrate is shown in Figure 3-9. Away from the cantilever heads, a window in the protective oxide layer was etched to contact the aluminum metal layer below. This contact provided the second parallel plate needed for the capacitive structure for the pull in measurements.

Using Equation 3.3, one can plot the resulting pull in voltage, V_{pi}, against the expected values for a specific spring constant. The resulting simulated curves can be seen in Figure 3-10. Several cantilevers were measured, two of which have their V_{pi} plotted as a function of gap spacing in the same figure. The data labeled Head 300 results from a 300 micron long cantilever. This data suggest this cantilever has a spring constant of 1.2 nt/m. The spring constant value obtained using the pull in method can be checked against what is obtained when the dimensions of the device are inserted into Equation 3.4. The resulting spring constant is 2 nt/m, the difference in the two constants is most likely due to the observed mask undercut

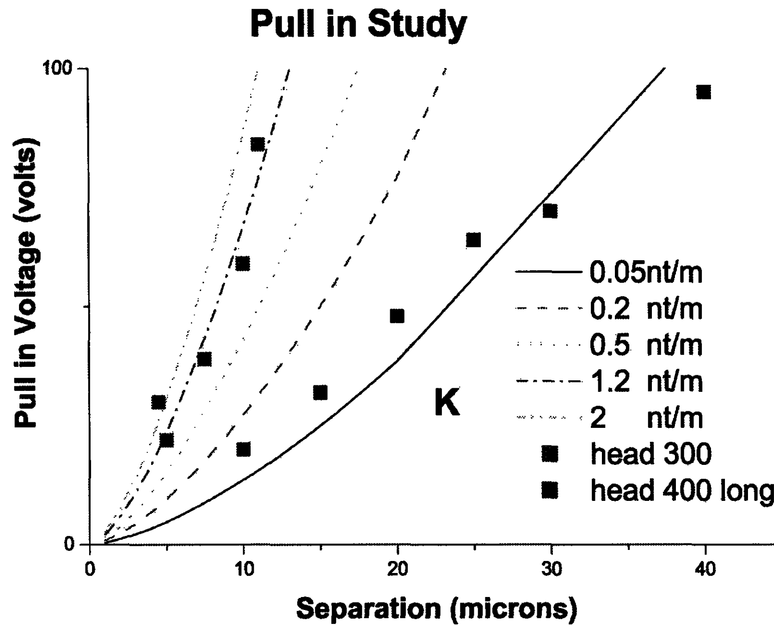


Figure 3-10: Modeled cantilever spring constants as a function of separation along with measured data from device heads.

thinning of the cantilever arms due etching. There is also a good deal of error with these measurements, variation in the pull in voltage for the same spacing often varied by 30%. The error of these measurement is approximately 30%, however exact force numbers are not the goal of this detection. The goal of these measurements are to show the magnitudes predicted by the MASA model show good correspondance to actual films. The variations in the force magnitude across the magnetic substrate can be analyzed and compared without the need for precise force measurements. This variation will be discussed in Section 3.4.2.

The goal of this measurement system is to detect forces as low as $5 \cdot 10^{-7}$nt. With a spring constant of 0.2, the system would be able to detect a 2.5 μm movement in the cantilever. Using the microscope setup, only a movement of 5 μm or larger can be reliably measured. A way to extend this cantilever, and thus decrease the spring constant was needed. To do this, the contact support seen in Figure 3-1, was used as an extension. This added length significantly reduced the overall spring constant. The data for this 400 nm long device can also be seen in Figure 3-10. This data corresponds to a spring constant of .05 nt/m, and agrees with the spring constant of .058 nt/m, obtained by using the dimensions of the cantilever and Equation 3.4. It

was assumed for this dimensional estimation of the spring constant that the K_s value was mainly determined by the dimensions of the contact support. A device with this spring constant requires the ability to measure 10 μm spacings to sense a force of $5 \cdot 10^{-7}$nt. Table 3.1 summarizes the cantilever measurement and simulation results.

Table 3.1: Spring Constant

Properties	Head 300	Head 400 long
Length μm	300	400
Head sizes μm^2	10,000	10,000
Contact support (length μm)	0	2,000
Young's modulus (GPa)	150	150
Measured K nt/m	1.2	0.05
Simulated K nt/m	2	0.06
$5 \cdot 10^{-7}$nt distance	2.5 μm	10μm

3.4.2 Magnetic Film Measurements

Patterned magnetic films were measured using the pull up technique described schematically in Figure 3-8 (c,d,e). A cantilever is brought down to the surface of the magnetic substrate, such that the head is in flat contact to the surface. The probe actuating the cantilever is then moved up in the out of plane direction, making the device flex. This flexing occurs until the stiction force on the head is no longer strong enough to oppose the pull from the devices arms. At this point the head releases, and the separation from the surface of the magnetics substrate to the head is the distance term needed to determine the force in the Kx=F spring model. The cantilever can be seen in its full down state, flexed state, and pulled up state in Figures 3-11 (a,b, and c, respectively).

One major concern when making these measurements are static forces. These force can dominate cantilever devices on the micron scale. Electrostatic forces can be identified by their pull in distance, which can exceed 10 μm, as opposed to the magnetic field force which decays to an insignificant force beyond 3μm. The static forces can be reduced by grounding both the cantilever and the surface of the magnetic

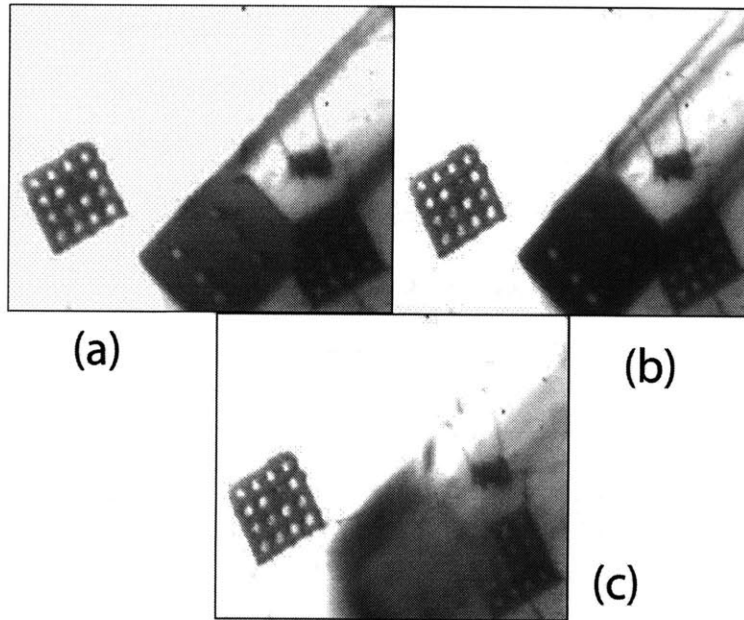


Figure 3-11: Micrograph of a cantilever above a magnetic substrate. The two squares in the background are patterned samarium cobalt.(a) The cantilever device in its full down position. (b) The device is sticking with flexed arms. (c) The device shown after stiction force released the cantilever. The device head is no longer within the microscopes depth of field.

substrate, preventing any charge from building up. Only the magnetic force is retained due to the patterned hard magnetic material.

A substrate with a samarium cobalt thin film obtained from Prof. Cadieu [24] was used for these measurements. It was patterned by Joe Rumpler in selected regions of the substrate (100 by 100 μm in area). Within these regions 10 μm squares were patterned in an array with a 20 μm pitch. Figure 3-11 shows a micrograph of this magnetic material with the cantilever above. The cantilever head could be placed and measured in both samarium cobalt patterned regions and non-patterned regions. The magnetic substrate was magnetized in a field of 5 kG.

The results of these experiments showed a force which varied greatly across the substrate. There were regions that showed a stiction force that pulled the cantilever 60-80 μm, while other regions only measured 10 - 20 μm of deflection. There are also some areas where there was no detectable forces at all. The higher force readings were found near or on areas where the magnetic film had been patterned. The pull up distance can be equated to a pressure force on the cantilever using Equation 3.5.

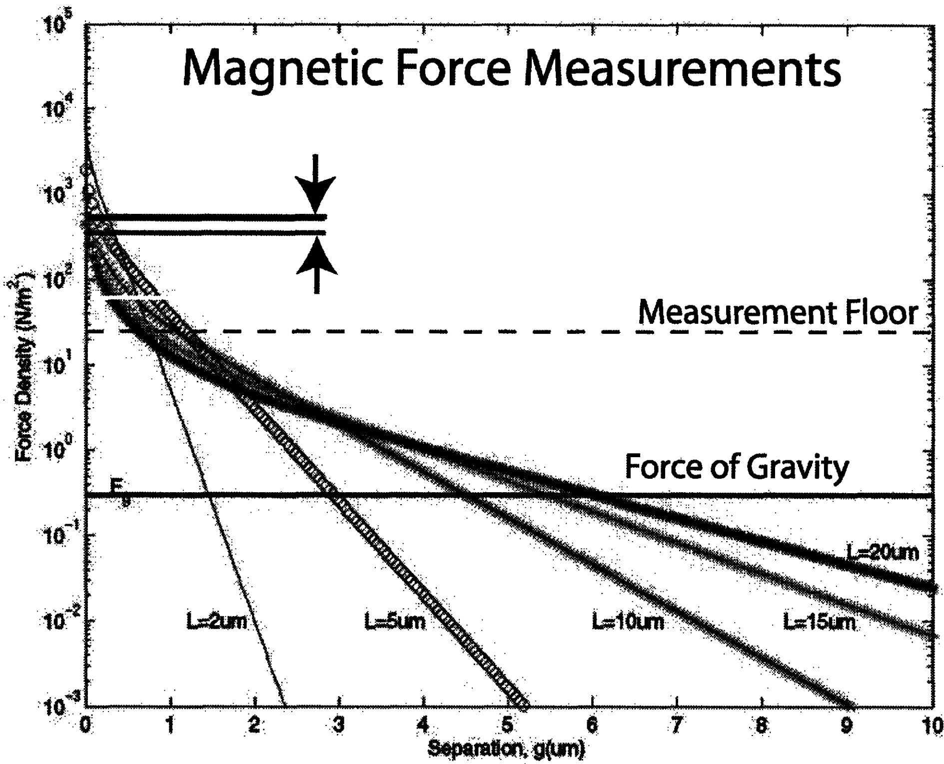


Figure 3-12: Modeled force measurements as a function of distance from Rumpler et. al. Force data range found in cantilever measurement shown within (separation ≤ 1 μm).

Pull up test were preformed on non-magnetic substrates and unpatterned magnetic substrates, revealing no significant stiction forces detected by the cantilever sensors, suggesting the forces seen using these cantilever devices were due to a magnetic retention force produces by the varying magnetic field.

$$Pressure = \frac{KX}{A} = \frac{0.05 \cdot 60 \cdot 10^{-6}}{10 \cdot 10^{-8}} = 300nt/m^2 \quad (3.5)$$

With spring constant K_s=0.05nt/m, area A= $10^{-7}m^2$, and separation x ranging from $6 \cdot 10^{-}5$ to $8 \cdot 10^{-}5$, a force density of $300nt/m^2$ to $400nt/m^2$ is calculated. This range of pressures can be compared to those predicted by the model in Chapter 2 Section 2.3. This comparison is shown in Figure 3-12. The force magnitudes are similar to those predicted by the model for a separation (between the pill and the recess) length scale of 1 μm or less.

3.5 Future Work

This work has measured for the first time the force from a varying magnetic field. A similar force is intended to be used in for retention magnetically-assisted statistical assembly. In doing so it has confirmed the force magnitude predicted from the model in Chapter 2 Section 2.3. However this work also gave greater insight into the issues associated with this type of assembly. In order for assembly based on this magnetic force to be feasible, the patterned magnetic film must exert a consistent force, materials and patterning techniques must be found to produce this environment. It has also been seen, as discussed in Section 3.4.2, that static electric force can dominate in this size regime, and attempts must be made to reduce charge build up on the surfaces. Metal coatings could be used to help reduce these forces for instance.

The cantilevers used were able to detect these magnetic forces, however design improvements can be made. Extending the length of the thin arms will decrease their K_s value proportional to $1/L^3$, removing the dependence on the contact extension to increase sensitivity. The metal head mask can be designed to place metal exclusively on the head of the device. The openings within the head of the cantilever can also be removed. These opening were only needed for a previous wet etch design. Accuracy depends on the microscope height adjustment, and any improvements to this mechanism would enable more exacting measurements.

Chapter 4

VCSEL Pill Development

There are several attributes required to make individual micron-scale optoelectronic pills suitable for integration techniques. The optoelectronic pill devices are designed to be cylindrical in shape for radial symmetry, and have a metalized backside ohmic contact layer that may include a magnetically susceptible layer that could be used for MASA. The VCSEL device pills are also designed to have either one or two topside contacts and a current aperture to confine current to the middle of the device's active region, reducing the threshold current. Each completed pill is a fully processed micro-laser that can be interconnected electrically to the circuit. This chapter will do a brief process overview in Section 4.1, and then discuss the specifics of the growth material, the mesa etch, aperture oxidation, metal deposition, pill release, backside metalization, WaferBOND^{tm}[25], and freed pill to pill stiction. The final two Sections (4.10 & 4.11) will discuss the resulting pill produced and improvements that can be made.

4.1 Procedure

To produce VCSEL pills, the heterostructure is patterned and the semiconductor is etched into two tier mesas compactly spaced to utilize as much growth material as possible. The material is etched down to an etch stop layer when forming the second tier of the device. The device mesas are oxidized to form the current aperture. The

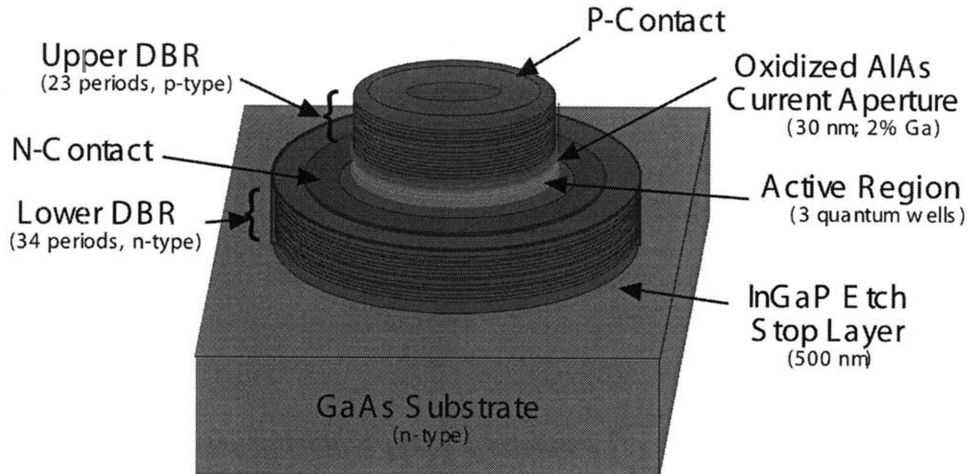


Figure 4-1: A cartoon illustrating a partially-processed two-tiered VCSEL pill after mesa etching and upper ohmic contact formation, and prior to substrate removal and back-side metalization. At this stage the first tests of VCSEL performance can be made.

top metalization steps are then performed. The mesas are next embedded in polymer or wax, and the backside substrate is then removed. The backside removal exposes the backsides of the pills so that a metal layer can be deposited on the bottom of the devices. These devices are then freed from the polymer and stored in isopropyl alcohol (IPA) until assembly. This process is illustrated schematically in Figure 4-2. The following sections will discuss observation, issues, and considerations associated with each particular processing step. Exact process flows can be found in Appendix C.

4.2 VCSEL Growth Material

The VCSEL heterostructure material used in these experiments was obtained from Landmark Optoelectronics ^{TM} [26], a foundry in Taiwan. The elements of the basic heterostructure are shown in Figure 4-1. The structure was based on a standard VCSEL design from the foundry. It is a top emitting AlGaAs VCSEL structure with p-type mirror layers on top and n-type layers on the bottom. The active region consists of three quantum wells emitting at 850 nm. Just above the active region is an $Al_{0.98}Ga_{0.02}As$ layer, which can be oxidized to produce a current aperture. An

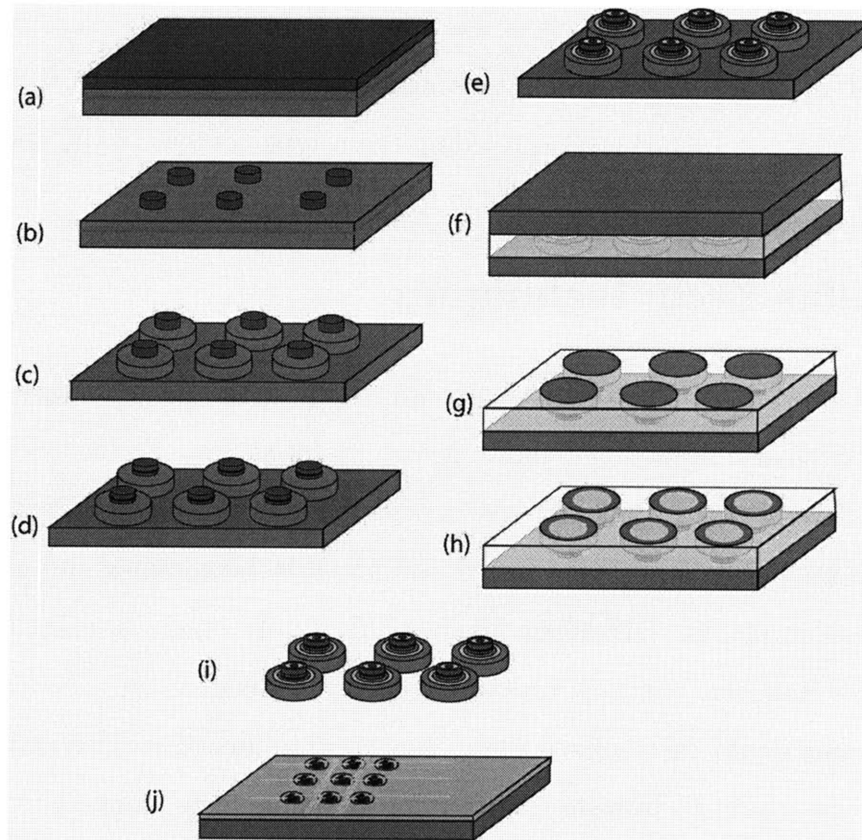


Figure 4-2: A schematic depicting the basic processing needed to obtain pill devices: a) AlGaAs growth material (p-type mirror dark, n-type mirror light), b) first tier etch removing p-type mirror material, c) second tier etch removing n-type mirror material and revealing InGaP layer, d) oxide aperture formation, e) n-type and p-type metalization (light circles), f) front surface embedded & handle wafer bond (silicon substrate is dark and embedding polymer is clear), g) substrate removal, h) backside metalization(light regions), i) pill release, j) integration onto integrated circuit.

InGaP layer is placed at the base of the structure for selective etching; the addition of this layer is the only change made to the standard VCSEL design.

The p-type mirror has eighteen $1/4\ \lambda$ mirror periods. The total height of the p-type mirror stack is 3μm, consisting of layers with varying aluminum composition. There is a highly doped p-type top GaAs buffer layer, providing the p-side contact to the structure. The n-type lower mirror stack has has thirty-four $1/4\ \lambda$ mirror periods and a height of 5μm. The bottom stack also contains a n-type ($10^{19}cm^{-3}$) buffer region just above the InGaP layer, providing the n-type contact to the device.

4.3 Pillar Etch Techniques

A GaAs/AlGaAs semiconductor etch is needed to expose the $Al_{0.98}Ga_{0.02}As$ oxidation layer. An etch is also needed to remove growth material down to the selective sacrificial layer. Several etch techniques were considered and tested, with varying results. Reactive ion etch chemistries were tested and found to be complex and inconsistent with the tools available. RIE trials involving BCl_3, Ar, and Cl_2 chemistries were investigated. However, the etch rates were highly dependent on the cleanliness of the system and would vary substantially. A smoothly etched surface and a reliable etch depth was sought to provide a surface for an ohmic metal contact to be placed, contacting the n-type mirrors exposed after the first tier etch. A topside contact allows for device testing before substrate removal, while also providing for a second interconnect pad option.

The hydrogen-peroxide / sulfuric acid wet etch used in this study produced a smooth surface, enabling the n-type topside contact added, while avoiding sidewall redeposition issues that are sometimes associated with RIE processing. A side-wall redeposition could promote non-uniform oxidation of the aperture. A wet etch technique is prone to undercutting, however predictable undercut can be tolerated if taken into account during mask layout. A wet etch of 2% sulfuric, 12% hydrogen peroxide, and 86% DI water was used with good results. The high percent Al layers can be differentiated from the low percentage layer, due to the dark color shading of these

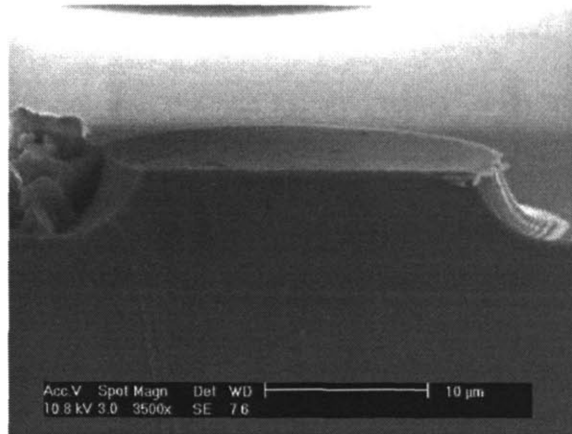


Figure 4-3: Etch profile of first tier wet etch showing undercut. The first tier reaches into the n-type layer

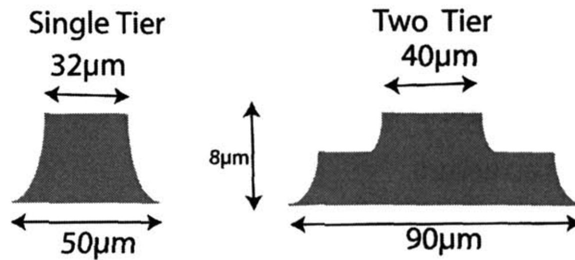


Figure 4-4: Cartoon depicting a single tier device and a two tier device, with approximate dimensions.

high percentage aluminum layers during the sulfuric wet etch. The difference in color enabled in-situ mirror layer removal monitoring. Highly reliable etch depths can be determined by counting the number of mirrors removed during the etch. This sulfuric etch is highly selective to the InGaP layer and will produce a mirror finish when it hits that layer, though this InGaP layer does etch to some degree and can be removed if left too long in the etchant. The resulting mesa as seen in Figure 4-3 has a sloping profile, which must be considered when calculating the oxidation time for the current aperture. Note that the top diameter is significantly smaller than the base, as the lateral etch distance is comparable to the etch depth. Two types of device pi8llars were produced: two tier mesas and single tier mesas. Figure 4-4 illistrates these two types of devices.

4.3.1 Two Tier Mesa Etch

For the two tier structure, a simple photo-resist mask can be used for both tier etches. 3μm NR7 3000P negative resist is used on both steps [23]. As mentioned previously, the mirror layer etching can be measured by observing the shade changes in the surface of the VCSEL substrate during etching. High Al content material is darker. There are 23 mirror layers to be etch before the active region is reached. The active region is identified by a long period of light shading of the etching VCSEL substrate. The n-type mirrors follow, and are etched more quickly than the p-type. After etching the first tier a 5 to 10 microns reduction in diameter can be seen due to undercut. A second photomask is then applied, covering and protecting the first tier. After the masking material is applied, The second tier etch can be preformed. This etch is stopped when the color no longer changes significantly. a highly smooth surface indicates that the sulfuric wet etch has reached the selective InGaP layer at the bottom of the heterostructure.

4.3.2 Single Tier Mesa Etch

A reproducible first tier can be produced in the two tier structure using photo-resist as the etch mask. This reproducibility is mainly due to the relatively shallow etch depth of the first tier (3.5 μm). It was observed that using the same photo-resist etch a mask to etch a single 8 μm tall tier (down to the InGaP etch stop layer) in one etch is inconsistent. The photoresist peals during the sulfuric etch, often resulting in a fully undercut tier. A hard mask is required and a 300 nm thick SiO_2 PECVD film was used in these studies to produce the single tier devices. This film was patterned with photoresist and etch using the standard SF_6 etch recipe (see Appendix B). Though there was significant undercutting of the hard mask, it was consistent with an 8 μm etch. The Mask used was 55 micron in diameter, which resulted in a 30 - 32 μm diameter pill after etching. The consistency of the etch can be seen in Figure 4-5. The hard mask can still be seen under higher magnification in Figure 4-6, where the outer shadow is from the hard mask suspended above the undercut region.

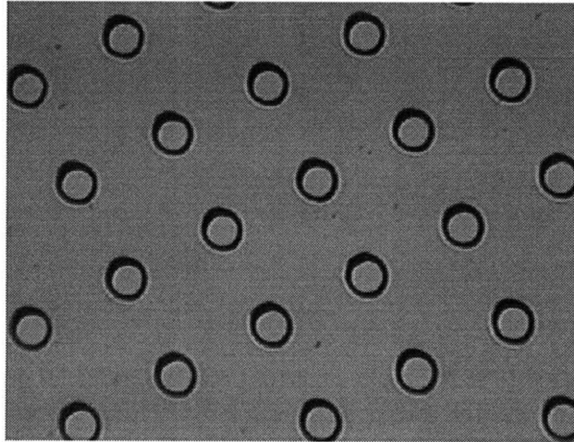


Figure 4-5: Array of single tier etched mesas produced using a hard mask (30-35μm diameter).

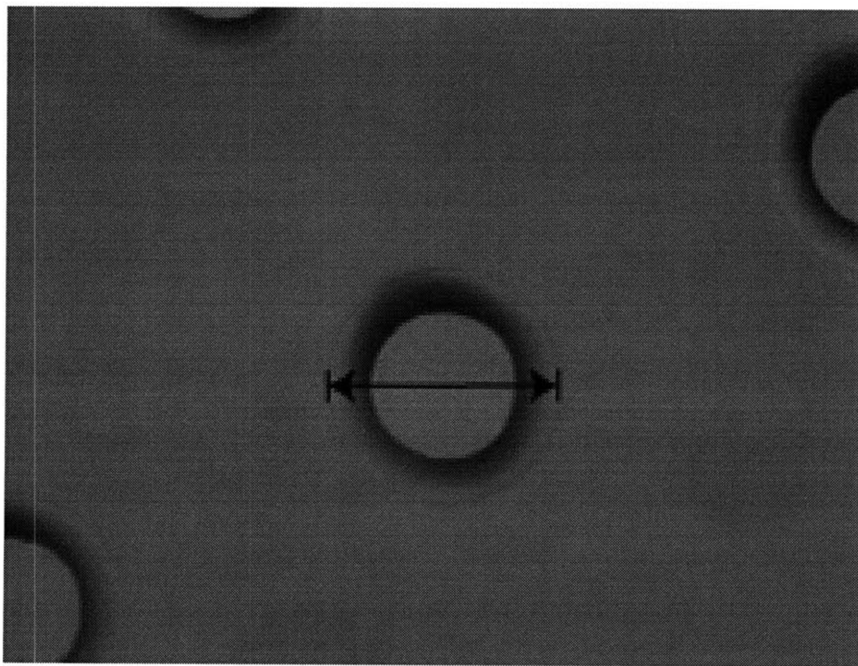


Figure 4-6: Single tier etch with hard mask seen(30-35μm diameter)

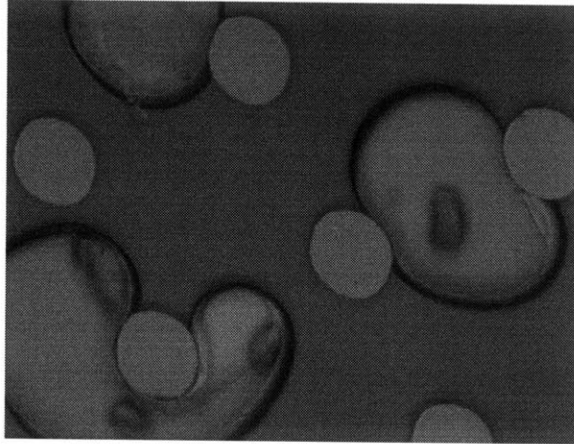


Figure 4-7: Backside of VCSELs showing the bottom of a single tier device. The oval shape of the tier due to non-uniform etching is evident.

The wet etching may not be cylindrically symmetric, and this fact is seen more with increased etch times. The etching can result in an oval bottom, which can be seen after the subsequent substrate removal step, as shown in Figure 4-7. The shaped produced from this tier will impact formation and the shape of the oxide aperture, discussed is Section 4.4. If the selectively oxidizable $Al_{0.98}Ga_{0.02}As$ region in the VCSEL is oval due to etching, a non-ideal oval aperture will be produced when this layer becomes oxidized. The degree to which these patterned circles etch into oval shapes varied across a substrate, and suggests uneven etching. Etching trials need to be done to see how stirring or etch composition might improve the results. However, a reduction in tier etch undercut is the main issue, and any reduction of the undercut would in turn make the tiers more circular.

After the tier has been etched, the hard mask must be removed in order to probe the devices during the oxidation processing. however, long exposure to BOE can undercut the high percentage aluminum layers in the mirror stack, and this needs to be avoided for a good oxidation step and a working device. To that end most of the oxide etch mask was removed using SF_6. However to avoid roughening the surface of the device, the last 50 nm of oxide had to be removed using BOE. A 1 min BOE dip was used in the processing of the single tier devices, which resulted in a visible ring in the mirror stack due to etching of the aluminum layer, similar to that shown in Figure 4-8. This depth was a manageable 1 μm and still produced working devices.

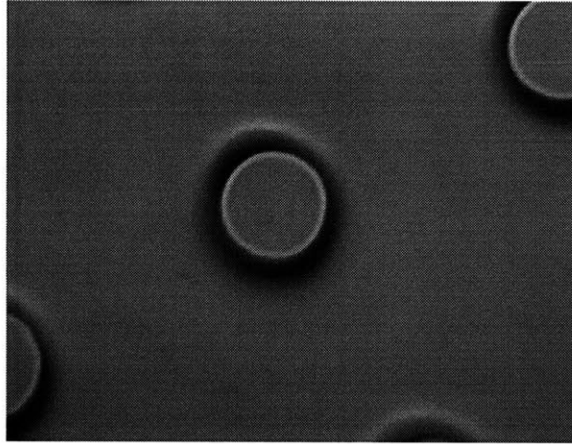


Figure 4-8: A visible ring can appear through the top of the mesa due to etching or oxidation of the $Al_{.92}Ga_{.08}$ layers

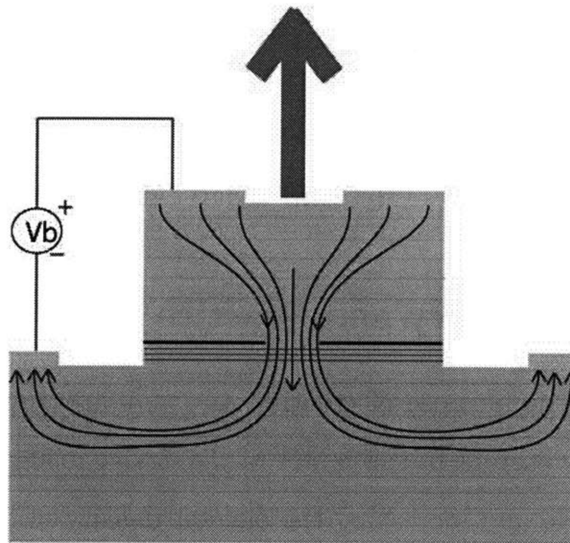


Figure 4-9: Current aperture design

4.4 Aperture Oxidation

In addition to the two contacts on the VCSEL device, a current confinement region (a.k.a current aperture) is added to the structure to obtain a low threshold laser. This aperture concentrates the current to the middle of the device. A schematic depicting the resulting increase in current density is shown in Figure 4-9. The current aperture will also define the light output profile of the device. A current aperture can be formed by ion implantation or with an oxide aperture produced within the structure above the active region. Selective wet oxidation of a high aluminum content layer was used

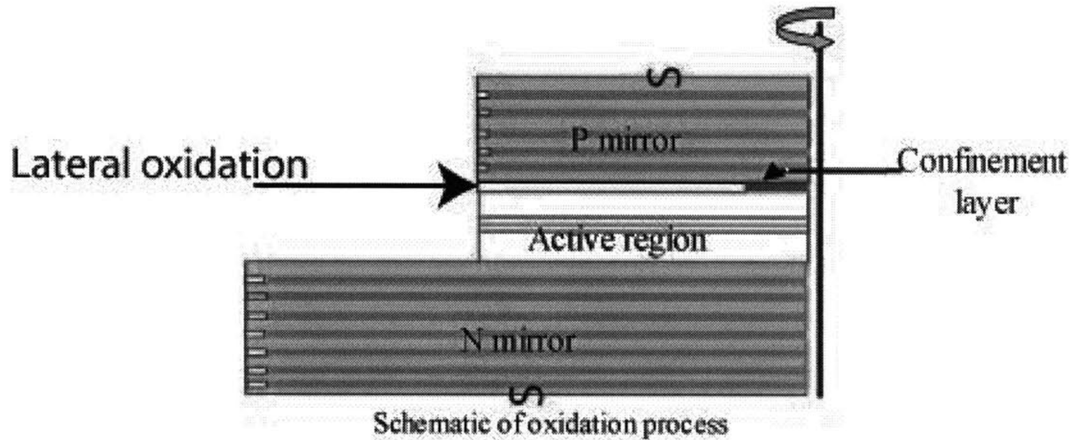


Figure 4-10: Schematic of wet oxidation process

in this work to produce an oxide aperture. The mesa etch removed material past the active region into the bottom mirror layer, exposing the edge of an $\mathrm{Al}_{.98}\mathrm{Ga}_{.02}\mathrm{As}$ layer which can then be selectively oxidized to form Al_2O_3, as shown in Figure 4-10. This layer oxidizes much faster than do the $\mathrm{Al}_{.90}\mathrm{Ga}_{.10}\mathrm{As}$ layers in the two mirror stacks.

4.4.1 Oxidation Theory and Practice

As previously stated, the purpose of creating an oxide aperture within the VCSEL device is to confine the current in the center of the device, using the active regions in the center of the device, and increasing the current density of the device for a given applied current. The oxide formed from wet oxidation of $\mathrm{Al}_{.98}\mathrm{Ga}_{.02}\mathrm{As}$ is Al_2O_3, which has been proven to be a mechanically stable oxide.

A wet oxidation chamber is used to oxidize the $\mathrm{Al}_{.98}\mathrm{Ga}_{.02}\mathrm{As}$ layer and convert all but the center of it to an Al_2O_3 layer. In the oxidation chamber an inert gas is forced through a DI water bubbler to saturate the chamber with water. The nitrogen then flows into the tube furnace where the gas nitrogen gas containing water vapor reacts with the $\mathrm{Al}_{.98}\mathrm{Ga}_{.02}\mathrm{As}$. The oxygen in the water vapor reacts with the aluminum to produce oxide, while the hydrogen within the gas produces a volatile arsenic species, removing the arsenic atoms from the structure. Choquette et. al.[27] has shown that oxidizing a pure AlAs layer using lateral wet oxidation produces an oxide layer that has shrunk linearly from the layer's original size by 12% to 13%, while an oxide

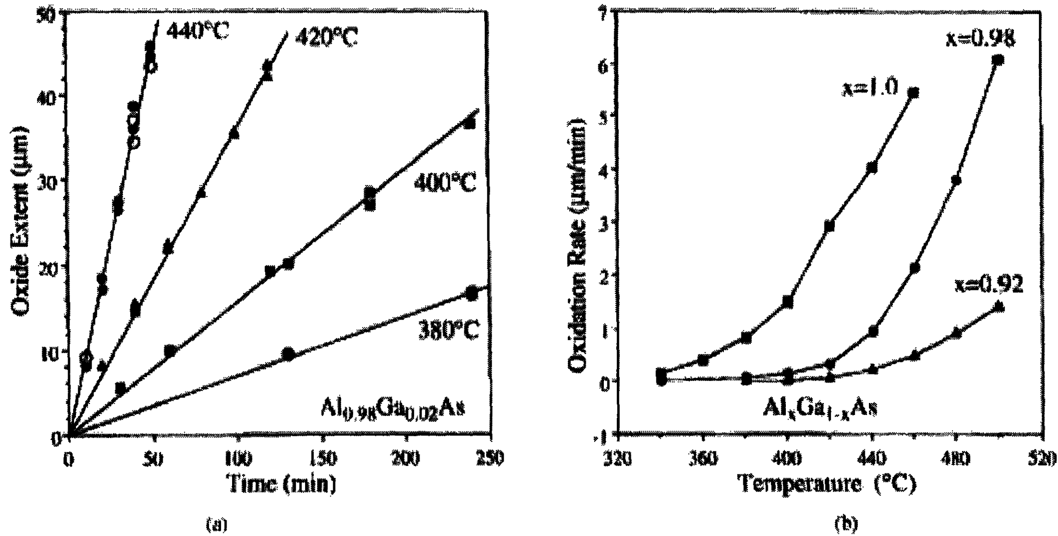


Figure 4-11: 84 nm thick film oxidation rate a) as a function of temperature b) as a function of Al concentration.[27]

produced using $Al_{.98}Ga_{.02}As$ shinks by 6.7%. Adding more Ga to the AlAS layer reduces the shrinkage further, but also reduces the oxidation rate significantly. Thus $Al_{.98}Ga_{.02}As$ layers are chosen to produce films that have less strain, are more stable, and can be preferentially oxidized over higher content Ga layers, such as $Al_{.90}Ga_{.10}As$ which is contained in the VCSEL DBR mirror stack.

Choquette et. al. reported the usage of a four inch furnace tube with a 3 l/min nitrogen carrier gas flow rate. The nitrogen gas was saturated with water vapor to obtain Al_2O_3 oxide apertures. Such conditions were found to be sufficient to provide a constant oxidation rate. Linear lateral oxidation rates were observed in several studies [28, 29, 30, 27], and trials used in the experiments in this study confirmed this linear oxidation rate. Choquette et. al. studied the temperature and layer content dependence of the oxidation rate for an 84 nm film. The temperature and content dependence of the oxidation rate from these experiments are seen in Figure 4-11[27].

Studies also show the film thickness dependence of the oxidation rate. The results of these study can be seen in Figure 4-12 [27]. From these studies, it was found that there was no significant reduction in oxidation rate due to film thickness for film thicknesses greater than 80 nm. Since the aperture layer in the device material used

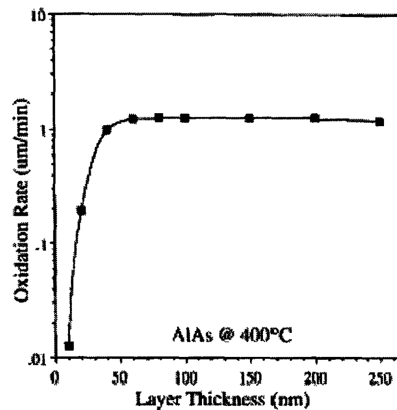


Figure 4-12: Oxidation rate as a function of layer thickness for $Al_{.98}Ga_{.02}As$.[27]

in this study had a thickness of 30 nm, these experiments suggest a significant rate reduction would be seen. Figure 4-12 suggest an oxidation rate reduction of as much as 80% might be seen due to the 30 nm oxide aperture layer.

Overall, the results in these studies were used as a gauge for what to expect from oxidation experiments, however lateral oxidation of these film can be a variable process and specific oxidation rates can be dependent on the setup used. Thus, oxidation trials for the specific setup and films to be used in this study were needed in order to determine repeatable parameters for the oxidation of the aperture.

4.4.2 Oxidation Set Up

The oxidation step uses a 3" tube furnace in Professor Kolodziejski's laboratory at M.I.T.. The furnace is heated to 455 °C, though the actual temperature of the furnace was found to be 10 °C below the reading shown on the temperature controller of the setup. As depicted in Figure 4-13, nitrogen flows into a 300ml beaker of DI water (the bubbler) at a rate of 1700 sccm. The DI water in the bubbler is heated to a temperature of 90 °C. The nitrogen bubbles at the bottom of the beaker through the DI water and flows into the tube furnace. The furnace has heating tape on either end of furnace to prevent condensation on th inlet and outlet of the chamber. However condensation does occur, and a beaker has been setup at the outlet to prevent water

from entering the furnace. Water still condenses on the inside of the tube, so the outlet of the chamber must be watched and emptied from time to time. Samples are placed on a glass boat and inserted into the tube furnace, making sure the side of the furnace are free from condensation. The furnace is then heated until it reaches the desired temperature of 455 ^{o}C, making sure the temperature variance of the chamber is only around 3 ^{o}C. The furnace needs 15 minutes to equilibrate to obtain this stability after insertion of the glass boat. The temperature controller power setting needs to be manually adjusted during insertion to prevent the power controller from over compensating for the sudden cool down upon insertion of the cooler glass boat . Only manual management will prevent the temperature from rising too far above the target set point. A temperature of as much as 10 ^{o}C above set point can be reached without manual management. Another concern when using this setup is the DI water supply in the bubbler. The beaker can run low on DI water after 2-3 hours of continual operation. This system includes water lines intended to maintain the water height in the bubbler beaker and the bath, however this system was found not to be dependable and these levels must be monitored.

Nitrogen flow into the system is continuous, and the nitrogen can be diverted around the bubbler providing a dry inert environment for insert and stabilization of the sample. Studies done by Choquette et. al.[27] use a system where an equilibrium with nitrogen flow, heat and moisture can be reached before insertion of the sample. Their system allowed the sample to be introduced at temperature, using a secondary furnace to heat the sample outside the oxidation furnace. Professor Kolodziejski's system did not have this feature, but it only took a few minutes for condensation to appear on the other side of the furnace, indicating the response time to equilibrium is reasonably fast. Once the temperature of the sample is stable at its desired point, the nitrogen flow is directed through the bubbler and through the furnace. When this occurs the oxidation process begins and a timer for the oxidation is started. Once the oxidation time is up, the nitrogen is rerouted around the bubbler so that dry gas is introduced into the system, stopping the oxidation. The end of the tube furnace is dried to prevent the boat from boiling any condensation deposited on the sides of

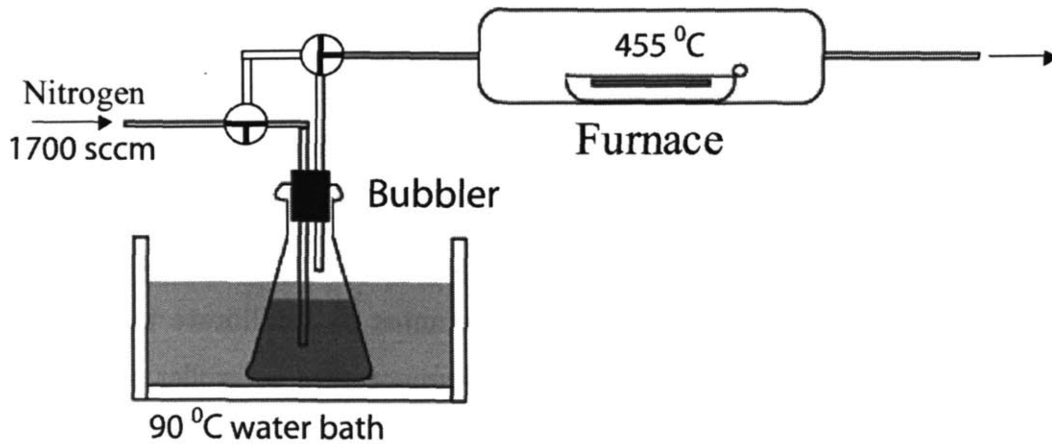


Figure 4-13: Schematic of Prof. Kolodziejski's wet oxidation furnace.

the outlet tube during removal. This condensation can spatter onto the surface of the sample, changing its surface properties. The boat can be removed hot and the sample can be removed from the boat with little cool down time.

Obtaining a dependable oxidation rate is key to obtaining a small aperture and thus obtaining a small threshold current. A trial oxidation run is needed to check the oxidation rate before the primary sample is oxidized. Upon removal from the furnace, the oxidation fronts from the trial sample need to be measured to determine the rate of oxidation. One way to do measure the length of oxidation is from an SEM image of this aperture within the VCSEL heterostructure, as is shown in Figure 4-14. However, the SEM technique requires that the oxidized sample be cleaved through one of the mesas. There are several problems associated with this cleaving process. A flat surface is required to get a good SEM picture, but often the break is non-uniform. The distance of oxidation is also hard to determine because it depends on the place where the mesa is cleaved. If it is not cleaved through the middle the SEM shows a longer oxidation than actually occurs, so separate features, on the oxidized sample, need to be designed specifically for the cleaved SEM measurement. This oxidation visualization technique also does not show the anisotropy of the oxidation within a pill.

Non-invasive techniques were developed to observe the oxidation front externally from the top, the first technique used an IR filter on a CCD camera, and the second

technique visualized the oxidation front by electrically stimulating the device without metal contacts. The current drive in the device produced light that scattered off the edges of the oxidation front. This light illumination could be observed using the CCD camera setup. These visualization techniques are non-destructive, allowing further processing and usage of the devices analyzed. An 850 nm long pass filter is used for the IR CCD analysis. Since the CCD camera is made out of silicon, it detects wavelengths longer than 850 nm. The filter is placed in front of the light source of the microscope and the sample is viewed on a video monitor hooked up to the CCD camera. An IR image of a oxidized pill can be seen in Figure 4-14 b). With ambient light turned off and the contrast turned to its maximum, measurements can be made. The main problem with the IR technique is getting enough long wavelength light to obtain a bright image on the CCD camera. A brighter light source emitting heavily between 850 nm & 1000 nm could be used to improve this technique. Ideally an IR microscope could be used to obtain the images.

Luminescence measurements can also be used to observe the oxidation front. Current can be injected into the device without the need of metalized contacts. One 5 μm tipped probe is placed on the top of the upper mesa and another on the base of the mesa structure. Low levels of current are needed for the device to emit light. One to two miliamps can be applied, while the CCD camera hooked up to a microscope detects the emitted light from the device. The injected current can be adjusted to reduce the flare on the CRT due to excess light collected. At these low emission levels the light reflects off of the oxide aperture layer, illuminating the opaque oxide aperture area. Using this light emission the size of the aperture can be determined. An image obtained from this technique can be seen in Figure 4-14 c).

The trial oxidation is key to determining the time of oxidation. A reliable length measurement of the oxidation front must be made. However with the non-invasive top down methods of oxide visualization described in the previous paragraph, the slope of the wet etch can hide some length of the aperture. This slope will create a situation where the oxidation depth is underestimated. to avoid this, the mesa height of the test sample can be reduced. By decreasing the p- mirror height from 3 μm to

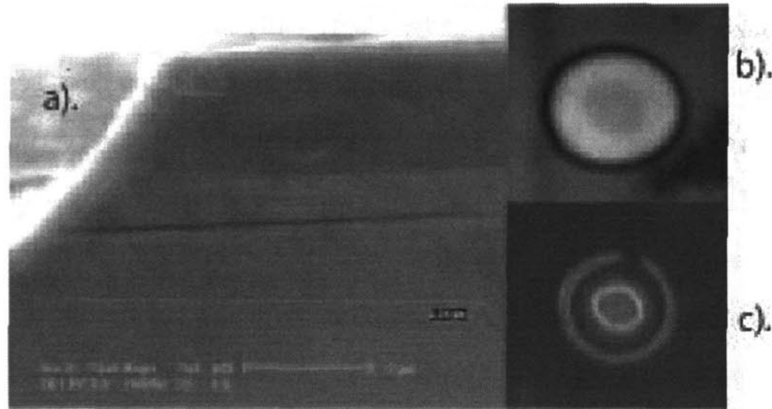


Figure 4-14: Wet Oxidation trials at 440 ^oC for 2 hours. Cleaved SEM (a), IR imaging (b), and luminescence techniques (c) are used to characterize oxidation.

.5 μm, the oxidation front using the non-invasive techniques are easier to see, and the slope at the edge of the mesa is less significant. In order to make such a sample from the same growth material, the AlGaAs mesa etch can be used without patterning. The mirror layers can be counted off and the etch is be stopped several layers before reaching the active region and the selective oxidation region. The same patterned mesa etch process can be used on the remaining p-type mirror to reveal the oxidation layer below. The diameter of this device and that of the actual device may vary, but a good rate can be obtained, which can be used for estimating the oxidation time of the primary sample. If oxidation does occur and the primary sample is under oxidized, it can be reinserted and oxidized further.

4.4.3 Oxidation Trials

Initial studies showed the oxidation technique as originally implemented was not consistent. There was a distribution of oxidized fronts running across a 1.2 cm piece. Aperture diameters varied by as much as 20 microns, with aperture length vary linearly across a substrate. To understand this problem single tier etched mesas were used, permitting a quicker processing transition between the mesa etch step and oxidation step, providing a clearer understanding of the variability in oxidation.

During the single tier pill trials, devices which were oxidized within one day of

mesa etching showed an even oxidation within the tier and across multiple devices on the surface of the sample. The oxidation time was also more consistent. There still were variations in threshold currents from mes to mesa (between 1ma-3ma) however ,suggesting an aperture size variation still existed. This remaining variation in most cases was found to be the direct result of the variation in mesa etch profiles of that device, due to the the non-ideal wet etch. The larger sized pills consistently exhibited larger threshold currents, as expected.

As stated in Section 4.4.2, the furnace temperature used was 455 ^{o}C controlled by a Eurotherm temperature controller, though separate tests showed the temperature of the furnace where the sample sits is 8 ^{o}C less than this, i.e. 447 ^{o}C. The nitrogen flow into the furnace was 1700 scmm, with the water bath temperature varying between 89 and 91 ^{o}C. Oxidation trials of single mesas with a 30 micron top diameter showed over oxidation after both 80 and 70 minute trials. A 15 μm opening after 55 minutes of oxidation was seen using the same oxidation conditions. The oxidation rate of the trials consistently showed a rate of around 0.3 μm a minute.

Sample reinsertion into the oxidation chamber can be used to adjust the aperture of the devices, allowing better control of the diameter, while preventing over oxidation in one long furnace run. The rate of the reinsertion oxidation is no longer linear from insertion, or at least does not exhibit the same oxidation rate for short oxidations. This is likely due to the time required for the oxidation chamber to equilibrate and for reactive gases to diffuse to the oxide semiconductor interface, creating an initial stage of no oxidation. A trial using a 15 min. reinsertion time resulted in around 1 - 2 μm of oxidation on each side of the aperture on samples that had been oxidized to a depth of 15 μm, which is typical of what is needed in this work. This rate is dependent on oxidation front depth and furnace time, creating a non-linear process. Consistency from subsequent runs on the same sample using the same oxidation time was seen. Reinsertion is vital to obtaining an aperture that can be accurately oxidized below 5 μm.

4.5 Metal Deposition and Patterning

Sputter deposition and sputter etch techniques were used in early pill processes [31], however in the present study a simple e-beam lift-off procedure has been used. Several alignment steps are required, due to the complex processing of the VCSEL pills, reducing the benefits of a self-aligned sputtering technique. Also lift-off became an option after it was determined that e-beam Ni deposition can be consistent if a chrome or titanium gettering cycle is preformed prior to Ni deposition and care is used during the Ni melt itself, though crucible cracking was still a common occurrence. Without these two steps Ni deposition was too unreliable for a process intensive device structure.

A basic metal stack was used to provide an ohmic contact to the p-type mirror of the device. The P-type metal stack used is Pt (65Å) Ti(500Å) Pt(500Å) Au(1300Å). The p-type contact is then annealed at 380 °C for 30 seconds. The contact that results is ohmic and relatively low resistance, on the order of $10^{-4}\Omega cm^2$. Figure 2-6 shows the results of the TLM contact study of the p-type contact system. The annealing step is done after both the n-type and p-type metalization steps have been completed.

A metal stack to provide an n-type ohmic contact to the n-type mirrors and a bonding surface was also developed. The n-type stack used from bottom to top was Ni(50Å) Au(100Å) Ge(500Å) Au(900Å) Ni(300Å) Au(1800Å). The top 1800Åof gold in the n-type layer is used as a bonding surface for the alloy with the AuSn bonding stack in Section 5.3.2. Once again the contact proved to be ohmic, but demonstrated relatively resistive characteristics as seen in Figure 4-15. The n-type contact was done on the n-type mirror stack which contained aluminum, which is not ideal for a good contact resistance. Measurement preformed on VCSEL devices still on their substrate used the n-type mirror contact and often showed high turn on voltages as a result. A procedure to produce a backside contact is described in Section 4.7. The backside metalization step contacts the GaAs buffer layer, while also being a wide area contact layer, producing constantly low contact resistance.

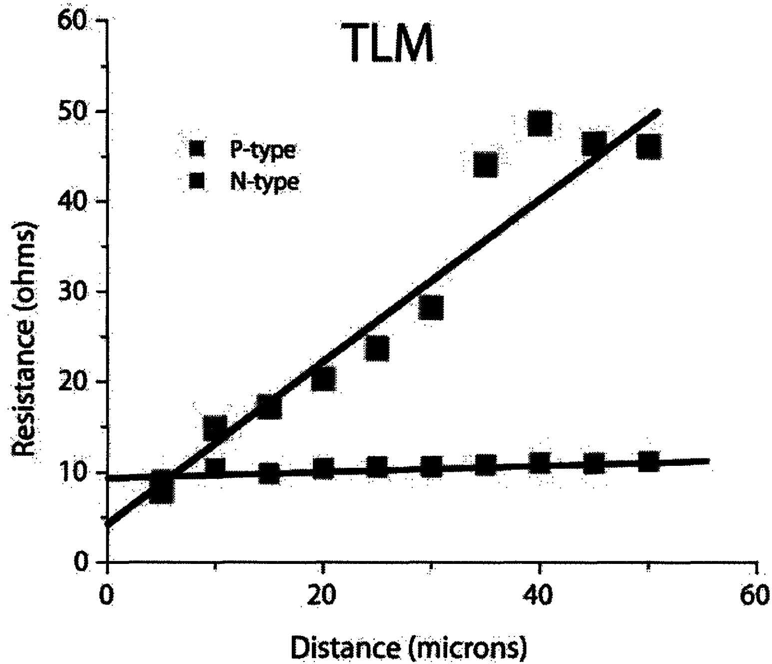


Figure 4-15: TLM measurement of P-type and N-type metal stacks used for ohmic metal contacts. The TLMs were not confined but showed the metals had decent contact resistances (p-type: 1.8610-4 ohm-cm^2; n-type: 3.7510-5 ohm-cm^2). The contacts also displayed good ohmic linearity.

4.6 Pill Release and Collection

After the semiconductor VCSEL pillars have been etched, oxidized, and metalized, the VCSEL devices are selectively removed from their substrate and stored in solution. The selective removal can be done by selectively etching away a thin layer of the heterostructure attaching the devices to the native substrate. One advantage to the undercut etch technique is the reuse of the substrate material. However, undercut techniques where substrates are immersed in etching materials were studied and several problems arose from such a process. The selective etch require immersion of several hours within solution to fully undercut and free the devices from their substrates. This long immersion tended to slowly etch the metal layers, though the metals used were thought to stand up to this etch. Collection of the pills in the acidic solution was also not an easy task. This undercut removal technique also prevents further processing of the pills after removal, specifically preventing the placement of a backside metal on the pills. The undercut removal technique deserves further in-

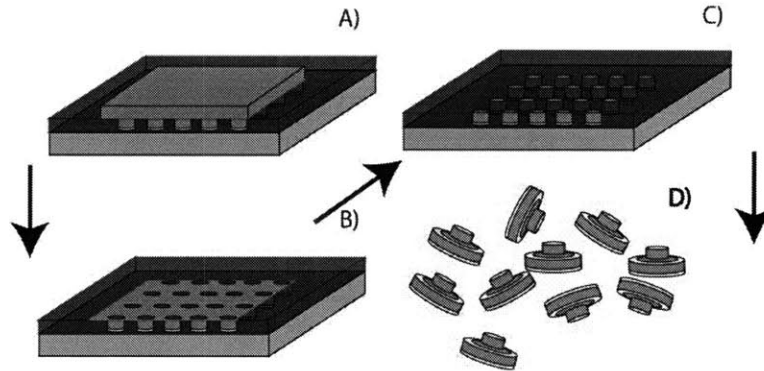


Figure 4-16: Pill release process flow. a) Devices protected in wax and attached to dummy substrate. b) Expose backside of substrate. c) Selectively etch to InGaP layer. d) Selectively remove InGaP layer. e) Dissolve polymer in solvent and store devices in IPA.

vestigation, however a simpler technique was devised. The main reason to use the undercut etch technique is to preserve the growth substrate, however the substrate cost is only a small fraction (20%- 30%) of total cost of an epitaxially grown VCSEL substrate, limiting the benefits of the undercut removal technique.

To avoid the problems inherent in the undercut approaches, an alternate backside substrate etch removal process was developed. A polymer is used to encase the VCSEL devices and attach the VCSEL material to a silicon dummy substrate, exposing the bottom of the GaAs substrate. In initial studies, black wax was used as the protective polymer, however Section 4.8 discusses an alternate polymer that was used in the process ultimately developed. The same solution of sulfuric acid, hydrogen peroxide and DI water used in tier etching was also used for removing the substrate, since the sulfuric is a GaAs etch that is highly selective to InGaP etch. This etch produces a mirror smooth InGaP surface, once the substrate is removed. After the InGaP layer is selectively removed from the pills, the black wax encasing the pills is dissolved using Trichloroethylene (TCE). The TCE solute containing the devices can be decanted into IPA, cleaning the pills through several steps. Significant numbers of pills can stick together due to undissolved black wax. This pill clumping has been shown to reduce the efficiency of fluidic assembly, however for pick and place assembly free pills can be chosen. The results of clumping of pills can be seen in Figure 4-17.

To avoid the clustering problems encountered when the pills are embedded directly

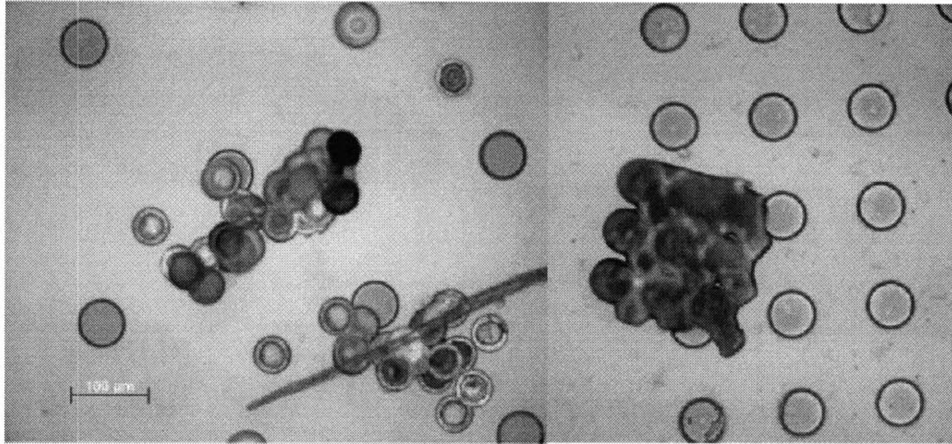


Figure 4-17: Released pills with polymer conglomeration

in black wax, a thick photo-resist layer can be spun onto the pillar face, as a first step prior to black wax encasement. This sample can then be placed face down in melted black wax. Once the native substrate's back has been etched back, the photo-resist can be selectively dissolved from the black wax using acetone and the pills released into solution. This technique showed the most promise in preventing clumping for fluidic assembly techniques. However, this photoresist layer can pose a problem during lift off steps of the backside metalization, which are discussed in Section 4.7. Section 4.8 describes trials using WaferBOND^{tm}[25] as the protective polymer coating, solving many of the problems associated with the use of black wax. This polymer proved to have the best characteristics of the polymers used in the trials.

4.7 Backside Metalization

Topside emission is a common arrangement for VCSEL growth, since the unetched surface producing an optically flat emission surface. A mesa etch can be preformed to place the n-type and p-type contacts on the top device of the device structure. However, most bonding techniques require metal on both surfaces that are being bonded, thus a metal layer needs to be placed on the bottom of the devices if it is to emit light out the top.. Magnetically assisted assembly also requires a Ni layer on the non-emission side of the VCSEL device, for the magnetic retention force to

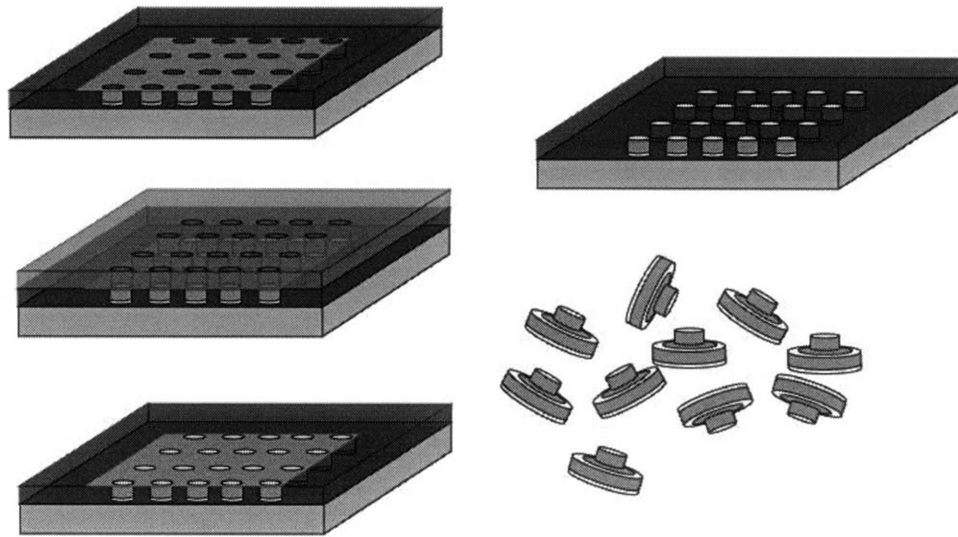


Figure 4-18: a) Black wax encases devices and fixes them onto a dummy wafer. b) Native substrate etch back. c) Photo patterning on thin film. d) InGaP wet etch removal. e) metal deposition. f) liftoff. g) pill release.

hold the VCSEL pill in place. A bottom emitting structure could be used, allowing this bonding metal to be place on the top of the device prior to substrate removal. However, the p-type contact would need to be placed after integration, reducing the alignment accuracy of this top p-type contact. To produce a bottom side contact, a post-substrate-removal metal deposition step was required. This section will discuss a backside metalization process using black wax as the cover polymer, while the following section will discuss the use of WaferBOND^{t}m [25] as the polymer coating and its advantages.

The surface that is to be bonded to the metal pad during integration is at the InGaP interface. InGaP makes a poor ohmic contact and thus the GaAs buffer layer just above it needs to be contacted. In order to do obtain this n-type contact, a metal layer needs to be placed and patterned on the bottom of the device after the substrate removal and before the embedding wax is dissolved. Black wax was used as an embedding wax in the initial studies, however the black wax process developed to produce these pills was relatively complicated. To maintain alignment and prevent wetting of the black wax on the semiconductor surfaces the InGaP layer is left on during photolithography for metalization liftoff. The black wax edge bead, that can be hundreds of microns in height and prevent contact alignment, is removed using a

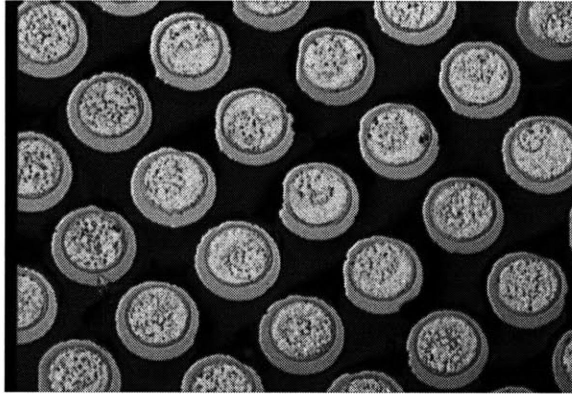


Figure 4-19: Pills embedded in black wax with metal on their backside

quick rinse in TCE, acetone, methanol, and IPA. Photoresist delaminates easily from InGaP and a way to ensure this stiction was required since the black wax backside metalization is a very sensitive process and continual stripping of photoresist had to be avoided. To enhance stiction of the resist to the InGaP layer, the substrate needs to be baked after the solvent clean prior to spinning. This bake is very important, and if possible the piece should be placed on the spinner while the sample is still cooling. The main problem associated with the use of black wax is that it softens with temperature and time, so the longer it stays on the hotplate trying to bake out the film, the more likely there will be misalignment of the pill due to migration.

The InGaP is selectively etched before metal deposition using HCl 50% DI 50%. A second selective etch is required to remove the remainder of the InGaP after lift-off is complete. This second InGaP etch can be hard to remove after liftoff. the cause of this removal problem is most likely due to polymer residue either from the black wax or the photolithography. An oxygen plasma has been used to treat this surface, resulting in full removal of the remaining InGaP during the HCl etch.

As described in Section 4.5 the metal stack placed on the back of the device is a series of ohmic contact layers and an Au cap preventing oxidation. The gold cap will alloy with the Au/Sn bonding layer to produce a soldered contact after heating.

Figure 4-20: Semiconductor remain after InGaP etch, due to unetched GaAs during tier etch.

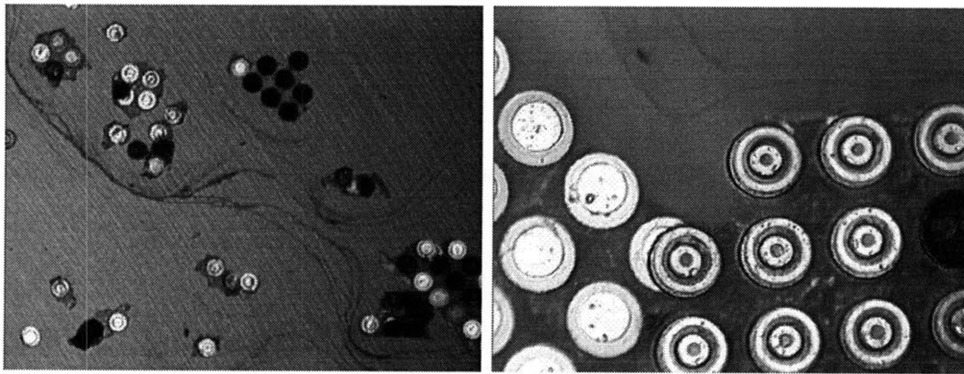


Figure 4-21: Black wax burnt residue producing a carbonized connective film between devices.

4.8 WaferBOND^{tm} Testing and Results

Black wax is not an ideal polymer for wafer removal, backside metalization, and pill release. Black wax is melted onto the dummy substrate and tends to produce large edge beads, that need to be removed. The wax also softens above 80 ^{o}C, leading to device migration during baking of the photoresist. Standard bake temperatures can be reduced, but lower bake temperatures are not a good fix. Black wax also has a tendency to dissolve a little and break apart in solvents, making photo processing more difficult. Black wax has will also leave a residue during release of the pills. Plasma etching of the black wax can burn the film as well, producing a non-dissolved connecting film between devices, as seen in Figure 4-21.

To avoid the black wax issues, a spin on bonding polymer from Brewer Science [25]

was used and compared to the black wax. The product is named WaferBOND^{tm}[25], and is design for substrate removal of III-Vs in MEMs applications. The polymer stands up to most III-V etches and is meant to be used in photo patterning applications. Thus the polymer stands up well to most solvents, including acetone, methanol, IPA, microstrip, and the resist remover 4 from Futurrex[23]. This section will discuss how this study processed with this material, and the following two subsections will discuss backside metalization and polymer cleaning respectively.

A simple spin is used to apply the polymer. 1.8 krpm for 30 seconds produces a film thickness of around 15 μm. The polymer is spun directly on the device wafer. The device wafer is then baked at a temperature between 100 and 150 ^oC for 1 to 2 minutes (2 minutes at 140 ^oC, was used in these trials). The device sample can then be bonded to a dummy silicon wafer. A bonding pressure and heating is needed for the polymer bond to cure. To provide temperature, the device bonding set up design by Mindy Tao and Prof. Fonstad [1] was used. A diagram of this setup can be seen in Figure 5-9, and its function is described in Section 5.3.1. The polymer side of the VCSEL sample is placed face side down on the silicon transfer chip, and a thick piece of aluminum foil is placed between the back of the III-V substrate and the thermal polymer of the bonding set up, preventing the sample from sticking to the thermal polymer. The chamber is then closed, flushed with forming gas, and then pressurized to produce a force of 50 PSI, pressing on the two chips to bond them. The samples are then brought to 160 ^oC for 8 minutes to cure the polymer bond. The trials found that the bonding set up provided the bonding force and temperature needed to cure the polymer bond. The processing of the WaferBOND^{tm}[25] material does call for a vacuum during the bonding of the two wafers, specifying between 1-15 PSI (15 PSI is 1 atm). The vacuum presumably prevents bubbles from forming in the film. Bubbles have been seen in the trials and evidence of them is shown in Figure 4-22. The bubble formation is concentrated in certain areas of the wafer constituting 10% - 20% of the total area of the WaferBOND^{tm}[25] surface. The pills within these areas still are bonded to the substitute wafer, even if there is no surounding WaferBOND^{tm}[25] material. There is still material on top of the pill

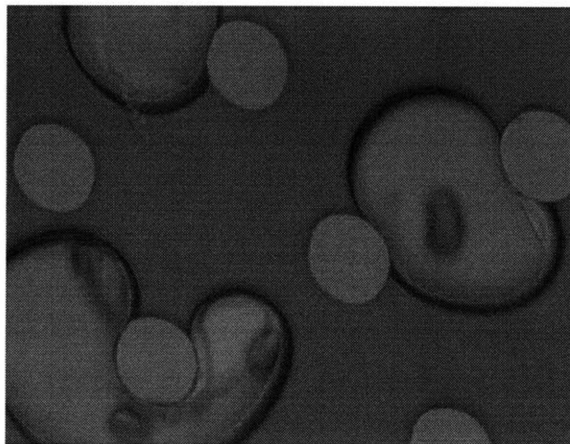


Figure 4-22: Pills Surrounded by WaferBOND^{tm}, with intermittent bubbles.

attaching the device to the wafer. Reducing the amount of gas by 1/10th would presumably reduce these bubble formation by the same amount, reducing the area of bubles to 1%- 2%.

The bonding chamber, seen in Figure 4-23, has a pump on the tail end of the exhaust lines. The chambers can be evacuated by shutting off the gas source lines and opening the exhausts lines to the chamber. Placing a vacuum on the inside chamber will pull the film down, possibly sealing and preventing gas from escaping the bond interface. However, the seal between the thermal polymer film and graphite bridge is not a perfect seal and enough gas escapes from the bond interface. A second option for the pumping scheme is to pump out both the inner chamber and the outer chamber, allowing the chambers to pump out without flexing the thermal polymer. The outer chamber can then be sealed off from the pump line and pressurized gas can be introduce providing the bonding pressure for the system. Bonding trials have been preformed using the vacuum pump stack, however there was a leak in the chamber at the thermocouple feed through, allowing air to be pulled in. Another issue with pumping out the inner chamber is that the thermocouple feed through is a teflon screw that tends to tighten under pressure. The tightening of the screw can twist the thermocouple line, increasing the possibility of shorting the thermocouple and preventing a good temperature reading. Further research needs to be done to determine how much an effect this evacuation process will have on the reduction of

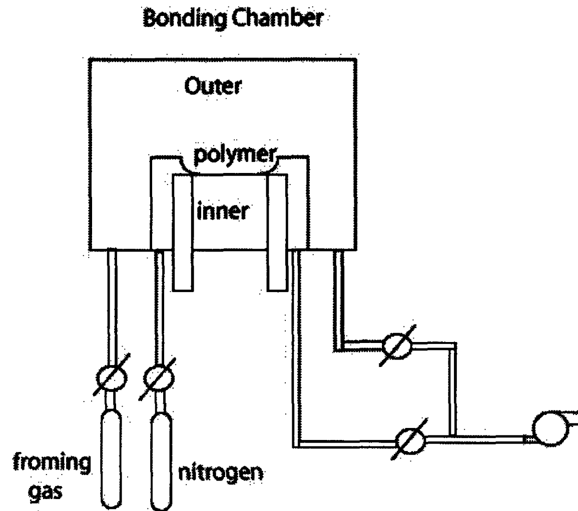


Figure 4-23: Schematic of Bonding chamber with pump stage

bubble formation. however, the bubbling issues do not seem to play a major factor in device yield.

Once the VCSEL device sample is bonded to their substitute wafer, residual WaferBOND^{tm}[25] needs to be cleaned off the substrate. This residual polymer prevents even etching during the substrate removal step, and can also create an edge bead around the pills, preventing contact lithography. The closer to the substrate that is to be patterned is to the photolithographic mask, the better the patterning. A maximum mask to substrate separation of 5 μm was used for the 60 μm bottom diameter pills and resulted in a patterning step that was consistent throughout the substrate. Larger separation produced smaller photoresist opening using the negative photoresist NR7 [23]. A 10 - 20 second dip in WaferBOND^{tm}[25] remover can provide enough edge bead reduction for the targeted patterning. The WaferBOND^{tm}[25] removal solvent is imiscible in water and the best way to remove the solvent from the substrate is to spray it off with the common degreasing treatment acetone/ methanol/ IPA. The substrate removal process is the same used in Section 4.6. After substrate etch back, another dip in WaferBOND^{tm}[25] remover can preformed, reducing the edge bead once more. However, this is only possible if the InGaP layer is still intact protecting the WaferBOND^{tm}[25] material underneath the InGaP during the solvent dip.

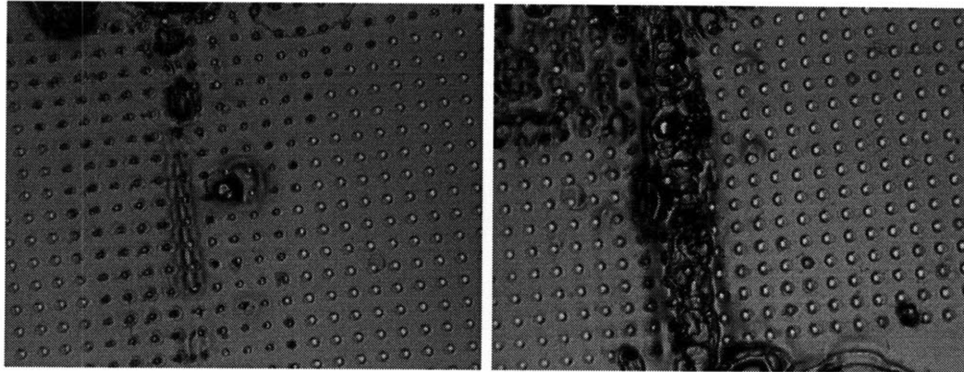


Figure 4-24: micropraphs of fissures in the WaferBOND^{tm}. Over etch pills are seen, and misalignment developed

During the etch back stage of a large 1 cm X 1cm substrate of single tier pills trial, two quickly etched areas were revealed. These etch lines revealed themselves as fully etched within the first hour of etch, the remainder of the substrate took 3- 4 hours of etching. These lines were most likely due to small cracks in the substrate. These cracks could have been produce by the contact alignment, and in retrospect there was a faint crack sound during alignment. These cracks could also have be caused during the pressuring of the wafer sandwich while in the bonding apparatus. These break lines not only created a quickly etch surface, which allowed etching through the InGaP, destroying the pills directly beneath those fissure, the cracks also produce misalignment between the pills affecting the backside metalization. The local pill to pill spacing was preserved, however across the wafer there was about a 50 μm shift in placement and a slight angle displacement between pills. These lines can be seen in Figure 4-24. These breaks highlight the fragility of the GaAs substrates. Care is needed during compressive steps to prevent small cracks from occurring.

When processing relatively large 1 cm X 1cm area substrate a problem occurs during the substrate removal step once the InGaP Layer is revealed. The InGaP layer is slowly etched by the sulfuric GaAs etch solution, and when the InGaP left exposed for an hour or more it will etch through the 300 nm layer, revealing the pills underneath. The InGaP protective layer etch through occurred during this study, though less than 10% of the pills were lost due to this problem. The InGaP would not etch through if the sulfuric etch uniformly removed the substrate, however the

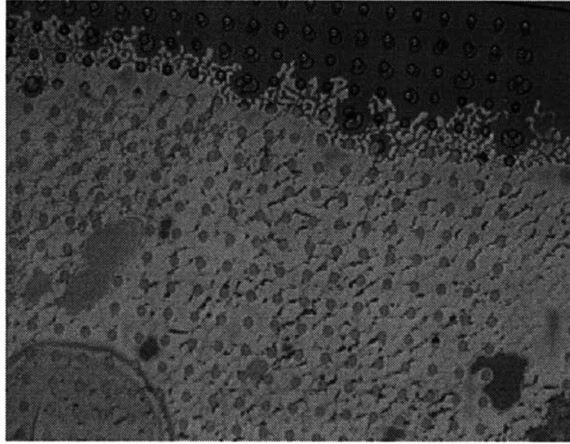


Figure 4-25: GaAs remaining after backside InGaP etch. This thin layer remains after being unetched during the tier etch.

etching of substrate occurred in a wave like pattern accross the substrate. It has been seen in multiple trials that the InGaP layer on one edge or corner is often revealed first, then a wavefront moves across the piece, finally removing all of the GaAs native substrate. It is necessary to remove all of the GaAs substrate since islands of unetched material can be hundreds of microns high, preventing unifrom contact during photolithography. Investigations into improving etch uniformity must be done when using this process techinique on larger size dies. Joe Rumpler has used stirring and placement techniques to improve etch uniformity [21], similar techniques could be done to improve the backside remvaol results.

Once the GaAs substrate is removed the InGaP layer is removed to reveal the GaAs pills below to enable metalization. Since the WaferBOND^{tm}[25] material is not dissolved in photoresist processing, it is best to remove all of the InGaP material before photolithography for liftoff. A simple 1:1 HCl DI water solution can be used and is selective to GaAs. However, there can be remaining non-patterned areas of GaAs bellow the InGaP due to a premature removal from etch solution during the device mesa etch. This premature removal can be a good option to preserve pill diameter, however the remaining thin layer GaAs has to be removed, and can be done using a RIE semiconductor etch. An example of this remaining film can be seen in Figure 4-25. The processing parameters for the GaAs RIE can be found in Appendix B.

4.8.1 Backside Metalization using WaferBOND^{tm}

Once the InGaP layer has been removed and the WaferBOND^{tm} surface holding the pills in place is planar a simple metalization liftoff process can be used to place the n-type ohmic contact on the backside of the pills. NR7 3000P [23] was used for the photoresist in this metalization lift-off process. The standard process for NR7 photoresist involves 2 hot plate bakes. The first involves baking the newly spun resist at 150 ^{o}C for 3 minutes. This step bakes out any remaining solvent within the film, reducing the photoresist's stickiness. If the film sticks to the mask the sample needs to be baked more for a longer time. The photoresist is then exposed using the high resolution aligner in EML, and a second bake takes place at 100 ^{o}C for 3 minutes. Standard processing parameters can be found in Appendix B. Though the specifications of the WaferBOND^{tm}[25] cite the film is resistant to temperatures up to 200 ^{o}C, movement in the polymer was observed at temperatures of 150 ^{o}C and some movement was seen at 125 ^{o}C. To keep the pill devices aligned for photolithography a 100°C hotplate bake was used, thus reducing the first bake to 100°C with an extended bake time of 5 minutes.

Once the sample is patterned, a quick oxygen plasma (5-15 minutes in the EML asher) can be used to clean the surface on the back of the VCSEL devices and a quick BOE dip can be used (5-10 seconds) to remove native oxide on the semiconductor. E-beam metalization is done and the same n-type Ni/Au/Ge/Au/Ni/Au metal stack is used as discussed in Section 4.5. To make these pills react to a magnetic film, the last of these Ni films in the contact was thickened to 200 nm.

4.8.2 WaferBOND^{tm} Polymer Cleaning

To remove the pills from the embedding WaferBOND^{tm}[25] on the Si dummy substrate, the WaferBOND^{tm} remover can be sprayed on using a pipette. The result remover solution which contains pills is collected using a vial. The standard cleaning procedure involves heating the solution and sonicating it. Moving the pills into a fresh solution of remover, than decanted into IPA. The decanting of the pills can be

preformed several times to clean the pills and the solution. This is done by letting the pills fall to the bottom, removing the solution on top, mixing, and wait for the pills to fall to the bottom. Pill decanting has been common in study, however sonication was introduced to the first trial. The resulting pills were clean, but a lot of the devices showed damage. Many of them were cracked in half, this damage was attributed to the sonication step and this sonication step was removed from the free pill processing steps.

4.9 Clumping

Once removed from the WaferBOND^{tm}[25] polymer, the VCSEL devices remain in solution. The first runs using this WaferBOND^{tm}[25] technique, clumping of devices occurred. It is clear the conglomeration of pill devices occurs during the test tube stage of the processing. It is also possible that the drying of the pills from their IPA solution on a glass slide could also promote clumping. It could be due to residual polymer or to static electric forces that can be important at these sizes. The root of this clumping remains unclear, and further trials using WaferBOND^{tm} [25] need to be done to reduce the impact of this adhesion.

A change in removal technique may be called for. Joe Rumpler has developed a technique with his in-plane laser microcleaved devices that could solve these issues. A teflon wafer is placed in remover. The handle wafer with pills embedded in wafer bond is then place face down. The wafer bond is dissolved and the pills fall onto the teflon substrate. This technique, however, is aided by the use of a sonicator [32]. A second process that may reduce clumping is to oxygen plasma the wafer bond material down to the handle wafer, removing the connecting material between pills. However the oxygen plasma his may create a carbonized film connecting the devices as seen previously in Figure 4-21.

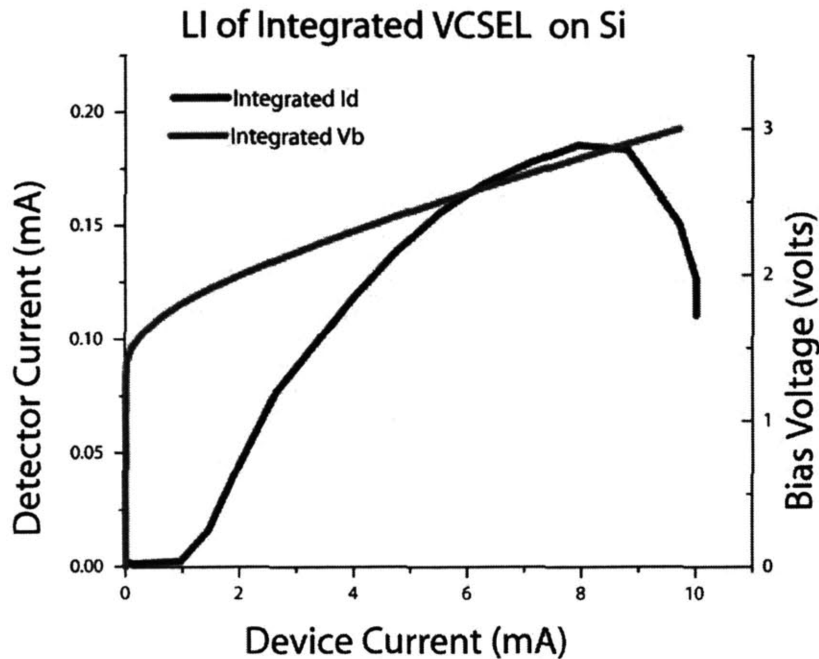


Figure 4-26: LI curve of two tier VCSEL integrated on Si with threshold currents of 1ma.

4.10 VCSEL Pill Results

This research sought to produce free standing, substrate independent micro-VCSELs. The purpose was to obtain devices that could be placed where ever a vertical lasing device was needed. This goal was accomplished. VCSEL pill device produced good electrical thermal and optical properties, and showed the versatility of such a device. Following is a brief summary of observations of the devices fabricated using the preceding technique. Full analysis of these pills can be found in Chapter 6.

The two-tiered VCSEL pill structures produced exhibit the designed structure. The two-tiered VCSELs exhibited low resistive ohmic contacts with light emission greater than .5 mW. These VCSEL pills were the first free standing lasers made in this study. Figure 4-26 shows the LI curve of a 1 ma threshold two-tier device bonded onto Si.

There were some notable drawback to the two-tier structure design. The second tier of the device structure was found to be unnecessary once a reliable technique

for backside metalization was developed. The second tier added size to the device and the contact pad on this second tier was highly resistive, since the metalization occurred on an AlGaAs mirror layer as opposed to a pure GaAs buffer layer. The 2nd tier layer could be used for probing the top side, however probing the 2nd tier could damage the pill. The application of pressure from the metal probe not at the center of the device during characterization often led to cleaving of the device along the 2nd tier. This is possibly due to thinness of 2nd tier layer, or due to the imbalance of load on the edge of the device. The VCSEL devices could be safely characterized by probing a metallic surface on which the VCSEL pill sat, allowing the bottom contact to be connected through the metal surface it was placed on.

The size of this second tier also doubled the diameter of this device from 45 μm to 90 μm in diameter, increasing the wafer area consumed by these devices four-fold. The 2nd tier increased the number of wet etch steps and increased the number of metalizations of this device. The second tier was also below the surface of contact alignment decreasing the reliability of these processing steps. The increased number of processing steps also increased the probability of destroying the devices.

The two tiered device had a more subtle drawback as well. Wet oxidation of these device was unreliable and resulted in about only about 10% of the devices produced having the desired threshold currents. During oxidation trials of the using single tier devices it was observed that oxidation of devices within 24 hours of etching their mesas improved the controlability and the uniformity of the oxidized layer. This 24 hour processing limit could not be done using the two tier structure. The two-tier devices required the first tier to be etched, photoresist had to be stripped and the second tier had to be made before oxidation. Both tier had to be etched before oxidation since this oxidation process step produced a surface that could not be etched unifromly with the sulfuric mesa etch. The two tier mesa proccessing steps added time and the possibility of non-uniform exposure to the wet etch during the second tier etch. The 24 hour time depedance window of the oxidatation process may be the result of the oxide aperture layer being exposed to ambient air, producing a native oxide on the high percentage alumiun aperture layer. This growth may not be uniform and can

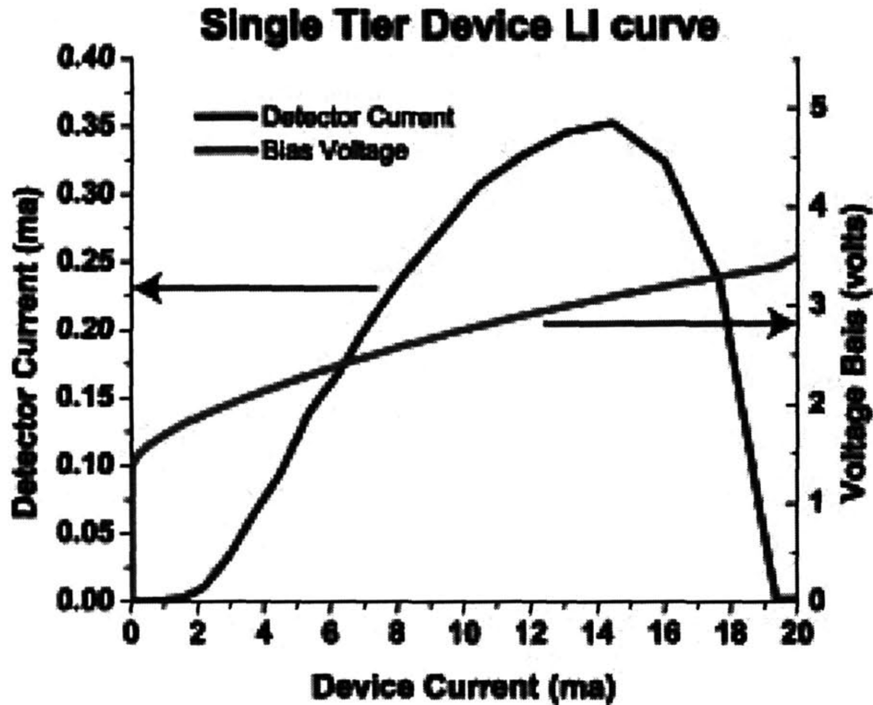


Figure 4-27: LI curve of single tier VCSEL integrated on chip with threshold current of 2 ma.

inhibit the growth of the oxide aperture. It has been reported that a BOE dip can remove the native oxide on the aperture layer, and can promote even oxide growth for samples sitting in ambient [27]. Trials using this technique were showed when the sample is dip in BOE for a minute pieces of material begin delaminating from the sidewalls of the VCSEL device, introducing more non-uniformity within the device.

Single tier devices had a much better yield and almost every device in this trial tested worked with a threshold from 1- 5 ma. The few non-functioning pills were mainly a result of lithography errors. The single tier devices were from 30 - 35 μm in diameter on top and around 50 microns in diameter on the bottom. The shaped etched by the wet etch tended to be oval. Most of the discrepancy in threshold current could be attributed to shape difference. An increase in the pill top diameter produced a increased the threshold current device.

The most variation in the processing of the single tier devices was seen in the backside metalization. As discussed in Section 4.8, during alignment of the photolithographic step of backside lift-off metalization, the pills were found to be skewed

across a fault line, the same line which etched quickly during the substrate removal step. The cause of this fault line was apparently a crack caused during the bonding, under 50 psi of pressure, of the GaAs substrate to the Si handle wafer using the WaferBOND^{tm}. This crack prevented good alignment of all of the pills during backside metalization.

4.11 Pill Processing Improvements

There are a few minor changes that can improve the yield of the devices produced and the yield of the growth heterostructure, while also decreasing the variance in the threshold currents. Firstly, a dependable and smooth reactive ion etch (RIE) process needs to be developed in the MTL facilities to reduce the undercut and the cone shape of the devices produced in these trials. A RIE would enable a more regular shape to the device. The regular shape would reduce the variance in diameter, resulting in better control over the threshold current of the devices. The reduced undercut would enable a smaller mask circle to pattern the same size device, enabling a closer mask spacing between devices, increasing the number of pill made per unit area of heterostructure. The GaAs reactive ion etch would have to have a reliable etch rate and be able to stop in InGaP. A process where a wet etch was used only to selectively etch the last part of the structure could also be used. GaAs RIE are common and can be reliable, however the tools available in MTL have not shown the ability to produce these etches. Dedicated etchers tend to reduce chamber contamination, however this tends not to be possible in shared facilities such as MTL.

Currently the spacing between the devices is 135μm, since the same mask set for the single tier devices were used for the two tier device. However a spacing of 45 μm could be used if a low undercut etch was found, increasing the number of pills per square millimeter from 55 to 493. If the spacing were optimized to a honeycomb like spacing the yield could be increased to 570 pills per square millimeter. The honeycomb pattern spacing would increase the amount of heterostructure used from 5.29% to 54%. The honeycomb calculation includes a minimum 10μm spacing between pills.

The amount of pills for a single 1 cm^2 area would be 57,000, up from 5,500.

The backside substrate removal process also needs improvements. Currently the H_2SO_4 / H_2O_2/ H_2O etch tends to etch unevenly in a wave across the surface, causing areas of InGaP to be exposed for long periods of time to the GaAs, eventually etching and destroying some of the pills below. Simply increasing the etch stop layer from 300nm to 600 nm will increase the amount of time this layer will stand up. However, changing the wet etch condition as discussed in Section 4.8 may also improve uniformity of the etch. An initial backside grind would decrease the thickness of the substrate, thus reducing time and variation in the etch. However, there have been reports that this sort of backside grind can induce fracture within the oxide apertures of the VCSELS.

Clumping of the devices is still a major issue, one that needs to be solved in order for fluidic type assembly to occur. The causes of this conglomeration need to be determined, whether the clumping is due to residual polymer or simply static electric forces on the pills surfaces. It must be determined whether cleaning and storing these devices in a test tube promotes clumping and whether drying of these devices out of IPA on a glass slides exacerbates the issue, making clumping appear to be more of an issue than it is. If pill clumping can be reduced, pills would be free to flow, and trials have been shown that fluidic assembly occurs much more readily.

Chapter 5

Device Integration Implementation

Individual VCSEL devices pills, once released, are ready for integration. In order to obtain a fully integrated chip with silicon MOSFETs and AlGaAs VCSELs, the target circuit has to be prepared for device insertion. The target IC preparation is done by forming a recess into the dielectric stack, opening up a contact pad connected to the IC. Bonding metal is patterned on the pad at the bottom of the recess and a VCSEL pill is put into the well. The pill is then bonded in the recess and a spin-on dielectric is used to planerize and cover over the device. Openings in IC dielectric are then etched and the final contact metal is deposited and patterned, connecting the top of the VCSEL to the rest of the circuit. Section 5.1 discusses the processing to form the recesses on the IC. Section 5.2 discusses pick and place assembly, while Section 5.3 discusses the bonding of these devices. The final two Sections (5.4& 5.5) discuss post assembly processing and the results obtained in these experiments.

5.1 Recesses on Integrated Circuits

A well is etched into the dielectric layer on top of an Aluminum contact pad. For initial studies a 250 nm Al layer was deposited on Si with a 3 micron SiO_2 layer on top. The SiO_2 oxide recess roughly simulated the integrated circuit Professor Warde's group developed, however the actual dielectric proved to be more challenging. Initially a single SF_6 reactive ion etch was used in an attempt to etch down to the contact pad

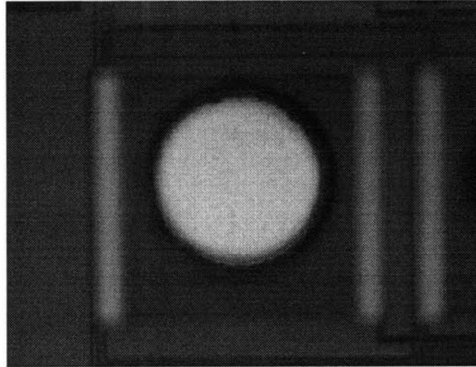


Figure 5-1: Etched well in an IC down to an aluminum pad using SF_6 and Silox Vapox.

of the IC, however the RIE stopped midway in the dielectric. The remainder of the dielectric could only be etched using a wet Silox Vapox etch. Silox Vapox can not be used to etch the entire stack however, because the first layer on the IC is resistant to this etch. Thus a sequence of several etchants is needed to produce the integration recess on the IC.

A single layer of NR7 3000P [23] photoresist spun to a thickness of 3 μm can be used to mask the chip for the two etch steps. The NR7 allows for better alignment, since the negative mask allows the sides of the contact area to be seen during alignment. SF_6 can be used to etch the recess for the first 20 minutes, and Silox Vapox can be used to etch down to the target metal layer. The silox vapox etch takes up to 40 minutes and exhibits characteristics seen from photo-micrographs in Figure 5-2. The Silox Vapox reaches a brown cover layer on the aluminum that the wet etch can not remove. After the Silox Vapox wet etch, a quick 5 minute SF_6 can be preformed to reveal the underlying aluminum layer seen in Figure 5-1.

Since a wet etch was used to etch much of the recess, at least 5 microns between the recess and the side contact metalization is needed to prevent damaging side contacts on the IC. The initial space provides by the chip was 95 micron, however the two-tier devices were at least 90 μm in diameter and the recess opening for these diameter pills would undercut into the side contact. The spacing was not a problem when the single tier pills were introduced, a much smaller radius recess could be used. Figure 5-5 is a schematic of the targeted contacts on the target IC substrate.

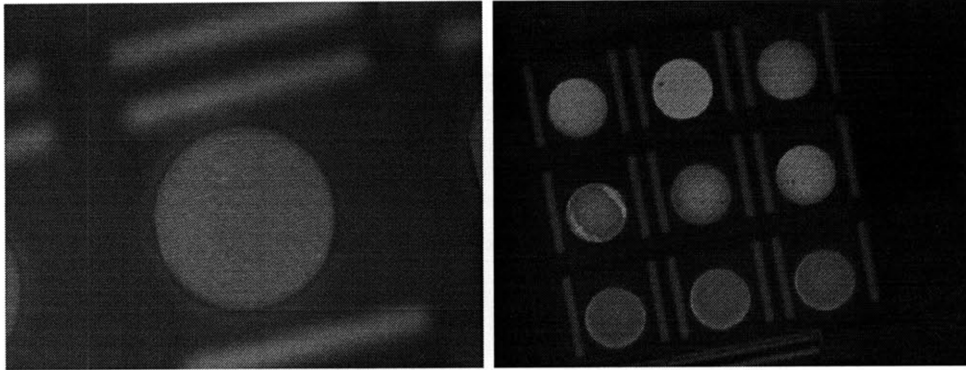


Figure 5-2: Silox Vapox can remove the last remained of material. Above are the last stage of recess opening. Color changes until etch is stopped just above the Al layer, seen in above figure.

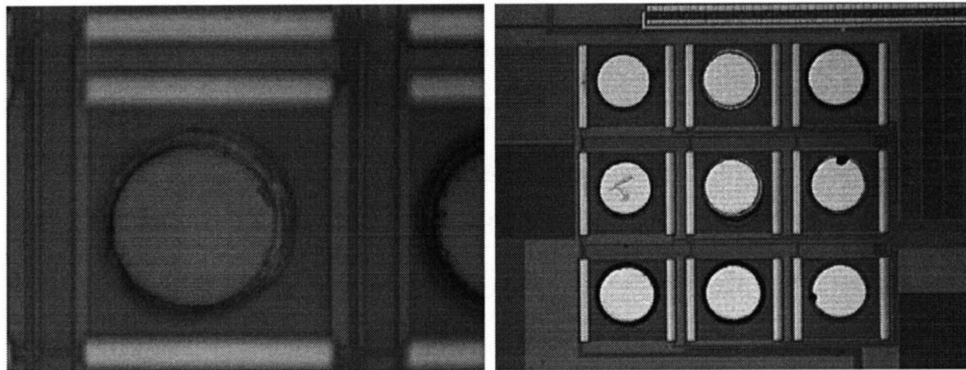


Figure 5-3: Brown film Silox vapox etch stops on. open recesses, Al layer revealed.

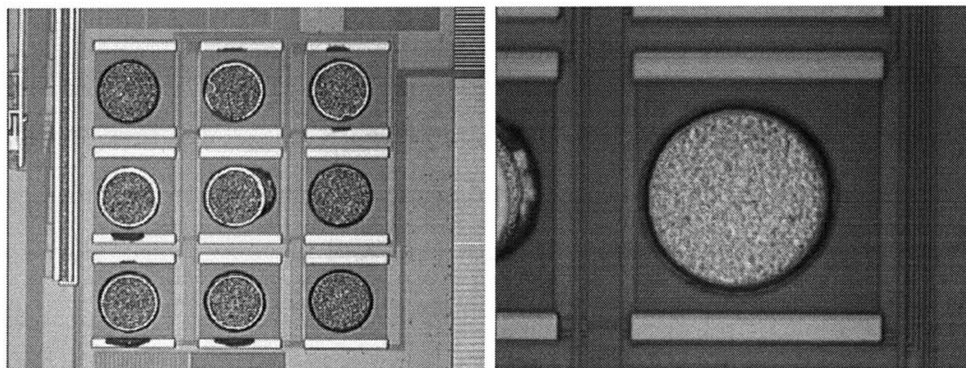


Figure 5-4: 500 nm of indium on aluminum within the chip recess.

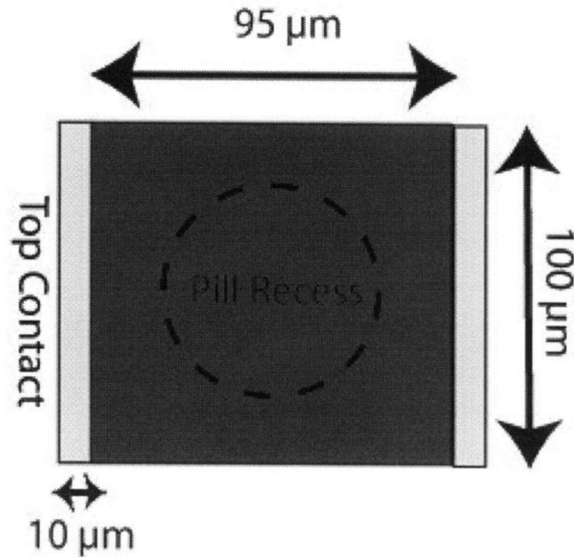


Figure 5-5: Schematic of recess dimensions

Once the recess is opened up, the bonding layer is deposited and patterned using liftoff. The first metal stack used from bottom to top was an Al/Pt/Au/Sn/Au (10/5/18/65/21) nm. This bonding metal alloys with the 180nm of gold on the bonding surface of the VCSEL device pills. Further trials used much thicker metalization. Indium was used at a thickness of 500 nm, while one trial used a Cr/Au/Sn/Au stack(100/300/110/50) nm. The bonding results from these films are described in Section 5.3.2.

5.2 Device Assembly using Pick and Place

Pick and place assembly has been used in this research to place individual devices onto Si substrate and within recesses. The pick and place technique was first developed by Mindy Tao and Prof. Fonstad [1]. Pick and place technique uses a micro-pipette to manually select and place individual devices. Pick and place assembly allows precise control of what devices are used and how finely they are placed, making it an ideal technique for initial study of device and integration operation. However pick and place technique suffers from its inherent lack of parallelism, making extension of the technique to large arrays of pills impractical. None the less, a 3X3 array could be

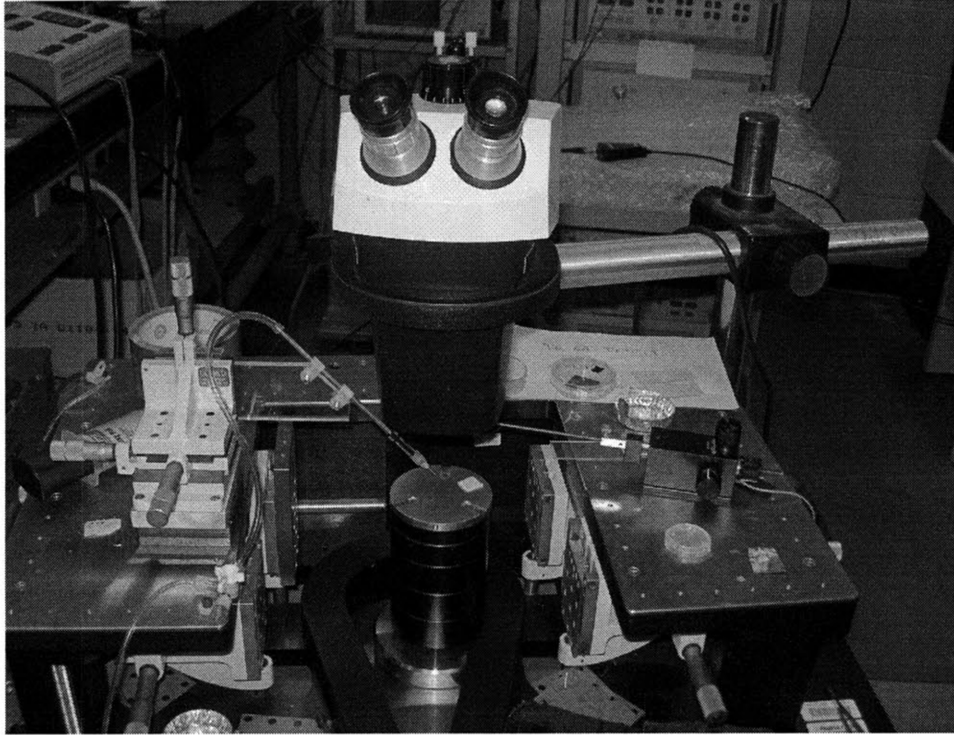


Figure 5-6: Pick and place apparatus, showing microscope, probe tip, wafer chuck, tip manipulator, and vacuum line.

assembled in less than an hour using pick and place technique. The next subsection will discuss the pick and place apparatus, and this section will be followed by a discussion of the assembly technique in practice.

5.2.1 Pick and Place Apparatus

The pick and place apparatus was developed at MIT Professor Fonstad's lab [1]. A glass pipette is used as the pick up tool for the pill devices. Often pipettes like the one used in a pick and place are used in micro-biology for cell manipulation. The micro-pipettes are tapered down at the end to a diameter of 30μm and the end is beveled to a 45° angle. The micro-pipettes are paced on an x-y-z micromanipulator stage and hooked up to a vacuum line with an on/off valve. The vacuum turns on and off the suction of the tip of the manipulator. Figure 5-6 shows a schematic of the pick and place apparatus.

The pipette holder and manipulator combination were retro-fitted onto a probe

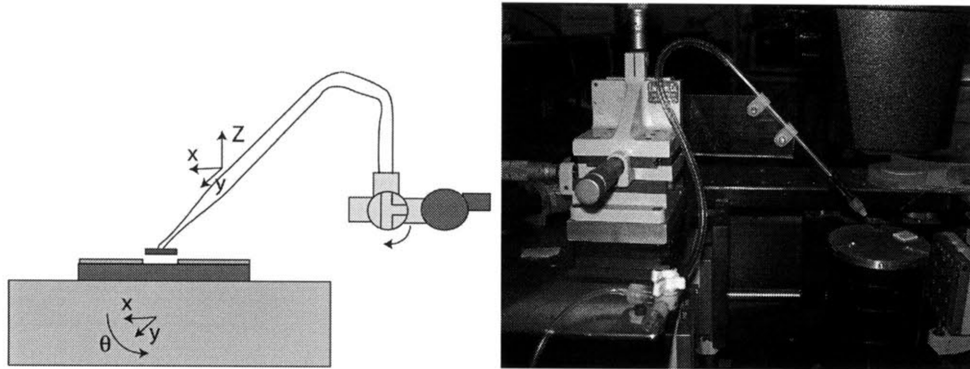


Figure 5-7: Schematic and picture of pick and place setup. The micro-pipette, vacuum lines,and micro-manipulator are shown

station. The pipette tip is fixed above a movable chuck, on which the target recess sample and the pill devices themselves are placed. By moving this chuck back and forth individual pill devices can be ferried to their target recess location. This chuck sits unmounted on a platform base and is moved and rotated by hand. The finer movements needed in assembly are made using their micro manipulator. Above the chuck and probe tip is a microscope looking down onto the pipette and chuck. The microscope allows the user to view, select, and manipulate the devices below.

The pipette tip is very fragile and can easily be broken if care is not taken. Most commonly a break occurs when the pipette is lowered too far onto the substrate, though the pipette is very flexible and will bend to a certain degree. Additionally, when sliding the chuck below the pipette, care must be taken. In normal operations the chuck moves with some resistance, and if it is moved with too much force, the chuck can tilt and raise ruining the tip that is above. When replacing a probe tip, it is easy to break the new probe tip, thus insertion and alignment of the tip must be done with the pipette raised well above the chuck surface.

The probe tip flat must be aligned parallel to the chuck. The pipette tip alignment can be done, with practice, using the probe station. After placing the probe in the holder on the manipulator stage, the micro-pipette's radial orientation needs to be set. By changing the field of view and magnification of the microscope onto the tip of the pipette, the oval opening of the pipette end can be seen. The aluminum chassis attached to the micro-pipette can the be rotated until the outline of the opening is

symmetric and facing down. The pick and place set up is such that the pipette can be rotated, but remains in place by friction. Every time the pipette is changed the rotation needs to be properly adjusted.

5.2.2 Pick and Place Assembly

The pill devices are removed from their vial solution of isopropanol using a standard chemistry pipette. The solution and pills are placed on a glass slide, where the isopropanol either is left to evaporate, or blown off. Blowing off the solution can result in some loss of pills while leaving the solution to evaporate can leave a residual film on the devices.

Once on a glass slide, the VCSEL devices can be picked up using the micro-pipette tool. The main concern when dealing with these pill structures are static electric forces. Keeping devices in a plastic insulating box, the VCSEL pills will have a tendency to move off of their glass slide or out of the recesses. Transporting them in aluminum dishes works well when dealing with prebonded pills, however major vibration can shake the devices out of their recesses as well. A fresh micro-pipette right out of the box also can have static electric built up that can impede the placement process. The static electric build up on the pipette is usually reduced after some time out of the probe tip box.

The VCSEL pills can be picked up by the probe tip by placing the flat surface of the pipette tip on the top of the pill. The pipette tends not break the pill due to its flexibility. Once the pipette is on the device, the vacuum is switched on and the device can be lifted, aligned and inserted in the recesses. Alignment can be difficult, it is hard to tell whether the pill is seated within the recess well due to the magnification of the setup. The maximum magnification of the set up is 7X, not good enough to see that fine of a resolution. However, a large working distance is needed such that the micro-pipette move beneath the microscope , so only certain magnification can be used. Using the pipette, the pills can be slid within the recess to make sure they are seated well within, however if the recess size and pill size are too close, it take time to fit these pill devices within the recess, and it is difficult to tell whether they

are situated flat within the recess. The pill fit within the recess was the major issue with the wide two-tier pill studies. The trials involving these two-tier pills resulted in a reducting of bond strength and thermal stability. Decreasing the size of the pills improved bonding yields from less than 40% to around 80%.

Micro-pipette Usage

The pick and place set up can be used to not only move individual devices, but pill devices can be flipped as well. The pipette can be placed touching the glass slide next to the device while the chuck is being moved, pushing the device into the pipette tip. The pipette is then raised during this movement, getting the pipette underneath the edge of the device, tilting it on end. While still gently moving the chuck, the tilted bottom edge of the device can be placed in contact with the chuck, twisting the pill device further until it has flipped over. The pipette tip can then flatten the pill to the substrate and the other side of the pill can be seen. Static electric forces can dominate when trying to flip these small devices, flinging the pill a couple millimeters, so trial, error, and patience are needed.

Static electric forces can also adhere the pills to the pipette and each other. If devices become attached to the micro-pipette, the pipette can be dragged against a surface to remove the devices. A second metallic probed tip was used for cleaning purposes. Once the metal probe is within the same plane as the pipette, the pipette tip can be dragged along the edge of the metallic probe, cleaning the pipette. The pills can also be found in clumps. The pipette can be dragged through the clumped regions freeing some pills, enabling their use in assembly.

In early pill production, the yield of the devices was low. About 20% of devices displayed reasonable thresholds. This device variation could not be determined by observin the device appearance. The two-tier devices needed to be probed before they were inserted into the chip recess. Preselection of two-toer devices was done using the probe setup to ensure good device integration. Pills were selected using the micro-pipette and lined up on the metallitc chuck of the probe station. The chuck provided a reasonable thermal sink. Most pills could be driven to 10 milliamps

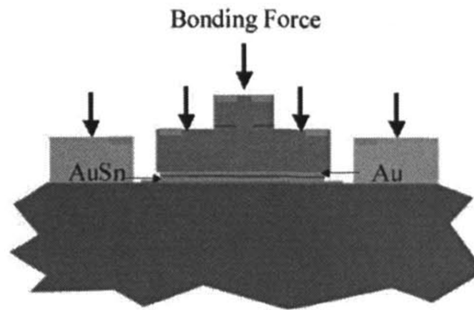


Figure 5-8: Bonding Force

before thermal heating quenched light output. Within this drive window, the well appertured devices, displaying a threshold below 5 mA, could be selected. The low threshold devices then could be integrated and bonded intothe IC.

5.3 Bonding

Once the devices are assembled within the recess, they need to be mechanically and electrically connected to the IC. The bonding metal processed within the recess enables this, however both a heat treatment and bonding force is required to achieve a significant and dependable bond. In the case of wafer-to-wafer or chip-to-chip bonding this is done with conventional bonder that places pressure on the wafers using flat metal plates, while also heating the devices up to the bonding temperature. The surface of IC in these experiments are not flat due to the height difference between the pills and the actual IC. A apparatus was needed to place a conformal force on the devices for bonding. A unique bonder was developed at in Prof. Fonstad's laboratory at M.I.T. to obtain the conformal bonding force. The following subsection will go into detail about the bonding apparatus used for bonding. Bonding experiments will be discussed in Subsection 5.3.2 and improvements will be discussed in Subsection 5.3.3.

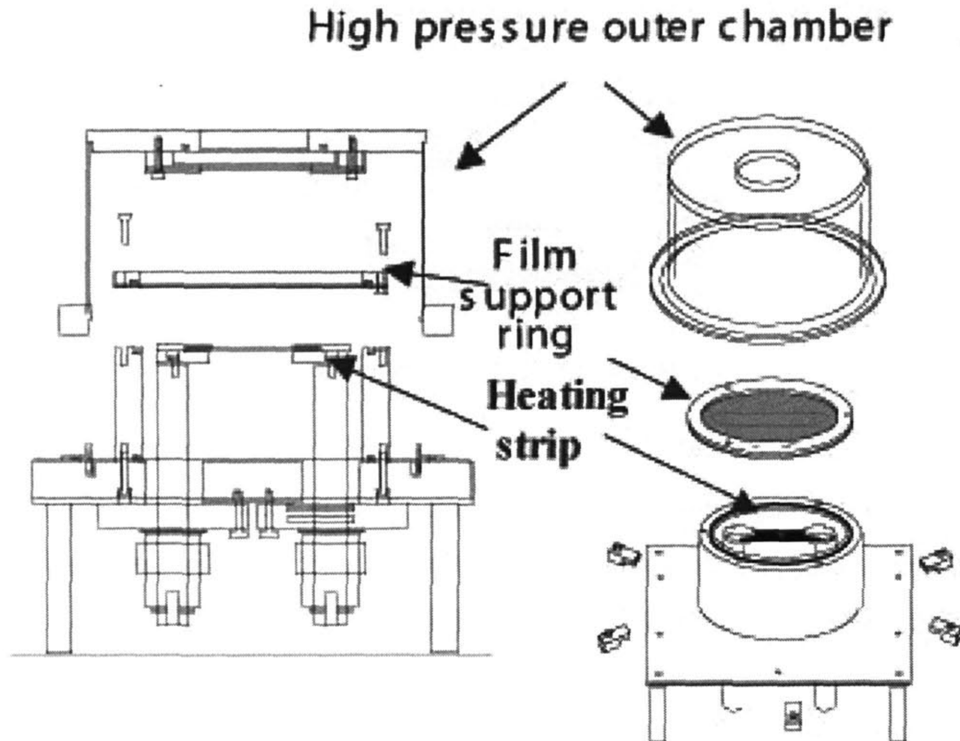


Figure 5-9: Bonding chamber

5.3.1 Bonding Apparatus

A bonding setup has been developed at M.I.T. [1] to obtain the conformal force and heat needed for uniform bonding. A graphite strip rapidly heats the sample while a polymer film presses down to provide the compressive force needed in bonding. The polymer bonding film is conformal, allowing pressure to be placed on pills within the wells. Jokerst et al. used a similar polymer film as a transfer wafer for bonding devices onto ICs [33]. Both a Au/Sn and an Indium solder bond is used in the experiments in this study.

Figure 5-9 shows a diagram of the conformal bonding apparatus. To heat the sample a graphite strip is used. When current passes through the strip the resistance of the graphite heats the area. This heating strip is suspended like a bridge by two metal post contact leads, supplying the current from the power supply. A thermocouple is attached to the bottom of the heating strip to read and control the temperature of the strip.

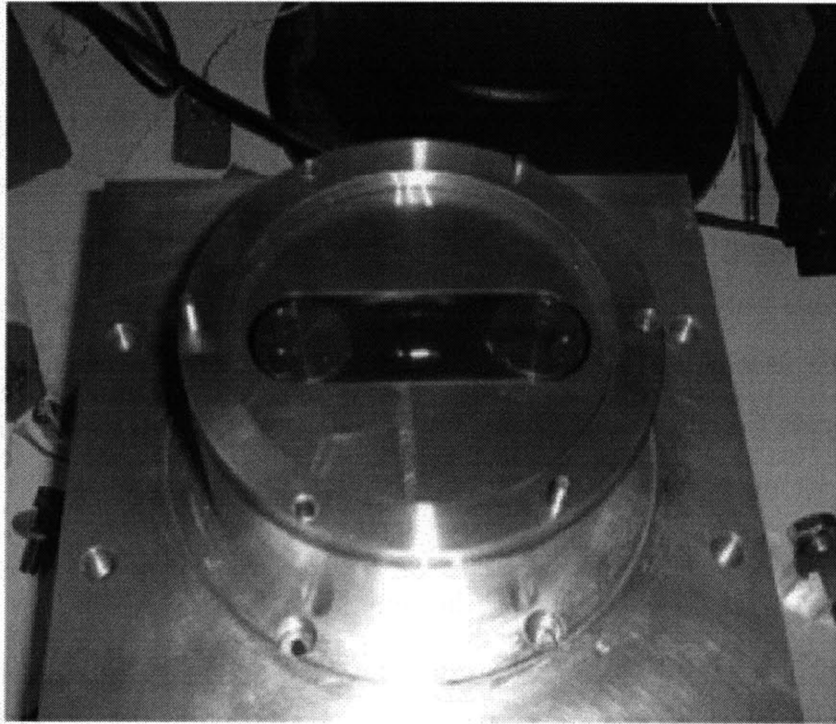


Figure 5-10: Picture showing inner chamber of bonding apparatus with thermal polymer cover.

The heating strip is in a vulnerable position. A pressure of up to 50 PSI is placed on the strip to supply the bonding pressure, and since the strip is only supported at the two ends, the graphite is susceptible to bending and breaking. Reinforcing this strip is necessary for proper bonding. As a first pass ceramic strips were cut and placed below the strip, with a hole cut out in the middle for the thermocouple to be placed. The ceramic was very brittle and cracked under load, suddenly placing all the load on the graphite heating strip, which then broke. A thick aluminum sheet was cut out to help cut down on the load, and once again a hole was drilled in the middle of the strip to provide for thermocouple access. The ceramic strips were added between the graphite strip and the aluminum to prevent current from running through the aluminum. Ceramic insulators were also used on the bottom of the aluminum to prevent the aluminum support from electrical contacting the metal posts. An ohmmeter is needed to insure an open circuit between the aluminum slab and the power circuitry. Lastly the clamps on the metal posts needed shims to obtain

a flat contact between the clamps and the graphite strip when clamps are screwed down. Broken pieces of ceramic and graphite were used as the shims, but care must be take to make sure these shims do not contact the aluminum metal support slab.

This entire bridge system is contained in an inner chamber, which was topped off and sealed by a thin aluminum plate with a hole cut above the strip. Above this hole the thermal polymer is placed. This hole allows the thermal polymer to press down onto the heating strip, but the aluminum sheet prevents the entire pressure load of the outer chamber to be placed on the heating strip. The inner chamber in the bonding set up is sealed with a series of rubber o-rings. The inner chamber is shown in Figure 5-10.

Care must be taken when placing the aluminum/polymer cover over the inner chamber. The cutout in the aluminum must clear the entire bridge. When screwed down, the aluminum layer can below the graphite and there is little tolerance in the spacing of this system. Some alignment of the strip to the metal overhang is required. Any secondary pieces of graphite and ceramic must also be tucked in to avoid contact to the aluminum overhang. The overhang will crack anything it contacts during sealing and during pressurization.

The apparatus also has a sealed outer chamber that surrounds the inner chamber. This outer chamber is to be pressurized, expanding the thermal polymer onto the heating strip, placing the conformal bonding pressure needed on the target sample for bonding. This outer chamber is screwed down to the chassis tightly, compressing its rubber o-ring. If the screws are too loose the o-ring can pop free while the chamber is under pressure, decompressing the chamber. The fixture keeping the o-ring in place can be easily reclamped by hand, if the o-ring does pop free.

Two sets of gas lines enter and exit the two chambers. The outer chamber is hooked up to a pressure regulator on the nitrogen line. This pressure regulator enables the selection of bonding pressure used. The exit gas line of the chamber leads to a pump line. The inner chamber also leads to a regulator and a tank of forming gas (95% nitrogen 5% hydrogen). A regular flow of forming gas is supplied to the chamber while in use above 100°C. The exit line also goes to the pump stage.

The inner chamber is not leak tight due to the lead of the thermal couple, which just feeds through a teflon screw. This screw can also, while in use, twist when the inner chamber is pressurized or pumped. This twisting can lead to the thermocouple wires crossing, leading to inaccurate temperature reading, resulting in the power supply pumping 100% of its current into the strip producing uncontrolled heating. There are insulators surrounding these thermocouple leads, but the thermocouple shorting can be one source of error. The metal post are connected to the power supply by insulated metal wires. The wires are held on via friction to the leads an can be pulled out, preventing power from being supplied to the heating strip. The power line must be checked for continuity before operation to prevent error.

The Eurotherm power controller for the bonder has the tendency to become unstable. The controller can over compensate, and either places 100% power or 0% power while trying to reach temperature. In this case the damping parameters have become too low creating an unstable temperature resuting in 30°C - 40 °C fluxuations. this underdamping could be caused by the change in impedance of the graphite strip, a change in impedance which seems to occur after the bridge is pressurized. The Eurotherm's parameters need to be recalibrated if large fluctuations occur. Recalibration is done by using the self-tune mode of the Eurotherm controller. After choosing a set point temperature, the controller will tune to that temperature and tweak its parameters to fit the thermal load. To preform this recalibration, the menu button is held down to obtain the long scroll menu enabling the choice of the St option. Pressing both the up and down arrows on the controller simultaniuosly will activate this mode. At this point A-T is illuminated, and the lower display indicates the SP at which the tune is to occur. SP will flash for a minute, during which time the temperature can be changed. After that minute the SP will stop flashing and the A-T will start. The temperature can not be changed at this time, and the controller will heat the strip. A-T will stop flashing once the tune has been completted [34].

5.3.2 Bonding Experiments

Initial bonding using Au/Sn/Au (18nm/64nm/21nm) on a simple Si surface (no recess) revealed inconsistent results, pills stuck to the polymer film within the bonding chamber were observed, ripping the pills off of the Si substrate after bonding. The pills remained on the film in their original orientation. An aluminum film was introduced between the pills and the polymer to prevent this sticking. The aluminum film was obtained from Alfa Aesar [35] and was 5 μm thick. After the addition of this aluminum film, the Au/Sn bonds were more consistently well formed and the pills were found to be mechanically rigid.

A series of bonding experiments was preformed using the bond metal combination summarized in Table 5.3.2. A thin Au/Sn/Au (18nm/64nm/21nm) bond stack was deposited within the recesses of an IC (Sample T-Au-100), which was used in initial recess bonding experiments. The bonding temperature of 315 °C for 5 minutes was used for the Au/Sn stack. The Au/Sn stack was designed to incorporate the 130 nm gold layer that capped of backside n-type metalization on the integrated pill (Chapter 4, Section 4.5 & 4.7), producing the proper ratio of Au:Sn of approximately 3:1 for the solder bond, as describe in studies by Metijasevic et. al. [36]. However, the total thickness of the initial Au/Sn bond stack was only 100 nm thick and surface roughness was a major factor in reducing bond strength. (See Table 5.2 for a summary of this and other results to be described in the following paragraphs.)

To improve thermal and mechanical characteristics of the bond, a thicker bonding metal was implemented. 400nm of indium was used as the bonding medium with a bonding temperature of 210 °C. The samples that used this metalization were T-In-400, S-In-400a, S-In-400b, and S-In-400c. Indium bonding avoids the complications in changing the eutectic compositions due thickness changes and showed very good bonding properties on flat silicon samples (no recess). However, Sample T-In-400, a two-tier mesa, showed limited results from its bonding experiments. These two-tier devices fit tightly and poorly within the IC recesses, and often the devices were not flush with the bonding surface. More room was required between the VCSELs and

the sides of the target recesses; thus single-tier devices were made.

Table 5.1: Bonding experiment samples

Name	Pill Type	bond psi	Bond Material (thickness nm)
T-Au-100	two tier	45	Cr/Au/Sn/Au (100 nm)
T-In-400	two tier	45	In (400 nm)
S-In-400a	single tier	45	In (400 nm)
S-In-400b	single tier	50	In (400 nm)
S-Au-500x	single tier	55	Cr/Au/Sn/Au (500 nm)
S-Au-500	single tier	43	Cr/Au/Sn/Au (500 nm)
S-In-400c	single tier	35	In (400 nm)

IC sample substrates S-In-400a, S-In-400b, and S-In-400c used single tier devices and showed a good deal of improvement in bonding percentage over their two-tier device counterparts. The bonding results are summarized in Table 5.2. Indium bonding places more constraints on post-assembly processing than the Au/Sn bond. Post-bonding processing temperature that exceed 150 °C for In bonds are problematic, due to indium's melting temperature of 154 °C. The temperature restriction is an important consideration for the BCB cures, which have to reach up to 250°C. A bond trial used a thick Cr/Au/Sn/Au stack (100nm/300nm/110nm/50nm) to allow the higher post bonding processing temperatures. These experiments resulted in sample S-Au-500. The thick Au/Sn stack meant most of the Au for the eutectic compositions was being integrated from the bond stack itself and not the 130 nm of Au on the VCSEL pill, possibly reducing the effectiveness of the bond. The top Au thickness on the Au/Sn bond stack was kept relatively thin such that the Au on the pill had could be incorporated into The Sn layer.

A few trials were attempted at elevated pressures. 55 PSI was used on Sample S-Au-500x to bond gold tin, however after several minutes of temperature ramping to obtain 318 °C, the substrate which sat between the IC and the heating strip began to crack, and finally crushed the sample, breaking the IC into 4 pieces. The aluminum strip allowed the heating bridge to take pressure but bending occurred, with the main sag at the center of the bridge, finally resulting in the graphite strip itself breaking.

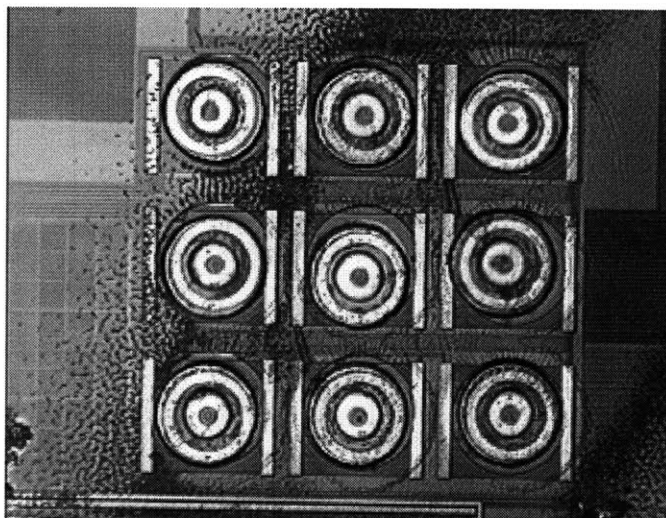


Figure 5-11: GaAs pills bonded in oxide recesses using pressure bonding system.

The graphite strip was replaced and the Aluminum reinforcement strip bent back to shape. Another trial showed initial cracking under 44 PSI and it was determined that the bonder could not reliable bond at this pressure, but this run resulted in sample S-Au-500. Pressures of above 35 PSI could not be used with the bonding setup without the possibility of damage to the sample and the graphite strip.

Table 5.2 shows the results of the bonding experiments. Table 5.2 shows that single-tier bonding trials were the most successful, due to the added room within the recess. The bonding results also favored 500 nm thick films, and high bonding pressures. The bonding experiments also suggested the indium trials provided a more reliable bond when compared to Au/Sn bonding. The bonding trials suggest a larger bond pressure may introduce more uniformity in the bond. Further investigation into the bonding process is required however. In order for this to be a feasible integration technology, a bonding process must be developed that can reliably bond 99% the devices down.

5.3.3 Bonding Improvements

In order to obtain more consistent bonding results, more trials need to be done with the bonding metalization, especially the gold tin contact. As noted in the previous

Table 5.2: Bonding Results

Name	Pill Type	bond psi	Bond Material (thickness nm)	(bonded/ total)
T-Au-100	two tier	45	Cr/Au/Sn/Au (100 nm)	(2/11)
T-In-400	two tier	45	In (400 nm)	(3/11)
S-In-400a	single tier	45	In (400 nm)	(8/11)
S-In-400b	single tier	50	In (400 nm)	(10/11)
S-Au-500x	single tier	55	Cr/Au/Sn/Au (500 nm)	break
S-Au-500	single tier	43	Cr/Au/Sn/Au (500 nm)	(7/11)
S-In-400c	single tier	35	In (400 nm)	(8/11)

section, most of the Au forming the eutectic was from the bond metal stack itself and not from the pill bonding layer. A thicker gold layer needs to be incorporated in the last metal step of the backside metalization on the pills to form a good bond with the thick (500nm) gold tin bond stack. Also, better alignment and wide coverage is needed during the backside metalization of the VCSEL pills. As discussed in Chapter 4, the major cause of misalignment during the single tier trial was due to a break during the bonding step of the WaferBOND^{tm} [25] process allowed for minor skew in the pill preventing accurate alignment. A lower WaferBOND^{tm} bonding pressure and a more rigid bonding apparatus would prevent such a break.

Metal bonding pressures need to be increased to at least 55 PSI. These higher bonding pressure consistently showed more pills bonded. In order to reach 55PSI or more minor modifications need to be made to the bonding setup. The metal reinforcing strip needs to be more rigid. A thickly machined (.5-.75 mm) piece of steel or aluminum could be used to reinforce the bridge. A ceramic post inserted in the center of the chamber below the heating strip could also be used to prevent sag at the center of the strip. Care must be taken to ensure these modification do not increase the thermal heat sinking of the chamber too much, preventing the strip from reaching target temperatures.

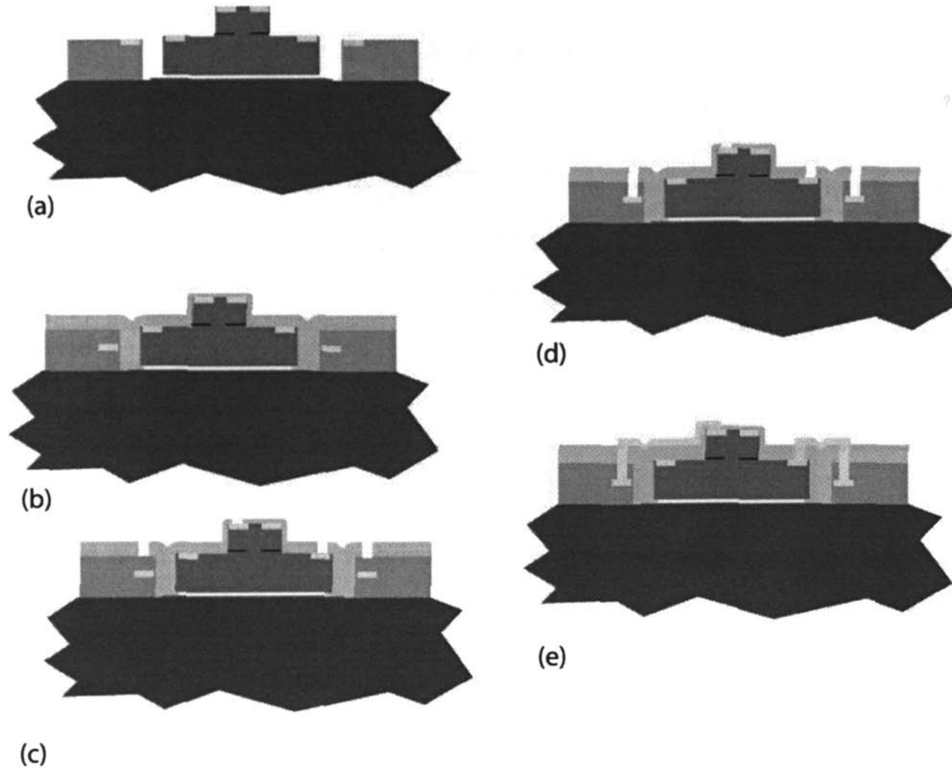


Figure 5-12: Schematic of post integration process flow. (a) Device is bonded within the recess. (b) Spin-on dielectric over coating planarizes recess. (c) Vias are etched through the spin on dielectric. (d) Vias are etched through the IC dielectric. (e)Metal is deposited and patterned, connecting the device contacts to the chip.

5.4 Post Integration Processing

After bonding the pills into place, the recesses need to be planarized with the dielectric stack and the top contact must be electrically connected to the rest of the circuitry. This section will discussed how this study was able to preform these steps, as illustrated in Figure 5-12. Section 5.5 will discuss modification to the post integration process that were used to obtain top contacts, and the resulting characteristics of the top contacts connecting the IC to the device pill will be discussed.

In order to passivate and planarize the devices a BCB dielectric is spun onto the IC. This layer is conformal and can be patterned. Metal lines can then patterned over the BCB dielectric, between contact pads to fully connect the devices to the IC. Cyclotene 3000 Series BCB from Dow Chemicals [37] has been used in post integration experiments and a spin speed of 2500 rpm was used. The BCB processing parameters

provides coverage of approximately 1.5 microns according to the spec sheet supplied by the manufacturer, which was confirmed by experimentation. Several spins are therefore required for total coverage, with an anneal step in between each. It is crucial for the pills to be bonded down, before spinning. The BCB will seep underneath the pills and move them from their recess if there is a failure to bond. Each anneal occurs in the EML tube furnace at 200 ^{o}C for 1 hour. A trial with Indium bonded pills on Sample S-In-400b included a furnace temperature of 140 ^{o}C for 30 minutes after the first spin, hardening the film before higher temperatures melt the indium on the bond. Despite of the lower temperature precaution the thermal properties of the Indium bond were found to have degraded after processing.

Low temperature BCB processing trials were attempted on Sample S-In-400c. These samples were cured at a temperature of 130 ^{o}C for 1.5 hours between spins. However, the targeted film thickness could not be achieved using this method, and the resilience of BCB to Acetone after the cure was lost. Thus it was found to be impractical to anneal BCB at such a low temperature. Using phase diagram for BCB for different cure time and temperatures as a reference, the cure time and the temperature used for this low temperature study correspond to a 35% phase change, which is was not enough to create a robust film. The 250 ^{o}C cure allows the BCB to reach a phase change above 90%.

The 1mm X 1mm chip size was especially hard to work with when dealing with the spin on films. The edge bead always limited photolithographic resolution. A technique was used to mitigate the edge bead problem, which involved spinning the film as thin as the processing allowed. While the spun polymer film was still soft, the chip can be placed polymer down on a clean aluminum dish. Each corner of the chip pressed down. Afterward the chip is carefully removed from the aluminum dish, avoiding in plane movement as much as possible. The pressure on the edges of the sample squashes the edge bead down on the corners. The hill to valley distance are reduced and the center of the chip is usually not effected by the flattening procedure. One can obtain less than 5 microns of separation using the flattening technique. The 5 microns separation is needed for fine patterning and for thick spin on polymers.

When curing the BCB, nitrogen must be flowed for 5 minutes before heating, to prevent yellowing of the BCB. Most of the BCB must also be removed from the back of the IC before annealing, to prevent adhesion to surface it is sitting on. The sample can also be annealed on a step of glass slides, angling the substrate and leaving the bottom surface free, ensuring stiction to surfaces does not occur. Three spins are required to cover the full pill. After the three spins, the top of the VCSEL pill is buried about 1 μm below the surface. There can be areas of the substrate that BCB does not stick to the surface, creating dips in the coverage. BCB can be removed with acetone before the anneal, so if a rework is needed, the removal of the BCB should be done prior to curing. Edge bead is a concern, especially on the small sample. Reduction of this is key to obtain good photolithography (see preceding paragraph).

The BCB processing was inconsistent, especially processing several spins on one sample. The pooling of BCB occurred during the curring step, making the sample unusable in its state for photolithography. The only way to clean the device at this stage is using a reactive Ion etch to remove all of the BCB. A solution to this pooling problem will be discussed in Section 5.5.

The best way to pattern the BCB is using an SF_6 / O_2 RIE. A photoresist etch mask can not be used, due to the high percentage of oxygen. Instead a thin Al etch mask was used to pattern the BCB. To allow accurate alignment to the contact pads below in the IC, a liftoff patterning technique can be used. The thickness of the Al should be limited, however a 40 nm mask did not hold up during via tests. A thickness of 150 nm is usable. A Lift-off technique can be used to pattern the aluminum. However since negative photoresist is needed and the via openings are small, it is impossible to align using the dark field mask. The mask with the via and recess openings had to be used. The recess opening allowed viewing of the IC substrate below and most of the alignment could take place using this open area, while the small via openings showed the underlying metal and could be used for the final small adjustments.

The use of the via mask with the recess opening to patterned the aluminum meant that there was an opening in the metal mask to the VCSEL devices below. To avoid

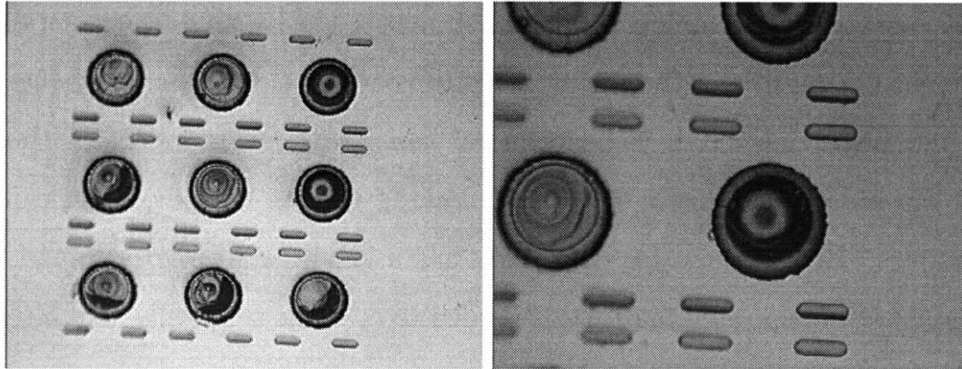


Figure 5-13: Lift off Al via mask revealing the yellow contact pads bellow. Circular center vias are also made and need to be covered during etch steps.

removing the BCB above these VCSEL, new photoresist was continually patterned above this opening to protect it. To avoid placing this photoresist continually, the light field mask of the vias can be used to pattern NR7 [23] everywhere but the vias. Using the photoresist as a mask, a few microns of BCB can be than etched using the RIE. The photoresist is then stripped and 150 nm of aluminum is deposited on top. The pattern in the BCB from the RIE can be seen in the aluminum overcoat and can be used to realigned the light field mask for photoresist openings of the vias. The aluminum can be wet etched to form the via openings and the photoresist can then be stripped. Using the quick BCB etch as an alignment mark for the aluminum mask the, hole above the VCSEL in the aluminum mask can be eliminated, and the BCB can be etched without the need for covering the VCSEL holes with photoresist.

Throughout this whole process one must consider the fact that this Al mask must be removed, even when the underlying Al pad is revealed, thus considerations must be taken to remove this mask but not the pads. A photoresist mask can be used to protect these sensitive pad areas during the mask removal.

The top VCSEL via and the side contact via can not be etched at the same time due to their different etch depths. A second patterning step could add error and complexity however. A blanket etch of the BCB that reveals the top of the pills without exposing the bottom tier would enable a patternless step.

Once the BCB is planarized and the vias are etched, revealing the top contacts on the pills and the side contacts on the IC, these pads need to be connected. Since

the BCB vias are approximately 4 microns in depth, ideally an e-beam metalization liftoff should not be used. The metal needs to coat the side of the vias since 5 μm of Al is not being deposited. E-beam metal has a long mean free path, thus does not coat the side walls during deposition making e-beam deposition ideal for lift-off techniques. However sputter deposition has a small mean free path and thus a smaller amount of deposited material is needed to coat the side walls, making a good conformal connection to the two pads.

Ideally, a blanket metalization of 300 nm of sputtered Al would be done to produce this last connection. Photoresist would then be patterned for the last contact layer. Metal will be deposited on the VCSEL emission surface, so care must be taken to remove all of the deposited metal over the VCSEL device. The VCSELs have Au as part of their metal stack. Depositing Au directly on Al can result in a purple haze which prevents a good metal contact. To prevent this a boundary Pt layer can be deposited on the Au. However, since a simple Al wet etch will be used in the patterning step, a thin layer of Pt can not be deposited. The Pt must be included on the last step of the N-type Contact on the pill. The p-type metal stack of the VCSEL is patterned using liftoff. There are several problems associated with the aluminum metalization process however and to these problems solutions will be discussed in Section 5.5.

The IC on which VCSEL devices have been assembled has exposed Al side bonding pads. These pads are buried during the BCB planarization step and must be revealed for testing. A blanket BCB etch could be preformed allowing the metal lines to mask the needed BCB, but the RIE would leave a pretty bumpy surface. A final photo patterning step can be done using thick resist to mask the BCB. An Al mask needs to be avoided since the Al pads below are being revealed. The blanket pattern for the BCB etch mask is not very intricate and a 5 μm thick photo-resist layer would be able to stand up for the 30 to 40 minutes that would be required to reveal the aluminum bonding pads.

5.5 Post Integration Processing Results

One problem with the above post-integration processing is that a sputtered aluminum film was not available. The sputter chamber of EML has oxygen contamination issues, preventing good quality aluminum films from being deposited, thus a gold sputtered film was used. However the initial run of Sample S-In-400b with the above parameters resulted in two main problems. First the gold etchant used to remove the gold on top of the VCSEL etched the VCSEL device itself, damaging the device. A few devices were spared, the spared devices were removed before the etchant went through the gold layer covering their tops. The remaining gold on the working devices, covering the output surface, was removed by scratching away their surface. However the remaining pills displayed a degradation in thermal heat sinking, most likely due to damage to the indium bond during the elevated temperatures of 200 ^oC and 250 ^oC during the BCB etch. More trials were perform to attempt to improve on these results. The following subsection will discuss attempts at a low temperature dielectric solution. Specifics results on the top connecting layer metal deposition are discussed in Section 5.5.2. Au/Sn bonded device post processing is discussed in Section 5.5.3 and the results are found in Section 5.5.4.

5.5.1 Low Temperature Dielectric

A low temperature spin on dielectric is needed for the processing of the indium bonded devices. Ideally the processing should not exceed 130^oC . The dielectric has to stand up to the metal etches, be etched with RIE, and stand up to photolithography. The WaferBOND^{tm} [25] material has these properties and was tried as a solution. These experiments used Sample S-In-400c.

The WaferBOND^{tm} material [25] was spun on and found that a spin rate of 2600 RPM was ideal. The WaferBOND^{tm} spin rate left about 4 micron of material above the VCSEL top. The material was then heated at 130 ^oC for 5-10 minutes. The polymer material becomes flatter over the main areas of the IC, however a large edge bead is developed. This edge bead needed to be reduced to obtain good photolithography.

Placing the sample face down on an aluminum dish on a 100 ^oC hotplate can reduce this edge bead. Heating the sample again at 130^oC will smooth out the surface once more. The sample can then be placed within the aligner in contact to measure the spacing between the mask ans the sample surface, to determine whether the edge bead has been reduced enough for good processing.

Once the WaferBOND^{tm} material was put down standard processing techniques at temperatures at or below 100 ^oC were preformed, with a caveat. Two complications were observed using the WaferBOND^{tm} polymer. During the heating steps of photolithography, movement in the WaferBOND^{tm} material [25] was observed. The movement resulted in a 5 μm error in a photo step. When metal was deposited and patterned, ripples were seen in the metal after the first hotplate bake. This became less of a problem with further processing, suggesting the material was not baked enough. Leaving the sample on the hot plate at 130 ^oC for 15 - 25 minutes might harden the film further, though care must be taken that an edge bead in the WaferBOND^{tm} does not form and harden again.

An incomplete RIE etch was also observed while using WaferBOND^{tm} as the dielectric. An O_2 / SF_6 plasma was used with the same processing parameters as the BCB etch. An etch rate of 2 μm every 10 minutes was observed. However there were pillars of material unetched during this process, possibly due to micromasking.

5.5.2 Metal deposition

Once the side IC contacts were revealed metal deposition was needed to string these contacts to the top surface. A sputter deposition was chosen in order to obtain metal on the side wall of the via contacting the top surface to the side contacts. Due to air leaks in the EML sputter chamber, oxidizer could not be chosen, aluminum could not be deposited, and even depositing a thin Cr stiction layer was impossible. A blanket layer of 400 nm of gold was deposited to the surface, on top of the aluminum mask already present. The sample was then patterned and etched using gold etch. The window to the VSEL device was not revealed to protect the VCSEL devices from the gold etch. This window would later be opened up and metal lift-off would be

used to contact the surface. The gold did not to stick during the etch step and there was a good amount of undercutting. The delamintaion was exacerbated when the photoresist was being removed from the sample. The gold preferentially stuck to the photoresist, making this metalization useless for the connecting metal lines.

A lift-off metalization was thought to be the best approach to overcome stiction issues problem. Lift-off enables a thick chrome layer to be inserted for stiction. The deposited film would be over a half a micron thick in hopes that it would coat the side walls of the via. Before this step could occur a blanket WaferBOND polymer etch was used to reveal the pill tops. The polymer RIE was found to be once again uneven, roughening the surface. Areas of the material etched all the way down to the chip dielectric before the top of the pills were fully revealed. Photolitography was attempted, however during the develop step,solution seeped underneath the WaferBOND ^{tm} [25] and during drying, broke open the dielectric revealing the bottom metal pad below. Further processing on Sample S-In-400c would have been in vane without a removal and reapplication of the WaferBOND^{tm} material. New vias would need to be etched. For the sake of time, Sample S-In-400c was laid aside.

5.5.3 AuSn Bonded Devices

A gold-tin bonding sample (S-Au-500) was assembled to avoid elevated temperature problems. Thick gold tin was used as described in the bonding results, and the bonding experiments showed limited results due to the lower pressure bond of 43 PSI. Further issues were present when BCB was spun on the sample. The last cure step for the third BCB layer resulted in pooling. Oxygen plasma was used to remove the BCB, for a rework in order to obtain a level surface.

Several attempts were done to obtain a good BCB stack, however none were successful. After another oxygen plasma rework a change in tactics was used. A single 1.5 micron spin of BCB was used and cured on sample S-Au-500, producing a smooth surface. The recesses are covered over in BCB spin step, concealing the bottom metal contact pad. The top of the VCSELS on sample S-Au-500 were still uncovered however. A 1 micron thick PECVD oxide layer was placed on top on top

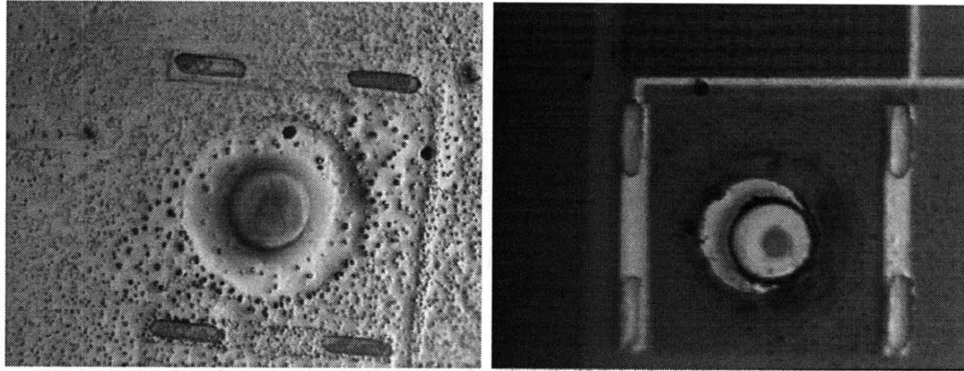


Figure 5-14: Via metal on AuSn substrate (S-Au-500). Contours of dielectric show underlying metal layers. Etched out side vias to contacts

of sample S-Au-500, covering the top and sidewalls of the VCSELs.

An aluminum via metal mask was deposited and patterned using the etch, metal deposition, etch technique described in Section 5.4. After metalization, the buried metal layer in the IC's metal stack could was observed through the metal mask due to bumps in the dielectric. If this pattern can be seen normally, the need for the first quick etch in the metal mask etch, dep, etch patterning technique is eliminated. Figure 5-14 shows the via metal mask covering with the shadows of the metal lines beneath.

Once the via mask openings were made, a simple combination O_2 / SF_6 plasma was used to etch down to the side contacts of the IC. The metal mask was then removed using Aluminum etchant, while the via opens are covered with photoresist. The remained of the aluminum metal over the Pills was also protected, however most of the metal above the pills was removed by brushing the surface of the sample with a foam swab in acetone.

The Pill vias needed to be opened, and a photo mask revealing only the pill area was used. First a quick Aluminum etch was used to remove any aluminum that remained above the VCSEL pills. During this step however, the solution was hard to blow off after etching. The photo resist kept beads of the etch solution the substrate. It is thought that due to the remaining trace etchant within these photoresist wells, etchant seeped through the PECVD oxide to 3 of the 7 VCSELs, partially etching their mirror stack, rendering them unusable. Care thus must be taken to fully clean

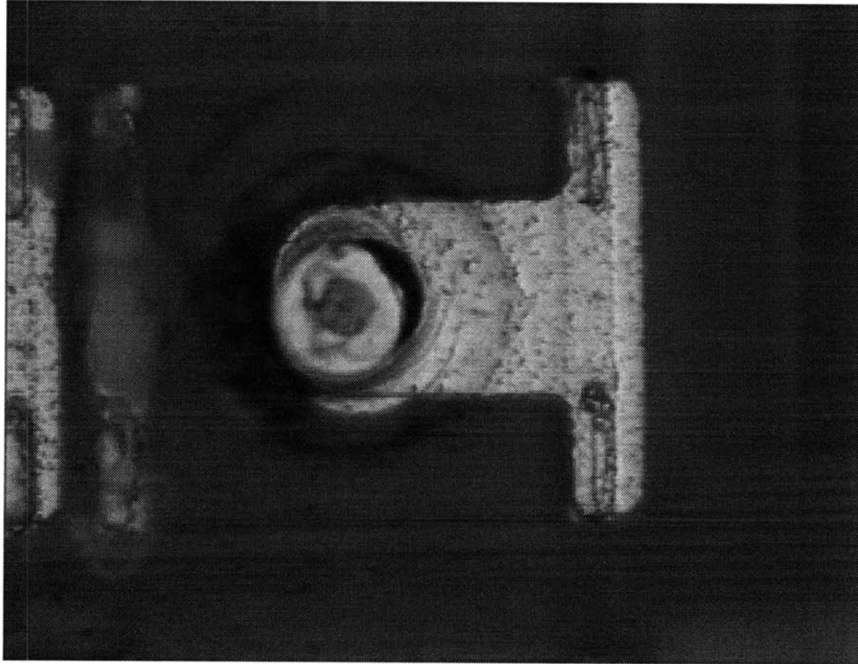


Figure 5-15: Top contact, connecting the P-side of the VCSEL to the side contact of the S-Au-500 chip.

these substrates off to prevent this kind of damage.

The top layer of PECVD oxide was then removed from the Pills. A straight SF_6 plasma for 25 minutes was used at first to avoid etching the photoresist mask, a O_2 / SF_6 plasma was then used to remove any BCB that might have been on the pill tops. Once the pill via was finished the photo resist was removed and the sample was prepped for metalization.

3000P NR7 [23] lift-off was used to place Au/Cr (500nm/100nm) on the IC. The metal stack adhered quite well to the IC and the metal pads. Gold was deposited on aluminum, even though there was a chance of a resistive contact. Once the interconnect contact were made, a thick 3 micron photo mask was placed over the IC revealing only the side bond pads. The IC was then placed in a O_2 / SF_6 plasma for 50 minutes to etch the BCB covering the side contact aluminum bond pads. Figure 5-15 is the resulting micrograph of the processing step, showing the metal coverage over the two contact areas.

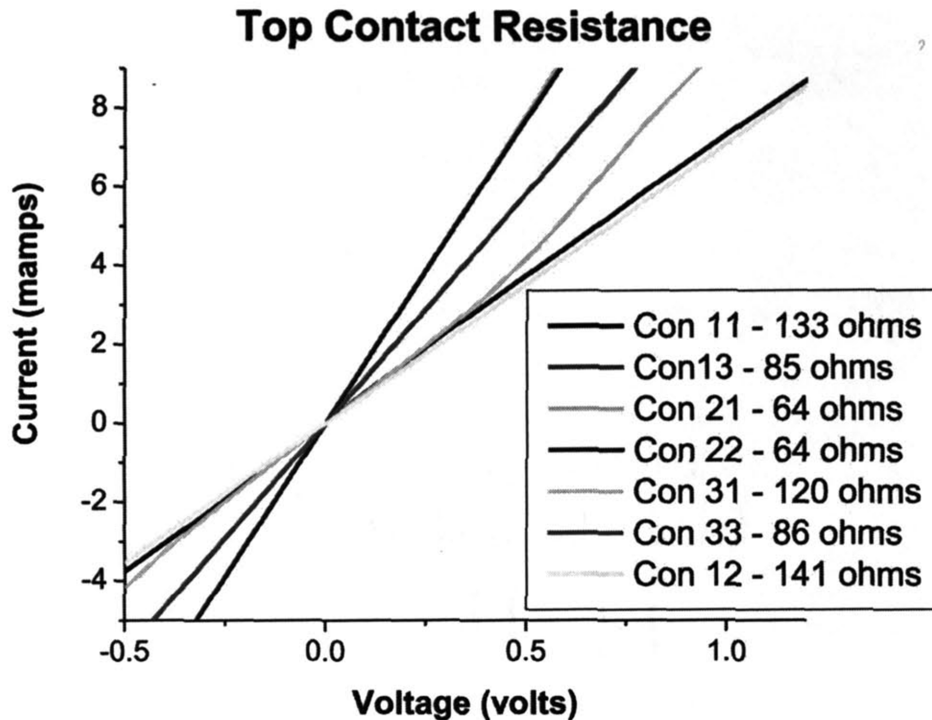


Figure 5-16: Resistance from contact pad to top of VCSEL Pill

5.5.4 AuCr Top Contact Results

Using the Cr/Au contacts and the combination BCB PECVD oxide, successful contacts were made to the top of the device. There was enough slope to the vias on the IC to allow the thick 600nm e-beam metal layer to coat the side and provide continuity. The PECVD oxide coated the side of the Pills preventing the metal layer from shorting the out along the sides. Figure 5-16 shows the resistances of top contact that resulting from the Au/Sn fully processed devices. Of the 9 top contacts in the 3 X 3 array 7 were connected to the side contact pads. All three of the remaining devices had good contact to the top of the devices. The contact resistance ranged from 64 to 144 ohms. These Contacts are not ideal and were a difficult processing endeavor. The size of the substrate, the unknown processing conditions, the state of the sputterer, and the state of the bonder created several process difficulties that had to be overcome. However these results suggest what can be done under more ideal conditions. Figure 5-15 shows a micrograph of these contacts on Sample S-Au-500x.

Chapter 6

VCSEL Micro-pill Electrical and Optical Characteristics

Device testing has shown that the micro-pill devices produced exhibit lasing characteristics and good IV curves. This chapter will show several measurements of various pills exhibiting lasing and how improvements made in their structure improve their properties. Lasing characteristics have been shown to be highly dependent on the current aperture diameter and quality, while also showing dependences on VCSEL mirror and gain spectrum matching. This chapter will also show lasing devices fully integrated on a silicon integrated circuit, which was the main objective of this thesis work. Some of the devices characterized have been integrated to IC substrates, a list of substrates used can be found in Table 6. The first Section 6.1 will describe the measurement apparatus used in these experiments. Early device, two tier device, and single tier device characteristics are discussed in Section 6.2, 6.3, and 6.4 respectively. Finally devices integrated on ICs will be discussed in Section 6.5.

6.1 Measurement Apparatus

The measurements taken in these experiments used a probe station, shown in Figure 6-1,which is connected to an HP4145B parameter analyzer. A silicon photo detector is placed on the top of the probe station microscope. The photodetector used was

Table 6.1: Samples used in characterization experiments

Name	Pill Type	bond psi	Bond Material (thickness nm)
T-Au-100	two tier	45	Cr/Au/Sn/Au (100 nm)
T-In-400	two tier	45	In (400 nm)
S-In-400a	single tier	45	In (400 nm)
S-In-400b	single tier	50	In (400 nm)
S-Au-500	single tier	43	Cr/Au/Sn/Au (500 nm)
S-In-400c	single tier	35	In (400 nm)

obtained from Edmund Optics(stock no. 53-373) [38]. It was a 100 mm^2 area device with a BNC mount. A portion of light that enters the microscope is directed through the top, to the detector. The silicon detector is biased at zero volts, and has a 58% conversion rate for 850 nm light. Not all light is collected through the microsope objective, and some of the light is directed to the eye ports, making it difficult to determine the total light power emitted of the devices.

Before proceeding to discuss the device measurements, a cautionary note is in order. VCSEL devices are very sensitive to current input. They can easily overheat and burn out the active region, permanently destroying the device. For all measurements a maximum current must be set. However this current maximum varies from device to device so care must be taken, though it is almost impossible to avoid burning out some devices. When light output of the device shuts off, the device has most likely reached its critical temperature, at which point further current drive output could cause permanent damage. The device can be driven past the point of optical emission roll off, but only by about 25 % of the current input. Beyond this point a device can easily overheat and be permanately damaged, preventing any further lasing behavoir.

6.2 Early Devices

Early devices showed good light emission, however lasing characteristics were rarely observed. The lack of lasing was mainly due to the lack of aperture control in the early processing. Figure 6-2 shows the output frequency of one device at both 10 ma,

Figure 6-1: Electrical probe station with affixed silicon photodetector, and HP4145B .

and 25 ma. The peak emission of the device occurs at around 850 nm, however the full width half max of the spectrum shown is too large to represent a lasing device. The device shown does have a small spectral width compared to normal LEDs due to the spectral filtering of the DBR top mirror.

One critical feature in identifying lasing behavior is the distinct knee in the luminescence vs. current (LI) curve , showing an increase in the incremental output of light of per incremental current through the device. The LI knee feature can be observed in Figure 6-3. This specific device was tested on its native substrate and had no aperture to reduce its threshold current. Only the diameter of the pill top restricted the active area of the device, resulting in a large threshold current. The device characteristics show a distinct knee at 22-23 ma, defining its threshold current there.

The current voltage (IV) curve shown in this same figure are typical for low resistance contacts and a well behaving device. Devices with high resistance contacts can have bias voltages 2 volts larger than similar current drives . High resistance

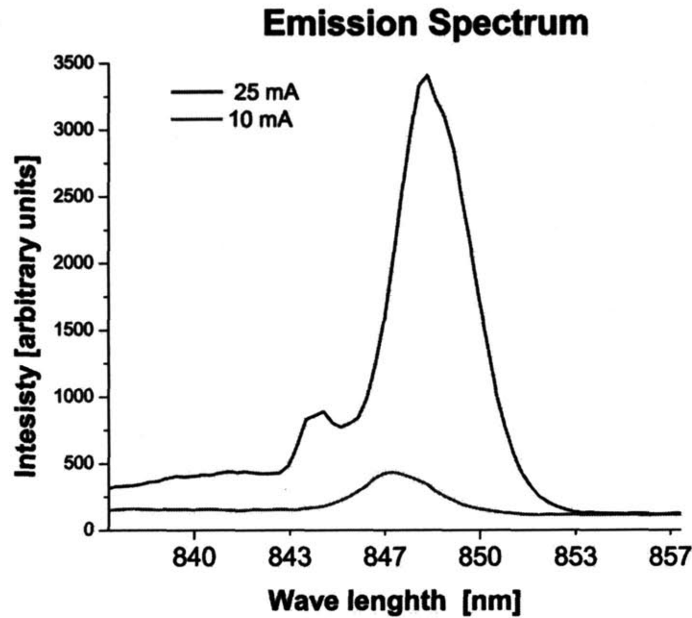


Figure 6-2: Spectral light output of non-current confined device at 10 ma and 25 ma input current. Spectral width is indicative of a LED device with spectral filter,

contacts can sometimes be burned inüsing applied current, ultimately reducing their resistance and this problem. High resistive contacts were mostly associated with poor second tier contacts or devices that were measured prior to an anneal step. One important consequence of high contact resistances can be an overestimation of the power dissipation within the active region of a device, due to the large I-V readings.

The device characteristics shown in Figure 6-4 are the first observed lasing devices using oxide apertures. The devices shown were tested on their native substrate and showed a wide variation in their threshold currents, due to device size variations and lack of control over the oxidation rate. The devices measured were very susceptible to heating due to the devices large threshold currents.

6.3 Two Tier Devices

The first stand alone VCSEL Pill devices were made using the two tier device structure. The two-tier devices were made after refinements to the oxidation process enabled controlled apertured devices. One of the first devices exhibiting low threshold

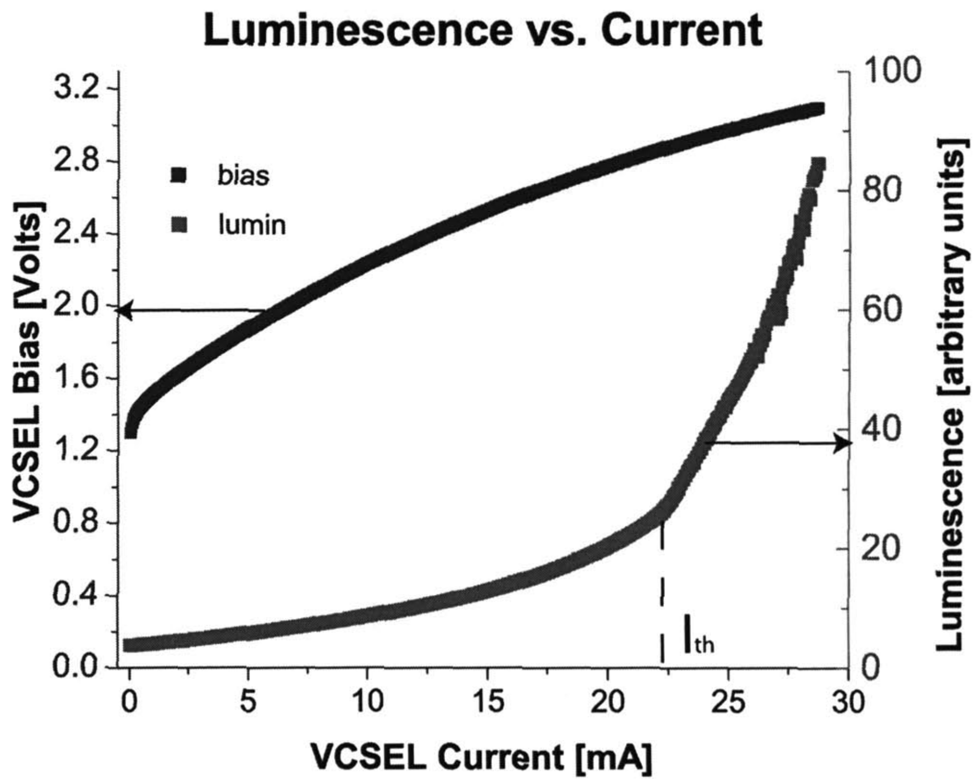


Figure 6-3: Unapertured device on its native substrate with a 35 μm diameter, and a 25 ma threshold current.

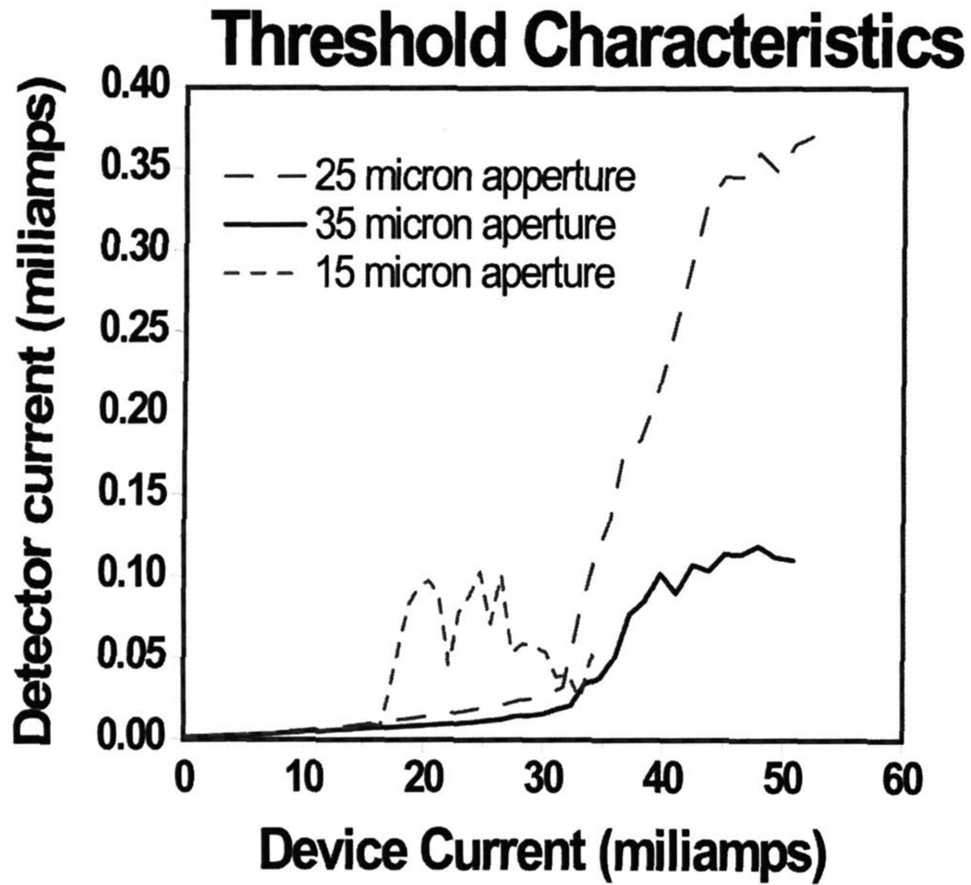


Figure 6-4: *LI curves of several nominally identical devices on native substrates displaying various threshold currents. Each are apertured using oxidation, and display relatively high threshold currents*

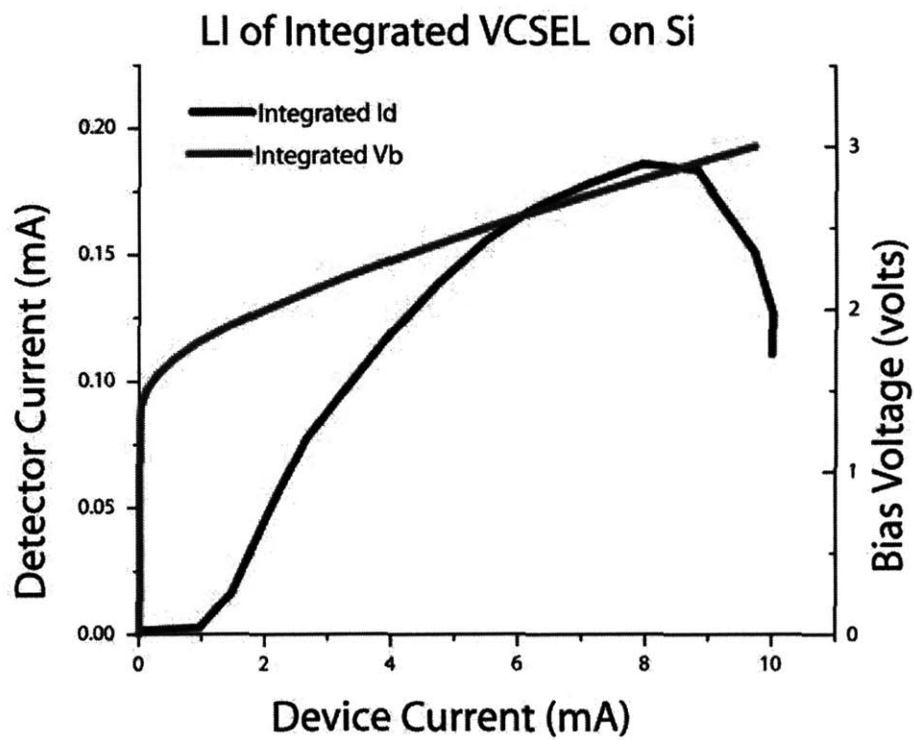


Figure 6-5: LI curve of integrated on Si VCSELS with threshold currents of *1ma*.

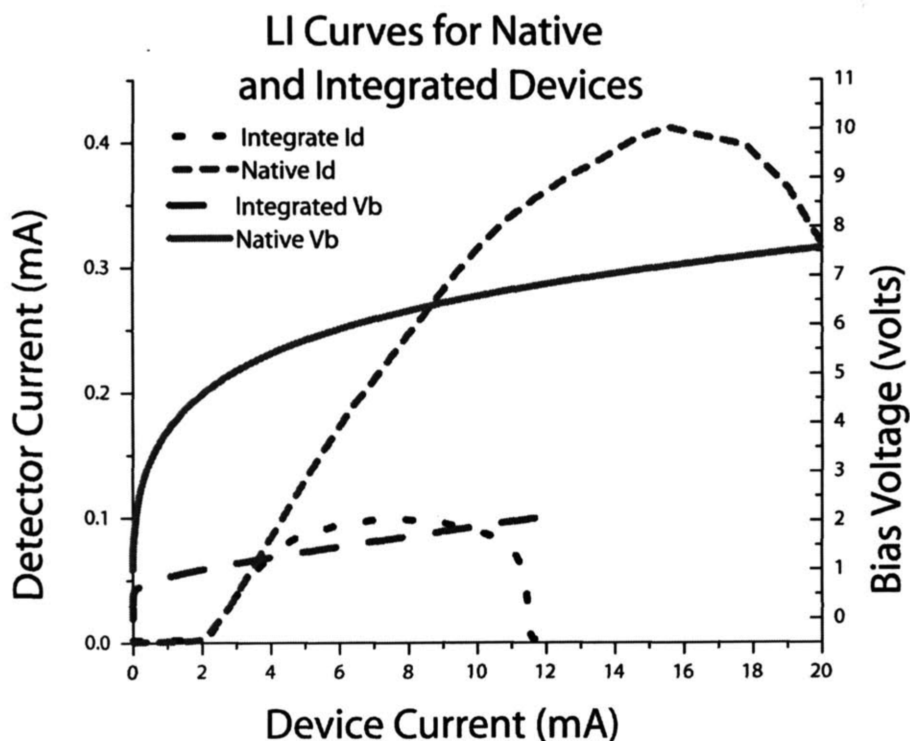


Figure 6-6: LI curves of two VCSELS, one on a native substrate and the second bonded to a Si substrate. Both show current thresholds of 2.5 ma

lasing in pill form is seen in Figure 6-5. The knee in the LI curve shows that the device has a threshold current of 1 ma. The device was bonded onto a silicon substrate using the 100 nm thin Au/Sn bond. The two-tier preliminary devices successfully demonstrated lasing, however there was a wide variation in device characteristics for reasons discussed in Chapter 4, Section 4.4.3.

Pill devices bonded to Si with 30 nm of Au/Sn alloy did not perform as well as similar devices on their native substrate. This observation can be seen in Figure 6-6, in which two similar devices have their LI curves plotted. Both devices have 2 ma threshold currents, though the native substrate device has a distinctly higher current voltage characteristic. This is expected, since the native device's contact had not been annealed. The main difference between the two devices, however, is in their light emission roll off at high current levels. The native substrate device shows continual light emission beyond 20 ma device current, however the bonded pill

device's light emission cuts off before 12 ma. The distinct difference in optical roll off can be attributed to the thermal heat sinking characteristic of the devices. The heat sinking issue will be discussed in length in Chapter 7. Due to the premature light emission roll off in the bonded devices, improvements in the thermal heat sink of integrated devices were sought. To this end, a better bond using thicker metal was investigated. Improvements were seen using these thicker bonding metals and comparative results can be found in Chapter 7 Section 7.4.3.

6.4 Single Tier Devices

Single tier devices were designed and developed as described in Chapter 4, Section 4.4.3. The single-tier devices decreased the the footprint of the device, the device variation, improved their bonding interface, and allowed for improved post processing of the target IC. Using the single-tier devices, a process was developed that successfully integrated these tiny devices fully onto the target IC. Figure 6-7 shows the characteristics of Device 11 on Substrate S-Au-500. The tests on Device 11 were done without the use of Si transistor device on chip. The device was measured by probing the bottom contact and the top contact, and then again by probing the bottom contact and the side contact that has continuity to the top contact. By comparing the two measurements the impact of the increased contact resistance from the side probe on the chip can be observed.

Observing the top probed device (probed on metal lines in Figure 6-8 left) improvements can clearly be seen in integration bonding. Pill Device 11 has a threshold current of 2.5 ma and continues to emit light up to 22 ma. Comparing Device 11 to devices with the same threshold currents, the two-tier pill device in Figure 6-6 has almost half the optical output drive range. The single-tier Device 11 has a similar drive range compared to the two-tier device on the native substrate in Figure 6-6.

When Device 11 is contacted through its side contact (probed on Al pads in Figure 6-8 right) there is a good deal of series resistance observed. The resistance is to be expected from Figure 5-16, which shows that Device 11 has a contact with a resistance

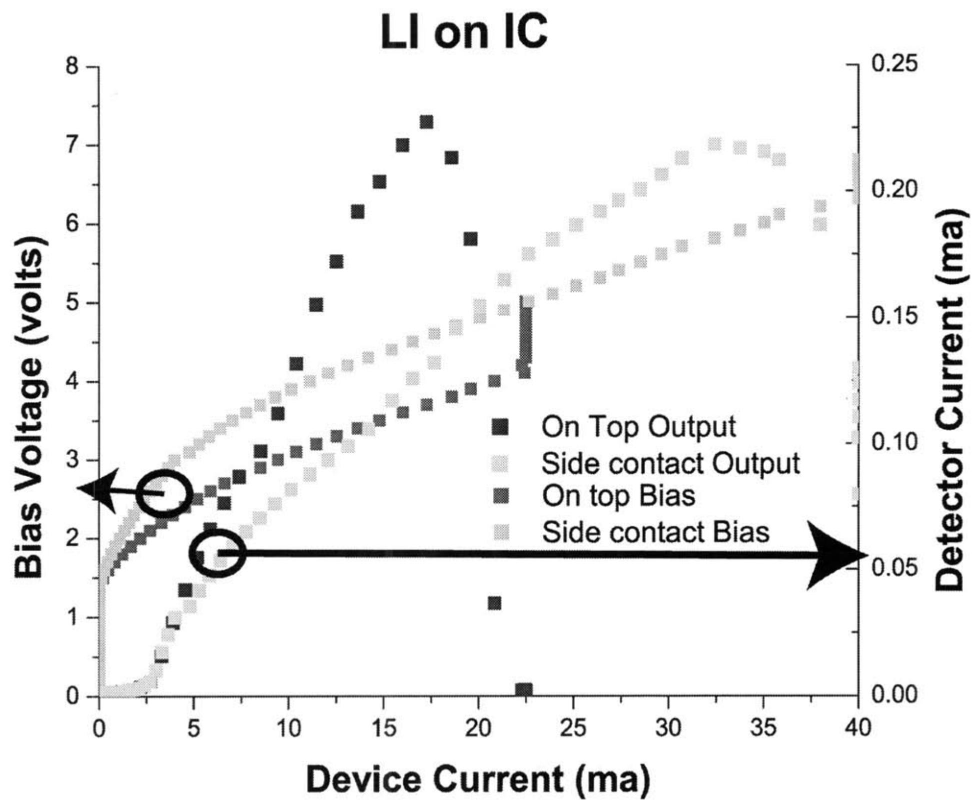


Figure 6-7: LI curves for fully integrated Device 11. The P-type contact is probed using both the top contact and side contact.

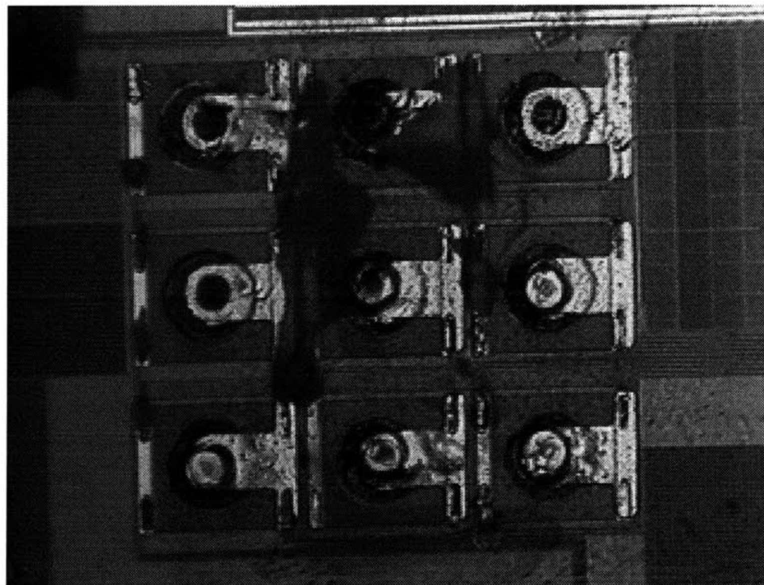


Figure 6-8: Array of devices showing gold connecting top contact.

of 133 Ohms from the pad to the top of the pill. The increased resistance increases the voltage needed to obtain a certain current, and the impact is seen by comparing the two the IV characteristics. A one volt bias difference is seen at 20 ma for Device 11 probed at two different points. The voltage measurements seems to suggest there is a smaller series resistance than shown in Figure 5-16, e.g.approximately 50 Ohms.

Another interesting difference is in the LI curves of Device 11 under the two different measurement conditions. Though the two measurements show a roll of at similar light outputs intensities, the side contacted Device 11 measurement does not reach its maximum light output until 32 ma, as opposed to the 18 ma maximum seen in the top contacted measurement for Device 11. This suggest there is a secondary current path that does not go through the active region when probing Device 11 using the side contact pad. This seems to be confirmed by the bias voltage plot of Device 11, which shows a 2 volt offset between two measurements at their peak light output. This 2 volt offset would agree with the expected bias voltage difference for a contact resistance difference of 133 ohms at a 18 ma current.

Similar measurements were performed on Device 21 on the same IC substrate (S-Au-500). Device 21 shows a much faster roll off in emission, which this can be explained by its threshold current of 1 ma. The lower threshold current of Device 21 suggests a smaller apertured device when compared to Device 11. The smaller aperture increases Device 21's thermal impedance. From the measurements in Figure 5-16 it is know that the contact resistance of Device 21 is about a half of Device 11. A reduction in bias voltage differential should be seen in this device. Figure 6-9 shows that the voltage bias differential is significantly reduced for Device 21. Figure 6-9 also shows that there is about a 4 ma difference in current bias at peak light output. Device 21 also exhibits a secondary shunting current path, however this difference is greatly reduced.

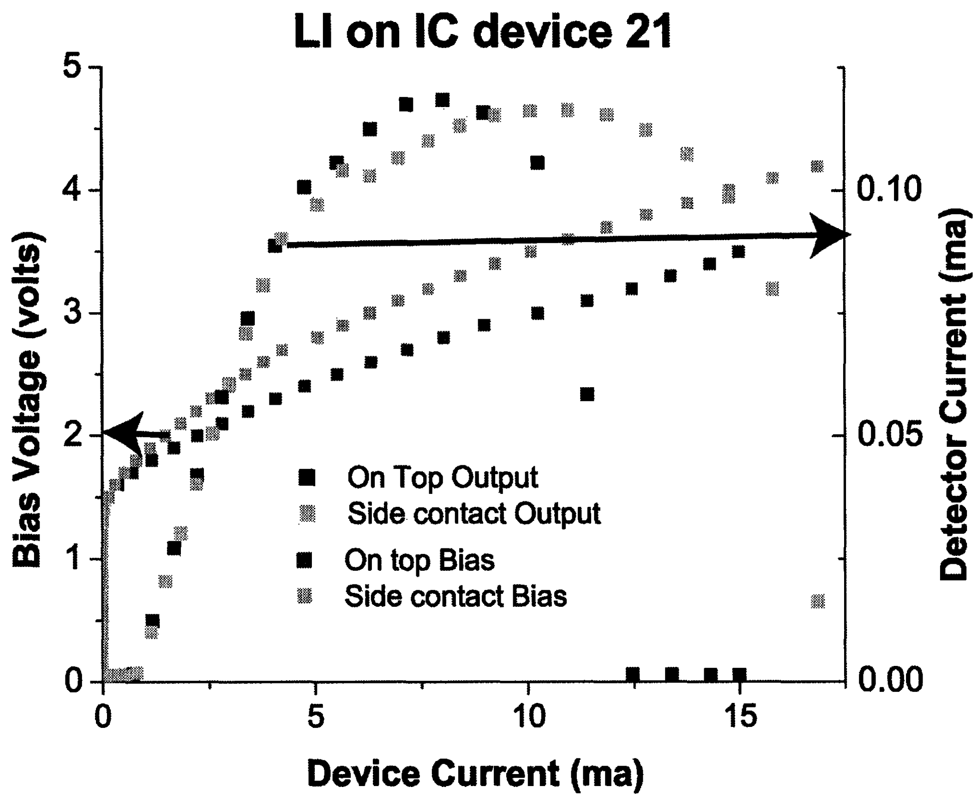


Figure 6-9: LI curves for fully integrated Device 21. The P-type contact is probed using both the top contact and side contact.

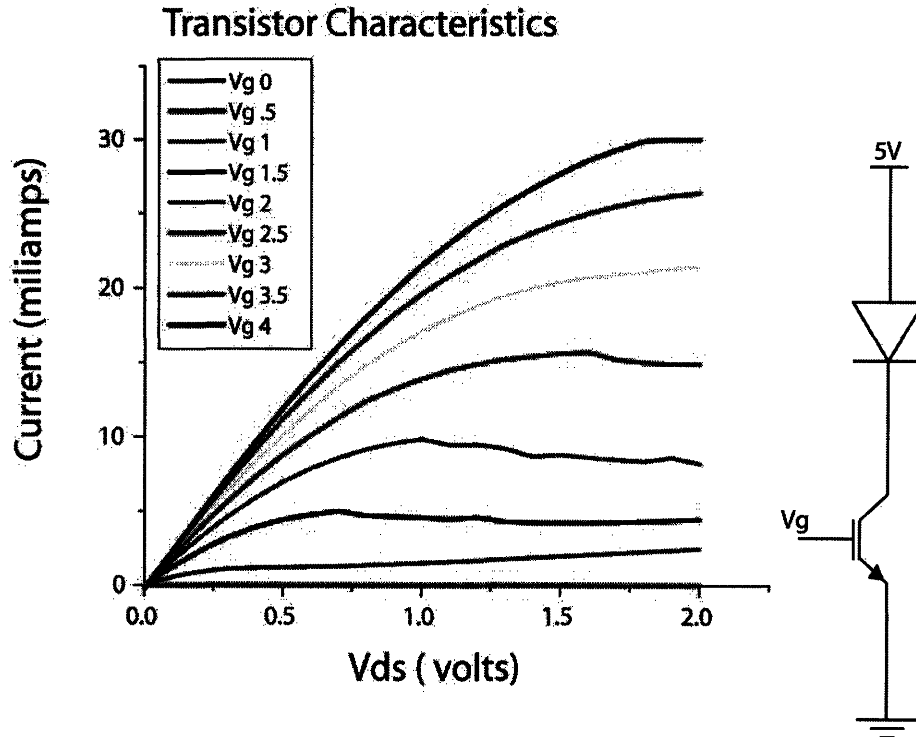


Figure 6-10: Transistors on chip, designed to power the VCSEL devices. Design by Simpkins, made by MOSIS. on the right a diagram showing the drive transistor diode circuit layout.

6.5 Transistor Driven Devices

The ultimate objective of the this project is to have a silicon transistor drive the VCSEL devices. The target IC was design by Travis Simpkins [6] and fabricated by MOSIS. The chip has large drive transistors sitting below each of the VCSEL target sites. Once the VCSEL recess is opened up to the target site aluminum pads the transistors can be probed and their characteristics can be measured. Figure 6-10 shows the output characteristics of one such transistor just after opening up the recess. The Vdd of the chip is tied to 5 volts during this testing. The characteristics show that the fabricated transistors are capable of producing the current required to drive the VCSEL pills. However, it was observed that the transistor devices are not stable when run above 20 ma, so a maximum Ids of 20 mA was be used.

The processing of these integrated circuit chips can damage the circuit. As discussed in Chapter 4, the two-tier devices left no extra room between the recess and the side contacts. The lack of room caused the wet enchant during the recess step

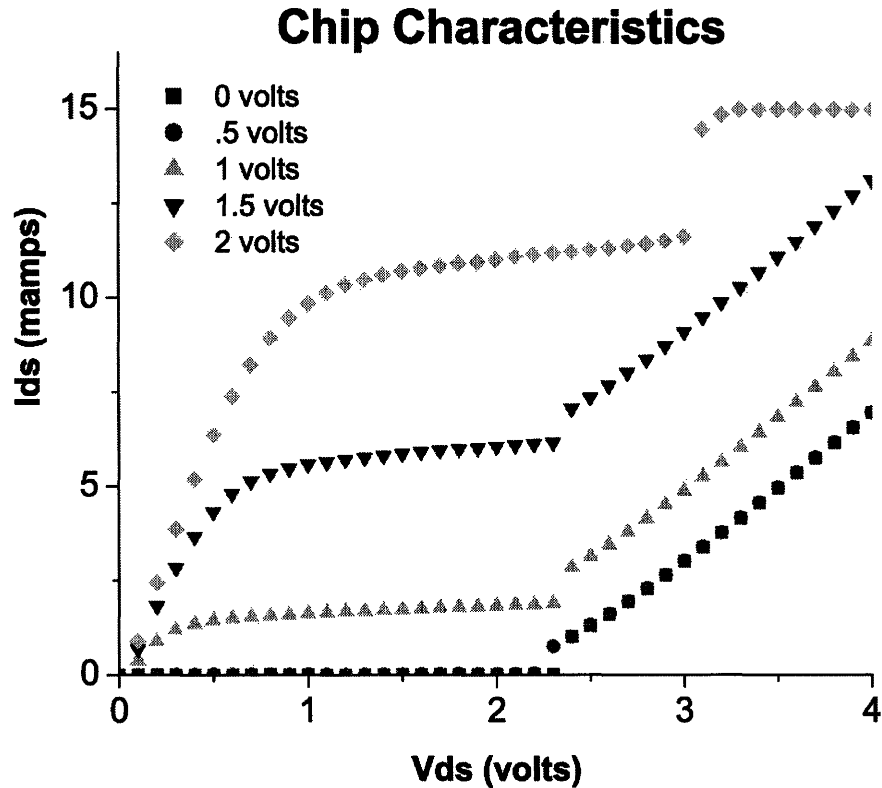


Figure 6-11: Transistors on chip after processing, Vdd = 5 volts. Design by Simpkins, made by MOSIS

touched these contacts, and often ruined the transistors. The single-tier devices allowed for greater room between the recess and the side contacts, keeping transistor contact intact, however both the side contact and the bottom contact, that are to be connected to the the VCSEL device, must survive the RIE etches that reveal them. Also errors in photolithography could induce unintended etching in parts of the integrated circuit. Care must be taken to protect the transistor devices and the metal interconnect circuitry during all assembly and post-assembly processing steps.

Similar transistor curves were taken after the integration of the VCSEL devices within the recesses. The top of the transistor was probed using a side via on an empty recess transistor (Location 33 in the 3X3 array on chip S-Au-500), while Vdd, Gnd, and Vg were probed from the side chip pads. Transistor characteristics are shown in Figure 6-11. Vdd was again biased at 5 volts. The transistor measurements are very similar to those seen in the Figure 6-10. However after VDS is biased beyond 2 volts the transistor exhibits non-ideal behavior. The non-ideal behavior should not

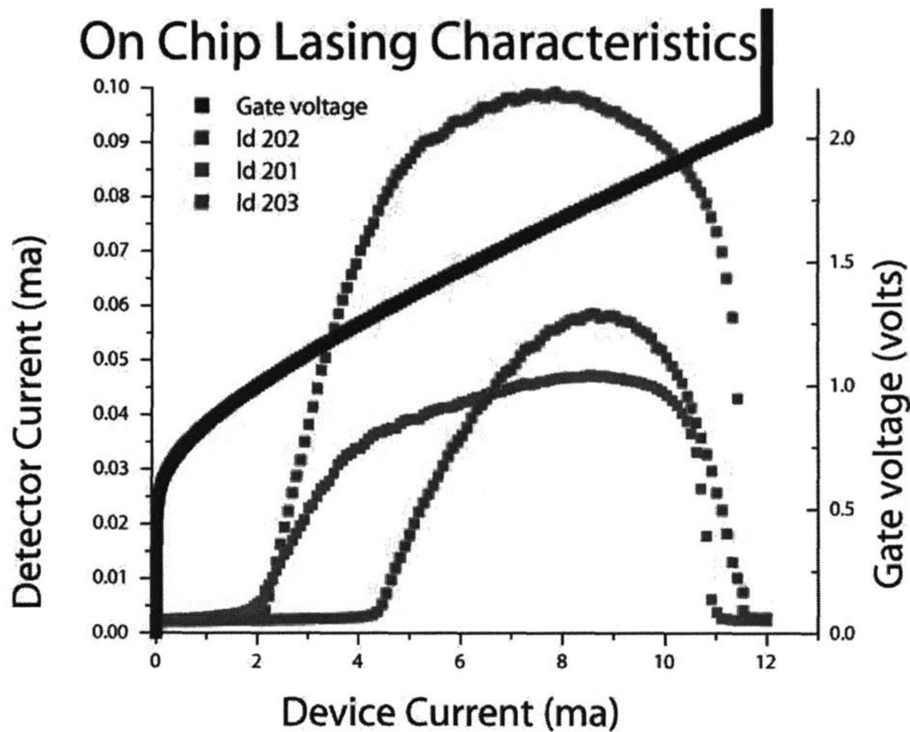


Figure 6-12: Two tier VCSEL lasers driven by the gate of on chip transistors. Devices bonded using thin Au/Sn on Chip T-Au-100. The devices shown have their top contact probed and are not fully integrated

be an issue since most of the voltage drop occurs across the VCSEL device. From the transistor curves in Figure 6-11 we see a gate voltage of 2 volts should produce the needed 10 ma current bias to turn on the VCSEL pill devices.

The first VCSELs driven on chip were two tier devices. The LI curves from the integrated two-tier devices can be seen in Figure 6-12. The two-tier devices were not post processed, thus their top contacts were probed to the VCSEL. Out of the 11 devices assembled on the chip, only three of the VCSELs bonded using the thin Au/Sn bond on Sample T-Au-100. The two-tier devices had threshold currents of 2-4 ma. The LI curve shows the VCSELs reach critical heating that suppressed light output at 12 mA. The 12 mA roll off suggest their bond was not ideal, limiting their current drive operation.

In an effort to improve integrated device characteristics, a thick 400 nm Indium bond was used on Sample T-In-400. The resulting LI curves of devices on Sample

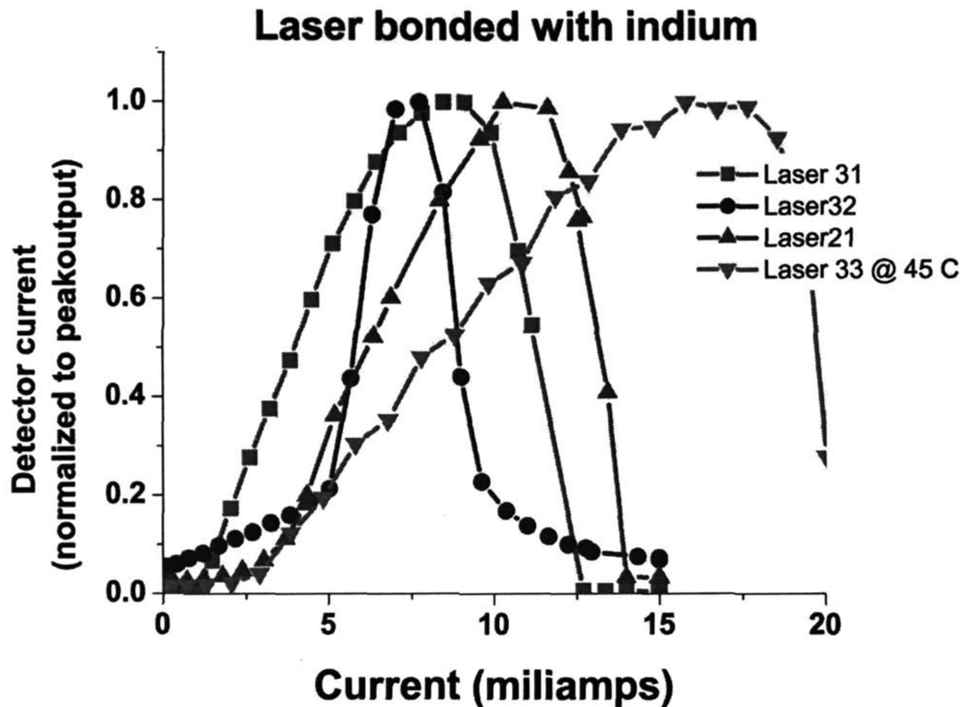


Figure 6-13: LI curves of Two tier VCSEL lasers driven by the gate of on chip transistors. Devices were bonded using 400 nm of indium on Chip T-In-400. The devices shown have their top contact probed

T-In-400 can be seen In Figure 6-13. Though more pills were bonded and one device showed lasing up to 20 ma applied current, some of the devices showed limited current drive ability. The 20 ma device also had to be heated to obtain reveal the low threshold current, the reason for this threshold dependence is discussed further in Chapter 7, Section 7.4.3. It was determined that the two-tier of VCSEL devices were a too close a fit to get a predictable bond to the surface. Single tier devices integrated within recesses that provided enough room were sought to obtain better device performance. The results of the single-tier devices, bonded using Indium, can be seen in Figure 6-14. The single-tier devices were bonded on Sample S-In-400b, and bonding resulted in all but one device bonded. Most of the single-tier devices bonded showed light output with high drive currents.

Post processing developments allowed for devices to be probed and driven using only the side aluminum pads of the chip. As discussed in Chapter 5 Section 5.5.3, only 4 of the seven devices on chip remained functional after the post processing, due

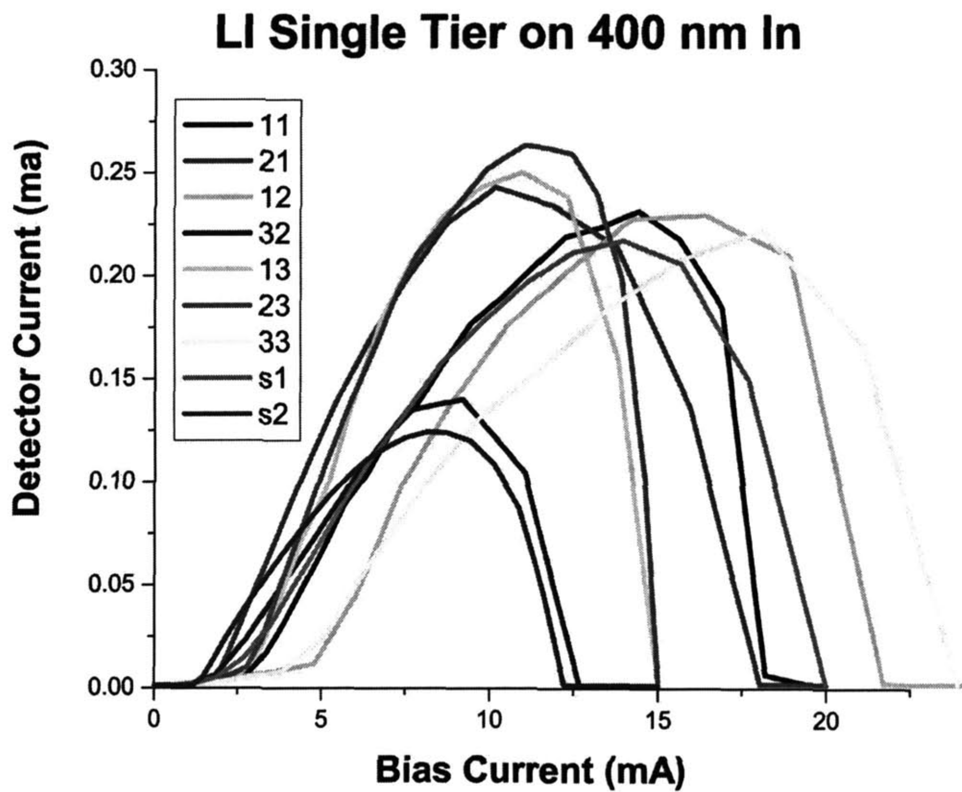


Figure 6-14: Integrated VCSEL lasers bonded using 400 nm of In on Sample S-In-400b. The devices shown has been probed from the top device contact to bottom aluminum pad.

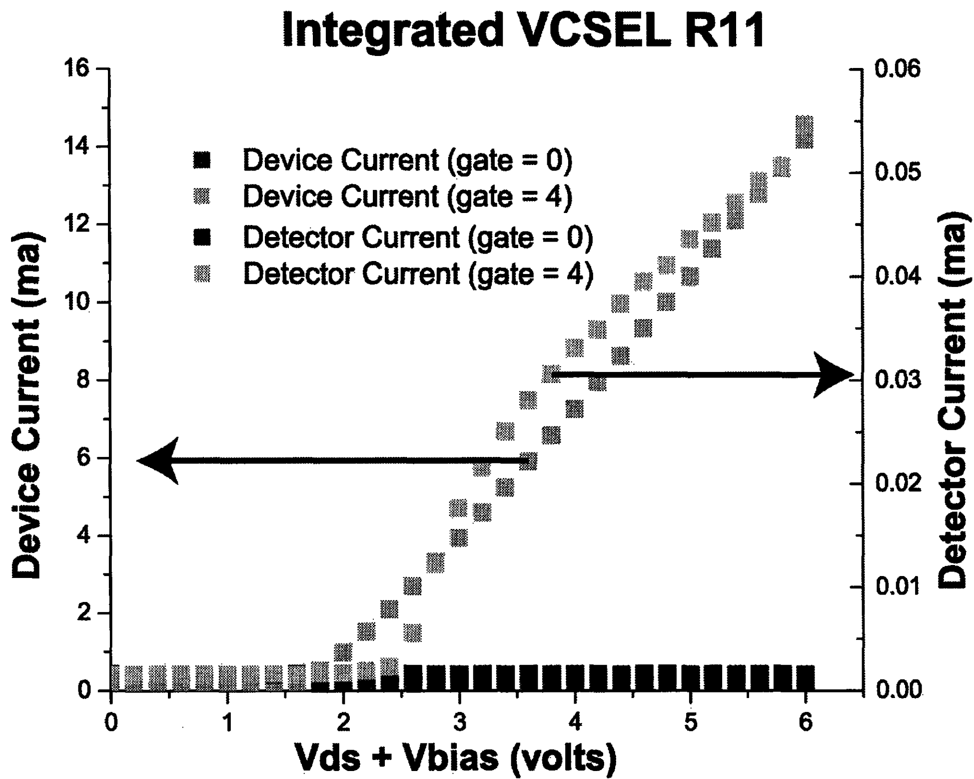


Figure 6-15: Fully integrated VCSEL lasers (Device 11) driven by the gate of on chip transistors. Devices were bonded using 500 nm of Au/Sn. The device shown has been probed from the side bond pad of the IC.

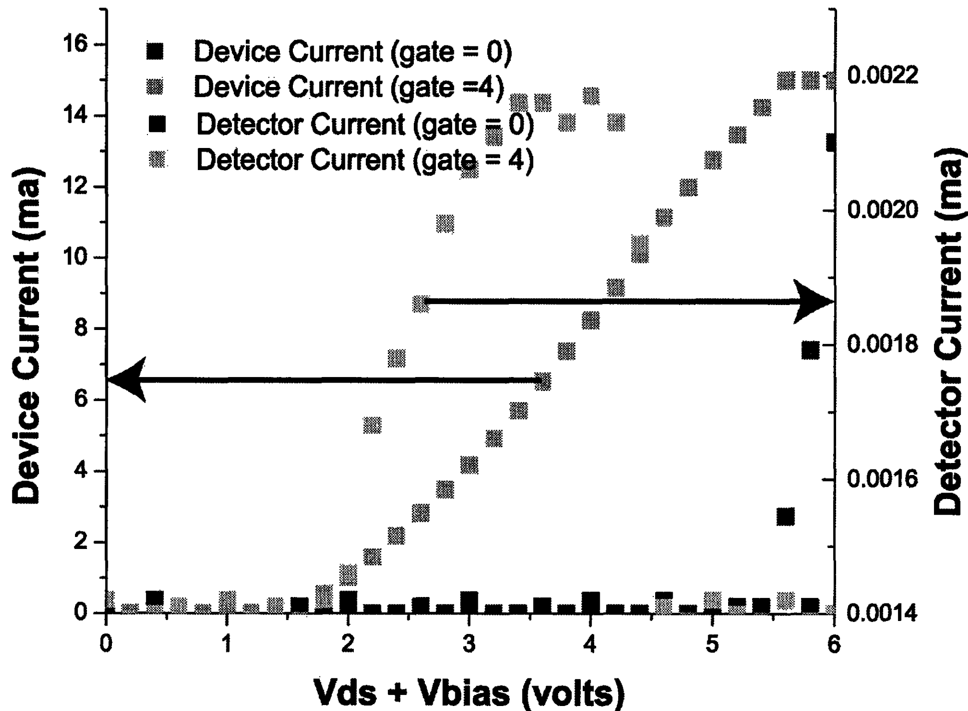


Figure 6-16: Fully integrated VCSEL lasers (device 21) driven by the gate of on chip transistors. Devices were bonded using 500 nm of Au/Sn. The device shown have been probed from the side bond pad of the IC.

to unexpected wet etching of three devices. One of the remaining four devices had unstable contacts, resulting in a final burn and burn out when 30 ma current was applied. Another device was ruined when 25 ma was allowed to flow through device mistakenly, even though the optical output of the device shut off at 15 ma. Two working fully processed devices were left on sample S-Au-500.

Figure 6-16 shows Device 11 driven using the transistor below its bond pad on Sample S-Au-500. The light output was taken with varying voltage biases at both 0 and 4 volts of gate bias. The VCSEL device showed similar LI behavior as that seen in Figure 6-7, while also showing the ability to turn on and off the device using the gate voltage of the transistor on chip. Similar results can be seen for Device 21 on Sample S-Au-500. The characteristics of this device are shown in Figure 6-16. Once again this device is shown to be turned on and off, while also displaying the same LI characteristics seen in the probed contact measurements in Figure 6-9.

The transistor below the VCSEL device has a certain amount of heating associated

it, thus using this transistor to power the device can inadvertently heat the VCSEL device. The transistor heating could impact the amount of drive current that can be used before light output roll off. Looking at the LI curve from device 21, it is seen that complete light roll off occurs at around 17 ma when probed without the transistor. The maximum drive current falls to around 11 ma for Device 21, when using the transistor below is used to power the device, which may be due to this heating effect. The reduction in drive current is a significant and may one disadvantage to placing the drive transistor so close to the transistor. However the secondary current path that gave rise to the 17 ma drive roll off found in Device 21 might be shut off when the chip is powered. Further investigation into the affects of transistor heating on above VCSEL devices need to be preformed.

Chapter 7

VCSEL Heating Simulations

Heat dissipation is a major limiting factor in laser operation. Device heating impacts the amount of optical output power obtained from a device. Heating effects can be seen in a device's LI curve. After a laser reaches it's threshold current, an increase in the slope of the LI curve is seen, producing a knee at the point of threshold. After a certain amount of device current is applied, a roll off of optical power emission is seen. Throughout the device's operation, as more current is applied to the device heating grows due to parasitic resistances and the temperature of the active region increases. The temperature increase spectrally shifts the gain curve of the active regions in the device, by slightly expanding the quantum well itself and increasing the band gap of the semiconductor in the active region. The increase in temperature also increases the relative effectiveness of non-radiative states, decreasing the quantum efficiency of the device, while also contributing to the heating of the device.

The temperature increase also affects the DBR of the device, as the semiconductor mirror stack expands and the index of refraction changes. Both expansion and the index change effectively increase the resonant cavity length in the VCSEL, resulting in a shift in laser output frequency to a longer wavelength. The different rate of DBR and band gap shift begin to detune the gain spectrum of the quantum well from the notch filter of the DBR mirror. A shift in the output frequency of the device to longer wavelengths results. The wavelength shift begins to decrease the efficiency of the device until the VCSEL no longer emits light. The light output roll off and

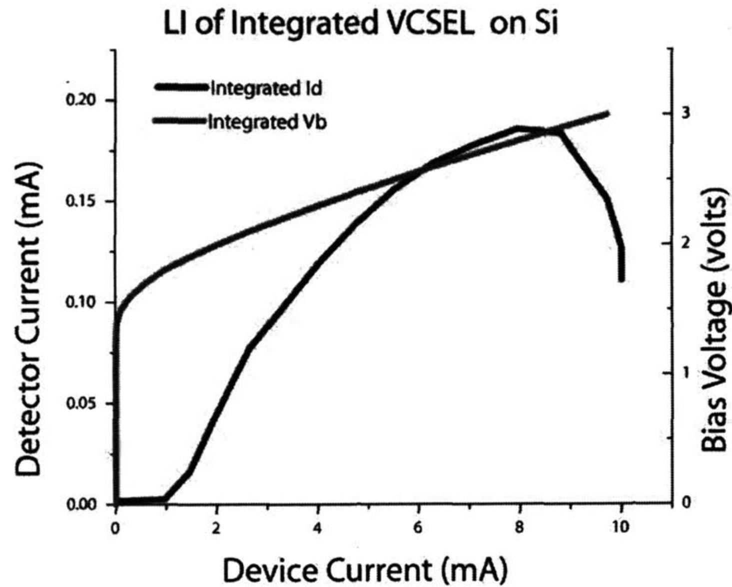


Figure 7-1: LI curve of integrated on Si VCSELS with threshold currents of 1ma.

quenching is shown in the LI curve of Figure 7-1. The DBR shift with temperature is discussed further in Section 7.3.

An important parameter that is often used to describe the thermal properties of a device is the device's thermal impedance. The thermal impedance parameter simplifies the relationship between the power dissipated in the device and the temperature within that device to a linear equation, Equation 7.1. Using this simple parameter devices' heating parameters can be compared.

$$\frac{\Delta T}{P_{dissipated}} \equiv Thermal\ Impedance \tag{7.1}$$

In an effort to understand what kind of heating to expect from single VCSELs and from arrays of VCSELs, a simple simulation platform was developed. The heating simulation program would provide insight into how devices heated during operation and how heating due to the external sources affects device operation. The goal of the simulation effort was to model the thermal implications of micro-pill integration, and to obtain a resulting thermal impedance from the integration scenarios. Using the heating simulations, a comparison could be made to other techniques used in

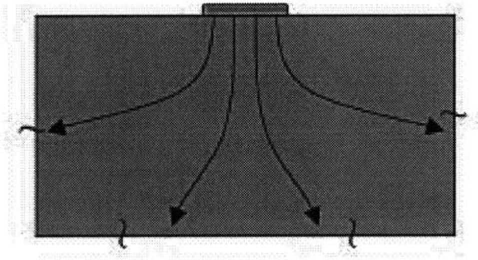


Figure 7-2: Schematic of the simple model for thermal behavior of a VCSEL device

research and in industry. A model was utilized to gauge the affect of aperture size, integration on silicon, integration on oxide films, and device spacing on the thermal characteristics of VCSEL devices. The heating effects were verified by measuring the thermal impedance of fabricated devices. The following section will discuss a simple model for heat dynamics that can be used for VCSEL structures. Section 7.2 will use a more complex model to help predict more accurately the results of integration. A technique for experimentally determining the thermal impedance of VCSEL devices will be discussed in Section 7.3, followed by a discussion of the experimental thermal results in Section 7.4.

7.1 Simple Thermodynamics Model

In order to simulate the temperature within the device several models were considered. A simple model often used in the literature to predict the thermal resistance of a VCSEL structure is given in Equation 7.2 [39]. The simple model's equation idealizes the system as a disc power source on top of a thermal conducting material with infinite boundaries, schematically described in Figure 7-2.

$$Thermal\ Impedance \equiv \frac{\Delta T}{P} = \frac{1}{2D\sigma} \tag{7.2}$$

From the diameter of the power source and the conductivity of the substrate the simple model estimates the thermal impedance of the device. There are several limitations with the model, making the simple model unsuitable for estimating some of

the thermal properties of these integrated devices. One limitation is the simplification of the diameter parameter to that of the aperture size of the active region. The surrounding mirror stack reduces the thermal resistance by some shape factor in actuality. Also, heat generation is not directly at the interface of the substrate, as assumed by the model. There is 4 μm of mirror material between the substrate and the active region above, producing a mixed material system. The simple model also gives no insight into how this material mixing affects the thermal resistance. The model assumes an infinite conductive medium, so smaller systems can not be modeled. In a real system there can be several heat sources producing multiple thermal gradients. To model secondary thermal gradients, isothermal boundaries would need to be specified, beyond which heat cannot be dissipated. A finite element method will add complexity to modeling, but will allow the simulation to reflect the complexity in the integration of pill devices.

7.2 Gauss-Seidel Iteration

In an effort to model integrated VCSELs more precisely, thermal simulations were done using an iterative differencing scheme known as Gauss-Seidel iteration [40]. A 2-D simulation in cylindrical coordinates was used, idealizing the VCSEL and its environment as symmetrical in the θ direction. The result of this simulation is a 2-D mapping of temperatures throughout the device. The model enables an understanding of heating spreading in the device and how each area can impact their characteristic of the VCSEL devices. In the subsequent subsection the specifics of this model and its implementation are discussed, followed by a discussion of the modeled thermal impedance aperture dependence (7.2.2), integration dependence(7.2.3), and bonding interface dependence(7.2.4).

7.2.1 The Model

Equation 7.3 is the second order differential equation describing temperature dynamics in a two dimensional system.

$$\frac{\delta^2 T}{\delta^2 x} + \frac{\delta^2 T}{\delta^2 y} + \frac{\dot{q}}{K} = 0 \tag{7.3}$$

$\dot{q}$ is the heating at a specific point and K is the thermal conductivity. In order to solve Equation 7.3 a finite element method is used. Each element has an initial temperature and heating value. Equation 7.3 is turned into the finite element Equation 7.4.

$$T_i' = (q_i + \sum_j \frac{T_j}{R_{ij}})/(\sum_j \frac{1}{R_{ij}}) \tag{7.4}$$

From this Equation 7.4 a new temperature is defined for each element, using the previous temperature and heating characteristics. Once all of the new temperatures in a space array have been solved, a new iteration is preformed creating a new set of temperatures based on the prior iteration temperature values. The iterations are repeated until a solution is obtained that varies little from iteration to iteration. The variation can be calculated by adding each elements absolute difference in new temperature and old temperature. The run time of this solution depends on the size of the 2-D array, how close the initial condition are to their actual value, and the time can depend on the variation of thermal impedance in the array. A schematic of the VCSEL simulation space can be found in Figure 7-3 (a).

Each element in the array has seven parameters, only two of which can change. The element has an old (T_i) and new temperature (T_i'). Both of these temperatures update with each iteration. The elements also have a thermal impedance ($1/R_{ij}$)value to each of it four nearest neighbors in the arrayed network. Finally each element has a heat source number $\dot{q}$. The last five values mentioned do not change with iteration. The code used for this simulation can be found in Appendix A.

In the iterative simulations there are several assumptions. For one, the outer boundary condition in the radial direction is idealized as non-conductive. The outer

boundary can be considered as either an isolated boundary or a boundary where there is no thermal gradient. At the boundary location, the temperature due to the heating of the outside elements has equaled the temperature due the heating inside the boundary. Though the boundary condition may not result in an exact thermal resistance of a device on its own, the boundary confinement simulates the thermal conditions in an array of devices, which is often the case for VCSEL devices applications. The iterative simulation also ignores convective heat dissipation, and all energy flows to the heat sink at the bottom of the substrate. The model assumes that the temperature across a material boundary is uniform, and only the thermal conduction coefficients are changed. To reduce simulation time, a uniform temperature gradient is assumed in the z direction from the heat sink to 65 μm below the substrate surface. Simulations have shown the error due to the artificial boundary 65 μm below the substrate surface is not very significant. A schematic of the simulated space and results from a simulation run are seen in Figures 7-3 (a) and (b) respectively.

7.2.2 Thermal Analysis of Aperture Dependence

One important feature depicted in thermodynamic VCSEL models is the thermal impedance dependence on aperture size. The thermal impedance dependence is proportional to $1/D$ in the simple model, as described in Section 7.1. The aperture dependence of the thermal impedance was also calculated for the mixed system state using the iterative finite element method. The results of the mixed simulations can be seen in Figure 7-4. Aperture simulations for VCSEL devices on GaAs substrates were also preformed showing the thermal impedance of the GaAs substrate devices were consistently larger than the mixed by .2 $^0C/mW$.

The threshold currents of VCSEL devices are also dependent on the aperture size of the devices, assuming there is a critical current density for the device to lase, $I_t = \alpha\frac{1}{d^2}$. Using data from device measurements, an approximation of the current density threshold was made. The dependence of the threshold current as a function of aperture diameter is plotted along with the thermal impedance simulations in Figure 7-4. This graph suggests that there is an optimal aperture diameter for thermal

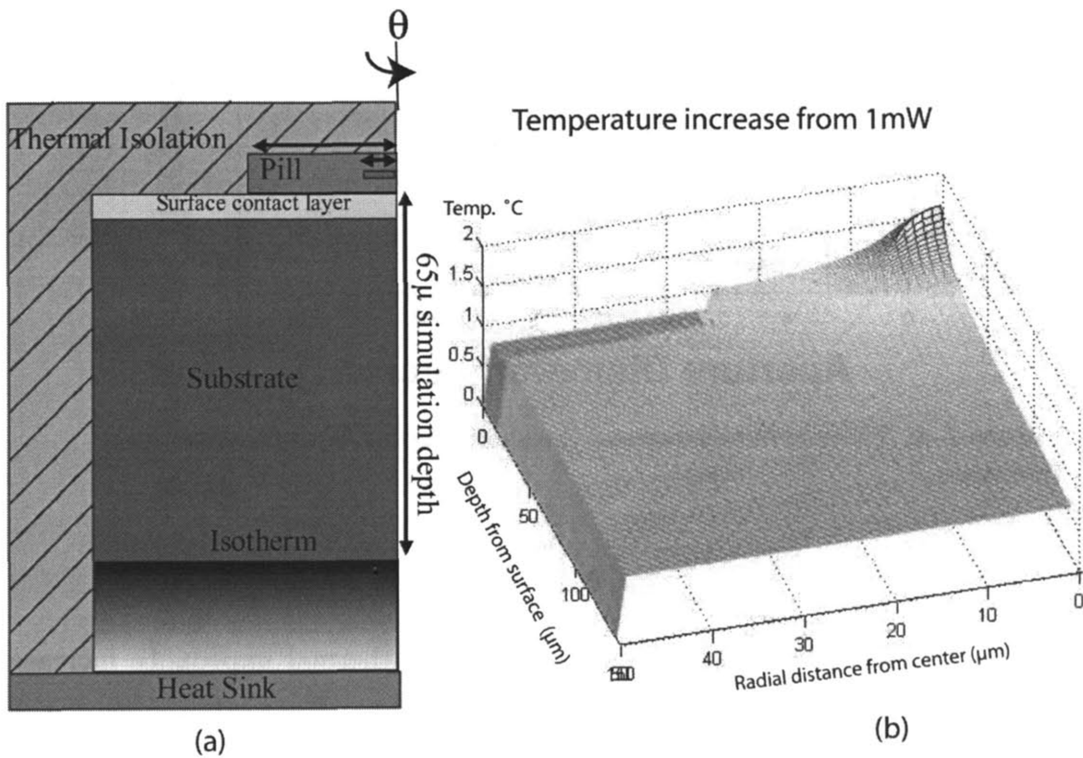


Figure 7-3: (a) A schematic of the simulation space, showing specific aspects of assumptions inherent in the radial thermal isolation boundary, the changeable surface contact layer, and the isotherm 65 μm below the surface. (b) Resulting simulated temperature gradients within of 10 μm diameter aperture with a 50 μm radial isolation for 1 mW power dissipation at the aperture. The peak temperature of 1.6 ^{o}C seen at the aperture. The thermal isolation boundary is seen as a sudden dip in temperature, outlining the pill and substrate.

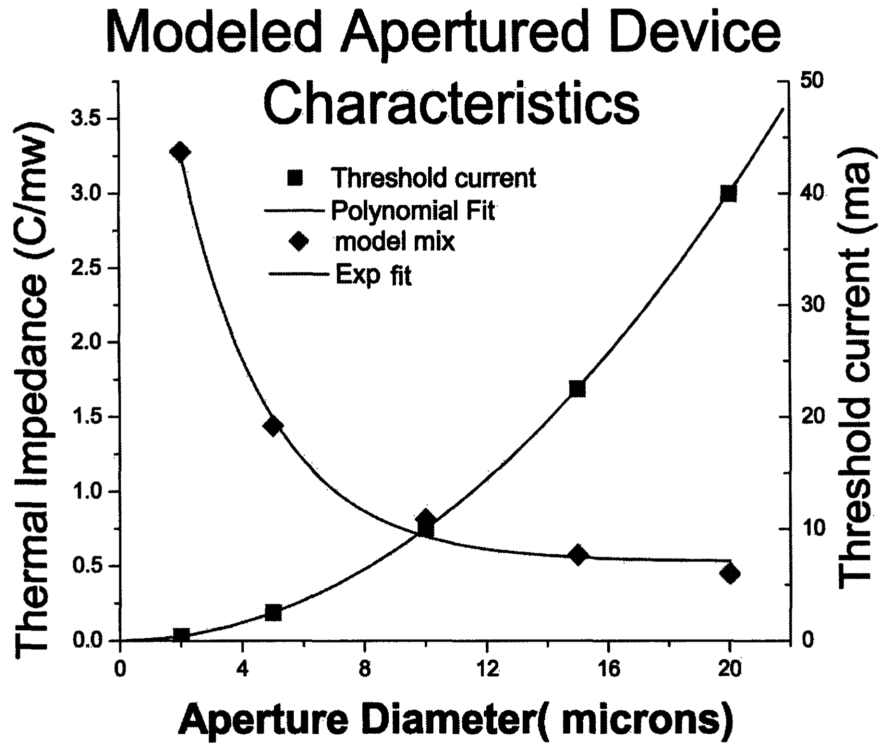


Figure 7-4: Thermal impedance and threshold current dependence on aperture size.

behavior of a VCSEL. If an aperture is too small the thermal impedance increase prevents operation, however if the diameter is too big, the threshold current to too large to be useful.

It can be seen from spectral measurements in Section 7.4 that VCSEL devices begin to fail when their active region reaches 150 °C. Since the temperature of these devices can be calculated from the simulated thermal impedance and the drive power, the drive range of these devices can be predicted. Figure 7-5 shows the temperature of a modeled device at both its threshold current and a common drive current of 10 ma. The modeled device temperatures are plotted for devices with a range of current apertures. For devices with apertures above 10 μm in diameter, the amount of power being wasted to get to threshold is considerable. This figure also suggest that normal device operation begins to be impacted significantly with apertures below 2 μm in diameter, due to the increased thermal impedance.

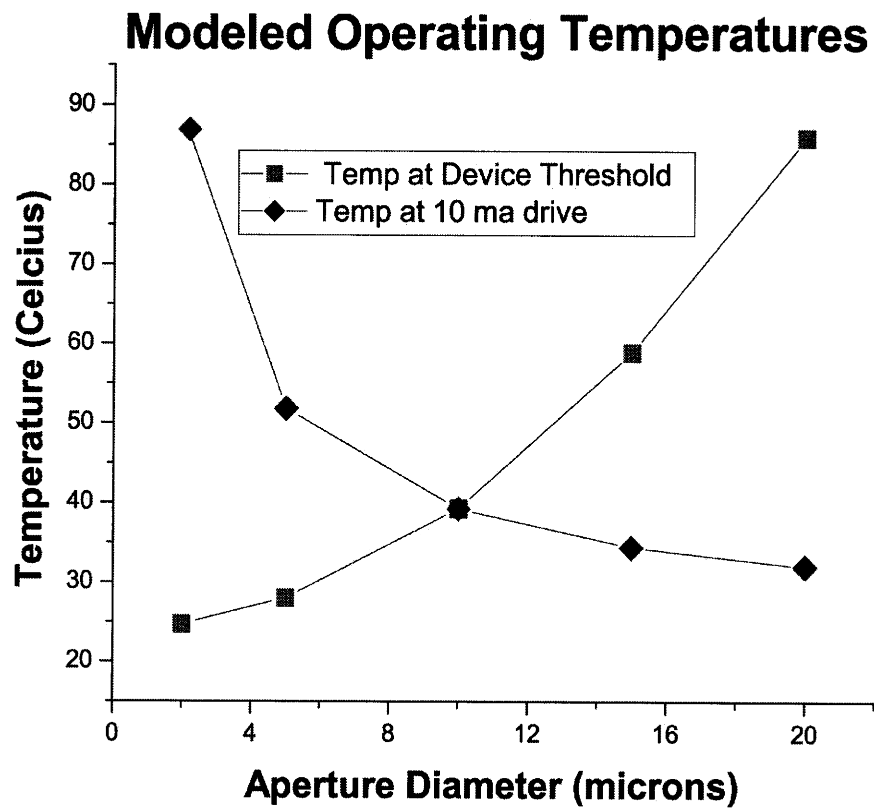


Figure 7-5: Operating temperature of devices as a function of aperture diameter both at threshold, and at 10 ma current bias

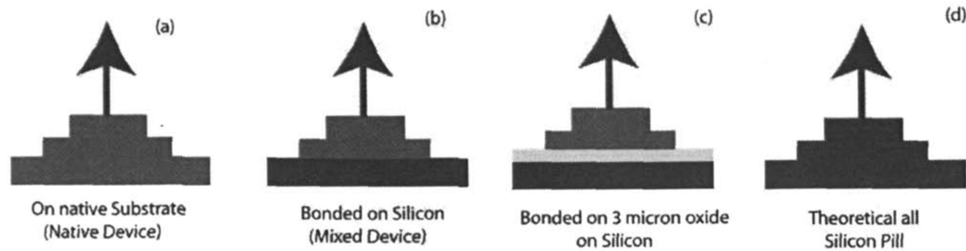


Figure 7-6: (a) Device on its native substrate,(b) Device bonded on Si,(c) Device bonded on oxide,(d) Device freed and unbonded

7.2.3 Thermal Simulation of Integrated Devices

In order to determine how integrating devices onto silicon substrates affects their thermal characteristics, both VCSEL devices on GaAs substrates and VCSEL devices on silicon were simulated. The integration simulations assumed had a pill diameter of 50μm with an aperture diameter of 10 μm. The thermal simulations were performed at various simulation radii, showing how thermal confinement of the VCSEL devices affect their thermal impedance.

The analysis using the finite element model showed a reduction in thermal impedance for III-V device integrated onto a Si substrate. The reduction in thermal impedance was anticipated, since silicon's thermal conductivity (1.3 W/cm/^{o}K) is significantly greater than GaAs (0.3W/cm/^{o}K). The increase in thermal conductivity reduces the temperature difference across the host substrate. Figure 7-7 shows thermal impedance reduction as a function of confinement. The mixed device has a 54% lower thermal impedance compared to a pure GaAs substrate of the same 650 μm thickness, with a radial coonfinement of 50 μm. Since III-V substrates are not usually this thick, a 350 μm simulation was done showing a 1.71 mw/^{o}C thermal impedance, while the mixed device has a thermal impedance of 1.358 mw/^{o}C, 79% the impedance of the regular GaAs substrate device. For a mixed device on a 350 μm thick Si substrate, the thermal impedance is reduced to 1.048 mw/^{o}C, 61% of the GaAs substrate device. Such a Si substrate thickness could be achieved using a backside grind of the substrate. All these simulations were done assuming a 50 μm radial isolated boundary.

The 50 μm radial restriction of the simulation increases the thermal impedance of the devices, overestimating the thermal impedance of an individual device. As

the radial length scale of the simulation is increased, the difference between the simulated and individual impedances is decreased. Calculations were done using large simulation radii and results agreed with those seen from the simple model, which assumes an infinite media. Figure 7-3 shows the dependence of thermal impedance on the simulated radial length scale. For a simulation radius greater than 100 μm on a pure GaAs device, the iterative model agrees with the results of the simple model, designated by a red dashed line in Figure7-3. The iterative model also allows the simulation of the mixed device (III-V devices bonded on silicon substrates as seen in Figure 7-6 (a)), which the simple model does not cover. These simulations show that a single mixed device can have a 25% reduction in thermal impedance due to the silicon substrate, but the mixed device has almost double the thermal impedance of a theoretical all Silicon VCSEL (silicon pill on silicon substrate, as seen in Figure 7-6(d)), reflecting how critical the thermal conductivity of the immediately surrounding material is. The VCSEL device only has to conduct through 4 μ of III-V material, but the surrounding area dominates the thermal behavoir. Any further reduction in the impedance of the material within microns of the aperture will improve the thermal charcteristic significantly.

When these devices are modeled is an array, the advantage of this mixed integration becomes greater. Due to the larger thermal conductivity of the silicon there is less thermal cross talk between devices. Devices on a GaAs substrate confined at a radius of 45 μm have their normal unconfined thermal impedance doubled. This radial confinement corresponds to an array period of 90 μm. The thermal impedance of the mixed devices is not doubled until the radial confinement is reduced to 33 μm or less, corresponding to a 66 μm period. In the infinite medium regime, the mixed device only reduces the thermal impedance by 25%, however at an array pitch of 60 μm the thermal impedance is halved for the mixed devices.

The results of the simulations shown in Figure 7-3 suggest the Gauss-Seidel model implemented verifies the simple model's thermal characteristics, while also enabling the modeling of complex systems like the mixed device, that the simple model cannot simulate. The Gauss-Seidel simulations suggest mixed integration reduces thermal

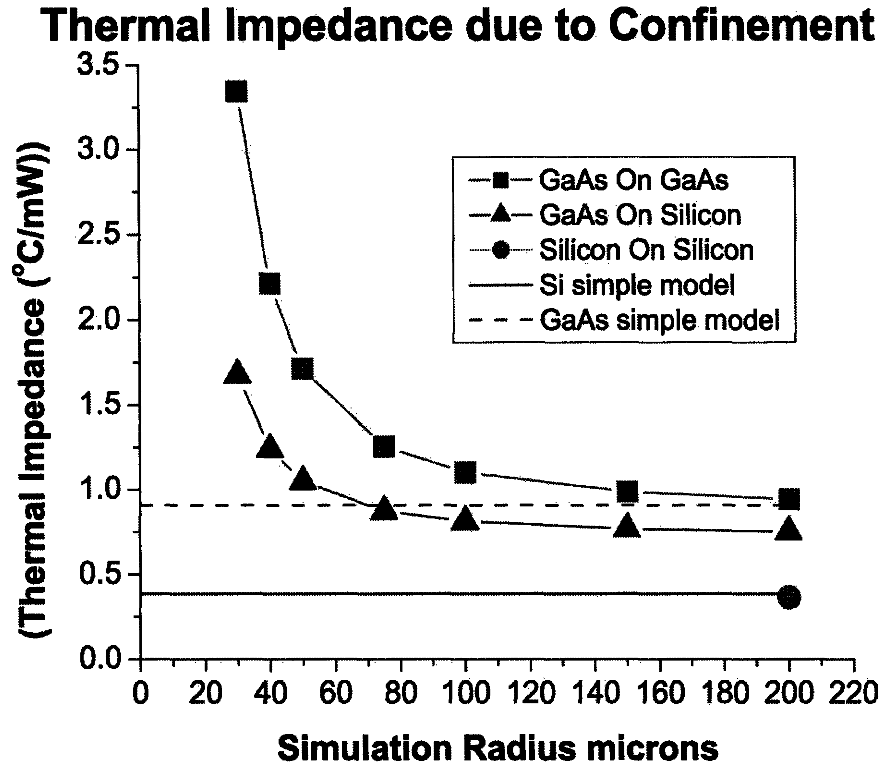


Figure 7-7: Thermal impedance as a function of simulation confinement. The results are confirmed by the simple model at large confinement lengths.

impedance, and potentially allows for tighter array pitches.

7.2.4 Integration on Oxide films Simulations

Different integration techniques vary in the placement of the devices on the IC circuit. Some techniques, like flip chip bonding and ELO, bond onto the dielectric stack of the silicon IC, while pick and place assembly and MASA techniques integrate into wells on the IC. Ideally the integration wells reach within the dielectric stack, close to the silicon substrate, reducing the effect of the highly thermally resistive dielectric, (SiO_2 has a thermal conductivity of .011 W/cm/^{o}K [41]). The Gauss-Seidel model was used to simulate the effect a dielectric intermediate layer would have on the thermal impedance of the device. A layer with thermal conductivity of .011 W/cm/^{o}K was placed at the bond interface as shown in the schematic of Figure 7-3 and simulations were run with different thicknesses of this layer. The results of oxide simulations can be found in Figure 7-8, showing integration on oxide films is a concern. Film

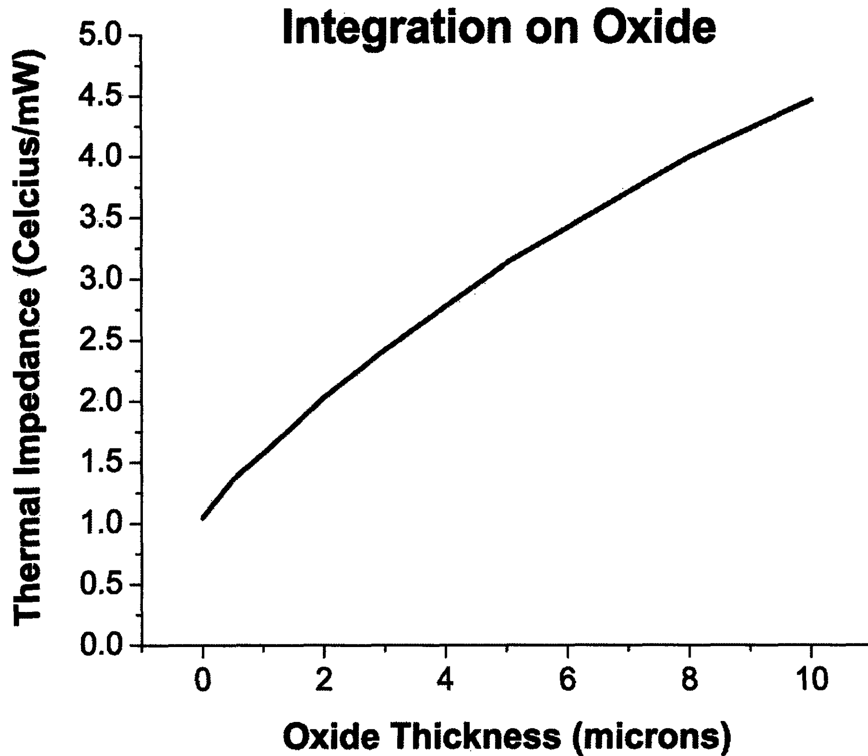


Figure 7-8: Thermal impedance dependence on interface oxide layer thickness

thicknesses on the order of a few μm significantly impact the thermal properties of the device. The thermal impedance doubles with a mere 2 μm of oxide, which is thinner than most IC back end dielectric stacks. To prevent the oxide film from dominating the thermal characteristics when integrating on thick oxide, metal lines and plugs have to be used to conduct the heat into the substrate. Confirmation of this model with measurements of VCSEL devices on oxide films can be seen in Section 7.4.2.

7.3 Thermal Impedance Measurement

To confirm and compare thermal simulation results to actual device characteristics, the thermal impedance of VCSEL devices can be measured. One common method of determining the thermal impedance in VCSEL devices is to use the frequency shift of the mirror stack induced by heating to determine the shift in temperature. The DBR mirror resonant frequency shift can be obtained both by theoretical and experimental

methods. The device emission shift as a function of input power can then be used to determine a power versus temperature linear relation, from which the thermal impedance of the device can be calculated.

The output frequency of these devices can be measured using the same probe station set up described in Chapter 6 Section 6.1. The output spectrum can be measured by replacing the silicon photodetector with a spectrometer. The spectrometer used in this setup was an Ocean Optics [42] USB2000 portable spectrometer. A five foot optical fiber was used to direct the light into the spectrometer. This detector has an accuracy of about .4 nm. The spectrometer data was collected on a laptop running SpectraSuite made by Ocean Optics [42], communicating to the spectrometer through a USB port.

Equation 7.5 shows the theoretical dependence mirror frequency shift as a function of temperature [39].

$$\frac{\delta\lambda_n}{\delta T} = \lambda_{no}(\frac{\delta(n/n_o)}{\delta T} + \frac{\delta(l/l_o)}{\delta T}) \tag{7.5}$$

There are two main components of to the thermally induced frequency shift in a VCSEL DBR represented in Equation 7.5. The index of refraction of the material in the DBR is a function of temperature, and induces a shift to longer wavelengths (red shift) when heated. The semiconductor material also expands due to the increased heating, contributing to the long wave length shift. Using a linearized index change and thermal expansion change as a function of temperature obtained from GaAs properties [43], this equation can be evaluated to find that $\frac{\delta\lambda_n}{\delta T} = \lambda_{no}5.05 \cdot 10^{-5}K^{-1}$, where λ_{no} is the DBR resonant wavelength of the VCSEL device. The calculation predict a mirror shift of .0429 $\frac{nm}{^\circ K}$ in a device emitting around 850 nm, as shown in Equation 7.6.

$$\frac{\delta\lambda n}{\delta T} = .0429\frac{nm}{^\circ K} \tag{7.6}$$

Experimental measurements of the thermally induced DBR shift were also obtained. A device substrate was placed within the probe station on top of a heater. The temperature of this heater could be controlled by applying a voltage bias across

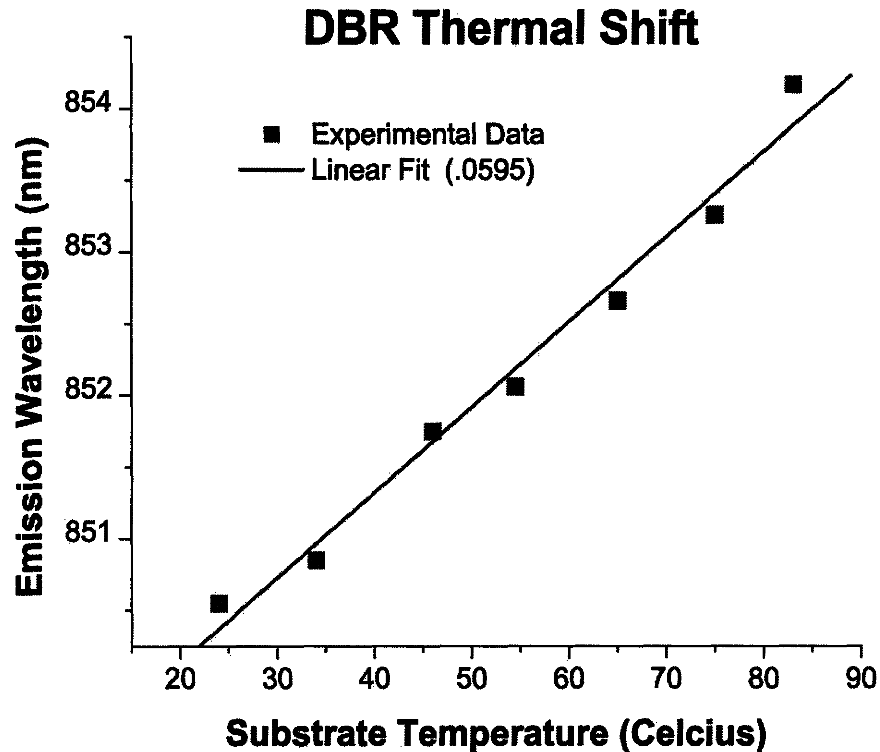


Figure 7-9: Peak emission shift of a bonded device on a heated substrate, biased at 4 mA .

the heater stage, while the thermocouple attached to its surface measured the surface temperature. The vacuum system on the probe station held down the heater, providing a good thermal contact the metal chuck. Devices on the heater could be probed, driven, and their light emission detected using the spectrometer set up. A stable, low level biased, DBR confined spectrum was obtained from the device. The temperature of the heater could then be changed, and the spectral shift could be observed. The DBR shift experimental set up assumes the heating from the bias current does not change as the temperature of the device is changed, essentially requiring that the efficiency of the devices is not changed significantly by the temperature increase, which is a reasonable assumption for low level heating. Figure 7-9 shows the results of a DBR thermal shift experiment. A device bonded on a silicon IC was biased with a 4 ma current, while the substrate was heated up from room temperature to 83°C. Using a linear fit to the data, a slope of $17^o K/nm$ suggesting the emission peak shift as a function of temperature was $17^o K$ per nm shift, which confirmed previous measurements. The above theoretical analysis predicted a shift of 23 °K/nm , however

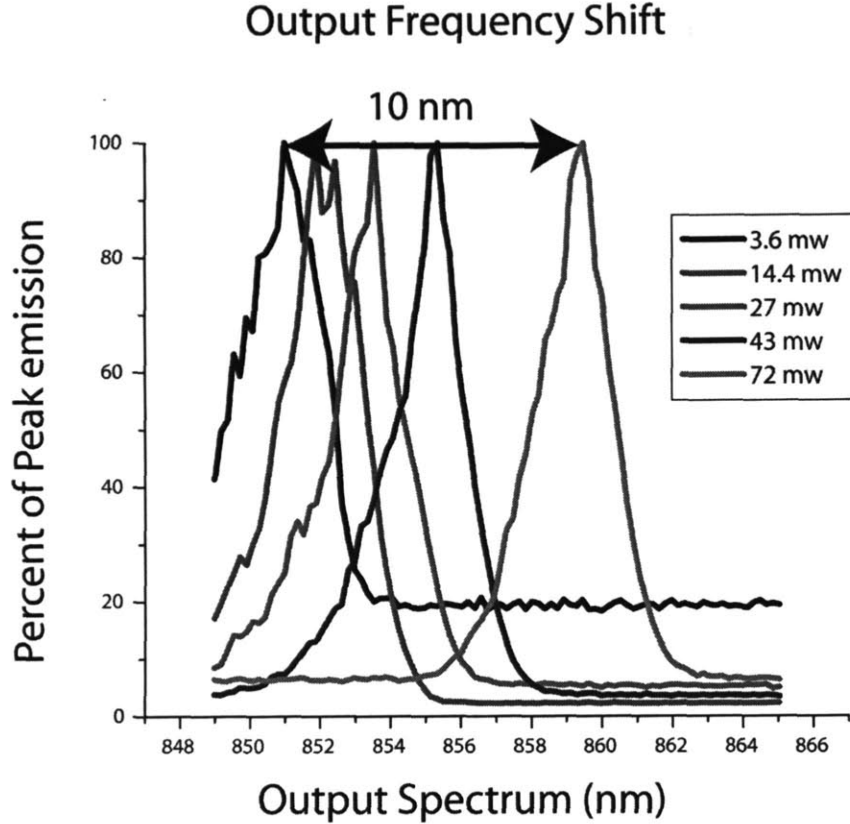


Figure 7-10: Normalized output frequency of a device driven with increasing current. A shift of 10 nm is observed

inaccurate material constant assumptions in the equations may be the source of this discrepancy.

Once the DBR thermal characteristics are analyzed, the output frequency shift as a function of input power can be used to determine the thermal impedance of a device. Figure 7-10 shows the spectral shift versus power in an early VCSEL device integrated onto silicon. The total shift is seen to be 10 nm over 70mw. Using the spectral shift result and the DBR characteristics discussed previously, Equation 7.7 calculates a $2.4\frac{^\circ K}{mW}$ thermal impedance.

$$\frac{\delta T}{\delta P} = \frac{\delta T}{\delta \lambda_n} * \frac{\delta \lambda_n}{\delta P} = \frac{\delta \lambda_n}{\delta P} * 17\frac{^\circ K}{nm} = \frac{10nm}{70mW} * 17\frac{^\circ K}{nm} = 2.4\frac{^\circ K}{mW} \tag{7.7}$$

The thermal impedance measured using this technique is somewhat large when com-

pared to expected values of around $1 \frac{^\circ K}{mW}$ form the simulations and native substrate device. However, the device analyzed was an early two-tier bonded device with poor heat sinking. Bonded devices exhibiting good thermal impedances were obtained in this thesis work and will be discussed later in this chapter.

7.4 Experimental Thermal Impedance Results

Thermal impedance measurements done in this study were performed on single devices, confining our study to the infinite boundary case. Separate experimental studies must be done to verify the thermal characteristic modeling results which took thermal cross talk into account for in arrayed devices. Measurements were done to see how well the iterative model predict the characteristics of integrated devices and the effect of integration parameters such as aperture size and bonding interface. The following subsection will discuss the measured aperture dependence found by experiment. Subsection 7.4.2 will discuss oxide dependence, while the bonding interface experimental results will be discussed in Subsection 7.4.3. Finally a summary of experimental results will be discussed in Subsection 7.4.4.

7.4.1 Measured Aperture Dependence

Thermal impedance measurements of several bonded devices with varying threshold current were obtained. Each device was bonded with indium onto silicon or a silicon IC. Since the device's threshold is easier to determine than its aperture diameter, the model graphed in Figure 7-4 was condensed into thermal impedance as a function of threshold current. The thermal impedance dependence on threshold current is plotted in Figure 7-11 along with the thermal impedance measure devices. As seen from the figure, the 1 mA and 2.5 mA devices show good correspondence to the model. These devices were single tiered and processed fully on a silicon IC(Devices 21 and 11 respectively). The devices shown with the 7.5 mA and 15 mA threshold were earlier two-tier devices, their processing non-ideal. However since the single-tier devices had very little spread in threshold current, only older devices were available for measure-

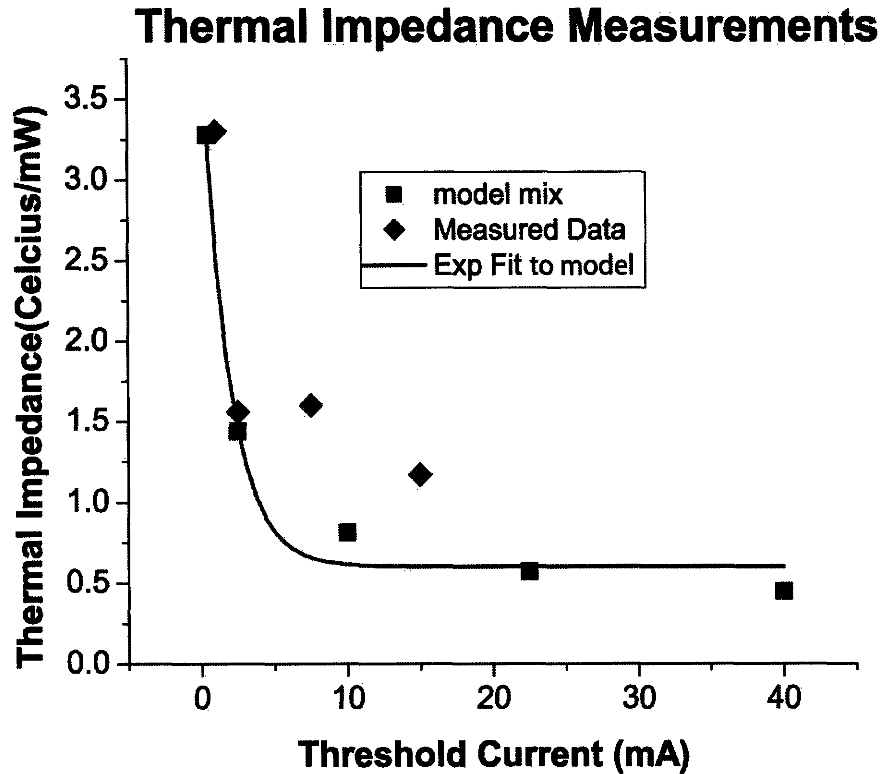


Figure 7-11: Modeled impact of device threshold current on thermal impedance. The measured data confirms the modeled trend. An exponential fit to the modeled data is also shown as a continuous line.

ments at high threshold currents. The model in Figure 7-11 provides a lower bound for the impedance of the device, any non-ideal bonding would increase the impedance of the device. The thermal impedance measurements of the VCSEL devices show the model accurately estimated their thermal impedance, while also suggesting the integration technique provided a good thermal bond to the target substrate. Overall these measurements suggest the thermal impedances of these integrated devices are on par with other integration techniques which have thermal impedances as low as 1 ^{o}C/mW [9].

7.4.2 Oxide Dependence

Measurements were done to determine how well the finite element method models the influence of oxide film on thermal impedance. Single tier device were bonded onto silicon substrates with 3.3 and 5.5 μm of oxide on top. The thermal impedances of

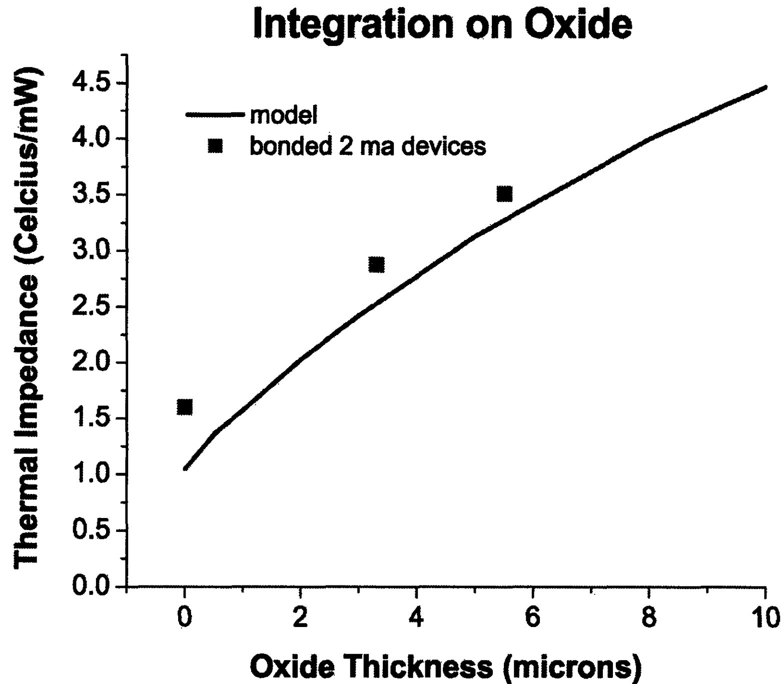
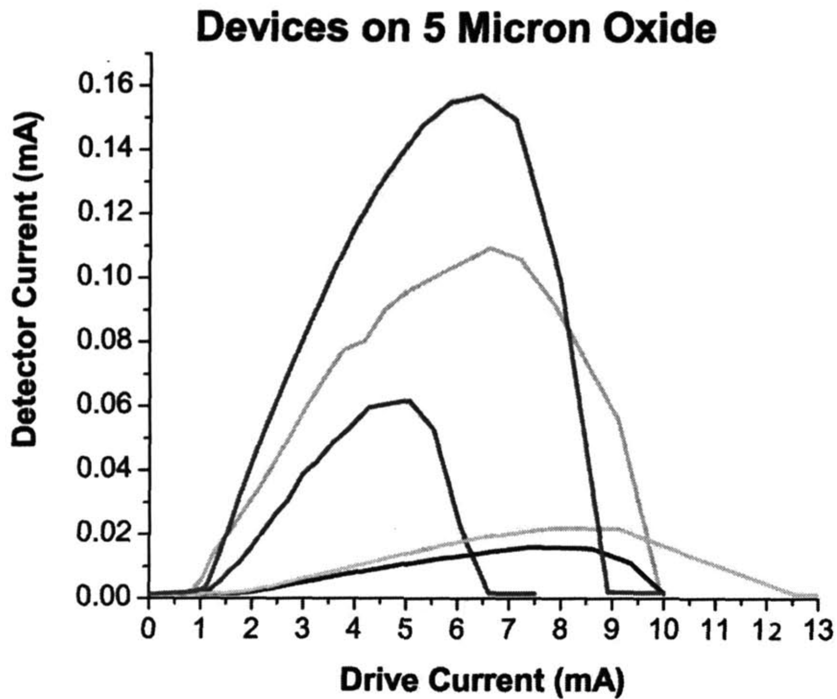


Figure 7-12: Measured devices confirm the affects of oxide film on thermal impedance.

these 2 ma threshold devices were measured. Two devices within this study were chosen and plotted along with their thermal impedance of a device directly on the silicon IC. Figure 7-12 shows good agreement between the measured thermal impedances of devices integrated on oxide films and the finite element model predicted impact of integrating on a dielectric. The measured devices are consistently .5 $^oC/mW$ above the predicted value, this is most likely due to a difference between the model device aperture size and the aperture size of the devices which were measured.

For each of the 3 and 5 μm film thickness measurements, five devices were bonded. The LI curves of all devices in this study are shown in Figure 7-13. The devices with the least thermal resistance were chosen for the model comparison in Figure 7-12. Choosing the low thermal impedance devices ensured the compared devices had similar aperture sizes, while also choosing devices with the best bonds to compare with a model that idealizes this bonding interface. Figure 7-13 shows all the devices in the oxide bonding study were significantly affected by the oxide film, limiting emission of 3 and 5 μm device below 15 and 12 ma respectively.



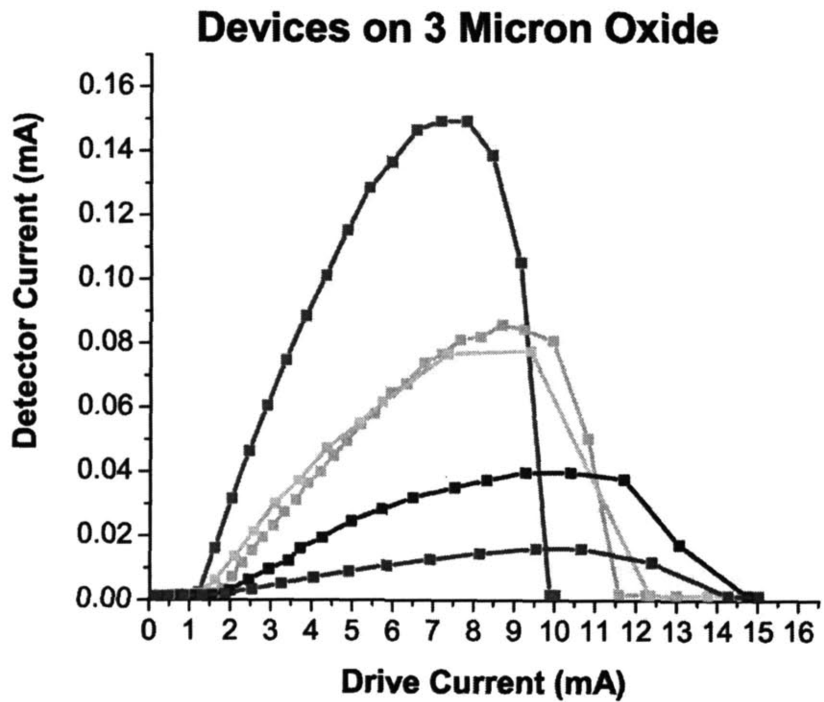


Figure 7-13: LI curves of the devices on the oxide study. High threshold devices were chosen for Figure 7-12 to minimize aperture dominance of the thermal impedance. Top: devices on 5 μm oxide. Bottom: devices on 3 μm oxide.

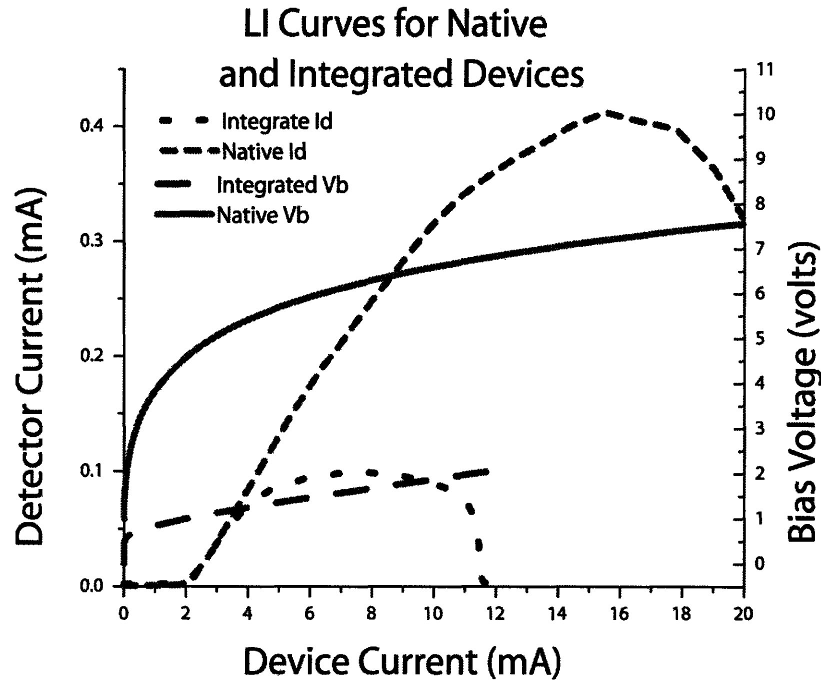


Figure 7-14: LI curves of two 2 ma threshold VCSELS, one on a native substrate, one integrated using 30 nm AuSN

7.4.3 Bonded Interface Dependence

Preliminary bonding experiments using a thin gold tin eutectic discussed in Chapter 5 Section 5.3.2 showed varying results. Two devices with the same threshold currents have LI curves shown in Figure 7-14. One device was measured on its native substrate and outputted optical power past 20 ma, while the second was a bonded device and could not emit past 10 ma. The importance of this bonded interface is revealed by the drive current differences. The results obtained from Figure 7-14 suggested a better bond was needed, thus 500nm of Indium was used.

A study was preformed to characterize the thermal implications of this indium bonded interface. The indium bond study integrated 10 two tier devices onto a Si substrate using 500 nm of Indium. Pills were on a flat surface, no wells were present. LI curves and thermal impedance measurements were taken before and after the thermal bonding treatment. Not all 10 devices exhibited lasing characteristics, due to VCSEL device abnormalities, but all devices emitted light and all showed improvements in their drive range after bonding. Figure 7-15 shows one of these devices. The

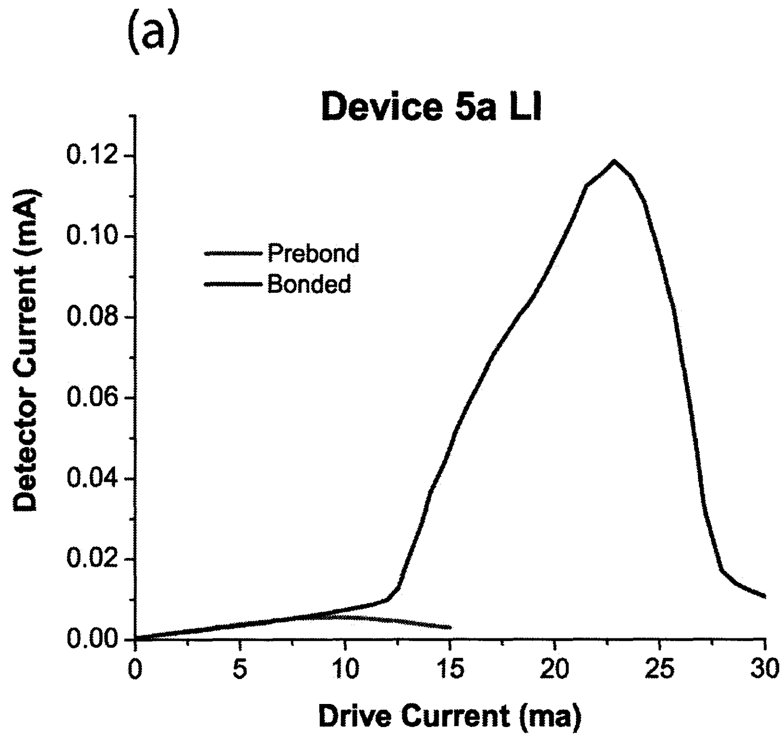
operating current drive range is nearly doubled after bonding, allowing this device to reach its 10 mA threshold current. Figure 7-15 also shows the corresponding increase in slope for the input power vs. peak output frequency graph, showing the decrease in thermal impedance that allowed this high drive current.

The indium bond study also revealed an interesting phenomenon associated with the thermal heat sinking. An increase in the threshold current of some devices appeared to increase after bonding in the indium bonding study. The increase in threshold current can be seen in Figure 7-16. Before bonding the device shown lased at 7.5 ma, while after bonding a 13 ma threshold current was seen. The device cooling introduce by the indium bond decreased the thermal impedance of the devices such that the peak emission of the active regions was no longer tuned to the mirror stack. In order to confirm this theory, LI curve were taken while the substrate was heated. The substrate heating would retune the device, pushing the mirror back within the rang of the active region gain curve.

Figure 7-16 shows the resulting data from this experiment. The lower threshold current is regained only after heating the substrate to 55 ^oC. The increase in threshold current was not a wide spread phenomenon, however the results of the experiment seen in Figure 7-16 suggest that there was significant variation in the mirror growth material, creating a detuned device at lower temperatures.

7.4.4 Summary of Results

The main goal of this thermal analysis work was to determine how these micro-pill devices compare to devices on native substrates and to those integrated by other integration techniques. Thermal simulations show that these devices should preform as well as or better than native devices, and hold a thermal impedance edge over devices bonded onto thick dielectrics. Through improvements in device processing and device bonding, it has been shown that these simulations were in fact correct, devices with low thermal impedances can be produced. The two main factors in determining a devices thermal impedance are its aperture size and its bonding interface. Figure 7-17 contrast devices in different states, and show their resulting thermal characteristics.



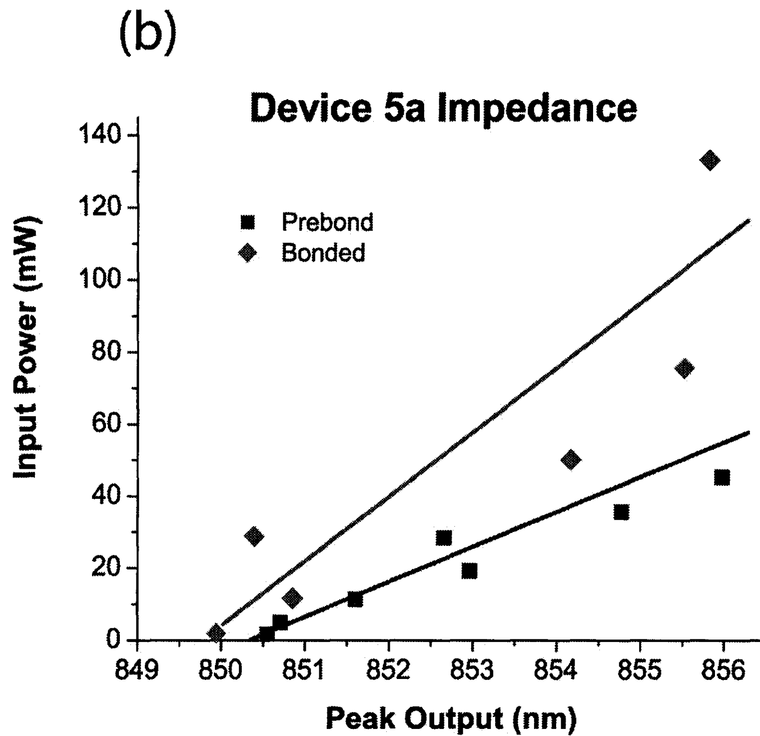


Figure 7-15: (a) LI curves of a device before and after indium bonding. Drive current range is significantly increased due to bonding. (b) Power vs. peak emission data from device before and after bonding. The increase in slope indicates a decrease in thermal impedance.

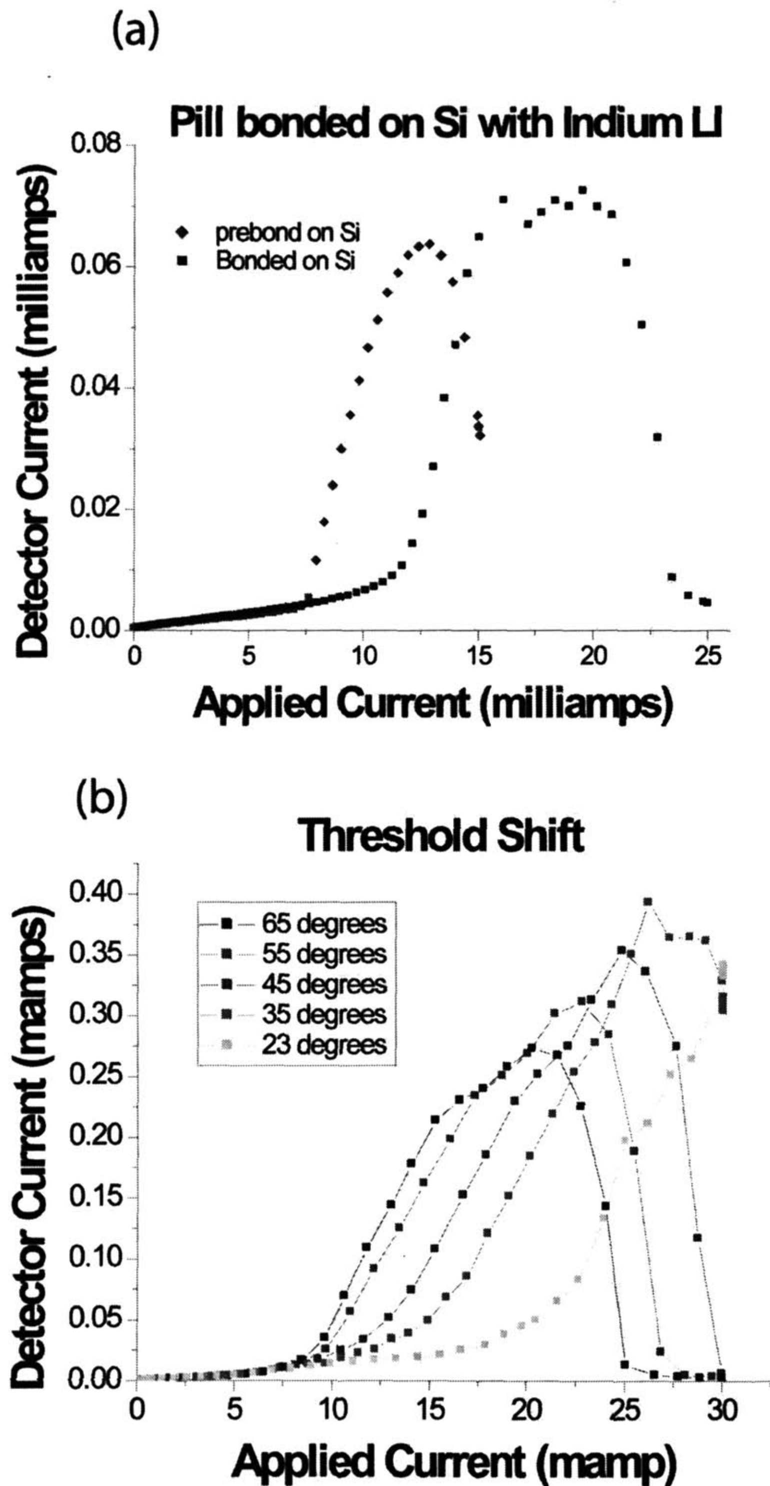


Figure 7-16: (a) an increase in threshold current is seen in the LI curve after the device is bonded. (b) The threshold current is returned to its previous state by heating the device, suggesting the DBR is out of tune for low temperature operation.

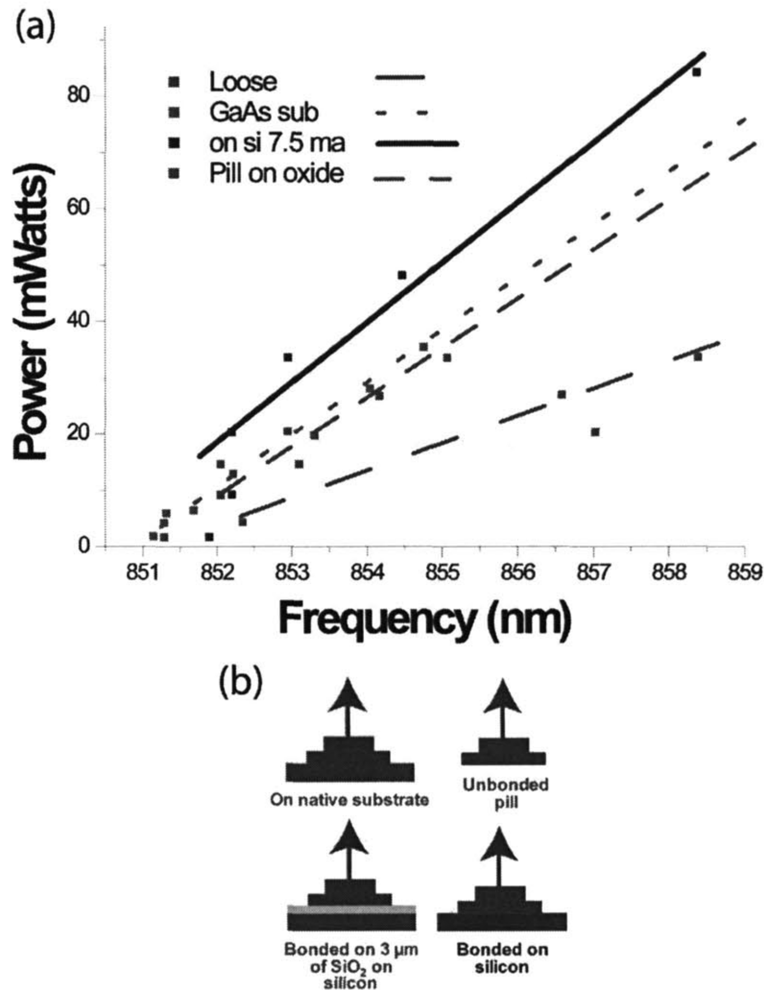


Figure 7-17: (a) Thermal impedance data from a variety of devices integrated differently. A larger slope suggest a smaller thermal impedance. (b) Schematic depicting device integration states

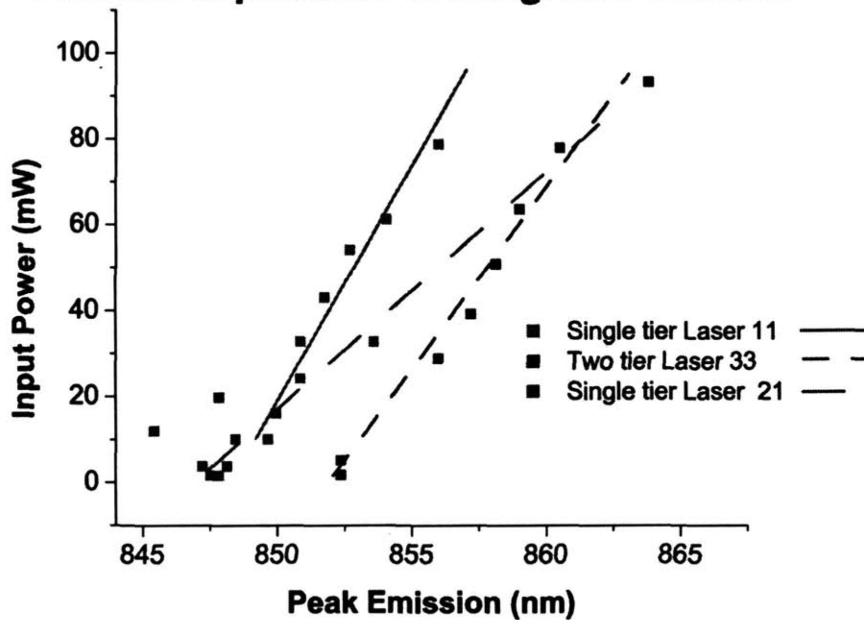


Figure 7-18: Thermal impedance data from 3 devices integrated onto ICs , demonstrating the input power attainable from these devices. Device 33 was a 2 tier device, while devices 11 and 21 were single tier fully integrated devices.

The devices compared include lasers on GaAs, loose, bonded on Oxide, bonded on silicon.

Thermal characteristics of devices bonded onto silicon ICs were also measured. The results from the IC measurements can be seen in Figure 7-18. The IC integrated devices showed very respectable thermal impedances. The two tier Device 33 on Sample T-In-400, was integrated using indium and had its top contact probed. Device 33 has a 2.5 ma threshold current and a thermal impedance of 1.8 °C/mW. Both devices 11 and 21 were fully integrated and bonded using 500nm AuSn on Sample S-Au-500. Device 11 had a threshold current of 2.5 ma and a thermal impedance of 1.5 °C/mW, while device 21 had a threshold current of 1 ma and a thermal impedance of 2.5 °C/mW. Table 7.1 shows the measured thermal impedances for these devices compared to those devices in Figure 7-17. The fully processed Laser 11 compares quite favorably to the other devices in this study and in literature [9, 14, 13]. Laser device 21 also had a very low thermal impedance when taking into consideration its 1 mA threshold current.

Table 7.1: Thermal Impedance Results

Structure	I_t mA	Thermal Impedance(^{o}C/mW)
On GaAs	2.5	2.1
Loose	7.5	4.0
Bonded on Oxide	2.5	2.9
Bonded on Silicon	7.5	1.6
Indium bond on Chip (LASER 33)	2.5	1.8
AuSn(400nm) bond on Chip (LASER 11)	2.5	1.5
AuSn(400nm) bond on Chip (LASER 21)	1	2.5

Chapter 8

Conclusion

The main goal of this work was to integrate III-V VCSEL micro-pill heterostructures into commercially processed ICs, using novel hybrid assembly techniques. Such a technology could enable optical interconnects on silicon ICs. Fully processed VCSELs were fabricated and successfully integrated within commercially fabricated silicon CMOS devices. The thermal, electrical, and optical properties of the integrated devices were studied. The integrated device characteristics revealed little or no degradation in devices properties from native substrate VCSEL device operation to fully integrated device operation. The integration techniques used in this work are still in their infancies, however many integration obstacles have been overcome. A fabrication technique providing high yield VCSEL pill devices has been developed. A new bonding apparatus and metalization has been explored, modified, and successfully used on these micro-pill devices. Techniques for post assembly processing assembled devices have been successfully implemented. A model has been developed and used to simulate the thermal characteristics of integrated devices, and the results of this model have been confirmed by thermal measurements. Finally, a measurement tool was developed to analyze the forces associated with magnetically assisted statistical assembly. The resulting measurements showed forces similar to those predicted by modeling. However variations in force magnitudes were seen. Section 8.1 will summarize the results of this work, while Section 8.2 will point to future efforts to improve these technologies.

8.1 Summary of Results

Chapter 3 discussed a sensing system that has been developed to measure the stiction force used in magnetically assisted statistical assembly. The sensing system uses a micro-cantilever (fabricated in MTL [44]) with a Ni film to interact a magnetic substrate. As predicted from MASA modeling, a force is induced on these cantilevers, the induced force can be measured from deflection of the cantilever device. A process scheme was developed to produce the sensing cantilever system. The spring constants of the produced cantilevers were measured and an interacting force from a silicon substrate with a patterned samarium cobalt thin surface film [24] was measured. The magnetic film measurements confirmed the predicted magnitude of the retaining forces modeled in previous work, while also showing the variation in induced the pressure (300 nt/m^2 to less than 20 nt/m^2). The measured pressure range can be attributed to variation in the patterned magnetic film.

A processing sequence for single tier micro-pill VCSEL devices have been produced, a description of which can be found in Chapter 4. The single tier devices are designed to be 40 μm in diameter and 8 μm in height. A method of growing an oxide current confinement layer was developed and refined, finally producing device threshold current ranging from 1 to 2 mA. Non-destructive measurement tools were developed to study these oxides, allowing the measurement of the oxide front and determining oxidation rates without breaking the devices. An oxidation reinsertion step was also used to help control and produce well apertured devices. Metalization techniques were developed that allowed low resistant ohmic contacts to both the n-contact and p-contact layers resulting in contact resistances less than $2 \cdot 10^{-4} ohm - cm^2$. Backside metalization techniques were investigated and implemented, producing the n-contact and bonding metal on the bottom of the device, eliminating the need for a second top contact. This technique has been improved by the use of WaferBOND^{tm} [25], making backside metalization reliable and reproducible. The pill devices produced using the these processing techniques show threshold currents between 1mA - 2.5 mA, and all integrated devices tested exhibited lasing characteristics. The vari-

ation seen in the devices could be attributed to differences in device dimensions due to variation in the wet tier etch.

As reported in Chapter 5, the integration of these devices into silicon CMOS was also successful. A process was developed to etch recesses within the dielectric stack of silicon ICs fabricated by MOSIS [45]. The IC recesses were etched to the aluminum metal layer target pad and a bonding metalization was integrated within. Both Indium and AuSn were tested as bonding metals, and showed good bond characteristics for layer thicknesses on the order of 500nm. The Bonding apparatus designed by Prof. Fonstad and Mindy Teo [1] was modified to produce more consistent bonds and allow higher bonding pressures. Bonding improvements were seen, allowing more than 75% of device to be consistantly bonded. A post-bonding process utilizing BCB and PECVD oxide was used to successfully conneact the top p-type contact on AuSn bonded devices to the IC circuit, allowing full control of these devices from the aluminum bond pads on the IC circuit.

The bonded devices have been characterized and show optical electrical and thermal characteristics similar to those of devices on native substrates. The bonded VCSEL devices show low threshold current lasing and some showed a continual optical emission beyond a 20 mA drive current. The devices' measured thermal impedances varied with aperture size, but integrated devices with impedances as low as 1.6 mw/^{0}C could be produced. The thermal impedances measured are similar to what the best integration techniques can achieve, and the impedance measurements are also similar to devices that were measured on their native substrates. Full device characterization can be found in Chapters 6 & 7

Modeling of the thermal characteristics took place using a Gauss-Seidel iteration method. The results of the iteration modeling help characterized the effect of aperture size, mixed materials, and surface interface on the thermal impedance of these VCSEL device. The Gauss-Seidel modeling showed a potential thermal impedance improvement of 20% for III-V VCSELs on integrated a silicon substrate over III-V VCSELs devices on their native GaAs substrates, modeled under unconfined conditions. The mixed material systems shows even greater improvement over native

devices when the device's thermal gradient is confined to its surrounding area on the substrate surface, which is the case for devices operating in an array. For devices with confinement, a 50% decrease in thermal impedance is seen for a mixed device in a 60 μm pitched arrayed. Modling shows device integration on 2 μm of oxide can double the thermal impedance of 10 μm aperture device, the modeling preformed was confirmed by measurement. The aperture dependance of thermal impdance was also measured confirming the modeled behavior. Overall, these VCSEL devices showed continual optical output up to tempertures of 150 ^{o}C.

8.2 Future Work

In order for this pill development technology to reach its full potential, the assembly of devices needs to become highly parallel. This work has shown the potential of an assembly system like MASA, but the MASA integration technique needs to be analyzed further. Films which induce consistent forces across a substrate are needed to enable the integration of thousands of devices at a time. Patterning techniques also need to be investigated to improve these forces, and possibly help in alignment of assembled devices. As mentioned in Chapter 3, much work can be done to improve these simple cantilever devices, and investigations need to be made into measurements that can be used to preform more accurate measurements using these devices.

As suggested in Chapter 4, there are several changes that can improve yield of the devices produced, while also decreasing the variance in their characteristics. A dependable and smooth reactive ion etch (RIE) process needs to be developed to reduce the undercut and reduce the cone shape of the devices produced in these trials. Currently the spacing between the devices is 135μm, however a spacing of 45 μm could be used if a low undercut etch was found. The backside substrate removal process also needs improvements. Currently the H_2SO_4 / H_2O_2/ H_2O etch tends to etch unevenly. Simply increasing the etch stop layer from 300nm to 600 nm would improve this step. However changing the etch condition may also improve the results. Better alignment and wide coverage is needed during the backside metalization alignment. Clumping

of the devices is the major issue, one that needs to be solved in order for fluidic type assembly to occur. The cause of clumping needs to be determined. If pill clumping can be reduced, pills are free to flow, and it has been shown that fluidic type assembly occurs much more readily.

The integration steps for these pill devices, as laid out in Chapter 5 could use improvement in several areas. In order to obtain more consistent bonding results, more trials needs to be done with the bonding metalization, especially the gold tin contact. Bonding pressures need to be increased to at least 55 PSI and in order to reach these pressures modifications need to be made to the bonding setup. Further refinement of the post processing steps are required. A thicker BCB might be appropriate as way to protect the devices during metal wet etches are required. Use of a sputtering system that has aluminum deposition available would be key to reducing the contact resistance seen in these top leads.

Appendix A

Thermal C++ Code

```
#include "stdafx.h"
#using <mscorlib.dll>
#include <iostream>
#include <complex>
#include <fstream>

using namespace std;
//using namespace System;


FILE *stream;

int main()
{
int num = 120;
int numj = 146;
double rfactor = 2;
double zfactor = 32;
double numjd = numj;
```

```
    double **T;
double **Tnew;
double **Cmm;
double **Cmp;
double **Ckp;
double **Ckm;
double **Q;
double error=0;
//.00005;  // in cm
double Ks = 1.3;//; // k in w / cm /k
double Kg = .5;
double Kox = 3.2;// usually .011
double Kal = 2.37;
double K = 0;
double phi = 2*3.1415927;
double pi = 3.1415927;
double subthick = .035;
double simthick = .0065;// normally .0065
double radialthick = .01;// simulation radius
double intthick = .0000;//oxide thick  usually 0

double pillrad = .0025;
double pillhi = .0005;//usuallly .0008
double aprad = .0005;
double bot =(numj);
double interval = (simthick+pillhi)/bot;
double holder2;
//if(num*interval>=radialthick){
num = radialthick/interval/rfactor;
//}
```

```
int iexpan = (radialthick/interval/rfactor-num)/(zfactor-1);
double iexpan2 = (radialthick/interval/rfactor-num)/(zfactor-1);
//iexpan = 0;
printf(" blah %f \n" , iexpan2);
//double inf = 900000000000000000;
//printf("int %e",interval);
T = new double* [num];
Tnew = new double* [num];
Cmm = new double* [num];
Cmp = new double* [num];
Ckp = new double* [num];
Ckm = new double* [num];
Q = new double* [num];

ofstream file;
    file.open("out.dat");
file <<"helloworld"<< endl;
int i;

for (i=0; i<num; i++){

T[i] = new double[numj];
Tnew[i] = new double[numj];
Cmm[i] = new double[numj];
Cmp[i] = new double[numj];
Ckp[i] = new double[numj];
Ckm[i] = new double[numj];
Q[i] = new double[numj];

}
```

```
int j;
double radius;
for (i = 0; i<num ; i++){

for( j=0; j<numj ; j++){

radius= (i+.5)*interval*rfactor;
T[i][j] =0;
Tnew[i][j] =0;
//if (j<pillhi/interval){
K = Ks;
//}
//else{
// K = Ks;
//}
if (i==0){

Cmp[i][j] =(radius+interval*rfactor/2)*K/rfactor;
Cmm[i][j]= 0;
}

else{

Cmp[i][j] =(radius+interval*rfactor/2)*K/rfactor;
Cmm[i][j] =(radius-interval*rfactor/2)*K/rfactor;

}

Ckp[i][j] =(radius)*K*rfactor;
```

```
Ckm[i][j] =(radius)*K*rfactor;
Q[i][j] =0;
}

}

double r1;
double r2;
double powerden = 0;
for(i =0; i<aprad/interval/rfactor ; i++){  // power rad 10 mw
j = .0003/interval;
powerden = .001/pi/aprad/aprad/phi;
r1 = (i)*interval*rfactor;

r2 = (i+1)*interval*rfactor;
Q[i][j]=pi*(r2*r2-r1*r1)*powerden;
if(i+1>aprad/interval/rfactor){
Q[i][j]=Q[i][j]+pi*(aprad*aprad-r2*r2)*powerden;
}

}

for(i = 0; i<num ; i++){

Ckp[i][0]= 0;

}
double holder;
// for(i = 0; i<40 ; i++){
// for(j= 12;j<13;j++){
```

```
// metal = 3.18;
// radius= (i+1/2)*interval;
// Rmp[i][j] =1/(radius+interval/2)/metal;
// Rmm[i][j] =1/(radius-interval/2)/metal;
// Rkp[i][j] =1/(radius)/metal;
// Rkm[i][j] =1/(radius)/metal;
// }
// }

for(i =pillrad/interval/rfactor; i<num-1 ; i++){  // mesa


for(j= 0;j<pillhi/interval;j++){
Cmp[i][j]= 0;
Cmm[i][j]= 0;
Cmp[i-1][j]= 0;
Cmm[i+1][j]=0;
Ckp[i][j]= 0;
Ckm[i][j]=0;
Ckp[i][j+1]= 0;
Ckm[i][j-1]= 0;

}
}
for(i =0; i<=pillrad/interval/rfactor+1 ; i++){ // pill thermal

for(j= 0;j<pillhi/interval;j++){
Cmp[i][j]=Cmp[i][j]* Kg/K;
Cmm[i][j]=Cmm[i][j]* Kg/K;
```

```
//Ckp[i][j]=Ckp[i][j]* Kg/Ks;
Ckm[i][j]=Ckm[i][j]*Kg/K;


if (i!=0){
//Cmp[i-1][j]= Kg;
}
else{
Cmm[i][j]=0;
}
if (j!=0){
//Ckm[i][j-1]= Kg;
}
else{
Ckp[i][j]=0;
}
// Cmm[i+1][j]=Cmm[i+1][j]*Kg/Ks;
Ckp[i][j+1]= Ckp[i][j+1]*Kg/K;



}



}
printf("yep, %d \n",j);
holder = j;//getting next line
for(i =0; i<num ; i++){ // interface thermal

 for(j= holder; j<pillhi/interval+intthick/interval;j++){

Cmp[i][j]=Cmp[i][j]* Kox/K;
```

```
Cmm[i][j]=Cmm[i][j]* Kox/K;

//Ckp[i][j]=Ckp[i][j]* Kg/Ks;
Ckm[i][j]=Ckm[i][j]*Kox/K;

if (i==0){
Cmm[i][j]=0;
}



Ckp[i][j+1]= Ckp[i][j+1]*Kox/K;

if(i==0){
printf("yep, %d  %e \n",j,Ckp[i][j+1]);
 }

}


}

for(i =pillrad/interval/rfactor; i<num-1 ; i++){  // mesa


for(j= 0;j<pillhi/interval;j++){
Cmp[i][j]= 0;
Cmm[i][j]= 0;
Cmp[i-1][j]= 0;
Cmm[i+1][j]=0;
```

```
Ckp[i][j]= 0;
Ckm[i][j]=0;
Ckp[i][j+1]= 0;
Ckm[i][j-1]= 0;

}
}
powerden =0;// 100 ; /// watt / cm^2  max 100
double area = 0;
for(i = 0; i<num-1 ; i++){  // surounding power sources
//for(j= 19;j<20;j++){

j = pillhi/interval+1;
//if (i==0){
// area =  (((i+.5)*interval*rfactor)*((i+.5)*interval
*rfactor)*pi)-(((i)*interval*rfactor)*((i)*interval*rfactor)*pi);
// area = 0;
//}
//if (i==num-2){
// area =  (((i)*interval*rfactor)*((i)*interval*rfactor)
*pi)-(((i-.5)*interval*rfactor)*((i-.5)*interval*rfactor)*pi);

//}
//else{
area =  (((i+1)*interval*rfactor)*((i+1)*interval*rfactor)
*pi)-(((i)*interval*rfactor)*((i)*interval*rfactor)*pi);
//}
Q[i][j]= powerden*area/phi;

}
```

```
double esink = 0;
double esink2 = 0;
double eright = 0;

double energy = 0;
double errormax=0;
for (i=0; i < num; i++){// energy inputted into sytstem
for (j=0; j < numj; j++){
energy = energy+ Q[i][j];
}
}
energy = energy*2*3.1415927;

int k;
int iter=20800;//2****************
double endint;
double endrad;
double a;
double b;
double c;
double d;
for (k = 0; k<iter; k++){

j=0;// top
i=0;
Tnew[0][0] =(Q[0][j] + T[i+1][j]*Cmp[i][j]+
  T[i][j+1]*Ckm[i][j])/(Cmp[i][j]+Ckm[i][j]);
for (i = 1; i<num-1 ; i++){
```

```
if (Cmp[i][j]== 0&&Cmm[i][j]==0&&Ckp[i][j]==0&&Ckm[i][j]==0){
Tnew[i][j] =T[i][numj-1];
}
else if(i == num-2){
Tnew[i][j] =(Q[i][j] + T[i-1][j]*Cmm[i][j]+
 T[i][j+1]*Ckm[i][j])/(Cmm[i][j]+Ckm[i][j]);


}
else{
Tnew[i][j] =(Q[i][j] + T[i+1][j]*Cmp[i][j]
+ T[i-1][j]*Cmm[i][j]+  T[i][j+1]*Ckm[i][j])
/(Cmm[i][j]+Cmp[i][j]+Ckm[i][j]);
}
}

for (i = 1; i<num-1 ; i++){
for( j=1; j<numj-1 ; j++){

if (Cmp[i][j]== 0&&Cmm[i][j]==0&&Ckp[i][j]
==0&&Ckm[i][j]==0){
Tnew[i][j] =T[i][numj-1];
}
else{


Tnew[i][j] =(Q[i][j] + T[i+1][j]*Cmp[i][j]
+ T[i-1][j]*Cmm[i][j]+ T[i][j-1]*Ckp[i][j]+
 T[i][j+1]*Ckm[i][j])/(Cmm[i][j]+Cmp[i][j]+
 Ckp[i][j]+Ckm[i][j]);
}
}
```

```
}


for( j=1; j<numj-1 ; j++){//inside
i = 0;
if (Cmp[i][j]== 0&&Cmm[i][j]==0&&Ckp[i][j]
==0&&Ckm[i][j]==0){
Tnew[i][j] =T[i][numj-1];
}
else{//Tnew[i][j] =(Q[i][j] + T[i+1][j]/Rmp[i][j]
+ T[i][j-1]/Rkp[i][j]+ T[i][j+1]/Rkm[i][j])/(
1/Rmp[i][j]+1/Rkp[i][j]+1/Rkm[i][j]);
Tnew[i][j] =(Q[i][j] + T[i+1][j]*Cmp[i][j]+
T[i][j-1]*Ckp[i][j]+ T[i][j+1]*Ckm[i][j])
/(Cmp[i][j]+Ckp[i][j]+Ckm[i][j]);
}

}


for( j=1; j<numj-1 ; j++){   // infinity edge
i = num-2;
if (Cmp[i][j]== 0&&Cmm[i][j]==0&&Ckp[i][j]==0&&Ckm[i][j]==0){
Tnew[i][j] =T[i][numj-1];
}
else{//cooler??  up down conduct??

//Tnew[i][j] =(Q[i][j] + T[i-1][j]*Cmp[i][j]
+ T[i-1][j]*Cmm[i][j]+ T[i][j-1]*Ckp[i][j]+
 T[i][j+1]*Ckm[i][j])/(Cmm[i][j]+Cmp[i][j]
```

```
+Ckp[i][j]+Ckm[i][j]);
//Tnew[i][j] =(Q[i][j] + (-T[i-1][j]+2*T[i][j])
*Cmp[i][j]+ T[i-1][j]*Cmm[i][j]+ T[i][j-1]*Ckp[i][j]+
 T[i][j+1]*Ckm[i][j])/(Cmm[i][j]+Cmp[i][j]+Ckp[i][j]
 +Ckm[i][j]);
Tnew[i][j] =(Q[i][j] + T[i-1][j]*Cmm[i][j]+ T[i][j-1]
*Ckp[i][j]+ T[i][j+1]*Ckm[i][j])/(Cmm[i][j]+Ckp[i][j]
+Ckm[i][j]);

}

}




error=0;
errormax = 0;
//printf("%e, %e\n",error, T[1][1]);

for (i = 0; i<num-1 ; i++){

for( j=0; j<numj-1 ; j++){
if(abs(T [i][j]- Tnew[i][j])>errormax){
errormax = abs(T [i][j]- Tnew[i][j]);
}
error =error+abs(T [i][j]- Tnew[i][j]);
T [i][j]= Tnew[i][j];
}

}
```

```
esink = 0;
esink2 = 0;
eright = 0;
  for (i=0; i<num; ++i){// energy to sink
r1 = (i)*interval*rfactor;
r2 = (i+1)*interval*rfactor;
if(r1<0){
r1=0;
}
j=pillhi/interval+1;
esink = esink+ (T[i][numj-4]-T[i][numj-3])
*K/interval*3.1415927*(r2*r2-r1*r1);
esink2 = esink2+ (T[i][j]-T[i][j+1])*Kox/interval
*3.1415927*(r2*r2-r1*r1);
//printf(" \n %e, %e ",esink,T[numi*numj-10*numi+i] );
}
  for (j=0; j<numj;j++){
r1 = (num-3.5+.5)*interval*rfactor;
//if (j<numj-40){
eright = eright+ (T[num-4][j]-T[num-3][j])*K*interval
*2*3.1415927*r1/interval/rfactor;
//}
//else{
// eright = eright+ (T[num-3][j]-T[num -
 4][j])*K*interval*2*3.1415927*r1/interval/rfactor;


//}
  }


  if( (iter-k)%100 == 0){
```

```
error = error/num/numj;

printf("%e,%e,%e,%e,%e,%d \n",error,
T[0][40], T[0][5],esink2/energy, esink/energy,iter-k);
if ((error >.00000001)||(iter-k)%10000==0){
holder = 0;
a= num-1;
for (i = 0; i<num-1 ; i++){
holder = holder +(T[i][numj-3]-T[i][numj-2]);
}

holder= holder /a;
iexpan = pillhi/interval;
holder = (subthick-(numj-iexpan-2)*interval)
/interval*holder;
for (i = 0; i<num-1 ; i++){
for( j=0; j<numj-1 ; j++){

T [i][j]=T [i][j]+holder-T [num-5][numj-1];



}


}
for (i = 0; i<num-1 ; i++){
j=numj-1;
T [i][j]=holder;
}
}
}
```

```
  if( (k ==5000||k ==6000 ||k ==7000||k ==8000||k ==9000||
  k ==10000||k ==150000||k ==200000||k ==250000||
  k ==300000||k ==350000)){

holder = 0;
holder2 = 0;
a= num-1;
for (i = 0; i<num-1 ; i++){
j=pillhi/interval;
holder = holder +T[i][numj-3]-T[i][numj-2];
holder2 = holder2 +T[i][j+1]-T[i][j+2];
}

holder= holder /a;
holder2= holder2 /a;
holder = holder/ esink*energy;//
holder2 = holder2/ esink2*energy;//
//a = numj;
//base = (subthick-simthick)/interval*holder;
for (i = 0; i<num-1 ; i++){
//for( j=pillhi/interval+1+intthick/interval; j<numj ; j++){
for( j=pillhi/interval+1+intthick/interval; j<numj ; j++){


T[i][j]=(subthick-(numj-iexpan-2)*interval)
/interval*holder+holder*(numj-1-j);



}
```

```
}
for (i = 0; i<num-1 ; i++){
for( j=pillhi/interval+1+intthick/interval;
 j>pillhi/interval+1 ; j--){
// T [i][j]=T [i][j+1]+holder2;

}
}

}
}

for (j = 0; j<numj ; j++){

for( i=0; i<num ; i++){

file << T[i][j]<<" ";
}
file << endl;
}

file <<"hello "<< error<<" "<< endl;

    file.close() ;

 file.open("x.dat");

 for (j = 0; j<num ; j++){
file << j*interval*rfactor << endl;
//file << Ckp[3][j] << endl;
```

```
 }
 file.close() ;

 file.open("y.dat");

 for (j = 0; j<numj ; j++){
file <<j*interval<<endl;
 }
 file.close() ;

esink = 0;
        for (i=0; i<num; ++i){// energy to sink
r1 = (i)*interval*rfactor;
r2 = (i+1)*interval*rfactor;

esink = esink+ (T[i][numj-5]-
T[i][numj-4])*K/zfactor/interval*3.1415927*(r2*r2-r1*r1);
//printf(" \n %e, %e ",esink,T[numi*numj-10*numi+i] );
}
printf("%e, %e,  %e,%e, %e,%e interval , radint %e,
 iexpan %d\n",error, energy, esink,T[2][100], T[3][0],interval*10000,
  interval*rfactor*10000,iexpan);
return 0;
}
```

Appendix B

Recipes

Table B.1: NR7 3000, 3 micron negative resist

krpm	spin time	prebake (^oC/min)	postbake (^oC/min)	expos (aligner/sec)	dev(sec)
2.5	45 sec	150/ 3 (hotplate)	100/ 3 (hotplate)	HiRes/45	20 +

Table B.2: NR7 1000, 1 micron negative resist

krpm	spin time	prebake (^oC/min)	postbake (^oC/min)	expos (aligner/sec)	dev(sec)
2.5	45 sec	150/ 3 (hotplate)	100/ 3 (hotplate)	HiRes/30	10 +

Table B.3: OCG, 1 micron positive resist

krpm	spin time	prebake (^oC/min)	postbake (^oC/min)	expos (aligner/sec)	dev(sec)
2.5	30 sec	90/ 30 (oven)	130/ 30 (oven)	HiRes/30	45 +

Table B.4: Thick resist, 5 micron positive resist

krpm	spin time	prebake (^oC/min)	postbake (^oC/min)	expos (aligner/sec)	dev(sec)
2.5	30 sec	90/ 60 (oven)	130/ 60 (oven)	lowRes/30	120 +

Table B.5: WaferBOND, 15 microns bonding agent

krpm	spin time(sec)	prebake (^oC/min)	bond pressure (PSI)	bond temp (^oC/min)
2.5	30 sec	130/ 3 (hotplate)	35	160/8

Table B.6: BCB cyclotene 3000 series, 1.5 microns BCB

ad-promoter (krpm/sec)	krpm	spin time (sec)	prebake (^oC/min)	Cure temp (^oC/min)
2/30	2.5	45 sec	130/ 2 (hotplate)	250/60

Table B.7: AlGaAs wet etch

etch rate	Sulfuric	30% Peroxide	DI	temp (^oC)
2000nm/min	2 ml	18 ml	20 ml	22

Table B.8: InGaP wet etch

etch rate	HCl	DI	temp (^oC)
200nm/min	10 ml	10 ml	22

Table B.9: Silicon wet etch

etch rate	KOH	DI	temp (^oC)
2000nm/min	10 grams	40 ml	80

Table B.10: SiO_2 BOE wet etch

etch rate	Buffered Oxide etch	temp (^oC)
200nm/min	20ml	22

Table B.11: PECVD oxide

etch rate	power (watts)	presure (mt)	N_2O(sccms)	SiH_4(sccms)	temp (^oC)
33nm/min	20	600	500	155	250

Table B.12: PECVD nitride

etch rate	power (watts)	presure (mt)	N_2(sccms)	SiH_4(sccms)	temp (^oC)
33nm/min	20	600	500	155	250

Table B.13: Si dioxide etch

etch rate	power (watts)	presure (mt)	SF_6(sccms)
20nm/min	175	20	25

Table B.14: Silicon etch (fast with undercut)

etch rate	power (watts)	presure (mt)	SF_6(sccms)
1000nm/min	175	20	25

Table B.15: Silicon etch (minimal undercut)

etch rate	power (watts)	presure (mt)	SF_6(sccms)
800nm/min	175	13	25

Table B.16: BCB, minimal undercut

etch rate	power (watts)	presure (mt)	SF_6(sccms)	O_2(sccms)
100nm/min	150	40	15	70

Table B.17: Silicon dioxide etch

etch rate	power (watts)	presure (mt)	HC23(sccms)
17nm/min	250	25	30

Table B.18: GaAs etch (inconsitant, use for small etch depths)

etch rate	power (watts)	presure (mt)	BCl_3(sccms)
variable	250	20	25

Table B.19: photo etch

etch rate	power (watts)	presure (mt)	O_2(sccms)
33nm/min	200	50	90

Appendix C

Single-tier VCSEL Process Flow

step	description	parameters	time
	Dye saw wafer		
1	spin 1 micron resist on front of wafer	2K RPM spin	30 sec
2	bake resist	90 C	30 minute
3	dye saw tape back of wafer		
4	cut 3X3 whole pieces	12X12 mm si blade	
5	carfully remove from tape		
6	solvet clean, remove photo	ace, meth, IPA	
7	box pieces		

Step	Equipment / Condition	Time
mesa mask		
6 deposit 1 micron PECVD oxide	PECVD recipe	30 min
7 spin 3 micron NR7 (neg)	3.5 K rpm spin	45 sec
8 bake	150 C hotplate	2.5 min
9 expose high res. Aligner	long filter	45 sec
10 bake	100 C hot plate	2.5 minute
11 develope until clear	RD6	~ 45 sec
12 etch 1 micron oxide BOE		5 minutes
13 remove photo	microstrip (70C if needed)	5 minutes
mesa etch		
14 mix sulfuric etch		
15 2 ml Sul, 18 ml perox 60%,25 ml DI	let sit	5 min
16 etch		
count mirrors in solution	p-type & ntype	~2sec
17 etch .8 micron oxide RIE	RIE recipe	25 min
18 etch .2 micron oxide BOE		2 min
aperture oxidation		
19 BOE dip	optional	10 sec
20 oxidize	chamber 450C	70 min
need a characterization step	dry insert	
metalization liftoff p-type		
21 spin 3 micron NR7 (neg)	2.5 K rpm spin	45 sec
22 bake	150 C hotplate	2.5 min
23 expose high res. Aligner	long filter	45 sec
24 bake	100 C hot plate	2.5 minute
25 develope until clear	RD6	~ 45 sec
26 clean open surface	oxygen plasma	15-30 min
27 BOE		10 sec
28 deposition		
metals		
29 liftoff until clear	microstrip 70C	10-20 min
substrate removal		
30 spin on WaferBOND	2.5 krpm	30 sec
31 bake	130 C	2 min
32 Bond Si dummy	33 PSI, 160 C	8 min
33 remove waferBOND residue and bead	Waferbond remover dip	30 sec
34 etch GaAs substrate	Sulfuric solution	3 hours
35 etch InGaP substrate	HCl solution	5 min
backside metalization liftoff n-type		
36 spin 3 micron NR7 (neg)	2.5 K rpm spin	45 sec
37 bake	100 C hotplate	5 min
38 expose high res. Aligner	long filter	45 sec
39 bake	100 C hot plate	2.5 minute
40 develope until clear	RD6	~ 45 sec
41 clean open surface	oxygen plasma	15-30 min
42 BOE		10 sec
43 deposition of metals		
44 liftoff until clear	microstrip 70C	10-20 min
VCSEL pill release		
45 spray with WaferBOND remover into vial	waferBond remover	30 sec
46 decant pills {heated remover}	waferBond remover wait	1 hour
47 decant pills {IPA}	IPA wait	1 hour
48 decant pills {IPA}	IPA wait	1 hour

Appendix D

Cantilever Process Flow

step	description	parameters	time
	Dye saw SOI wafer		
1	spin 1 micron resist on front of v	2K RPM spin	30 sec
2	bake resist	90 C	30 minute
3	dye saw tape back of wafer		
4	cut 3X3 whole pieces	12X12 mm si blade	
5	carfully remove from tape		
6	solvet clean, remove photo	ace, meth, IPA	
7	box pieces		

metal head deposition		
8 spin 3 micron NR7 (neg)	2.5 K rpm spin	45 sec
9 bake	150 C hotplate	2.5 min
10 expose high res. Aligner	long filter	45 sec
11 bake	100 C hot plate	2.5 minute
12 develope until clear	RD6	~ 45 sec
13 clean open surface	oxygen plasma	15-30 min
14 BOE		10 sec
15 deposition metals		
16 liftoff until clear	microstrip 70C	10-20 min
Silicon window etch		
17 coat & bond with black wax	bond front to glass slide dumby	
18 pattern window	place glass slide mask covering	
19 RIE backside silicon	RIE silicon fast etch	30 min
20 nitrogen clean window	blow with nitro gun	10 sec
repeat RIE & clean 20 X		10 + hours
oxide removal		
21 BOE etch	etch 1 micron of oxide	8 min
Cantilever pattern		
22 bond back to glass slide	cover window with glass slide	
23 attach to spinner chuck		
24 spin 1 micron NR7 (neg)	3.5 K rpm spin	45 sec
25 bake	150 C hotplate	2.5 min
26 expose high res. Aligner	long filter	30 sec
27 bake	100 C hot plate	2.5 minute
28 develope until clear	RD6	~ 15 sec
29 remove from glass slide	hot plat removal, 150 C	30 sec
30 RIE silicon	RIE low pressure Si etch	5 min
31 oxygen plasma resist	remove 1 micron resist	30 min

Bibliography

[1] Mindy Teo. Development of pick and place assembly techniques for monolithic optopill integration. Master's thesis, Massachusetts Institute of Technology, 2005.

[2] J. Smith. High density, low parasitic direct integration by fluidic self-assembly. *IEDM Technical Digest*, 10(13):201–204, December 2000.

[3] Clifton G. Fonstad. Magnetically assisted statistical assembly - a new heterogeneous integration technique. Singapore-MIT Alliance Symposium, January 2002.

[4] J.A. Kash, F.Doany, D. Kuchta, and et. al. Terabus: a chip-to-chip parallel optical interconnect. *LEOS 2005*, pages 363–364, December 2005.

[5] Brian R. Koch, Alexander W. Fang, Oded Cohen, and John E. Bowers. Mode-locked silicon evanescent lasers. *Optics Express*, 15(18):11225, September 2007.

[6] T. Simpkins. *Design, Modeling, and Simulation of a Compact Optoelectronic Neural Coprocessor.* PhD thesis, Massachusetts Institute of Technology, 2005.

[7] John C.C. Fan, Julia M. Phillips, and Bor-Yeu Tsaur. Heteroepitaxy on silicon ii. Number 91. Material Reseach Society, 1998.

[8] Lecture notes 6.772 Lecture 25 5/03 http://ocw.mit.edu/OcwWeb/Electrical-Engineering-and-Computer-Science/6-772Spring2003/LectureNotes/index.htm.

[9] A. V. Krishnamoorthy, K. W. Goossen, and et.al. 16x16 vcsel array flip-chip bonded to cmos vlsi circuit. *IEEE Photonics Letts.*, 12(8):1073–1075, 2000.

[10] Joanna M. London, Andrew H. Loomis, Joseph F. Ahadian, and Clifton G. Fonstad Jr. Preparation of silicon on gallium arsenide wafers for monolithic optoelectronic integration. *IEEE Photonics Technology Letters*, 11(8):958–960, August 1999.

[11] Edward Barkley. Wafer bonding of processed si cmos vlsi and gaas for mixed technology integration. Master's thesis, Massachusetts Institute of Technology, 2002.

[12] Wojciech Giziewicz. Optoelectronic integration using aligned metal-to-semiconductor bonding. Master's thesis, Massachusetts Institute of Technology, 2000.

[13] Alex Katsnelson, Vadim Tokranov, Michael Yakimov, and Serge Oktyabrsky. Integration of iii-v optoelectronic components on si platform. *Mat. Res. Soc. Symp. Proc.*, page B7.4.1, 2004.

[14] S. Daryanani, H. Fathollahnejad, D.L. Mathine., R. Droopad, A. Kubes, and G.N. Maracas. Integration of a single vertical-cavity surface emitting laser onto a cmos inverter chip. *Electronic Letters.*, 31(10):833, May 1995.

[15] J.K. Tu, J.J. Talghader, M.A. Hadley, and J.S. Smith. Fluidic self-assembly of ingaas vertical cavity surface emitting lasers onto silicon. *Electronic Letters*, 31(17):1448, August 1995.

[16] His jen Yeh and J Smith. Fluidic self-assembly for the integration of gaas light-emitting diodes on si substrates. *IEEE Photonics Letters*, 6(6):706–708, June 1994.

[17] Joseph J. Talghader, Jay K. Tuand, and J. Smith. Integration of fluidically self-assembled optoelectronic devices using a silicon-based process. *IEEE photonics technology letters*, 7(11):1321–1323, November 1995.

[18] C.F. Edman, R.B. Swint, and et al. Electric field directed assembly of ingaas led onto silicon circuitry. *IEEE Photonics Technology Letters*, 12(9):1198–1200, September 2000.

[19] U. Srinivasa, D. Liepmann, and R.T. Howe. Microstructure to substrate self-assembly using capillary forces. *Journal of Micromechanical Systems*, 10(1):17–24, 2001.

[20] Clifton G. Fonstad. Magnetically assisted statistical assembly - a universal heterogeneous integration technique. March 2001.

[21] Joseph Rumpler. Optoelectronic integration using the magnetically assisted statistical assembly technique : initial magnetic characterization and process development. Master's thesis, Massachusetts Institute of Technology, 2002.

[22] Stephen D. Senturia. *Microsystem Design.* Kluwer Academic Publishers, 2001.

[23] Futurrex Inc., 12 Cork Hill Road, Franklin, NJ 07416, USA, Phone: 973-209-1563 http://www.futurrex.com/.

[24] samarium cobalt film obtained from Professor F. Cadieu, Department of Physics of Queens College of the City University of New York.

[25] Brewer Science Inc., 2401 Brewer Drive, Rolla, MO 65401 USA Phone: +1.573-364-0300 http://www.brewerscience.com/.

[26] Landmark Optoelectronics Corporation^{tm}, Taiwan, http://www.lmoc.com.tw/.

[27] Kent D. Choquette, Kent M. Geib, and et. al. Advances in selective wet oxidation of algaas alloys. *IEEE Journal of Selected Topics In Quantum Electronics*, 3(2):916–927, June 1997.

[28] W. T. Tsang. Self-terminating thermal oxidation of alas epilayers grown on gaas by molecular beam epitaxy. *Applied Physics Letters*, 33:426429, 1978.

[29] R. S. Burton and T. E. Schlesinger. Wet thermal oxidation of $al_xga_{1-x}as$ compounds. *Journal of Applied Physics*, 76:5503–5507, 1994.

[30] H. Nickel. A detailed experimental study of the wet oxidation kinetics of $al_xga_{1-x}as$ layers. *Journal of Applied Physics*, 78:52015203, 1995.

[31] James M. Perkins. Magnetically assisted statistical assembly of iii-v heterostructures on silicon: Initial process and technology development. Master's thesis, Massachusetts Institute of Technology, 2002.

[32] private communication with Joe Rumpler on pill release techniques.

[33] N. M. Jokerst and et. al. Thin-film multimaterial optoelectronic integrated circuits. *IEEE Transactions on Computation, Packaging, Manufacturing Technology B*, 19(1):97–106, February 1996.

[34] *Eurotherm Controller/Programmer operating Instructions.*

[35] Alfa Aesar, 26 Parkridge Road, Ward Hill, MA 01835 USA Telephone: 1-978-521-6300 http://www.alfa.com/.

[36] Goran S. Matijasevic, Chin Lee, and et. al. Au-sn alloy phase diagram and properties related to its use as a bonding medium. *Thin Solid Films*, 223:276–287, September 1993.

[37] Dow Chemical Company, Midland, Michigan USA http://www.dow.com/cyclotene/index.htm.

[38] Edmond Optics, 101 East Gloucester Pike, Barrington, NJ/USA 08007 Telephone: (800) 363-1992 http://www.edmundoptics.com/US/.

[39] T.E Sale. *Vertical Cavity Surface Emitting LASERS.* John Wiley & Sons, 1995.

[40] J.P. Holman. *Heat Transfer, 8th edition.* McGraw Hill, 1997.

[41] MEMS exchange website, material properties http://www.memsnet.org/material/silicondioxidesio2film/.

[42] Ocean Optics, 830 Douglas Ave. Dunedin, FL 34698 USA 727.733.2447 http://www.oceanoptics.com/.

[43] J.S. Blakemore. Semiconducting and other major properties of gallium arsenide. *Journal of Applied Physics*, 53(10):R123–R181, 1992.

[44] Microsystems Technology Laboratory, Massachusetts Institute of Technology, 77 Massachusetts Avenue Building 39, Room 321 , Cambridge, MA 02139 USA http://mtlweb.mit.edu/index.html.

[45] The MOSIS Service,4676 Admiralty Way, Marina del Rey, California 90292-6695 USA http://www.mosis.com/.