Dynamics of the Kink Effect in InAlAs/InGaAs/InP HEMTs

by

Alexander N. Ernst

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Abstract

InAlAs/InGaAs/InP High Electron Mobility Transistors (HEMTs) show significant promise for low-noise and high-power millimeter-wave applications (60 GHz and above). Unfortunately, these HEMTs show a detrimental behavior in their output characteristics, the *kink effect*. The kink is a sudden rise in drain current at a certain drain-to-source voltage that results in high drain conductance and transconductance compression, leading to reduced voltage gain and poor linearity.

In this study we report the first experimental pulsed measurements of the dynamics of the kink effect in InAlAs/InGaAs/InP with nanosecond resolution. Our measurements show that the kink turns on first the higher V_{DS} is. The rate at which the kink builds-up is seen to increase with both V_{DS} and V_{GS} . In general, the kink's characteristic time constant strongly depends on both V_{DS} and V_{GS} : for small values of V_{DG} , it decreases exponentially with V_{DG} ; on the other hand, for large values of V_{DG} , it becomes independent of V_{DG} . Values between 50 ns and 100 μ s have been measured in a single device. This suggests that, from a small signal point of view, the kink should not be visible in the millimeter-wave range.

Our research also shows that the kink is related to impact ionization that takes place in the high-field region at the drain end of the channel. We have found that the rate at which the kink builds-up in its early stages follows a classical $1/(V_{DS}-V_{DS,SAT})$ dependence characteristic of impact ionization. Our data should be instrumental in formulating a hypothesis and building a model for the physical origin of the kink.

Thesis Supervisor: Jesús A. del Alamo Title: Associate Professor

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Contents

1	Introduction					
2	The	Theoretical Background				
	2.1	Introd	uction	14		
	2.2	Trap I	Related Theories	14		
		2.2.1	Traps in the Buffer	14		
		2.2.2	Traps in the Insulator	19		
		2.2.3	Comments on Trap Related Theories	21		
	2.3	Pure I	mpact Ionization	21		
	2.4	SOI M	Iodel	22		
	2.5	Source	Resistance Reduction due to Excess Drain Current	23		
	2.6	Barrie	r-Induced Hole Pile-up Theory	24		
	2.7	Expec	ted Transient Behavior	27		
		2.7.1	Constant Lifetime	28		
		2.7.2	Concentration Dependent Lifetime	28		
		2.7.3	Hole Concentration Reaching a Plateau	28		
	2.8	Summ	ary	30		
3	Experimental					
	3.1	Introd	uction	31		
	3.2	3.2 Experimental Details		31		
		3.2.1	Pulsed I-V Setup	31		
		3.2.2	Device Structure	35		
	3.3	Result	S	36		
		3.3.1	Pulsed I-V Curves	36		

		3.3.2	Kink Build-up	38	
		3.3.3	Kink Rise Time: $T_{90\%}$	42	
	3.4	Summ	ary	44	
4	Disc	cussion	1	45	
	4.1	Introd	uction	45	
	4.2	Obser	vations on V_{kink}	46	
		4.2.1	Dynamics of V_{kink}	46	
		4.2.2	Saturation of V_{kink}	47	
		4.2.3	Universal Behavior of $T_{90\%}$	49	
	4.3	3 Comparison of Theory and Experimental Results			
		4.3.1	Impact Ionization	51	
		4.3.2	Trap Related Theories	55	
		4.3.3	SOI Like Mechanism	57	
		4.3.4	Barrier-Induced Hole Pile-up Model	58	
	4.4	Summary			
5	Con	nclusions and Suggestions			
A	Mat	themat	cical Derivations	63	
	A.1	1 Computation of ΔV_T^{kink}		63	
		A.1.1	Traps in the Buffer	63	
		A.1.2	Traps in the Insulator	65	
		A.1.3	SOI Like Mechanism	65	
	A.2	Turn-o	on Dynamics of the Holes	66	
	A.3	Impac	t Ionization Generation Function	67	

List of Figures

1-1	Schematic cross-section of a HEMT with dopants in both the insulator and	
	the buffer. The source and drain are contacted to the channel by means of	
	allowed ohmic contacts. The cap reduces the resistance between the gate and	
	the source and drain contacts	11
1-2	(a) Typical kink in output characteristics of a HEMT and (b) resulting	
	transconductance compression (g_m) and sudden rise in output conductance	
	(g_d) when moving along the load line (Courtesy of M. H. Somerville)	12
2-1	Kink mechanism when negatively charged electron traps are present in the	
	buffer. a) At low V_{DS} , the traps remain charged and no kink occurs. b)	
	At $V_{DS} \simeq V_{DS,kink}$, some electrons are released from the traps causing a	
	threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are empty and so the	
	kink saturates.	15
2-2	Kink mechanism when neutrally charged electron traps are present in the	
	buffer. a) At low V_{DS} , some electrons are captured by the traps. b) At $V_{DS} \simeq$	
	$V_{DS,kink}$, some electrons are released from the traps causing a threshold shift.	
	c) For $V_{DS} \ge V_{DS,kink}$, all the traps are empty and so the kink saturates.	16
2-3	Kink mechanism when neutrally charged hole traps are present in the buffer.	
	a) At low V_{DS} , the traps are in equilibrium and no kink occurs. b) At	
	$V_{DS} \simeq V_{DS,kink}$, some holes are trapped in the buffer leading to a small	
	threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are filled and so the kink	
	saturates.	18

- 2-4 Kink mechanism when neutrally charged hole traps are present in the insulator. a) At low V_{DS} , the traps are in equilibrium and no kink occurs. b) At $V_{DS} \simeq V_{DS,kink}$, some holes are trapped in the insulator leading to a small threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are filled and so the kink saturates.
- 2-5 SOI like mechanism. a) At low V_{DS} , no impact ionization occurs and there is no kink. b) At $V_{DS} \simeq V_{DS,kink}$, impact ionization begins and the buffersource junction begins to get forward biased. c) For $V_{DS} \ge V_{DS,kink}$, significant impact ionization occurs but the kink seems to saturate due to the logarithmic relation between the hole concentration and the threshold shift.

20

23

27

29

- 2-8 Simulated hole turn-on transient as a function of time for a single characteristic time constant. The different curves correspond to increasing values of the generation rate.
- 2-9 Simulated hole turn-on transient as a function of time in the case where the characteristic time constant depends on the hole concentration p(t), where we assumed $\tau = \tau_o/(1 + p(t))$, τ_o being constant.
- 2-10 Simulated hole turn-on transient as a function of time for the case when the traps or the well become(s) full (solid lines). This is, the kink saturates for sufficiently large generation rate. The dashed lines correspond to the single characteristic time constant case with no well/traps saturation.
 29

Ideal pulsed I-V measurement: the gate is pulsed from off-state ($V_{GS} \leq V_T$)	
to some on-state V_{GS} . The drain response to such a pulse is then measured	
after a delay that we denote T_d . Notice that the drain I-V characteristics are	
constrained to follow a load line path.	32
Schematic of the pulsed I-V setup used in this work. The system has nano-	
second resolution and is fully automated.	34
${\it Schematic\ cross-section\ of\ single\ InAlAs/InGaAs\ single-heterostructure\ HEMT}$	
used in this work. 1.2 and 2 μm gate length and 100 μm wide devices were	
characterized	35
Pulsed I-V set-up validation: pulsed I-V curves for $T_d \simeq 500 \ \mu s$ (crossed-lines)	
are compared with DC HP-4145B I-V curves (full lines). Good agreement is	
observed.	36
Pulsed I-V curves for varying delay times, T_d . No kink is seen below $T_d =$	
10 ns. For a given V_{GS} , the larger V_{DS} , the earlier the kink turns on and the	
faster it saturates.	37
Semilog plot of ΔI_D as a function of T_d for different values of V_{DS} but	
constant V_{GS} . a) $V_{GS} = -1.1$ V; b) $V_{GS} = -0.9$ V; c) $V_{GS} = -0.7$ V	40
Semilog plot of ΔI_D as a function of T_d for different values of V_{GS} and	
constant V_{DS} . a) $V_{DS} = 1.7 \text{ V}$; b) $V_{DS} = 2.1 \text{ V}$; c) $V_{DS} = 2.5 \text{ V}$	42
Semilog plot $T_{90\%}$, the time it takes for the kink to reach 90% of its final DC	
value, as a function of V_{DG} for different values of V_{GS} .	43
Measured transconductance, a_{m} , and resulting intrinsic transconductance.	
q_{m0} , as a function of V_{CS} ($V_{DS} = 2.5$ V) for the $L_c = 1.2$ µm device tested	
in this work, a_{m0} is obtained from a_{m} as: $a_{m0} = a_m/(1 - a_m R_s)$ where R_s	
$= 0.5 \Omega.\text{mm has been used.}$	47
V_{tight} as a function of T_{d} for increasing values of V_{CG} and constant V_{DG} a)	1,
$-1.3 \text{ V} \le V_{CS} \le -0.7 \text{ V}$ and $V_{DS} = 1.7 \text{ h}$ $-1.3 \text{ V} \le V_{CS} \le -0.7 \text{ V}$ and V_{DS}	
= 2.1, c) -1.3 V < Vag < -0.9 V and Vag = 2.5	49
Visit of as a function of $(V_{DS} - V_{DS} g_{AT})^{-1}$. For $V_{DS} - V_{DS} g_{AT})^{-1}$.	10
$(D_{0}, SAI) = (D_{0}, SAI) + (D_{$	
	Ideal pulsed I-V measurement: the gate is pulsed from off-state ($V_{GS} \leq V_T$) to some on-state V_{GS} . The drain response to such a pulse is then measured after a delay that we denote T_d . Notice that the drain I-V characteristics are constrained to follow a load line path

4-4	$T_{90\%}$ as a function of $V_{kink,DC}$ for all values of V_{GS} and V_{DS} in a semilog	
	scale. $T_{90\%}$ seems to depend only on the value of $V_{kink,DC}$, independent of	
	the $V_{GS} - V_{DS}$ bias	51
4-5	Early stages of V_{kink} build-up in a linear scale. Data (dots) and third order	
	polynomial fit (solid lines) for $V_{GS} = -0.9$ V. Similar results were obtained	
	for all values of V_{GS} except for V_{GS} = -1.3 V where the data is very noisy	53
4-6	Rising rate (R) of V_{kink} for the same values of V_{GS} and V_{DS} . R is obtained	
	from the derivative of the fitted polynomial to V_{kink} (fig. 4.5)	53
4-7	Semilog plot of $\kappa g/I_D$ as a function of $(V_{DS} - V_{DS,SAT})^{-1}$. A classical impact	
	ionization behavior is observed	54
A-1	Conduction band diagram at threshold for a single heterostructure with undoped buffer	
	and gate insulator	64
A-2	Conduction band diagram at threshold with net charge in the buffer. Positive net charge	
	has been assumed	65

Chapter 1

Introduction

Since the first demonstration of mobility enhancement in modulation-doped heterostructures in 1978 by Dingle and co-workers [1], there has been an explosion of research and development on High-Electron Mobility Transistors (HEMTs), also known as Modulation-Doped Field Effect Transistors (MODFETs). The main reason for this is that these device exhibit extremely high frequency response. World record current-gain cut-off frequencies (f_T) and f_{max} have been reported such as $f_T = 350$ GHz [2] and $f_{max} = 600$ GHz [3]. This figures place HEMTs as ideal candidates for low-noise and power applications in the millimeter-wave range (60 GHz and above).

A typical HEMT consists of a wide bandgap insulator such as AlGaAs or InAlAs, a narrow-gap channel such as GaAs or InGaAs, a widegap buffer, and a semi-insulating substrate, usually GaAs or InP as shown in fig. 1-1. Dopants are placed in the insulator and sometimes also in the buffer. Due to the energy band structure, electrons from these dopants are confined to the channel layer where they form a two-dimensional electron gas. Therefore, channel electrons are spatially separated from the ionized dopants and thus impurity scattering effects are minimized. This results in exceptional transport characteristics and consequently large f_T 's [4].

There are two major families of HEMTs: pseudomorphic HEMTs (pHEMTs) grown on GaAs substrates with InGaAs channels containing $\sim 20\%$ Indium composition and latticematched InAlAs/InGaAs HEMTs on InP (InGaAs channel with 53 % Indium composition). The transport characteristics of the latter are better due to the higher Indium content in the channel [5, 6]. Consequently major efforts have been made to develop a lattice-matched



Figure 1-1: Schematic cross-section of a HEMT with dopants in both the insulator and the buffer. The source and drain are contacted to the channel by means of allowed ohmic contacts. The cap reduces the resistance between the gate and the source and drain contacts.

InP HEMT technology¹.

However, the increased channel Indium composition also induced a couple detrimental effects: InP HEMTs suffer from low-breakdown voltage [7] and a significant anomaly in their output characteristics known as the kink-effect [8]. The kink effect is a sudden rise in drain current, I_D , at a certain drain-to-source voltage, V_{DS} , as shown in fig. 1-2 (a). In power applications where voltages swing from rail to rail, the kink results in a dramatic voltage gain drop, g_m/g_d , where g_m and g_d are respectively the device transconductance and output conductance. Circuit designers believe that this voltage gain drop distorts the transmitted signals. To see how the voltage gain drop may occur, we need to place ourselves along the load line in the $I_D - V_{DS}$ plane of fig. 1-2 (a) and move along it. As we can see, we eventually hit the region where the kink is very pronounced. In this region, g_m compresses drastically whereas g_d increases (fig. 1-2 (b)). This results in voltage gain drop and non-linear output

¹The reason for this is that only materials with a similar lattice constant can be grown on top of each other while still maintaining good crystal quality. Since the lattice constant of InGaAs increases with increasing Indium composition and the lattice constant of InP is higher than the one of GaAs (5.88 Å vs. 5.65 Å [4]), InP HEMTs have channels with higher Indium composition.



Figure 1-2: (a) Typical kink in output characteristics of a HEMT and (b) resulting transconductance compression (g_m) and sudden rise in output conductance (g_d) when moving along the load line (Courtesy of M. H. Somerville).

conductance.

The kink effect has also been observed in devices other than InP HEMTs, such as Siliconon-Insulator (SOI) transistors [9, 10], MESFETs [11], and pHEMTs [12]. The kink effect is fairly well understood in SOI [10] but little is known in heterostructures, and in particular in InP HEMTs. For example, the kink is know to be present at DC, but its high-frequency behavior (which is the one of interest in millimeter-wave applications) is still obscure. Consequently, the physical origin of the kink is an issue of considerable contention at this time. The conventional wisdom has attributed the kink effect to traps or their interaction with high-fields or impact ionization (II) [13]-[15]. Recently, simulations [12] as well as light emission, channel-engineering and body contact experiments [16]-[18] have suggested a link between impact ionization and the kink. Indeed, measurements showing direct correlation between II and the kink have been presented [19]. Several models involving II have been proposed including pure II [20], an SOI-like mechanism [18], hole trap charging [21], and *conductivity modulation* of the source [8, 22].

A new perspective on this problem can be obtained by studying the dynamics of the kink under pulsed operation. Besides providing insight about the origin of the kink, pulsed characterization has been proven to be a good predictor of large-signal high-frequency performance which is the relevant one for power applications [23]. In this work we have carried out the first experimental time-domain study of the kink effect in InAlAs/InGaAs HEMTs on InP with nanosecond resolution [24].

This thesis is organized as follows. We first discuss previously proposed theories for the kink effect in HEMTs in chapter 2. We begin with trap related theories, then we proceed with pure impact ionization, an SOI-like mechanism, source-resistance reduction, and finally a barrier-induced hole pile-up model. For each case, we discuss the validity of the model based on experimental results found in the literature. For the plausible theories, we examine the mechanism of the dynamics of the kink and list the expected key associated time constants. We also discuss three type of exponential turn-on transients that might govern the dynamics of the kink under pulsed operation.

We next present our pulsed I-V set-up and experimental results in chapter 3. We begin by providing a description of the set-up, how it works, and what its limitations are. Next, we validate the set-up by comparing pulsed I-V curves for long enough transients to static or DC I-V curves. Finally, we present experimental pulsed I-V transients with nanosecond resolution on InAlAs/InGaAs HEMTs at room temperature. We present the first reported results on the characteristic time constant of the kink effect for a wide range of operating biases, $V_{DS} - V_{GS}$. We also describe the general behavior of the kink dynamics for different values of V_{DS} and V_{GS} .

Finally, we discuss our experimental results in light of the possible mechanisms for the kink effect in chapter 4. Our key conclusions are that the early stages of the kink buildup correlate with impact ionization, that there is a saturation mechanism beyond which the magnitude of the kink can not increase any further, and that the characteristic time constant of the kink follows a universal behavior. That is, it only depends on the final value of the kink. We also find that the kink is not present within a few nanoseconds from the time that the transistor was excited, which suggest that the kink should not be prominent in millimeter-wave applications.

Chapter 2

Theoretical Background

2.1 Introduction

There have been a number of theories proposed that try to explain the physical origin of the kink. The conventional wisdom is that the kink arises from a combination of traps with high electric fields and/or impact ionization. Other theories invoked mechanisms such as pure impact ionization, an SOI like model, source resistance reduction, or hole pile-up in the extrinsic source. In this chapter, we will examine each one of these theories and discuss their validity. For the plausible theories, we will highlight the expected kink dynamics.

2.2 Trap Related Theories

Most theories incorporating traps suggest that high fields and/or impact ionization generated electrons/holes charge/discharge traps either in the buffer [13, 25] or in the insulator [21], leading to a shift in the threshold voltage. We summarize in this section the key mechanisms behind such theories.

2.2.1 Traps in the Buffer

2.2.1.1 Negatively Charged Traps

Brown *et al.* postulated that negatively charged traps in the buffer below the channel might cause the kink by the sudden release of trapped electrons at high electric fields [13]. Essentially, for sufficiently large drain to source voltage, V_{DS} , when the (horizontal) electric field is high, some of the trapped electrons in the buffer are released from the traps and



Figure 2-1: Kink mechanism when negatively charged electron traps are present in the buffer. a) At low V_{DS} , the traps remain charged and no kink occurs. b) At $V_{DS} \simeq V_{DS,kink}$, some electrons are released from the traps causing a threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are empty and so the kink saturates.

drift to the drain (fig. 2-1). As a result, the net charge in the buffer becomes more positive and the buffer potential increases. This induces a (negative) threshold shift which in turn results in increased drain current.

This theory is dubious in the InAlAs/InGaAs on InP system for the following reason: when the narrow bandgap InGaAs layer (channel) is replaced by a wider bandgap material, such as InGaAsP or InP, while keeping the same InAlAs as the buffer layer, the kink disappears [16, 26, 27]. If negatively charged traps in the buffer were responsible for the kink effect, then different channel materials should not play any role in the origin of the kink as long as electron transfer from buffer to channel is still favorable. In the above experiment, the conduction band discontinuity, ΔE_C , between buffer and channel is reduced from ~ 0.45 eV to ~ 0.3 eV when going from narrow to wider bandgap channel and so electron transfer from buffer to channel remains energetically favorable [4]. One could however argue that since the material growth process varies between the two different channel structures, then trap states might also be different. Nonetheless, as we will see later on, there has been



Figure 2-2: Kink mechanism when neutrally charged electron traps are present in the buffer. a) At low V_{DS} , some electrons are captured by the traps. b) At $V_{DS} \simeq V_{DS,kink}$, some electrons are released from the traps causing a threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are empty and so the kink saturates.

strong evidence showing that holes are involved in the formation of the kink, and so we do not discuss any further this theory.

2.2.1.2 Neutral Electron Traps

Another trap-buffer related mechanism was proposed by Zimmer *et al.* [14]. These authors postulated that the presence of neutral electron traps in the buffer might be the origin of the kink. They assumed that when a small V_{DS} is applied, some electrons from the channel are injected in the buffer where they are trapped (fig. 2-2). Consequently, the net charge in the buffer becomes negative. As V_{DS} is further increased, generation via impact ionization (II) takes place at the drain end of the device where the electric fields are high [16, 17, 18, 19, 28] and electron/hole pairs are generated. The II generated electrons drift to the drain whereas the holes are injected into the buffer where they recombine with the captured electrons. As a result, the net charge in the buffer becomes more positive and a negative threshold shift occurs, similarly to section 2.2.1.1. This theory is dubious for the following two reasons: first of all, electron injection from channel to buffer can only occur if the ΔE_C between channel and buffer is small and V_{DS} is high. This is unlikely to happen in InAlAs/InGaAs on InP HEMTs where ΔE_C is ~ 0.45 eV.

Second, as the traps begin to be filled with electrons (low V_{DS}), the net charge in the buffer becomes more negative and so the buffer potential drops. This results in a positive threshold shift, $\Delta V_{T,pre-kink}$. Notice that $\Delta V_{T,pre-kink}$ must be larger in magnitude than the threshold shift that creates the kink. As a result, some type of negative output conductance in the output characteristics of the device should be visible for $V_{DS} \leq V_{DS,kink}$, where $V_{DS,kink}$ is the value of V_{DS} at which the kink turns on. Such a negative output conductance is rarely seen in the literature. For these reasons, we do not proceed any further with this theory.

2.2.1.3 Hole Traps

Haruyama *et al.* suggested that hole traps in the buffer might be the cause of the kink [25]. They postulated that holes created by impact ionization can be injected in the buffer and be trapped by hole traps (fig. 2-3). This increases the buffer potential and consequently shifts the threshold (negatively) giving extra drive to the transistor.

Their experiments strongly support this idea: while measuring the output characteristics of a AlGaAs/InGaAs/GaAs HEMT, $I_D vs. V_{DS}$, they also monitored the buffer potential, V_{SB} [25]. It turns out that V_{SB} suddenly increases with V_{DS} for $V_{DS} \ge V_{DS,kink}$. This suggests a direct correlation between V_{SB} and the kink effect.

However, some of the results presented in Haruyama's work are questionable: measurements under light illumination show that V_{SB} increases sub-linearly with V_{DS} after the kink's onset [25]. However, a sub-linear change in V_{SB} must result in a similar (sub-linear) change in the threshold (see Appendix A.1). As a result, the kink current should also increase sub-linearly with V_{DS} , for $V_{DS} \ge V_{DS,kink}$ (eq. 2.1). This is not seen in their measurements. On the contrary, the kink is seen to saturate at high values of V_{DS} . A similar argument is obtained for measurement in the dark, except that V_{SB} increases exponentially with V_{DS} , for $V_{DS} \ge V_{DS,kink}$, but the kink still seems to saturate at high values of V_{DS} .

Another word of caution must be added to this discussion: Haruyama *et al.* used $Al_{0.2}Ga_{0.8}As$ for insulator, undoped $In_{0.2}Ga_{0.8}As$ for channel, $GaAs/Al_{0.2}Ga_{0.8}As/GaAs$



Figure 2-3: Kink mechanism when neutrally charged hole traps are present in the buffer. a) At low V_{DS} , the traps are in equilibrium and no kink occurs. b) At $V_{DS} \simeq V_{DS,kink}$, some holes are trapped in the buffer leading to a small threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are filled and so the kink saturates.

for buffer, and a GaAs semi-insulating substrate. As a result, the valence band discontinuity, ΔE_V , between channel and buffer is small ($\Delta E_V \sim 5\text{-}10 \text{ meV}$) and so hole injection from channel to buffer is very favorable. In our case, that is for lattice-matched InAlAs/InGaAs/InP, $\Delta E_V \simeq 0.3$ eV and so hole injection from channel to buffer is questionable.

In any case, hole accumulation in the buffer has not yet been proven nor refuted to be the origin of the kink, and so remains as a possible hypothesis. So, we will give an expression for the kink current, ΔI_D , and discuss the dynamics of this mechanism. Since the kink originates from a threshold shift, ΔI_D should be simply given by:

$$\Delta I_D \simeq g_{m0} |\Delta V_T^{kink}|, \qquad (2.1)$$

where ΔV_T^{kink} is the threshold shift induced by the trapping of holes in the buffer (see Appendix A.1.1 for derivation of ΔV_T^{kink}). As eq. 2.1 indicates, the threshold shift must be negative in order to create the kink.

In terms of the dynamics of such a mechanism, first of all, electrons must drift from source to drain in order to cause impact ionization. Next, II generated holes are injected into the buffer where they are captured. This increases the buffer potential and thus shifts the threshold. The key time dependencies in this mechanism are: electron transit time from source to drain, hole transport time in the channel and/or the buffer, and hole capture time.

To conclude this section, we list all the key assumptions made in this theory:

- impact ionization
- small ΔE_V between channel and buffer
- significant concentration of hole traps in the buffer
- hole capture in the buffer
- threshold shift

2.2.2 Traps in the Insulator

Hori *et al.* suggested that the presence of hole traps in the insulator might cause the kink [21]. The idea is the following: for $V_{DS} \ge V_{DS,kink}$, when II takes on, generated holes might be injected into the insulator where they are captured by the hole traps (fig. 2-4). As a result, the net charge in the insulator becomes more positive. This positive net charge change is imaged by a negative net charge change in the channel layer in order to maintain overall charge neutrality¹. That is, the electron concentration in the channel increases and thus results in increased drain current. This is equivalent to a threshold shift.

There are however two drawbacks in this theory. First of all, hole injection from channel into the insulator must occur. This is unlikely in lattice-matched InAlAs/InGaAs on InP HEMTs due to the significant valence band discontinuity between channel and insulator $(\Delta E_V \simeq 0.3 \text{ eV})$. Second, light irradiation experiments seem to indicate that the insulator does not play a major role in the formation of the kink [21]: Hori *et al.* irradiated an AlGaAs/InGaAs on GaAs HFET with three different wavelength lasers, two of them corresponding to the channel and insulator bandgap energy $(h\nu_{ch} \text{ and } h\nu_{ins} \text{ respectively})$,

¹Some charge will also be imaged on the gate metal, but this is not relevant for this discussion.



Figure 2-4: Kink mechanism when neutrally charged hole traps are present in the insulator. a) At low V_{DS} , the traps are in equilibrium and no kink occurs. b) At $V_{DS} \simeq V_{DS,kink}$, some holes are trapped in the insulator leading to a small threshold shift. c) For $V_{DS} \ge V_{DS,kink}$, all the traps are filled and so the kink saturates.

and the third having an energy smaller than the two previous $(h\nu_{small})$. It turns out that $h\nu_{small}$ does not affect neither the drain nor gate currents as one would expect since no electron-hole pairs are generated. However, $h\nu_{ch}$ has a bigger impact on I_D than $h\nu_{ins}$: for given V_{GS} and $V_{DS} \leq V_{DS,kink}$, the increase in I_D due to $h\nu_{ch}$ is around four times bigger than the one due to $h\nu_{ins}$. Notice that since ΔE_C between channel and insulator is about equal to (the corresponding) ΔE_V , electrons generated by $h\nu_{ins}$ are equally likely to be injected into the channel than the generated holes. As a result, electron-hole recombination in the insulator is unlikely (unless the electron-hole recombination lifetime in the insulator is very short) and so holes should effectively be captured by the traps. Notice also that in the case of $h\nu_{ch}$, only the holes having enough kinetic energy to surmount ΔE_V can be injected into the insulator. From these arguments, $h\nu_{ins}$ should have a bigger impact on the drain current than $h\nu_{ch}$, which contradicts with Hori's hypothesis.

However, hole traps in the insulator remains as a plausible theory for the kink effect as it has not yet been proven to be true or false. The expression for the kink current ΔI_D is given by eq. 2.1 (see Appendix A.1.2 for derivation of ΔV_T^{kink}). The dynamics of such a mechanism are similar to those discussed in 2.2.1.3 except that II generated holes are injected from channel to insulator. The characteristic time constants are then the electron transit time from source to drain, and hole transport and hole capture time in the insulator (respectively $\tau_{tr}^{h,ins}$ and $\tau_{cap}^{h,ins}$). Notice that hole capture will occur only if $\tau_{cap}^{h,ins} \ll \tau_{tr}^{h,ins}$.

Again, we list the key assumptions made in this theory:

- impact ionization
- small ΔE_V between channel and insulator
- significant concentration of hole traps in the insulator
- hole capture in the insulator $(\tau_{cap}^{h,ins} \ll \tau_{tr}^{h,ins})$
- threshold shift

2.2.3 Comments on Trap Related Theories

To conclude the discussion about trap related theories, it is worthwhile noticing that these (trap) theories are of little predictive value due to the large number of variables involved such as the trap concentration, trap type (electron/hole, acceptor/donor type) capture and emission times, trap cross-section, etc., not to mention that traps are material, growth, and process dependent [13, 28, 29]. As a result, CAD and circuit models would require a large number of fitting parameters very unique to each process which is not desirable. From this point of view, a trap-related explanation of the kink is not very practical. These issues, in addition to other experimental results as we will see, led some authors to consider other possible mechanisms for the kink effect.

2.3 Pure Impact Ionization

The plausible trap-related theories discussed previously agree with the idea that impact ionization is the indirect cause of the kink effect. Direct correlation between the kink and impact ionization has indeed been demonstrated in [19]. Some authors proposed that impact ionization is fully responsible for the kink [20, 30]. That is, the II generated electrons drift to the drain and produce the excess drain current whereas the holes either escape through the gate or drift to the source where they eventually recombine. However, it is shown in [8] that the extra drain current due to the II generated electrons cannot by the origin of the kink: by means of a specially designed sidegate structure, a fraction of the impact ionization current, I_{II} , is measured when tracing the usual $I_D - V_{DS}$ curves [31]. While I_{II} grows exponentially with V_{DS} , the kink is seen to saturate for increasing V_{DS} . Consequently, impact ionization by itself cannot explain the kink. Furthermore, it has been shown in [18] that the impact ionization current is only a small fraction of the drain current (~ 1-2 %). Again, this indicates that pure impact ionization cannot explain the kink. So, we rule out this hypothesis and do not discuss it any further.

2.4 SOI Model

Brar et al. proposed an SOI like mechanism as a possible explanation for the kink effect [18, 9, 10]. This is, the undoped buffer and the extrinsic source (the capped portion of it) might behave like a $i-n^+$ or $p-n^+$ junction. The idea is the following: impact ionized holes are injected in the buffer, where they drift to the extrinsic source (fig. 2-5). At the buffer-source junction, the holes encounter an energetic barrier which they need to overcome in order to diffuse into the source where they eventually recombine. This is achieved by forward biasing the $i-n^+$ junction which in turn, results in a buffer potential increase. Consequently, the threshold shifts giving extra drive to the transistor, similarly to section 2.2.1.3. The expression for the kink current ΔI_D is again given by eq. 2.1 (see Appendix A.1.3 for derivation of ΔV_T^{kink}).

The dynamics of this mechanism are: electrons must drift in the channel from source to drain in order to cause impact ionization. Next, II generated holes are injected into the buffer where they drift to the source. Finally, holes are injected from buffer to the source where they diffuse and recombine. The characteristic time constants are then the electron transit time from source to drain (τ_{tr}^e) , hole transit time from drain to source $(\tau_{tr}^{h,buf})$, and the characteristic time constant governing the $i-n^+$ junction, τ_{i-n^+} , which is the smallest of the hole recombination lifetime in the source or electron recombination lifetime or transit time in the buffer.

To conclude this discussion, we list again the key assumptions made in this model:



Figure 2-5: SOI like mechanism. a) At low V_{DS} , no impact ionization occurs and there is no kink. b) At $V_{DS} \simeq V_{DS,kink}$, impact ionization begins and the buffer-source junction begins to get forward biased. c) For $V_{DS} \ge V_{DS,kink}$, significant impact ionization occurs but the kink seems to saturate due to the logarithmic relation between the hole concentration and the threshold shift.

- impact ionization
- small ΔE_V between channel and insulator
- hole drift from drain to source (inside the buffer)
- hole injection from buffer to source leading to a buffer potential increase
- threshold shift

2.5 Source Resistance Reduction due to Excess Drain Current

Source resistance reduction theories have been presented under various forms, as one due to excess drain current [22], or a *barrier induced hole pile up* effect which is discussed in the next section [8]. Enoki *et al.* suggested that the II generated holes drift into the low field

source-gate region, where they diffuse and recombine. To maintain quasi-neutrality, the electron concentration must be increased, resulting in reduced source resistance. However, if this were the case, the excess current would be of the form $\Delta I_D = g_{m0}I_D\Delta R$, where g_{m0} and I_D are "pre-kink" values, and ΔR is the drop in source resistance brought about by the hole accumulation. However, as shown in [8], $|\Delta R|$ should increase with increasing I_D , and thus, the kink current ΔI_D should be superlinear in I_D , which is not the case [8]. So, we do not discuss this theory any further.

2.6 Barrier-Induced Hole Pile-up Theory

Although simple source resistance reduction does not fully explain the kink, recent reports of light emission from the extrinsic source [32] and kink suppression by means of a buried player [18, 33] led several authors to further explore the relation between the extrinsic source and the II-generated holes. Two similar theories have been proposed which essentially consist of *source conductivity modulation* due to hole accumulation near the source [12, 8]. In the case of Kunihiro *et al.*, the hole accumulation originates from hole traps [12]. The accumulated holes lower the potential barrier of the source-channel junction, resulting in increased drain current². Nonetheless, their simulations do predict increased drain current, but no saturation of the kink. This drawback combined with the unpredictability of traps leads us to look at the work presented in [8].

Somerville *et al.* proposed a new mechanism responsible for the kink which they called the *barrier-induced hole pile-up* theory. They postulated that the kink is due to *conductivity* modulation at a small location in the source-end of the device. Essentially, holes generated by II at the drain drift through the channel to the extrinsic source where effective pile-up may occur if they encounter an energy barrier (fig. 2-6). Such a barrier may exist between the capped and uncapped portions of the source, or between the capped portion and the n^+ ohmic contact (the latter junction is the one considered in [12]). The resulting hole pile-up demands that electrons accumulate there in order to maintain local quasi-neutrality. This decreases the source resistance in the vicinity of the barrier hence reducing the extrinsic ohmic drop and giving the transistor an extra drive, V_{kink} (fig. 2-7).

²The source-channel junction that these authors are referring to is actually junction between the uncapped portion of the source and the ohmic contact. Effectively, this is a $n-n^+$ type of junction.



Figure 2-6: Band diagram along the channel from source to drain for a device biased in saturation. The high fields at the drain-end cause impact ionization (1). The II-generated holes drift to the source (2) where they pile-up in a well (3). In order to maintain local quasi-neutrality, electrons from the ohmic contact recombine with the holes (4) (Courtesy of M. H. Somerville).

In this hypothesis, the additional drive on the gate V_{kink} results in increased current given by:

$$\Delta I_D \simeq g_{m0} V_{kink}. \tag{2.2}$$

In [8], Somerville *et al.* postulated that, to the first order, V_{kink} should be related to the excess hole concentration in the vicinity of the barrier, p', and the background electron concentration in the uncapped region, n_o , by a Boltzman type of relation:

$$V_{kink} \simeq \frac{kT}{e} \ln(1 + \frac{p'}{n_o}). \tag{2.3}$$

Notice that since holes pile up in a well, p' cannot exceed the electron concentration in the capped region. That is, we must have $p'/n_o \leq n_o^{cap}/n_o$, where n_o^{cap} is the electron concentration in the capped region.

To date, the expression for V_{kink} is still in dispute for a couple reasons: electrons statistics are more of a 2-D nature and degenerate whereas holes are 3-D (and more likely non-



Figure 2-7: Kink mechanism for the barrier-induced hole pile-up. a) For $V_{DS} \leq V_{DS,kink}$, no II occurs and thus, there is no kink. b) At $V_{DS} \simeq V_{DS,kink}$, weak II causes a small hole pile-up in the vicinity of the source, leading to a decrease in the source resistance. c) II takes on and a significant number of holes accumulate near the source (Courtesy of M. H. Somerville).

degenerate). However, eq. 2.3 seems to agree well with the experiments in [8]. So, even though this expression might not be entirely accurate, we will adopt it in this work.

Regarding the dynamics of such a mechanism, electrons must drift from source to drain in order to cause impact ionization. Next, II generated holes drift to the source where they pile up. The characteristic time constants are: electron transit time from source to drain (τ_{tr}^{e}) , hole transit time from drain to source $(\tau_{tr}^{h,chan})$, and the well recombination lifetime, τ_{well} .

Finally, to conclude, we list the assumptions made in this theory:

- impact ionization
- significant ΔE_V between channel and insulator
- energetic hole barrier in the vicinity of the source
- hole pile-up



Figure 2-8: Simulated hole turn-on transient as a function of time for a single characteristic time constant. The different curves correspond to increasing values of the generation rate.

• source conductivity modulation

2.7 Expected Transient Behavior

Sections 2.2 to 2.6 discussed different mechanisms for the kink effect and the respective dynamics. In all cases, the dynamics were characterized by a transit time and a capture and/or recombination process. In this section, we are interested in the general behavior of these dynamics in the environment of our measurements (see chapter 3). That is, we are interested in the turn-on transient dynamics of the kink. Since the kink is intimately related to hole capture/pile-up (or simply to the number of holes in the area of interest), we need only to be concerned with the dynamics of the holes³. Hole capture/recombination processes are expected to follow some exponential transient behavior from which we describe three possible cases (see Appendix A.2 for derivation of the hole dynamics).

³In this transient analysis, the transit time of electrons and/or holes simply adds a constant delay to the dynamics of the kink and thus need not to be a concern.

2.7.1 Constant Lifetime

The simplest exponential transient is one in which the hole concentration builds-up until recombination matches generation. An expression for this is:

$$p(t) = g_o \tau (1 - e^{-t/\tau}), \tag{2.4}$$

where p, τ , and g_o are respectively the hole concentration, characteristic time constant, and generation function. We plot the transient turn-on hole concentration as a function of time in a semilog scale (eq. 2.4) in fig. 2-8.

Three interesting features are observed in this figure: first, the steady state value of p(t) increases with g_o (see eq. 2.4). Second, the rate at which p(t) rises increases with g_o^4 . Third, the 90% rise time of p(t), $T_{90\%}$, is independent of g_o , where $T_{90\%}$ is the time for p(t) to reach 90% of its final steady state value. In particular, we find that $T_{90\%} \sim 2\tau$.

2.7.2 Concentration Dependent Lifetime

The second case to be considered is one in which the hole concentration builds-up to the point in which high-level injection and/or Auger recombination take place. In this situation, the characteristic time constant τ will depend on the hole concentration p(t).

We plot in fig. 2-9 eq. 2.4 where τ is now dependent on p(t). That is, τ drops with increasing p(t) as recombination is enhanced with a high hole concentration. Compared to fig. 2-8, we now observe that $T_{90\%}$ drops for increasing g_o . The dependence of $T_{90\%}$ on g_o is directly correlated to the functionality of τ on $p(t)^5$. Notice also that, since the final value of the hole concentration depends on τ and g, a drop in τ leads to a smaller DC hole concentration.

2.7.3 Hole Concentration Reaching a Plateau

The third case to be considered is the one in which all the traps or the well become full. That is, there is maximum attainable hole concentration, p_{max} . In this situation, since p(t) can not exceed p_{max} , the final value of p(t) becomes independent of g_o if g_o is sufficiently

⁴This can be seen by taking the derivative of p(t) with respect to time in eq. 2.4. The resulting expression is directly proportional to g.

^bFor simplicity, we assume that τ takes the form $\tau(p) = \tau_o/(1 + p(t))$, where τ_o is constant.



Figure 2-9: Simulated hole turn-on transient as a function of time in the case where the characteristic time constant depends on the hole concentration p(t), where we assumed $\tau = \tau_o/(1 + p(t))$, τ_o being constant.



Figure 2-10: Simulated hole turn-on transient as a function of time for the case when the traps or the well become(s) full (solid lines). This is, the kink saturates for sufficiently large generation rate. The dashed lines correspond to the single characteristic time constant case with no well/traps saturation.

high. Consequently, for high g_o , the kink saturates prematurely. We show this (eq. 2.4) in fig. 2-10 where we assumed $p_{max} = 20$ a.u. and a single characteristic time constant. As it can be seen, $T_{90\%}$ drops when p(t) approaches p_{max} .

Notice also that since ΔV_T^{kink} or V_{kink} are related one-to-one to the hole concentration (eqs. 2.1 and 2.2), if the hole concentration saturates to p_{max} then a similar saturation should be expected for both ΔV_T^{kink} and V_{kink} . This can be expressed as:

$$\Delta V_T^{kink}(t), V_{kink}(t) = \min\{V(t), V_{max}\},\tag{2.5}$$

where V(t) is either ΔV_T^{kink} or V_{kink} , and V_{max} is the plateau value of V(t).

2.8 Summary

In summary, this chapter explored different theories for the kink effect. Four of them seem to be possible: hole traps in either the buffer or the insulator, an SOI-like mechanism, and a barrier-induced hole pile-up model. These theories have in common that impact ionized holes are the indirect cause of the kink, and that the kink current ΔI_D is given by the product of the intrinsic transconductance g_{m0} and some voltage, be it a threshold shift, or a small extra-drive given to the transistor. This will lead to interesting results, as we will see in chapter 4. We also explored three possible exponential turn-on transients for the hole concentration build-up.

In the next chapter, we describe our pulsed I-V setup and present experimental results of the kink dynamics. As these are the first reported measurements of the kink dynamics with nano-second resolution [24], we will describe all the observed features of the kink. In chapter 4 we will discuss these experimental results in light of the theories presented in this chapter.

Chapter 3

Experimental

3.1 Introduction

In this chapter, we describe our pulsed I-V set-up and present experimental measurements on the dynamics of the kink in InAlAs/InGaAs/InP HEMTs. We begin by giving the motivation behind the need of a pulsed I-V setup. We then describe its implementation and its validation. Finally, we present experimental pulsed I-V measurements of the dynamics of the kink effect. We focus on the rise time of the kink, $T_{90\%}$, the time it takes for the kink to reach 90% of its final value, as a first order indicator of the kink's characteristic time constant. We find that $T_{90\%}$ is strongly dependent on V_{DS} . In particular, $T_{90\%}$ drops from 100 μ s down to ~ 50 ns as V_{DS} increases from 1 V to 2.5 V. These results are the first reported measurements of the kink dynamics with nanosecond resolution on InAlAs/InGaAs HEMTs and should be useful in predicting the behavior of the kink at high frequencies [24].

3.2 Experimental Details

3.2.1 Pulsed I-V Setup

Pulsed characterization has been proven to be a good predictor of large signal high-frequency performance which is the relevant one for power applications at high frequencies [23]. There are essentially two reasons for this: first, by definition, in power applications voltages swing over a broad range and thus large signal characterization is required. This eliminates small-signal high frequency characterization (typically S-parameters characterization [34]) in which the device under test is initially biased (DC bias), and then tested with some small



Figure 3-1: Ideal pulsed I-V measurement: the gate is pulsed from off-state $(V_{GS} \leq V_T)$ to some on-state V_{GS} . The drain response to such a pulse is then measured after a delay that we denote T_d . Notice that the drain I-V characteristics are constrained to follow a load line path.

AC high frequency signal. Second, DC characterization masks all fast transient processes and thus cannot be used for high-frequency characterization. Other advantages of pulsed I-V characterization are that pre-measurement thermal effects (self-heating) and possible trap charging/discharging are avoided and thus bias/time dependent states are avoided. This leads to reliable measurements, specially if one is interested in transient behavior.

The main idea to achieve such goals is to pulse the gate from off-state (below threshold) to some on-state gate voltage and to capture the drain response to such a pulse after some (programmable) delay (see fig. 3-1). This scheme avoids self-heating as well as the trap charging/discharging effects mentioned above. The drain response is then measured via a resistive load. By doing so, full control of the drain response is achieved and no hysteresis nor state-dependent transients take place.

We have designed a pulsed I-V setup with the above characteristics that is able to measure drain response transients with nanosecond resolution¹ [24]. The setup is illustrated

¹Previously published work only achieved μ s or ms resolution [15, 35].

in fig. 3-2 and works as follows: the drain is biased via a DC power supply² (V_{DD}) and a load resistance, R_L ($R_L = 50 \ \Omega$). The current drawn by the transistor is evaluated by measuring the voltage at the drain through the R_1/R_2 voltage divider, which is required to protect the T&H due to its limited maximum input voltage. The gate is pulsed from threshold to the desired gate-to-source voltage, V_{GS} , by a dual pulsed generator (PG). The 10 dB attenuator is used to minimize reflections due to impedance mismatch between the 50 Ω environment presented by the cables and the gate. After a programmable delay (T_d) from the gate pulse, a second pulse is sent to a track-and-hold amplifier (T&H). When triggered, the T&H holds constant the voltage read at node V_N at the instant of the trigger³. This allows the digital voltmeter HP3458A (DVM) to read V_N when triggered by the PG⁴. The relative delays between the pulses sent from the PG to the gate, T&H, and voltmeter are independently programmable and have nanosecond resolution⁵.

The whole schematic is implemented in a specially designed high-speed board to minimize wire inductance, crosstalk, and ground bouncing. Measurements are carried out "on-wafer" using coplanar microwave probes. All components have a bandwidth of at least 4 GHz. All measurements have been carried out at room temperature. Further details on the limitations of the setup as well as the Code that has been used can be found in Appendix A.

As mentioned above, the drain response of the transistor is sampled indirectly at node V_N (see fig. 3-2). Once $V_N(T_d)$ is known, $V_{DS}(T_d)$ and $I_D(T_d)$ are easily calculated as:

$$V_{DS}(T_d) = V_N(T_d) \ (1 + \frac{R_1}{R_2}) \tag{3.1}$$

and

$$I_D(T_d) = \frac{V_{DD}}{R_L} - V_{DS}(T_d) \ (\frac{1}{R_L} + \frac{1}{R_1 + R_2}). \tag{3.2}$$

²The HP4145 has been used for V_{DD}

³The T&H works as follows: it has two inputs, one analog and one digital (DIG_{IN}), and one output. The analog input is connected at V_N , whereas DIG_{IN} to the second pulse output of the PG. When DIG_{IN} is low, the T&H output tracks the analog input; when high, the output holds constant the analog input voltage value read at the moment of the low-high transition of DIG_{IN}.

⁴The HP-3458A DVM needs at least to read the input signal for ~ 4-5 μ s in order to digitalize it. This time scale is way much longer than one of interest (ns time scale). Consequently, direct evaluation of the drain response cannot be used for our goals.

⁵The pulses send to the gate and the T&H are the two outputs of the PG; the one send to the DVM is the "Trigger-out".



Figure 3-2: Schematic of the pulsed I-V setup used in this work. The system has nanosecond resolution and is fully automated.

In practice, we find that there is a small DC offset when measuring V_N (around -32 mV) which is due to the internal biasing condition of the T&H⁶. We have accounted for this when computing I_D (eqs. 3.1 and 3.2).

In order to trace the I-V characteristics for given V_{GS} and T_d , we sweep V_{DD} from 0 V up to $V_{DD,max}$ in 0.13 V steps⁷, where $V_{DD,max}$ is such that V_{DS} is kept below the off-state breakdown voltage, $V_{DS,BV}$ ($V_{DS,BV} \simeq 4-5$ V in the measured devices). By setting $I_N = 0$ in eq. 3.2, we find

$$V_{DD,max} \le \left(\frac{R_1 + R_2 + R_L}{R_1 + R_2}\right) V_{DS,BV}.$$
(3.3)

This procedure is then repeated for several values of V_{GS} . For each $V_{DD} - V_{GS}$ pair, T_d samples between 5 ns and 500 μ s were acquired.

Lastly, we want to comment on the duty cycle of our set-up. The duty-cycle must be kept low (below 5-10%) for a couple reasons: first, a fast duty cycle would tend to heat-up

⁶The T&H requires of three different power supplies (+15 V, +5 V, and -5 V). This can lead to a small offset between its input and its output, as is the case in our measurements.

⁷Given the V_{DD} power supply that has been used in this work (HP-4145), the maximum number of V_{DD} increments is 32 (VARIABLE 2 of the HP-4145 is used as V_{DD}). Given this restriction, the V_{DD} increment is such that eq. 3.3 holds for $V_{DS,BV} \simeq 3.5$ V.



2550 A

In_{.52}Al_{.48}As

Figure 3-3: Schematic cross-section of single InAlAs/InGaAs single-heterostructure HEMT used in this work. 1.2 and 2 μ m gate length and 100 μ m wide devices were characterized.

and stress the device. Second, and probably more important, V_{DD} cannot be stepped too fast because of the decoupling capacitor (see fig. 3-2 and Appendix A). It is crucial that V_{DD} is stable before pulsing the gate. Otherwise, eq. 3.2 does not hold and the data is unreliable. In our case, we used a pulse period of 150 ms with a maximum pulse length of 500 μ s yielding a duty cycle of at most 0.3 %. This also prevents self-heating of the device.

3.2.2 Device Structure

As a vehicle for this study we used a lattice-matched, MBE-grown, InAlAs/InGaAs HEMT schematically illustrated in fig. 3-3. The layer structure consists of a 2550 Å InGaAs buffer, a 200 Å InGaAs channel, a 300 Å pseudo-insulator, and a 70 Å InGaAs cap. A delta-doped electron supply layer located 30 Å above the channel yields a sheet carrier concentration of 3.6×10^{12} cm⁻². Fabrication consists of device isolation via a mesa etch with sidewall recess, a PECVD Si₃N₄ layer for liftoff assistance, Au/Ge ohmic contacts, a selective gate recess, and Pt/Ti/Au gates and interconnects [8, 19]. 100 μ m wide devices with gate lengths 1.2 μ m and 2 μ m were characterized. The devices exhibit $I_{D,max} = 700$ mA/mm, $g_{m,peak} = 540$ mS/mm, and $BV_{DS(off)} \simeq 4-5$ V.



Figure 3-4: Pulsed I-V set-up validation: pulsed I-V curves for $T_d \simeq 500 \ \mu s$ (crossed-lines) are compared with DC HP-4145B I-V curves (full lines). Good agreement is observed.

3.3 Results

We will now present our experimental results accompanied with first pass observations. Further discussion of the data is presented in chapter 4. We begin by validating the setup. For this, we measuring pulsed I-V characteristics for relatively long T_d ($T_d \simeq 500 \ \mu$ s) and compared them with DC characteristics obtained using an HP4145. Good agreement is observed as shown in fig. 3-4.

3.3.1 Pulsed I-V Curves

Pulsed I-V characteristics of an $L_g = 1.2 \ \mu m$ device for 8 ns $\leq T_d \leq 10 \ \mu s$ are shown in Fig. 3-5 for a wide range of V_{DS} and V_{GS} . Several observations can be made:

- 1. There is no kink for short T_d (below 10 ns).
- 2. The kink turns-on first and rises faster the higher V_{DS} is. Consequently, $V_{DS,kink}$ is a function of T_d , where, again, $V_{DS,kink}$ is the value of V_{DS} at which the kink turns-on.
- 3. The kink also saturates first the higher V_{DS} is.


Figure 3-5: Pulsed I-V curves for varying delay times, T_d . No kink is seen below $T_d = 10$ ns. For a given V_{GS} , the larger V_{DS} , the earlier the kink turns on and the faster it saturates.

- 4. For $V_{DS} \leq V_{DS,kink}$, I_D is initially static, but eventually builds-up.
- 5. Three time scales can be identified: i) a fast regime where time constants are in the order of a few tenths of nanoseconds (high V_{DS}); ii) a medium fast regime where time constants are in the μ s time scale (V_{DS} close to $V_{DS,kink}$); iii) a slow regime with characteristics time constant above the tenths of μ s (for $V_{DS} \leq V_{DS,kink}$).
- 6. No overshoots nor undershoots are observed.

Similar results are obtained for $L_g = 2 \ \mu m$ devices.

Observations 1 to 3 are consistent with reports in the literature on output conductance measurements of both InAlAs/InGaAs/InP HEMTs [15] and InAlAs/InGaAs/InAlAs MES-FETs [11] in which no kink is observed at high frequencies despite its prominence at DC. Observation 4 was however not reported in the above references. However, notice that the characteristic time constant of the build-up of I_D for $V_{DS} \leq V_{DS,kink}$ is much longer than the one for the build-up of the kink which suggests that the two processes are independent from each other. We believe that these are thermal effects. Regarding observation 6, drain current overshoots have been reported elsewhere even though the nature of their measurement is different [15, 35].

3.3.2 Kink Build-up

The above results provide a rich first pass characterization of the kink dynamics. Nonetheless, these results are difficult to quantify and/or analyze. Consequently, we will now focus on the kink current build-up, *i.e.* on $\Delta I_D(T_d)$, where we define ΔI_D to be the drain current exceeding the pre-kink saturation drain current, $I_{D,prek}$ (see fig. 3-5). However, by doing so, one must take into account the two following points: first, from fig. 3-5, we see that the $I_{D,prek}$ builds-up with time. This must be taken into account in order to decouple the kink from other effects. Second, notice also that the background saturation output conductance, g_d , is small but non-zero and should be taken into consideration when computing $\Delta I_D(V_{DS})$ (see for example the I-V curves in fig. 3-5 corresponding to small values of T_d). From these two arguments, we have decided to compute $\Delta I_D(T_d, V_{DS})$ as:

$$\Delta I_D(T_d, V_{DS}) = I_D(T_d) - [I_{D,prek}(T_d) + g_d(V_{DS} - V_{DS,kink})], \qquad (3.4)$$

where g_d is computed as

$$g_d = \frac{\delta I_D}{\delta V_{DS}} \tag{3.5}$$

at $T_d = 8$ ns and where $V_{DS,sat} \leq V_{DS,prek} \leq V_{DS}$. In other words, ΔI_D is the drain current exceeding the "pre-kink" saturation drain current after output conductance compensation.

3.3.2.1 ΔI_D at Constant V_{GS}

There are several ways of analyzing ΔI_D . We begin by fixing V_{GS} and looking at the kink build-up for $V_{DS} \geq V_{DS,kink}$ in 0.1 V increments. Notice however that, with our pulsed I-V setup, discrete or finite values of V_{DS} are not obtained (eq. 3.1). Consequently, some sort of interpolation is needed. For simplicity, we used linear interpolation around the desired value of V_{DS} from the closest greater and lower values of V_{DS} . ΔI_D is interpolated accordingly.

We show in fig. 3-6 a semilog plot of the interpolated ΔI_D as a function of T_d for three values of V_{GS} ($V_{GS} = -1.1$ V, -0.9 V, and -0.7 V) and 0.9 V $\leq V_{DS} \leq 2.1$ V. Some peculiar features of the kink can be observed:







Figure 3-6: Semilog plot of ΔI_D as a function of T_d for different values of V_{DS} but constant V_{GS} . a) $V_{GS} = -1.1$ V; b) $V_{GS} = -0.9$ V; c) $V_{GS} = -0.7$ V.

- 1. ΔI_D increases with V_{DS} but seems to saturate for sufficient large values of V_{DS} . This is the standard DC behavior of the kink [8, 19].
- 2. Dynamically, the rate at which ΔI_D builds up with time is faster the higher V_{DS} is.
- 3. The kink's saturation also gets sharper for increasing V_{DS} .
- 4. Both the 10 and 90 % rise time of the kink, respectively $T_{10\%}$ and $T_{90\%}$, drop significantly for increasing V_{DS} , where $T_{10\%}$ ($T_{90\%}$) is defined as the time for ΔI_D to reach 10 % (90 %) of its final value.
- 5. For long enough sample delays $(T_d \ge 1 \ \mu s)$, some second order effects (probably thermal effects) take place and lead to small increases of ΔI_D . The origin of this might the same as the one that leads to the increase of I_D for $V_{DS} \le V_{DS,kink}$ (see fig. 3-5).
- **3.3.2.2** ΔI_D at Constant V_{DS}







Figure 3-7: Semilog plot of ΔI_D as a function of T_d for different values of V_{GS} and constant V_{DS} . a) $V_{DS} = 1.7$ V; b) $V_{DS} = 2.1$ V; c) $V_{DS} = 2.5$ V.

Let us now examine the characteristics of the kink dynamics for different values of V_{GS} (-1.3 V $\leq V_{GS} \leq$ -0.7 V) and constant V_{DS} ($V_{DS} = 1.7$ V, 2.1 V, and 2.5 V) (fig. 3-7). The following features can be observed:

- 1. The DC magnitude of ΔI_D increases with V_{GS} , for V_{GS} close to V_T .
- 2. For -0.9 V $\leq V_{GS} \leq$ -0.7 V, the DC magnitude of ΔI_D is about the same.
- 3. The kink saturates faster the higher V_{GS} is.
- 4. $T_{10\%}$ and $T_{90\%}$ also drop significantly for increasing V_{GS} .
- 5. For $T_d \ge 1 \ \mu$ s, the same second order effects are observed, except maybe at $V_{GS} = -0.7 \text{ V}$, where ΔI_D seems to become independent of T_d .

3.3.3 Kink Rise Time: $T_{90\%}$

Section 3.3.2 clearly shows that the kink's characteristic time constant is strongly dependent on both V_{DS} and V_{GS} . We will now quantify the above results by examining the rise time



Figure 3-8: Semilog plot $T_{90\%}$, the time it takes for the kink to reach 90% of its final DC value, as a function of V_{DG} for different values of V_{GS} .

of the kink, $T_{90\%}$. $T_{90\%}$ is plotted in fig. 3-8 as a function of V_{DG} for different values of V_{GS} in a semilog scale. The following features are observed:

- 1. $T_{90\%}$ is found to be a strong function of V_{GS} and V_{DG} for $V_{DG} \leq 2.8$ V: it drops exponentially with V_{DG} . For example, for $V_{GS} = -0.7$ V, $T_{90\%}$ drops by three decades, from ~ 100 µs down to ~ 50 ns, as V_{DG} increases from 1.7 to 2.8 V.
- 2. $T_{90\%}$ becomes rather independent of V_{DG} for $V_{DG} \ge 2.8$ V.
- 3. $T_{90\%}$ is smaller for constant V_{DG} but increasing values of V_{GS} .

Clearly, the dynamics of the kink are not characterized by a single time constant that is independent of V_{DS} and V_{GS} . These results might allow us to understand the physical origin of the kink. We will analyze our observations in chapter 4 and compare them to theoretical predictions.

3.4 Summary

In summary, in this chapter we have described and validated our pulsed IV setup. We have presented for the first time pulsed measurements of the kink dynamics of InAlAs/InGaAs HEMTs in the nanosecond regime. We examined the build-up of ΔI_D with time for both constant V_{GS} and V_{DS} . Our measurements show that the kink's characteristic time constant is characterized by two regimes: for small values of V_{DG} , it decreases exponentially with V_{DG} ; for large values of V_{DG} , it becomes independent of V_{DG} . Time constants between 50 ns and 100 μ s have been observed.

Chapter 4

Discussion

4.1 Introduction

In chapter 3 we presented the first reported measurements on the kink dynamics in In-AlAs/InGaAs/InP HEMTs with nano-second resolution¹ [24]. From this point of view, the experimental characterization of the 90% rise time of the kink, $T_{90\%}$, is a useful result since it suggests that no kink should be present in the millimeter-wave range (from the small signal point of view; fig. 3-8). Furthermore, the peculiar behavior of $T_{90\%}$ can be used to study the physics of the kink².

In this chapter we examine the results presented in chapter 3. Our results seem to indicate that there is a maximum attainable kink. We also find that $T_{90\%}$ is ruled by a universal behavior which only depends on the DC value of the extra voltage drive that generates the kink voltage, V_{kink} . Furthermore, we demonstrate the correlation between the early stages of the kink build-up and impact ionization, supporting the work presented in [19]. To conclude, we compare our findings with the theoretical work presented in chapter 2. We find that the barrier-induced hole pile-up theory for the kink effect and the SOI like mechanism are in agreement with the experiments.

¹Previous work used either small signal AC characterization or μ s resolution transients measurements [15]. ²Small signal high-frequency measurements of the output characteristics, I_D vs. V_{DS} , of HEMTs have indeed shown that no kink is seen in the millimeter-wave range [11, 15]. However, these measurements do not provide any physical insight of the formation of the kink.

4.2 Observations on V_{kink}

In chapter 2, we argued that the kink originates from extra drive given to the transistor, V_{kink} , where V_{kink} results from either a threshold shift or source resistance reduction. Consequently, it is V_{kink} that reveals the physics of the kink rather than ΔI_D^3 . In this section, we examine the general dynamics and behavior of V_{kink} .

4.2.1 Dynamics of V_{kink}

From eqs. 2.1 and 2.2, V_{kink} is simply given by:

$$V_{kink} = \frac{\Delta I_D}{g_{m0}}.$$
(4.1)

The normalization by g_{m0} in eq. 4.1 becomes important when g_{m0} is not constant. In InAlAs/InGaAs HEMTs, g_{m0} is a strong function of V_{GS} as shown in fig. 4-1.

We proceed now to explore the dynamics of V_{kink} as given by eq. 4.1, where the value of $g_{m0}(V_{GS})$ is the one given in fig. 4-1. In fig. 4-2, we plot V_{kink} as a function of T_d for increasing values of V_{GS} and constant V_{DS} ($V_{DS} = 1.7$ V, 2.1 V, and 2.5 V; the raw data $\Delta I_D(T_d)$ was shown in fig. 3-7). We observe the following:

- 1. V_{kink} seems to saturate at around ~ 40 mV for $V_{GS} \ge -1.1$ V and $V_{DS} = 2.1$ V and 2.5 V.
- 2. The rate at which V_{kink} rises increases with V_{GS} for $V_{DS} = 2.1$ V and 2.5 V.
- 3. The saturation of V_{kink} is sharper for increasing values of V_{GS} .
- 4. V_{kink} seems to rise uniformly for -1.1 V $\leq V_{GS} \leq$ -0.7 V and $V_{DS} = 1.5$ V.
- 5. At low values of V_{GS} ($V_{GS} \leq -1.1$ V), V_{kink} increases with V_{GS} , independent of V_{DS} .
- 6. For $T_d \ge 1 \ \mu$ s, V_{kink} seems to continue increasing at a lower rate for all values of V_{GS} and V_{DS} . We believe that these are thermal effects.

We discuss observation 1 in section 4.2.2, and 2, 4-6 in section 4.3.1. Observation 3 is simply a consequence of 1-4. Regarding observation 6, it is important to notice that the kink is a

³In chapter 3 we focused on ΔI_D rather than V_{kink} . The main reason for this is that the frequency-bias dependence of ΔI_D is the relevant parameter in real applications.



Figure 4-1: Measured transconductance, g_m , and resulting intrinsic transconductance, g_{m0} , as a function of V_{GS} ($V_{DS} = 2.5$ V) for the $L_g = 1.2 \ \mu m$ device tested in this work. g_{m0} is obtained from g_m as: $g_{m0} = g_m/(1 - g_m R_S)$, where $R_S = 0.5 \ \Omega$.mm has been used.

rather fast process: as shown in fig. 4-2, the kink builds up in a few tenths of nano-seconds. This suggests that the effects seen for $T_d \ge 1 \ \mu$ s are not correlated to the kink mechanism.

4.2.2 Saturation of V_{kink}

As discussed in the previous section, V_{kink} seems to saturate at around ~ 40 mV for sufficiently high values of V_{GS} and V_{DS} . To see if this is indeed the case, we plot the DC magnitude of V_{kink} , $V_{kink,DC}$, as a function of $(V_{DS} - V_{DS,SAT})^{-1}$ in fig. 4-3⁴, where $V_{kink,DC}$ is defined to be the value of V_{kink} at $T_d = 5 \ \mu$ s. By doing so, we decouple thermal effects from the value of $V_{kink,DC}$ for $T_d \ge 1\text{-}10 \ \mu$ s. However, this definition of $V_{kink,DC}$ cannot be used at small values of V_{DS} ($V_{DS} \sim V_{DS,kink}$): when $V_{DS} \sim V_{DS,kink}$, V_{kink} saturates only after a few tenths of μ s and consequently, the DC value of the kink is not achieved at

⁴As shown in section 4.3.1, the impact generation rate saturates at sufficiently high values of V_{DS} (eq. 4.2) and consequently a saturation behavior of $V_{kink,DC}$ is expected. However, when plotted as function of $(V_{DS} - V_{DS,SAT})^{-1}$, $V_{kink,DC}$ should be linear in $(V_{DS} - V_{DS,SAT})^{-1}$ for all values of V_{DS} if no saturation occurs, as shown in [19].







Figure 4-2: V_{kink} as a function of T_d for increasing values of V_{GS} and constant V_{DS} . a) -1.3 $V \leq V_{GS} \leq -0.7 V$ and $V_{DS} = 1.7$. b) -1.3 $V \leq V_{GS} \leq -0.7 V$ and $V_{DS} = 2.1$. c) -1.3 $V \leq V_{GS} \leq -0.9 V$ and $V_{DS} = 2.5$.

 $T_d = 5 \ \mu$ s. In this case, we computed $V_{kink,DC}$ at the value of T_d at which V_{kink} saturates. This introduces some arbitrariness on the definition of $V_{kink,DC}$, but given that at small values of V_{DS} the data is noisy, a large variance in $V_{kink,DC}$ is expected anyway, regardless of the definition of $V_{kink,DC}$.

As shown in fig. 4-3, $V_{kink,DC}$ does indeed saturate at around ~ 40 mV. At high values of V_{DS} , $V_{kink,DC}$ does not increase linearly any longer with $(V_{DS} - V_{DS,SAT})^{-1}$. On the contrary, $V_{kink,DC}$ bends and seems to saturate. These results are different than those reported in [19], in which no saturation of $\Delta I_{D,DC}$ (and consequently $V_{kink,DC}$) is observed for a wide range of V_{GS} and V_{DS} values. We will see in section 4.3 how this saturation might occur.

4.2.3 Universal Behavior of $T_{90\%}$

As sections 4.2.1 and 4.2.2 indicate, $V_{kink}(T_d)$ provides a rich insight of the dynamics of the kink. As shown earlier, these dynamics are a strong function of both V_{GS} and V_{DS} . However, as fig. 4-2 suggests, the same value of $V_{kink,DC}$ can be obtained with different



Figure 4-3: $V_{kink,DC}$ as a function of $(V_{DS} - V_{DS,SAT})^{-1}$. For $V_{DS} - V_{DS,SAT})^{-1}$, $V_{kink,DC}$ seems to saturate. This suggests that there is a maximum $V_{kink,DC}$ attainable.

combinations of V_{GS} and V_{DS} . Consequently, it is interesting to see if the dynamics of the kink depend only on $V_{kink,DC}$, rather than V_{GS} and V_{DS} . One way of doing this is by exploring the behavior of $T_{90\%}$ as a function of $V_{kink,DC}$.

We plot $T_{90\%}$ as a function of $V_{kink,DC}$ in fig. 4-4. As it can be seen, $T_{90\%}$ depends exponentially on $V_{kink,DC}$, regardless of V_{GS} and V_{DS} . In particular, we observe that, for $V_{kink,DC} \leq 35 \text{ mV}$, $T_{90\%}$ drops with $V_{kink,DC}$ at a rate of one decade every 15 mV, for all V_{GS} and V_{DS} . For $V_{kink,DC} \geq 35 \text{ mV}$ and -1.0 V $\leq V_{GS} \leq -0.7 \text{ V}$, $T_{90\%}$ appears to drop at a rate twice as fast, this is by one decade every ~ 6-7 mV. It seems however that, at the lowest values of V_{GS} ($V_{GS} = -1.2 \text{ V}$ and -1.1 V), this rule of thumb is broken: $T_{90\%}$ drops at one decade every 15 mV regardless of $V_{kink,DC}$.

To the first order, the universal behavior of $T_{90\%}$ observed in fig. 4-4 does not make physical intuitive sense: the higher $V_{kink,DC}$ is, the less time it takes to get there. We saw in chapter 2 (figs. 2-9 and 2-10) that a drop in the recombination/capture lifetime or some type of saturation process might lead to such results. We examine this in the next section.



Figure 4-4: $T_{90\%}$ as a function of $V_{kink,DC}$ for all values of V_{GS} and V_{DS} in a semilog scale. $T_{90\%}$ seems to depend only on the value of $V_{kink,DC}$, independent of the $V_{GS} - V_{DS}$ bias.

4.3 Comparison of Theory and Experimental Results

Section 4.2 provided a first insight of the general characteristics of V_{kink} . We will now discuss such characteristics in light of the models discussed in chapter 2. We first show that the early stages of the kink are correlated to impact ionization. Next, we will see if the saturation of the kink at high values of V_{DS} and V_{GS} and the drop of $T_{90\%}$ are in agreement with the postulated theories in chapter 2.

4.3.1 Impact Ionization

As argued in chapter 2, the four possible mechanisms for the kink effect, hole traps in either the buffer or the insulator, SOI like mechanism, and barrier-induced hole pile-up model (respectively sections 2.2.1.3, 2.2.2, 2.4 and 2.6) agree in that impact ionization is indirectly the origin of the kink. We must consequently demonstrate that the dynamics of V_{kink} do correlated with impact ionization⁵. We proceed similarly to [19] by first extracting the generation function, g, responsible for the kink and then comparing it with classical impact

⁵DC side-gate measurements have already confirmed the correlation between the kink and impact ionization [19]. However, dynamically, this correlation has not yet been demonstrated.

ionization theory (see Appendix A.3). That is, we want to see if

$$g \simeq AI_D e^{-B/(V_{DS} - V_{DS,SAT})},\tag{4.2}$$

where A and B constants, I_D the drain current, and $V_{DS,SAT}$ the saturation drain to source voltage.

The generation function g can be extracted from the early stages of the kink buildup, that is, from $V_{kink}(T_d)$ as $T_d \to 0$ for any V_{GS} and V_{DS} and whatever the origin of g might be. As argued in chapter 2, V_{kink} is related one-to-one to the concentration of impact ionization generated holes, p, in the region of interest (the "regions of interest" are described in chapter 2). In particular, in the limit when p is very small (or equivalently when $T_d \to 0$), $V_{kink}(T_d)$ tracks (one-to-one) $p(T_d)$. In this case, $V_{kink}(T_d)$ takes the form (see Appendix A.2):

$$V_{kink}(T_d) \propto p(T_d) \propto \kappa g \tau (1 - e^{-T_d/\tau}), \qquad T_d \to 0, \qquad (4.3)$$

where κ is some constant independent of V_{GS} and V_{DS} and τ the characteristic time constant. From this equation, we can see that the rate at which V_{kink} builds up, R, is simply:

$$R(T_d) = \frac{d V_{kink}(T_d)}{d T_d} \simeq \kappa g e^{-T_d/\tau}, \qquad T_d \to 0, \qquad (4.4)$$

which in the limit when $T_d \to 0$ (or equivalently $T_d \ll \tau$) becomes

$$R(T_d) \simeq \kappa g, \qquad \qquad T_d \to 0.$$
 (4.5)

As eq. 4.5 indicates, the generation function g (multiplied by κ) can be obtained by extrapolating $R(T_d)$ to $T_d = 0$. In order to see if indeed impact ionization is taking place, the resulting κg intercept should then be compared to equation 4.2⁶.

In practice, $R(T_d)$ can be obtained by fitting a polynomial to $V_{kink}(T_d)$ for small values of T_d and then computing its derivative. By doing so, the noise in $V_{kink}(T_d)$ at small values of T_d is minimized (see fig. 4-2). In particular, we fitted a third order polynomial to $V_{kink}(T_d)$ for $T_d \leq 80$ ns for all values of V_{GS} and V_{DS} . This gave very good fits as shown in fig. 4-5.

⁶The constant κ has no qualitative implications in eq. 4.2 and so is of no concern.



Figure 4-5: Early stages of V_{kink} build-up in a linear scale. Data (dots) and third order polynomial fit (solid lines) for $V_{GS} = -0.9$ V. Similar results were obtained for all values of V_{GS} except for $V_{GS} = -1.3$ V where the data is very noisy.



Figure 4-6: Rising rate (R) of V_{kink} for the same values of V_{GS} and V_{DS} . R is obtained from the derivative of the fitted polynomial to V_{kink} (fig. 4.5).



Figure 4-7: Semilog plot of $\kappa g/I_D$ as a function of $(V_{DS} - V_{DS,SAT})^{-1}$. A classical impact ionization behavior is observed.

The resulting slope is shown in fig. 4-6.

We plot the extrapolated slope of the fitted polynomial, $R(T_d = 0)$, normalized by the drain current I_D as a function of $(V_{DS} - V_{DS,SAT})^{-1}$ in a semilog scale in fig. 4-7. We find that all the data points for all values of V_{GS} and V_{DS} fall into a straight line. This confirms the correlation between the early stages of the kink build-up and impact ionization. For comparison purposes, we find that the rate at which γ/I_D and ζ/I_D drop (*B* constant in eq. 4.2) is around ~ two decades per volt inverse, which is a little less than a half of the one reported in [19]. Notice however that "*B*" is essentially a impact ionization multiplication factor which strongly depends on detailed device structure such as design, cap recess, etc. Given the number of parameters that might change from device to device, a factor of two might be reasonable.

Now that we have confirmed the correlation between the early stages of the kink buildup and impact ionization, some characteristics of the kink dynamics fall into place. In particular, we discuss now observations 2, 4-6 made in section 4.2.1 (also refer to figs. 4-2 and 4-7).

Observation 2: As discussed earlier, $R(T_d)$ is proportional to the impact ionization rate,

 G_{II} . From eq. 4.2, we see that G_{II} (and consequently $R(T_d)$) increases with both V_{GS} (through I_D) and V_{DS} (for sufficiently high V_{DS}).

- **Observation 4:** V_{GS} primarily affects G_{II} through I_D ; however, $V_{DS,SAT}$ is also a function of V_{GS} ($V_{DS,SAT} \simeq V_{GS} - V_T$). Consequently, for V_{DS} close to $V_{DS,SAT}$, increasing V_{GS} has two effects: on one hand, I_D increases; on the other hand, the strength of the electric field at the drain end of the gate is reduced. Consequently, the impact ionization rate remains constant, leading to constant $R(T_d)$.
- **Observation 5:** When V_{GS} is close to threshold, I_D is small. In this case, impact ionization is essentially limited by the amount of carriers that are able to impact ionize (I_D) , provided that the electric field at the drain end of the gate is sufficiently high ($V_{DS} \ge V_{DS,SAT}$). Consequently, G_{II} (and thus $R(T_d)$) only depends on V_{GS} .
- **Observation 6:** As the above discussion suggests, the same value of G_{II} can be obtained for different $V_{GS} - V_{DS}$ combinations and consequently the same value of $V_{kink,DC}$ may be attained provided that the saturation mechanism of V_{kink} for these bias points.

The above discussion on impact ionization and the related effects explain a good deal of the behavior of the kink dynamics. The only two issues that remain to be discussed are the saturation mechanism of V_{kink} and the strong dependency of $T_{90\%}$ on $V_{kink,DC}$. We discuss these issues in light of the four possible mechanisms for the kink effect discussed in chapter 2.

4.3.2 Trap Related Theories

The saturation of $V_{kink,DC}$ at ~ 40 mV at high values of V_{GS} and V_{DS} (fig. 4-3) can be explained by the number of traps being finite: once all the traps are occupied with holes, no extra charge can be accumulated in either the buffer or in the insulator and consequently there must be a maximum attainable threshold shift ($V_{kink,DC}$).

Regarding the exponential dependency of $T_{90\%}$ on $V_{kink,DC}$ there are some possible explanations. As discussed in section 2.7, a saturation mechanism or some type of high level injection effects and/or Auger recombination (which strongly enhance recombination) lead to a drop in $T_{90\%}$. However, as the (initially neutral) hole traps become all full, the average capture time of the traps should become longer and not shorter as fig. 3-8 suggests: as more holes occupy the traps, positive net charge is accumulated. This should induce a local electric field that would tend to repel any close-by free holes. Consequently, the trap cross-section should drop, meaning that the average trap capture time should increase (and not decrease). This contradicts with the results presented in figs. 3-8 and 4-4.

Even though experiments by Brown *et al.* strongly support the idea that hole traps in the buffer are the origin of the kink $[13]^7$, the buffer/insulator trap related theories have a major drawback: these theories can not explain the correlation between light emission in the extrinsic source and the kink effect [32] which suggests that a source related mechanism is the cause of the kink.

Another word of caution must be added to this discussion: experiments by Suemitsu *et al.* showed that the insertion of a *p*-layer underneath the channel suppresses the kink. The idea behind this is that impact ionization generated holes are extracted via the *p*-layer and consequently hole accumulation does not occur. If this were the case, getting rid off of the holes is the key factor to suppress the kink. Returning to Brown's experiments, when growing the buffer at low temperatures, not only the buffer characteristics are changed, but also the buffer/channel interface characteristics. In particular, this interface might become a highly efficient recombination center. In this situation, the buffer/channel interface can prevent impact ionized holes to drift back to the source since they might recombine at the channel/buffer interface⁸ and consequently, a low temperature grown buffer can also suppress the kink in source related mechanisms. Furthermore, non-published experiments in InAlAs/InGaAs HEMTs showed that the kink disappears by passivating the uncapped region between the cap and the gate (see fig. 3-3) [36]. This suggests that neither traps in the buffer nor in the insulator are at the origin of the kink. In any case, more work must be done in this area in order to fully understand the physical origin of the kink.

⁷In their experiments, they found that if the buffer is (MBE) grown at low temperatures (150 °C), the kink is eliminated. Notice that this rules out the theory of traps in the insulator.

⁸When impact ionization occurs at the drain-end of the device, some holes remain confined to the channel due to the ΔE_V between channel and buffer/insulator. In this case, when drifting towards the source, the holes are pushed to the channel/buffer interface by the vertical electrical field and thus hole recombination at this interface is enhanced. This might prevent holes from getting to the source.

4.3.3 SOI Like Mechanism

The SOI like mechanism predicts well the behavior of $V_{kink,DC}$ in fig. 4-3 for $(V_{DS} - V_{DS,SAT})^{-1} \ge 1 V^{-1}$: from eqs. A.8 and 4.2, we have that

$$\Delta V_T^{kink} \propto \ln[1 + AI_D e^{-B/(V_{DS} - V_{DS,SAT})}],\tag{4.6}$$

where A and B are constants. If the hole concentration in the buffer exceeds the intrinsic hole concentration as it should be the case in order to produce a kink (*i.e.*, $p \gg p_o$; see Appendix A.1.3), the above equation can be simplified to

$$\Delta V_T^{kink} \propto C \ln(I_D) - \frac{B}{V_{DS} - V_{DS,SAT}}$$
(4.7)

where C is another constant.

As eq. 4.7 indicates, a linear dependency of ΔV_T^{kink} (or $V_{kink,DC}$) on $(V_{DS} - V_{DS,SAT})^{-1}$ is expected. However, this simple analysis does not explain the saturation of V_{kink} for $(V_{DS} - V_{DS,SAT})^{-1} \le 1 V^{-1}$ (fig. 4-3). To understand how this can happen in this SOI like picture, let us focus on the hole injection mechanism from buffer to source. Due to fermilevel pinning at the InAlAs/InP interface (buffer/substrate interface), there is a vertical electric field, ε_{pin} , that pushes the holes located in the buffer to the InAlAs/InP interface. Consequently, if holes are injected from the buffer to the channel, they must overcome this electric field. Since no electric potential is applied between the substrate and the source, the only way that this hole injection might occur is by diffusion. In particular, since there is a hole impact ionization current in the buffer drifting from the drain towards the source, some type of hole pile-up must occur near the InAlAs/InP interface underneath the extrinsic source. This generates the required hole concentration gradient that will inject holes to the channel. Under pulsed operation, steady state is achieved when the hole concentration gradient is such that the impact ionization current in the buffer diffuses into the source, and thus overcomes ε_{pin} . However, ε_{pin} might not be very large. In this case, when the impact ionization hole current is sufficiently high (high impact ionization rate), the barrier lowering between buffer and source (so that diffusion takes place) might be large enough to cancel ε_{pin} . Beyond this point, holes do not encounter any barrier between the back-end of the buffer and the channel. In this situation, there is also a saturation mechanism. That

is, since the barrier for holes is not reduced any longer even if the impact ionization rate is increased, a maximum threshold shift occurs, producing the effect observed in fig. 4-3.

Following the above line of thought, a drop of $T_{90\%}$ with increasing $V_{kink,DC}$ is also expected. In order to have a kink, the holes from the back end of the buffer must diffuse to the portion of the channel underneath the source. The "ability" of these holes to diffuse to the channel can be interpreted as a buffer resistance, R_{buff} , which is modulated by the hole concentration gradient. Since the holes are lowering the channel/buffer barrier all the way from the InAlAs/InP interface, the buffer effectively behaves like a capacitor, C_{buff} . In this case, the transient behavior under pulsed operation is simply characterized by the buffer $R_{buff}C_{buff}$ constant. Since the buffer resistance is determined by the hole concentration gradient in the buffer which in turn is set by the impact ionization rate, R_{buff} decreases when the impact ionization rate increases. In this situation, $T_{90\%}$ must drop for increasing V_{DG} . This is in agreement with fig. 3-8.

The SOI like mechanism is also in agreement with the experiments in [13], [25], and [33]. In addition, since the injected holes from buffer to source must recombine somewhere, light emission is also very possible in the extrinsic source area of the device, in agreement with the work presented in [32]. The only drawback of this model is that device passivation should not affect this mechanism at all. In any case, the SOI like mechanism remains as a strong candidate for the physical origin of the kink.

4.3.4 Barrier-Induced Hole Pile-up Model

The barrier induced hole pile-up theory predicts a saturation of V_{kink} : since the well where the holes pile-up at the cap/uncapped or the ohmic contact/capped portions of the source is finite (fig. 2-6), only a finite amount of holes can pile-up. Once the well is full, no additional holes can pile-up (additional holes simply drift to the source since the barrier is suppressed) and consequently the source resistance can not be modulated any longer. In this case, the kink simply saturates, independent of V_{GS} and V_{DS} .

Regarding the dependence of $T_{90\%}$ on $V_{kink,DC}$, as discussed in chapter 2, the characteristic time constant can drop by either a saturation mechanism and/or Auger/high level injection effects. In the barrier induced hole pile-up model, the kink saturates because either recombination in the well matches generation, or because the well is full. However, in order to have source conductivity modulation, the source must be driven into high level injection. In this case, a drop in the life time is expected due to Auger recombination and/or other high level injection effects. In addition, when the well saturates, as discussed earlier, $T_{90\%}$ must drop if the impact ionization generation rate is increased.

In conclusion, we find that the barrier induced hole pile-up model predicts well the dynamics of the kink. Furthermore, this model also explains the light emission experiments in [32] since effective recombination is taking place in the extrinsic source.

4.4 Summary

This chapter explored the dynamics of V_{kink} as well as its saturation behavior. We found that there seems to be a maximum V_{kink}^{max} beyond which V_{kink} cannot increase any further. This can be explained by either a finite number of traps (be it in the buffer or in the insulator), or a finite well (barrier induced hole pile-up model). We also found that the 90% rise time of the kink only depends on the final value of V_{kink} , $V_{kink,DC}$, independent of the $V_{GS} - V_{DS}$ bias: $T_{90\%}$ drops exponentially with $V_{kink,DC}$ at a rate of one decade every 15 mV, provided that $V_{kink,DC}$ is less than V_{kink}^{max} . However, when $V_{kink,DC}$ approaches V_{kink}^{max} , $T_{90\%}$ drops at a higher rate. We also confirmed the correlation between the dynamics of the kink and impact ionization by exploring the early stages of the kink build-up. This explains the faster kink build-up rate for increasing values of both V_{GS} and V_{DS} . Our measurements together with other experimental work [32, 33] are consistent with the barrier-induced hole pile-up theory for the kink effect and the SOI like mechanism.

Chapter 5

Conclusions and Suggestions

The high potential of lattice-matched InAlAs/InGaAs HEMTs on InP for millimeter-wave low noise and power applications motivates a study for the understanding of the physical origin of the kink effect as well as its behavior at high frequencies. The study includes a theoretical discussion of previous proposed models for the kink effect, and a experimental characterization of the kink dynamics under pulsed operation for a wide range of bias points $V_{GS} - V_{DS}$. The results of the study suggest that, from the small signal point of view, no kink should be present in the millimeter-wave range at any operating bias.

Previous reported works allowed us to conclude that there are four possible explanations of the physical origin of the kink: hole traps in either the buffer or the insulator that get (positively) charged with impact ionization generated holes, leading to a threshold shift; an SOI like mechanism which forward biases the buffer-channel junction in order to get rid off of impact ionized holes injected in the buffer, also leading to a threshold shift; and a barrier induced hole pile-up model in which holes accumulate in the extrinsic source causing a source resistance reduction which in turn gives extra drive to the transistor. The first three theories require of impact ionized holes transfer from channel to buffer or insulator. This might not be a valid assumption since the valence band discontinuity in InAlAs/InGaAs HEMTs between channel and insulator or buffer is relatively large ($\Delta E_V \simeq 0.3 \text{ eV}$). In the barrier induced hole pile-up model, it is assumed that (most) holes are confined to the channel. In any case, the "kink current" has a similar origin in these four theories; that is, a small voltage, V_{kink} , gives extra drive to the transistor and generates extra drain current. We argue that the dynamics of the four theories are similar and are characterized by the following time constants: the electron transit time from source to drain; hole transit time from drain to source (be it in the buffer or the channel) or hole transport time in the insulator; hole capture and hole recombination time constants. We also argue that the SOI mechanism might involve some RC time constant. In any case, the hole dynamics are characterized by a exponential behavior.

Using a specially designed pulsed I-V setup, we carried out the first experimental characterization of the kink dynamics with nano-second resolution. In our setup, the gate of the HEMT is pulsed from off-state to some on-state and the drain response to such a pulse is measured via a load line and after a variable delay, T_d . We have validated the setup by comparing long pulsed transient measurements to conventional DC I-V curves. Good agreement is observed.

We measured the output characteristics, $I_D - V_{DS}$, of a 1.2 μ m gate length HEMT for increasing values of -1.3 V $\leq V_{GS} \leq$ -0.7 V, 0 V $\leq V_{DS} \leq$ 3.5 V, and 5 ns $\leq T_d \leq$ 500 μ s. V_{GS} is limited by the DC power supply on the drain side whereas V_{DS} by off-state breakdown voltage. In order to analyze the transient behavior of the output characteristics of the HEMT under pulsed operation, we have defined a kink current, $\Delta I_D(T_d)$, which is the excess drain current on top of the pre-kink saturation drain current. In particular, we focused on $\Delta I_D(T_d)$ for either constant V_{GS} and increasing V_{DS} , or constant V_{DS} and increasing V_{GS} . The key results are that: $\Delta I_D(T_d)$ turns on earlier and rises faster for increasing V_{GS} and V_{DS} ; the saturation of $\Delta I_D(T_d)$ is sharper for increasing V_{GS} and V_{DS} ; the DC magnitude of ΔI_D is higher the larger V_{GS} and V_{DS} are (at least for the measured values of V_{GS} ; no overshoots nor undershoots were observed. In order to characterize the kink's characteristic time constant, we have considered the 90% rise time of the kink, $T_{90\%}$, the time it takes for the kink to reach 90% of its final DC value, as a first order approximation of this time constant. In particular, our measurements show that $T_{90\%}$ is characterized by two regimes: for small values of V_{DG} , it decreases exponentially with V_{DG} ; for large values of V_{DG} , it becomes independent of V_{DG} . Time constants between 50 ns and 100 μ s have been observed.

To interpret our results, we argue that the meaningful physical parameter to analyze is V_{kink} rather than ΔI_D . By focusing on $V_{kink}(T_d)$, our measurements show that there is a maximum attainable V_{kink} , V_{kink}^{max} . We also found that $T_{90\%}$ only depends (exponentially) on $V_{kink,DC}$, independent of the $V_{GS} - V_{DS}$ bias, where $V_{kink,DC}$ is the DC value of V_{kink} .

Furthermore, our findings show the early stages of the kink-build-up do indeed correlate with impact ionization. This confirms reports correlating the DC behavior of the kink with impact ionization.

Finally, we argue that the saturation behavior of $V_{kink,DC}$ (V_{kink}^{max}) can be explained by the four suggested theories for the kink effect. However, the sharp drop of $T_{90\%}$ is hardly explained by the trap related theories. Furthermore, light emission experiments strongly support a source-related mechanism. Given the above considerations, our results are consistent with the barrier induced hole pile-up model for the kink effect and the SOI like mechanism.

However, our results do not provide a convincing proof of any one particular mechanism. More work needs to be done, both experimentally, and in simulations. For example, the dependence of the dynamics of the kink on gate length must be analyzed: state of the art technology uses uses sub-micron gate length HEMTs and we only characterized a $L_g = 1.2 \mu$ m device. Furthermore, since HEMTs do operate in a wide range of temperatures, the temperature dependence of the kink dynamics should also be experimentally determined. In order to be able to distinguish the different type of mechanisms that are creating the kink, the effect of the gate recess on the kink can be analyzed. This should clearly identify whether or not buffer and/or insulator traps might originate the kink. Also, pulsed characterization of passivated/non-passivated devices (non-published work [36]) could also provide great insight on the physical origin of the kink. Finally, computer simulations could also give valuable information on the location(s) where holes possibly accumulate, the dependency of V_{kink} on the impact ionization generated holes, and the characteristics of the kink build-up dynamics.

Appendix A

Mathematical Derivations

A.1 Computation of ΔV_T^{kink}

In chapter 2, we saw that three possible theories for the kink effect postulate that the kink arises from a threshold shift, ΔV_T , which gives extra drive to the transistor. This threshold shift might be due to charge build-up in the buffer (section 2.2.1.3) or in the insulator (section 2.2.2) or an SOI like effect (section 2.4). We derive in this appendix a first pass derivation of ΔV_T for these theories.

A.1.1 Traps in the Buffer

We begin by finding the threshold voltage, V_T^0 , of a single InAlAs/InGaAs heterostructure with no traps, and with undoped buffer and insulator (fig. 3-3). The computation of V_T^0 is easily derived by looking at the conduction band diagram at threshold (fig. A-1). Notice that because the buffer is undoped (*i.e.*, there is no net charge) and the channel is depleted, both the conduction and valence bands (respectively E_C and E_V) in the channel must be flat. In this case, V_T^0 is simply obtained as:

$$V_T^0 = \Phi_B - \frac{1}{e} \Delta E_C - \frac{eN_S}{\epsilon_{ins}} t_{ins}, \tag{A.1}$$

where Φ_B , ΔE_C , N_S , t_{ins} , ϵ_{ins} , and e are respectively the InAlAs Shottky barrier height, the conduction band discontinuity between insulator and channel, insulator δ -doping concentration (in cm⁻²), insulator thickness, InAlAs dielectric constant, and electron charge.

If net charge is present in the buffer, V_T^0 and fig. A-1 must be modified: band bending



Figure A-1: Conduction band diagram at threshold for a single heterostructure with undoped buffer and gate insulator.

must occur in the buffer. We show this in fig. A-2 where positive net charge in the buffer has been assumed. The threshold voltage, V_T^{kink} , in this situation is obtained as:

$$V_T^{kink} = \Phi_B - \frac{1}{e} \Delta E_C - \varepsilon_1 t_{ins} - \varepsilon_B (t_s + t_c), \qquad (A.2)$$

where t_s and t_c are respectively the spacer and channel thickness, and ε_1 and ε_B are respectively the electric fields due to the insulator δ -doping and the charge in the buffer and are related by (see fig. A-2):

$$\varepsilon_1 = \varepsilon_B + \frac{eN_S}{\epsilon_{ins}} t_{ins}.$$
 (A.3)

By using Gauss's law, we can relate ε_B to the net buffer charge as:

$$|\varepsilon_B| = \frac{e}{\epsilon_{ins}} \int_{t_{ins}+t_s+t_c}^{\infty} N_t(x) dx, \qquad (A.4)$$

where N_t is the net ionized trap/impurity concentration in the buffer. From eqs. A.1 to A.4, we find that the threshold shift, $\Delta V_T^{kink} = V_T^{kink} - V_T^0$, is:

$$\Delta V_T^{kink} = -\frac{e(t_{ins} + t_s + t_c)}{\epsilon_{ins}} \int_{t_{ins} + t_s + t_c}^{\infty} N_t(x) dx.$$
(A.5)



Figure A-2: Conduction band diagram at threshold with net charge in the buffer. Positive net charge has been assumed.

As eq. A.5 indicates, if $N_t(x) = 0$, then $\Delta V_T^{kink} = 0$ as we would expect since there is no net buffer charge. Notice also that positive net charge leads to a negative threshold shift, which is the one required to give extra drive to the transistor (eq. 2.1).

A.1.2 Traps in the Insulator

When traps are located in the insulator, ΔV_T^{kink} can be found by the same procedure as in section A.1.1. In this case, ΔV_T^{kink} is found to be:

$$\Delta V_T^{gate} = -\frac{e}{\epsilon_{ins}} \iint_0^{t_{ins} + t_s^-} N_t(x) dx.$$
 (A.6)

A.1.3 SOI Like Mechanism

As discussed in section 2.4, the threshold shift ΔV_T^{kink} arises from forward biasing the buffer-channel junction so that the holes in the buffer diffuse to the source. We denote the resulting potential difference between source and buffer as V_{SB} . An expression for ΔV_T^{kink}

can obtained by assuming that ΔV_T^{kink} is proportional to V_{SB}^{1} . In this case, we must find the separation of the quasi-fermi level for holes and electrons, $\Delta \xi$, at the buffer-source junction since $V_{SB} = \Delta \xi/e$. Notice that, since the source is degenerate and the buffer is intrinsic, $\Delta \xi$ will essentially be a fraction of the shift of the hole quasi fermi level due to the hole population increase (this is, the holes generated by impact ionization):

$$\Delta \xi \simeq \beta \ (\xi_i - \xi_h) = \beta \ kT \ln(1 + \frac{p'}{p_o}), \tag{A.7}$$

where β is a constant less than unity, and ξ_i , ξ_h , k, T, p', and p_o are respectively the intrinsic fermi level, quasi-fermi level for holes, Boltzmann constant, temperature (in ${}^{o}K$), excess hole concentration in the buffer near the buffer-source junction, and intrinsic buffer hole concentration.

From the above discussion and eq. A.7, we find that ΔV_T^{kink} is

$$\Delta V_T^{kink} \simeq \gamma \frac{kT}{e} \ln(1 + \frac{p'}{p_o}), \tag{A.8}$$

where γ is a constant less than unity.

A.2 Turn-on Dynamics of the Holes

The dynamics of the kink in each one of the four plausibles theories for the kink effect are governed by hole recombination and/or hole capture processes (see sections 2.2 and 2.6)². If we are interested in the hole dynamics when the generation function, g, is suddenly turnedon (this is, g(t) = 0 for $t \le 0$, and $g = g_0$ for $t \ge 0$, where g_0 is positive and non-zero), we must solve the holes' continuity equation:

$$\frac{\delta p(x,t)}{\delta t} = g - \frac{p}{\tau} - \frac{1}{e} \frac{\delta J_h}{\delta x},\tag{A.9}$$

where g, τ , and J_h are respectively the generation function, hole time constant (be it recombination or capture time constant), and hole current density, and where Shockley-

 $^{{}^{1}\}Delta V_{T}$ is actually proportional to the threshold electric field between channel and buffer. The exact relation between the electric field and V_{SB} is complicated and we don't deal with it here. However, to the first order, we can assume that this electric field is proportional to V_{SB} .

 $^{^{2}}$ As mentioned in section 2.7, this hypothesis fails if either all the traps or the well become full (respectively sections 2.2 and 2.6).

Read-Hall statistics have been assumed [37, 38].

For constant current density $(\delta J_h/\delta x = 0)$ and assuming g_o independent of position, p(t) is given by:

$$p(t) = g_o \tau (1 - e^{-t/\tau}).$$
 (A.10)

A.3 Impact Ionization Generation Function

The impact ionization rate G_{II} has been found to be (empirically):

$$G_{II} = \alpha_n \frac{|j_n|}{e} + \alpha_p \frac{|j_p|}{e}, \qquad (A.11)$$

where j_n and j_p are the electron and holes current densities, e the unit electric charge, and α is (empirically) given by:

$$\alpha = A e^{-(B/E)^{\beta}},\tag{A.12}$$

where A, B, and β are constants, and E the electric field.

To the first order, E can be approximated to $(V_{DS} - V_{DS,SAT})/l$, where $V_{DS,SAT}$ is the drain to source saturation voltage, and l some constant. Combining eqs. A.11 and A.12 with $j_p = 0$, we obtain

$$G_{II} \simeq A' I_D e^{-(B/(V_{DS} - V_{DS,SAT}))},$$
 (A.13)

where A' some constant, and I_D the drain current.

Bibliography

- R. Dingle, H. Stormer, A. C. Gossard, and W. Wiegmann, "Electron mobilities in modulation doped semiconductors heterojunction superlattices," *Appl. Phys. Lett.*, vol. 33, no. 7, pp. 665-667, 1978.
- [2] L. D. Nguyen, et al., "50 nm Self-aligned gate pseudomorphic AlInAs/GaInAs High Electron Mobility Transistors," *IEEE Trans. Electron Devices*, vol. 39, pp. 2007-2014, 1992.
- [3] P. M. Smith, S. J. Liu, M. Y. Kao, P. Ho, S. C. Wang, K. H. Duh, S. T. Fu, and P. C. Chao, "W-Band high efficiency InP-based power HEMT with 600 GHz f_{max}," *IEEE Microwave and Guided Lett.*, vol. 5, no. 7, pp. 230-232.
- [4] S. Tiwari, Compound Semiconductors Device Physics, Academic Press, 1992.
- [5] S. Krishnamurthy and A. Sher, "Velocity-field characteristics of III-V semiconductor alloys: Band structure influences," J. Appl. Phys., vol. 61, pp. 1475-1479, 1987.
- [6] K. Hikosaka, S. Sasa, N. Harada, and S. Kuroda, "Current-gain cutoff frequency comparison of InGaAs HEMT's," *IEEE Electron Device Lett.*, vol. 9, no. 5, pp. 241-243, 1988.
- [7] S. R. Bahl, "Physics and Technology of InAlAs/n⁺-InGaAs Heterostructure Field Effect Transistors," Ph.D. Thesis, Massachusetts Institute of Technology (1993).
- [8] M. H. Somerville, J. A. del Alamo, and W. Hoke, "A new physical model for the kink effect on InAlAs/InGaAs HEMT's," in 1995 Int. Electron Devices Meeting Tech. Dig., pp. 201-204.

- [9] K. Kato, T. Wada, and K. Taniguchi, "Analysis of kink characteristics in silicon-oninsulator MOSFET's using two-carrier modeling," *IEEE Trans. Electron Devices*, vol. ED-32, no. 2, pp. 458-462, 1985.
- [10] H. Hazama, M. Yoshimi, M. Takahashim S. Kambayashi, amd H. Tango, "Suppression of drain-current overshoot in SOI-MOSFET's with floating body," *Electron.Lett.*, vol. 24, no. 20, p. 1266, 1988.
- [11] J. B. Kuang, P. J. Tasker, G. W. Wang, Y. K. Chen, L. F. Eastman, O. A. Aina, H. Hier, and A. Fathimulla, "Kink effect in submicrometer-gate MBE-grown In-AlAs/InGaAs/InAlAs Heterojunction MESFET's," *IEEE Electron Device Lett.*, vol. 9, no. 12, pp. 630-632, 1988.
- [12] K. Kunihiro, H. Yano, N. Goto, and Y. Ohno, "Numerical analysis of kink effect in HJFET with heterobuffer layer, *IEEE Trans. Electron Devices*, vol. 40, no. 3, pp. 493-497, 1993.
- [13] A. S. Brown, U. K. Mishra, C. S. Chou, C. E. Hooper, M. A. Melendes, M. Thompson, L. E. Larson, S. E. Rosenbaum, and M. J. Delaney, "AlInGas-GaInAs HEMT's utilizing low-temperature AlInAs buffers grown by MBE," *IEEE Electron Device Lett.*, vol. 10, no. 12, pp. 565-568, 1989.
- [14] T. Zimmer, D. Ouro Bodi, J. M. Dumas, N. Labat, A. Touboul, and Y. Danto, "Kink effect in HEMT structures: A trap-related semi-quantitative model and an empirical approach for spice simulation," *Solid-State Electron.*, vol. 35, no. 10, pp. 1543-1548, 1992.
- [15] W. Kruppa and J. B. Boos, "Examination of the kink effect in InAlAs/InGaAs/InP HEMT's using sinusoidal and transient excitation," *IEEE Trans. Electron Devices*, vol. 42, no. 10, pp. 1717-1723, 1995.
- [16] G. G. Zhou, A. F. Fischer-Colbrie, and J. S. Harris, "I-V kink in InAlAs/InGaAs MODFET's due to weak impact ionization in the InGaAs channel," in 6th Int. Conf. on InP and Rel, Mater., Mar. 1994, pp. 435-438.

- [17] T. Akazaki, H. Takayanagi, and T. Enoki, "Kink effect in an InAs-inserted-channel InAlAs/InGaAs inverted HEMT at low temperature," *IEEE Electron Device Lett.*, vol. 17, no. 7, pp. 378-380, 1996.
- [18] B. Brar and H. Kroemer, "Influence of impact ionization on the drain conductance of InAs/AlSb quantum well HFET's," *IEEE Electron Device Lett.*, vol. 16, no. 12, pp. 548-550, 1995.
- [19] M. H. Somerville, J. A. del Alamo, and W. Hoke, "Direct correlation between impact ionization and the kink effect in InAlAs/InGaAs HEMT's," *IEEE Electron Device Lett.*, vol. 17, no. 10, pp. 473-475, 1996.
- [20] M. Chertouk, H. Heiß, D. Xu, S. Kraus, W. Klein, G. Böhm, G. Tränkle, and G. Weimann, "Metamorphic InAlAs/InGaAs HEMTs on GaAs substrates with composite channels and f_{max} of 350 GHz," 7th Int. Conf. on InP and Rel. Mat., p. 737, 1995.
- [21] Y. Hori and M. Kuzuhara, "Improved model for the kink effect in AlGaAs/InGaAs heterojunction FET's," *IEEE Trans. Electron Devices*, vol. 41, no. 12, pp. 2262-2266, 1994.
- [22] T. Enoki, T. Kobayashi, and Y. Ishii, "Device technologies for InP-based HEMT's and their applications to IC's," *IEEE GaAs IC symp.*, 1994, pp. 337-339.
- [23] A. Platzker, A. Palevsky, S. Nash, W. Struble, and Y. Tajima, "Characterization of GaAs devices by a versatile pulsed I-V measurement system" 1990 IEEE MTT Symposium Digest, pp. 1137-1140.
- [24] A. N. Ernst, M. H. Somerville, and J. A. del Alamo, "Dynamics of the kink effect in InAlAs/InGaAs HEMTs," 9th Int. Conf. on InP and Rel. Mat., pp. 353-356, 1997.
- [25] J. Haruyama, H. Negishi, Y. Nishimura, and Y. Nashimoto, "Substrate-related kink effects with strong ligh-sensitivity in AlGaAs/InGaAs pHEMT," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 55-33, 1996.
- [26] W.P. Hong, R. Bhat, J.R. Hayes, C. Nguyen, M. Koza, and G.K. Chang, "High-Breakdown, high gain in InAlAs/InGaAsP quantum-well HEMT's," *IEEE Electron Dev. Lett.*, vol. 12, no. 10, pp. 559-561, 1991.

- [27] G.G. Zhou, A.F. Fischer-Colbrie, J. Miller, Y.C. Pao, B. Hughes, L. Studebaker, and J. S. Harris, "High output conductance of InAlAs/InGaAs/InP MODFET due to weak impact ionization in the InGaAs channel," in Tech. Dig. of 1991 IEDM, pp. 247-250.
- [28] A. S. Brown, U. K. Mishra, and S. E. Rosenbaum, "The effect of interface and alloy quality on the dc and RF performance of Ga_{0.47}In_{0.53}As - Al_{0.48}In_{0.52}As HEMTs," *IEE Trans. Electron Devices*, vol. 36, no. 4, pp. 641, 1989.
- [29] U. K. Mishra et al., "Impact of buffer layer design on the performance of AlInAs-GaInAs HEMTs," presented at the DRC, Cambridge, MA. 1989.
- [30] C. Heedt, F. Buchali, W. Prost, W. Brockerfoff, D. Fritzsche, H. Nickel, R. Losch, W. Schlapp, and F. Tegude, "Drastic reduction of gate leakage in InAlAs/InGaAs HEMT's using a pseudomorphic InAlAs hole barrier layer," *IEEE Trans. Electron Devices*, vol. 41, no. 10, pp. 1685-1689, 1994.
- [31] A. A. Moolji, S. R. Bahl, and J.A. del Alamo, "Impact ionization in InAlAs/InGaAs HFETs," *IEEE Electron Dev. Lett.*, vol. 15, p. 315, 1994.
- [32] N. Shigekawa, T. Enoki, T. Furuta, and H. Ito, "Electroluminescence measurement of InAlAs/InGaAs HEMTs lattice-matched to InP substrates," in 8th Int. Conf. InP and Rel. Mater., 1996 pp. 681-684.
- [33] T. Suemitsu, T. Enoki, and Y. Ishii, "Body contacts in InP-based InAlAs/InGaAs HEMTs and their effects on breakdown voltage and kink suppression," *Electron. Lett.*, vol. 31, p. 758, 1995.
- [34] J. L. Lee, J.K. Mun, H. Kim, J.J. Lee, and H.M. Park, "A 68% PAE, GaAs power MESFET operating at 2.3 V drain bias for low distortion power applications," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 519-526, 1996.
- [35] A. Gautier-Levine, P. Audren, G. Post, M.P. Favennec, and J.M. Dumas, "A study of trap related drain lag effects in InP HFETs," 8th Int. Conf. on InP and Rel. Mat., pp. 670-673, 1996.
- [36] Personal discussion with Hans Rohdin from Hewlett-Packard Laboratories, Palo Alto, California, on May 13, 1997.

- [37] W. Shockley and W. T. Read, "Statics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835-842, 1952.
- [38] R. N. Hall, "Recombination processes in semiconductors," *Proc. Inst. Elec. Eng.*, vol. 106B, suppl. 17, pp. 923-931, 1959.