Nested Chopper Stabilization in Analog Multipliers and Mixers

by

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Abstract

We describe a general offset-cancelling architecture for analog multiplication using chopper stabilization. Chopping is used to modulate the offset away the output signal where it can be easily filtered out, providing continuous offset reduction which is insensitive to drift. Both square wave chopping and chopping with orthogonal spreading codes are tested and shown to reduce the offset down to the microvolt level. In addition, we apply the nested chopping technique to an analog multiplier which employs two levels of chopping to reduce the offset even further. We discuss the limits on the performance of the various chopping methods in detail, and present a detailed analysis of the residual offset due to charge injection spikes. An illustrative CMOS prototype of a chopper-stabilized general-purpose multiplier in a 0.18μm process is presented which achieves a worst-case offset of 1.5μV. This is the lowest measured offset reported in the DC analog multiplier literature by a margin of two orders of magnitude. The prototype multiplier is also tested with AC inputs as a squarer, variable gain amplifier, and direct-conversion mixer, demonstrating that chopper stabilization is effective for both DC and AC multiplication. The AC measurements show that chopping removes not only offset, but also 1/f noise and 2nd-order harmonic distortion. The specific application of chopper stabilization to RF direct-conversion mixers is also discussed in detail, showing how it can be used to improve the sensitivity of direct-conversion receivers by reducing the mixer’s offset, 1/f noise, and even-order distortion. A prototype IC of a chopper-stabilized RF mixer in a 0.18μm CMOS process is presented, along with measured results.
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Contents

1 Introduction 17
   1.1 Motivation ........................................ 17
   1.2 Organization ...................................... 19

2 Multiplier Offset Cancellation Techniques 21
   2.1 Trimming ........................................... 21
   2.2 Nonlinear Multiplicative Feedback .................. 23
   2.3 Digital Integrator in Feedback ..................... 24

3 Chopper Stabilization in Multipliers 27
   3.1 Principle of Chopper-Stabilized Amplifiers ........ 27
   3.2 Principle of Chopper-Stabilized Multipliers ........ 28
   3.3 Square-wave Chopping ................................ 31
   3.4 Chopping with Orthogonal Spreading Codes ........ 34
   3.5 Chopping in Specific Multiplier Applications ...... 37
      3.5.1 DC Multiplier .................................... 38
      3.5.2 Variable-Gain Amplifier ......................... 38
      3.5.3 Direct-conversion Mixer ......................... 39

4 Limits on Performance 41
   4.1 DC Content in Chopping Waveforms ................. 41
   4.2 Charge Injection Spikes ................................ 42
   4.3 Parasitic Coupling between Input Ports .......... 45
4.4 Thermocouple Effects ........................................... 45
4.5 Layout Issues .................................................... 46

5 Nested Chopper Stabilization in Multipliers ............... 47
5.1 Chopping Frequency Limitations ................................. 47
5.2 Nested Chopping Technique .................................... 48

6 Prototype Multiplier IC ............................................ 51
6.1 System Overview ................................................... 51
6.2 Circuit Details .................................................... 53
   6.2.1 Multiplier Core ............................................. 53
   6.2.2 Unity-Gain Buffer ......................................... 54
   6.2.3 Differential Chopper ....................................... 55
   6.2.4 Chopping Waveform Generation Logic ..................... 55
   6.2.5 Input Selection Circuitry .................................. 57
   6.2.6 Output Polarity Switch ................................. 59
6.3 Measurement Results .............................................. 60
   6.3.1 DC Multiplier ............................................... 60
   6.3.2 Squarer ....................................................... 64
   6.3.3 Variable Gain Amplifier ................................... 64
   6.3.4 Direct-conversion Mixer .................................... 67
6.3.5 Filtering Design Considerations .............................. 70

7 Chopper Stabilization in RF Mixers ............................. 71
7.1 Problems with the Direct-conversion Architecture ............ 72
   7.1.1 DC Offset ....................................................... 72
   7.1.2 Even-order Distortion ....................................... 72
   7.1.3 Flicker Noise ............................................... 73
7.2 Principle of Chopper-Stabilized Mixers ......................... 74
   7.2.1 Simplified Chopping Architecture ....................... 74
   7.2.2 2nd-order Intermodulation Distortion .................... 77
7.2.3 Pseudorandom Noise Chopping .................................. 79
7.3 Nested Chopper Stabilization in Mixers ........................ 79

8 Prototype RF Mixer IC ............................................. 81
  8.1 System Overview ............................................. 81
  8.2 Circuit Details ................................................ 84
    8.2.1 Mixer Core ............................................. 84
    8.2.2 Differential Chopper .................................... 84
    8.2.3 Chopping Waveform Generation Logic .................... 86
  8.3 Measurement Results ......................................... 86

9 Conclusion ......................................................... 89
  9.1 Future Work .................................................. 90

A Experimental Setup .............................................. 91
  A.1 Prototype Multiplier Test Setup .............................. 91
    A.1.1 Input Stages ............................................. 91
    A.1.2 Output Stage ............................................ 93
  A.2 Prototype RF Mixer Test Setup ............................... 94
    A.2.1 Input Stages ............................................. 94
    A.2.2 Output Stage ............................................ 96
List of Figures

2-1 Multiplier offset current cancellation by laser-trim of R1 and R2 [1]........................................ 22
2-2 Circuit schematic of a floating-gate PMOS differential pair [2].................................................. 23
2-3 Block diagram of nonlinear offset-compensated multiplier [3]................................................... 24
2-4 Block diagram of offset cancellation scheme using digital integrator and DAC in feedback [4].......................... 25

3-1 Chopper stabilization in amplifiers............................................................... 28
3-2 Chopper stabilization in amplifiers using pseudorandom noise (PN) modulation........................................ 29
3-3 Three offset model for a general multiplier......................................................... 30
3-4 System block diagram for chopper-stabilized multiplier............................................ 31
3-5 Time-domain waveforms illustrating chopper stabilization in multipliers using square-wave modulation................................................................. 33
3-6 Frequency-domain representation of chopper stabilization in multipliers using square-wave modulation................................................................. 34
3-7 Time-domain waveforms illustrating chopper stabilization in multipliers using orthogonal spreading codes................................................................. 36
3-8 Frequency-domain representation of chopper stabilization in multipliers using orthogonal spreading codes................................................................. 37
3-9 Simplified chopping architecture for multipliers used as VGAs or direct-conversion mixers................................................................. 39

4-1 Residual offset due to charge injection spikes in a chopper stabilized amplifier................................................................. 43
4-2 Residual offset due to charge injection spikes in a chopper stabilized multiplier under three different input voltage conditions. ............. 44

5-1 Nested chopper stabilization in analog multipliers. ......................... 49

6-1 Block diagram of prototype chopper-stabilized analog multiplier. .... 52
6-2 Die photo of the prototype chopper stabilized analog multiplier in the National 0.18μm CMOS process. .......................... 53
6-3 Circuit schematic of multiplier core. .................................................. 54
6-4 Fully differential, unity-gain buffer. .................................................. 55
6-5 Circuit schematic of the single-ended op-amp used in the unity-gain buffer. .......................................................... 56
6-6 Circuit schematic of the current mirrors which provide the bias current for the two op-amps used in the unity-gain buffer. ............... 56
6-7 Circuit schematic of the differential chopper. .................................. 57
6-8 Block diagram of chopping waveform generation logic circuitry. ....... 58
6-9 Block diagram of input selection logic circuitry. ............................. 59
6-10 Measured DC voltage transfer characteristics of the multiplier. (a) Without chopper stabilization. (b) With square wave chopping at a down-chopping frequency of 10kHz. ........................................... 62
6-11 Output spectrum of DC multiplier with square wave chopping at a down-chopping frequency of 10kHz and 9-bit PN chopping spread over 100kHz. ................................................................. 63
6-12 Measured plot of square-law transfer curve. .................................... 65
6-13 Measured output spectrum of analog squarer with a 50kHz input sine wave. ................................................................. 65
6-14 Measured output spectrum of variable gain amplifier with a 50kHz input sine wave. ......................................................... 66
6-15 Measured output spectrum of variable gain amplifier with a 50kHz input sine wave, showing improvement in 1/f noise. ............... 67
6-16 Measured output spectrum of variable gain amplifier set at zero gain with a 50kHz input sine wave. ............................................. 68
6-17 Measured output spectrum of direct-conversion mixer showing base-band output signal. ............................................. 69
6-18 Measured output spectrum of direct-conversion mixer showing undesired spectral components modulated to chopping frequencies. .... 69
7-1 Effects of even-order distortion on interferers [5]. .................. 73
7-2 System block diagram for the chopper-stabilized mixer. ............ 75
7-3 System block diagram for the chopper-stabilized mixer, where both choppers are driven by the same chopping waveform. ............ 77
7-4 Nested chopper-stabilized mixer. .................................... 80
8-1 Block diagram of prototype chopper-stabilized RF mixer. .......... 82
8-2 Die photo of the prototype chopper-stabilized mixer in the National 0.18μm CMOS process. ............................................. 83
8-3 Circuit schematic of the mixer core. ................................... 85
8-4 Differential choppers used in the prototype RF mixer IC. .......... 85
8-5 Block diagram of chopping waveform generation logic circuitry for the prototype mixer. ............................................. 86
A-1 Package bonding diagram for the prototype IC. .................... 92
A-2 Test setup for the prototype multiplier. ................................ 92
A-3 Input stages for multiplier testing. .................................... 93
A-4 Instrumentation amplifier, used to perform the differential to single-ended conversion. ............................................. 94
A-5 Test setup for the prototype RF mixer. ................................ 95
List of Tables

6.1 Offset Performance Summary for DC Analog Multiplier. ............... 63
6.2 Offset Comparison for Various Multiplier Offset Cancellation Techniques. 64
8.1 Measured Mixer Performance Summary . ............................. 87
Chapter 1

Introduction

1.1 Motivation

Analog multipliers are an important building block in many electronic systems which require analog signal processing. Examples include phase alignment systems [6], neural networks [7], and sensor systems [3]. A persistent problem with analog multipliers is DC offset, which limits the precision of these systems. For example, several commercial accelerometers and sensitive instrumentation systems employ lock-in techniques to detect faint signals, in which analog multipliers are an essential building block for performing the demodulation necessary to extract the input signal. The offset in the multiplier can decrease the multiplier’s gain, degrade its noise performance and minimum detectable signal, and increase the nonlinearity and distortion introduced by the multiplier in the demodulation process, all of which degrade the sensitivity of the sensing system [3].

Some strategies to reduce the DC offset have been proposed in [3, 4, 2]. A trimming method is used in [2], in which floating gate transistors are used for the input transistors of the multiplier, and charge is injected onto the floating gates until the offset is cancelled out. Nonlinear feedback is used to suppress the offset in [3], in which an additional multiplier is used to extract the DC content in the output of the main multiplier and subtract it from the input signal, removing any offset in the process. Feedback is also used in [4], but a digital integrator is used to extract the
DC content instead of another multiplier. The output of the integrator is converted to an analog signal with a digital-to-analog converter (DAC), which feeds an error compensating signal back to the input. While all of these methods are effective in reducing the offset of the multiplier, each of these methods suffers from one of two drawbacks: (1) it requires a calibration step during which the multiplier cannot be used and which must be periodically repeated to eliminate drift; or (2) it only works for AC signals, removing not only offset but also any DC content in the output, and so cannot be applied to DC multiplication.

With an important modification, chopper stabilization, a technique long used to achieve low-offset amplification, can be applied to multipliers to continuously reject DC offset without sacrificing DC performance. Chopping has been applied to specific types of multipliers before for various applications. In [8], chopping is used to reduce the 2nd-order intermodulation distortion and $1/f$ noise of a down-conversion mixer. In [1], a similar technique is used to reduce the temperature-dependent offset of a squaring circuit used for power measurement. Chopping is also applied in [9] to reduce the offset of the demodulator (i.e., mixer) in a temperature-to-frequency converter. What each of these applications lack, however, is a chopping architecture suitable for general-purpose multiplication. Such a chopping architecture was first reported in [6] to reduce the offset of a DC multiplier. This work considered only the simplest case of chopping waveforms, which are two quadrature square waves. Chopper-stabilized multipliers were further characterized in [10], where the theory was generalized to include pseudorandom noise (PN) chopping waveforms.

In this thesis, the theory of chopper stabilization for general-purpose multipliers is described in detail, including both square-wave and PN chopping. Measured results for a chopper-stabilized DC multiplier using orthogonal spreading codes are also presented for the first time. In addition, we further generalize the theory of chopper-stabilized multipliers to include nested chopping. Nested chopping was used to achieve benchmark offset performance for instrumentation amplifiers in [11]. In our work, we apply nested chopping to analog multipliers to reduce the DC offset even further than before. Finally, we apply chopper stabilization to a multiplier
configured as a squarer, variable-gain amplifier (VGA), and direct-conversion mixer, demonstrating the effectiveness of the technique for AC multiplication as well as DC multiplication. Our AC measurements show that chopping is not only effective in removing DC offset, but also 1/f noise and 2nd-order harmonic distortion.

The limits on the offset performance of a chopper-stabilized multiplier are also examined. In particular, we present a detailed analysis of the residual offset due to the charge injection mismatch in the differential input choppers, which is the main cause of residual offset in chopped amplifiers. Our analysis of this source of offset in chopped multipliers shows that the residual offset depends heavily on the inputs applied to the multiplier, and that when both input voltages are zero, no residual offset results. Other possible sources of residual offset are discussed, including DC content in the chopping waveforms, parasitic thermocouples, nonzero port-to-port coupling, and asymmetrical layout of bond-pads, choppers, and wires.

Chopper stabilization can also be applied to RF direct-conversion mixers (a special type of analog multiplier) for improved receiver sensitivity. This technique was first applied to an RF direct-conversion mixer in [8]. Two well-known problems with the direct-conversion receiver architecture are (1) 2nd-order intermodulation (IM2) distortion which introduces undesirable spectral components at base-band; and (2) 1/f noise [5]. Several techniques have been proposed to solve these two problems (see for example [12, 13]), but nearly all of them involve the use of large inductors which consume a great deal of area. This work aims to demonstrate the effectiveness of chopper stabilization in solving these problems without the need for bulky inductors, reducing both area and cost.

1.2 Organization

The outline of this thesis is as follows. In chapter 2, we briefly review current techniques used to reduce the offset in analog multipliers. In chapter 3, we explain the chopper stabilization technique for analog multipliers using both square wave waveforms and pseudorandom noise sequences. Chapter 4 describes the limits on the
performance of the chopper stabilization technique, and in chapter 5, we introduce the nested chopper stabilization technique as a method to overcome some of these limitations. An illustrative CMOS prototype of a chopper-stabilized multiplier in a 0.18\textmu m process is presented in chapter 6, along with measured results. In chapter 7, we discuss how chopper stabilization can be applied to an RF downconversion mixer (a specific type of analog multiplier) to improve IM2 distortion, offset, and noise performance. Chapter 8 presents a CMOS prototype of a chopper-stabilized RF mixer along with the measured results. Finally, conclusions are drawn in chapter 9.
Chapter 2

Multiplier Offset Cancellation Techniques

Several methods have been proposed to reduce the DC offset in analog multipliers. The most straightforward method to reduce offset is to use large-geometry devices that are well-matched, as described in [14, 15]. However, while large device sizes mitigate the effects of random process-induced mismatches, they also add large parasitic capacitances which impose low bandwidth and long settling time limits on the system [16], as well consume a great deal of area. Careful layout techniques, such as common-centroid layout and insertion of dummy devices, can also be used to reduce mismatch leading to offset. While it is good practice in general to follow these techniques, the offset reduction that can be achieved through careful layout is typically limited to the millivolt range or larger in CMOS technologies [17]. In order to reduce the offset further, some specialized circuit technique must be applied.

2.1 Trimming

One method of offset cancellation is trimming, a post-fabrication circuit adjustment aimed at correcting the process-induced offsets of various circuits components [18]. Typically, one or more strategically placed resistors are tuned to offset the mismatch errors of two or more devices. An example of this is depicted in Figure 2-1 for a
Figure 2-1: Multiplier offset current cancellation by laser-trim of R1 and R2 [1].

Gilbert multiplier cell, in which the resistors R1 and R2 are laser-trimmed to create an intentional mismatch to compensate for the offset current of the multiplier [1]. The resistance can be varied by: (1) fabricating a number of binary weighted resistors and open- and/or short-circuiting them with on-chip fuses or switches, or (2) reshaping and therefore resizing a resistor with a laser. Another trimming method makes use of floating gate transistors for the input transistors of the multiplier [2]. Figure 2-2 shows a schematic of a PMOS differential pair which uses floating gate devices. Charge is injected onto the floating gate until the offset is cancelled out.

The major disadvantage of most trimming methods is cost. Special processing techniques and/or devices are often required which are not available in standard CMOS processes (e.g., floating-gate devices). Furthermore, a test infrastructure is generally required to tune the trimmed devices to cancel out the offset, further increasing manufacturing time and equipment costs. Another disadvantage of trimming methods is that they generally do not eliminate drift or $1/f$ noise, since the trimming is typically performed only once at a specified temperature. Even in cases where
the calibration step can be repeated (e.g., if the trimming is done on-chip using a bank of resistors or transistors, each of which can be switched in with MOS switches controlled by digital configuration bits), the circuit usually cannot be used while the calibration is being performed, and so these methods cannot be used if continuous multiplication is required.

2.2 Nonlinear Multiplicative Feedback

Another method of offset cancellation uses an additional multiplier placed in feedback with the main multiplier to suppress the offset [3]. The principle of this nonlinear feedback technique is shown in Figure 2-3. An amplifier cannot be used in the feedback path because the sign of the multiplier gain depends on two inputs, and so both positive and negative feedback would be possible. Thus a multiplier is placed in the feedback loop in such a way as to ensure that negative feedback is always in effect. The feedback multiplier extracts the DC content in the output of the main multiplier and subtracts it from the input signal, removing any offset in the process. While this method is extremely effective at canceling out the offset of the multiplier, it cannot be used for DC multiplication since all DC content in the multiplier output is lost.
2.3 Digital Integrator in Feedback

This offset cancellation technique also makes use of feedback, but uses a digital integrator and a DAC in the feedback path instead of another multiplier, as shown in Figure 2-4 [4]. The digital integrator computes the offset while the DAC feeds an error compensating signal back to the input. This technique can be used under two configurations. It can be run in the foreground as a calibration step where the offset information is extracted while the multiplier is not in use, in which case it must be periodically repeated to eliminate drift. If continuous multiplication is required, this technique can instead to be run continuously in the background, in which case all DC content will be removed from the output signal and thus cannot be used for DC multiplication.
Figure 2-4: Block diagram of offset cancellation scheme using digital integrator and DAC in feedback [4].
Chapter 3

Chopper Stabilization in Multipliers

Chopper stabilization has long been successfully applied to amplifiers to remove not only DC offset, but also other undesirable low-frequency spectral components present at the amplifier output, including drift and $1/f$ noise. For two recent examples see [11] and [19]. In this chapter we will review chopper stabilization in amplifiers and then explain its application to analog multipliers.

3.1 Principle of Chopper-Stabilized Amplifiers

The principle of chopper stabilization for amplifiers is shown in Figure 3-1. The input signal $V_{in}$ is modulated by a waveform $c_0$, amplified, and then modulated back to baseband using the same waveform $c_0$. The offset $\delta_o$ is only modulated once, thus separating the desired signal from the offset in the frequency domain. The amplifier’s $1/f$ noise is also separated from the desired signal, since it appears at the output of the amplifier along with $\delta_o$.\footnote{In fact, $1/f$ noise can be thought of as nothing more than a slow time-varying offset.} To achieve full separation of the desired signal from the offset and $1/f$ noise, the signal energy of $c_0$ must be distributed over frequencies high enough to be filtered out. The simplest choice for $c_0$ is a periodic square wave which switches between -1 and +1, in which case the modulator can be easily realized using
MOS switches. With this choice the modulation process is called chopping.

Chopping results in strong tones in the output spectrum of the amplifier because it modulates the offset to the chopping frequency and its odd harmonics. If these strong tones are unacceptable, even after filtering, another possibility for $c_0$ is a pseudorandom noise (PN) sequence which randomly switches between -1 and +1. The principle of PN chopping for amplifiers is shown in Figure 3-2. This type of modulation spreads the offset and $1/f$ noise over a wide frequency range rather than concentrating them at specific frequency locations, thus avoiding strong tones in the output which may simplify the filtering process. The drawback is that the noise floor at the output is raised, reducing the signal-to-noise ratio (SNR). PN sequences can be easily generated using linear feedback shift registers (LFSRs) [20].

### 3.2 Principle of Chopper-Stabilized Multipliers

Chopper stabilization for multipliers works in much the same way as amplifiers, but is complicated by the fact that there are two inputs instead of one. As such, a complete description of a multiplier’s offset behavior requires three separate offsets $\delta_x$, $\delta_y$, and $\delta_o$, one for each of the inputs and one for the output [10]. Figure 3-3 shows the three offset model for a general multiplier, from which we can write the output of the...
Figure 3-2: Chopper stabilization in amplifiers using pseudorandom noise (PN) modulation.
multiplier as the following:

\[
V_{\text{out}} = k (V_x + \delta_x) (V_y + \delta_y) + \delta_o
= kV_x V_y + kV_x \delta_y + kV_y \delta_x + (k\delta_x \delta_y + \delta_o)
\]  

(3.1)

where \(k\) is the constant of multiplication (we assume that the multiplier is operating in its linear region and therefore neglect any higher-order nonlinearities in this analysis). \(kV_x V_y\) is the desired product, but the other terms in equation 3.1 are undesired products resulting from the three different offsets of the multiplier. However, just as in the case of amplifiers, the effect of these offsets can be suppressed by applying chopper stabilization.

Figure 3-4 shows a block diagram of a chopper-stabilized multiplier. To separate the offsets from the desired product in the frequency domain, a chopper is placed before each multiplier input and after the multiplier output, each modulated by a different waveform. Referring to Figure 3-4, the output of the chopped multiplier is given by the following equation:

\[
V_{\text{out}} = [(kV_x c_x + \delta_x)(V_y c_y + \delta_y) + \delta_o] c_z
= kV_x V_y c_x c_y c_z + kV_x \delta_y c_x c_z + kV_y \delta_x c_y c_z + (k\delta_x \delta_y + \delta_o) c_z
\]

(3.2)

where \(c_x\), \(c_y\), and \(c_z\) are the modulation waveforms for each chopper. We see from this equation that in order to recover the desired product \(kV_x V_y\) at baseband, the product
Figure 3-4: System block diagram for chopper-stabilized multiplier.

$c_xc yc_z$ must equal 1. Furthermore, to modulate the offsets away from baseband, the signal energy of $c_x c_z$, $y c_z$, and $z$ must be distributed over frequencies high enough to be filtered out. As in the amplifier case, both square-waves and PN sequences can be used to meet these criteria. The details of both of these methods will be described next.

It should also be noted that the frequencies of the chopping waveforms set a minimum bandwidth requirement on the analog multiplier core, since this core must be able to multiply the two signals $V_x c_x$ and $V_y c_y$ to generate the product $V_x V_y c_x c_y$ for correct operation. This reduces the multiplier's useful bandwidth, since the signal bandwidth should be made lower than the chopping frequencies to effectively separate the multiplier offsets from the desired signal. This bandwidth requirement must be taken into account when designing the multiplier and in choosing the frequencies of the chopping waveforms.

### 3.3 Square-wave Chopping

To separate the desired product from the multiplier offsets using square-wave modulation, it is sufficient to use two quadrature square waves for the two input chopping waveforms $c_x$ and $c_y$ (each of which switch between -1 and +1), and then make the output chopping waveform $c_z = c_x c_y$ [10]. This results in an output chopping waveform which is a square wave at twice the frequency of the two input chopping waveforms.
waveforms. With this choice the following identities result:

\[ c_i c_i = 1 \quad (3.3a) \]

\[ c_x c_z = c_y \quad (3.3b) \]

\[ c_y c_z = c_x \quad (3.3c) \]

Plugging these into equation 3.2, we can write the output of the chopped multiplier as

\[ V_{out} = kV_x V_y + kV_x \delta_y c_y + kV_y \delta_x c_x + (k \delta_x \delta_y + \delta_o) c_z \quad (3.4) \]

From this equation, we see that the desired product is recovered at baseband while all the offsets are modulated by a square wave, and are therefore removable using a low-pass filter. The multiplier’s 1/f noise is also separated from the desired signal, since it appears at the output of the multiplier along with \( \delta_o \). Figure 3-5 illustrates the principle of chopper stabilization in multipliers using square-wave modulation in the time domain. Figure 3-6 illustrates the principle in the frequency domain (frequency components at odd harmonics of the chopping waveforms are omitted for clarity).

Using the identities of equation 3.3, we can now see why chopping is not only effective at reducing offset and 1/f noise, but also 2nd-order distortion. To see why, we use the following equation to model the output of a general multiplier, which takes into account the multiplier’s nonlinearities:

\[ V_{out} = \sum_{i=0}^{\infty} \sum_{j=0}^{\infty} (k_{ij} \cdot V_x^i \cdot V_y^j) \quad (3.5) \]

Using this model, \( k_{00} \) corresponds to the output offset \( \delta_o \), \( k_{10} \) and \( k_{01} \) correspond to the input offsets \( \delta_x \) and \( \delta_y \), respectively, and \( k_{11} \) is the linear gain of the multiplier. The 2nd-order distortion terms are

\[ V_{HD2} = k_{02} V_y^2 + k_{20} V_x^2 + k_{12} V_x V_y^2 + k_{21} V_x^2 V_y + k_{22} V_x^2 V_y^2 \quad (3.6) \]

When chopper stabilization is applied, we replace \( V_x \) with \( V_x c_x \) and \( V_y \) with \( V_y c_y \),
Figure 3-5: Time-domain waveforms illustrating chopper stabilization in multipliers using square-wave modulation.
multiply the result by $c_z$, and apply the identities of equation 3.3 to obtain the following:

$$V_{HD2,\text{chop}} = k_{02}V_x^2c_z^2 + k_{20}V_x^2c_z^2 + k_{12}V_xV_y c_z^2c_y c_z + k_{21}V_xV_y^2c_z^2c_y c_z + k_{22}V_x^2V_y^2c_z^2c_y c_z + k_{22}V_x^2V_y^2c_z^2c_y c_z$$

(3.7)

$$= k_{02}V_x^2c_z + k_{20}V_x^2c_z + k_{12}V_xV_y c_z^2c_y c_z + k_{21}V_xV_y^2c_z^2c_y c_z + k_{22}V_x^2V_y^2c_z^2c_y c_z$$

(3.8)

From equation 3.8, we see that all 2nd-order distortion terms are modulated by one of the chopping waveforms, and so they can be filtered out along with the offset and $1/f$ noise. In fact, it can easily be shown that chopper stabilization modulates all even-order distortion terms in this way.

### 3.4 Chopping with Orthogonal Spreading Codes

PN sequences can also be used for the modulation waveforms in chopped multipliers if it is desirable to avoid strong tones in the multiplier’s output spectrum. In this case, the two input chopping waveforms should be orthogonal spreading codes such that
time average of their product $\langle c_x c_y \rangle$ is zero, and the output chopping waveform should be set to $c_z = c_x c_y$ [10]. Note that this is a generalization of square wave chopping described in the previous section, and the same identities given in equation 3.3 apply. The difference is that now each of the multiplier offsets are modulated by a PN sequence, spreading the offsets over a wide frequency range. Figure 3-7 illustrates the principle of chopper stabilization in multipliers using orthogonal spreading codes in the time domain. Figure 3-8 illustrates the principle in the frequency domain.

The most common way of implementing PN sequences is to use LFSRs [20]. A maximal length sequence, or M-sequence, from a properly designed $n$-stage LFSR will produce a sequence of length $2^n - 1$, with $2^{n-1}$ occurrences of +1 and $2^{n-1} - 1$ occurrences of -1. The average value of this waveform is therefore $1/(2^n - 1)$. Since each of the multiplier offsets is modulated by one of these M-sequences, the offset improvement is limited by this factor. Note that this is not the case for square waves, which have no DC content and thus translate all of the offset away from DC. However, the offset performance using PN chopping can be improved simply by increasing the length of the M-sequences. Another drawback of PN chopping is that the noise floor at the output is raised, reducing the SNR. The amount of noise added in the signal bandwidth can be reduced by increasing the frequency range over which the undesired products are spread, which is set by the sampling frequency at which the PN sequence is clocked. However, this also increases the minimum required bandwidth of the multiplier core, since the core must be able to multiply the two signals $V_x c_x$ and $V_y c_y$ to generate the product $V_x V_y c_x c_y$ for correct operation of the chopping technique.

Since $c_z = c_x c_y$, it is also important that the correlation between the two input PN sequences $\langle c_x c_y \rangle$ be as small as possible, since the last offset term in equation 3.2, $\delta_o$, is modulated by this factor, along with the $1/f$ noise. Using Gold codes for $c_x$ and $c_y$, which are easily generated from M-sequences, ensures that this correlation is minimized [20].
Figure 3-7: Time-domain waveforms illustrating chopper stabilization in multipliers using orthogonal spreading codes.
3.5 Chopping in Specific Multiplier Applications

The chopper stabilization technique described above can be applied to any differential multiplier topology to separate the multiplier’s inherent offsets from the desired product. However, depending on the way the multiplier is used, it may not be necessary to modulate all of the undesired products shown in equation 3.1 by the chopping waveforms. For example, if the multiplier is used as an RF down-conversion mixer, then both inputs $V_x$ and $V_y$ are high-frequency AC signals. By equation 3.1, each of the input offsets will be modulated to one of these frequencies, and so they can be easily filtered out without modulating them by a chopping waveform. Chopping is still desirable to remove the output offset, $1/f$ noise, and 2nd-order harmonic distortion, but since the input offsets are not a problem in this case, the chopping architecture may be greatly simplified. In this section, we will discuss three different multiplier applications—DC multiplier, variable-gain amplifier (VGA), and direct-conversion mixer—and how the chopping architecture described above may be simplified depending on how the multiplier is used.
3.5.1 DC Multiplier

In the case of DC multiplication, both of the multiplier inputs are DC signals, and so the desired output is also a DC signal. In this case, all of the undesired products in equation 3.1 \((kV_x\delta_y, kV_y\delta_x, k\delta_x\delta_y + \delta_o)\) will corrupt the desired product \(kV_xV_y\), and so the full chopping architecture described above should be applied to modulate the offsets to the chopping frequencies where they can be filtered out.

3.5.2 Variable-Gain Amplifier

When a multiplier is used as a VGA, one of the multiplier inputs is set to a DC signal which determines the gain of the amplifier, while the other input is the AC signal to be amplified. In this case, the VGA is very similar to a regular amplifier, and so the same chopping architecture used for amplifiers may be applied to the VGA, instead of the standard chopping architecture used for a general multiplier. If we let \(V_y = V_{gain}\) be the DC signal and \(V_x = V_{in}\) be the AC signal, then we can set \(c_y = 1\) and \(c_x = c_z = c_0\) to simplify the general multiplier chopping architecture to the standard amplifier chopping architecture, as shown in Figure 3-9. Plugging these into equation 3.4, we can write the chopper stabilized VGA output as

\[
V_{out} = kV_{gain}V_{in} + k\delta_yV_{in} + [k\delta_x(V_{gain} + \delta_y) + \delta_o]c_0 \\
= k(V_{gain} + \delta_y)V_{in} + [k\delta_x(V_{gain} + \delta_y) + \delta_o]c_0
\]  

(3.9)

From this equation, we see that most of the undesired products generated by the multiplier offsets are modulated by the chopping waveform \(c_0\), separating them from the desired output \(kV_{gain}V_{in}\) where they can be filtered out (note that the 1/f noise is also modulated by \(c_0\), since it appears at the multiplier output along with the output offset \(\delta_o\)). The only term that cannot be separated from the desired output is the term \(k\delta_yV_{in}\), which corresponds to an offset in the gain setting voltage \(V_{gain}\). For some applications, an offset in the VGA gain may not matter (for example, if the VGA gain is set by a feedback loop), and so simplifying the chopping architecture
Figure 3-9: Simplified chopping architecture for multipliers used as VGAs or direct-conversion mixers.

in this way is acceptable. The advantage gained is that only one chopping waveform needs to be generated instead of the three required for the general multiplier case. However, if the offset in the VGA gain is unacceptable, the full multiplier chopping architecture should be applied.

3.5.3 Direct-conversion Mixer

When a multiplier is used as a direct-conversion mixer, the multiplier inputs are both high-frequency AC signals, such that the desired output signal is at the difference of the two input frequencies, which is typically much lower than the either of the two input frequencies. Thus, the undesired products $kV_x\delta_y$ and $kV_y\delta_x$ in equation 3.1 will be located at much high frequencies than the frequency of the desired product $kV_xV_y$, so that they can be easily filtered out without modulating them by a chopping waveform. However, to remove the output offset $k\delta_x\delta_y + \delta_o$, the $1/f$ noise, and the 2nd-order harmonic distortion, some kind of chopping must still be applied. In this case we can simplify the general multiplier chopping architecture by setting $c_y = 1$ and $c_x = c_z = c_0$, just as in the case of the VGA. Plugging these into equation 3.4,
we can write the chopper stabilized mixer output as

\[ V_{out} = kV_x V_y + k\delta_y V_x + k\delta_x c_0 V_y + (k\delta_x \delta_y + \delta_o) c_0 \]  \hspace{1cm} (3.10)

From this equation, we see that the undesired products are located at \( V_x, c_0 V_y, \) and \( c_0. \) Since \( V_x \) and \( V_y \) have frequencies much higher than the desired product \( kV_x V_y, \) the term at \( V_x \) can be easily filtered out. The chopping waveform \( c_0 \) is designed to be located at frequencies much higher than the signal bandwidth, so the term at \( c_0 \) can also be filtered out. The term at \( c_0 V_y \) can be filtered out as long as the frequency difference between \( c_0 \) and \( V_y \) is large enough to effectively separate this term from the desired product, which is located at the difference in frequency between \( V_x \) and \( V_y. \) Thus, the chopping architecture for a direct-conversion mixer can be simplified from the general multiplier case, so that only one chopping waveform needs to be generated instead of three.

The specific application of chopper stabilization to RF direct-conversion mixers will be discussed more thoroughly in chapter 7.
Chapter 4

Limits on Performance

No technique is ever perfect and so some residual offset will always remain after chopper stabilization is applied. In this chapter we describe the various sources of residual offset which limit the offset performance of chopped multipliers.

4.1 DC Content in Chopping Waveforms

The most direct source of residual offset in chopped multipliers is due to DC content in the chopping waveforms. As was shown in equation 3.2, each of the multiplier offsets is modulated by one of $c_xc_z$, $c_yc_z$, and $c_z$, and so if any of these terms have DC content, a fraction of the multiplier offsets will remain at DC. The $1/f$ noise and 2nd-order harmonic distortion will leak through to the output as well. In this respect, square wave chopping is seen to be nearly ideal when compared to PN chopping, as described in Section 3.4. However, producing a truly 50% duty cycle square wave is usually not possible. For example, a perfect square wave at the input of a CMOS inverter will not result in a perfect square wave at the output due to the asymmetry between the driving strength of the PMOS and NMOS devices. Thus most realizable square waves will have a small DC component which will cause some offset to leak through to the output.

Clock skew among the chopping waveforms will also cause a residual offset. In the case of square wave chopping, since the output chopping waveform is $c_z = c_xc_y$, any
skew between $c_x$ and $c_y$ will result in a DC component in $c_z$, causing residual offset due to the last offset term in equation 3.2. Skew between the input and output chopping waveforms will have a similar effect, since the multiplier input offsets are modulated by $c_x c_z$ and $c_y c_z$. Furthermore, skew among $c_x$, $c_y$, and $c_z$ will cause distortion in the multiplier since the desired product is modulated by $c_x c_y c_z$.

To reduce the DC content in the chopping waveforms due to mismatched rise/fall times and skewed clocks, the chopping frequency should be made as low as possible so that the average value of the mismatch or skew integrated over one clock period is minimized.

### 4.2 Charge Injection Spikes

A more indirect source of residual offset occurs due to the spikes which appear at the input choppers. This source of offset is described in [11] as the main source of residual offset in chopped amplifiers and is illustrated in Figure 4-1. Given a square wave chopping waveform, voltage spikes appear at the output of the input chopper due to the charge injection mismatch of the switches which perform the chopping operation. These spikes are amplified and then multiplied by the same chopping waveform, rectifying the spikes at the output and causing a DC offset. It can be shown that the residual offset is given by the following equation [21]:

$$ V_{os,res} = 2 f_{ch} V_{spike} \tau \quad (4.1) $$

where $f_{ch}$ is the chopping frequency, $V_{spike}$ is the height of the voltage spikes, and $\tau$ is the time constant of the spikes. From this equation, we can see that there are three main options to reduce the residual offset due to charge injection spikes: 1) lower the chopping frequency; 2) lower the input resistance to lower $\tau$; or 3) lower the charge injection [11].

Charge injection spikes also occur in chopped multipliers, but since there are two inputs there are two sets of spikes, one corresponding to each of the input chopping
waveforms $c_x$ and $c_y$. In our analysis let us assume that quadrature square waves are used for $c_x$ and $c_y$. The residual offset due to charge injection spikes will depend on the input voltages applied to the multiplier. Figure 4-2 illustrates the resulting offset for three different cases of input voltages: 1) $V_x = V_y = 0$; 2) $V_x = 0, V_y \neq 0$; and 3) $V_x \neq 0, V_y \neq 0$. The spikes due to the $c_x$ and $c_y$ waveforms are denoted by $S_x$ and $S_y$, respectively. For the first case in which both inputs are zeroed out, each set of spikes will be multiplied by one of the input offsets and then multiplied by the output chopping waveform, resulting in the terms $S_x \delta_x c_x$ and $S_y \delta_x c_x$ at the multiplier output. Since $c_x = c_x c_y$ is a square wave at twice the frequency of $c_x$ and $c_y$, we see that the spikes are not rectified, and thus no residual offset results in this case. However, in the second case in which $V_y$ is set to a nonzero voltage, an additional term $S_x V_y c_y c_x$ appears at the multiplier output. Using the identity given in equation 3.3, we see that in this case the x-input spikes will be rectified at the output, resulting in a residual offset given by equation 4.1. In the third case, where both input voltages are set to some nonzero voltage, both sets of spikes will be rectified at the output, and total residual offset will be the sum of the two individual components.

In conclusion, the residual offset due to charge injection spikes in a chopped multiplier will depend heavily on the input voltages applied to it, and when both inputs are zeroed out, no residual offset results. This is in contrast with chopped amplifiers,
Figure 4-2: Residual offset due to charge injection spikes in a chopper stabilized multiplier under three different input voltage conditions.
in which the residual offset due to charge injection spikes is unavoidable regardless of the input voltage applied. Note that this residual offset is an additional offset added to the multiplier output which is not proportional to the multiplier’s inherent offsets. To reduce this source of residual offset, the designer should lower the chopping frequency as much as possible (therefore lowering the DC content of the rectified charge injection spikes) and minimize the charge injection of the chopping switches by using small transistors that are well matched.

4.3 Parasitic Coupling between Input Ports

An additional source of offset that occurs in any kind of multiplier system is caused by the parasitic coupling between the two input ports of a multiplier. If either input to the multiplier is an AC sinusoidal signal, then a fraction of that signal will couple to the other input due to nonzero port-to-port isolation. The multiplier will then effectively square the AC signal, resulting in a DC offset and a tone at twice the signal frequency. Because the signals appear at the inputs of the multiplier, the chopping technique will not remove these undesirable spectral components. To minimize this source of residual offset, the port-to-port coupling between the two multiplier inputs should be minimized.

4.4 Thermocouple Effects

Another possible source of residual offset is parasitic thermocouples, which exist in normal circuit wiring wherever two dissimilar metals are joined and temperature gradient exists across them. For example, thermocouple junctions between copper traces of a circuit board and Kovar package pins can create voltage errors as large as 35μV/°C [22]. While this offset may seem small, it sets a practical lower limit on the measurable offset of a chopped multiplier system.
4.5 Layout Issues

The two main causes of residual offset in chopped multipliers, DC content in the chopping waveforms and charge injection spikes, both occur due to component mismatch. Thus careful layout is critical in achieving the lowest possible offset when the chopping technique is applied. Special care should be taken to ensure that the layout of choppers, amplifiers, wires, and bond pads are as symmetrical as possible to avoid mismatch leading to residual offset. In addition, the two multiplier input ports should be as isolated from each other as possible, to minimize parasitic coupling leading to self-mixing.
Chapter 5

Nested Chopper Stabilization in Multipliers

The previous chapter described the various limitations of the chopper stabilization technique in removing the offset from analog multipliers. In this chapter we introduce the nested chopping technique as a method to overcome some of these limitations.

5.1 Chopping Frequency Limitations

After chopper stabilization is applied, there will always be some residual offset at the output of the multiplier. Chapter 4 described the sources of this residual offset in detail. In that chapter it was shown that in the case of square wave chopping, the main sources of residual offset are directly proportional to the chopping frequency, just as in the case of chopped amplifiers [11]. However, there are practical limits on how low the chopping frequency can be. The chopping frequency should be higher than the signal bandwidth to separate the undesired spectral components from the desired signal, higher than the $1/f$ noise corner frequency to remove the $1/f$ noise, and also high enough to meet the design requirements of the low-pass filter used to remove the unwanted tones which are modulated to the chopping frequency and its odd harmonics.

There is also an upper limit to the chopping frequency. Since the multiplier core
must be able to multiply the two signals $V_x c_x$ and $V_y c_y$ to generate the product $V_x V_y c_x c_y$ for correct operation of the chopping technique, the chopping frequencies should be within the multiplier core’s bandwidth. As the chopping frequency increases, the filtering required at the output becomes easier, but the multiplier core bandwidth must also increase to allow it to perform the necessary multiplication. As multiplier bandwidth is generally proportional to power consumption, this creates a tradeoff between offset performance, filtering requirements, and power consumption when choosing the chopping frequency.

5.2 Nested Chopping Technique

Given the lower limits on the chopping frequency, we can reduce the residual offset of a chopped multiplier even further by applying an additional level of chopping, which is referred to as the nested-chopper technique [11]. The principle of nested chopper stabilization in multipliers is shown in Figure 5-1. The inner choppers greatly suppress the offsets $\delta_x$, $\delta_y$, and $\delta_o$ and the $1/f$ noise of the multiplier by modulating them to a high chopping frequency where the $1/f$ noise is fully separated from the desired signal and where they can be easily filtered out. The outer choppers then reduce any residual offsets of the inner-chopped multiplier system by modulating them to a lower chopping frequency. Since the residual offset is proportional to the chopping frequency, the offset performance is improved. Furthermore, since the residual offset of the inner-chopped multiplier system is much smaller than the multiplier’s inherent offsets, it is easier to meet the filtering requirements at the lower chopping frequency.

Referring to Figure 5-1, the output of the nested-chopped multiplier is given by
the following equation, where we have applied the identities of equation 3.3:

\[
V_{out} = [k [(V_x c_{x2} + \delta_{xx}) c_x + \delta_x] [(V_y c_{y2} + \delta_{yy}) c_y + \delta_y] + \delta_o] c_z + \delta_{or}] c_{z2} \\
= kV_x V_y + \\
kV_x \delta_y c_{y2} c_y + kV_y \delta_x c_{x2} c_x (k \delta_x \delta_y + \delta_o) c_{z2} c_z + \\
kV_x \delta_{yr} c_{y2} + kV_y \delta_{xr} c_{x2} + (k \delta_{xr} \delta_{yr} + \delta_{or}) c_{z2} + \\
k\delta_y \delta_{xr} c_{z2} c_y + k\delta_x \delta_{yr} c_{z2} c_x
\]

(5.1)

\(\delta_{xx}, \delta_{yy}, \) and \(\delta_{or}\) are the residual offsets of the inner-chopped multiplier system; \(c_{x2}, c_{y2},\) and \(c_{z2}\) are the chopping waveforms for the outer choppers; and the other terms are the same as those given in equation 3.2. The 1st line in equation 5.1 is the desired product, \(kV_x V_y\). The 2nd line gives the inherent offsets of the multiplier, which are modulated to the chopping frequencies of the inner choppers (assumed to be much higher than the chopping frequencies of the outer choppers). The 3rd line gives the residual offsets of the inner-chopped multiplier system, which are modulated to the chopping frequencies of the outer choppers. Although the outer chopping frequencies are much lower than the inner chopping frequencies, the residual offsets are also much
lower, making filtering at these frequencies easier. The last line in equation 5.1 gives
the offsets that result from multiplying the inherent offsets with the residual offsets,
which are modulated to the outer chopping frequencies. In our work we apply nested
chopping to an analog multiplier for the first time to demonstrate the effectiveness of
this technique.
Chapter 6

Prototype Multiplier IC

A prototype IC was fabricated in a 0.18μm CMOS process to experimentally evaluate the effectiveness of the different methods of chopper stabilization – square wave, orthogonal spreading codes, and nested chopping – in removing offset, $1/f$ noise, and 2nd-order harmonic distortion from a general purpose analog multiplier. This chapter describes the circuit details for each block in the system and presents our measured results.

6.1 System Overview

A block diagram of the chopper-stabilized multiplier prototype IC is shown in Figure 6-1. For the multiplier core, a four-quadrant $V_{gs}V_{ds}$ type multiplier as described in [23] was chosen for this work as it is widely implemented in CMOS processes. However, we emphasize that the chopper stabilization technique described in this paper can be applied to any differential analog multiplier topology. The multiplier core is followed by a fully differential, op-amp based unity-gain buffer, in order to drive the large off-chip capacitance. Two levels of chopping switches surround this multiplier core and buffer combination. In our prototype each level of chopping can be enabled or disabled by controlling the inputs to the chopping waveform generation logic circuitry. To measure the DC offset, we are able to short the differential inputs directly on-chip to an externally-provided bias voltage, thus avoiding any external
Figure 6-1: Block diagram of prototype chopper-stabilized analog multiplier.

offspects (e.g., thermocouple effects) at the multiplier inputs.

The chopping operation is implemented by four NMOS switches, which commutate the differential signals according to the pattern dictated by the chopping waveforms. Mathematically, the effect is to multiply the input signal by a signal that alternates between +1 and -1. To generate the square wave chopping waveforms, an externally supplied reference clock is divided using flip-flops from a standard cell library. The PN sequences for the input chopping waveforms are generated externally for flexibility (although they can very easily and efficiently be generated on-chip using LFSRs), while the output chopping waveform $c_z = c_x c_y$ is generated with a simple XNOR gate. Flip-flops are used to buffer all chopping waveforms to prevent skew which can lead to residual offset. The layout of all blocks, especially the choppers and chopping waveform traces, were made to be as symmetrical as possible to avoid mismatch leading to residual offset.

A die photo is shown in Figure 6-2. The IC was fabricated in National Semiconductor’s 0.18$\mu$m CMOS process, and the active area of the chip occupies 0.05mm$^2$. 

52
6.2 Circuit Details

6.2.1 Multiplier Core

Figure 6-3 shows the multiplier core topology we chose for this work. It is a four-quadrant $V_{gs}V_{ds}$ type multiplier, which was surveyed in [23] as the most recommended analog MOS multiplier structure, due to its low noise, good linearity, and low power supply operation. Transistors M1-M4 are biased in the triode region while transistors M5-M8 are biased in the saturation region. It can be shown that the output voltage
of the multiplier is given by the following equation \[23\]:

\[
V_o = \mu_n C_{ox} \left( \frac{W}{L} \right) \frac{R_L V_x V_y}{1-4} \tag{6.1}
\]

The current through each of the four branches of the multiplier is nominally 25\(\mu\)A in this design. The common-mode voltage of the x-input transistors (M1-M4) is 635mV, and the common-mode voltage of the y-input transistors (M5-M8) is 500mV. These bias voltages are provided off-chip as part of the multiplier inputs.

### 6.2.2 Unity-Gain Buffer

Figure 6-4 shows the implementation of the fully differential, unity-gain buffer. It is composed of two single-ended op-amps in the non-inverting amplifier configuration. Figure 6-5 shows the circuit schematic of the single-ended op-amp. It is a two-stage op-amp, a telescopic stage followed by a common-source stage, with Miller compensation for stability. The core amplifier (excluding the bias network) consumes 1.4mA. Figure 6-6 shows the circuit schematic of the current mirrors which provide
the bias current for the two op-amps used in the buffer. The bias current is set by an
off-chip resistor.

6.2.3 Differential Chopper

Figure 6-7 shows the circuit schematic for the differential chopper. It is implemented
by four NMOS switches, which commutate the differential signals according to the
pattern dictated by the chopping waveforms. Mathematically, the effect is to multiply
the input signal by a signal that alternates between +1 and -1. The four NFETs are
laid out with a common-centroid scheme to minimize mismatch leading to residual
offset.

6.2.4 Chopping Waveform Generation Logic

Figure 6-8 shows the block diagram of the chopping waveform generation logic cir-

cuitry. The $PN_{en}$ control signal determines the type of chopping applied to the

multiplier: logic 0 enables square-wave chopping while logic 1 enables PN chopping.
When square-wave chopping is enabled, the input chopping waveforms $c_x$ and $c_y$ are
Figure 6-5: Circuit schematic of the single-ended op-amp used in the unity-gain buffer.

Figure 6-6: Circuit schematic of the current mirrors which provide the bias current for the two op-amps used in the unity-gain buffer.
quadrature square waves (90° out of phase) at a frequency four times lower than the reference clock $CLK$, while the output chopping waveform $c_z$ is a square wave at twice the frequency of $c_x$ and $c_y$, or two times lower than $CLK$. When PN chopping is enabled, $c_x$ and $c_y$ are set by the externally-provided logic signals $PN_x$ and $PN_y$, respectively, while $c_z = c_x c_y$ is generated by an XOR gate. To disable chopping, the three chopping waveforms can be continuously set to logic 1 by enabling PN chopping and then setting $PN_x$ and $PN_y$ to logic 1.

### 6.2.5 Input Selection Circuitry

Figure 6-9 shows the block diagram of the input selection logic circuitry. The purpose of this circuit block is to allow each differential multiplier input to be shorted together directly on-chip to an externally provided bias voltage, thus avoiding any external offsets (e.g., thermocouple effects) at the multiplier inputs which would cause additional DC offset at the multiplier output. This circuit takes advantage of the fact that the common-mode voltages for the two multiplier inputs ($V_x$ and $V_y$) are both lower than $V_{DD}/2$ (where $V_{DD}$ is the supply voltage). This allows us to use the $V_{icm}$ input as a control voltage which determines whether or not to short the two terminals of the differential input together. We set the switching threshold of the inverters to $V_{DD}/2$, so that if $V_{icm}$ is higher than $V_{DD}/2$, the three inverters restore the voltage to the supply rail to generate a logic 0, which control the switches so that the input
Figure 6-8: Block diagram of chopping waveform generation logic circuitry.
is set to the externally-provided differential voltage. If \( V_{icm} \) is lower than \( V_{DD}/2 \), the three inverters restore the voltage to the supply rail to generate a logic 1, which control the switches to short the input together to \( V_{icm} \). Thus, to apply a differential voltage to the input, \( V_{icm} \) should be set to a voltage higher than \( V_{DD}/2 \), and \( V_{ip} - V_{in} \) should be set to the differential voltage to be applied. To short the input together to a common-mode voltage (applying a differential voltage of 0V), \( V_{icm} \) should be set to the common-mode voltage, and the voltages applied to \( V_{ip} \) and \( V_{in} \) do not matter.

### 6.2.6 Output Polarity Switch

The input selection logic circuitry allows us to remove any external offsets present at the multiplier inputs which would cause additional DC offset at the multiplier output. We also need a way to remove any external offsets which are added at the multiplier output, such as the internal DC offset of the voltmeter. To account for these offsets, a control signal \( SIGN \) is used to switch the polarity of the multiplier output, which allows us to calibrate out the offset. The switch is implemented with a differential chopper as shown in Figure 6-1. To calibrate out the the external offset added at the multiplier output, \( V_{OS,ext} \), we make the following two measurements,
one for \(SIGN = 0\) and one for \(SIGN = 1\):

\[
V_{\text{meas}0} = V_{\text{sig}} + V_{\text{OS,ext}} \quad (6.2a)
\]
\[
V_{\text{meas}1} = -V_{\text{sig}} + V_{\text{OS,ext}} \quad (6.2b)
\]

We can then extract the multiplier output signal without the external offset as follows:

\[
V_{\text{sig}} = \frac{V_{\text{meas}0} - V_{\text{meas}1}}{2} \quad (6.3)
\]

Note that this output polarity switch is nothing more than another chopper which is used to chop away any external offsets added to the output of the chopper-stabilized multiplier system.

### 6.3 Measurement Results

For the prototype multiplier, we measured the offset performance under four different configurations: DC multiplier, squarer, variable-gain amplifier (VGA), and direct-conversion mixer. The DC value of the multiplier output voltage was measured differentially using a Keithley 2001 digital multi-meter (DMM), which can measure 7.5 digits from 200mV. The DMM also has an internal low-pass filter and several averaging features, which we used to filter out the chopping artifacts and any noise at the multiplier output. To obtain the frequency spectrum graphs, an instrumentation amplifier was used to convert the differential output of the multiplier to a single-ended signal. The instrumentation amplifier adds its own offset, so it was not used when measuring DC values. More information regarding the experimental setup used to make the measurements for the prototype multiplier can be found in Appendix A.

#### 6.3.1 DC Multiplier

Figure 6-10 shows the measured DC transfer characteristics of the multiplier with chopping disabled and then with one level of square wave chopping enabled at a
down-chopping frequency of 10kHz. Before chopping we see a substantial offset of 15mV. After chopping we see that the offset is almost completely removed. In another experiment, we measured the worst-case residual offset using a single level of square wave chopping to be 6μV, representing an offset reduction of over 3 orders of magnitude. The multiplier has a gain $k$ of 5.3V$^{-1}$.

Figure 6-11 shows the output spectrum of the multiplier under both square wave and PN chopping. In both cases one level of chopping is enabled, and both inputs of the multipliers are zeroed out. In the square wave case, a down-chopping frequency of 10kHz is used, and we can see that the multiplier's inherent offset is modulated away from DC to the frequency components of the square wave. In the PN case, 9-bit Gold codes were used for the PN sequences spread over a frequency range of 100kHz. The Gold code PN sequences were generated in MATLAB and then programmed into an arbitrary function generator to drive the chopping waveform generation logic block. From the figure, we can see that there are no strong chopping tones present in the output, which may ease the requirements on the subsequent low-pass filter. The noise floor of the multiplier output in the PN case can be lowered simply by increasing the sampling frequency at which the PN sequence is clocked, which increases the frequency range over which the offset is spread. It should also be noted that the tone at DC in these and subsequent spectrum plots is larger than expected from the offset measurements taken with the DMM. This is due to the offset added by the instrumentation amplifier used to interface the differential multiplier output to the spectrum analyzer.

Table 6.1 summarizes the offset performance of our DC multiplier under various inputs and chopping scenarios. With no chopping enabled, the multiplier offset is 15.6mV. When we apply PN chopping using Gold codes of various lengths, we are able to reduce the offset by a factor of $(2^n - 1)$, where $n$ is the number of bits in the Gold code, which is consistent with mathematical predictions. With one level of square wave chopping, the worst case offset is 6μV, representing over three orders of magnitude improvement in the multiplier's inherent offset of 15.6mV. Note that the offset when either of the multiplier inputs is nonzero is worse than when both
Figure 6-10: Measured DC voltage transfer characteristics of the multiplier. (a) Without chopper stabilization. (b) With square wave chopping at a down-chopping frequency of 10kHz.
Figure 6-11: Output spectrum of DC multiplier with square wave chopping at a down-chopping frequency of 10kHz and 9-bit PN chopping spread over 100kHz.

inputs are zero. This is consistent with our analysis of the causes of residual offset, due to both charge injection spikes and DC content in the chopping waveforms (see equation 3.2). By enabling the second level of chopping, the worst-case offset becomes $1.5\mu V$, a full four orders of magnitude improvement from the unchopped case. It should be noted that all chopping methods are able to reduce the offset to the microvolt level, and that nested chopping gives the lowest possible offset. Table 6.2 compares the offset performance of this work to that of other recent works.

<table>
<thead>
<tr>
<th>Inner Chopper</th>
<th>Outer Chopper</th>
<th>$V_x$</th>
<th>$V_y$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>7-bit Gold codes, $f_s=100kHz$</td>
<td>–</td>
<td>0</td>
<td>0</td>
<td>123 $\mu V$</td>
</tr>
<tr>
<td>9-bit Gold codes, $f_s=100kHz$</td>
<td>–</td>
<td>0</td>
<td>0</td>
<td>30.6 $\mu V$</td>
</tr>
<tr>
<td>11-bit Gold codes, $f_s=100kHz$</td>
<td>–</td>
<td>0</td>
<td>0</td>
<td>7.8 $\mu V$</td>
</tr>
<tr>
<td>Square wave @ 100kHz</td>
<td>–</td>
<td>0</td>
<td>0</td>
<td>0.36 $\mu V$</td>
</tr>
<tr>
<td>Square wave @ 100kHz</td>
<td>–</td>
<td>150mV</td>
<td>0</td>
<td>6.06 $\mu V$</td>
</tr>
<tr>
<td>Square wave @ 100kHz</td>
<td>–</td>
<td>0</td>
<td>150mV</td>
<td>4.00 $\mu V$</td>
</tr>
<tr>
<td>Square wave @ 100kHz</td>
<td>Square wave @ 10kHz</td>
<td>0</td>
<td>150mV</td>
<td>0.66 $\mu V$</td>
</tr>
<tr>
<td>Square wave @ 100kHz</td>
<td>Square wave @ 10kHz</td>
<td>150mV</td>
<td>0</td>
<td>1.52 $\mu V$</td>
</tr>
</tbody>
</table>
Table 6.2: Offset Comparison for Various Multiplier Offset Cancellation Techniques.

<table>
<thead>
<tr>
<th>Offset Compensation</th>
<th>DC Offset</th>
<th>Technology</th>
<th>DC Mult?</th>
<th>Cont?</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multiplicative Feedback [3]</td>
<td>9 µV</td>
<td>1.5µm BiCMOS</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Digital Integrator [4]</td>
<td>110 µV</td>
<td>0.18µm CMOS</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Single-level Chopping [10]</td>
<td>204 µV</td>
<td>0.18µm CMOS</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Nested Chopping [This Work]</td>
<td>1.52 µV</td>
<td>0.18µm CMOS</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

6.3.2 Squarer

We configured the prototype multiplier as an analog squarer by shorting the two input voltages $V_x$ and $V_y$ together. Figure 6-12 shows the measured DC transfer curve of the squaring circuit both with and without chopping. Again, we see that enabling chopping almost completely removes the offset. Figure 6-13 shows the output spectrum of the squarer for a 150mV$_{pp}$, 50kHz sinusoidal input, both without chopping and with square wave chopping at a down-chopping frequency of 1MHz. We can see that chopping attenuates the undesired tone at 50kHz by 7.6dB and the tone at 150kHz by 8.8dB. These tones appear at the output due to the input offsets and 2nd-order distortion of the multiplier but are attenuated by the chopping technique as described in equation 3.2 and equation 3.8. Note that there is considerable energy at DC due to the desired squaring action of the circuit, but that the inherent offsets of the multiplier are still translated to the frequencies of the chopping waveforms. It should also be noted that the tone at 200kHz is likely the result of 3rd-order harmonic distortion arising from the terms $k_{31}V_x^3V_y$, $k_{13}V_xV_y^3$, and $k_{33}V_x^3V_y^3$ in equation 3.5, which, unlike the 2nd-order terms, are not suppressed by the chopping technique.

6.3.3 Variable Gain Amplifier

To configure the prototype multiplier as a VGA, we set the $V_y$ input to a DC voltage which determines the gain of the amplifier and the $V_x$ input to the sinusoidal voltage to be amplified. The 3dB bandwidth of the VGA was measured to be about 10MHz. Figure 6-14 shows the output spectrum of the VGA for a 150mV$_{pp}$, 50kHz sinusoidal input with $V_y = 150$mV, both without chopping and with square wave chopping. From this plot we can see that the chopping removes not only the offset from DC,
Figure 6-12: Measured plot of square-law transfer curve.

Figure 6-13: Measured output spectrum of analog squarer with a 50kHz input sine wave.
Figure 6-14: Measured output spectrum of variable gain amplifier with a 50kHz input sine wave.

but the $1/f$ noise of the VGA as well. Furthermore, the 2nd-order harmonic distortion at 100kHz is reduced by 13.6dB. As expected, these undesirable spectral components are translated to the frequencies of the chopping waveforms. Figure 6-15 shows the output spectrum on a log-log plot, where the $1/f$ noise improvement can be more readily seen.

The residual offset after chopping for this input vector is measured to be 41$\mu$V, which is about an order of magnitude worse than the measured offsets for the DC multiplier. This is due to additional offset terms which are not present in the case of DC multiplication, caused primarily by the nonzero AC coupling between the two input ports which are mixed together by the multiplier to produce a DC offset which cannot be reduced by the chopping technique. In addition, thermocouple effects at the AC input of the VGA can create an offset, which is not a problem in the DC multiplication testing because our prototype allows each of the input voltages to be shorted together on-chip. Still, chopping is able to improve the offset by almost 3 orders or magnitude when compared to the unchopped case.

Figure 6-16 shows the output spectrum of the VGA for a 150mV$\text{pp}$, 50kHz sinu-
Figure 6-15: Measured output spectrum of variable gain amplifier with a 50kHz input sine wave, showing improvement in 1/f noise.

soidal input with \( V_y = 0 \)V, both with and without chopping. For this input vector we would expect the output spectrum to be free of any spurious tones since the VGA gain should be zero. However, due to the input offsets of the multiplier, a fraction of the input tone leaks through to the output. We can see from the plot that by enabling chopping, the spurious tones at 50kHz and 100kHz are completely removed. These tones are translated to the frequencies of the chopping waveforms, along with the offset and 1/f noise. The residual offset after chopping was measured to be 0.5\( \mu \)V. This is much better than the measured offset for the previous input vector, which can be attributed to the fact that in this case we were able to short the \( V_y \) input voltage together on-chip to suppress the effect of any AC coupling from the other input port.

6.3.4 Direct-conversion Mixer

To configure the prototype multiplier as direct-conversion mixer, we set the multiplying inputs to have a small difference in their frequency around a base carrier frequency,
Figure 6-16: Measured output spectrum of variable gain amplifier set at zero gain with a 50kHz input sine wave.

Figure 6-17 shows the output spectrum of the mixer where the two inputs have a frequency difference of 50Hz around a base carrier frequency of 500kHz, both without chopping and with 50kHz square wave chopping. Again we see that the offset and 1/f noise are reduced when chopping is applied. The tones at 60Hz, 120Hz, and 180Hz are caused by power line noise in the instrumentation amplifier used to drive the spectrum analyzer. The residual offset after chopping is measured to be 63μV. Again, this is worse than the measured offsets for the DC multiplier due to the parasitic coupling between the two input ports, which sets the performance limit in our multiplier system when AC inputs are used. Figure 6-18 shows the output spectrum of the mixer over a wider frequency range, where we can see that the undesired spectral components are modulated away from baseband to the chopping frequencies.
Figure 6-17: Measured output spectrum of direct-conversion mixer showing baseband output signal.

Figure 6-18: Measured output spectrum of direct-conversion mixer showing undesired spectral components modulated to chopping frequencies.
6.3.5 Filtering Design Considerations

As shown in the various plots of the multiplier output spectrum, the chopping technique generates several spurs or chopping artifacts located at the frequencies of the chopping waveforms. Each of these chopping artifacts correspond to an undesirable spectral component generated by the multiplier, including the input and output offsets, $1/f$ noise, and 2nd-order harmonic distortion, each of which is modulated to one of the chopping frequencies in order to remove them from the desired signal bandwidth. Filtering of the chopping artifacts is not a primary concern in this work, as filtering requirements are highly dependent on the specific application of the multiplier. The amount of attenuation required from the lowpass filter will depend on the magnitude of the various spurs and their frequency locations, as well as the amount of chopper ripple that can tolerated in the multiplier output. For example, assume that the largest spur is caused by the output offset which has a magnitude of 10mV and is modulated by a 1MHz square-wave. If the ripple from this spur must be kept below 100μV, then the lowpass filter should provide approximately 40dB of attenuation at 1MHz. If this filter is implemented as a simple 1st-order RC lowpass filter with a 20dB/dec rolloff, the corner frequency should be 10kHz (note that this sets a limit on the output signal bandwidth of the multiplier). The choice of chopping frequencies affects not only the requirements of the lowpass filter, but also the minimum required multiplier core bandwidth as well as the residual offset performance. As such, the chopping frequencies should be carefully chosen based on the specifications of the given application.
Chapter 7

Chopper Stabilization in RF Mixers

A mixer is a type of analog multiplier used specifically to perform frequency translation. A general-purpose multiplier can be used as a mixer, but not all mixers can be used as general-purpose multipliers. For example, a chopper is a type of mixer because it performs a frequency translation of the input signal, but it cannot be used to multiply two DC signals. Choppers (a type of passive mixer) can be used to perform the mixing function with relatively high linearity; however, they typically do not provide any gain to the signal. Since it is desirable in many applications for the mixer to provide gain, we will focus our attention to active mixers, which do provide gain at the expense of signal quality. In this chapter, we will discuss the specific application of chopper stabilization to RF direct-conversion mixers and show how it can be used to improve the sensitivity of direct-conversion receivers by reducing the mixer's offset, 1/f noise, and even-order distortion.
7.1 Problems with the Direct-conversion Architecture

There are many design challenges associated with the direct-conversion architecture, most of which are summarized in [5]. Here we will discuss only the three which can be improved through applying chopper stabilization to the mixer: DC offset, even-order distortion, and flicker (1/f) noise.

7.1.1 DC Offset

One issue with the direct-conversion architecture is DC offset. Since the downconverted band extends to zero frequency, offset voltages can corrupt the signal and saturate the following stages [5], and the DC offset added by the down-conversion mixer is the main source of this problem. Chopper stabilization can be used to remove the inherent DC offsets in multipliers, and mixers, being a special type of multiplier, are no exception. However, chopping cannot be used to improve the offset caused by the parasitic coupling between the RF and LO ports, which leads to self-mixing as discussed in section 4.3. To combat the offset due self-mixing, the port-to-port coupling between the RF and LO ports should be minimized by isolating the ports as much as possible.

7.1.2 Even-order Distortion

Even-order distortion is another problem with the direct-conversion architecture. Figure 7-1 illustrates the problem [5]. Suppose two strong interferers close to the channel of interest experience a 2nd-order nonlinearity such that the output of the LNA is $y(t) = \alpha_1 x(t) + \alpha_2 x^2(t)$. If $x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t$, then $y(t)$ contains the term $\alpha_2 A_1 A_2 \cos (\omega_1 - \omega_2) t$, a low-frequency spurious tone. The generation of this tone is known as 2nd-order intermodulation (IM2) distortion. If the output of the LNA is multiplied by an ideal mixer, this tone is translated to high frequencies where it can be easily filtered out. However, any real mixer will have a finite direct feedthrough
Interferers

A L7i-Ik 0)

Figure 7-1: Effects of even-order distortion on interferers [5].

from the RF input to the IF output, due to the offset associated with the LO port (caused primarily by transistor mismatch). Thus, a fraction of the undesired tone will appear at the output of the mixer and corrupt the desired signal. As shown in equation 3.2, chopper stabilization modulates the offsets associated with the multiplier input ports to the chopping frequencies, and thus can be used to remove the undesired tone from the desired baseband signal.

Chopping also removes the even-order distortion caused by the mixer, as explained in section 3.3. However, as noted in section 4.3, chopping cannot remove the distortion caused by nonzero coupling between the RF and LO ports which results in self-mixing. To minimize this source of 2nd-order distortion, the port-to-port isolation between the RF and LO ports should be made sufficiently high such that this does not limit the IM2 performance, which can be achieved through careful layout [24]. A more thorough explanation of how chopping removes IM2 products will be given in section 7.2.2.

7.1.3 Flicker Noise

Since the downconverted spectrum is located around zero frequency, the $1/f$ noise at mixer output and in the following stages also corrupts the signal [5]. This is a particularly severe problem in MOS implementations, in which the $1/f$ noise of the devices is relatively large. Chopper stabilization can modulate the $1/f$ noise of the
mixer to the chopping frequencies where it can be filtered out, greatly alleviating this problem.

### 7.2 Principle of Chopper-Stabilized Mixers

#### 7.2.1 Simplified Chopping Architecture

Chopper stabilization was first applied to an RF direct-conversion mixer in [8] to reduce both IM2 and 1/f noise. As previously explained in section 3.5.3, the chopping architecture for direct-conversion mixers can be made much simpler than the chopping architecture for a general-purpose multiplier. This is because the LO input is known to have no DC content, and so the LO input does not need to be chopped to separate it from the DC offset associated with the mixer’s LO port, \( \delta_{LO} \). \( \delta_{LO} \) will still be multiplied by the RF input, but since the RF frequency is much higher than the baseband output, this undesired product can be easily filtered out. Thus, it is sufficient to place one chopper at the RF port and another chopper at the IF (output) port, each modulated by the same chopping waveform (just as in the case of chopper-stabilized amplifiers). As long as the signal energy of the chopping waveform is distributed over frequencies high enough to be filtered out, the desired baseband output signal will be separated from the undesired spectral components generated at mixer output, namely the DC offset, 1/f noise, and IM2 products.

In the above analysis, we have assumed that the RF port contains no low-frequency tones. However, in section 7.1.2, we saw that even-order nonlinearities in the LNA preceding the mixer can create low-frequency spurious tones. In this case, the LO port offset will cause feedthrough of the spurious tones which will corrupt the baseband output signal of the mixer. In the simplified chopping architecture described above, these spurious tones will not be modulated to the chopping frequency (although the even-order distortion products generated by the mixer will). The spurious low-frequency tones at the RF port can be removed by using the full chopping architecture described in section 3.2, at the cost of added complexity (one extra chopper at the LO port).
port and the generation of three different chopping waveforms instead of one). Thus there is a tradeoff between complexity and performance. If the even-order nonlinearity of the LNA is sufficiently low, the extra complexity may be unnecessary. In the following analysis, we ignore the even-order distortion generated by LNA and use the simplified chopping architecture, which still removes the IM2 products generated by the mixer itself, as will be shown in the next section.

Figure 7-2 shows a block diagram of a chopper-stabilized mixer, from which we can write the output of the chopped mixer as follows:

\[
V_{IF} = [(kV_{RF}c_{RF} + \delta_{RF})(V_{LO} + \delta_{LO}) + \delta_{o}]c_{IF}
\]

\[
= kV_{RF}V_{LO}c_{RF}c_{IF} + k\delta_{LO}V_{RF}c_{RF}c_{IF} +
\]

\[
k\delta_{RF}V_{LO}c_{IF} + (k\delta_{RF}\delta_{LO} + \delta_{o})c_{IF}
\]  

(7.1)

\(k\) is the constant of multiplication, \(\delta_{RF}\) is the offset associated with the RF port, \(\delta_{LO}\) is the offset associated with the LO port, \(\delta_{o}\) is the output offset, and \(c_{RF}\) and \(c_{IF}\) are the modulation waveforms for the RF port chopper and IF port chopper, respectively. In this analysis we assume that the mixer is operating as a multiplier in its linear region and therefore neglect any higher-order nonlinearities. Typically the LO port of the mixer is driven with a large sinusoidal voltage or a square wave in order to maximize the conversion gain of the mixer, in which case this assumption is
no longer valid. However, in most implementations this is equivalent to setting $V_{LO}$ to a square wave which switches between -1 and +1 at the LO frequency, so that the mixer becomes similar to a chopper. In this case, only the fundamental component of the square wave at the LO frequency is of interest, since it is this component which results in the desired baseband output when multiplied with the RF input. The odd harmonic components of the square wave are located at frequencies high enough that they can safely be ignored, as they will ultimately be filtered out at mixer output. Thus, the same type of analysis can still be applied.

From equation 7.2, we can see that in order to recover the desired product $kV_{RF}V_{LO}$ at baseband, the product $c_{RFCIF}$ must equal 1. Furthermore, to modulate the output offset and $1/f$ noise away from baseband, the signal energy of $c_{IF}$ must be distributed over frequencies high enough to be filtered out. Just as in the case of amplifiers, to fulfill these conditions it is sufficient to make $c_{RF} = c_{IF} = c_0$, with $c_0$ a square wave which switches between -1 and +1. This modulates the offset and $1/f$ noise to the chopping frequency and its odd harmonics. Figure 7-3 shows the chopper-stabilized mixer where both choppers are driven by the same chopping waveform $c_0$. With this choice the output of the chopped mixer becomes the following:

$$V_{IF} = kV_{RF}V_{LO} + k\delta_{LO}V_{RF} + k\delta_{RF}V_{LO}c_0 + (k\delta_{RF}\delta_{LO} + \delta_0)c_0 \quad (7.2)$$

The first term in equation 7.2, $kV_{RF}V_{LO}$, corresponds to the desired product, while the last term, $(k\delta_{RF}\delta_{LO} + \delta_0)c_0$, corresponds to the output offset and $1/f$ noise which is modulated to the chopping frequencies where it can be filtered out. The second term, $k\delta_{LO}V_{RF}$, corresponds to feedthrough of the RF input to the mixer output due to the multiplication of the RF input with the LO port offset. Although this term is not modulated by the chopping waveform, it is normally not a problem since the RF frequency is much higher than output signal bandwidth, and so it can be easily filtered out. The third term in equation 7.2, $k\delta_{RF}V_{LO}c_0$, corresponds to feedthrough of the LO input to the mixer output, but unlike the RF feedthrough
term, it is modulated by the chopping waveform. This term appears at the difference between the LO frequency and the chopping frequencies, so to filter this term out, the frequency difference should be larger than the output signal bandwidth. In summary, to effectively filter out all the undesired products of the chopper-stabilized mixer, the chopping frequency should be much greater than the output signal bandwidth and much less than the LO frequency.

### 7.2.2 2nd-order Intermodulation Distortion

To see the effect of chopper stabilization on the IM2 products of the mixer, we refer again to equation 3.7, which shows the 2nd-order distortion terms of a general multiplier. If we set the $x$ input as the RF port and the $y$ input as the LO port, set $c_x = c_z = c_0$ and $c_y = 0$ (corresponding to the simplified chopping architecture used for mixers), and apply the identities of equation 3.3, we obtain the following result:

$$V_{HD2,chop} = k_{02}V_{LO}^2c_0 + k_{20}V_{RF}^2c_0 + k_{12}V_{RF}V_{LO}^2 + k_{21}V_{RF}V_{LO}c_0 + k_{22}V_{RF}^2V_{LO}^2c_0 \quad (7.3)$$

In regards to IM2 distortion, we are only concerned about strong interferers at the RF input port (let us assume that the isolation between the RF and LO ports is
sufficiently high that the coupling of these interferers to the LO port can be neglected; this can be achieved with a properly designed layout). Thus the IM2 distortion products will occur due to the three terms containing $V_{RF}^2$ in the above equation. Let us denote the LO frequency by $f_{LO}$ and the chopping frequency by $f_{ch}$. The first term, $k_{20}V_{RF}^2c_0$, modulates the IM2 product to $f_{ch}$. The second term, $k_{21}V_{RF}V_{LO}c_0$, modulates the IM2 product to $f_{LO} \pm f_{ch}$. The third term, $k_{22}V_{RF}^2V_{LO}^2c_0$, modulates the IM2 product to $f_{ch}$, since $V_{LO}^2$ produces a tone at DC (since $V_{LO}^2$ also produces a tone at twice the LO frequency, the IM2 product is also modulated to $2f_{LO} \pm f_{ch}$, which is at a high enough frequency that it can safely be ignored). Thus the IM2 distortion products are modulated to either $f_{ch}$ or $f_{LO} \pm f_{ch}$, where they can be filtered out by choosing the chopping frequency appropriately. Another important factor which determines the location of the IM2 products is the frequency difference of the interferers, which can be as large as the bandwidth of the preselection filter of the receiver. Since the IM2 products can span this bandwidth, special care should be taken to select a chopping frequency such that all the IM2 products fall outside the signal bandwidth where they can be effectively filtered out. In general, this can be achieved by making $f_{ch}$ much greater than the output signal bandwidth and much less than $f_{LO}$. Note that this is the same condition required to filter out the undesired products generated by the mixer’s inherent offsets, as concluded in section 7.2.1.

As shown in equation 7.3, the 2nd-order nonlinearities of the mixer generate other undesirable tones other than the IM2 products. It can be easily shown that after chopping is applied, all the tones are modulated to one of the following frequencies: $f_{ch}$, $f_{LO} \pm f_{ch}$, $f_{RF}$, $2f_{LO} \pm f_{RF}$, $2f_{RF} \pm f_{LO} \pm f_{ch}$, $2f_{LO} \pm f_{ch}$, $2f_{RF} \pm f_{ch}$, and $2f_{LO} \pm 2f_{RF} \pm f_{ch}$. To effectively filter out all these undesired products, all these frequency locations should be much higher than the signal bandwidth. Once again, this can be achieved by making the chopping frequency should be much greater than the signal bandwidth and much less than the LO frequency.
7.2.3 Pseudorandom Noise Chopping

Just like chopper-stabilized amplifiers and multipliers, another possibility for the chopping waveform $c_0$ is a PN sequence which randomly switches between -1 and +1. This type of modulation spreads the undesired spectral components over a wide frequency range rather than concentrating them at specific frequency locations, which may simplify the filtering process. However, since PN sequences are usually generated using LFSRs which generate sequences with $2^{n-1}$ occurrences of +1 and $2^{n-1} - 1$ occurrences of -1 (where $n$ is the number of stages in the LFSR), the average value of these waveforms is $1/(2^n - 1)$. This means the reduction in DC offset, $1/f$ noise, and IM2 products is limited by this factor. Furthermore, by modulating the undesired spectral components by pseudorandom noise, the noise floor at mixer output is raised proportionally, lowering the SNR. The amount of noise added in the signal bandwidth can be reduced by increasing the sampling frequency at which the PN sequence is clocked, which effectively spreads the undesired products over a wider frequency range. Thus, both the length and the sampling frequency of the PN sequence should be properly chosen to achieve the offset, SNR, and IM2 requirements for the specific application.

7.3 Nested Chopper Stabilization in Mixers

To effectively remove the undesired spectral components generated at mixer output, including the DC offset, $1/f$ noise, and IM2 products, it is desirable to make the chopping frequency much higher than the output signal bandwidth. However, the effectiveness of chopper stabilization degrades as the chopping frequency increases, since the main sources of residual offset after chopping is applied are proportional to the chopping frequency, as explained in chapter 4. To overcome this tradeoff, the nested-chopping technique can be applied as described in chapter 5, which allows the chopping frequency to be lowered to improve the performance. There is a limit to this technique, however, as the chopping frequency should still be greater than the signal bandwidth. As such, nested chopping is generally not suitable for high bandwidth
Figure 7-4: Nested chopper-stabilized mixer.

applications. Figure 7-4 shows a block diagram of a nested chopper-stabilized mixer.

It should also be noted that, even though it is desirable to make the chopping frequency high to ease filtering requirements on the modulated offset, $1/f$ noise, and IM2 products, a higher chopping frequency makes it more difficult to filter out the LO feedthrough term in equation 7.2 and the $k_2 V_{RF}^2 V_{LOC_0}$ term in equation 7.3, both of which appear at the difference between the LO frequency and the chopping frequency. For carrier frequencies in the GHz range, this is typically not a concern. The chopping frequency should be carefully chosen to meet the design requirements of the specific application.
Chapter 8

Prototype RF Mixer IC

A prototype IC was fabricated in a 0.18μm CMOS process to experimentally evaluate the effectiveness of chopper stabilization in removing offset, 1/f noise, and 2nd-order distortion from a RF direct-conversion mixer. The prototype mixer is designed to operate in the 1800MHz band of the GSM standard. This chapter describes the circuit details for each block in the prototype IC and presents our measured results.

8.1 System Overview

A block diagram of the chopper-stabilized mixer prototype is shown in Figure 8-1. For the mixer core, a pseudo-differential Gilbert cell was chosen for this work. However, we emphasize that the chopper stabilization technique described in this paper can be applied to any differential mixer topology. Two levels of chopping switches surround the mixer core. Each level of chopping can be enabled or disabled by controlling the inputs to the chopping waveform generation logic circuitry.

The chopping operation is implemented by four MOS switches, which commutate the differential signals according to the pattern dictated by the chopping waveforms. Mathematically, the effect is to multiply the input signal by a signal that alternates between +1 and -1. To generate the square wave chopping waveform, an externally supplied reference clock is divided using flip-flops from a standard cell library. This is to help ensure the duty cycle is as close to 50% as possible. The PN chopping
Figure 8-1: Block diagram of prototype chopper-stabilized RF mixer.
waveforms are generated externally for flexibility (although they can very easily and efficiently be generated on-chip using LFSRs). The layout of all blocks, especially the choppers and chopping waveform traces, were made to be as symmetrical as possible to avoid mismatch leading to residual offset.

A die photo is shown in Figure 8-2. The IC was fabricated in National Semiconductor’s 0.18µm CMOS process, and the active area of the chip occupies 0.012mm². The mixer draws 3.5mA from a 1.8V supply.
8.2 Circuit Details

8.2.1 Mixer Core

Figure 8-3 shows the mixer core topology we chose for this work. It is a type of pseudodifferential Gilbert cell multiplier. A pseudo-differential topology was chosen due to its lower 3rd-order nonlinearity and increased voltage headroom [12]. The penalty is higher 2nd-order nonlinearity, but this will be improved through the chopping technique. The charge-injection technique is also employed, in which the current in the switching stage (the LO transistors) is made less than the current in the input stage (the RF NMOS transistors) by injecting the current difference into the RF NMOS transistors [25]. This lowers the current through the load resistors so that they can be made larger for the same amount of voltage swing, thus increasing the gain. Additionally, the injected current is reused by adding a PMOS to the RF input stage, so that the total input transconductance is the sum of the transconductance of the PMOS and NMOS transistors [26]. The mixer was designed to operate at an RF/LO frequency of 1.8GHz. Matching networks for the RF and LO ports were implemented off-chip, and the bias current was provided by an off-chip resistor. The mixer core draws 3.2mA from a 1.8V supply.

8.2.2 Differential Chopper

Figure 8-4 shows the circuit schematics for the differential choppers used in the RF mixer prototype. Each chopper is implemented by four MOS switches, which commutate the differential signals according to the pattern dictated by the chopping waveforms. NMOS devices are used for the RF-port choppers, while PMOS devices are used for the IF-port choppers, due to the respective DC common-mode levels at the RF and IF ports. The MOS switches are sized large enough to meet the bandwidth requirements of the mixer and so that they do not contribute too much extra noise to the mixer. The choppers are laid out with a common-centroid scheme to minimize mismatch leading to residual offset.
Figure 8-3: Circuit schematic of the mixer core.

Figure 8-4: Differential choppers used in the prototype RF mixer IC.
Figure 8-5: Block diagram of chopping waveform generation logic circuitry for the prototype mixer.

8.2.3 Chopping Waveform Generation Logic

Figure 8-5 shows the block diagram of the chopping waveform generation logic circuitry. The $PN_{en}$ control signal determines the type of chopping applied to the mixer: logic 0 enables square-wave chopping while logic 1 enables PN chopping. When square-wave chopping is enabled, the chopping waveform is a square wave at half the frequency of the reference clock $CLK$. When PN chopping is enabled, the chopping waveform is set by the externally-provided logic signal $PN$. To disable chopping, the chopping waveform can be continuously set to logic 1 by enabling PN chopping and then setting $PN$ to logic 1.

8.3 Measurement Results

For the prototype mixer, we measured the improvement in the offset and 2nd-order intermodulation distortion of the mixer after chopper stabilization was applied. The DC value of the mixer output voltage was measured differentially using a Keithley 2001 DMM, which can measure 7.5 digits from 200mV. To obtain the frequency spectrum graphs, an instrumentation amplifier was used to convert the differential output of the mixer to a single-ended signal. More information regarding the experimental setup used to make the measurements for the prototype mixer can be found
Table 8.1: Measured Mixer Performance Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>No Chopping</th>
<th>Chopping @5MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>8.2 mV</td>
<td>21 μV</td>
</tr>
<tr>
<td>Offset w/ -21dBm two-tone RF input</td>
<td>6.65 mV</td>
<td>-1.46 mV</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>7.8 dB</td>
<td>7.8 dB</td>
</tr>
<tr>
<td>IIP2</td>
<td>55.7 dBm</td>
<td>56.7 dBm</td>
</tr>
<tr>
<td>IIP3</td>
<td>7.2 dBm</td>
<td>7.3 dBm</td>
</tr>
<tr>
<td>Supply</td>
<td>1.8V</td>
<td></td>
</tr>
<tr>
<td>Current Dissipation</td>
<td>3.5mA</td>
<td></td>
</tr>
<tr>
<td>RF/LO Frequency</td>
<td>1.8GHz</td>
<td></td>
</tr>
</tbody>
</table>

Table 8.1 summarizes the mixer’s measured performance. With no chopping enabled, the mixer offset is 8.2mV. When we apply square-wave chopping at 5MHz, the offset is reduced to 21μV, representing over two orders of magnitude improvement. However, when performing the two-tone test to measure the mixer’s intermodulation distortion, the offset worsens dramatically. The two tones applied to the RF port for the two-tone test were 1.801GHz and 1.8011GHz, both at -21dBm power. For these inputs, the offset was measured to be 6.65mV without chopping and -1.46mV with 5MHz chopping. Based on the considerable offset improvement when no AC inputs are applied to the RF port, we can conclude that the mixer offset performance is severely limited by self-mixing due to poor port-to-port isolation between the RF and LO ports, as explained in section 4.3, in this case resulting in an additional offset of about 1.5mV. The self-mixing caused by the port-to-port coupling also limits the improvement in the IM2 distortion when chopping is applied, which we can see from the table is only 1dB.¹ A goal of future research will be to employ more careful layout techniques to make sure the coupling between the RF and LO ports is minimized such that it does not limit the offset and IM2 performance.

¹The measure of the mixer’s IM2 distortion is given by the 2nd-order input intercept point, or IIP2. This IIP2 specification represents a fictitious input amplitude at which the desired signal becomes equal in amplitude to the spectral component generated from IM2 distortion [8]. Thus a high IIP2 is desirable. A analogous specification exists for 3rd-order intermodulation (IM3) distortion, called the 3rd-order input intercept point, or IIP3.
Chapter 9

Conclusion

In this thesis a method of offset cancellation for analog multipliers using chopper stabilization is described which provides continuous offset rejection without sacrificing DC performance. The theory of chopper-stabilized multipliers is discussed in detail, including both square-wave chopping and chopping with orthogonal spreading codes, and the nested chopping technique is introduced and applied to analog multipliers for the first time.

The limits on the offset performance of a chopper-stabilized multiplier are also examined, including a detailed analysis of the residual offset due to the charge injection mismatch in the differential input choppers, which is the main cause of residual offset in chopped amplifiers. Other possible sources of residual offset are discussed, including DC content in the chopping waveforms, parasitic thermocouples, nonzero port-to-port coupling, and asymmetrical layout of bond-pads, choppers, and wires.

A prototype IC of a chopper-stabilized, general-purpose multiplier was fabricated in a 0.18μm CMOS process, achieving a worst-case offset of 1.5μV through the application of the nested chopping technique. This is the lowest measured offset reported in the analog multiplier literature. AC measurements were performed on the prototype multiplier configured as a squarer, VGA, and direct-conversion mixer, demonstrating that chopper stabilization is effective at reducing not only DC offset, but also 1/f noise and 2nd-order harmonic distortion.

The specific application of chopper stabilization to RF direct-conversion mixers
is also discussed in detail, showing how it can be used to improve the sensitivity of direct-conversion receivers by reducing the mixer’s offset, $1/f$ noise, and even-order distortion. A prototype IC of a chopper-stabilized RF mixer in a 0.18μm CMOS process is presented, along with measured results.

9.1 Future Work

The offset and IM2 distortion of the prototype mixer presented in this thesis is severely limited by self-mixing due to poor port-to-port isolation between the RF and LO ports. This limits the improvement obtained when chopper stabilization is applied, since chopping cannot suppress the effects of self-mixing, as explained in section 4.3. A goal of future research will be to employ more careful layout techniques to make sure the coupling between the RF and LO ports is minimized such that it does not limit the offset and IM2 performance.
Appendix A

Experimental Setup

This appendix describes the experimental setup used to make the measurements for the prototype multiplier and RF mixer. A printed circuit board was designed and manufactured in order to test the both the multiplier and the mixer, which were fabricated on the same IC. A QFN package was chosen for the IC due to its relatively small pad parasitics. The package bonding diagram for the prototype IC is shown in Figure A-1.

A.1 Prototype Multiplier Test Setup

A block diagram of the test setup for the prototype multiplier is shown in Figure A-2. The circuit details of the chopper-stabilized multiplier were described in section 6.2. This section will describe the input stages and the output stage in more detail, which provide the interface between the packaged IC and the test and measurement equipment.

A.1.1 Input Stages

Two different types of input stages were used, one for AC signal inputs and one for DC signal inputs. Figure A-3(a) shows the input stage used for AC inputs. The AC signals were generated by a function generator, which were then connected to a power splitter.
Figure A-1: Package bonding diagram for the prototype IC.

Figure A-2: Test setup for the prototype multiplier.
to transform the single-ended signal to a differential one. The differential signal was then AC coupled to the multiplier inputs. The common-mode voltages were generated by a DC power supply and connected to the multiplier inputs through bias resistors. Figure A-3(b) shows the input stage used for DC inputs. The two terminals of the differential voltage were both generated by a DC power supply and connected to the multiplier inputs through bias resistors.

For testing it was also necessary to provide a differential voltage of 0V, in order to measure the DC offset of the multiplier. The input selection logic circuitry implemented on-chip and described in section 6.2.5 accomplished this function. The $V_{x,\text{en}}$ and $V_{y,\text{en}}$ inputs shown in Figure A-2 (corresponding to the $X_{\text{en}}$ and $Y_{\text{en}}$ pads in Figure A-1) were used to determine if the inputs were shorted together on-chip or tied to the input stages described above.

### A.1.2 Output Stage

The DC value of the multiplier output voltage was measured differentially using a Keithley 2001 digital multi-meter (DMM) connected directly to the multiplier output pads. The DMM has an internal low-pass filter and several averaging features, which we used to filter out the chopping artifacts and any noise at the multiplier output. This DMM can measure 7.5 digits from 200mV.

To measure the frequency spectrum of the multiplier output voltage using a spectrum analyzer, the differential signal must be converted to a single-ended signal. An instrumentation amplifier was used to accomplish this function. Figure A-4 shows the...
A.2 Prototype RF Mixer Test Setup

A block diagram of the test setup for the prototype RF mixer is shown in Figure A-5. The circuit details of the chopper-stabilized mixer were described in section 8.2. This section will describe the input stages and the output stage in more detail, which provide the interface between the packaged IC and the test and measurement equipment.

A.2.1 Input Stages

The input stages for both the RF and LO ports are shown in Figure A-5. The RF and LO signals were generated by a function generator, which were then connected to a bandpass filter to remove any harmonics generated by the function generator. The signals are then connected to transformers to convert the single-ended voltages into a differential ones for the mixer IC. After the transformers are matching networks to
Figure A-5: Test setup for the prototype RF mixer.
provide a power match to the RF and LO port impedances.

A.2.2 Output Stage

The prototype RF mixer uses the same output stage used in the testing of the prototype multiplier (see section A.1.2). The DC value of the mixer output voltage was measured differentially using a Keithley 2001 DMM connected directly to the mixer output pads. To measure the frequency spectrum of the mixer output voltage using a spectrum analyzer, the differential signal was converted to a single-ended signal with an instrumentation amplifier, implemented with the Analog Devices part AD8250.
Bibliography


