An Exploratory Design of a 65 nm CMOS Buck Converter for Maximum Efficiency

by

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Abstract

Portable battery-operated consumer devices, such as mp3 players, cell phones, and digital cameras, are becoming ever more prevalent and so the need for long battery life is increasingly important. These small devices contain power converters that produce lower supply voltages from the fixed battery voltage source. For long battery life, it is necessary to maximize the efficiency of the power converter. A design is proposed for the topology and control of a 65 nm CMOS DC/DC switch-mode converter converting a 3 V battery supply to a 1.2 V output voltage for a maximum output current of 100 mA. The goal of the project was to maximize converter efficiency and improve on the maximum 40% efficiency of a traditional linear regulator. With the proposed topology and control scheme described in this report, the buck converter operates at a switching frequency of 10 to 75 MHz with a maximum efficiency of 93.63%.
Acknowledgements

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Additionally, a huge thank you goes out to the MIT Women’s Ultimate Frisbee team, sMITe. The past four years I have spent on the team have provided me with some of my most fulfilling and memorable experiences at MIT. Frisbee has taught me focus and
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Chapter 1: An Introduction to Integrated Power Management

1.1 Surge in Power Management

When you walk out the door in the morning, you may see runners on the sidewalks, pumping their legs to the beat of the music from their mp3 players. Throughout the day, you see people gabbing on cell phones with friends. If you are in the city, there may even be a camera-happy tourist snapping away with his digital camera. Portable battery-operated consumer devices, such as mp3 players, cell phones, and digital cameras, are becoming ever more prevalent and to keep these devices running, long battery life is necessary. From this growing market in portable consumer devices comes the surge of interest in power management that has occurred in the past few years.

Many of these consumer devices contain chips of the most advanced semiconductor technology. In accordance with Moore's Law, CMOS processes have gone down to 65 nm and soon will reduce even more to 45 nm. As CMOS devices decrease in size, the power supply on which the chip runs must also decrease in voltage. However, battery inputs are remaining at relatively high voltages. Hence, a voltage converter is needed to produce lower input voltages from the fixed battery voltage source. In all converters, though, there will be power loss, and the goal is to minimize that power loss and avoid draining the battery while doing this voltage conversion.

My thesis proposes a design for the topology and control of a 65 nm DC/DC switch-mode converter in order to maximize converter efficiency and improve on the efficiency of a traditional linear regulator, thus reducing the power lost when converting the battery input to a lower supply voltage for a 65 nm IC. In Chapter 1, I will provide background on the advantages of a switching converter over a linear regulator and the specific goals of my buck converter. Chapter 2 characterizes the switching and conduction loss of the 65 nm transistor devices. Chapter 3 discusses how to choose an inductor and Chapter 4 describes how the switch topology was chosen. The control scheme for the buck converter is discussed in Chapter 5 and final simulation results shown in Chapter 6. The conclusion and ideas for future work are given in Chapter 7.
1.2 Linear Regulators versus Switched Converters

1.2.1 Voltage Conversion for Digital Cameras

At Analog Devices, Inc. (ADI) in Wilmington, MA, the digital imaging systems (DIS) group makes analog-front-end (AFE) ICs that are predominantly used in digital cameras. The camera normally has a 3 V battery supply, but the voltage actually range between 2.25 V and 3.6 V. The chips that the DIS group makes have been fabricated in the 0.18 \( \mu \)m process but they are moving toward the 65 nm process. For a 0.18 \( \mu \)m process, a conversion from 3 V to 1.8 V is needed while for the 65 nm CMOS process, a conversion of 3 V to 1.2 V is needed. Either a linear regulator or a switching power converter may be implemented to achieve the step down in voltage.

1.2.2 Linear Regulator Efficiency

DIS has thus far used linear regulators, specifically low dropout regulators (LDOs), as the power converter in their chips. An LDO is shown in Figure 1. The MOSFET of the LDO is always active and power is dissipated through both the transistor and the many resistors in the linear regulator.

![Low-Dropout Regulator (LDO)](image)

**Figure 1: Low-Dropout Regulator (LDO)**

The LDO is a type of linear regulator. There are many lossy components in this configuration. If the voltage across the PMOS is given as \( V_{DS} \), then the maximum achievable efficiency is only \( 1 - \frac{V_{DS}}{V_{DD}} \) [1].
While LDOs are straightforward to implement, they have the disadvantage of limited efficiency. Efficiency is defined by:

\[ \eta = \frac{P_{\text{out}}}{P_{\text{in}}} \]  

(Eq. 1)

In the case of a linear regulator, the maximum possible efficiency is only:

\[ \eta = \frac{V_{\text{out}}}{V_{\text{in}}} \]  

(Eq. 2)

For a 0.18 \( \mu \)m AFE, the maximum efficiency that the LDO can have for a 3 V input is only \( \eta = 1.8/3 = 60\% \). The efficiency for a 65 nm process chip is even worse at \( \eta = 1.2/3 = 40\% \). As fine processes are introduced into the industry, the needed output voltage will continue decreasing. Meanwhile, the input voltage remains fixed around 3 V, and efficiency continues to drop drastically with each new process. In addition, DIS AFEs may have a input voltage range between 2.25 V and 3.6 V. Within this input voltage range, the efficiency will vary widely depending on the input voltage. In Figure 2, the efficiency of a linear regulator is shown for 0.18 \( \mu \)m, 0.13 \( \mu \)m, and 65 nm processes for the input voltage range of 2.25 V to 3.6 V. From 2.25 to 3.6 V, the efficiency of a linear regulator drops by 20-30\%. The variance of the LDO efficiency is high and the efficiency becomes very low for high input voltages. In the 65 nm case, the efficiency can be as high as 53.33\% but as low as 33.33\%.
Figure 2: Linear Regulator Efficiency vs. Input Voltage
Linear regulator maximum efficiency for 0.18μm, 0.13μm, and 65 nm processes are shown for 2.25 V to 3.6 V input voltages. Efficiency drops with smaller processes as well as with greater input voltages.

1.2.3 Switching Converter Efficiency

Switching converters allow more flexibility in the output voltages they can provide. While linear regulators can only convert voltage down, switching converters can change voltages up or down with either a boost or a buck converter. For digital cameras, a buck converter would be used to step down the 3 V input to a 1.2 V output voltage. A synchronous buck converter implemented in CMOS can be seen in Figure 3.
The buck converter is a switching converter that produces a lower output voltage $V_{out} = DV_{in}$, where $D$ is the duty cycle ratio of the switch control. The converter uses all ideally lossless components and is high in efficiency.

Ideally, switching converters are 100% efficient since all the components, such as switches, an inductor, and a capacitor, are ideally lossless. In actuality, there exist internal losses in the converter so that efficiency may be reduced to 80-90% or less, depending on the switching frequency, load current, etc. These non-idealities include conduction and switching loss of the transistor switches and series resistance of the inductor or capacitor. Even though the efficiency is reduced from 100% due to non-idealities, it is still possible to drastically improve upon the efficiency of linear regulators.

### 1.2.4 Previous Research

In previous research for integrated switched DC/DC converters, the efficiency improvement over linear regulators has been significant. Integrated DC/DC converters have been fabricated in 0.18 um down to 90 nm processes and example results are shown in Table 1.

The LDO maximum efficiency was calculated by dividing the converter’s output voltage by its input voltage. The maximum efficiencies of the switched converters are shown in the previous column and in almost all cases, the converter efficiency is at least
20% more efficient than the LDO. In the worst scenario, in the 0.18 um process, one of the converters has the same efficiency for both the switched converter and linear regulator. In the best case, also in the 0.18 um process, the DC/DC converter is around 63% more efficient than an LDO.

Table 1: Results of Previous Integrated DC/DC Converters

<table>
<thead>
<tr>
<th>0.18 um</th>
<th>Vin (V)</th>
<th>Vout (V)</th>
<th>Iload (mA)</th>
<th>DC/DC Efficiency</th>
<th>LDO Max Efficiency</th>
<th>fsw (MHz)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.4</td>
<td>0.9</td>
<td>250</td>
<td>79.60%</td>
<td>16.67%</td>
<td>97</td>
<td>[2]</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td>0.9</td>
<td></td>
<td>88.00%</td>
<td>50.00%</td>
<td>102</td>
<td>[3]</td>
<td></td>
</tr>
<tr>
<td>2.8</td>
<td>1.8</td>
<td>200</td>
<td>64.00%</td>
<td>64.29%</td>
<td>45</td>
<td>[4]</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>0.13 um</th>
<th>Vin (V)</th>
<th>Vout (V)</th>
<th>Iload (mA)</th>
<th>DC/DC Efficiency</th>
<th>LDO Max Efficiency</th>
<th>fsw (MHz)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.6</td>
<td>2.5</td>
<td></td>
<td>80.00%</td>
<td>69.44%</td>
<td>100</td>
<td>[5]</td>
<td></td>
</tr>
<tr>
<td>3.6</td>
<td>1.5</td>
<td></td>
<td>70.00%</td>
<td>41.67%</td>
<td>100</td>
<td>[5]</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>90 nm</th>
<th>Vin (V)</th>
<th>Vout (V)</th>
<th>Iload (mA)</th>
<th>DC/DC Efficiency</th>
<th>LDO Max Efficiency</th>
<th>fsw (MHz)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8</td>
<td>0.9</td>
<td>500</td>
<td>72.00%</td>
<td>50.00%</td>
<td>480</td>
<td>[6]</td>
<td></td>
</tr>
<tr>
<td>1.8</td>
<td>0.9</td>
<td>500</td>
<td>76.00%</td>
<td>50.00%</td>
<td>250</td>
<td>[6]</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>0.9</td>
<td>300</td>
<td>80-87%</td>
<td>75.00%</td>
<td>100</td>
<td>[7]</td>
<td></td>
</tr>
<tr>
<td>3.6</td>
<td>1.3</td>
<td>100</td>
<td>94%</td>
<td>36.11%</td>
<td>1.5</td>
<td>[8]</td>
<td></td>
</tr>
</tbody>
</table>

1.3 Buck Converter Topologies

When working in 65 nm, some means is needed to interface the process devices with the relatively high-voltage input. One means of doing this is shown in Figure 3 where the extended 65 nm devices used have longer channels and can handle a maximum 3.3 V stress across any two terminals. However, core devices have short channel lengths and can only handle 1.2 V stress across any two terminals. To compensate for the reduced voltage blocking capability of the core devices, a cascode bridge topology is proposed (see e.g., [2]).

In addition to considering different switches, it is also necessary to consider different inductors, such as whether to implement an external inductor or an on-chip one.

To understand the reason for exploring these different topologies, it is important to understand how the buck converter operates.
1.3.1 Basic Operation of a CMOS Buck Converter

The basic buck converter has at least two power switches driven by a clock. The clock and its duty cycle determine when each switch is on or off. A simple example is shown in Figure 4. The CMOS buck converter has two switches, a PMOS switch and an NMOS switch in inverter topology. The inverter output at the $v_x$ node is filtered by the LC output filter. The capacitor is large enough so that $V_{\text{out}}$ is nearly a DC value with only a small AC ripple. In the case of ADI's 65 nm buck converter, the input voltage, $V_{\text{in}}$, is around 3 V and output voltage, $V_{\text{out}}$, is 1.2 V.

![Figure 4: Operation of a Buck Converter](image)

Looking at the buck converter in more detail, in Figure 4(a), the clock has transitioned low and the top switch is turned on for duty cycle $D$ of the period $T$. In this case, the $v_x$ node is pulled to $V_{\text{in}}$, which is greater than $V_{\text{out}}$. A positive voltage across the inductor leads to a ramp up in inductor current. In (b), the clock has transitioned high so the bottom switch is on and $v_x$ is pulled to ground. A negative voltage across the inductor leads to a ramp down in inductor current. The inductor current as it varies with the clock can be seen in Figure 5.
In periodic steady state, the average current across the inductor must equal the load current so that the ramp-up height equals the ramp-down height. With some simple algebra, the relationship between $V_{in}$ and $V_{out}$ can be determined.

\[
\frac{(V_{in} - V_{out})}{L} DT = \frac{V_{out}}{L} (1 - D)T \quad \text{(Eq. 3)}
\]

\[
(V_{in} - V_{out})D = V_{out} (1 - D) \quad \text{(Eq. 4)}
\]

\[
V_{in}D = V_{out} \quad \text{(Eq. 5)}
\]

For an ideal buck converter, it can be seen that $V_{out} = DV_{in}$ in periodic steady state. Hence the output voltage can be easily adjusted by just varying the duty cycle of the clock that drives the switches. In the case where $V_{in} = 3$ V and $V_{out} = 1.2$ V, duty cycle $D$ will be around 40%.
1.3.2 Switch Topologies

1.3.2.1 Inverter Topology and High Voltage Devices

For the inverter topology in Figure 3 and 4, each switch will have a maximum of $V_o$ across its drain-to-source when the switch is in the off-state. In this CMOS implementation, the two switches are driven by the same clock. When the clock transitions low, the top PMOS switch turns on and the $v$ node is pulled to $V_o$. Meanwhile, the bottom NMOS switch has a voltage stress of $V_o$ from drain to source. The same scenario applies to the PMOS switch when it is off. In the inverter topology, the maximum stress across all the switches is $V_o$ or 3 V. High voltage devices must be used in this topology in order to withstand the high voltage stress.

The advantage of using the inverter topology is its simplicity. An inverter is a simple design with only two switches driven by one clock. However, a drawback of the inverter topology is the use of high voltage devices. These MOSFETs have longer channels to allow for higher voltage stresses, but longer channels also leads to more gate capacitance and greater switching losses. In the considered process, the extended NMOS have minimum length of 0.5 $\mu$m while the extended PMOS have minimum length of 0.4 $\mu$m.

1.3.2.2 Cascode Bridge Topology and Core Devices

Cascode variants of the synchronous buck converter are often used when the input voltage exceeds the individual device voltages [2]. The cascode topology considered here allows for the use of core devices that can only handle 1.2 V maximum stress but are typically much better in performance than extended voltage devices. The cascode bridge switch configuration explored here is shown in Figure 6.
For a 3 V input voltage, a six-switch cascode topology gives a maximum voltage stress of 1 V for each switch. However, intermediate voltages are needed to make this work.

Since the input voltage is 3 V for the desired buck converter, the 3 V must be divided across three core device switches so as to not exceed the 1.2 V maximum stress allowed on an individual switch. This results in a total of six switches in the cascode bridge, increasing the complexity of the buck converter. As seen in Figure 6, the input voltage has to be divided into thirds and the gates of M2 and M5 held at $2/3 \times V_i$ and $1/3 \times V_i$ respectively. The 1V-amplitude clock must be level-shifted to the appropriate voltage range for M6, M4, M3, and M1. The clock signal driving M1 and M6 are in phase whereas the signal driving the gates of M3 and M4 are out of phase of the clocks at M1 and M6 [2].

The cascode bridge configuration can be advantageous, though, since the core devices have a minimum channel length of 60 nm, which allows for a much smaller device area and a reduction in capacitances. Less capacitance will mean less switching losses as
well as the capability of switching more quickly. With the cascode topology, it is possible to
switch at high frequencies such as hundreds of MHz while the high voltage devices in the
inverter topology cannot even operate at 100 MHz.

1.3.3 Inductor Implementations

Typically inductors for integrated DC/DC converters are off-chip and external to
the IC. External inductors tend to have a higher quality factor, $Q$, between 20 and 100 and
lower DC series resistance, ESR. Being off-chip, they can also be larger in inductance, and
the converter can run at a slower switching frequency, allowing for less switching loss. A
disadvantage of an external inductor, however, is that anything off-chip means extra I/O
pads and more parasitics such as bonding wires and board capacitances. More parasitics
can lead to a decrease in efficiency as well as more noise.

Implementing an on-chip inductor would remove the problem of additional
parasitics as in the case with the external inductor, but there are some drawbacks in terms
of size and efficiency. Internal inductors occupy a large portion of the chip and when chip
area is limited, inductor area can be a deciding factor. Also, the inductance of an internal
inductor must be small to keep the area of the inductor reasonable, but this means the
switching frequency of the converter must be much higher in order to keep current ripple
across the inductor small. Higher switching frequency leads to higher switching loss and
restricts the buck converter switch topology to that of the cascode bridge. Another
drawback is that integrated inductors tend to have a low $Q$ of less than 10 and a high ESR,
which can mean a hit in efficiency due to resistive power loss [9]. In recent years, though,
researchers have been looking at new methods to fabricate higher $Q$ and lower ESR
integrated inductors. When exploring whether to use an external or internal inductor, the
type of internal inductor used was determined by what ADI had available in the 65 nm
process.

1.4 Sources of Efficiency Loss in a Buck Converter

As previously mentioned, switched-mode converters are not 100% efficient due to
non-idealities. To understand in greater depth the loss mechanisms in a DC/DC switched
converter, it is necessary to take a closer look at the power switches and inductor. Non-idealities in the switches lead to power loss in the form of conduction loss and switching loss. Switching losses include overlap loss as well as gating loss.

Another possible source of significant efficiency loss is the resistance of the inductor. Since the load current and its ripple flow across the inductor, any series DC or AC resistance may lead to substantial power loss.

1.4.1 Conduction Loss

Conduction loss is the power loss from the MOSFET switches while they are on and conducting current. To calculate conduction loss, the transistors can be modeled as an ideal switch in series with a resistor, $R_{on}$, as shown in Figure 7.

![Figure 7: Switch-resistor Model of MOSFET](image)

When a transistor switch is turned on, the load current flows across the MOSFET and power loss occurs as the current flows across the MOSFET's drain-to-source resistance.

The conduction loss calculation is a simple formula,

$$P_{loss} = I_{DS,RMS}^2 R_{DS} = <i_{DS} v_{DS}>$$

(Eq. 6)

where $I_{DS,RMS}$ is the RMS drain-to-source current (which is approximately equal to the load current), $R_{on}$ is the drain-to-source on-resistance of the device, and $V_{DS}$ is the drain-to-source voltage when the device is on. For a 3 V input and a 1.2 V output, the PMOS switch or
switches are on for 40% of the time and the NMOS for 60% of the time. The total conduction loss of this buck converter is given by

\[ P_{\text{loss}} = (D I_{DS,PMOS})^2 R_{DS,PMOS} + ((1 - D) I_{DS,NMOS})^2 R_{DS,NMOS} \]  
(Eq. 7)

1.4.2 Switching Losses

While conduction losses occur when the transistor devices are fully on, switching losses occur when the devices are transitioning between on and off. Hence, switching losses are directly proportional to the frequency at which the switches are clocked. Two types of switching losses are overlap loss and gating loss.

1.4.2.1 Overlap Loss

MOSFETs are not ideal switches. When turning on or off the device, neither the \( I_{ds} \) nor \( V_{ds} \) rise or fall instantaneously. When turning on the switch, there will be a duration of time when \( v_{ds} \) is dropping toward zero volts while \( i_{ds} \) is rising to the load current as shown in Figure 8. This overlap of significant nonzero \( v_{ds} \) and \( i_{ds} \) is the source of overlap loss. The same type of efficiency loss occurs when at turn off when \( v_{ds} \) begins rising while \( i_{ds} \) is still dropping to zero.

![Overlap Loss](image)

**Figure 8:** Overlap Loss When Turning On the Switch

When the switch turns on, there is a transition period where the drain-to-source voltage falls and the drain-to-source current rises. Overlap loss occurs during this transition.
1.4.2.2 Gating Loss

Gating loss also occurs at transitions when the switches are turning on or off. Each of the MOSFET gates are driven by inverters that are connected between $V_{ss}$ and $V_{dd}$. These inverters lossily charge and discharge the gate capacitance of the power switches. The charging and discharging of the gate capacitance is the source of gating loss.

As an example, in Figure 9, when the bottom NMOS power switch, M3, is transitioning to the on-state, the PMOS, M1, of the inverter gate driver is conducting current from $V_{DD}$. Charge is drawn from $V_{DD}$ to charge up the gate capacitance of the power switch. Once the gate is charged above the threshold voltage, the power switch has been turned on. When the clock transitions high and turns on the NMOS of the inverter gate driver, M2, the gate of M3 is discharged and the charge that was drawn from $V_{DD}$ is now flowing to $V_{SS}$. The same type of charge and discharge of gate capacitance

Figure 9: Gating Loss from Charge and Discharge of Gate Capacitance
M1 and M2 are the inverter driver to the gate of M3, a power switch. (a) M3 is turned on and its gate capacitance is charged from $V_{ss}$. (b) M3 is turned off and its gate capacitance is discharged to $V_{ss}$.
occurs for the PMOS power switch, M4, and this flow of charge from one source to the other is gating loss.

1.4.3 Inductor Loss

Inductors are ideally lossless, but in reality, each inductor has some series resistance that leads to power loss whenever current conducts across the inductor. In the case of the buck converter, the inductor on average carries the full load current so the resistive loss can be significant.

The effective resistance of an inductor is a combination of wire resistance, radiation loss, eddy currents and hysteretic loss. All of these resistances increase with switching frequency, so a high switching frequency will not only increase switching losses but also lead to higher effective resistance [10].

On the other hand, a low switching frequency or a small inductance can lead to a large current ripple through the inductor. It can be seen from Figure 5 that current ripple is inversely proportional to switching frequency and the inductance. The DC power loss across the ESR of the inductor is simply \( I^2 \cdot R_{ESR} \). The AC power loss from the ESR is proportional to the square of the ripple current. The total power loss from the DC and AC values of ESR is approximately given by:

\[
P_{ind} = I_{DC}^2 R_{ESR,DC} + \frac{(i_{ripple})^2}{3} R_{ESR,AC} \quad \text{(Eq. 8)}
\]

where \( I_{DC} \) is the load current and \( i_{ripple} \) is the half peak-to-peak current ripple, \( i_{rpm} \), of the inductor and is calculated as

\[
i_{pp} = DT \frac{V}{L} \quad \text{(Eq. 9)}
\]

with \( V \) as the voltage across the inductor. In this case, the assumption was made that the AC inductor current is a zero-mean triangular waveform, which results in

\[
i_{AC,RMS} = i_{ripple}/\sqrt{3}.
\]

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1.5 Converter Specifications

To deem any 65 nm DC/DC converter design a success, it must meet the same specifications as the previous LDO design used by the DIS group. The focus is on maximizing efficiency with a strict requirement that the converter must exceed the 33.33-53.33% efficiency range of a 65 nm LDO. To determine to the specifications to be met by the 65 nm buck converter, it is first necessary to consider the specifications of the 0.18 μm LDO used by Analog Devices.

<table>
<thead>
<tr>
<th>Table 2: 0.18 μm LDO Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vin</strong></td>
</tr>
<tr>
<td><strong>Vout</strong></td>
</tr>
<tr>
<td><strong>Iload</strong></td>
</tr>
<tr>
<td><strong>Efficiency</strong></td>
</tr>
<tr>
<td><strong>Startup Time</strong></td>
</tr>
<tr>
<td><strong>Line Regulation</strong></td>
</tr>
</tbody>
</table>

From the LDO specs, I built goals for a 65 nm buck converter design, which are shown in Table 3.

<table>
<thead>
<tr>
<th>Table 3: 65 nm DC/DC Converter Goals</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Vin</strong></td>
</tr>
<tr>
<td><strong>Vout</strong></td>
</tr>
<tr>
<td><strong>Iload</strong></td>
</tr>
<tr>
<td><strong>Fsw</strong></td>
</tr>
<tr>
<td><strong>Efficiency</strong></td>
</tr>
<tr>
<td><strong>Startup Time</strong></td>
</tr>
<tr>
<td><strong>Settling Time</strong></td>
</tr>
<tr>
<td><strong>Vout ripple</strong></td>
</tr>
<tr>
<td><strong>Vout transient</strong></td>
</tr>
<tr>
<td><strong>Vout SS error</strong></td>
</tr>
</tbody>
</table>

The buck converter should handle the same input voltage range as the LDO, and output a steady 1.2 V +/- 50 mV, despite variations in input voltage. The converter should also provide the same range in load current. The switching frequency was chosen so that the buck converter could operate off the same clock as the AFE clock. Not only would this avoid having to create a separate clock, but also the AFE already takes measures to lessen
the effect of noise that is at its clock frequency. Hence, using the same clock for both converter and AFE could reduce the effect of switching noise on the AFE.

For transient behavior, the startup time should be less than 0.1 ms to match the 0.18 μm LDO and settling time after a step in load or input voltage should be less than 1 μs. After a load or \( V_i \) step, the output voltage should peak up or down by only 100 mV at most and settle to an average value within 50 mV of the desired 1.2 V output. The output voltage should also have a small ripple no greater than 20 mV peak-to-peak in its steady state. The focus, though, of the buck converter was to maximize the efficiency across all loads, switching frequencies, and input voltages. The spec goal was a converter with greater than 60% efficiency in all cases but over 90% in the best case.
Chapter 2: Characterizing 65 nm Power Switch Devices

In order to compare losses in 65 nm implementations, schematics were created in Cadence and simulations run in ADI’s ADICE software to characterize the power switches. The conduction and switching losses of the two device types in their respective topologies were found across different switch widths, switching frequencies, and load currents.

2.1 Conduction Loss of 65 nm Devices

Before a switch topology could be chosen, the high voltage and core device losses had be characterized. Conduction loss was found for a high voltage PMOS or NMOS and for a stack of core PMOS or NMOS through ADICE simulations. Test schematics were created to find the $R_{ds}$ of the devices for a 100 mA and 10 mA load. The setups in Figure 10(a) and (b) were used in simulation to find the conduction loss of the high voltage devices at a specific load current. The $I_{dc}$ current source was a DC source that was set to 100 mA and 10 mA. The high voltage switches were driven with a 3 V difference between gate and source while the low voltage devices were driven with a 1.2 V difference between gate and source. The widths of the PMOS and NMOS were varied to determine the relationship of the $R_{ds}$ with device width. As the width of the device increases, the drain-to-source resistance decreases and eventually flattens out. The channel on-resistance is given by the expression $R_{ds} = \frac{1}{\mu C_{ox}} \left( \frac{W}{L} \right) (V_{gs} - V_T)$ and is inversely proportional to the device width. The NMOS switches for both types of devices have a lower $R_{ds}$ than the PMOS switches and the $R_{ds}$ at lower loads is lower when the device widths are smaller. For the NMOS switches, the $R_{ds}$ of one high-voltage device is roughly the same as the total $R_{ds}$ of the stacked low-voltage devices. For the PMOS switches, at widths of greater than 4000 µm, the $R_{ds}$ of one high-voltage PMOS is about the same as the total $R_{ds}$ of the three core PMOS devices. Hence, beyond 4000 µm width devices, the conduction loss is comparable between the high voltage and core devices. Another consideration, though, is that for the same width, the area of extended devices is nearly 10 times that of the low-voltage core devices due to the much longer channels of the extended devices.
Figure 10: Conduction Loss Test Schematics

(a) Test schematic for the high voltage PMOS, (b) Test schematic for high voltage NMOS, (c) Test schematic for core PMOS devices in cascode configuration, (d) Test schematic for core device NMOS in cascode configuration.
2.2 Switching Loss of 65 nm Devices

To find switching loss of the high voltage and core devices, the inverter and cascode topologies were simulated with a 1 pF capacitive load. The high voltage switches in the inverter setup were controlled by one square wave oscillating between ground and 3 V. The core devices were controlled by 1 V amplitude clocks as shown in Figure 6. The setup was tested at 10 and 100 MHz. The widths of the PMOS and NMOS were varied between different simulations, but for each simulation, all PMOS and NMOS device widths were the same and lengths were kept at the minimum allowed value. Switching loss was determined by integrating the current drawn from the clock, averaging it over the period, and then multiplying by the clock voltage amplitude. By measuring the switching loss using this method, the switching loss measured was predominantly gating loss.
Figure 12: Switching Loss Across Device Width
(a) Switching loss for high voltage inverter topology and low voltage cascode topology for a 100 MHz clock, (b) switching loss for high voltage inverter topology and low voltage cascode topology for 1 MHz clock. The percentage loss was calculated as a ratio of power burned in switching to the maximum output power of the desired buck converter, $1.2V \times 100 mA = 0.12 W$.

In Figure 12, the measured switching loss for each topology is shown for a 100 MHz clock and a 1 MHz clock. The loss is shown as a percentage of the maximum output power, 0.12 W, of the 65 nm buck converter. For the 100 MHz clock, loss for the high voltage devices due to switching is much greater than that of the low voltage devices. As the device widths increase, the difference between high voltage and low voltage topologies becomes even more extreme. At 5000 um width, the low voltage cascode bridge configuration is 18.6% more efficient in terms of switching loss and for all widths, the loss is 9.3-9.4 times larger for the two-switch inverter topology than for the cascode topology.

While switching at 1 MHz, the same trend is seen. The high voltage inverter switching loss is approximately 9.5 times greater than the low voltage cascode loss across widths from 500 to 6000 μm. However, even at 6000 μm at 1 MHz switching frequency, the percent efficiency loss due to switching for the high voltage setup is only 0.25%, which is an insignificant loss. At lower frequencies, the switching loss is so small for both topologies that the difference in loss between high voltage and low voltage switch configurations can be ignored.

For both switching frequencies, there is an upward trend in switching loss as device width increased. For a larger width and a fixed length, the device gate capacitances are
greater, meaning more charge is needed from the $V_{DD}$ supply to charge up the capacitances to the correct gate-source voltage. That charge is then discharged to ground or $V_s$. With more capacitance, more charge flows from $V_{DD}$ to $V_s$ and gating loss is larger.

### 2.3 Tradeoff in Conduction and Switching Losses

When sizing the switches, it is important to take into consideration the tradeoff in conduction and switching losses. As seen in section 2.1, the drain-to-source resistance and thus conduction loss decreases with device width. In section 2.2, though, it is shown that with a larger device width, there is greater switching loss, namely greater gating loss. When plotting the sums of conduction and switching losses, there will be a width that gives a minimum total efficiency loss due to the power switches.

In Figure 13(a), the efficiency loss of each switch topology is shown for a 100 mA load and 100 MHz switching frequency for various device widths. The simulations were run in cases (a)-(d) with the widths of the PMOS and NMOS sized to the same value in order to make a preliminary characterization of the CMOS switches. The cascode topology settles to below 5% efficiency loss for widths 3000 to 6000 μm whereas the inverter topology has a minimum efficiency loss at 1600 μm of approximately 13%. As the width of the inverter switches are increased, the efficiency loss from the power switches rises to 23% by 5000 μm. At the same switching frequency and a 10 mA load, shown in Figure 13(b), the switching loss becomes more significant since output power is low for a 10 mA load and conduction losses are also small for low currents. In this case, the cascode topology losses are still much lower than that of the inverter topology across all widths. In Figure 13(d), with 10 mA at 1 MHz, the high voltage inverter configuration is still less efficient than the cascode bridge for widths greater than 300 μm, but the efficiency loss for the high voltage setup is less than 2% for even large device widths. Only for high load and low frequency as shown in Figure 13(c) are the two topologies comparable in efficiency loss of the power switches.
For low frequencies, the high voltage topology is acceptable in efficiency loss. Even at high loads and low frequencies, less than 2% efficiency loss is not significant and is worth the tradeoff for a simpler switch topology. However, for higher frequencies, the switching loss of the high voltage devices is too high to worth the tradeoff. Instead, for good high frequency performance, the more complex cascode bridge is a better choice.
Chapter 3: External vs. Internal Inductor

3.1 External Inductor

Efficiency loss from a bulk inductor is in most part due to its ESR, so when choosing an external inductor to model in simulation, a low ESR is a key feature. The Taiyo Yuden inductor wound chip power inductors, CB series were therefore a suitable fit. The smallest packaging for the Taiyo Yuden inductor is 0603 packaging (1.6 mm x 0.8 mm x 0.8 mm) and is available for a range of inductances from 1 μH to 47 μH [11]. An external inductor can be large in inductance since it is off-chip. A larger inductance will give a smaller current ripple for a given frequency, and a smaller ripple means less noise at the output and less AC power loss. However, for a greater inductance, the Taiyo Yuden DC-resistance is also larger. 1 μH is sufficiently large for a converter running between 10 and 75 MHz with a load of 50-100 mA when the AFE is fully on. The current ripple was calculated using Eq. 9 and is shown in Table 4. The Taiyo Yuden CB 0603 1 μH inductor only has a DC-resistance of 90 mΩ. In Table 4 the calculated efficiency loss due to inductor DC-resistance from a 100 mA load is shown for frequencies of 10 to 75 MHz. The lower the frequency, the larger the current ripple and the higher the efficiency loss.

<table>
<thead>
<tr>
<th>Inductor value (H)</th>
<th>DC Res (ohms)</th>
<th>Frequency (MHz)</th>
<th>( I_{PP}^2 ) (A)</th>
<th>( P_{IND} ) (W)</th>
<th>Efficiency loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00E-006</td>
<td>0.09</td>
<td>10.00</td>
<td>0.0360</td>
<td>9.39E-04</td>
<td>0.78</td>
</tr>
<tr>
<td>1.00E-006</td>
<td>0.09</td>
<td>20.00</td>
<td>0.0180</td>
<td>9.10E-04</td>
<td>0.76</td>
</tr>
<tr>
<td>1.00E-006</td>
<td>0.09</td>
<td>40.00</td>
<td>0.0090</td>
<td>9.02E-04</td>
<td>0.75</td>
</tr>
<tr>
<td>1.00E-006</td>
<td>0.09</td>
<td>60.00</td>
<td>0.0060</td>
<td>9.01E-04</td>
<td>0.75</td>
</tr>
<tr>
<td>1.00E-006</td>
<td>0.09</td>
<td>75.00</td>
<td>0.0048</td>
<td>9.01E-04</td>
<td>0.75</td>
</tr>
</tbody>
</table>

The efficiency loss from the inductor is less than 1%, which is an insignificant amount of power loss when compared to the loss of the switches.

The external inductor was simulated with the full buck converter circuit and parasitics, but in order to simulate the complete converter, it was necessary to choose an external capacitor.
3.1.1 External Capacitor

The capacitor in a buck converter must be large enough to hold the output voltage at a near DC value and keep output voltage ripple low. The output voltage ripple can be calculated by the following formula.

\[ \Delta v_{\text{ripple}} = \frac{(\Delta i_{pp}/2)(T/2)}{2C} \]  

(Eq. 10)

The ripple voltage will be larger for a lower switching frequency. At a low frequency of 10 MHz, the current ripple is calculated to be 72 mA peak-to-peak for 3 V input and 1.2 V output. Then, for a maximum peak-to-peak output voltage ripple of 10 mV, or 20 mV peak-to-peak, at 10 MHz, the capacitance must be greater than 90 nH. To keep the ripple small, a 1 \( \mu \)F capacitor value was chosen for the output filter.

The 1 \( \mu \)F capacitor that was chosen was a Tanceram chip capacitor. The advantages of the Tanceram chip capacitor include low ESR, small size, and these devices are recommended for DC/DC converter smoothing [12]. The chosen 1 \( \mu \)F, 16 V capacitor has .02 to .07 ohms of ESR in the frequency range of 10-100 MHz. The case size is 0402, which has dimensions of 1.02 x 0.51 x 0.64 mm.

3.1.2 Simulation Results

When simulating the buck converter with the specified external output filter, the high voltage devices were first chosen as the power switches for simplicity. The full converter circuit is shown in Figure 14.
Figure 14: High Voltage Switch Topology with Parasitics and External Output Filter
The external inductor and capacitor were modeled with a high voltage inverter topology. The $V_{DD}$ and $V_{SS}$ input pins of the converter are connected to 3 V and ground via modeled bond wires. The output pin connects to the external output filter with a bond wire and 3 pF board capacitance on either side of the connection.

Simulations were started at 4 MHz and the frequency was swept until the frequency began dropping drastically. In this case, the simulations were run from 4 to 20 MHz with a 100 mA load. The switches were sized at a width of 4000 μm and then at 5000 μm. In addition, parasitics were modeled in these simulations as shown in Figure 14. Bond wires were placed at every input and output pin and were modeled by a 2 nH inductor in series with a 100 mΩ resistor. At the $\text{v}_x$ node, an output pin is simulated with a bond wire out to the external inductor and 3 pF parasitic capacitance on either side of the bond wire.

The simulation results are shown in Figure 15. The efficiency of the converter is plotted versus switching frequency for each switch width value. For low frequencies, the efficiency is in the range of 88-89% but begins to decline quickly past 8 MHz. By 20 MHz,
the efficiency has dropped to between 82 and 84%. For a 100 mA load, the efficiency loss due to parasitic resistance is around 3% and as previously mentioned, inductor ESR loss is less than 1%. The majority of the efficiency loss is in the power switches. For low frequencies, the efficiency curve is flatter since conduction loss is dominant. At higher frequencies, the switching loss of the converter begins to dominate as seen in the efficiency dropping with increasing frequency.

![Efficiency vs Frequency Graph](image)

**Figure 15: 65 nm Buck Converter Simulation Results with External Output Filter**

4000 μm and 5000 μm high-voltage power switches were simulated with a 1 μH external inductor and 1 μF capacitor. The efficiency of the converter with modeled parasitics is plotted against switching frequency.

Despite switching losses, the simulations show that efficiencies much greater than 40% can be achieved using an external inductor and the high voltage devices, and that an efficient 65 nm DC/DC buck converter is a feasible goal.

### 3.2 Internal Inductor

The internal inductor used in simulation was a spiral inductor using a thick top metal layer of the chip. When simulating the inductor, four parameters could be adjusted—number of turns, radius, track width, and distance from the guard ring. To keep inductor series resistance low, the radius and track width were set to large values of 90 μm
and 30 μm respectively. The distance from the guard ring was a suggested 50 μm and was not varied between simulations. The only parameter of the internal inductor that was varied was the number of turns in the spiral inductor.

While increasing the number of turns in a spiral inductor increases the inductance value, it also means a greater series metal resistance since a greater length of metal is used for the spiral tracks. A larger inductance allows for a slower switching frequency and thus lower switching loss. However, higher series metal resistance results in greater resistive power loss from the inductor. In addition, on-chip inductors use a large portion of chip area and increasing the number of turns of the inductor only exacerbates the space issue. The tradeoff in inductance and series resistance is shown in Table 5.

Table 5: Internal Inductor Characteristics

<table>
<thead>
<tr>
<th>no. of turns</th>
<th>rad (μm)</th>
<th>w (μm)</th>
<th>gdis (μm)</th>
<th>L (nH)</th>
<th>Rs (ohms)</th>
<th>Min fs w for CCM (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>90</td>
<td>30</td>
<td>50</td>
<td>4.33</td>
<td>0.81</td>
<td>831</td>
</tr>
<tr>
<td>4.5</td>
<td>90</td>
<td>30</td>
<td>50</td>
<td>7.04</td>
<td>1.09</td>
<td>511</td>
</tr>
<tr>
<td>5.5</td>
<td>90</td>
<td>30</td>
<td>50</td>
<td>10.79</td>
<td>1.40</td>
<td>333</td>
</tr>
</tbody>
</table>

The minimum switching frequency required for continuous conduction mode (CCM) as specified in Table 5 was determined for a 40% duty cycle and a load of 100 mA so maximum peak-to-peak current ripple was 200 mA. In CCM, the output current remains positive even at its minimum. The 10.79 nH inductance allows for a much slower switching frequency than the 4.33 nH but at the price of nearly double the series resistance. For a 100 mA load, the DC series resistance efficiency loss is calculated to be only 6.75% for 4.33 nH as opposed to 11.67% for 10.79 nH. The efficiency loss due to the internal inductor was verified using Cadence and ADICE simulations.

Simulations were run at 200 MHz even though the inductor current ripple dipped to negative values at this frequency. Above 200 MHz, switching loss increased greatly with switching frequency. Initial simulations were run with a cascode topology with an ideal inductor at various frequencies between 200 MHz and 400 MHz. The PMOS switches were sized at 7000 μm width and 60 nm gate length while the NMOS switches were sized at 3000 μm width and 60 nm gate length. The PMOS width was sized larger than the NMOS switches since the $R_{ds}$ of the PMOS device is higher than that of the same width...
NMOS. By sizing the PMOS larger, the conduction loss was reduced and split more evenly between PMOS and NMOS. The best efficiency results for the converter occurred at a lower frequency of 200 MHz as seen in Figure 16.

Figure 16: Converter Efficiency Across Switching Frequency with Ideal 10.8 nH Inductor

The converter efficiency with an ideal 10.8 nH inductor drops from 80.55% at 200 MHz to 69.08% at 400 MHz. The total switching loss increases from 11.47% at 200 MHz to 19.39% at 400 MHz. Majority of the converter efficiency drop is due to increasing switching loss at higher switching frequencies.

To determine the efficiency penalty from the series resistance of the non-ideal internal inductor, the same simulation was run at 200 MHz except with the non-ideal 10.79 nH inductor replacing the ideal 10.8 nH inductor. The converter with the non-ideal inductor is 66.86% efficient. Replacing the ideal inductor with the non-ideal model resulted in a 13.69% efficiency drop. The remaining 19.45% efficiency loss is predominantly due to a combination of conduction, overlap, and gating loss.

3.2.1. Zero Current Switching

In the initial simulations, the switches were driven by clocks with the same fixed duty cycle and phase. With a clock of 200 MHz, the current ripple was around 300 mA peak-to-peak in simulation and dipped to approximately -60 mA. The overlap efficiency loss at 200 MHz was 8.85%. However, if the clocks were adjusted so that the PMOS and
NMOS switches were run at different duty cycles and phases, then, zero current switching (ZCS) could be implemented and overlap loss reduced.

From simulation plots, it was determined that overlap loss mainly occurs when turning on the PMOS switches. One method of reducing this overlap loss is to adjust the timing of the clocks. Before turning on the PMOS, the NMOS switches are on and current through the inductor is negative. The current flows through from \(v_x\) to \(V_o\) through the NMOS, shown in Figure 17(a). Instead of turning on the PMOS immediately after the NMOS are turned off, the non-overlap time between PMOS and NMOS clocks is extended so that there is a longer dead time when all switches are not driven. The PMOS are then switched on when the inductor current is approximately zero. If turned on while the load current is small and near zero, the overlap loss will also be zero since the overlap loss is due to the product of \(I_s\) and \(I_{Ls}\) during the switching transition. Additionally, during this dead time, the inductor current charges up parasitic capacitance at node \(v_x\), increasing the voltage at that node to above 2 V, shown in Figure 17(b). The \(v_x\), \(p0\), and \(p1\) nodes were at 0 V, 1 V, and 2 V respectively when the NMOS switches were conducting, but when the PMOS switches are turned on, all three nodes rise to 3 V. However, the time it takes for these nodes to charge up to 3 V is the transition time in which overlap loss occurs. By adding the dead time and allowing \(v_x\) and thus \(p0\) and \(p1\) to charge up close to 3 V before the PMOS are turned on, the transition time that leads to overlap loss is shortened and overlap loss reduced.
With the added dead time and zero current switching, the overall efficiency of the converter increased by 3.13% from 66.86% to 69.99%. The overlap loss decreased by 3.56%, so the dead time did improve converter efficiency slightly by reducing overlap loss in the converter.

3.2.2 Multiphase

While zero-current switching improved the converter efficiency by a few percent, efficiency was only increased by 3.13%. To achieve a more significant improvement in efficiency, a dominant source of power loss was targeted—inductor resistive loss. The 10.79 nH non-ideal inductor resulted in an additional 13.7% efficiency loss since the series resistance is high at 1.4 Ω. One method to reduce the resistive loss is to decrease the amount of current passing across the inductor, which can be achieved by having multiple buck converters and inductors in parallel. Each converter is run at a different phase so the
converters can actually be run faster but maintain a reasonable output ripple current and voltage. An example of a two-phase topology is shown in Figure 18.

![Two-phase Buck Converter Diagram](image)

Figure 18: Two-phase Buck Converter
The two-phase buck has two sets of identical power switches and two identical inductors that connect at the output capacitor. The clocks driving each set of switches are 180° out-of-phase. Multiphase allows for a smaller output ripple current and voltage for a given frequency and splits the current equally through each parallel branch.

By using a multiphase converter, each converter branch only takes \( \frac{100}{n} \) mA when running at maximum load, where \( n \) is the number of branches. By splitting the amount of current through each inductor and its 1.4 \( \Omega \) ESR, efficiency will increase significantly since resistive loss is proportional to current squared. As can be seen from Table 6, total calculated efficiency loss due to the series resistor from a DC 100 mA load drops nearly 10% from 11.6% to 2.9% when two-phases are used instead of just one. As the number of phases is increased, the efficiency loss continues decreasing but not quite as significantly.

<table>
<thead>
<tr>
<th># of phases</th>
<th>Power loss (W)</th>
<th>% Eff loss</th>
<th>Inductor area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.014</td>
<td>11.628</td>
<td>0.3393</td>
</tr>
<tr>
<td>2</td>
<td>0.003</td>
<td>2.907</td>
<td>0.6787</td>
</tr>
<tr>
<td>3</td>
<td>0.002</td>
<td>1.289</td>
<td>1.018</td>
</tr>
<tr>
<td>4</td>
<td>0.001</td>
<td>0.727</td>
<td>1.357</td>
</tr>
</tbody>
</table>

Table 6: Multiphase Efficiency Loss and Area Calculations for 100 mA Load
A two-phase topology was simulated in Cadence and ADICE. The same 10.79 nH internal inductor with 1.4 Ω ESR was used for each branch and the power switches were all sized at 5000 μm. The switching frequency was doubled to 400 MHz. In these simulations, zero current switching was not used but instead all switches were run with a clock of the same fixed duty cycle. The efficiency of the two-phase converter for a 100 mA load improved to 84.56%, a near 20% efficiency improvement upon the original single-phase fixed duty-cycle simulation.

The additional improvement beyond the previously expected 9% efficiency improvement when adding a second-phase comes from parasitic losses. In the original single-phase converter, when the power switches would turn off, the $V_{\text{dd}}$ and $V_s$ nodes would ring due to the sudden voltage change across the bond wire inductor. The ringing would lead to power dissipation in the bond wire resistor. In addition, the $v_x$ node settled more slowly due to the ringing so when the output filter averaged the voltage at $v_x$, the output voltage would be too low. To compensate, the duty cycle would be increased. PMOS drain-to-source resistance is higher than that of the NMOS so the conduction loss would then increase and efficiency would be lowered.

With two phases, the $V_{\text{dd}}$ and $V_s$ supplies are connected to both cascode bridges so even though the switches are turning on off, between the two bridges, there is always current being sourced or sunk into $V_{\text{dd}}$ and $V_s$ and little ringing occurs since there are no sudden voltage changes across the bond wire inductances.

### 3.3 Inductor Decision

When choosing between an external and internal inductor, two critical deciding factors were converter efficiency and inductor chip area. The efficiencies measured from simulation were compared, and the calculated internal inductor chip area was considered.

#### 3.3.1 Efficiency

The difference in efficiency between the external and internal inductor buck converters can be attributed mostly to the difference in ESR between the Taiyo Yuden external inductor and the internal spiral inductor. The DC resistance of the external
inductor resulted in only 0.75% efficiency loss whereas for the internal inductor, the DC series resistance loss was calculated to be 11.63% for a single-phase buck converter. As seen in Table 6, as more phases are added, the total ESR efficiency loss of the internal inductors decreases significantly. However, four phases must be implemented in order to reduce DC loss down to 0.72%, which is in the same range as for the external inductor. With each new phase, another internal inductor is added and more chip area must be devoted to inductors. Additionally, each phase also requires another set of power switches and a phase-shifter, increasing the complexity of the converter.

From simulation, the overall achievable efficiency for a 100 mA current load was comparable between the external and internal inductor configurations if the topology for the internal inductor was at least two-phase. The external inductor converter ranged between 82-89% efficient for 4-20 MHz switching frequency while the internal inductor two-phase buck was 84.56% efficient at 400 MHz switching frequency. While these two converters resulted in similar efficiencies, the much higher frequency required by the small internal inductor also resulted in ringing across the parasitic bond wires that affected the settling time of the \( V \) node of the buck. As for the slower frequency buck, there was little noticeable ringing and the parasitics had less of an effect on the converter than in the high frequency case.

3.3.2 Size

A major concern of having on-chip inductors is the amount of chip area that the inductor will occupy. From Table 6, the area for one 10.79 nH, 1.4 \( \Omega \) spiral inductor is 0.34 mm\(^2\). The area of one inductor is about half the area of the desired chip size. Adding another phase and another spiral inductor exceeds the amount of area allowed for the full chip. With the technology used to create the spiral inductor, it is also recommended to isolate it from the rest of the chip, so no circuitry can be created in metal layers beneath the spiral inductor. Hence, multiphase and even single phase are not feasible for the internal inductor.

Due to the large size of the spiral internal inductor, an external inductor was chosen for the output filter of the buck converter. In addition, the external inductor will allow for a less complex topology that can be run at a slower frequency. Only one phase is necessary
for high efficiency since the external inductor’s ESR is only 90 mΩ. The slower frequency allowed by the large inductance of the external inductor will prevent ringing from significantly affecting the performance of the converter as it did in the case of the internal inductor.
Chapter 4: Choosing a Switch Topology

Upon choosing an external inductor for the output filter, the next step was to choose a switch topology. For an internal inductor, only the low voltage core devices could be used for switching at hundreds of megahertz. However, for a 1 μH inductor, the switching frequency can be slowed to the AFE clock frequency range of 10 to 75 MHz, in which case, either high or low voltage devices can be used, and hence either the inverter or cascode bridge topology are possible implementations. In order to choose a switch configuration, simulations were run for each topology across frequency and load, and then converter efficiencies were compared. For each simulation, the clocks were run at a fixed duty cycle with no feedback control or dead times. The output filter consisted of the 1 μH Taiyo Yuden inductor model and the 1 μH Tanceram chip capacitor, and all parasitic bond wires and board capacitances were included.

4.1 High Voltage Inverter Topology

The high voltage power switches were all sized at 5000 μm width and minimum length for lower conduction loss at high loads. The buck converter was first simulated across frequency from 10 to 75 MHz at a fixed load current of 100 mA and a 3 V input voltage. Parasitic loss was comparable across all frequencies so conduction loss, overlap loss, and gating loss were compared and results are shown in Table 7. As frequency increases, the overall efficiency drops from 88.73% at 10 MHz to 68.40% at 75 MHz. With faster frequency, the conduction loss remains roughly the same. However, both overlap and gating loss increase with gating loss becoming the dominant loss at high frequencies. The increase in total switching loss from 10 MHz to 75 MHz is 17.38% while the drop in total efficiency is 20.33%. Majority of the decrease in efficiency from 10 to 75 MHz is due to the greater switching losses, and more specifically due to large gating loss at high frequencies.
Table 7: Converter Efficiency for Inverter Topology across Frequency, 100 mA Load

<table>
<thead>
<tr>
<th>Freq (MHz)</th>
<th>Efficiency (%)</th>
<th>Conduction Loss (%)</th>
<th>Overlap loss (%)</th>
<th>Gating Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>88.73</td>
<td>3.997</td>
<td>0.898</td>
<td>2.499</td>
</tr>
<tr>
<td>40</td>
<td>78.55</td>
<td>3.415</td>
<td>3.595</td>
<td>8.834</td>
</tr>
<tr>
<td>75</td>
<td>68.40</td>
<td>3.012</td>
<td>6.065</td>
<td>14.716</td>
</tr>
</tbody>
</table>

The buck converter was then tested across varying current loads from 1 to 100 mA at a fixed switching frequency of 40 MHz and a 3 V input voltage. When the AFE is powered up, the current load may range between 50 and 100 mA, but when on standby, the load may only be 1 to 10 mA. Simulations were run at the edges of these two modes. Total efficiency as well as conduction and switching losses are shown in Table 8. As before, conduction loss is not too significant while gating loss becomes the most dominant loss mechanism. When the AFE is powered up and running at 40 MHz, the efficiency is in the 70-80% range at 40 MHz switching frequency, which is much greater than the 40% maximum achievable efficiency of an LDO. However, for standby mode, the efficiency drops down to 6-40%. In this case, an LDO would be both more efficient and simpler to build.

Table 8: Converter Efficiency for Inverter Topology across Load Current, 40 MHz

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>Efficiency (%)</th>
<th>Conduction Loss (%)</th>
<th>Overlap loss (%)</th>
<th>Gating Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>78.55</td>
<td>3.415</td>
<td>3.596</td>
<td>8.834</td>
</tr>
<tr>
<td>80</td>
<td>77.16</td>
<td>2.671</td>
<td>4.132</td>
<td>10.443</td>
</tr>
<tr>
<td>50</td>
<td>72.12</td>
<td>2.018</td>
<td>5.529</td>
<td>14.738</td>
</tr>
<tr>
<td>10</td>
<td>40.14</td>
<td>1.350</td>
<td>13.430</td>
<td>36.386</td>
</tr>
<tr>
<td>1</td>
<td>5.94</td>
<td>2.197</td>
<td>20.528</td>
<td>55.742</td>
</tr>
</tbody>
</table>

4.2 Low Voltage Cascode Bridge Topology

The same simulations were run for the low voltage cascode bridge substituted in for the high voltage inverter configuration. The PMOS were sized at 6000 µm wide and 60 nm long while the NMOS were sized at 3000 µm wide and 60 nm long. The conduction loss due to PMOS and NMOS were roughly equal with this sizing. Again, the frequency was swept from 10 to 75 MHz for a 100 mA load and 3 V input voltage, and the resulting converter efficiency and loss mechanisms shown in Table 9. Similar to the buck with the inverter topology, efficiency decreases as frequency increases due to greater switching...
losses. One difference is that most of the switching loss in the cascode bridge case is due to overlap loss instead of gating loss as in the case of the inverter topology. Of the 8.42% efficiency drop, 5.49% of that can be attributed to an increase in overlap loss as switching frequency increases.

Table 9: Converter Efficiency for Cascode Topology across Frequency, 100 mA

<table>
<thead>
<tr>
<th>Freq (MHz)</th>
<th>Efficiency (%)</th>
<th>Conduction Loss (%)</th>
<th>Overlap loss (%)</th>
<th>Gating Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>89.59</td>
<td>6.991</td>
<td>0.000</td>
<td>0.250</td>
</tr>
<tr>
<td>40</td>
<td>86.40</td>
<td>5.752</td>
<td>3.010</td>
<td>0.820</td>
</tr>
<tr>
<td>75</td>
<td>81.17</td>
<td>6.025</td>
<td>5.490</td>
<td>1.450</td>
</tr>
</tbody>
</table>

The efficiency of the buck converter was then measured for different load currents, again at the two extremes of both power-on and standby modes. Current was swept from 1 to 100 mA and converter efficiency results shown in Table 10. In these simulations, the switching frequency was held at 40 MHz and input voltage at 3 V. At low loads in standby mode, switching loss, specifically overlap loss, is clearly the dominant loss mechanism. For higher loads, though, the overlap loss is in the same range as conduction loss and is a tolerable efficiency drop. At full load of 100 mA, the conduction loss for the cascode topology is nearly double that of the inverter topology for a given switch sizing. However, at low loads, gating loss can be as large as 12.25% and increasing switch width for lower conduction loss at high loads would result in a higher gating loss. Since overall converter efficiency at higher loads is still above 80%, the larger conduction loss for the cascode topology is acceptable.

Table 10: Converter Efficiency for Cascode Topology across Current Load, 40 MHz

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>Efficiency (%)</th>
<th>Conduction Loss (%)</th>
<th>Overlap loss (%)</th>
<th>Gating Loss (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>86.40</td>
<td>5.752</td>
<td>3.010</td>
<td>0.820</td>
</tr>
<tr>
<td>80</td>
<td>86.45</td>
<td>4.608</td>
<td>3.970</td>
<td>0.900</td>
</tr>
<tr>
<td>50</td>
<td>85.72</td>
<td>2.921</td>
<td>5.690</td>
<td>1.330</td>
</tr>
<tr>
<td>10</td>
<td>64.40</td>
<td>1.057</td>
<td>18.130</td>
<td>5.070</td>
</tr>
<tr>
<td>1</td>
<td>16.08</td>
<td>2.279</td>
<td>44.300</td>
<td>12.250</td>
</tr>
</tbody>
</table>
4.3 Topology Decision

At high loads, the efficiency for both topologies is above the desired 60% goal. At a low frequency of 10 MHz and 100 mA current load, the efficiency is comparable for both configurations at 88.73% for the inverter topology and 89.59% for the cascode. However, the efficiency drops much more quickly for the high voltage switches as frequency is increased. At 40 MHz, the high voltage buck converter has dropped to 78.55% and then to 68.40% at 75 MHz. The cascode topology has an efficiency of 81.17% at 75 MHz, 12.77% more efficient than using the high voltage switches. The lower efficiency at high frequencies for the inverter configuration, as previously mentioned, is due to gating loss. Gating loss can be reduced by decreasing the switch width. The tradeoff of reducing switch width is that conduction loss will be greater, thereby reducing the converter efficiency at lower frequencies. A comparison of the converter efficiency for switches 3000 μm wide and 5000 μm wide is shown in Figure 19. For the 3000 μm width, the decrease in efficiency is slower as the converter is run at a faster frequency, but the efficiency starts out lower at 10 MHz.

![Figure 19: Efficiency of Buck with Inverter Topology for Various Switch Widths](image-url)
One solution to the tradeoff in conduction and gating loss is to optimize the converter for a specific frequency. For a given frequency, the switches can be sized so that the combination of conduction and gating loss are a minimum. This method leaves no room for flexibility for different operation frequencies and does not solve the tradeoff problem if the customer requires a large range of operating frequency.

At low loads, both low voltage and high voltage switch implementations result in very low efficiencies, but for different reasons. The high voltage topology suffers from gating losses while the low voltage configuration suffers from high overlap loss. In the case of high gating loss at low loads, one possible solution would be to implement width switching. This technique uses two sets of inverters—one used for high loads and the other used during low loads when the AFE is on standby. The switches for high loads would have larger widths for lower conduction loss, since conduction loss can be significant for high currents. The other switch set would have much smaller widths for low loads during which conduction loss is insignificant and gating loss is dominant.

Another solution that addresses both gating and overlap loss is using a control method at low loads that reduces switching loss. For higher efficiency at light loads, previous research has used such control methods as pulse frequency modulation and burst mode control for lower switching loss.

In the end, the cascode bridge topology was chosen. For light loads, both configurations suffered from switching loss, which could either be alleviated by choosing a proper control method or in the case of the inverter topology, using smaller switches. The deciding factor was the performance of each topology at high loads when the AFE is powered on. The cascode bridge performed better at high loads with efficiency in the range of 81.17-89.59% across all frequencies. The inverter topology with 5000 μm wide switches had efficiency results of 68.40-88.73% where the efficiency at high frequencies is over 10% less efficient for the high voltage switch implementation. For 3000 μm switches, the lower end of that efficiency range increases to 76.24% but is still lower than the 81.17% of the cascode topology. Meanwhile, the high end of that efficiency range drops to 87.12%, also lower than the 89.59% of the cascode topology. The low voltage switch implementation allows high efficiency for a wide frequency range and does not requiring
optimizing switch width to a particular frequency, allowing greater flexibility for the customer.
Chapter 5: Control Schemes

The buck converter will operate in two distinct modes based on whether or not the AFE is powered on or on standby. As previously mentioned, when the AFE is on, the buck must supply a high load current, which implies that output power is higher and switching loss less significant. Pulse-width modulation was chosen as the control method for this high-load mode. In standby mode, output power is very low due to small load currents and switching loss, especially overlap loss, decreases the converter efficiency considerably. For this mode, burst mode control was implemented.

5.1 Pulse-Width Modulation

Pulse-width modulation (PWM) control is a commonly used control that is reliable and simple to implement for converters operating at higher loads. In PWM, the converter is run at a fixed frequency, and duty cycle is adjusted according to the output voltage. The output voltage is monitored and compared to a reference voltage. The voltage error is amplified through an error amplifier. The result is then compared to a ramp of the same frequency as the operating frequency. The output of the comparator is a square wave at the operating frequency with a duty cycle that is a function of the output voltage [1]. When the output voltage is above the reference, the duty cycle will be shortened so NMOS are conducting longer, and when it is below, the duty cycle will be lengthened so the PMOS switches are on for a longer duration. The PWM control method was chosen for high loads since efficiency was already high for the previous simulations run at a fixed frequency and duty cycle. PWM is fixed frequency control but with added tweaking of the duty cycle by monitoring the output voltage. PWM is also commonly used and has been proved to be an effective control method for buck converters.
The circuitry for PWM control includes an error amplifier, a comparator, and compensation components as shown in Figure 20. The buck converter was simulated with a PWM feedback loop. All PWM circuitry was modeled behaviorally. The feedback loop begins at the output of the buck converter. The output voltage connects to the error amplifier negative input via a 1.4 kΩ and 1 kΩ voltage divider. The positive input of the error amplifier is the 0.5 V voltage reference, and the amplifier has a gain of 50. Loop compensation is provided around the amplifier for converter stability. The output of the error amplifier is compared to a ramp function using a non-hysteretic comparator. The output voltage is fed back via an error amplifier to a comparator. The clock is level shifted to drive the power switches of the buck.

Figure 20: Buck with PWM Control
ramp rises from 0 to 1.5 V and repeats at the converter’s switching frequency. The comparator output is a $V_{dd}/3$ amplitude square wave with duty cycle dependent on the output voltage. It is then passed through a flip-flop to rid of any glitches that might have resulted from the comparator. The non-overlap clock generator produces the clocks for the PMOS and NMOS switches to prevent cross conduction. The clocks are then level-shifted to drive the gates of the power switches in the cascode bridge.

### 5.1.1 Compensation

A combination of capacitors and resistor are placed in a feedback loop around the error amplifier. These passives serve to compensate the buck converter loop and ensure stability. Without this compensation circuit, the loop has only a phase margin of 37°. For acceptable performance, a phase margin of at least 45° is preferred and a higher margin of 60° is even more desirable. The loop transfer function $\frac{v_{out}}{d(s)}$ is plotted in Figure 21. The gain at low frequencies is only 30 dB, so steady state errors may be high due to the low loop gain. The gain must be low in this non-compensated case in order to keep a decent phase margin and prevent too much ringing in the system.

The compensation that was used is shown in Figure 22. Without the added compensation, the transfer function is a second order system with two poles determined by the inductor and capacitor of the output filter, as given by Eq. 11 [1]. There is also a resulting zero from the series resistance of the output capacitance, which was set to 100 mΩ in simulation. In Eq. 11, $K$ is the constant factor in the transfer function that is a result of the voltage divider at the output, the error amplifier gain, and the PWM ramp equivalent gain.

$$ L(s) = \frac{v_{out}}{d(s)} = K \frac{sR_{ESR,C}C_o + 1}{s^2L_oC_o + s(R_{ESR,C} + R_{ESR,L})C_o + 1} \quad \text{Eq. 11} $$
The crossover frequency of the loop transfer function with no compensation, given in Eq. 11, is around 7.2 MHz with a phase margin of 37°. The low frequency gain is around 30 dB. This was determined with $R_{\text{vac}} = 100$ mΩ, $R_{\text{base}} = 100$ mΩ, $C_0 = 1$ µF, and $L_0 = 1$ µH.

With the additional compensation circuitry, the gain transfer function of only the error amplifier is given by Eq. 12.

$$\frac{V_e}{V_{\text{out}}} = \frac{s + 1/R_2C_2}{s + \left(\frac{C_1 + C_2}{R_2C_2C_1}\right)} \quad (\text{Eq. 12})$$

The loop transfer function is then shown in Eq. 13, where $K$ is now determined by the voltage divider at the output and the PWM ramp equivalent gain.
\[
L(s) = \frac{v_{out}(s)}{d(s)} = K \frac{s + 1/R_2 C_2}{s^2 + \frac{C_1 + C_2}{R_2 C_2} s + \frac{s R_{ESR,C} C_o + 1}{s + \frac{R_{ESR,L}}{P_{DC} C_o} + \frac{s R_{ESR,C} C_o + 1}{s}}}
\]  
(Eq. 13)

The compensation adds a zero at \(1/R_C\) and a pole at zero as well as at \((C + C)/R_C\). The pole at zero adds DC gain and minimizes steady state error. For good phase margin, the second pole must be at a high frequency past the 1 MHz of the second order output filter poles, and the zero should be near one decade below the 1 MHz poles to add phase margin before crossover occurs. The limitations on the values of the resistor and capacitors were that resistor values must be 100 kΩ or less and capacitor values 10 pF or less. The lowest frequency zero that could be achieved was then at 1 MHz. For a high frequency pole at 100 MHz, \(C\) was chosen to be 0.1 pF. The loop transfer function with compensation is shown in Figure 23. The crossover frequency is now a little higher than before at 16 MHz with a phase margin of 47°, a 10° increase. The zero from the output capacitor occurs at 10 MHz and boosts up the phase margin before crossover.

Additionally, the integrator from the compensator is seen as the transfer function slopes up in magnitude with lower frequency, allowing for a large low frequency gain.

![Figure 22: Error Amplifier with Compensation](image)

A feedback loop is placed around the error amplifier to compensate the loop transfer function of the buck converter and ensure stability.
5.2 Burst Mode

Several existing control methods aim to minimize switching and control loss when operating at light loads. One method of interest is operating the converter in burst or sleep mode [13]. In this technique, hysteretic comparison is used to determine when the output voltage is overdriven. When this occurs at light loads, all switches are turned off and put in "sleep" mode, so the output voltage is maintained only by the discharge of the output capacitor. When the output voltage drops below a threshold as monitored by the hysteretic comparator, the switch is turned back on for a brief period to recharge the capacitor with a "burst" of charge. The sleep mode allows for little conduction loss at light...
loads as well as little switching loss since the total amount of switching is greatly reduced due to the lack of switching during the sleep mode.

The circuitry for burst mode control uses fewer stages than PWM as can be seen in Figure 24. The main component is a hysteretic comparator that compares the output voltage to a reference. As in the PWM control, the output voltage is compared to a 0.5 V reference via a 1.4 kΩ and 1 kΩ voltage divider. However, now it is compared to the reference voltage using a hysteretic comparator rather than an error amplifier. The comparator has a 10 mV hysteresis band. When the divided output voltage is 10 mV below the 0.5 V reference, the comparator output transitions high, which will lead to switching the converter at a fixed frequency and duty cycle. When the voltage-divided output is 10 mV above the reference, the comparator output transitions low, which will lead to no switching at all so that the converter is now in “sleep” mode. The comparator output passes to digital logic, which is included in the feedback loop to determine when to clock the gates and when to turn off all the switches. At the digital logic, the comparator output is compared to level-shifted non-overlapping versions of the fixed frequency, fixed duty cycle clock. The output of the logic is then level-shifted to the appropriate voltage ranges.
Figure 24: Buck Converter with Burst Control
The output voltage is fed back via a hysteretic comparator. If the voltage input to the comparator reaches the top hysteresis band, the switches are turned off via logic gates, and if it reaches the bottom of the hysteresis band, the switches are driven by a 75% duty cycle clock.

5.2.1 Burst Mode Clock

The clock used to drive the switch gates in burst mode control is the same frequency as the AFE as in PWM control, but rather than controlling the duty cycle as in PWM mode, the duty cycle of the burst mode clock is fixed. In determining what duty cycle to choose for the clock, there was a tradeoff between conduction loss and switching loss. If duty cycle is too low, the amount of time to reach the top hysteresis band is longer, meaning the switches are clocked for a longer period of time and more switch transitions occur. A greater number of switch transitions leads to greater switching loss. However, if the duty cycle is too high, conduction loss will become significant. The drain-to-source
resistance of the PMOS switches is still higher than that of the NMOS despite the doubled width of the PMOS. If duty cycle is large, the PMOS are conducting for a longer portion of each period and since their $R_{DD}$ is higher than that of the NMOS, conduction loss increases. Switching loss, though, will decrease for high duty cycle since fewer switching transitions are necessary to boost the output voltage to the top hysteresis band when the switches are clocked. Clocks of 50%, 75% and 90% duty cycle were tested to determine the impact of duty cycle on the converter efficiency in burst mode. The results can be seen in Figure 25. For the higher load of 10 mA, at low frequencies, the 50% duty cycle clock gives the best efficiency, but as frequency increases, the 75% duty cycle clock gives the highest converter efficiency while the 50% and 90% clocks yield about the same efficiency. For very low loads of 1 mA, the 75% duty cycle clock dominates from 10 MHz to almost 60 MHz. Above 60 MHz, the 90% duty cycle clock gives a better efficiency. The 50% duty cycle clock yields the lowest efficiency across all frequencies.

![Effect of Clock Duty Cycle on Efficiency, 10 mA load](image)

![Effect of Clock Duty Cycle on Efficiency, 1 mA load](image)

Figure 25: Buck Converter Efficiency in Burst Mode for Different Duty Cycles
(a) Efficiency of the converter across frequency for duty cycles of 50%, 75%, and 90% at a load of 10 mA. (b) Efficiency of the converter across frequency for duty cycles of 50%, 75%, and 90% at a load of 1 mA.

At the higher 10 mA load and at lower switching frequency, conduction loss is much more significant than at higher frequencies or at lower loads. Hence, the 50% duty cycle clock results in better efficiency for this case. At lighter loads and higher switching frequency, switching loss is greater and switching less will improve efficiency. In this case, a higher
duty cycle is more desirable. The 75% duty cycle clock yielded the best overall efficiency across all frequencies and low load range and was chosen as the duty cycle for the switch-driving clocks.
Chapter 6: Summary of Results

The buck converter was simulated across three different parameters—frequency, current load, and input voltage. For loads of 50-100 mA, PWM control was used as the feedback control method, and for loads less than 10 mA, the burst mode control was implemented. Frequency was once again swept from 10 to 75 MHz, and current and frequency were swept for each input voltage of 2.5 V, 3 V, and 3.6 V.

6.1 AFE Power-On Mode Efficiency

To simulate the buck converter operation when the AFE is powered on, the buck was controlled using PWM for load currents ranging from 50 to 100 mA. The efficiency of the converter was found for 2.5 V, 3V, and 3.6 V input voltages running between 10 MHz and 75 MHz. The results are shown for the extremes of the high current load range in Figure 26. Efficiency is overall greater for the 50 mA load. At 50 mA, the conduction loss is a factor of 4 lower than at 100 mA, but output power is still large enough that switching loss is not a significant percentage of power loss.

Figure 26: Buck Efficiency across Frequency for High Loads, Varying Input Voltage
(a) Results are for simulations with a 100 mA load at input voltages of 2.5 V, 3 V, and 3.6 V. (b) Results are for simulations with a 50 mA load at input voltages of 2.5 V, 3 V, 3.6 V.
At maximum load of 100 mA, the efficiency is comparable for 3 V and 3.6 V input voltages. However, the 2.5 V input voltage yields an efficiency approximately 8-12% below that of the higher input voltages. This considerable difference in efficiency is due to a large conduction loss for low input voltages at high loads. As shown in Figure 27, as input voltage decreases, so does the magnitude of the gate-to-source voltages applied to the switches, since gate voltages are determined by dividing the input voltage in thirds. As an example, the voltages are shown at various nodes in Figure 27 when the PMOS switches are turned on. One disadvantage of the stacked topology is that the decrease in gate-to-source voltage is exacerbated for switches further from the input source due to the voltage drop across above switches. In the case of the 2.4 V input, the bottom PMOS is only driven with a $V_{sc}$ of 0.70 V. The $V_{thw}$ of the 65 nm NMOS and PMOS devices is +/- 410 mV and the actual magnitude of the threshold voltage is even higher. The CMOS switches are thus not being driven with a large enough $V_{gs}$ or $V_{sc}$ and suffer power loss due to high channel resistance. In the 2.25 V input case, the bottom PMOS has an even lower $V_{sc}$ and the switch no longer operates in strong inversion. With a lower differential voltage between source and gate, the PMOS switches have a larger drain-to-source resistance than for higher input voltages and higher $V_{sc}$, leading to large conduction losses, especially at high current loads. For a lower current load of 50 mA, the voltage drops across the switches is lessened so $V_{sc}$ is greater for M2 and M3 and $R_{ds}$ lower. At the same time, the current through the switches is halved so overall conduction loss is more than four times less than in the 100 mA load case. From Figure 26, it can be seen that all three input voltage simulations yield roughly the same efficiency for the 50 mA load, and the 2.5 V input voltage case for the 50 mA load has about a 10% increase in efficiency across all frequencies when compared to the 100 mA case.
For lower input voltages, the stacked configuration of the cascode bridge results in lower $V_{cs}$ for lower PMOS switches. The lower the $V_{cs}$, the larger the voltage drop, and thus power dissipation, across the switch.

The highest efficiency for the buck converter in AFE power-on mode is 93.63% for a 3.6 V input voltage, 50 mA load, and switched at 10 MHz. The lowest efficiency in this high current operation is 71.66% for a 2.5 V input, 100 mA load, and 75 MHz switching frequency. However, other than the 2.5 V input case at 100 mA load, the efficiency of the buck stays above 79% for all other scenarios, which is more than double the maximum efficiency of a 65 nm LDO.
6.2 AFE Standby Mode Efficiency

To simulate operation in AFE standby mode, the buck converter was simulated with burst mode control for current loads of 1-10 mA. As with previous simulations, the converter was tested with 2.5 V, 3 V, and 3.6 V input voltages at switching frequencies of 10-75 MHz. Efficiency results are shown in Figure 28. The efficiency is in the 70-80% range for 1-10 mA current loads rather than in the 80-90% range as it was for high loads. The efficiency across all frequencies and input voltages is 5-7% lower for the 1 mA load than for the 10 mA load.

Unlike at high loads, the lower supply voltage actually gives a better efficiency result at low loads. The stacked switches are no longer an issue since the current conducting across the switches is low and the voltage drop across the switches is small. For both the 10 mA and 1 mA cases, the 2.5 V input voltage yields the best efficiency while the 3.6 V input gives the lowest efficiency.

The highest efficiency in standby mode is 84.31% and occurs for a 2.5 V input voltage and 10 mA load at 10 MHz. The lowest efficiency occurs at 75 MHz switching frequency for a 3.6 V input voltage and 1 mA load, but it is still well above the 60% goal at a value of 67.13%.

![Figure 28: Buck Efficiency across Frequency for Low Loads, Varying Input Voltage](image)

(a) Results are for simulations with a 10 mA load at input voltages of 2.5 V, 3 V, and 3.6 V. (b) Results are for simulations with a 10 mA load at input voltages of 2.5 V, 3 V, 3.6 V.
6.3 Other Specifications

Aside from efficiency, other specifications included startup and settling time, output voltage ripple, output voltage transients, and output voltage steady-state error. The desired values for these specs are given in Table 11 along with the actual measured specs from simulations. The table shows the worst-case scenarios for each of the specifications. The correct output voltage was achieved for the full desired current load and frequency ranges at efficiencies greater than 67.13%. The full input voltage range was not achieved due to the stacked switch configuration of the cascode bridge. The input voltage could drop as low as 2.5 V and still achieve a decent efficiency, but below 2.4 V, the middle switches would begin operating in weak inversion due to low gate-to-source voltages. One solution to this disadvantage of the cascode bridge is at low input voltages, to bypass one of the PMOS and one of the NMOS switches so the cascode bridge essentially has only four operational switches instead of six. Dividing a low input voltage across two switches instead of three will allow for higher gate-to-source voltages across each switch.

Table 11: 65 nm DC/DC Converter Goals and Actual Performance

<table>
<thead>
<tr>
<th>Specification</th>
<th>Desired Spec</th>
<th>Actual Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin</td>
<td>2.25-3.6 V</td>
<td>2.5-3.6 V</td>
</tr>
<tr>
<td>Vout</td>
<td>1.2 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Iload</td>
<td>0-100 mA</td>
<td>1-100 mA (tested)</td>
</tr>
<tr>
<td>Fsw</td>
<td>10-75 MHz</td>
<td>10-75 MHz</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt; 60% (all loads, freq, Vin)</td>
<td>&gt; 67.13% (all loads, freq, Vin)</td>
</tr>
<tr>
<td>Startup Time</td>
<td>&lt; 0.1 ms</td>
<td>&lt; 6 µs</td>
</tr>
<tr>
<td>Settling Time</td>
<td>&lt; 1 µs</td>
<td>&lt; 1.63 µs</td>
</tr>
<tr>
<td>Vout ripple</td>
<td>&lt; 20 mV peak-to-peak</td>
<td>&lt; 25.2 mV peak-to-peak</td>
</tr>
<tr>
<td>Vout transient</td>
<td>&lt;</td>
<td>100mV</td>
</tr>
<tr>
<td>Vout SS error</td>
<td>&lt;</td>
<td>50mV</td>
</tr>
</tbody>
</table>

The desired startup time was exceeded in simulation, as was output voltage steady-state error and output voltage transients. Startup time and settling time were both measured as the time that it took the output voltage to settle within +/- 20 mV of the final output voltage value either at startup or after changes in load or input voltage. The output
voltage transient was measured as the maximum or minimum that the output voltage would go below or above its previous settled value when there was a step change in input voltage or load current.

The only specs that were not met in simulation were settling time and output voltage ripple. However, the settling time was less than 1 µs for all simulated cases of the buck except for the lowest switching frequency of 10 MHz. Output voltage ripple was also less than 20 mV p-p for all cases except for a 10 MHz switching frequency and 3.6 V input. Only in two simulation scenarios was the settling time slightly long and the output voltage ripple slightly high. Plots of simulation results can be seen in the Appendix as can a full table of results for each tested frequency, current load, and input voltage.
Chapter 7: Conclusion

From simulation results, a 65 nm buck converter is feasible for high efficiency if the proper topology and control are chosen. In designing the power supply for ADI’s digital camera AFEs, a cascode bridge topology was chosen and the converter controlled by PWM at high current loads of 50-100 mA and by burst mode at low currents of 1-10 mA. Efficiency was high between 67.13% and 93.63% across all input voltages and switching frequencies. A 65 nm LDO would have a maximum efficiency of only 33.33% to 48% for an input voltage range of 2.5 to 3.6 V. The 65 nm buck converter about doubles the efficiency range of its LDO counterpart.

Aside from efficiency, the 65 nm buck also meets specifications for low output voltage ripple, small output voltage steady state error, and fast settling at startup and after steps in input voltage or load current.

7.1 Further Research

One direction that would be worthwhile to pursue further is the elimination of external passives and the use of internal, on-chip inductors for the output filter. The on-chip inductor was scrapped in this project due to both lower efficiency and size constraints. However, the selection of the on-chip inductor in this project was limited by what was available at ADI in 65 nm. In recent layers, new on-chip inductor designs beyond the standard spiral inductor have been studied for both lower series resistance and smaller chip area. One proposed structure for a lower series resistance inductor is to create a series of trenches [14]. Each row of trenches is physically out-of-phase with the neighboring row, and each one is connected to the next by a wide link for a low resistance path. The current flow is in the opposite direction for each row of trenches so that magnetic flux is parallel to the substrate as opposed to perpendicular as in spiral inductors. Eddy currents, which cause power dissipation across the inductor, are thus avoided. The trenches are then filled with a magnetic material to increase the inductance while maintaining a low series resistance.
Another possible topology is the multi-layer inductor. Multi-layer inductors have been explored as an alternative to planar spiral inductors for a reduction in chip area [15]. The multi-layer inductor is a 3-D inductor that splits up the spiral inductor into a fewer number of turns but spread down through multiple metal layers. By stacking a smaller spiral in each metal layer, the total chip area is much smaller than for a spiral inductor. Additionally, mutual inductance between spirals of different layers adds to the total inductance of the on-chip inductor [16].

The thesis focus was on maximizing efficiency of the 65 nm buck converter, but a tradeoff of switching converters is addition of switching noise and EMI. The switching noise of the converter can be seen in the simulation plots at the input source $V_{dd}$. It is unclear what the affect of this noise will be on the AFE without simulating the AFE and buck power supply together. One advantage, though, of using the same frequency clock for both AFE and power supply is previous designs for the AFE already take measures to reduce noise that is at the same frequency as the clock. As for EMI noise, LDOs have no magnetic components unlike switching converters so EMI is not an issue for linear regulators. EMI and its effect on the AFE operation should be tested on a fabricated buck converter.

After exploring different topologies and control methods, a 65 nm buck converter is a promising improvement to a 65 nm LDO, and even to a 0.18$\mu$m LDO in some modes of operation, in terms of efficiency. However, further research can be done to explore how switching noise and EMI, two disadvantages of a switching converter, will affect the operation of the AFE.
## Appendix

**Frequency = 10 MHz**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Efficiency</th>
<th>Vout SS Error</th>
<th>Vout Ripple</th>
<th>Vout Load Step</th>
<th>Transient Settling Time</th>
<th>Startup Time</th>
<th>Startup Transient</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 V, 100 mA</td>
<td>91.05</td>
<td>-0.000</td>
<td>0.0135</td>
<td>1.471</td>
<td>5.914</td>
<td>1.839</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3 V, 50 mA</td>
<td>93.45</td>
<td>0.001</td>
<td>0.0195</td>
<td>1.158</td>
<td>1.465</td>
<td>5.607</td>
<td>1.919</td>
<td></td>
</tr>
<tr>
<td>3 V, 1 mA</td>
<td>74.19</td>
<td>-0.007</td>
<td>0.0615</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>1.356</td>
<td>1.286</td>
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<tr>
<td>3.6 V, 100 mA</td>
<td>90.64</td>
<td>-0.006</td>
<td>0.0126</td>
<td>1.621</td>
<td>5.971</td>
<td>2.270</td>
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<td></td>
</tr>
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<td>3.6 V, 50 mA</td>
<td>93.29</td>
<td>0.007</td>
<td>0.0160</td>
<td>1.169</td>
<td>1.607</td>
<td>5.570</td>
<td>2.390</td>
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<tr>
<td>3.6 V, 1 mA</td>
<td>72.34</td>
<td>-0.011</td>
<td>0.0629</td>
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<td>No</td>
<td>N/A</td>
<td>1.714</td>
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<td>2.5 V, 100 mA</td>
<td>83.59</td>
<td>0.019</td>
<td>0.0084</td>
<td>0.476</td>
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<td>0.013</td>
<td>0.0088</td>
<td>1.226</td>
<td>1.144</td>
<td>6.014</td>
<td>1.617</td>
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<tr>
<td>2.5 V, 1 mA</td>
<td>72.74</td>
<td>-0.006</td>
<td>0.0656</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>2.545</td>
<td>1.265</td>
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<tr>
<td>3.6 V, 100 mA</td>
<td>88.17</td>
<td>-0.006</td>
<td>0.0201</td>
<td>0.862</td>
<td>4.851</td>
<td>2.248</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.6 V, 50 mA</td>
<td>86.14</td>
<td>-0.009</td>
<td>0.0202</td>
<td>1.242</td>
<td>1.175</td>
<td>4.816</td>
<td>2.348</td>
<td></td>
</tr>
<tr>
<td>3.6 V, 1 mA</td>
<td>76.81</td>
<td>-0.011</td>
<td>0.0684</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
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<td>1.370</td>
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<tr>
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<td>0.0014</td>
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<td>1.444</td>
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<tr>
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<td>0.012</td>
<td>0.0015</td>
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<td>1.147</td>
<td>5.302</td>
<td>1.587</td>
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</tr>
<tr>
<td>2.5 V, 1 mA</td>
<td>74.08</td>
<td>-0.002</td>
<td>0.0552</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>2.700</td>
<td>1.258</td>
</tr>
</tbody>
</table>

**Frequency = 40 MHz**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Efficiency</th>
<th>Vout SS Error</th>
<th>Vout Ripple</th>
<th>Vout Load Step</th>
<th>Transient Settling Time</th>
<th>Startup Time</th>
<th>Startup Transient</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 V, 100 mA</td>
<td>87.50</td>
<td>0.001</td>
<td>0.0018</td>
<td>0.550</td>
<td>5.052</td>
<td>1.805</td>
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<tr>
<td>3 V, 50 mA</td>
<td>86.13</td>
<td>-0.004</td>
<td>0.0168</td>
<td>1.163</td>
<td>0.716</td>
<td>5.027</td>
<td>1.892</td>
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<tr>
<td>3 V, 1 mA</td>
<td>72.74</td>
<td>-0.006</td>
<td>0.0656</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>2.545</td>
<td>1.265</td>
</tr>
<tr>
<td>3.6 V, 100 mA</td>
<td>88.17</td>
<td>-0.006</td>
<td>0.0201</td>
<td>0.862</td>
<td>4.851</td>
<td>2.248</td>
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<tr>
<td>3.6 V, 50 mA</td>
<td>86.14</td>
<td>-0.009</td>
<td>0.0202</td>
<td>1.242</td>
<td>1.175</td>
<td>4.816</td>
<td>2.348</td>
<td></td>
</tr>
<tr>
<td>3.6 V, 1 mA</td>
<td>76.81</td>
<td>-0.011</td>
<td>0.0684</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>1.621</td>
<td>1.370</td>
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<td>2.5 V, 100 mA</td>
<td>79.78</td>
<td>0.020</td>
<td>0.0014</td>
<td>0.313</td>
<td>5.667</td>
<td>1.444</td>
<td></td>
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<tr>
<td>2.5 V, 50 mA</td>
<td>87.66</td>
<td>0.012</td>
<td>0.0015</td>
<td>1.225</td>
<td>1.147</td>
<td>5.302</td>
<td>1.587</td>
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</tr>
<tr>
<td>2.5 V, 1 mA</td>
<td>74.08</td>
<td>-0.002</td>
<td>0.0552</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>2.700</td>
<td>1.258</td>
</tr>
</tbody>
</table>

**Frequency = 75 MHz**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
<th>Efficiency</th>
<th>Vout SS Error</th>
<th>Vout Ripple</th>
<th>Vout Load Step</th>
<th>Transient Settling Time</th>
<th>Startup Time</th>
<th>Startup Transient</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 V, 100 mA</td>
<td>63.27</td>
<td>-0.001</td>
<td>0.0009</td>
<td>0.896</td>
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<td>1.816</td>
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<td>1.166</td>
<td>0.570</td>
<td>4.880</td>
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<tr>
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<td>-0.004</td>
<td>0.0615</td>
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<td>No</td>
<td>N/A</td>
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<tr>
<td>3.6 V, 100 mA</td>
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<td>0.0011</td>
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<tr>
<td>3.6 V, 50 mA</td>
<td>79.13</td>
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<td>0.0011</td>
<td>1.244</td>
<td>0.836</td>
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<td>No</td>
<td>N/A</td>
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<td>1.447</td>
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</tr>
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<td>82.23</td>
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<td>0.0009</td>
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<td>5.214</td>
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<tr>
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<td>0.0552</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>1.256</td>
<td>1.243</td>
</tr>
<tr>
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<td>-0.001</td>
<td>0.0549</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
<td>2.185</td>
<td>1.247</td>
</tr>
</tbody>
</table>
65nm DC/DC Converter with PWM control
Vin steps from 3.6V to 2.5V
100 mA load
40 MHz
65nm DC/DC Converter with PWM control
Vin = 3V
Load steps between 50 mA and 100 mA
65nm DC/DC Converter with Hysteresis control
Vin steps between 2.5 and 3.6 V
Load = 10 mA
40 MHz

V(out)
1.5
1
.5
0
15
i(v-test)
x1e-3
5
10
0
-5
200
i(10)
x1e-3
160
120
80
40
0
-40
V(vx)
2
0
-2
V(vdd)
4
3
2
1
0 2 4 6 8 10 12 14 16 18 20 22 24 26
time, x1e-6 Seconds
65nm DC/DC Converter with Hysteretic control
Vin = 3 V
Load steps between 1 mA and 10 mA
40 MHz

74
References


