

Package and PCB Solutions for High-Speed Data Link Applications

by
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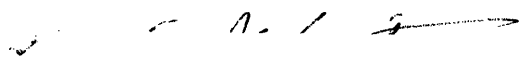
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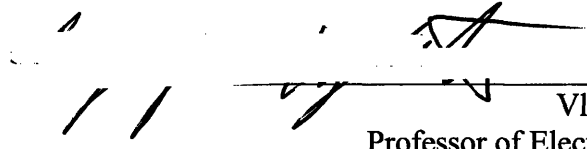
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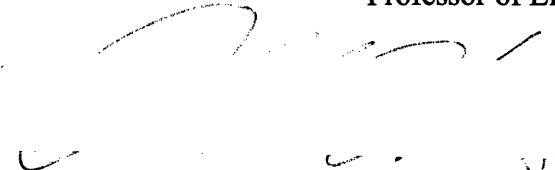
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ABSTRACT

Continual increase in high-speed transfer rates is essential in today's world in order to keep up with Moor's law scaling and to meet application demands. This increase in information transfer rates is essentially limited by the bandwidth of the communication channel. Channel loss, signal crosstalk, and power integrity are the important factors affecting the bandwidth of the channel and must be fully understood when designing such high-speed links. Moreover, channel performance optimization requires system level analysis with co-design of different channel components in order to approach the maximum capacity of a channel. In this thesis, we focus on the essential aspects of high-speed channel design with an emphasis on the design of the package area. A technique for reducing discontinuities in the package is introduced, studied, and simulated on IBM package designs to obtain improved package performance. The critical Plated-Through-Hole (PTH) via region at the package and Printed Circuit Board (PCB) interface is also analyzed in a co-study to suggest design rules for overall improved system performance.

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Dedication

To my mom, my dad, my two sisters, and my brother

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Chapter 1 : Introduction

Higher bandwidth has become more important than ever in today's computing systems. Personal computers, routers, switches, and game consoles all require higher bandwidth to meet the increasing performance demand of new applications. Moreover, the continuous scaling of integrated circuit technology, confirming Moore's prediction, over the recent years has resulted in massive computational capacity and hence data processing capability which in turn has created the demand for high-speed communication across different components in a system [1]. These systems extend to optical communication networks spanning across the globe, but all come down to chip-to-chip communication in a single board [2-4]. The massive flux of information in and out of the chip has caused simple input/output (I/O) drivers to be replaced with sophisticated high-speed circuits which in turn depend on reliable high bandwidth channels.

Channel design, which was conveniently and justifiably ignored at lower frequencies, has become a major bottleneck for high-speed communication [5]. The increase in data rates to the tens of Giga bits per second (Gbps) region has prompted more careful signal integrity considerations in the design of the channel from the transmitter of one chip to the receiver on the next [6]. The decrease in wavelength size due to higher frequency signaling has caused the once short electrical lengths of different components to become significant due to transmission line delays, loss and signal coupling in these components [7].

Different channel components are traditionally designed separately with the goal of optimizing each component in isolation, assuming overall channel performance improvement. Modern work in high-speed channel design, however, requires an overall system analysis to quantify component level improvements as we show in this thesis.

This thesis presents an in depth analysis of different bottleneck areas in high-speed channel design with a focus on the package (substrate) and PCB regions. A technique for reducing inherent discontinuities at the package level is studied and performance

improvement is obtained at relatively low cost. In addition, the critical region of package and PCB interface is analyzed and system level simulations are performed, in time and frequency domain, in order to allow for better design rules for package and PCB design.

Chapter 2 provides an overview of the structure of a typical high-speed channel and the different components which constitute the channel in a chip-to-chip application. The different causes impacting signal integrity in high-speed channels is outlined in Chapter 3, providing the theoretical challenges faced in high-speed channel design. The effects of signal losses, reflection, crosstalk and power integrity on signal integrity is described to provide the fundamentals for the work in this thesis.

As a step towards package performance enhancement, a concept of discontinuity cancellation for package design is presented in Chapter 4 and is rigorously analyzed with 3D electromagnetic structure simulations which are modeled based on IBM package offerings to quantify performance improvements seen both at the package and channel level along with the impact on the channel bandwidth.

It is recognized that isolated package design cannot be the solution to overall optimized channel performance nor the effective way of obtaining minimized cost for performance and thus a package-board co-study is performed at the critical area of Printed Circuit Board (PCB) Plated-Through-Hole (PTH) via design. Chapter 5 outlines the methods used for this study and the impact on both component level and more importantly system level performance. Different tools are used to quantify this performance impact in high-speed channels both in the time-domain and in the frequency domain.

Chapter 6 concludes this work with the key understandings obtained from this work that can be used to achieve better performance/cost optimized design rules for high-speed package design. Chapter 7 provides an outline for future work in this area.

Chapter 2 : Background

Due to the density constraint on the number of wires between chips in chip-to-chip communication and the increased demand for higher flow of information, blocks of parallel data are serialized and transmitted off chip using high-speed links by utilizing Serialize/Deserialize circuitry. A general structure of a high-speed serial link is given in Figure 2.1. The channel can contain different components such as the package, connector, PCB, and possibly the socket.

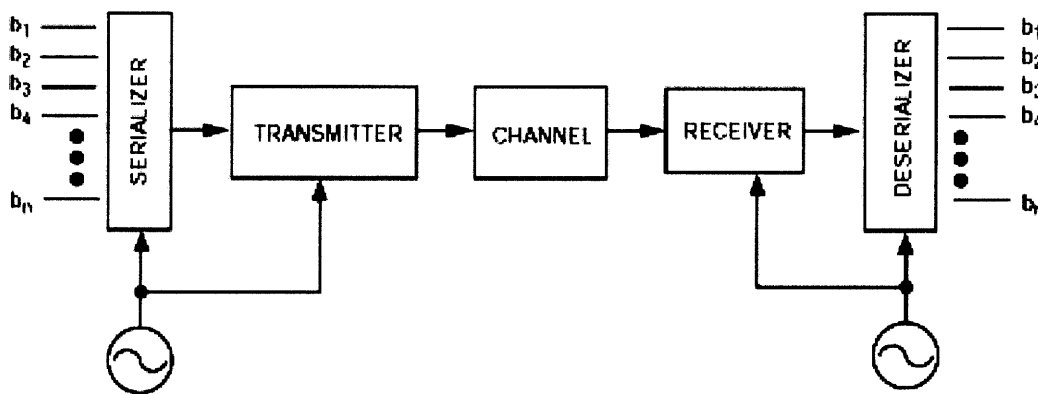


Figure 2.1: Diagram of a high-speed serial link

The use of these high-speed links has become ubiquitous today. Around eighty percent of Application Specific Integrated Circuits (ASIC) produced by IBM Microelectronics today contain High-Speed SerDes (HSS) links. SerDes, which stands for serializer/deserializer, is a circuit technique for rapid transmission of high-speed data [8]. In the past few years we have witnessed a rapid increase in data transmission rates over different processing technologies.

At this stage, the bottleneck in achieving higher HSS signaling rates lies in the limitation of channel bandwidth [9]. In order to address this bandwidth limitation, several designs started to use transmit pre-emphasis to compensate for the low-pass nature of the channel [10-12]. Four-level signaling has also been considered as another solution, instead

of binary NRZ signaling, to increase the data rates without increasing the signaling rate beyond the channel limit [13, 14]. However, such sophisticated equalization and modulation techniques increase link cost and limit the achievable bandwidth since this complexity comes with significantly larger power requirements. Thus improving channel performance with simple solutions can keep the cost of the link low while simplifying the link circuits and improving their energy-efficiency. For these reasons, this thesis focuses on solutions to maximizing channel efficiency while keeping the link complexity at a minimum.

The channel bandwidth limitation is highly dependent on the channel design, structure as well as channel length in the application space. The materials used, the component physical structure, signal coupling due to compact routing, and power integrity are all important factors which directly and indirectly impact the bandwidth of the channel. In order to improve the band-limited channel, we thus need to look at the structure of the channel as well as the mechanism that produces this limitation.

A typical backplane system depicting the different sections of the signaling path in a backplane communication channel is displayed in Figure 2.2. The typical channel consists of transmitter and receiver chips, the packages for the chips, connectors, and mother board traces. The subsequent sections expand upon each of these components.

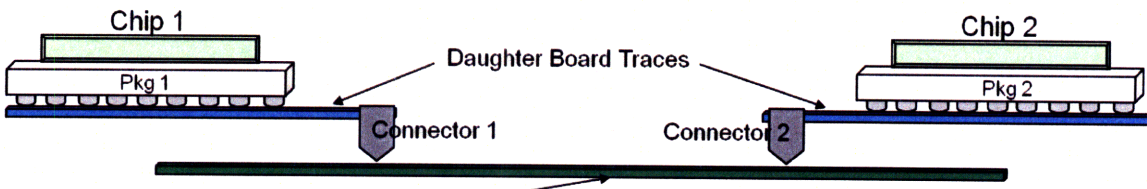


Figure 2.2: Typical backplane communication channel indicating the different sections of the signaling path

2.1 Chip

The chip consists of the silicon circuitry as well as the metal layers for signal and power redistribution. High-speed transceivers with potential sophisticated channel equalization circuitry reside in the chip. Channel equalization can compensate frequency-

dependant loss and dispersion of long traces in boards and packages as well as dispersion due to device loadings [15, 16]. Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE) are two commonly employed equalization techniques in the design of the transceiver, in order to flatten the channel frequency response [17].

The aggregate termination impedance becomes frequency selective because of parasitic capacitance and does not match the transmission line characteristic impedance of 50 Ohms at all frequencies. Electrostatic Discharge (ESD) protection circuitry is a major source of this parasitic capacitance which if not accounted for can be a source for signal degradation [18].

2.2 Package

The package is the holder of the chip and is essentially a space transformer between the chip and the motherboard. It provides the mechanical, thermal, and electrical connections necessary to properly interface the circuits in the chip to the rest of the system. The physical attributes of a package can be divided into three categories: the attachment of the die (chip) to the package, the on-package connections, and the attachment of the package to the PCB [19].

2.2.1 Attachment of the Die to the Package

Figure 2.3 depicts the two most common methods of die attachment: wire bond attachment and flip chip attachment. Wire bond is cheaper than flip chip but is limited in its performance due to the increased amount of parasitic impedance it introduces. A wire bond is a very small wire with a diameter on the order of 1 mil (diameter of a human hair is about 3mils, where one mil is a milli-inch). The primary impact of the bond wire is its added series inductance. The length of a bond wire is on the order of 100mils, which is significant at the operating frequencies and thus produces transmission line behavior. In addition, wire bonds also exhibit large amount of crosstalk, which limit the proximity of signal nets to each other on the wire bonds and thus the number of I/Os that a wire bond package can provide [20, 21].

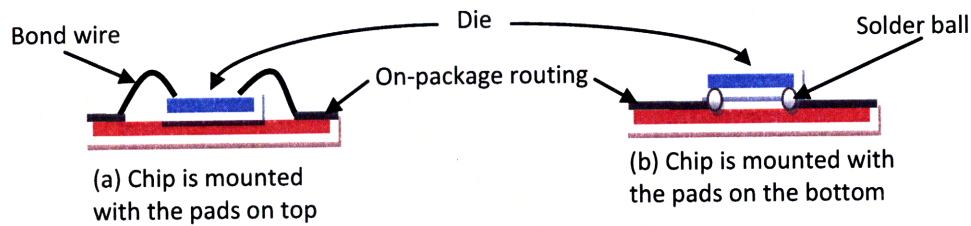


Figure 2.3: Common Methods of die attachment: (a) wire bond attachment; (b) flip chip attachment.

Flip-chip packaging, on the other hand, is almost ideal from an electrical perspective. As depicted in Figure 2.3, a flip-chip connection is obtained by placing small balls of solder on the pads of the die and then placing the die upside down on the package substrate. The series inductance of the flip-chip connection is on the order of 0.1 nH, which is an order of magnitude less than that of a typical wire bond [19]. Other advantages are that the effect of crosstalk in the solder balls (also called Controlled-Collapsed-Chip-Connector or C4) is minimal, and the I/O count on the flip-chip package is larger due to the fact that the solder ball connections can potentially be placed over the entire die, not just on the periphery.

Thermally and mechanically, however, flip-chip packaging is dismal. The thermal coefficient of expansion must be similar between the die and the substrate so that heating of the chip doesn't cause the solder balls to be strained. In addition, cooling of the chip is more challenging and requires costly methods since the whole side of the die is covered with solder balls and this reduces heat transfer. For these reasons, flip-chip packaging is more costly and is mainly used for high performance applications.

2.2.2 Routing of the Signals on the Package

The routing of the signals in the package can be done in a controlled or non-controlled impedance fashion. High-speed digital designs require the use of controlled impedance packaging and this is the type we are concerned with in this thesis. A controlled impedance package typically resembles a miniature PCB with different layers and power and ground planes with the die placed at the center. Both wire bond and flip-chip connections can be

used to connect the die for routing through the package. Small dimensioned transmission lines are used to route the signals from the bond pad on the package to the board attachment. The different layers are connected through buried, blind, and plated-through-hole vias for signal routing as well as for power delivery. Controlled impedance routing requires careful design for maximum signal transmission and minimum coupling between signal nets. Power delivery through the package also requires minimum inductance to reduce switching noise.

2.2.3 Attachment of the Package to the Board

Similar to the attachment of the die to the package, there are a variety of methods to connect the package to the PCB. The most common method used in ASIC packaging is the Ball Grid Array (BGA) method which is essentially a larger version of flip-chip. The BGA descended from the older Pin Grid Array (PGA) connection type. Land Grid Array (LGA) has also recently gained some ground with most of Intel's current processors being mounted using LGA. LGA uses pads of bare gold-plated copper to connect the package to the socket on the PCB.

2.3 Connector

Connectors are devices that are used to connect one PCB board to another. An example of a high-speed connector is the slot connector used to connect the Pentium III processor to the motherboard. Despite their relatively shorter electrical lengths, connectors contribute significantly to the loss in a high-speed channel. The primary electrical factors affecting high-speed performance in connectors are: [22]

- 1 Mutual inductance – causes crosstalk
- 2 Series inductance – slows down signal propagation and creates electromagnetic interference (EMI)
- 3 Parasitic capacitance – Slows down signal propagation

2.4 Printed Circuit Board (PCB)

A printed circuit board is used to mechanically support and electrically connect electronic components using conductive pathways, or traces. These traces are etched from copper sheets laminated onto a non-conductive substrate. PCBs are rugged, inexpensive, and can be highly reliable.

The typical PCB stackup consists of alternating layers of core and prepregs (short for pre-impregnated). A core layer is a thin piece of dielectric with copper foil bonded to both sides. The core dielectric is cured fiberglass-epoxy resin. Prepeg layers are uncured fiberglass-epoxy resin which cure (i.e. harden) when heated and pressed. The most common, widely available, and relatively low cost dielectric material used in the PCB industry is FR-4 (woven glass and epoxy).

PCB traces are used for high-frequency connections within a single PCB and on backplanes connecting one or more PCBs. The traces in the PCB are generally either microstrip or stripline. Microstrip traces have a solid reference plane on one side while striplines lie between two solid reference planes, as shown in Figure 1.5.

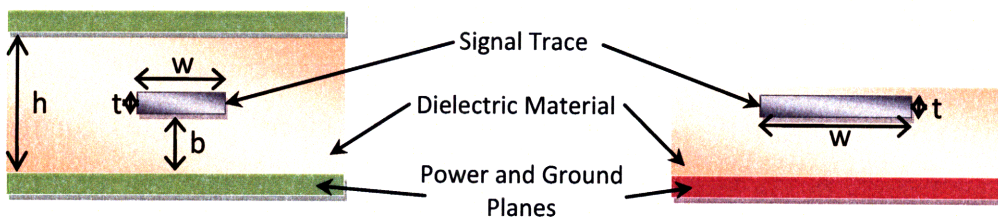


Figure 2.4: Cross-section of PCB trace configurations defined by parameters w , t , h , and b : Stripline (left), Microstrip (right)

A major piece of the transmission path through a PCB that has a dominant effect on high-speed signals is the Plated-Through-Hole (PTH) via. PTH vias are means of transporting signals into interior layers of a multi layer PC board. Depending on how the signal is routed through the PTH via, the PTH can become very 'visible' to signals with increased frequency content. The major source of impedance discontinuity in the PTH via occurs when the signal

is routed through the via in such a way that a portion of the via is not used for signal transmission. This extra portion of the via is sometimes called the 'via stub'. Back drilling is a technique used to remove this extra via stub, but is expensive and avoided in low cost applications thus forgoing signal integrity at higher frequencies.

Chapter 5 will present an in depth analysis of the effect of the PTH via and via stub on signal transmission and signal coupling in the PCB. The analysis is based on 3D electromagnetic field simulations of 3 differential signal nets in the PCB via escape region. In order to fully appreciate the simulation results, in the following chapter we will discuss the physical effects that cause degradation of signal integrity.

Chapter 3 : Signal Integrity of High-Speed links

In order to improve the performance of high-speed links, we must have a good understanding of the physical effects that cause the signal degradation we wish to avoid. In this chapter, we present the challenges of attaining signal integrity at higher frequencies in general interconnects. These tools will be used in our analysis of key performance limiting areas in the chip-to-chip high-speed channel design in subsequent chapters.

Higher signaling rates and faster edge rates or rise times (defined as the time required for the signal to change from %10 to %90 of its final level) require increased high frequency content transmission through the channel. Given this high frequency content, the channels can no longer be considered as ideal interconnects and frequency dependant losses and signal interference must be taken into account.

The signal integrity challenges can be divided into the four categories of signal loss, reflection, crosstalk, and power integrity issues. Signal loss and reflections will prevent the transmitted signal from reaching its destination with full power while crosstalk and power supply noise can cause the received signal to become noisy and unreliable.

3.1 Transmission Line Losses

As the frequency of operation increases, and the wavelength ($\lambda=c/f$, c is the speed of light, f is the frequency of operation) of the highest frequency component of the signal approaches the circuit's physical size, the signal travelling through the interconnect is no longer a simple digital signal going through a lumped Resistor Capacitor (RC) network, it begins to behave like a wave propagating along a transmission line. Transmission line behavior typically starts to appear when physicals lengths of the components are larger than one hundredth the length of the wavelength. This transmission line is modeled as a

distributed series of inductors, capacitors, and resistors. The transmission line is defined by its characteristic impedance, propagation delay and losses [23].

In modern interconnects smaller dimensions and high-frequency content cause the resistive losses in the transmission line to intensify and become ever more important. Resistive losses affect the performance of the digital system by decreasing the signal amplitude, thus affecting noise margins and slowing edge rates, which in turn affects timing margins. We thus consider both the frequency dependant and frequency independent losses of the transmission line.

3.1.1 Conductor DC Losses

The conductor DC loss is essentially the resistive component of transmission lines which is due to conductors not being perfect conductors. Based on this, the DC loss depends primarily on two factors: the resistivity of the conductor and the total area in which the current is flowing. The resistive loss is given by

$$R = \frac{\rho L}{A} = \frac{\rho L}{Wt} \quad (3.1)$$

where R, in ohms (Ω), is the total resistance of the line, ρ is the resistivity of the conductor material in ohm-meters, L the length of the line, W the width, t the thickness, and A the cross-sectional area of the signal conductor.

3.1.2 Dielectric DC Losses

Dielectric materials used in different components of the channel are not perfect insulators and thus there is a DC loss associated with the resistive drop across the dielectric material between the signal conductor and the reference plane. The dielectric dc loss is, however, negligible for conventional dielectrics and can thus be ignored [19].

3.1.3 Frequency-Dependant Conductor Losses

At low frequencies the DC loss is sufficient for accurate system simulation; however, as the frequency increases other phenomena that vary with the spectral content of the

digital signals begin to dominate. The most prominent of these frequency-dependant variables is the *skin effect*.

3.1.3.1 Frequency-Dependant Resistance and Inductance

Skin effect manifests itself primarily as resistance and inductance variations. At higher frequencies, the current tends to flow closer to the surface of the conductors instead of flowing uniformly throughout the conductor cross section. The measure of the distance over which the current falls to 1/e of its original value is termed the *skin depth* [23]. The skin depth delta is calculated with the equation

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi F\mu}} \text{ meters} \quad (3.2)$$

where ρ is the resistivity of the metal, ω the angular frequency ($2\pi F$), and μ the permeability of free space (in henries per meter). From equation 3.2 it can be seen that as the frequency increases, the current will be confined to a smaller area, which will increase the resistance, as seen in the DC resistance equation 3.1.

The total inductance of a conductor is caused by magnetic flux produced by the current. The total inductance can be divided into internal inductance caused by current flowing through the center of the wire and external inductance caused by the current flowing through the skin depth of the conductor. At high frequencies the internal inductance approaches zero as the current through the center of the wire disappears. Thus for high-speed digital systems, internal inductance is safely ignored and the external inductance is used as the conductor inductance.

3.1.3.2 Effect of Conductor Surface Roughness

In reality, due to manufacturing limitations, metal surfaces are rough and this effectively increases the resistance of the material especially at higher frequencies when the mean surface roughness is a significant percentage of the skin depth. It has been empirically shown that surface roughness can account for up to 10-50% increase in loss

compared to the ideal smooth surface case [19]. Figure 3.1 is a cross section of a stripline displaying surface roughness. In this particular case the surface roughness on the top of the conductor is approximately 0.2mils (5 μm).

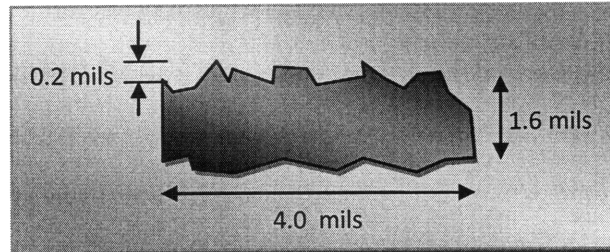


Figure 3.1: Cross section of a stripline in a typical PCB, showing surface roughness.

The roughness of the conductor is dubbed as the *tooth structure* and the magnitude of the surface variations is described as *tooth size*. For example, the measured tooth size in Figure 3.1 is 5 μm . PCB vendors indicate that typical FR4 boards have a tooth size of 4 to 7 μm .

3.1.4 Frequency-Dependant Dielectric Losses

When a time-varying electric field is impressed onto a material, any molecules in the material that are polar in nature will tend to align in the direction opposite that of the applied field. This is termed *electric polarization*. The classical model for dielectric losses, which was inspired by experimental measurement, involves an oscillating system of molecular particles, in which the response to the applied electric fields involves damping mechanisms that change with frequency [24]. Any frequency variations in the dielectric loss are caused by these mechanisms.

Frequency-dependant dielectric loss increases linearly with signal frequency:

$$\alpha_D = \pi \frac{\sqrt{\epsilon_r}}{c} f \tan \delta \quad (3.3)$$

where $\tan \delta$ is the loss tangent, c is the speed of light and ϵ_r is the relative permittivity [22].

Dielectric loss is typically specified with the loss tangent which strongly depends on the type of insulator material. Table 3.1 shows the loss tangent for some typical PCB insulators.

Table 3.1: Loss Tangent for Typical PCB insulator.

Material	FR4	Polyamide	GETEK	Rogers4350	Teflon
Loss Tangent	0.035	0.025	0.01	0.004	0.001

Most legacy backplanes use FR4 material, which has the highest loss tangent. Newer and higher performance backplanes use either Rogers or one of the NELCO materials with lower loss.

The linear dependence of dielectric loss to frequency causes it to dominate over the skin-effect at very high frequencies. The crossover frequency of skin effect and dielectric loss depends on the material properties and dimensions of the trace. Both effects are illustrated in Figure 3.2 for an FR4 material.

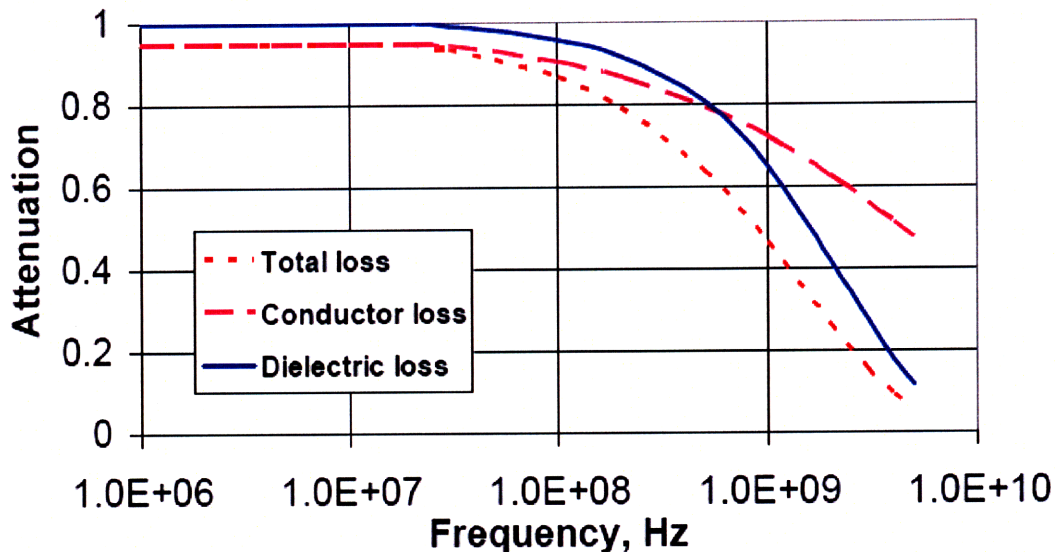


Figure 3.2: Crossover between skin-effect and dielectric loss, FR4 8 mil wide and 1 m long 50 ohm stripline [25]

3.2 Reflections (Impedance Discontinuities and Stubs)

When a light wave passes to a medium different from the original one, some of the signal gets reflected back to the original medium due to the difference in the refractive indexes of the two mediums. The same behavior occurs with EM waves passing from one material to a different one, some of the incident wave's energy passes through the line but the remaining portion is reflected. The amount of reflection depends on the characteristic impedance of the transmission line. The characteristic impedance of a lossy transmission line is given by:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + i\omega C}} \text{ Ohms} \quad (3.4)$$

where R is the series resistance of the inductor, G is the parallel conductance of the capacitor, and ω is the radial frequency. The reflection coefficient is thus dependent on frequency when R and G are not significantly small to ignore.

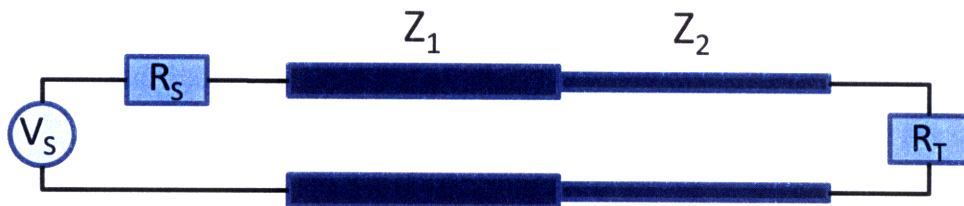


Figure 3.3: Transmission line system with multiple line impedance.

If the characteristic impedance of the transmission line matches that of the load or source, the incident wave is delivered without reflection. Otherwise the mismatch in characteristic impedance will cause reflections at the mismatch boundary. The *Reflection Coefficient* describes the amount of reflection at the boundary where the characteristic impedance seen by a traveling wave changes causing an impedance discontinuity. For example, the reflection coefficient at the junction of two transmission line segments with impedances Z_1 and Z_2 , as seen in Figure 3.3, is given by:

$$\Gamma = \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad (3.5)$$

Characteristic impedances of different components are designed to a consistent value when possible (typically 50 ohms is used for single ended traces and 100 ohm for differential traces). However, manufacturing variability in the fabrication of the traces results in variation in characteristic impedance which is beyond the designer's control. In addition, the unavoidable impedances of the certain components in the channel produce potentially large impedance discontinuities in the interconnect structure that can severely degrade performance.

Other sources of reflections are via stubs which have stronger frequency dependence. Here the stub acts as a capacitor which reflects high frequency energy. Back-drilling the via stub can help alleviate this problem in high performance designs but is not desirable for low cost applications.

3.3 Crosstalk (*FEXT, NEXT*)

The coupling of energy from one line to another called crosstalk occurs when the electromagnetic fields from different signal nets interact. Crosstalk is very widespread in digital designs, occurring on the chip, the PCB board, connectors, the chip package, and on cables with the strongest crosstalk occurring between the signal lines in chip packages and connectors [26]. Moreover, as applications demand physically smaller and faster products, the amount of crosstalk in digital systems is increasing dramatically.

Excessive line to line coupling, or crosstalk, can have two detrimental effects: First, crosstalk will induce noise onto other lines, which may further degrade the signal integrity and reduce noise margins. Second, and as a less impacting effect, it can change the performance of the transmission line in a bus by modifying the effective characteristic impedance and propagation velocity, which in turn affect the system-level timing and the integrity of the signal. Due to these consequences of crosstalk, system performance

depends heavily on data patterns, line-to-line spacing, and switching rates [19]. We now look at the mechanisms that cause crosstalk.

3.3.1 Mutual Inductance and Mutual Capacitance

Mutual inductance is one of two ways crosstalk is produced. Mutual inductance L_m induces current from an aggressor line onto the victim line by means of the magnetic field. Mutual inductance L_m injects a voltage noise onto the victim proportional to the rate of change of the current on the aggressor line. The magnitude of this noise is calculated as

$$V_{noise, L_m} = L_m \frac{dI_{aggressor}}{dt} \quad (3.6)$$

The induced noise is proportional to the rate of change, and thus the mutual inductance becomes more significant in high-speed digital applications.

Mutual capacitance is the other mechanism that causes crosstalk. Mutual capacitance is the coupling of the two conductors via the electric field. Mutual capacitance C_m injects current onto the victim line proportional to the rate of change of voltage on the aggressor line:

$$I_{noise, C_m} = C_m \frac{dV_{aggressor}}{dt} \quad (3.7)$$

Thus, mutual capacitance also becomes significant in high-speed digital applications [19].

3.3.2 Types of Crosstalk

Crosstalk can be divided into far-end (FEXT) and near-end (NEXT) crosstalk. In FEXT, the aggressor signal travels in the same direction as the victim signal. NEXT, on the other hand, is the coupling of the aggressor signal to the victim traveling in the opposite direction, and is in general much more critical since the strong aggressor signal can couple into an attenuated victim signal in the connector or package located on the receiver side where the signal is already attenuated. Since crosstalk is caused by either capacitive or inductive coupling of two signal lines (more so inductive in modern dense connectors), it is relatively less at lower frequencies. Due to the low-pass nature of the channel, FEXT is also

attenuated at higher frequencies but still remains significant as the signal itself will be attenuated at the receiving end. As an example, Figure 3.4 depicts the FEXT and NEXT crosstalk in a modern package trace and cable.

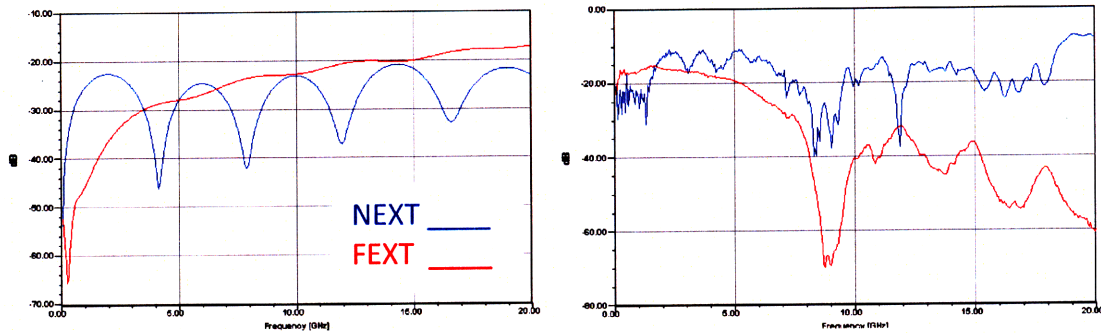


Figure 3.4: Example NEXT (blue) and FEXT (red) in a modern package (left) and a modern 1 meter cable (right)

3.4 Power Integrity (digital, analog)

Figure 3.5 shows a simplified circuit of the power supplied to High-Speed Serdes (HSS) cores. The current demand at the chip must be supplied through the power nets and from the ‘ideal’ voltage regulator on the motherboard. Voltage drops due to the parasitic resistance in the power nets as well as voltage noise due to parasitic inductance of the power nets is of major concern for power integrity which in turn leads to signal integrity [27]. Power supply circuitry for digital circuits generally employs decoupling capacitors placed in various sections of the power nets to alleviate noise caused by parasitic elements. Board-Side Caps (BSC) on the motherboard near the Voltage Regulator (VR), Motherboard caps (MBC) in the socket cavity on the board, Land-Side Caps (LSC) on the cavity in the BGA/LGA side of the package, Die-Side Caps (DSC) on the top side of the package, embedded capacitors between the package layers, and on-chip capacitance in the chip are examples of decoupling capacitors used to alleviate voltage noise to provide a steady voltage for the circuitry in the silicon at different frequency ranges [28]. Many algorithms

have been developed for efficient decoupling capacitor (de-cap) placement in various regions of the power net [29].

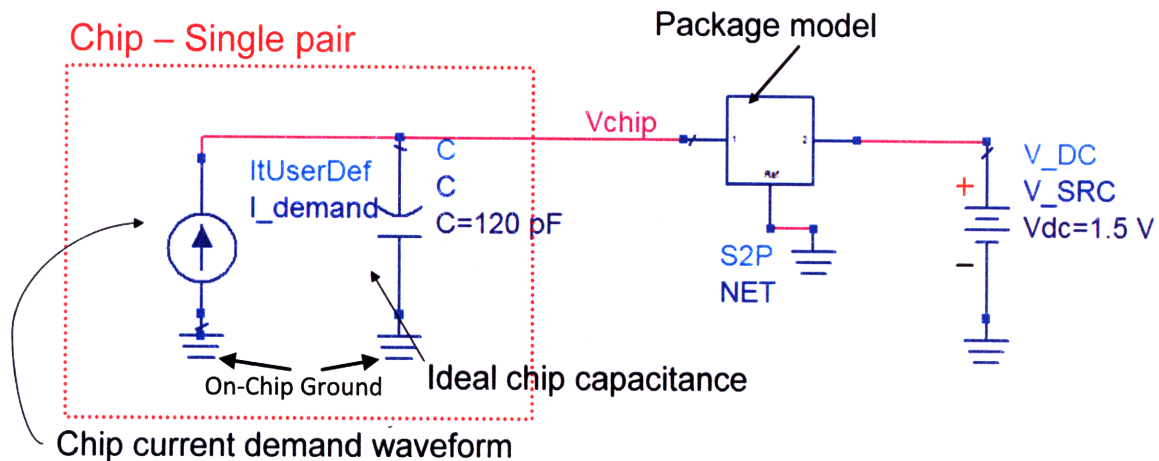


Figure 3.5: Power supply circuit including package parasitic model

Power supplied to analog circuits has thus far not been of much concern due to the constant power supply nature of Current-Mode Logic (CML) circuits used in HSS cores. However, the increase in CMOS logic used in HSS cores, to achieve power saving, is changing the nature of analog power net design in the package as well as in various other components. Analog power nets must account for voltage noise caused by the increased current fluctuations to assure a steady voltage supply. Figure 3.6 displays a current demand waveform for HSS cores along with the associated voltage supplied through analog power nets in the package.

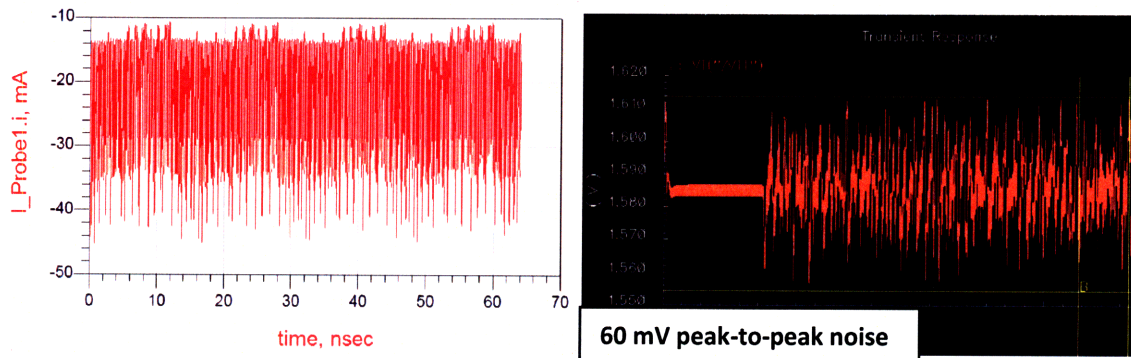


Figure 3.6: Chip current demand waveform (left) along with the corresponding voltage supplied through the package analog power nets with reference to on-chip ground.

Figure 3.6 depicts a 60 mV voltage fluctuation due to the package parasitic behavior. Assuming that this is within the tolerance range of the analog circuits and taking into account other noise caused by chip and board parasitic behavior, this package net design can be appropriate for the given current demand waveform, otherwise, more careful design must be performed for the analog power nets in the package.

This analog net power integrity analysis example demonstrates how power net parasitic effects can translate into high voltage fluctuations at the circuit resulting in undesirable signal transmission and thus loss of signal integrity.

In the remaining portion of this thesis we concentrate on challenges in high-speed channel design, caused by factors outlined in this chapter, that contribute to signal integrity.

Chapter 4 : Discontinuity Cancellation at the Package Level

This chapter discusses a package design technique to enhance high-speed signal performance by reducing the large impedance discontinuity effects of various regions in the package such as vias and solder balls. The technique involves inserting an intentional counter-discontinuity in complementary phase to the existing discontinuity in order to mitigate this discontinuity. In the next sections, the transmission line behavior of short multiple discontinuities are analyzed using theoretical approximation and simulation examples to demonstrate the validity of the mentioned technique. This broadband impedance matching technique is then applied to package via and solder ball transitions of high-speed differential nets using 3D simulation to evaluate improvement at target frequencies and its impact on bandwidth.

Discontinuities in high speed package interconnects are having more significant impacts as data rates have increased beyond 10Gbps. Vias in thick laminates cores and solder balls at the package to PCB interface introduce large capacitive discontinuities (Figure 4.1), while bond wires in wire-bond packages introduce large inductive discontinuities. In such cases, the behavior of the structure is inherent to the package and the designer has limited options to control the impedance given the package technology. The variables available to the designer are in the dependant on the packaging technology but may include trace width, via to via pitch, via plane opening, and BGA plane opening, which we will consider in our FBGA 3D model simulation.

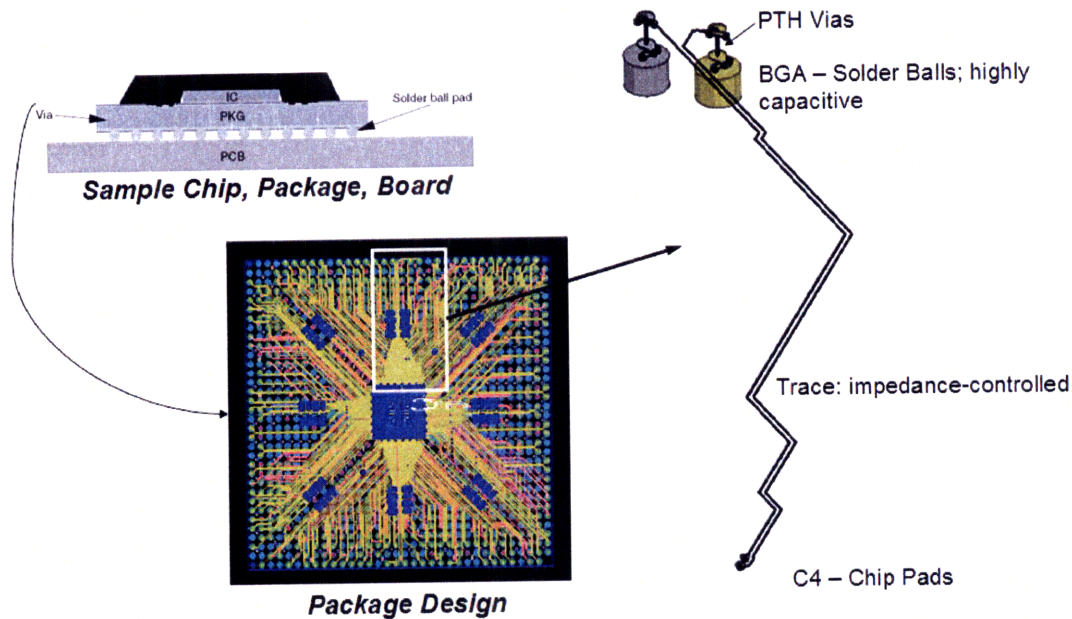


Figure 4.1: High-speed net in a flip-chip package. Solder balls are highly capacitive.

4.1 *The Counter-Discontinuity Cancellation Technique Description*

In an effort to decrease capacitive discontinuity in the solder ball path, intentional voids in the ground conductor layers above the solder balls of high speed signal nets have been used in recent package design practices [30]. While voiding the ground conductor helps reduce capacitance and hence the discontinuity significantly, it can interfere with neighboring signal structures and reduces either the power plane or signal routing space both also detrimental to signal integrity.

In this chapter we look at an alternative approach for obtaining further improvement in signal transmission. The technique uses transmission line behavior in short discontinuities. For example, if the existing discontinuity is capacitive, an inductive discontinuity is introduced to compensate for the capacitive discontinuity to achieve matching impedance as seen by the traveling wave over the short distance. This inductance insertion has been used in chip termination of high speed circuits and ESD devices to compensate for the large parasitic capacitance of chip circuits and pads [31, 32].

Contrary to narrowband impedance matching with lumped elements which is used for RF narrowband applications, insertion of transmission line discontinuities allows for broadband impedance matching which is desirable for the broadband high-speed communication we are studying. In addition, we take advantage of the current structure of the signal net to insert transmission line discontinuities which is much simpler and cost effective than lumped element matching for the package.

In the next sections, transmission line behavior with short discontinuities is revisited from a distributed line behavior and a lumped element circuit point of view. Package design structures in via-solder ball transition are studied for discontinuity compensation and its effectiveness is discussed using 3D EM (electromagnetic) simulations.

4.2 Theory: Distributed Network Behavior of Short Discontinuities

Consider the lossless transmission line with a short discontinuity of $l \ll \lambda/10$ in Figure 4.2. The transmission line is terminated at both ends with matching impedance to Z_0 . Assuming negligible phase shift with $l \ll \lambda/10$, the transmitted wave arriving at the end of Z_1 , at $t=0$, T_0 , can be approximated as $(1-\Gamma_1^2)$ [33]. For example, 81% of the incident wave will be transmitted at $t=0$ if $Z_0=50\Omega$ and $Z_1=20\Omega$.

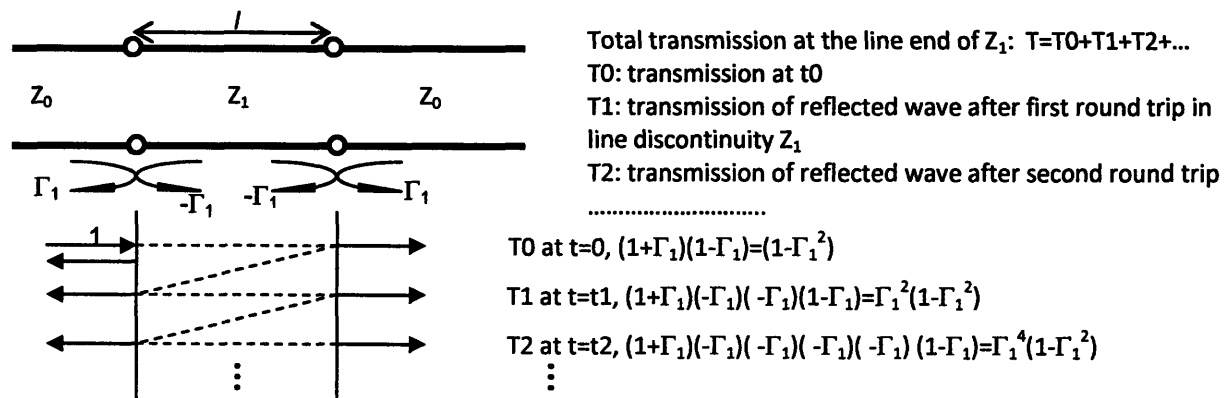


Figure 4.2: Illustration of transmission and reflection on a transmission line with a discontinuity

Next consider two transmission line configurations in Figure 4.3 where an extra discontinuity Z_2 is purposely inserted at the end(s) of the existing discontinuity Z_1 .

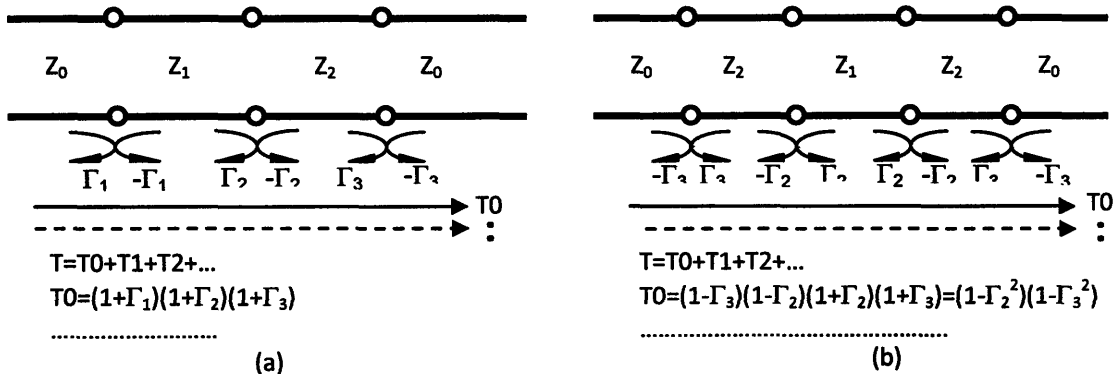


Figure 4.3: Transmission lines with an extra discontinuity inserted (a) at one discontinuity end and (b) at both discontinuity ends of existing discontinuity Z_1

A traveling wave encountering physical discontinuity experiences a gradual impedance transition rather than abrupt impedance change as the field interacts with structures in both sides of the discontinuity. Impedance seen by the wave is observed as an integrated characteristic of line segments alongside the discontinuity. Transmission line behavior can be seen more intuitively using lumped circuit elements if the line length is considerably smaller than the wavelength. Consider a transmission line with a discontinuity at $x=0$ as in Figure 4.4. Assuming a lossless transmission line ($G=0$, $R=0$), the characteristic impedances are characterized as $\sqrt{\frac{L_1}{C_1}}$ and $\sqrt{\frac{L_2}{C_2}}$, respectively. Traveling waves entering at $x=0$ will experience an integrated characteristic of two discontinuities. Assume line impedance 20Ω with $L_1=40\text{pH}$ and $C_1=0.1\text{pF}$ at $x<0$, and line impedance 125Ω with $L_2=250\text{pH}$ and $C_2=16\text{fF}$ at $x>0$ in Figure 4.4. Impedance at the discontinuity would be seen as 50Ω with $L=290\text{pH}$ and $C=116\text{fF}$ near the discontinuity $x=0$, which effectively offsets each other's large discontinuity.

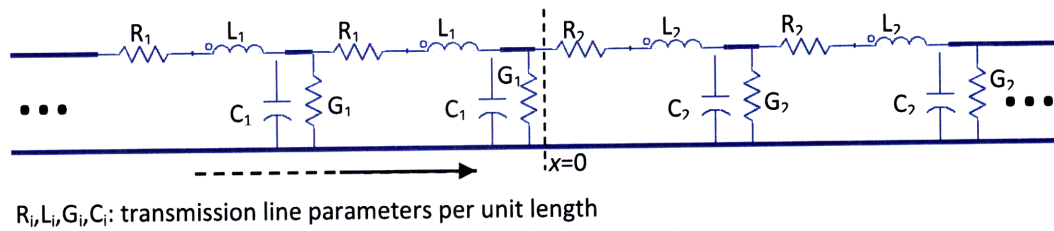


Figure 4.4: Distributed transmission line with a discontinuity represented by lumped elements

The configuration of Figure 4.3 (b) is used in the following analysis to further look into the behavior of package design options. Simulations of transmission line configuration in Figure 4.3 (b) were conducted using lossy transmission lines in Agilent ADS with the discontinuity Z_2 varying in length and impedance while maintaining the discontinuity length of Z_1 and overall transmission line length remain at 1mm and 5mm. As seen in Figure 4.5, improved transmission is observed with higher impedance of inserted discontinuity. This suggests that inserted inductive discontinuity and existing capacitive discontinuity effectively offset each other over a wide frequency bandwidth. As observed in Figure 4.5, better insertion loss can be achieved with higher impedance and longer discontinuity lines in the lower frequency range but this improvement dies out quickly at the higher frequency range. Moreover, wider bandwidth is achieved with relatively lower impedance and short discontinuity. While shorter discontinuity lines such as 0.3mm and 0.5mm can be more efficient in performance and bandwidth as observed in Figure 4.5, much higher impedance and hence larger inductance in the interconnect is required to achieve the target improvement and may not be realizable in practical manufacturing space.

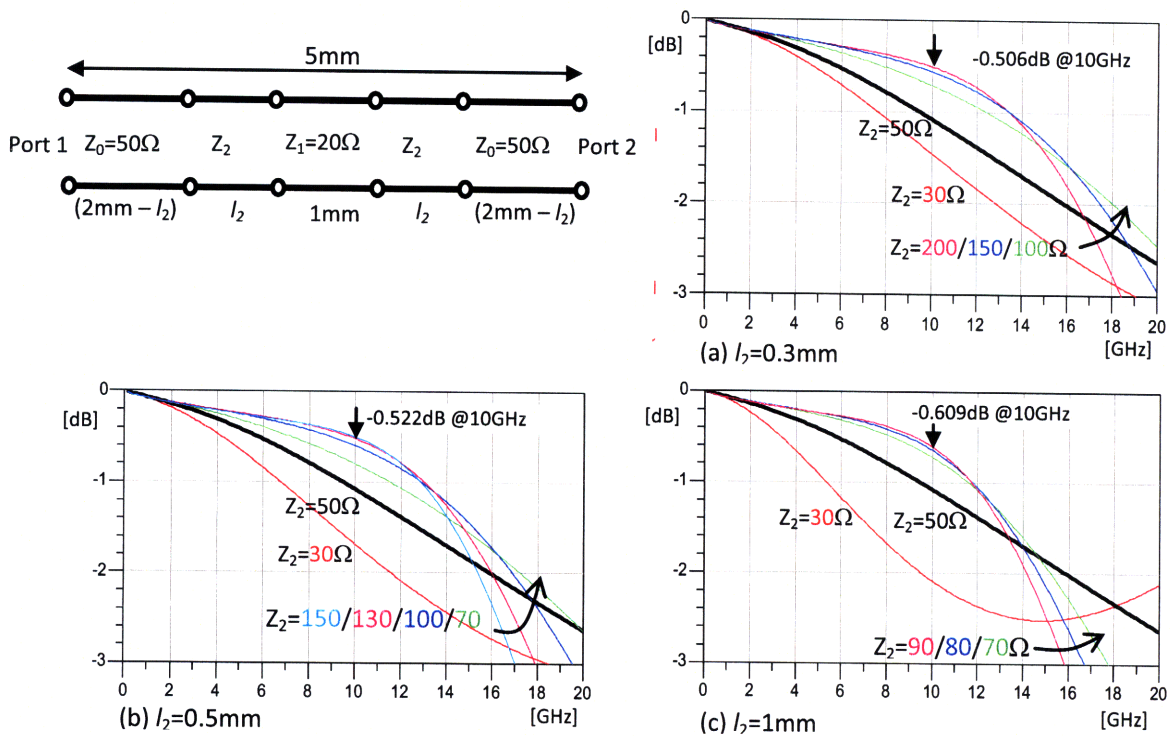


Figure 4.5: Insertion loss, S21, simulated using lossy ideal transmission lines with varying line impedances of (a) 0.3mm, (b) 0.5mm, and (c) 1mm for inserted counter-discontinuity Z_2 . $Z_2 = 50\Omega$ represents no discontinuity insertion.

4.3 3D Package Structure Simulations with Discontinuity Improvement

A 3D model of laminate core vias and solder balls of a differential pair was simulated to study the effectiveness of the discontinuity cancellation technique in a 4-layer Enhanced Plastic Ball Grid Array (EPBGA) wire-bond package as shown in Figure 4.6 where Plated-Through-Hole (PTH) vias are connected from the top to bottom layers including the middle core layer. Part of the package and board traces at escape edges of balls and vias were designed with higher impedance, 70Ω and 90Ω , than the target matching impedance to offer counter-discontinuity to the capacitive discontinuity of the solder balls and vias while maintaining an overall 2mm of lossy traces. It is observed in Figure 4.6 that higher gain was achieved with higher line impedance and longer discontinuity length but at the cost of

further limited bandwidth consistent with the transmission line behavior observed in Figure 4.5. Compared to the simulation results using transmission lines, insertion loss bandwidth of this package structure is observed to decrease more quickly with longer discontinuity with little gain at lower frequencies.

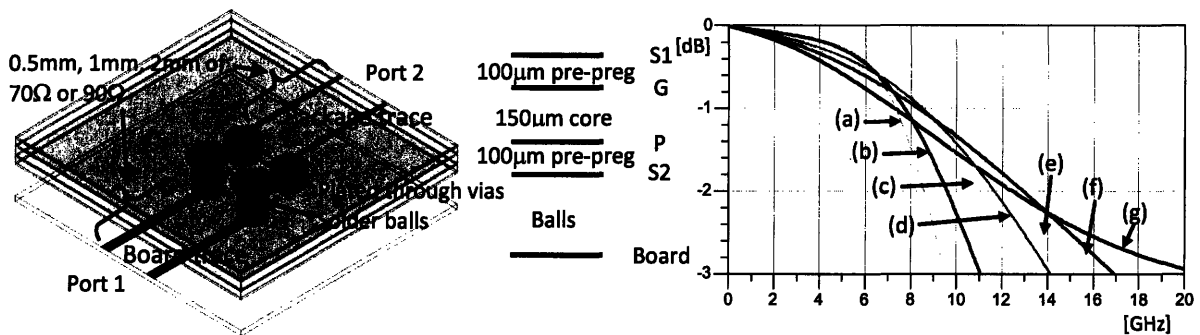


Figure 4.6: Insertion loss of a differential signal, SDD21, through solder balls of 1mm pitch and PTH vias in a 4-layer EPBGA package where package and board traces are designed with (a) 90Ω 2mm, (b) 70Ω 2mm, (c) 90Ω 1mm combined with 50Ω 1mm, (d) 70Ω 1mm with 50Ω 1mm, (e) 90Ω 0.5mm with 50Ω 1.5mm, (f) 70Ω 0.5mm with 50ohm 1.5mm and (g) 50Ω 2mm which is a nominal design structure with no discontinuity insertion, that is the basis for comparing the other cases.

A further design experiment was conducted with a 4-layer Fine Ball Grid Array (FBGA) package stack-up where blind vias are used in the outer thin pre-preg layers. With more design flexibility available using blind vias, performance improvement of inserting inductive discontinuities using the following three different areas of the structure was analyzed as is shown in Figure 4.7: escaping trace impedance on package/board, via transition, and plane void above balls and via clearance. Table 4.1 summarizes the different variables available in the FBGA package for impedance matching as well as the effect on the characteristic impedance of the component as the variable is increased in size.

Table 4.1: Design variables considered for opposite phase impedance insertion and their effect on the characteristic impedance

Feature	Size	Characteristic Impedance
Trace width	↑	↓
Trace length	↑	No Change
Via-via trace width	↑	↓
Via-via pitch	↑	No Change
Plane void above ball	↑	↑
Via clearance size	↑	↑

It is observed that insertion loss and bandwidth vary over a wide range depending on whether inductive counter-discontinuity is introduced or not. Structure (a) of Figure 4.7 represents a typical design of solder ball-via transition with no plane voids, minimum anti-via diameter and escaping traces matching to termination. Inductive discontinuities in (b) and (c) of Figure 4.7 are implemented as part of the escaping trace and at via to via connecting traces, respectively. In structure (f), inductive discontinuity of escaping trace is combined with plane voids and larger via clearance. While voids on plane layers above balls as in (d) and (e) of Figure 4.7 offer the most desirable improvement and bandwidth gain by reducing existing capacitive discontinuity, those voids reduce routing space and are not always feasible to implement without interfering with neighboring signal structures. Although inductive discontinuities added to escaping traces and via to via traces as in (b) and (c) are not as effective as plane voids with limited bandwidth, those still provide a very practical solution with improved performance up to 11 to 16GHz, a suitable upper range for many applications. Combining inductive trace design, plane voids, and larger via clearance as shown in (f) yields further performance improvement.

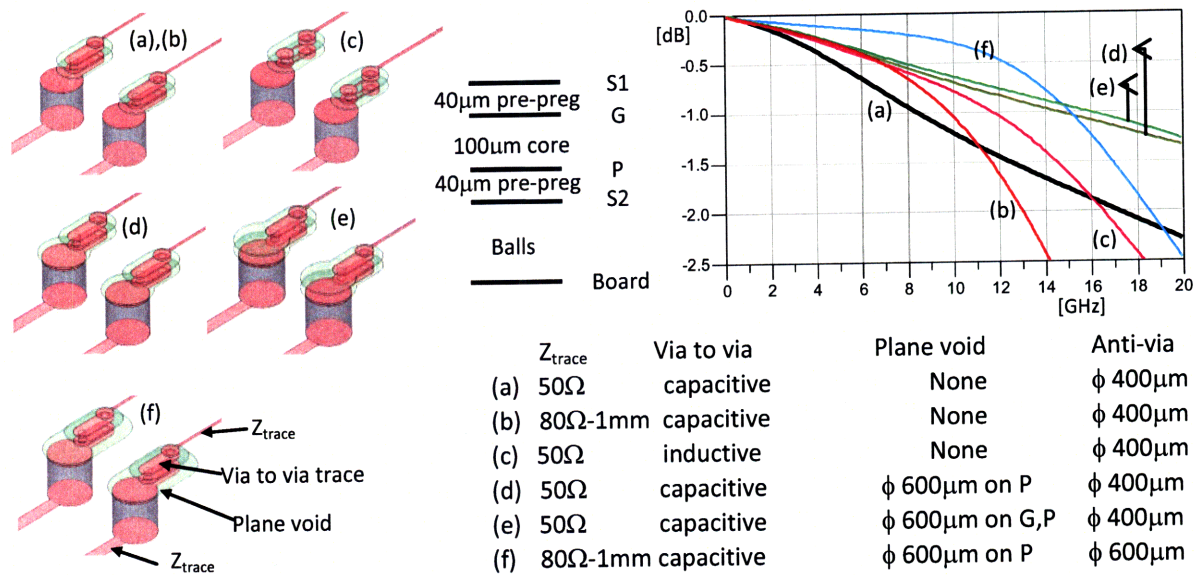


Figure 4.7: Insertion loss of a differential signal, SDD21, through solder balls and PTH/blind vias in 4 layer FBGA package varying plane voids above balls, via to via traces and routing trace impedance on package and board. Structure (a) represents a typical package design with no plane voids, minimum anti-via diameter and escaping traces of matching impedance and is used as a base structure to measure performance improvement of other design options.

4.4 Time Domain System Analysis

A technique to improve the performance of a high-speed links in the package by demonstrating the improvement in insertion loss of the package net for high-speed differential signaling has been presented. However, the effects of the given improvement must be analyzed in light of the system as a whole to be able to fully quantify the improvement in the channel performance. In this section, the package component along with discontinuity cancellation optimization is incorporated in a typical channel scenario for system level analysis. Since ultimately signals are measured at the receiver end in time-domain, time-domain eye diagram simulations are performed to quantify the improvements investigated in this chapter.

Note that modern high-speed channels operate at fast enough rates that require active channel equalization in order to correctly decipher transmitted bits at the receiver end. However, channel equalization can mask over the component level improvements we wish to observe in the channel and as such we purposely avoid any equalization in our eye diagram simulations. We use High-Speed Signal Clock Data Recovery (HSSCDR), an internal IBM tool, to perform the eye diagram simulations in this section. A 6.2 Giga bits per second (Gbps) and an 11Gbps high-speed transmitter (TX) and receiver (RX) circuit, based on an in production IBM circuit design, is used to perform the simulations. As seen in Figure 4.9, the simulated channel consisted of the TX and RX chips and a symmetrical structure with package models connected to daughter PCB stripline traces with PTH vias subsequently leading to high-speed connectors and finally connecting to the motherboard stripline trace via short stubbed PTHs. A 1 million bit long, Pseudo-Random-Bit-Sequence (PRBS) is used for the simulation.

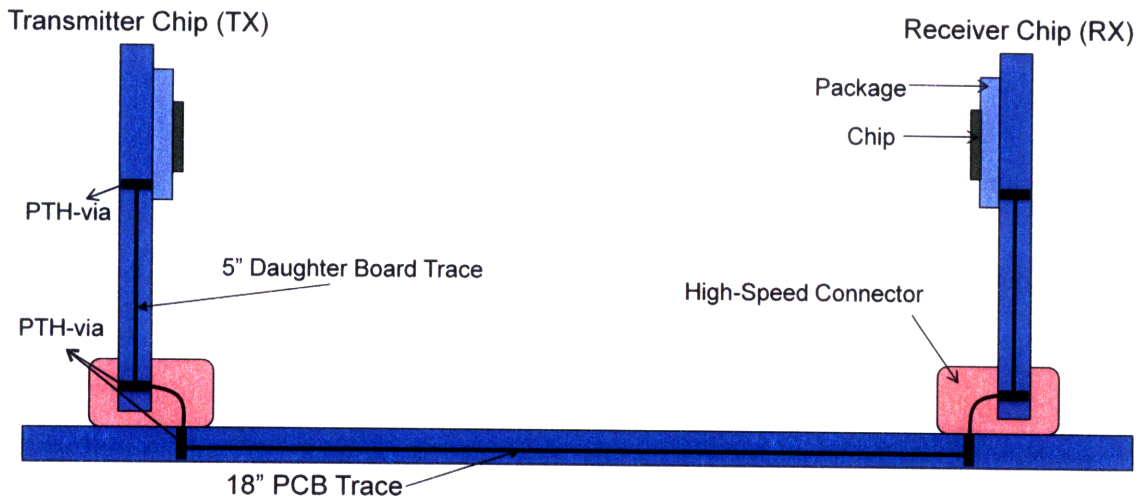


Figure 4.8: High-speed channel used for time-domain system simulation

Table 4.2 depicts the average height of the eye at the receiving end of the channel. The width is not displayed in the table since the coupling between the signals was not taken into account in the time-domain simulations. As table 4.2 shows, at both 6.2Gbps and 11Gbps transfer rates, a significant eye height improvement is seen at the receiving eye. In

the case of the 6.2Gbps transfer rate, the average eye height for the base and optimized cases are 158mV and 164mV respectively, therefore obtaining a 3.8% improvement over the base case with the discontinuity cancellation. For the 11Gbps rate while the worst case eye was closed in both cases due to the lossy PCB trace, the base and optimized cases produce a 161mV and 168mV average eye height respectively, in other words generating a 4.3% improvement over the base case due to the discontinuity optimization.

Table 4.2: Time-Domain simulation of discontinuity cancellation for a typical chip-to-chip channel

Package	Ave. Eye Height (6.2 Gbps)	Ave. Eye Height (11.0 Gbps)
Base Case	158 mV	161 mV
Discontinuity Optimized Case	164 mV	168 mV

The time-domain results of the system analysis highlight the significance of the performance improvement due to the discontinuity cancellation. This technique is especially valuable given that the cost of implementing it in the package is minimal and simply requires knowledge of the channel discontinuities at the frequencies of interest.

Chapter 5 : PCB Plated-Through-Hole (PTH) Via Design

A critical region in a high-speed chip-to-chip channel is the escape region from the package to the PCB traces. The high density of signals transmitted through the Ball Grid Array (BGA) structure of the package require more than a single PCB layer for signal routing and thus the use of vias and more specifically PTH vias. PTH vias are placed under the pad array of the package and transport signals into interior layers of the multi layer PC board. As the frequency content of signals increases to produce sharp rise and fall times for the digital pulse, the PTH via portion of the PCB becomes visible to the signal and signal loss and coupling in the vias becomes of major concern.

The fundamental frequency of the spectrum in Non Return to Zero (NRZ) signaling occurs at one half the data rate. The fundamental frequency of a 6.25Gbps signal, for example, would occur at 3.125GHz with some contributions from the third (9.38 GHz) and fifth (15.25 GHz) harmonics. The PTH via can behave as a parasitic element or a transmission line discontinuity based on the data rate of operation, as we saw in chapter 4. It acts as a notch filter centered around a frequency primarily determined by the unused portion of the via, henceforth referred to as the stub. Due to the stub resonance, signals traveling through the via experience major reflections at frequencies near the notch filter frequency [34, 35].

High-speed differential signaling greatly improves high-speed signaling especially shielding it from excessive noise and coupling from nearby signals. This is because the receiver only sees the relative voltage or voltage difference between the two transmission lines in the differential pair. The inherently superior noise immunity and high gain of differential circuits makes them less sensitive to the attenuation of the signal in the transmission medium, thus allowing for signal levels to be reduced with consequent improvements in switching speed, power dissipation and noise [36]. We thus analyze the performance and coupling of high-speed differential signaling in the PCB via escape region through 3D electromagnetic simulations performed by Ansoft's HFSS (High Frequency

Structure Simulator) [37]. The structure is a 28 layer PCB with 3 differential signal pairs considered in different coupling configurations.

5.1 PCB PTH-Via Structure Setup

The PCB modeled is a 28 layer PCB with copper planes of 0.6mil thickness each (Figure 5.1). The dielectric material used is FR4 with $\epsilon_r = 4.2$, which is widely used in

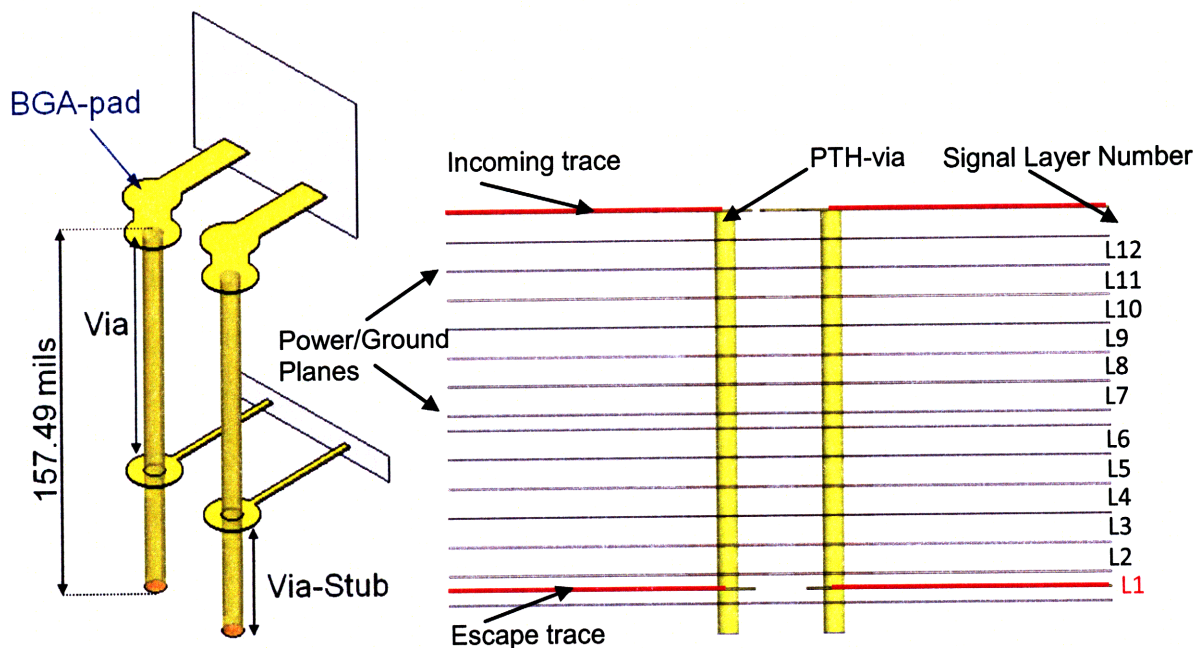


Figure 5.1: Modeled 16 layer PCB structure on the right displaying the via traces in red; Dimensions and structure of a differential via pair on the left.

the PCB industry, and the thickness of each of the dielectric layers is 10.2mils (with the exception of the core layer which is 4.8 mils thick). The PTH via diameter is 8mils with a via-to-via pitch of 40mils (about 1mm), corresponding to the pitch of the BGA solder-balls on the package. The via-pad diameter is 21mils and each GND/VDD has a via clearance with diameter 30mils. In addition, each via is directly connected to a BGA pad of diameter 21 mils, required for structural stability.

In a practical application, the signal is routed from the BGA pad through the via and onto a different PCB plane. We model the signal being routed to different layers in the PCB

which results in different via and via-stub lengths. The traces are used for measurement purposes and their effect is removed after simulation by de-embedding them in a post-process. Table 5.1 displays the different layers in the PCB that a signal can travel through along with the corresponding via and stub lengths. In addition to the models with via stubs, structures with the via stub back-drilled are also constructed and simulated to compare with the stubbed models. In the back-drilled models, the signal escape layers in the PCB are similar to those in Table 5.1 with the stub length corresponding to the back-drill length.

Table 5.1: Stubbed PCB Via Configuration

Escape Level	Stub (mils)	Via (mils)	Stub $\lambda/4$ Resonance Freq (GHz)
12	140.7	16.8	10.0
11	129.8	27.7	10.8
10	119.0	38.5	11.8
9	108.2	49.3	13.0
8	97.4	60.1	14.5
7	86.6	70.9	16.3
6	70.3	87.2	20.0
5	59.5	98.0	23.7
4	48.7	108.8	28.9
3	37.9	119.6	37.2
2	27.1	130.4	52.0
1	16.2	141.3	86.7

Three different via configuration models are constructed to study the effect of differential coupling among the vias in the PCB escape region. As seen in Figure 5.2 and Figure 5.3, these models are boxed, staggered and diagonal configurations.

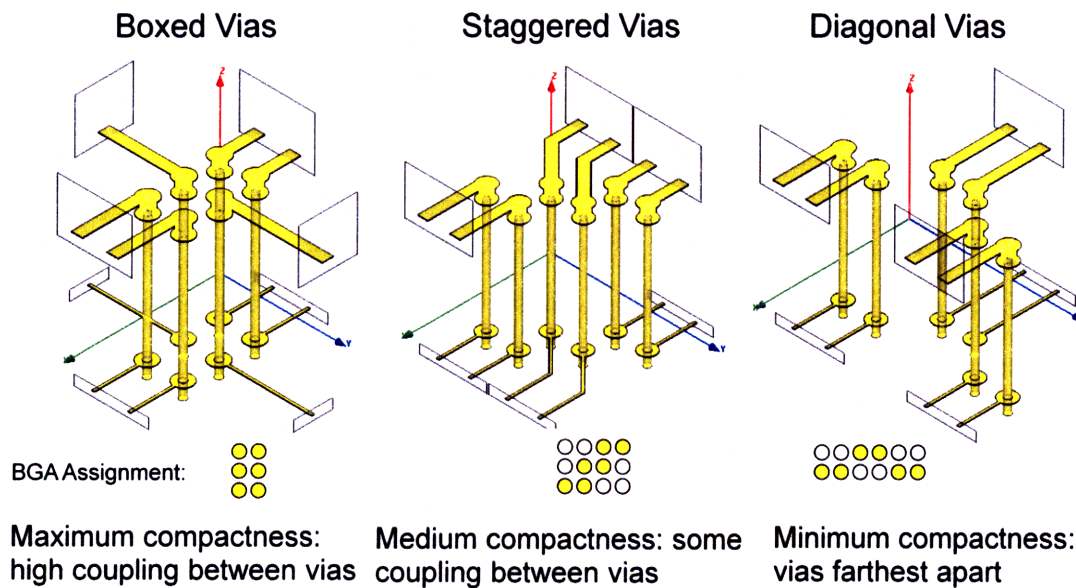


Figure 5.2: Via configurations with different signal densities.

The different power planes as well as the via clearance on every GND/VDD plane is depicted in the 3D models in Figure 5.3. One will also note that except for one via pair in the staggered configuration, all incoming and escape traces are routed on the same side of the model. This allows for consistency in the return path current of the different models.

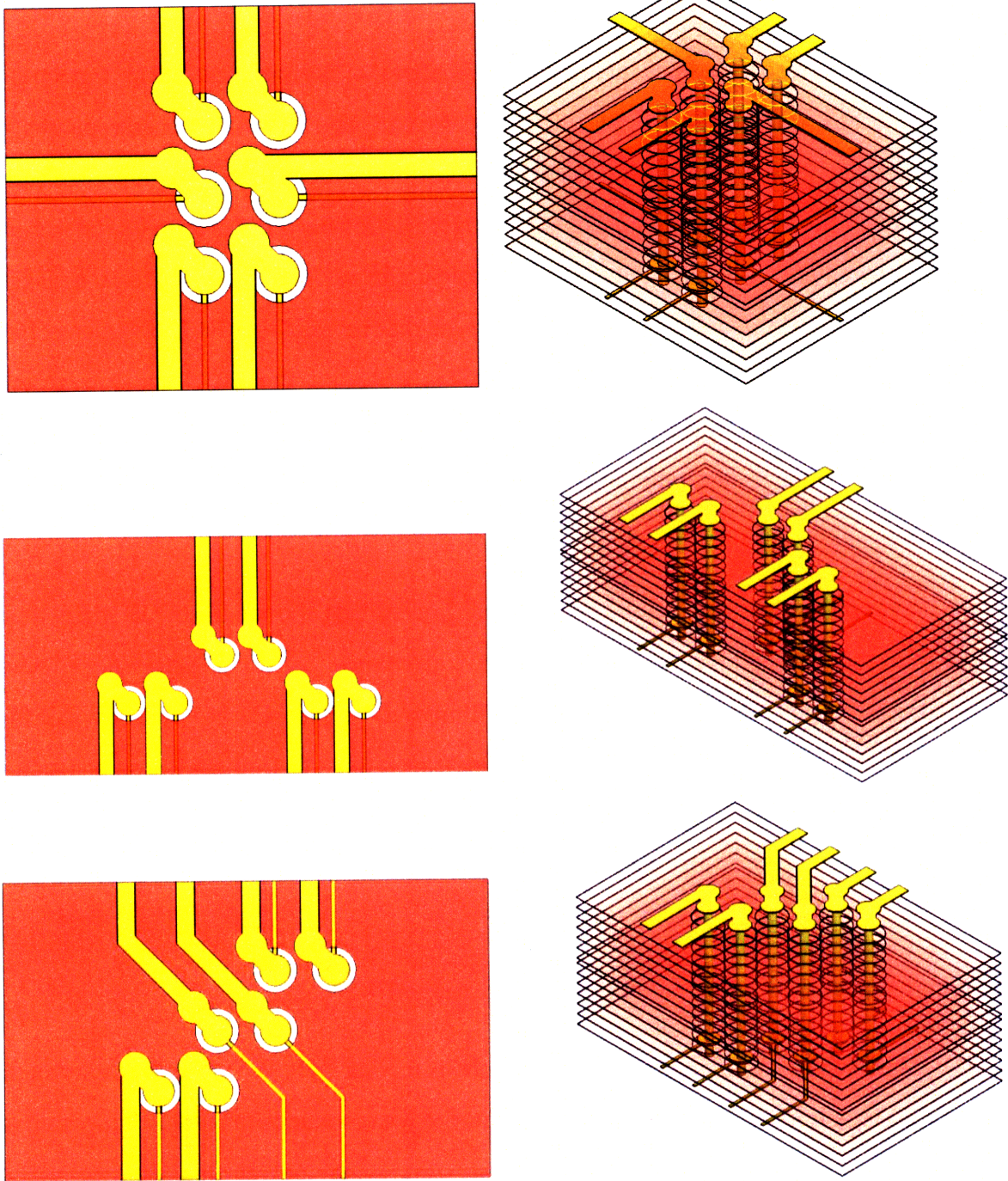


Figure 5.3: Top and 3D view of the Box, Diagonal, and Staggered via configurations

5.2 Signal Transmission

Impedance discontinuities are the main causes of signals not being transmitted through the PCB escape region. The BGA pad, via pad, and the via stub are sources for capacitive discontinuity while the via itself contributes both inductive and capacitive impedances to the signal path. Capacitive impedance arises from the proximity of the signal paths to power and ground planes. In our design, the via pad capacitance is negligible compared to the BGA pad due to the via clearances that remove the GND/VDD planes from underneath the via pad. The capacitive coupling between the BGA pad and ground, however, causes the BGA pad to be a highly capacitive region of the signal path and thus creating an impedance discontinuity that is lower than the matched 100 Ω characteristic impedance.

The via parasitic is also significant especially given that the length of the via is much longer than the BGA pad. Every via has parasitic capacitance to ground. Moreover, PTH vias are electrically long structures relative to the interested frequencies of operation and thus behave like transmission lines [38]. The minimum transit time, t_v , through the stub structure can be approximated by:

$$t_v = \frac{l\sqrt{\epsilon_r}}{c} \quad (5.1)$$

Thus, in the given PCB setup, equation 5.1 evaluates to 0.027ns.

The potentially more impacting discontinuity is the via stub. The via stub acts as an un-terminated transmission line, generating a quarter-wave resonance (a zero) in impedance at a frequency corresponding to four times t_{stub} . Any signal power near this resonance frequency will be subsequently attenuated by the via stub [39].

The results of the PCB via simulations with the stub back-drilled display two distinct behaviors for relatively shorter and longer vias. The cut-off for these two groups is approximately at half the PCB length, thus we group the vias escaping in layer 1-6 as long

vias and layers 7-12 as short vias. As shown in Figure 5.4, in the long via region, increased via lengths contribute to less insertion loss and thus degraded performance at higher frequencies. For the short vias, however, we find that shorter vias tend to decrease the insertion loss, as seen in Figure 5.5. It is also noted that in all the PCB models of vias with the stubs back-drilled, via length is almost irrelevant for insertion loss at frequencies below 8 GHz.

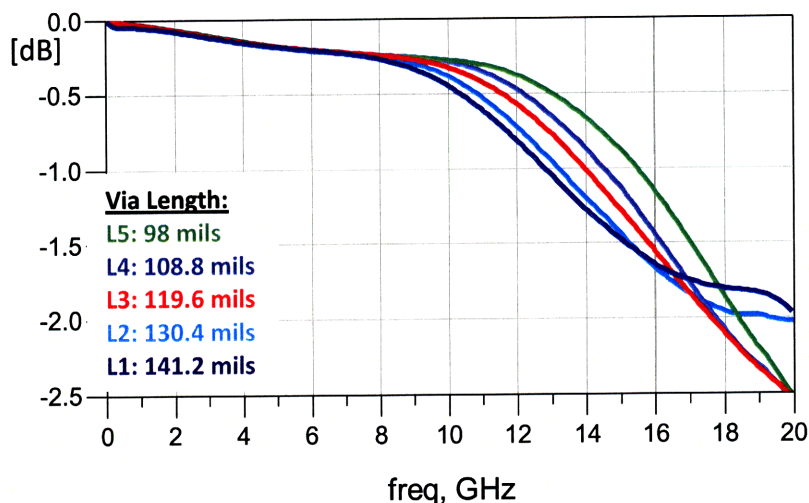


Figure 5.4: Insertion loss for differential vias with back-drilled stubs (longer via lengths)

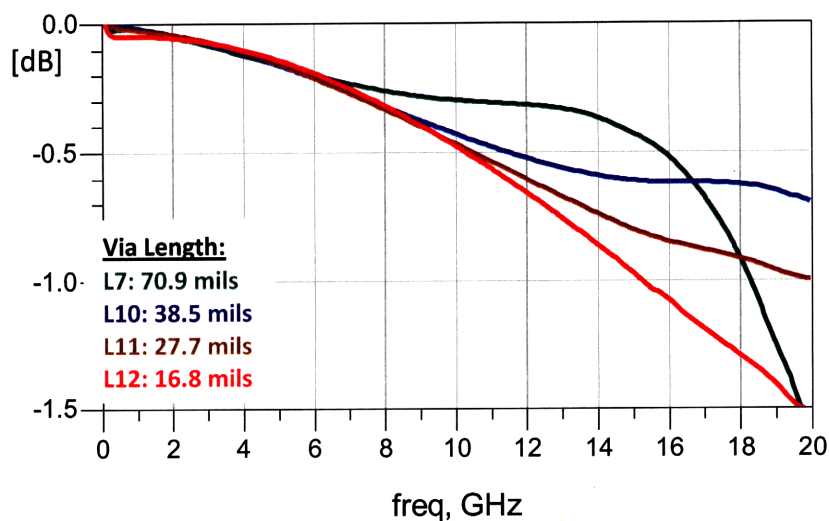


Figure 5.5: Insertion loss for differential vias with back-drilled stubs (shorter via lengths)

In order to characterize the signal net structure, we perform Time Domain Reflectometry (TDR) simulations. TDR refers to measuring a system by injecting a signal and observing the reflections back at the source end. Using this method, the impedance discontinuities in the net can be observed. Figure 5.6 depicts the TDR simulation waveform of the PCB via structure with different via lengths. The key observation is the discontinuity difference between the long via in Layer 12 and the short via in layer 1. The longer via displays a smaller capacitive discontinuity and a sudden increase in the impedance in the center of the waveform. This is due to the relatively larger impedance of the longer via which produces impedance cancellation of the capacitive impedance present in the structure.

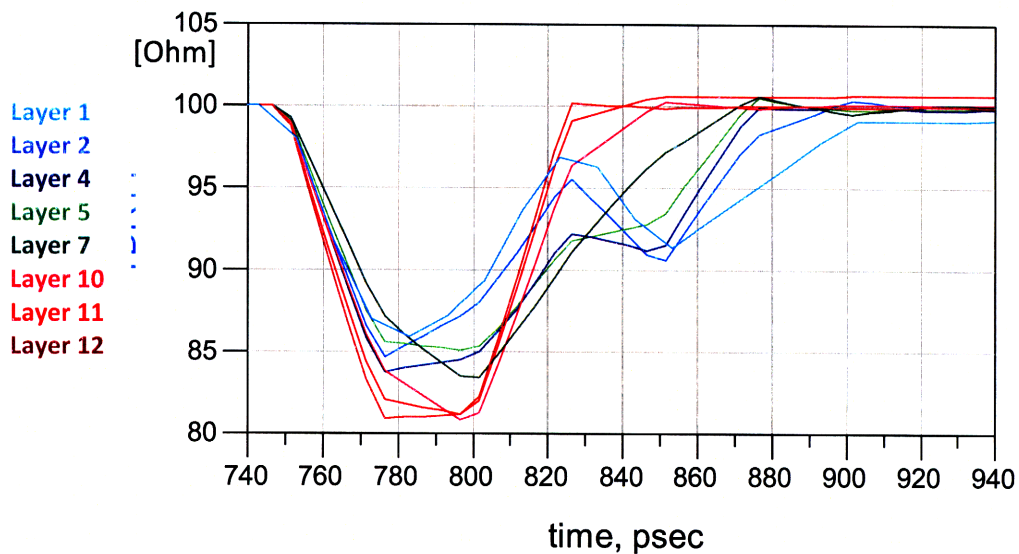


Figure 5.6: TDR impedance waveform of different length differential vias

These observations can explain why from the results of our simulations the insertion loss tends to degrade both for smaller via lengths as well as for longer via lengths. From our simulations we see that layer 7 via escape produces the best performance for our particular PCB setup.

The PCB via structures with the stubs produces significantly larger losses due to the resonance caused by the stub discontinuity. In Figure 5.7, we observe that the resonance frequency of the vias with different stub lengths occurs at a lower frequency than the ones predicted by the quarter-wave length theoretical approximation seen in Table 5.1. For example, the simulated resonance for the 16.2mil stub is 8GHz with the theoretical approximation being 10GHz; and the simulated resonance for the 59.5mil stub is 18.5GHz with the theoretical approximation being 23.7GHz. This difference is due to the fact that theoretical values were calculated assuming the stub inside a dielectric material with relative permittivity of $\epsilon_r = 4.2$. The PCB, however, consists of layers of FR4 material ($\epsilon_r = 4.2$) separated by layers of conducting planes which interfere with the electromagnetic waves passing through the FR4 material, thus creating a different effective dielectric constant. In addition, the coupling of the vias with conducting planes was assumed to be negligible while in reality this is not the case and the coupling will reduce the resonance frequency [23].

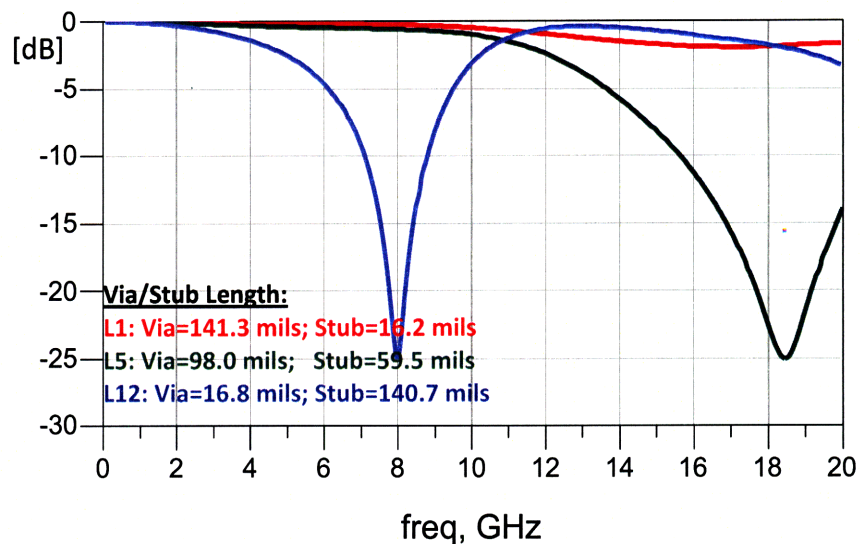


Figure 5.7: Insertion loss for three differential via pairs with stubs

5.2.1 Time-Domain System Analysis

We now look at the effect of the stub and via lengths in light of the system as a whole in order to fully quantify the impact on overall channel performance. As in Chapter 4, we incorporate the PTH-via structure in a typical channel scenario for system level analysis and simulate the time-domain eye diagram to quantify the PCB-via design variables considered in this chapter.

Simulations without any channel equalization produced severe eye closure at the receiver end due to large losses caused by the lossy PTH, thus making any comparison impossible. Therefore, we employed Feed Forward Equalization (FFE) to obtain an eye opening at the receiver in order to compare the effect, after equalization, of the PTH stub and via length. Once again, we use IBM High-Speed Signal Clock Data Recovery (HSSCDR) to perform the eye diagram simulations in this section. A 6.2Gbps and an 11Gbps high-speed transmitter (TX) and receiver (RX) circuit, based on an in production IBM circuit design, is used to perform the simulations. Two channels were considered in our time-domain simulations: one including the PCB PTH-via variation only at the package interface and a second worst-case channel which includes the varying PTH-via at the connector/PCB interface as well. The channels are displayed in Figure 5.8. We used a 1 million bit long, Pseudo-Random-Bit-Sequence (PRBS) for the simulation.

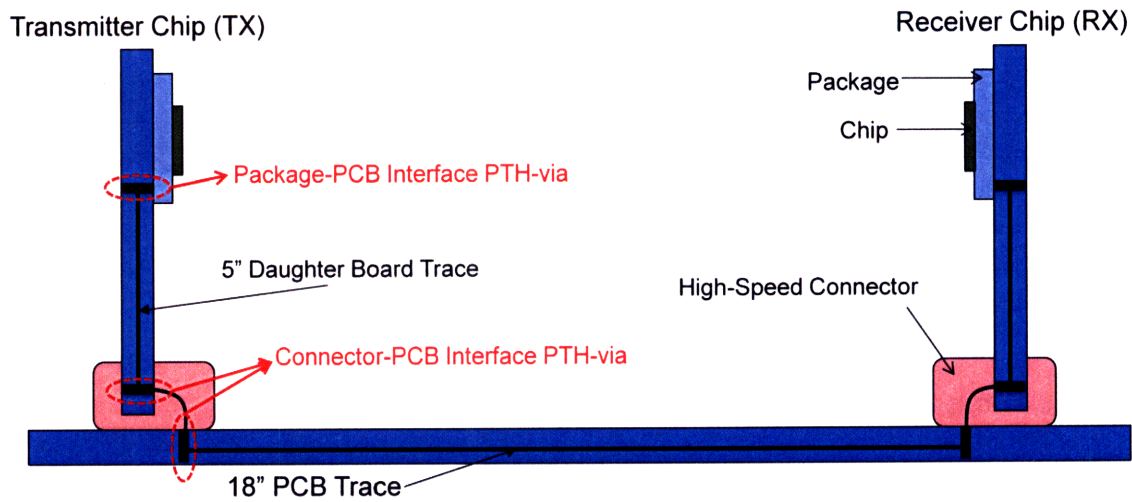


Figure 5.8: High-speed channel used for time-domain simulations

Tables 5.2 and 5.3 depict the average height of the eye at the receiving end of the channel for the 6.2Gbps and 11Gbps transfer rates with FFE. The eye width is not of interest here since the coupling between the signals was not taken into account in the time-domain simulations.

It is observed that longer stub lengths translate into larger average eye height closure with more severe eye closure occurring at the 11Gbps transfer rate compared to 6.2Gbps. A 141 mil long stub closes the average eye height by an additional 17% in the case of the channel with the PTH-via inserted at the package while keeping the connector PTH-vias as low loss vias. Moreover, the worst-case channel amplifies the loss caused by the stub since more discontinuities are introduced into the channel. The effect of the back-drilled vias is overshadowed by the equalization and thus the average eye height is similar for the two via lengths considered. It is also noted that the worst-case channel does not affect the back-drilled PTH performance since no stub discontinuity exist in these cases.

Table 5.2: 11Gbps time-domain eye simulation with FFE

PCB Layer	Via Length (mils)	Stub Length (mils)	Ave. Eye Height	WC-Ave. Eye Height
1	141.3	16.2	63.3%	61.3%
5	98.0	59.5	61.3%	53.3%
12	16.8	140.7	46.3%	31.8%
2 – Back-drilled	130.4	None	63.3%	63.0%
5 – Back-drilled	98.0	None	61.7%	61.7%

Table 5.3: 6.2Gbps time-domain eye simulation with FFE

PCB Layer	Via Length (mils)	Stub Length (mils)	Ave. Eye Height	WC-Ave. Eye Height
1	141.3	16.2	62.3%	61.0%
5	98.0	59.5	61.3%	58.7%
12	16.8	140.7	59.0%	49.7%
2 – Back-drilled	130.4	None	63.3%	62.0%
5 – Back-drilled	98.0	None	63.3%	63.3%

As shown in Figure 5.9, the channel insertion loss of the layer 12 via with the longest stub incurs large losses compared to the shorter subs or no stubs. In addition, the worst case channel insertion loss can also be seen to be more severe at the same frequencies compared to the regular channel. Eye diagrams for the layer 12 and layer 1 PTH-vias are depicted in Figure 5.10.

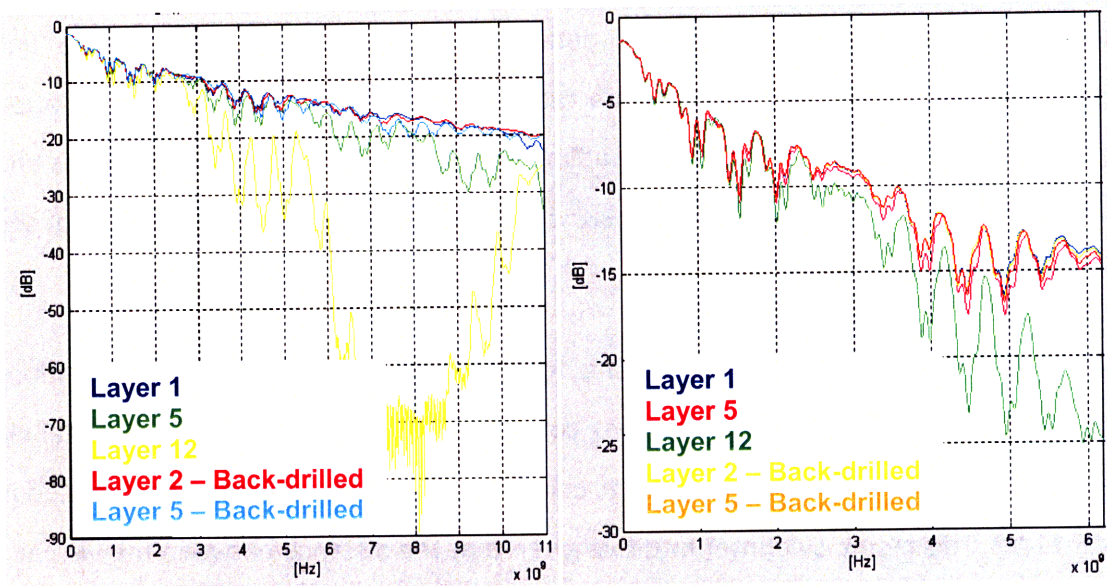


Figure 5.9: Insertion loss plots for channels with different PTH-vias. Left plot: worst case channel for 11Gbps simulation. Right plot: channel with package PTH-via and 6.2Gbps transfer rate simulation.

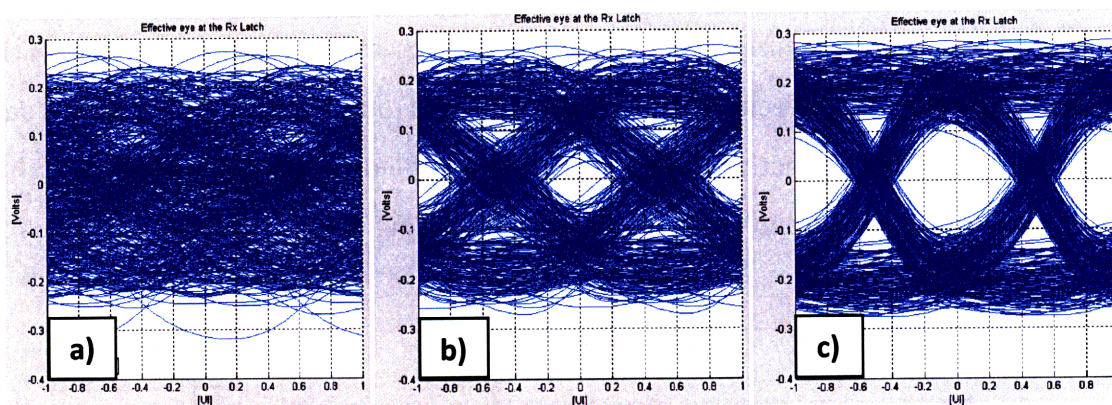


Figure 5.10: Eye diagram for 11Gbps simulation of a) Layer 12 PTH-via with worst case channel, b) Layer 12 PTH-via, and c) Layer 1 PTH-via.

5.3 Signal Coupling

Chapter 3 described how signal coupling is caused by capacitive and inductive coupling between two conducting signal paths. These parasitic couplings are governed by the PCB structure and the distance and configuration of the signal nets. Noise coupling is of major concern in the design of high wiring density packages with high speed SerDes (HSS) signals.

Adequate isolation between high speed data links is a good measure of the link performance along with the increase in data rates and wiring density. IBM ASIC isolation requirements for include a -30dB or lower coupling between transmit differential signals and -35dB or lower coupling between receiving signals up to the fundamental frequency of the transmission data [40].

The simulated differential via coupling for the three different via configurations studied suggests that the coupling in the box configuration is higher than the diagonal via configuration which in turn is higher than the coupling in the staggered case, as depicted in Figures 5.11-12. This result is counter intuitive given that the distance between the via pairs is smaller in the staggered case as compared to the diagonal configuration. As we saw earlier in this section, the staggered PCB configuration contained a via pair with traces routed on different sides on the PCB model box. This inconsistency between the models might explain why the staggered performs better than the diagonal configuration especially that the staggered case optimizes for return current, thus minimizing the coupling with other nets. However, the effects of the traces into and out of the PTH via were de-embedded and assuming perfect de-embedding, this should not be the case. Moreover, the single-ended coupling results don't confirm this de-embedding error.

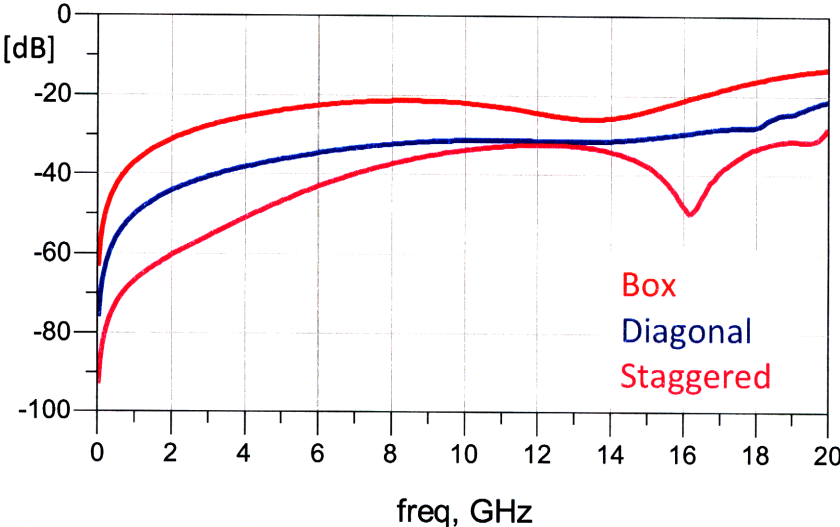


Figure 5.11: Near-End crosstalk (NEXT) for the Box, Staggered, and Diagonal via configurations

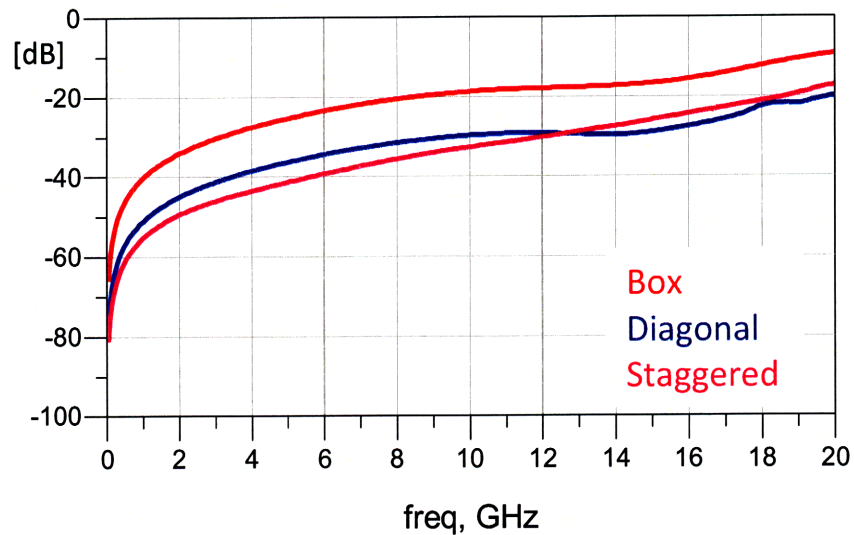


Figure 5.12: Far-End Crosstalk (FEXT) for the Box, Staggered, and Diagonal via configurations

At frequencies approaching the stub resonance frequency, NEXT differential coupling in vias with subs is significantly larger than the coupling between vias of the same length yet with the stubs back-drilled, as depicted in Figure 5.13. In addition, vias with longer stubs produce larger differential coupling at lower frequencies.

The FEXT differential coupling in stubbed vias, however, is not affected as much as the NEXT near the resonance frequency of the stub since the stub is a source of reflection and prevents the signal from reaching the far end on the aggressor net and thus cannot affect the victim net as significantly. This is shown in Figure 5.14 for the L5 via stub.

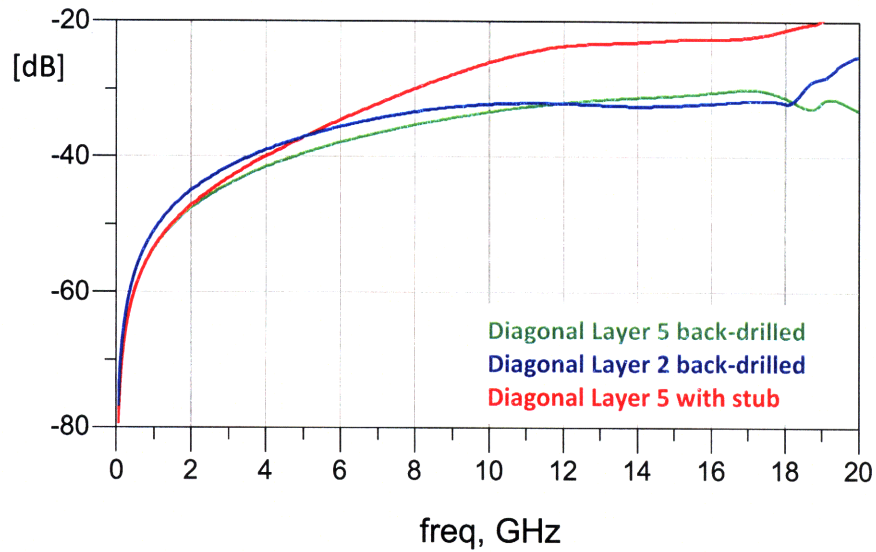


Figure 5.13: Differential NEXT for the diagonal configuration for layer 2 back-drilled (Blue), layer 5 back-drilled (Green), and layer 5 with stub (Red)

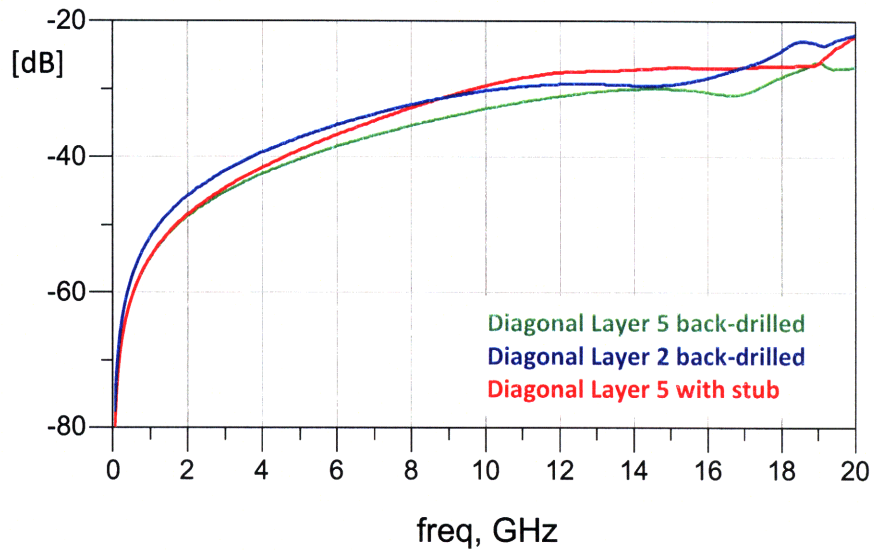


Figure 5.14: Differential FEXT for the diagonal configuration for layer 2 back-drilled (Blue), layer 5 back-drilled (Green), and layer 5 with stub (Red)

Finally, we see that the amount of NEXT differential coupling increases along with the via length as area of the vias where electromagnetic waves can interact is increased. This is shown in Figure 5.15.

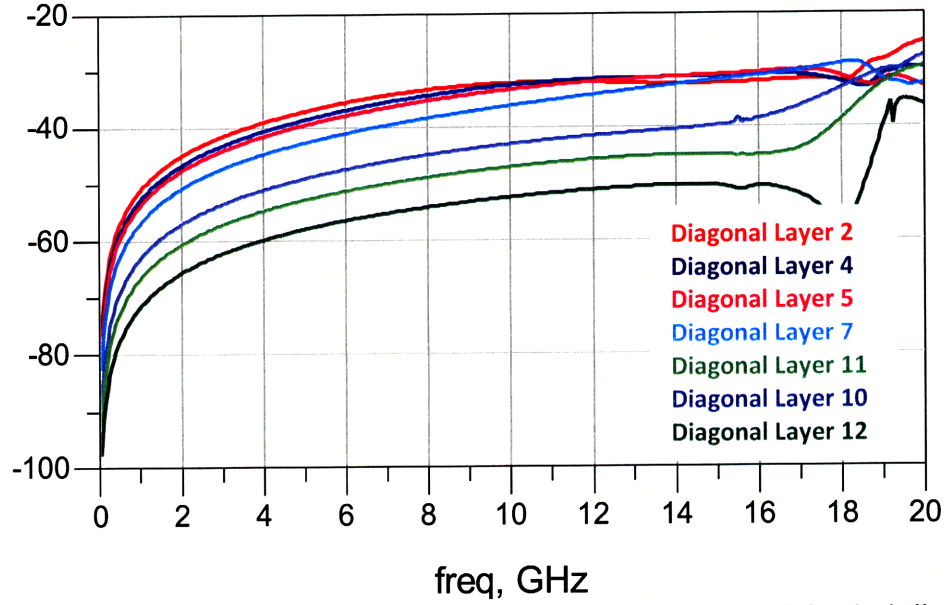


Figure 5.15: Differential NEXT coupling for different via lengths with back-drilled stubs

Chapter 6 : Conclusion

The package, the PCB, connectors, and cables are all components of a high-speed channel. Optimization of each of these components is only valuable when significant improvement is seen in the high-speed channel as a whole. Traditionally in the microelectronics industry, each component has been designed by a separate team responsible for optimizing their specific component for the needs of the market and given the tools and technologies available at the time. As the improvement margins within each component have reached their limits, co-designing especially at different component interfaces is becoming more commonplace. A package-PCB co-design, for example, might result in a less desirable or even lower performance design in the PCB that will facilitate a solution in the package that allows for overall improved performance in the high-speed channel system. An additional factor other than improved performance is reduced cost which is sometimes as significant as performance, in the industry.

In this thesis, we have analyzed critical aspects of high-speed channel design with a focus on the package and PCB region. A technique for reducing inherent discontinuities at the package level was studied and performance improvements were obtained at relatively low cost. In addition, the critical region of package and PCB interface was studied and system level simulations were performed, in time and frequency domain, in order to allow for better design rules for package and PCB design.

We have seen that better transmission performance in the package can be achieved by compensating for inherent discontinuities by inserting a counter-discontinuity of short electrical length. As the lengths of both the counter-discontinuity and existing discontinuities is increased, distributed network behavior of the transmission lines becomes more prominent resulting in reduced bandwidth. Fortunately, the package dimensions of the laminate core vias and solder ball structures are well within a tenth of a

wavelength of application speeds of interest and hence these techniques for inserting counter-discontinuities in complementary phase are effective for improving transmission while maintaining the necessary bandwidth. System level time domain analysis also confirms the transmission performance improvement gained by this technique. Although only capacitive discontinuity examples of vias and solder balls were presented, this technique can be applied to inductive discontinuities such as short bond-wires as well.

Maximum channel performance can only be obtained when package design is performed in conjunction with other nearby structures in the channel. As such, the performance of PTH-vias in the package and PCB region was studied for signal transmission performance and coupling configurations. We have seen that long stubs reduce performance significantly especially that PTH-vias occur very often and repeatedly in a typical channel. As back-drilling is a costly operation, utilizing shorter stubbed, albeit long, PTH vias can help reduce the performance loss due to the stubs significantly. Signal coupling is also significantly affected by the stub length, and shorter stubs help reduce coupling as well. NEXT coupling is far more impacted with longer stubs especially at higher frequencies near the resonance frequency, while FEXT is not impacted as much due to the high loss in the channel due to the stub.

It has been shown that although vias are capacitive in general, via length increases the relative inductance of the via and with our PCB structure dimensions even became inductively dominated at longer lengths, thus providing an optimized length at which maximum channel transmission occurs due to minimal discontinuity. This, however, is the case for back-drilled vias with no stub being present. In the stubbed PTH case, the stub length overshadows any improvement due to optimized via discontinuity.

Coupling between the PTH and the ground layers of the PCB as well as with other signal nets effects the resonance frequency due to the stub by lowering the resonant frequency compared to the calculated theoretical quarter-wavelength frequency. In addition, signal coupling was shown to be directly related to via length, and decreased with

shorter vias. With regards to different BGA configurations, the Box via created the largest differential coupling compared to Staggered and Diagonal configurations.

As we have seen, channel design at the package level and the larger system level is largely application dependant. The problem is not only to maximize performance, but to do so at a reduced cost while meeting the demand of the particular application. The tradeoff between cost and performance requires exact knowledge of the channel limits and design implications. For example, back-drilling of stubs is the clear solution to optimizing performance, yet as we have shown, the impact of short stubs is not significant enough to warrant the cost of back-drilling for all applications.

Chapter 7 : Future Work

High-speed channel design is a challenging field especially when cost is added to the equation. Signaling data rates keep increasing and new problems start occurring as these rates increase. Therefore, further work has to be done to determine new limiting factors at higher rates. One of these factors is the increased importance of coupling analysis in signal integrity studies. At higher rates, not only immediate neighboring signals but a neighborhood of signals needs to be analyzed for coupling effects. Time-domain simulations need to take coupling into account as well since the eye width is significantly impacted by this jitter due to coupling.

Channel equalization impacts channel performance in non-linear ways. As both Feed Forward Equalization (FFE) and Decision Feedback Equalization (DFE) become commonplace at higher signaling rates, channel design must be studied together with equalization effect on the design similar to the co-design process of channel components. The challenge is to optimize for cost by fully utilizing channel equalization.

Finally, a section beyond the scope of this thesis yet crucial to signal integrity is power integrity of the high-speed circuitry. Current in power rails for analog circuits are switching at faster rates creating large leakage current and thus large voltage noise due to power net parasitics. As signaling rates increase, power delivery to the HSS cores for serial communication must be closely studied to ensure reliable power delivery and thus circuit performance.

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