Homework #8 - November 8, 2002

Due: November 15, 2002 at lecture

1. *[40 points]* Consider an n-channel MOSFET in the saturation regime.

a) Derive expressions and sketch the spatial dependence of $V(y)$, $\mathcal{E}_{ox}(y)$, $\mathcal{E}_y(y)$, $v_e(y)$, and $Q_i(y)$ from source to drain. Explain your results.

b) Derive also an expression for the electron velocity due to diffusion. Compare the diffusion velocity with the drift velocity obtained in part a). Under what conditions is electron diffusion safely ignored?

c) Obtain an expression for the transit time of electrons through the channel from source to drain by computing:

$$\tau_t = \int_0^{L_g} dt = \int_0^{L_g} \frac{dy}{v_e(y)}$$

d) Compute the transit time again using the following expression:

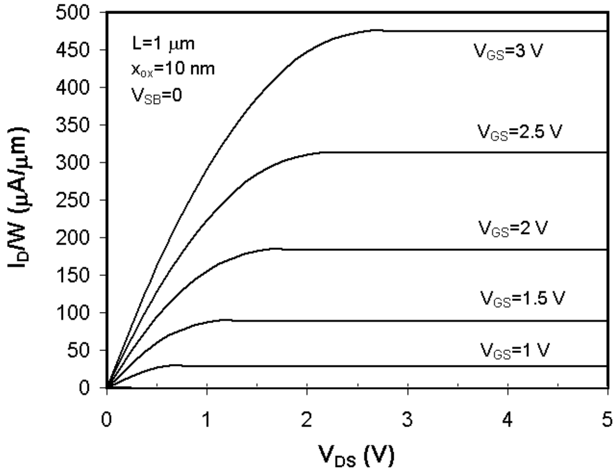
$$\tau_t = \frac{|Q_I|}{I_D} = \frac{W_g |\int_0^{L_g} Q_i(y) dy|}{I_D}$$

Compare this result with the one obtained on part c).

For all parts, neglect the body effect, that is, assume that the current of the transistor is given by Eq. **??**.

2. *[10 points]* You have been given the specs of a foundry's digital CMOS technology that you are considering for one of your company's designs. Some of the values that characterize the n-MOSFET at room temperature are: $I_{off} = 1\ nA/\mu m$, $V_T = 0.5\ V$, and $S = 70\ mV/dec$. For your design, it is crucial that you know I_{off} at 85 C, which is not given in the spec sheet. You consult some books and you find that V_T changes typically about $-4\ mV/C$. Also the inversion layer mobility goes approximately as T^{-2}. With all this, *estimate* I_{off} at 85 C. State any assumptions that you need to make.

3. *[30 points]* Consider the output I-V characteristics of a long-channel n-MOSFET for $V_{SB} = 0$ below. The device has a gate length $L_g = 1\ \mu m$ and a gate oxide thickness $x_{ox} = 10\ nm$. The output characteristics have been normalized for a unity width device.



a) Assuming that this device is an ideal long-channel MOSFET, estimate the threshold voltage of the device.

b) Assuming that this device is an ideal long-channel MOSFET, estimate the mobility of the electron inversion layer.

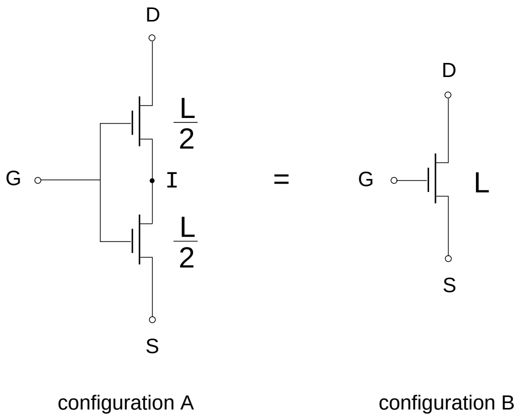
c) Assuming that this device is an ideal long-channel MOSFET, estimate the transconductance g_m at a bias of $V_{GS} = 3\ V$, and $V_{DS} = 3\ V$ for $W_g = 10\ \mu m$.

d) At a bias of $V_{GS} = 3\ V$, and $V_{DS} = 3\ V$, estimate the gate-source capacitance C_{gs} of a $W_g = 10\ \mu m$ device.

e) Now you are given the additional information that the inverse subthreshold slope of this transistor technology at room temperature is $S = 78\ mV/dec$. At a bias of $V_{GS} = 3\ V$, and $V_{DS} = 3\ V$, estimate the back-gate transconductance g_{mb} of a $W_g = 10\ \mu m$ device.

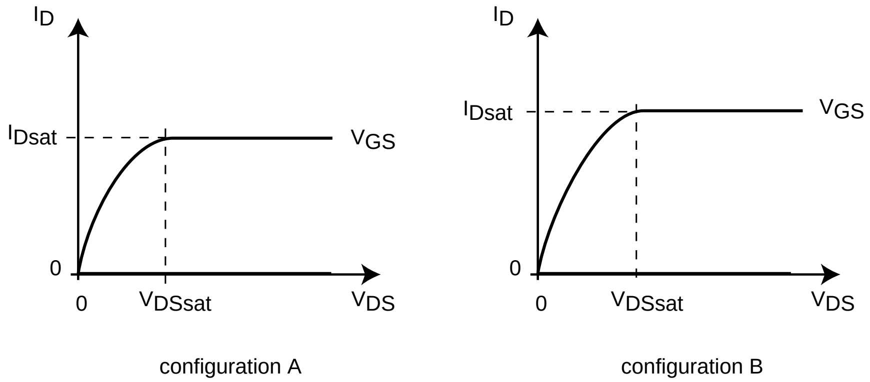
f) At a bias of $V_{GS} = 3\ V$, and $V_{DS} = 3\ V$, how much less current do you expect to have as a result of the body effect? (Considering the additional subthreshold current information, if needed).

4. *[20 points]* One of my colleagues asserts that:



This basically means that a configuration of two MOSFETs in series with a common gate voltage is equivalent to a single MOSFET with a channel length that is twice as long, all other aspects of the device unchanged. This problem is about evaluating this assertion for an ideal MOSFET (no body effect, no back bias, no channel length modulation, no short-channel effects).

Consider the following sketches of the I-V characteristics for these two configurations for the same value of V_{GS}:



Label the internal node in configuration A as "I", that is, refer to its voltage with respect to the source as V_{IS}.

a) For $V_{DS} > V_{DSsat}$, in what regime is each of the transistors in configuration A biased?

b) For configuration A and for $V_{DS} > V_{DSsat}$, derive equations for the drain current through each transistor as a function of V_{GS}, V_{DS}, V_T, and V_{IS}. From this, derive an expression for V_{IS}.

c) For configuration A, derive an expression for I_{Dsat} as a function of V_{GS}, V_{DS}, V_T and structural parameters. How does this compare with I_{Dsat} of configuration B for the same values of V_{GS} and V_{DS}?

d) For configuration A, derive an expression for V_{DSsat}. How does it compare with that of configuration B for the same V_{GS}?