Lecture 31 - The "Short" Metal-Oxide-Semiconductor Field-Effect Transistor *(cont.)*

November 18, 2002

Contents:

Reading assignment:

P. K. Ko, "*Approaches to Scaling.*"

Seminar:

Nov. 19 - C. Stork (TI): *Sub 100 nm Process Development for System-on-Chip Devices.* Rm. 34-101, 4 PM.

Key questions

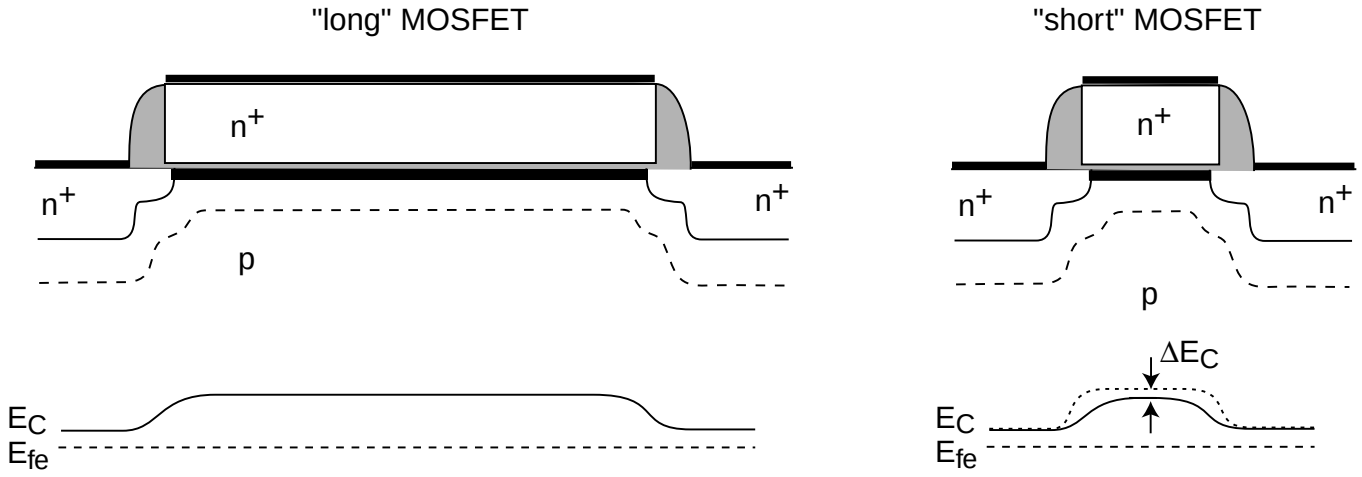
- Why does the threshold voltage seem to depend on the gate length of a MOSFET?
- Why does the threshold voltage of a MOSFET seem to depend on V_{DS}?

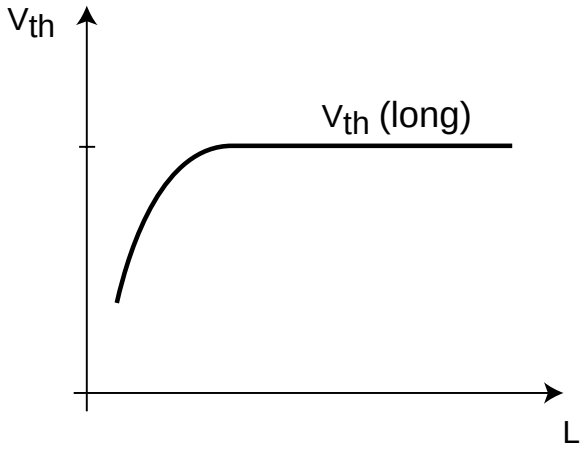
1. Short-channel effects

□ V_{th} dependence on L

Ideally, V_{th} does not depend on L, it only depends on x_{ox} and N_A.

If L is short enough, depletion regions of source and drain start overlapping underneath channel.



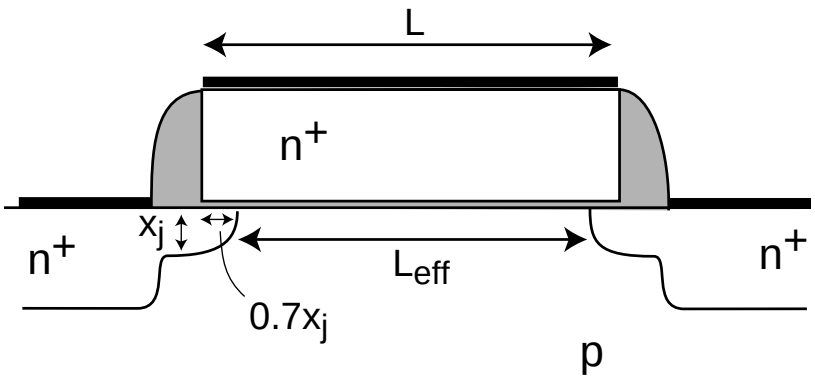


Complex 2D electrostatic problem:

- ΔV_{th} depends on the relative strength of the lateral electrostatics vs. the transversal electrostatics (*"electrostatic integrity"*).
- The tighter the gate controls ϕ_s, the weaker ΔV_{th} dependence on L.

Key dependencies:

- $x_{ox} \downarrow \Rightarrow |\Delta V_{th}| \downarrow$
- $N_A \uparrow \Rightarrow |\Delta V_{th}| \downarrow$
- $x_j \downarrow \Rightarrow L_{eff} = L - 2 \times 0.7\, x_j \uparrow \Rightarrow |\Delta V_{th}| \downarrow$



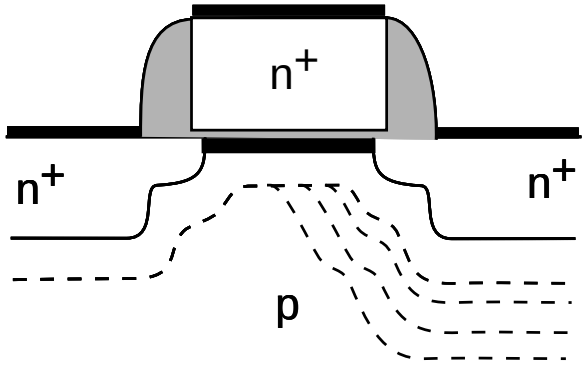
This is bad! long MOSFET: $V_{th} = f(x_{ox}, N_A)$
short MOSFET: $V_{th} = f(x_{ox}, N_A, L, x_j)$

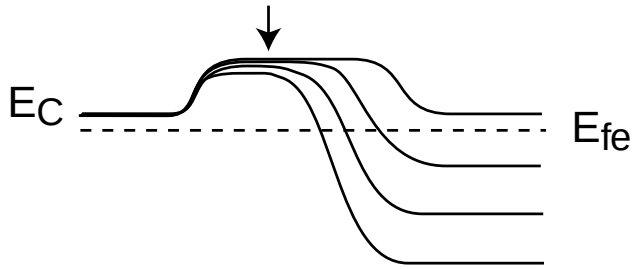
Most important consequence: V_{th} harder to control in manufacturing environment.

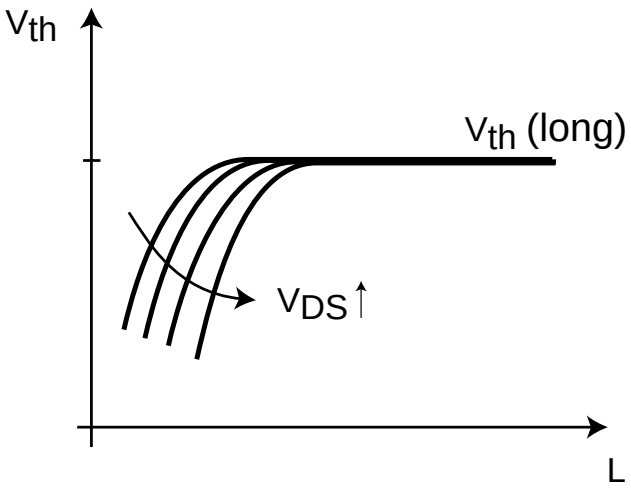
V_{th} model in next section.

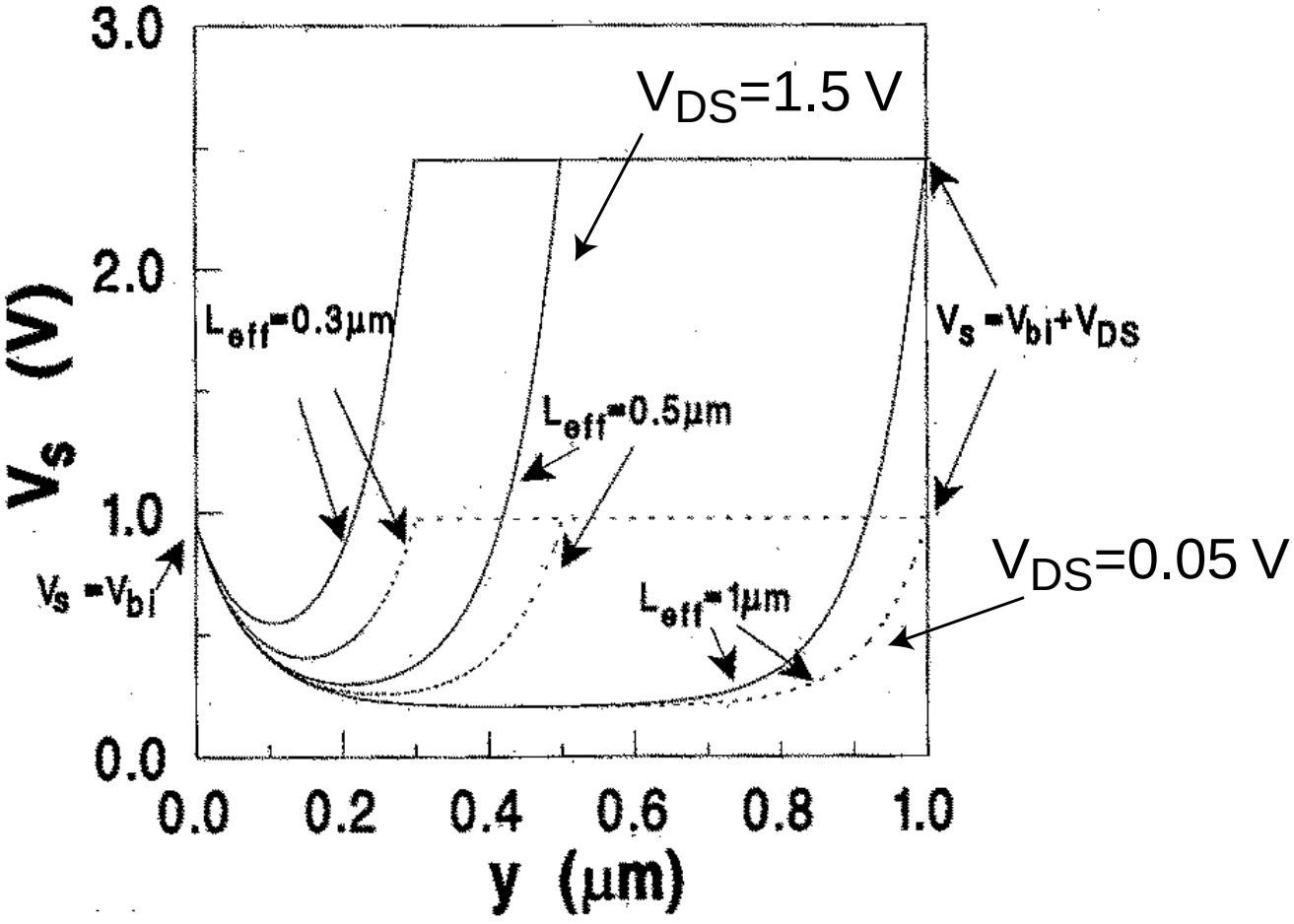
□ Drain-induced barrier lowering (DIBL)

Depletion region associated with drain junction expands as $V_{DS} \uparrow \Rightarrow$ additional V_{th} shift.









[from Liu et al., TED 40, 86 (1993)]

Simple analytical approximation to ΔV_{th} [Liu et al., TED 40, 86 (1993)]:

$$\begin{aligned}\Delta V_{th} &= [3(\phi_{bi} - \phi_{sth}) + V_{DS}]e^{-L_{eff}/\lambda} \\ &+ 2\sqrt{(\phi_{bi} - \phi_{sth})(\phi_{bi} - \phi_{sth} + V_{DS})}e^{-L_{eff}/2\lambda}\end{aligned}$$

with characteristic length:

$$\lambda = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} x_{ox} x_{dmax}}$$

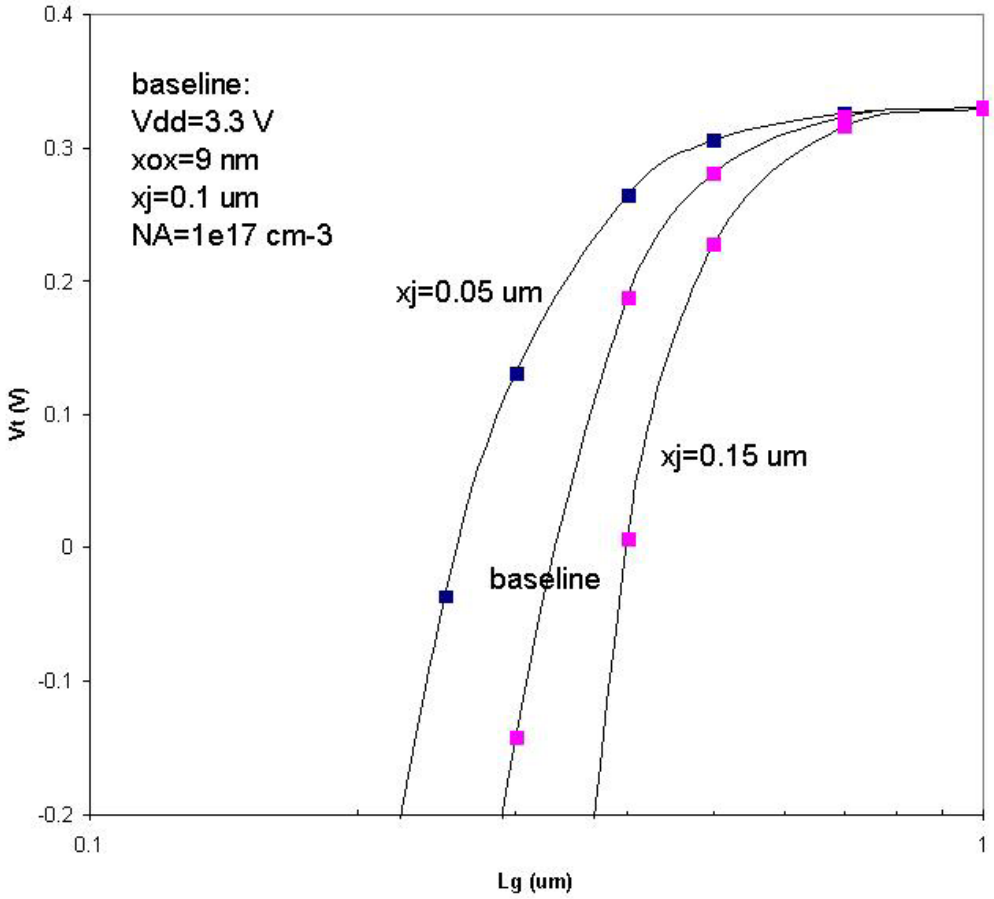
and

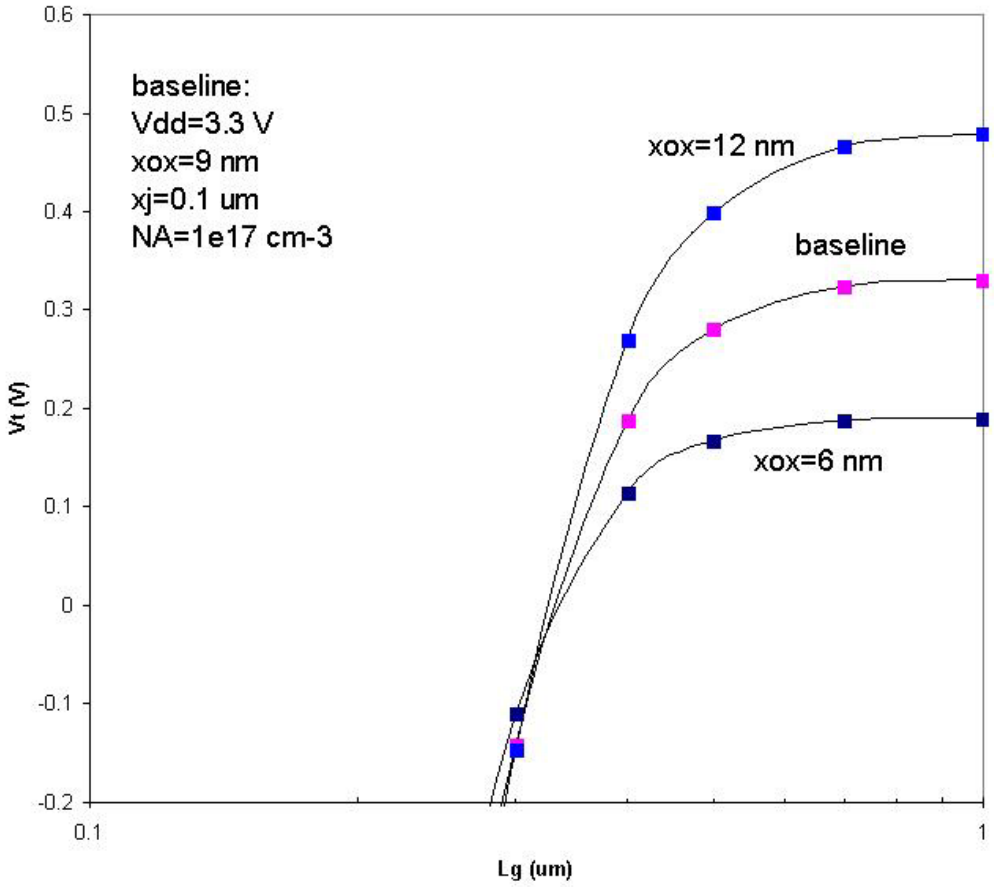
$$L_{eff} = L - 2 \times 0.7\, x_j$$

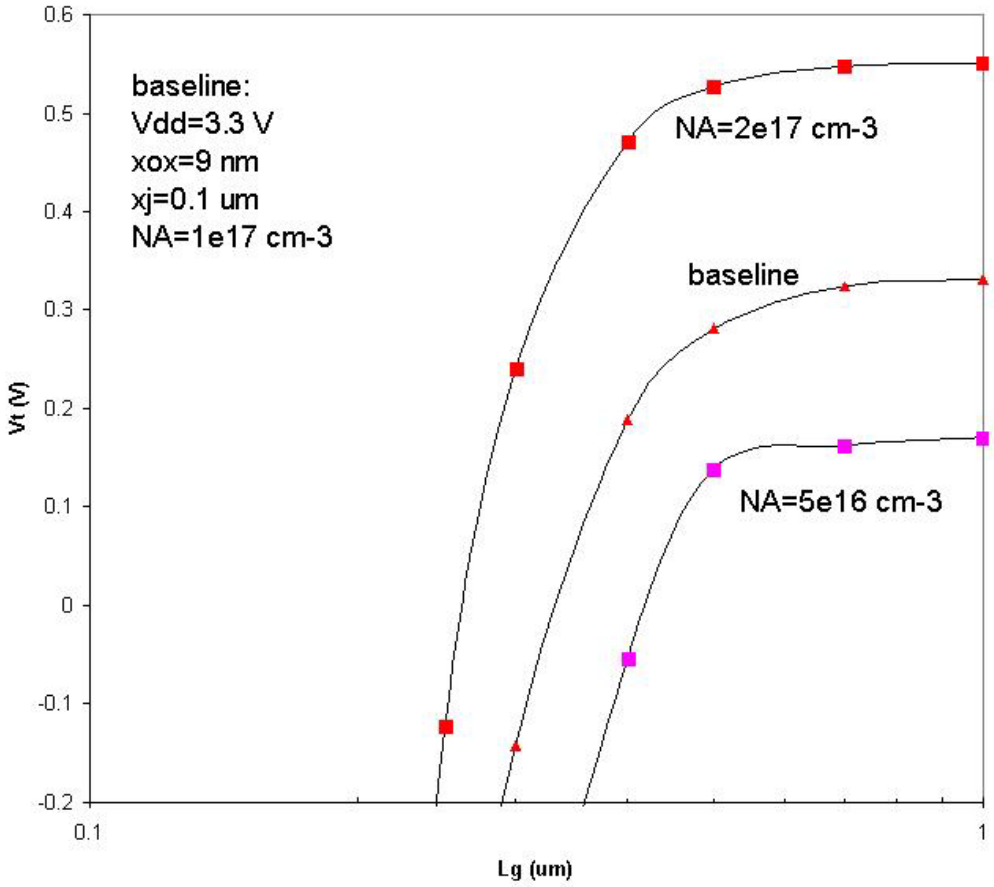
Quantification of DIBL:

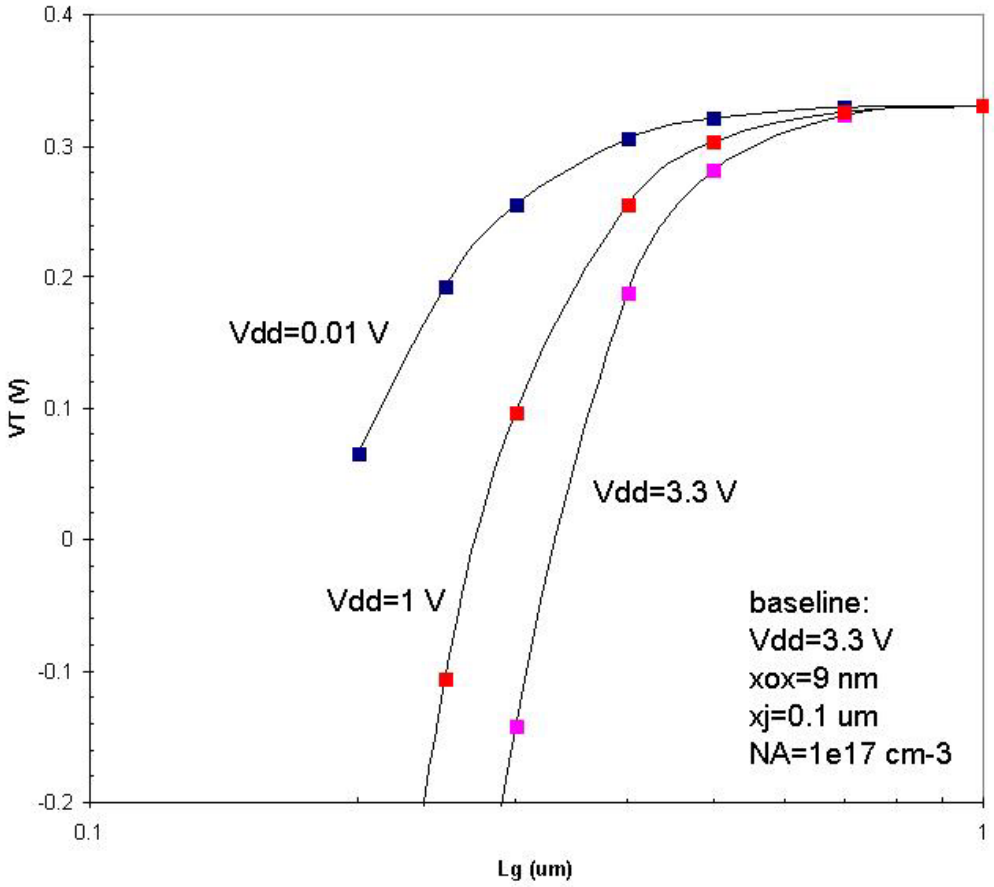
$$DIBL = |\frac{V_{th}(V_{DS} = V_{DD}) - V_{th}(V_{DS} = 0.1\ V)}{V_{DD} - 0.1}| \ \ mV/V$$

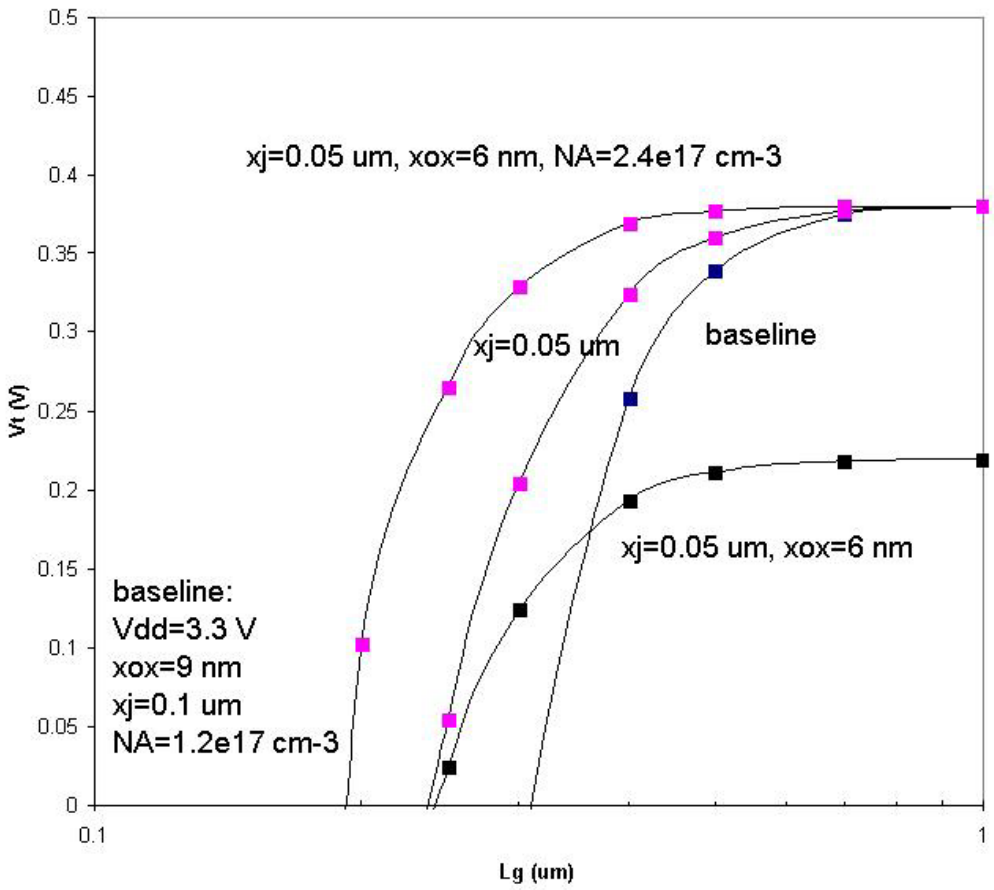
for a certain L device.


baseline:
Vdd=3.3 V
xox=9 nm
xj=0.1 um
NA=1e17 cm-3
xj=0.05 um
xj=0.15 um
baseline
Vt (V)
Lg (um)
0.4
0.3
0.2
0.1
0
-0.1
-0.2
0.1
1


baseline:
Vdd=3.3 V
xox=9 nm
xj=0.1 um
NA=1e17 cm-3
xox=12 nm
baseline
xox=6 nm
Vt (V)
Lg (um)
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
0.1
1


baseline:
Vdd=3.3 V
xox=9 nm
xj=0.1 um
NA=1e17 cm-3
NA=2e17 cm-3
baseline
NA=5e16 cm-3
Vt (V)
Lg (um)
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
0.1
1


0.4
0.3
0.2
0.1
0
-0.1
-0.2
VT (V)
0.1
1
Lg (um)
Vdd=0.01 V
Vdd=3.3 V
Vdd=1 V
baseline:
Vdd=3.3 V
xox=9 nm
xj=0.1 um
NA=1e17 cm-3



MOSFET design approach to manage DIBL:

1. shallower S/D junctions: $x_j = 0.1\ \mu m \rightarrow 0.05\ \mu m$
2. thinner gate oxide: $x_{ox} = 9\ nm \rightarrow 6\ nm$
3. increased body doping: $N_A = 1.2{\times}10^{17}\, cm^{-3} \rightarrow 2.4{\times}10^{17}\, cm^{-3}$

Comparison of simple model with 2D simulations:

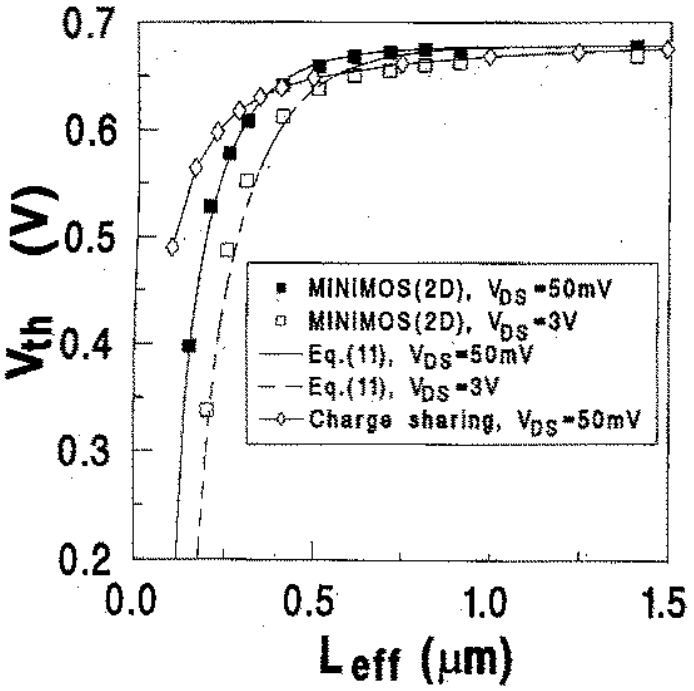


Fig. 4. A comparison of the V_{th} calculated using the charge sharing model, the two-dimensional numerical simulation (MINIMOS), and our model. The device parameters used are the same as those in Fig. 3.

[from Liu et al., TED 40, 86 (1993)]

Comparison of simple model with experiments:

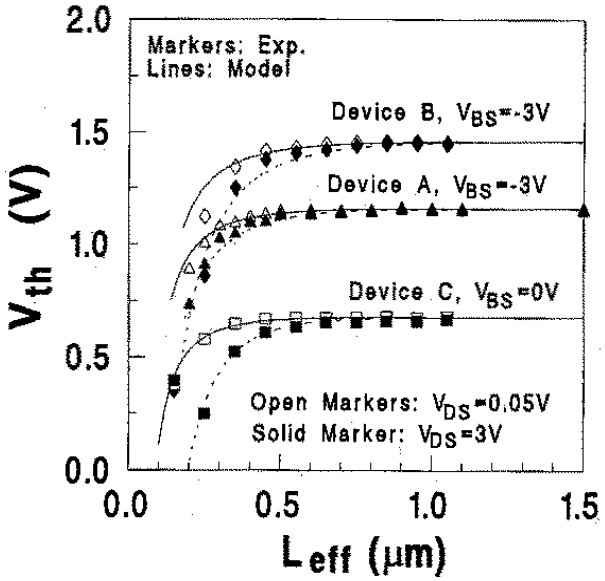


Fig. 5. Experimental and calculated threshold voltage versus effective channel length for non-LDD MOSFET's from different technologies, i.e., Device *A*: $T_{OX} = 55$ Å, $N_{SUB} = 3.6 \times 10^{17}\text{cm}^{-3}$, $X_j = 0.25$ μm, $l = 0.04$ μm; Device *B*: $T_{OX} = 86$ Å, $N_{SUB} = 1.5 \times 10^{17}\text{cm}^{-3}$, $X_j = 0.2$ μm, $l = 0.05$ μm; and Device *C*: $T_{OX} = 156$ Å, $N_{SUB} = 4 \times 10^{16}\text{cm}^{-3}$, $X_j = 0.2$ μm, $l = 0.09$ μm.

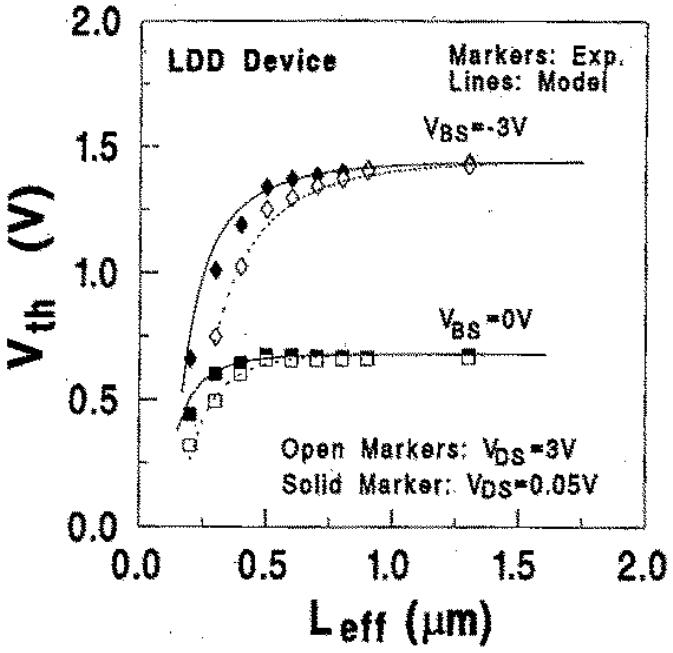
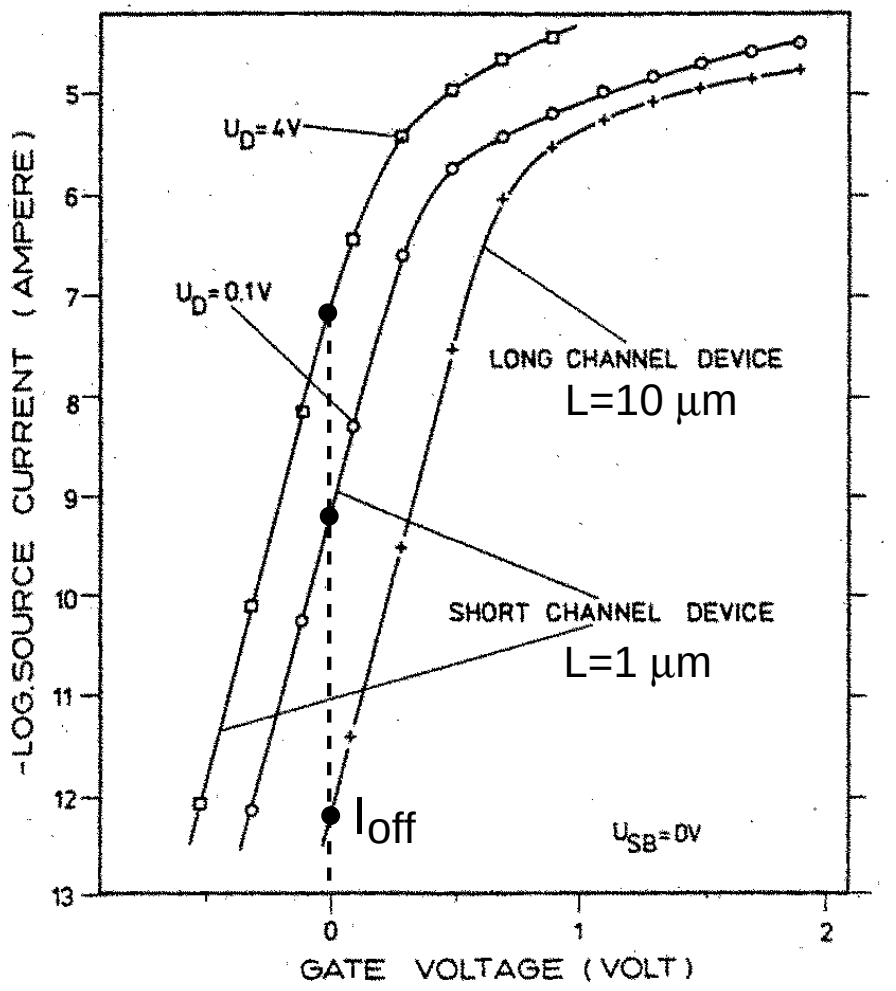


Fig. 7. Typical threshold voltage behavior for LDD device.

DIBL also affects I_{off}: $V_{DS} \uparrow \Rightarrow V_{th} \downarrow \Rightarrow I_{off} \uparrow$



[from Fichtner and Potzl, 1979]

Empirical criteria for short-channel effects (from 2D simulations):

Figure 1, Graph from: High-Speed Semiconductor Devices. S.M. S2- 1990 John Wiley & Sons.

Critical gate length for short-channel behavior (set by DIBL):

$$L_{min}\ (\mu m) = 0.41[x_j x_{ox}(W_S + W_D)^2]^{1/3}$$

with:

- $x_j \equiv$ source and drain junction depth $[\mu m]$
- $x_{ox} \equiv$ gate oxide thickness $[\mathring{A}]$
- $W_S, W_D \equiv$ source and drain depletion region thickness $[\mu m]$

Key conclusions

- V_{th} depends on L and V_{DS}:
  - For short L, V_{th} depends on L: $L \downarrow \Rightarrow V_{th} \downarrow$.
  - *Drain-induced barrier lowering (DIBL)*: impact of V_{DS} on V_{th}: $V_{DS} \uparrow \Rightarrow V_{th} \downarrow$.
- ΔV_{th} reflects relative strength of lateral electrostatics vs. transveral electrostatics (*"electrostatic integrity"*).
- Electrostatic integrity improves if $x_{ox} \downarrow$, $N_A \uparrow$, $L \uparrow$, $x_j \downarrow$.
- DIBL problematic because:
  - V_{th} hard to control
  - $I_{off} \uparrow$