New Architectures for RF Power Amplifier Linearization

by

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Abstract

Power amplifier linearization has become an important part of the transmitter system as 3G and developing 4G communication standards require higher linearity than ever before. The thesis proposes two power amplifier linearization solutions : two-point architecture and adaptive digital predistortion using a $\Delta\Sigma$ modulator for automatic inversion of power amplifier nonlinearity.

Two-point architecture can be seen as a solution that extends the linearization bandwidth of the traditional feedback architecture while also offering decent digital predistortion linearization at much higher frequencies as well. It overcomes the bandwidth problem by combining Cartesian feedback and digital predistortion. As the Cartesian feedback loses its loop gain in high frequencies, the predistorted signal gradually takes over the linearization role. Effectively, this increases the operation bandwidth of the Cartesian feedback and allows wide-band transmission.

For digital predistortion, the complexity involved in the implementation of adaptive algorithm and convergence issues in the look-up table training has limited its application in handset devices. Predistortion using a $\Delta\Sigma$ modulator presented in this work eliminates these problems as it is based on open-loop look-up table training and does not require adaptive algorithm.

Thesis Supervisor: Joel L. Dawson
Title: Assistant Professor

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Reminiscing my student life during my master's work here at MIT, I am grateful for having been part of such a special community. I realize that I have developed tremendously, not just as a student, but also as a better person.

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Chapter 1

Introduction

1.1 The Need for Linear Transmitters

The demand for high data rate wireless transmission has increased significantly in the last several decades. Previously, systems based on frequency modulation, such as GSM, have been dominant. However, frequency modulation has low spectral efficiency and low data rate. To cope with the problem, spectrally efficient variable-envelope modulation strategies have been increasingly deployed. There is now high consumer demand for complex air interfaces such as WCDMA, HSUPA, CDMA2000 EV/DO, and WiMAX. These systems feature signals that are high bandwidth and have high peak-to-average power ratios (PAPR). This sets challenges in designing the transmitter as amplitude modulated signals are sensitive to the linearity.

The power amplifier (PA) now determines the performance bottleneck. Transceivers designed to succeed in wireless markets continue to suffer the difficult design tradeoff between PA linearity and efficiency. RF designers have traditionally operated the PA well below its most efficient point to reach satisfactory linearity. This is exacerbated by the fact that evolving communication standards will require transmission of signals with increasing PAPR to accommodate higher data rate. This indicates that even higher backoff is necessary, leading to even bigger efficiency problem. Efficiency, however, is a very important factor in mobile terminals and needs to be maximized as much as possible. This has stimulated the investigation of PA linearization techniques that soften the traditional linearity

and efficiency tradeoff.

1.2 PA Nonlinearity

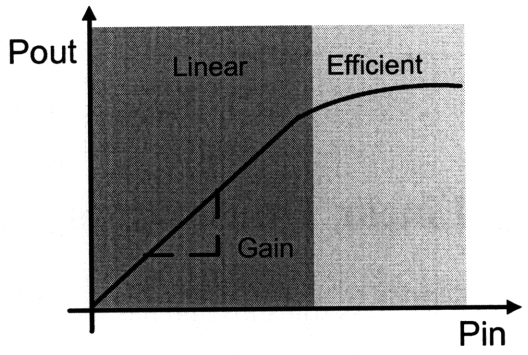


Figure 1-1: PA characteristics

Two different type of nonlinearities characterize the PA distortions: static nonlinearity and memory effects. Static nonlinearity is the time-independent or frequency-independent distortions in the PA shown in Fig. 1-1. It often refers to amplitude-to-amplitude (AM/AM) and amplitude-to-phase (AM/PM) nonlinearity. Memory effects, on the other hand, is the time-dependent or frequency-dependent distortions caused by PA self-heating and biasing changes. The combination of these two is illustrated in Fig. 1-2. In the time domain, for a modulated signal going into the PA, the PA outputs an amplified version of the input with gain compression observed in the high swing section. This compressive nonlinearity becomes more severe as the PA reaches higher output. Also, even with the same input signal, the PA displays different output behavior depending on the PA conditions. In the frequency domain, a two-tone test output spectrum displays intermodulation distortions. These distortions are comprised of consistent static nonlinearity and nonlinearity that have varying amplitude and phase at different frequencies.

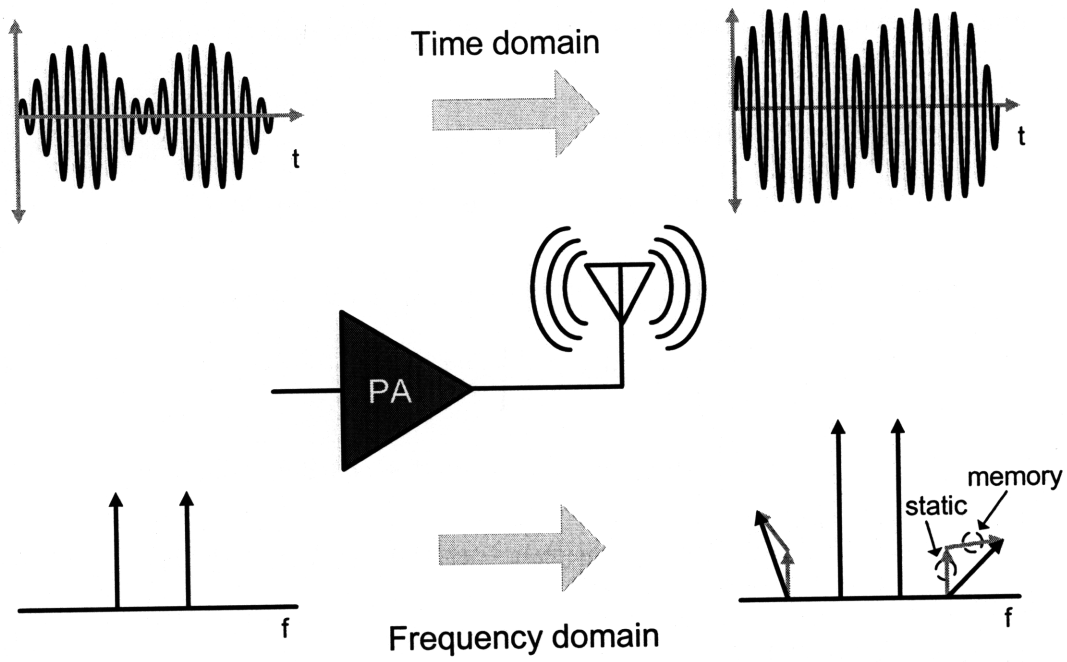


Figure 1-2: Nonlinear behavior of PA.

1.2.1 Static Nonlinearity

The static PA behavior can be modeled by a power series expansion

$$y \approx k_1 x + k_2 x^2 + k_3 x^3 \tag{1.1}$$

where x represents the input and y is the output quantity. Power series is limited up to third order for simplicity. Suppose that the input signal includes two tones:

$$v_i(t) = a_1 cosw_1 t + a_2 cosw_2 t \tag{1.2}$$

then

$$\begin{aligned} v_0(t) \approx\ & k_1 \left[a_1 cosw_1 t + a_2 cosw_2 t\right] \\ & + k_2 \left[a_1 cosw_1 t + a_2 cosw_2 t\right]^2 \\ & + k_3 \left[a_1 cosw_1 t + a_2 cosw_2 t\right]^3 \end{aligned} \tag{1.3}$$

The output can be rewritten in terms of first, second and third order nonlinearity.

$$\begin{aligned}
v_0(t)_{1^{st}} &= k_1\left[a_1 cosw_1 t + a_2 cosw_2 t\right] \\
v_0(t)_{2_{nd}} &= k_2\left[\frac{1}{2}(a_1^2+a_2^2)+\frac{1}{2}a_1^2 cos2w_1 t+\frac{1}{2}a_2^2 cos2w_2 t\right] \\
v_0(t)_{3_{rd}} &= k_3\left[(\frac{3}{4}a_1^3+\frac{3}{2}a_1a_2^2)cosw_1 t+(\frac{3}{4}a_2^3+\frac{3}{2}a_1^2a_2)cosw_2 t\right] \\
&\quad +k_3\left[\frac{1}{4}a_1^3 cos3w_1 t+\frac{1}{4}a_2^3 cos3w_2 t\right] \\
&\quad +k_3\left[\frac{3}{4}a_1a_2^2\left(cos(2w_2-w_1)t+cos(2w_2+w_1)t\right)\right] \\
&\quad +k_3\left[\frac{3}{4}a_1^2a_2\left(cos(2w_1-w_2)t+cos(2w_1+w_2)t\right)\right] \qquad (1.4)
\end{aligned}$$

The effective gain of the PA is

$$k_1a_1+k_3\frac{3}{4}a_1^3+\frac{3}{2}a_1a_2^2 \qquad (1.5)$$

for $cosw_1t$ and

$$k_1a_2+k_3\frac{3}{4}a_2^3+\frac{3}{2}a_1^2a_2 \qquad (1.6)$$

for $cosw_2t$. k_1 and k_3 have opposite sign, and the PA exhibits more compressive nonlinearity with increasing input signal magnitude. The derivation shows that the PA nonlinearity give third order terms that are spectrally adjacent to the ideal first order locations. Although, the second order terms are located far away and can be filtered away, the third order terms fall within the band of interest and cannot be suppressed by filtering.

1.2.2 Memory Effects

In two-tone tests, memory effects manifest as intermodulation distortion products whose amplitudes and phase vary with the spacings of the two tones [1–3]. This dynamic distortion can be categorized into electrical memory or thermal memory. Electrical memory is caused by variation in PA terminal impedance. The varying biasing and impedance seen at

baseband and harmonic frequencies modulate the second order intermodulation distortion terms to add on top of the third order terms, leading to bigger spectral regrowth. Thermal memory is caused by the changes in temperature. The instantaneous dissipated power generates heat and the temperature-dependent transconductance fluctuates the PA gain. Since temperature changes slowly, thermal memory manifests in narrowband signals up to 1MHz.

1.3 Research Contribution

This thesis focuses on two different linearization systems, a two-point linearization architecture and a predistorting $\Delta\Sigma$ modulator.

The two-point linearization architecture in Chapter 3 combines the strengths of the Cartesian feedback (CFB), chiefly memory effect suppression and relaxed PA modeling requirements, with the increased speed of open-loop digital predistortion. CFB is initially used to efficiently train a look-up table (LUT) for a predistorted feedforward path. Then, both the CFB and the predistorted feedforward path run simultaneously during transmission. This offers the benefit of highly linearized output while extending the bandwidth of traditional feedback systems.

The predistorting $\Delta\Sigma$ modulation architecture is particularly suited to mobile handset applications and is explored in Chapter 4. The central idea is to build a LUT that directly captures the static, compressive nonlinearity of the power amplifier, and then insert this LUT into the *feedback path* of a $\Delta\Sigma$ modulator. The oversampled $\Delta\Sigma$ modulator automatically performs both the inversion of the PA nonlinearity and the interpolation between LUT entries, permitting complex modulation strategies to be handled with an absolute minimum of LUT entries and with a dramatically simplified computational structure. The advantages of this architecture over previous methods include: there is no need to explicitly invert the PA nonlinearity, reducing the complexity for the system designer; the LUT training is done with an open-loop method, improving training speed; there is no need to explicitly employ numerical interpolation between LUT entries; DAC nonlinearity is incorporated into the predistortion, allowing, fast, low-resolution DACs to be used in the final system.

Chapter 2

Power Amplifier Linearization Overview

2.1 Introduction

This chapter provides an overview of PA linearization methods. Specifically, the focus is placed on feedback and digital predistortion of PA linearization as these two techniques form the fundamental blocks in the two-point linearization in Chapter 3 and using a $\Delta\Sigma$ modulator in Chapter 4.

2.2 Feedforward

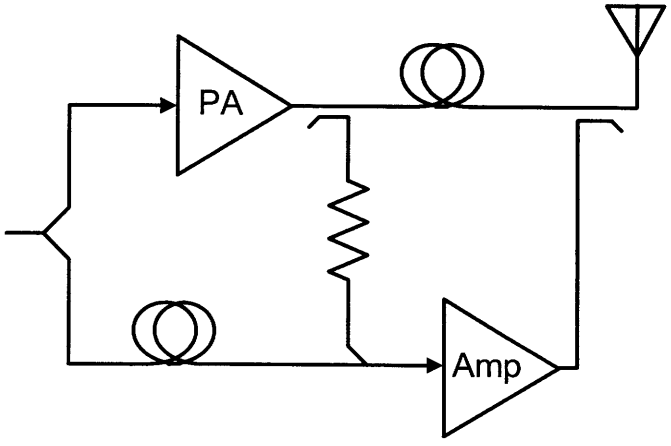


Figure 2-1: Feedforward linearization.

Proposed by Black [4], the feedforward linearization in Fig. 2-1 consists of a signal-cancellation loop followed by a error-cancellation loop. In the signal-cancellation loop, an attenuated sample of the PA output distortion is subtracted with a delayed version of the PA input signal. The sampling coupler and fixed attenuation are chosen to match the PA gain. Therefore, only the PA distortion components are extracted. This signal is linearly amplified in the error-cancellation loop and injected in anti-phase to the delayed version of the PA output. At the output of the error-cancellation loop only appears the ideally amplified version of the input signal.

Feedforward has been popular for base station applications since the lack of feedback path allows wide-band operation with significant linearity improvement. However, it suffers from practical issues as the delay between the parallel branches need to be accurately aligned [5]. The performance is sensitive to the gain and phase variation of the error amplifier as these nonlinearities cannot be corrected. Further, having two amplifiers significantly worsens the overall efficiency. Also, the bulky size and the cost of and the isolators, couplers, and delay lines make it an unlikely on-chip solution.

2.3 Feedback

Feedback is a traditional method known to suppress not only static nonlinearity, but time-dependent nonlinearities as well. Envelope detection and CFB are the most extensively explored techniques among many different feedback variations. Envelope feedback compares the envelope of the PA input and output to adjust the RF signal to compensate for the nonlinearity [6–8]. Cartesian feedback, on the other hand, requires the baseband signal and the demodulated quadrature PA output signal and have been demonstrated for up to 30dB reduction in intermodulation distortion [9–11].

Feedback systems boast high linearity and have been demonstrated for GSM/EDGE and WCDMA [8, 10]. Unfortunately, the technique enjoys only limited application. This is because high group delays from passive components in the signal path render high closed-loop bandwidths impossible. Even for handset PAs, where output power is only 1-2 Watts, the need for SAW filters in the forward path makes the implementation difficult [12].

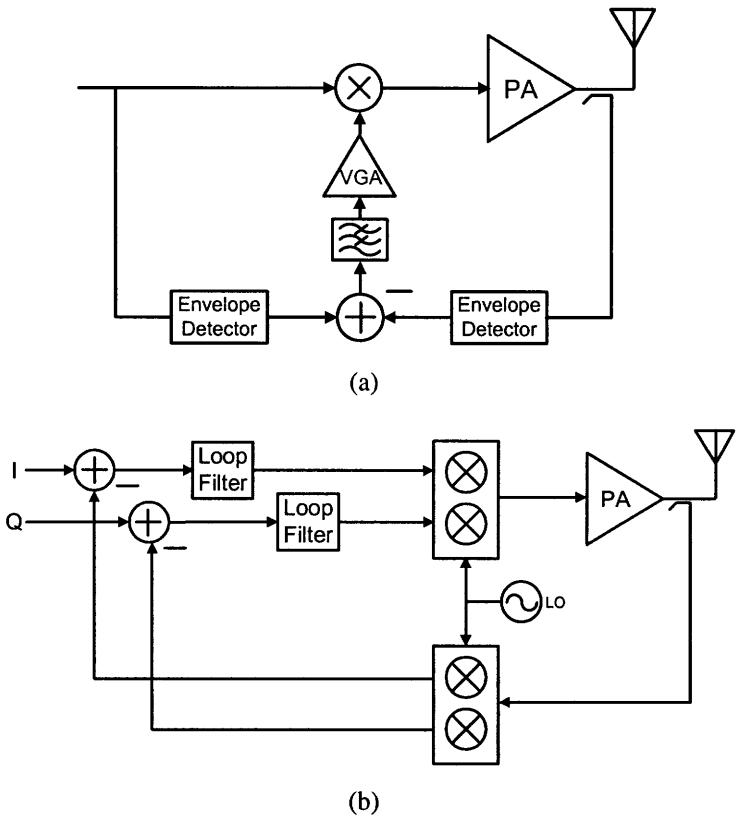


Figure 2-2: Feedback linearization using (a) envelope detection, (b) CFB.

2.4 Digital Predistortion

Digital predistortion (DPD) has established itself as the dominant linearization technique [12–18]. The central idea is to precede the PA with a LUT that captures the functional inverse of the PA nonlinearity, such that the overall cascade is linear as shown in Fig. 2-3. The LUT training relies on feedback and adaptive algorithm, and upon completion, the feedback is turned off for fast open-loop operation.

The implementation is mainly categorized into mapping predistortion or complex-gain predistortion as shown in Fig. 2-4. In mapping predistortion, the two-dimensional LUT stores the predistorted signal. The LUT takes Cartesian baseband signal as the input and outputs a corresponding corrected signal. This straightforward solution however requires large memory [17]. To reduce the LUT size, the LUT output can be interpolated to increase the virtual number of LUT entries at the cost of added complexity [12,19,20]. On the other hand, multiplying the input with a complex-gain as shown in Fig. 2-4(b) requires less

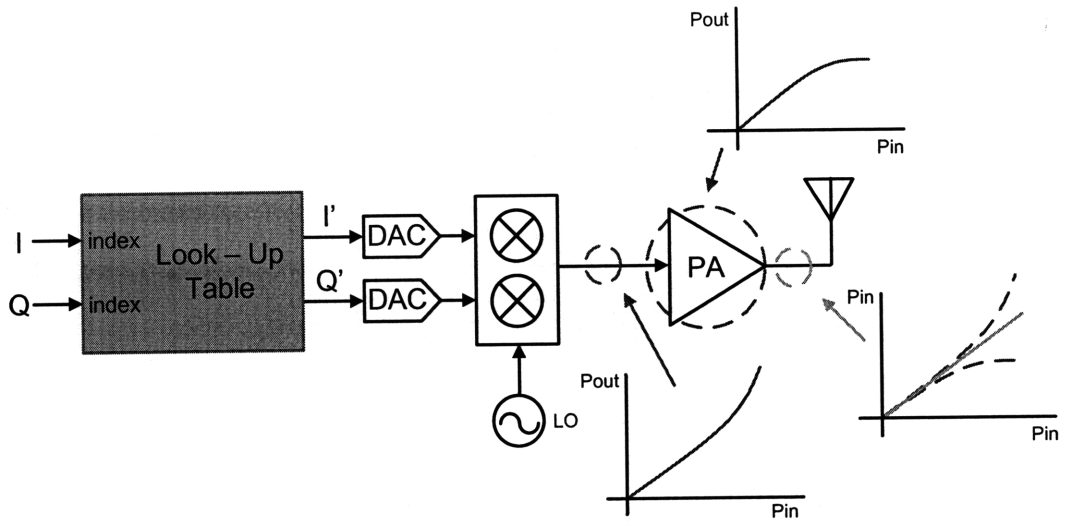


Figure 2-3: Digital predistortion.

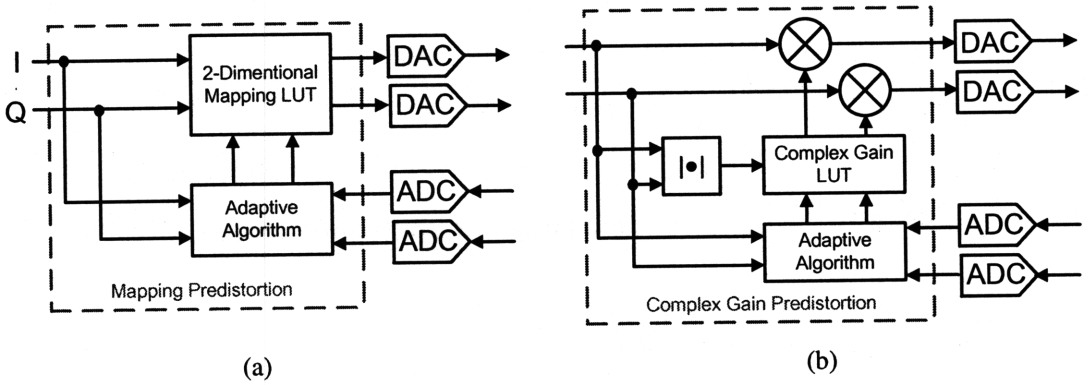


Figure 2-4: Digital predistortion implementaion using (a) mapping LUT, (b) complex-gain LUT.

LUT size. It uses either the input magnitude or magnitude-squared to calculate the LUT addressing and improves adaptation time [13, 14].

Systems that use DPD, however, share fundamental difficulties. First of all, these systems do not account for changes in PA conditions. Although it can be designed to be adaptive by continuously updating the LUT during data transmission, this is a power-hungry operation. Stability and/or convergence issues associated with closed loop control must be handled as well. Further, computational overhead is added since the systems depend on full characterizations of the PA nonlinearity and then mathematically inverting that characterization in order to do predistortion. Mathematical inversion does not present a fundamental

difficulty, but it is computationally intensive. Also, predistortion extends the original signal bandwidth by $5\times$. This puts heavy burden on the digital to analog converters (DACs) as high resolution and high speed are required.

Chapter 3

Two-Point Linearization

3.1 Introduction

Recently, a system was demonstrated that combined many of the advantages of CFB and DPD [12, 21]. The relaxed PA modeling requirements of the former were retained, while the bandwidth of the latter was fully exploited. The CFB is used as a way of training a LUT. Once the LUT is established, the system functions as an ordinary, open-loop predistorter. The outstanding feature of this architecture is that, because the training process can be done slowly, the filling of the LUT can be done with extremely low energy overhead. However, unlike the more sophisticated adaptive predistortion systems, it is not capable of suppressing PA memory effects.

This work builds on Chung's work [12] and introduce a new two-point architecture for PA linearization. The main advantage of this new architecture is that it allows for the suppression of PA memory effects, while still permitting broader bandwidth transmission than unaided CFB. Two-point architectures have long been used in high-speed PLLs [22–25]. In those cases, though, the nonlinearity of the VCO/DCO was not so severe as to require predistortion in the feedforward path. In the system described here, both CFB and a predistorted feedforward path run simultaneously as shown in Fig. 3-1. In addition, we leverage the system of [12] to retain all the power advantages of using CFB to train the LUT.

This chapter starts with an analysis showing how the two-point architecture performs.

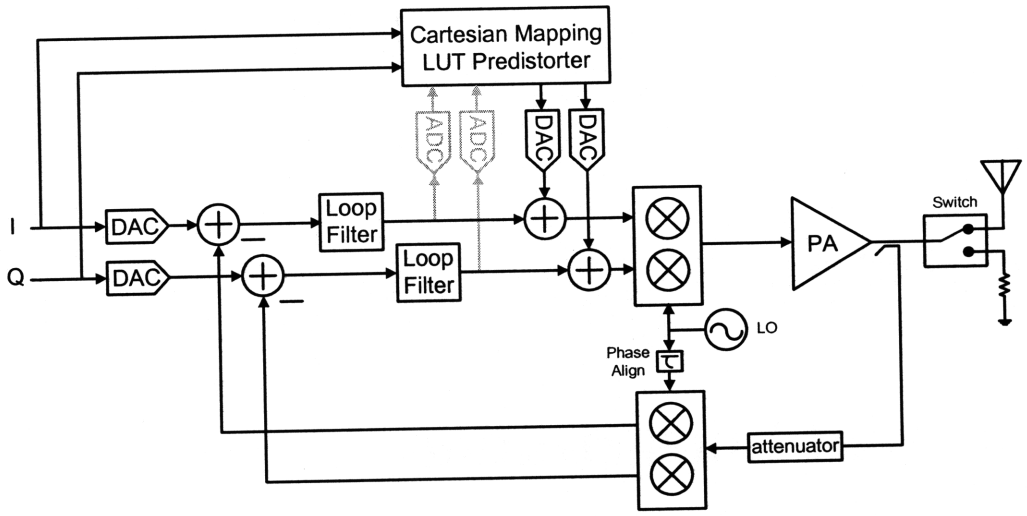


Figure 3-1: Proposed two-point linearization combining CFB and DPD.

The two-point linearization performance is described relative to the Cartesian feedback and DPD linearization for different baseband bandwidths. Then, widely explored memory polynomial PA model is used as a basis for simulation and the results are presented.

3.2 Analysis of the Two-Point Architecture

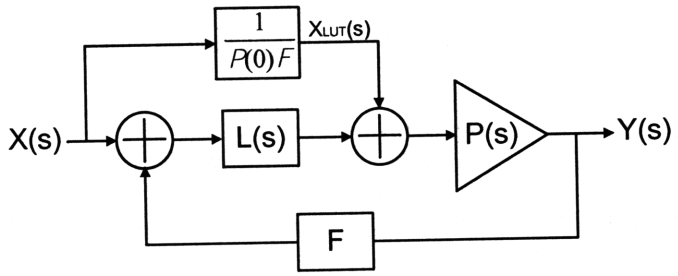


Figure 3-2: Block diagram of the two-point architecture.

A two-point architecture allows for a tradeoff between memory effects compensation and high modulation bandwidth. A simplified two-point architecture is shown in Fig. 3-2. In this diagram, $L(s)$ represents all of the gain and dynamics in the forward path preceding the power amplifier, and $P(0)$ represents the static characteristics of the power amplifier as seen at baseband. For purposes of our analysis, f_{3dB} is the -3dB frequency of $L(s)$

and f_{unity} is the frequency at which the magnitude of the loop transmission, $L(s)P(s)F$, crosses unity.

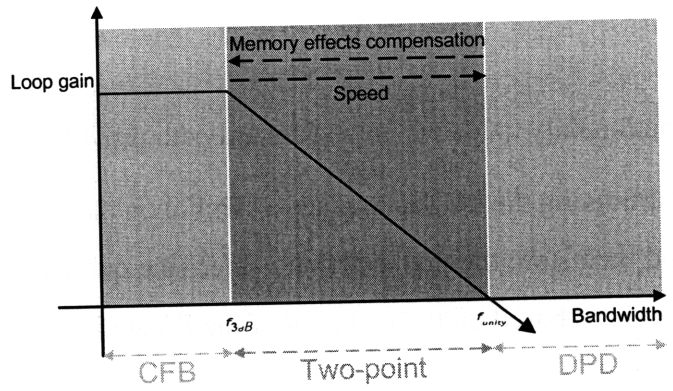


Figure 3-3: Illustration of the two-point linearization range compared to CFB and DPD.

Fig. 3-3 can be used to illustrate the tradeoff this architecture affords between linearization bandwidth and memory effects suppression. In the first region, for bandwidths below f_{3dB}, the loop gain is high and the feedforward path is almost completely rejected. The feedback system compensates for all nonlinearities, including memory effects. In the third region, for bandwidths exceeding f_{unity}, the feedback system's capacity for correction is exceeded and only memoryless nonlinearity can be corrected by the still-active feedforward path. The middle is a tradeoff region, where the memory effects suppression is superior to DPD, but where the bandwidth for a given linearity is superior to that achievable by CFB alone. It is in this region that the two-point architecture can be used to the greatest advantage.

3.2.1 System Transfer Function

Fig. 3-2 shows the block diagram of the two-point architecture. F is the feedback attenuation and $P(s)$ represents the PA transfer function.

If only the CFB is considered without the feedforward path, the output is characterized

by

$$\begin{aligned} Y_c(s) &= \frac{L(s)P(s)}{1+L(s)P(s)F}X(s) \\ &\approx \frac{1}{F}X(s). \end{aligned} \tag{3.1}$$

The above approximation only holds when the forward path provides high gain.

The procedure for training the LUT is to place a symbol on the I and Q inputs, wait for the loop to settle, and then store the predistortion values (the output of the loop filters) as the LUT entry. The LUT is based on the mapping of the PA static characteristics, and that is captured mathematically as

$$\begin{aligned} X_{LUT}(s) &= \frac{L(0)}{1+L(0)P(0)F}X(s) \\ &\approx \frac{1}{P(0)F}X(s) \end{aligned} \tag{3.2}$$

If this data is used solely for DPD [12], The output of the PA could be expressed as

$$Y_{DPD}(s) = \frac{P(s)}{P(0)F}X(s). \tag{3.3}$$

In the two-point architecture, however, the feedback loop and the predistortion path work together. The adders before the PA combine the CFB and DPD. Combining results,

$$\begin{aligned} Y_{tp}(s) &= \frac{L(s)P(s)}{1+L(s)P(s)F}X(s) + \frac{P(s)}{P(0)F}\frac{1}{1+L(s)P(s)F}X(s) \\ &= \frac{\left[L(s)P(s)F + \frac{P(s)}{P(0)}\right]}{F[1+L(s)P(s)F]}X(s). \end{aligned} \tag{3.4}$$

A striking feature noticeable here is that if the PA doesn't have any memory effect, $P(s) = P(0)$ and the system output is exactly $\frac{X(s)}{F}$ across all bandwidths. The stronger the memory effects in the PA, the more two-point linearization relies on loop gain for memory effects compensation. For PAs with strong memory effects, the two-point architecture will

result in better distortion compensation for lower frequencies than for higher frequencies.

It is useful to compare two-point linearization directly with CFB and then with DPD. When comparing with CFB, infinite loop gain at all frequencies would result in $Y_{tp}(s) = Y_c(s)$. When the loop gain drops at high frequencies, CFB loses its linearization capability. Returning to equation 3.4 and examining it in the limit of $L(s)P(s)F << 1$, $Y_{tp}(s)$ reduces exactly to equation 3.3, $Y_{DPD}(s)$ and the quality of linearization depends on the relative strength of the memory effects in the PA. Qualitatively, between f_{3dB} and f_{unity}, the linearization ability of the unaided CFB system is boosted, effectively extending its linearization bandwidth.

Comparing DPD and two-point, both benefit from the condition $P(s) \approx P(0)$. Two-point, however, is less sensitive to this condition since the large loop gain of the CFB masks any inaccuracy of the feedforward predistortion path. Ultimately, two-point linearization gives better performance than DPD at frequencies where loop gain is available. As the loop gain falls to unity or below at high frequencies, $Y_{tp}(s) \approx Y_{DPD}(s)$ and two-point linearization performance converges to that of DPD.

To summarize, the CFB part of the two-point architecture linearizes signals at low frequencies in a lowpass type fashion while DPD works in a highpass type fashion and linearizes only the signals at high frequencies. This architecture can be viewed as either an enhancement of CFB, or as an enhancement of DPD. In the case of the former, the feedforward path is a bandwidth enhancement technique. In the case of the latter, it adds memory effects suppression to DPD while adding very little in the way of computational overhead.

Two-point linearization can be implemented with any feedback and open-loop predistortion scheme. All that is needed is a summing junction for the two linearization techniques. For example, there is no reason in principle this idea cannot be applied to a polar modulated transmitter.

3.3 Simulation

A dynamic PA model is needed to represent spectrum asymmetries caused by memory effects. The method proposed in [26–28] uses sparse delay taps and nonlinear static functions

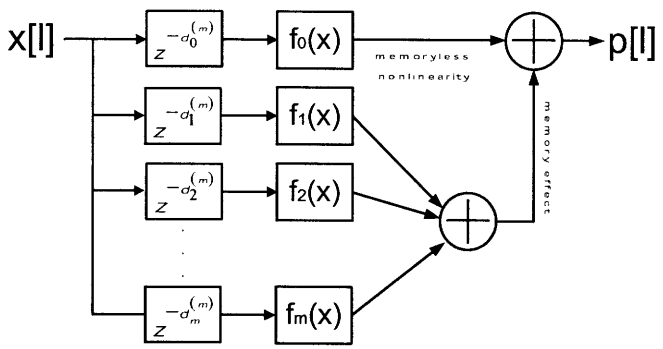


Figure 3-4: Memory polynomial model with sparse delay.

to model memory effects and odd-order bandpass nonlinearity. The discrete baseband PA model in Fig. 3-4 is represented as follows:

$$p[l] = \sum_{q=0}^{m} \sum_{k=1}^{n} a_{2k-1,q} \left| x\left[l - d_q^{(m)}\right] \right|^{2(k-1)} x[l-q] \tag{3.5}$$

where x[l] is the discrete input complex envelope, $d_q^{(m)}$ is the delay tap at the $(m+1)$th parallel branch and p[l] is the discrete output complex envelope. The model uses parallel finite impulse response (FIR) filters each cascaded by polynomial function

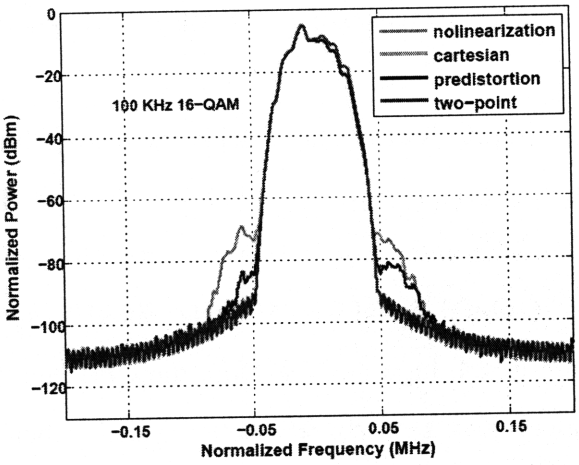
$$f_q(x) = \sum_{k=1}^{n} a_{2k-1,q} |x|^{2(k-1)} x. \tag{3.6}$$

The first branch represents the memoryless AM/AM and AM/PM nonlinearity, and adding parallel branches incorporates the memory effect into the model. If $p[l]_q$ is the output of qth parallel branch, then

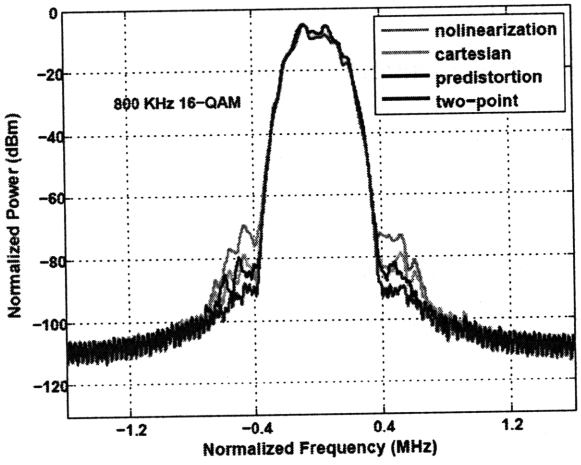
$$p[l] = \sum_{q=0}^{m} p[l]_q. \tag{3.7}$$

Adding more parallel branches increases the memory model accuracy at the cost of convergence speed.

Using the coefficients in [26] for the sparse delay memory polynomial PA model, four cases were simulated: CFB, DPD, two-point, and no linearization. The feedback system is characterized by $f_{3dB} = 14$kHz and $f_{unity} = 1.4$MHz with a loop gain of 40dB. The result is shown in Fig. 3-5 for 16-QAM signal with 100kHz, 800kHz, and 2MHz of bandwidth. At 100kHz, the loop gain is still high and therefore the CFB and two-point linearization outputs are almost identical, giving nearly 8dB better linearity than DPD. At 100kHz, the CFB already performs worse than the DPD while two-point linearization gives the best linearity. For 2MHz 16-QAM, the CFB leads to output attenuation and DPD and two-point linearization outputs are almost identical. The results confirm the expectation.



(a)



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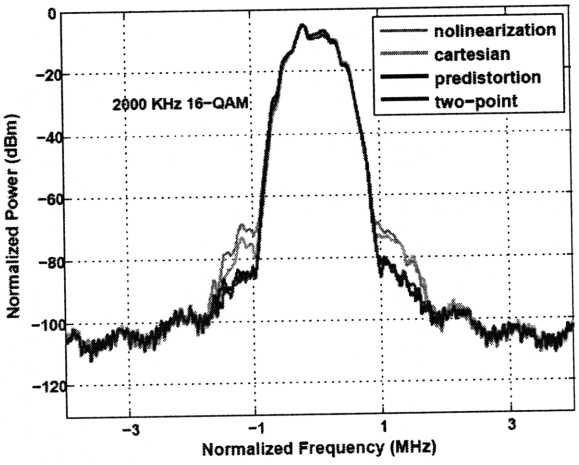

(c)

Figure 3-5: The simulated linearization spectrum for system with $f_{3dB} = 14$KHz and $f_{unity} = 1.40$MHz with 16-QAM input bandwidths of (a) 100KHz, (b) 800KHz, and (c) 2000KHz.

Chapter 4

Predistorting $\Delta\Sigma$ Modulator

4.1 Introduction

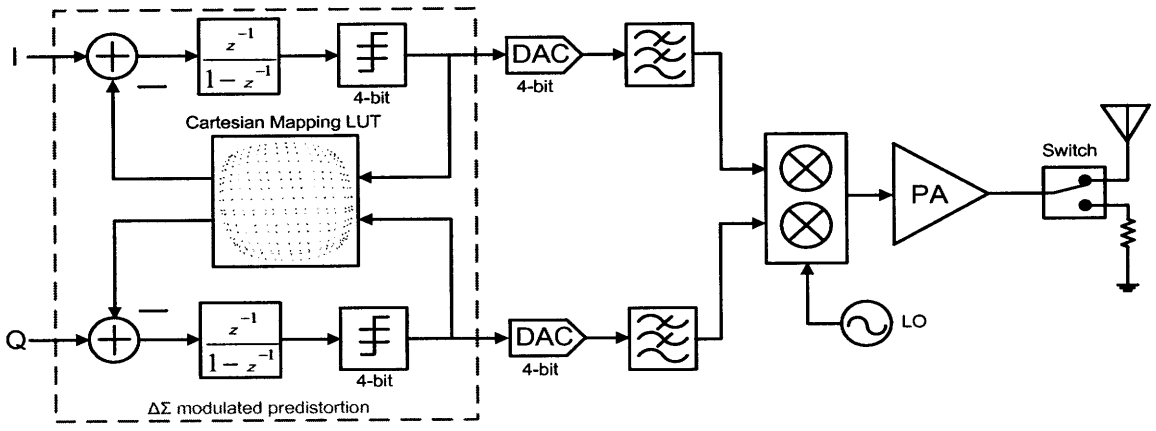

Figure 4-1: Proposed predistorting $\Delta\Sigma$ modulator.

The proposed simple and effective adaptive DP architecture using a $\Delta\Sigma$ modulator is shown in Fig. 4-1. It requires less complexity than other adaptive predistortion techniques and makes practical application to mobile devices more feasible. The use of $\Delta\Sigma$ modulators has been previously explored in RF transmitters in order to take greater advantage of digital scaling trends [15, 29–31]. In this architecture, the LUT is first trained in an open-loop manner as shown in Fig. 4-2. This has he tremendous practical advantage over closed-loop Cartesian feedback training that the training symbol rate is not limited by stability

requirements of the closed-loop Cartesian feedback system [12]. Next, the trained LUT is placed in the *feedback path* of the predistorting $\Delta\Sigma$ modulator. The effect is that the closed-loop transfer function of the $\Delta\Sigma$ modulator becomes the inverse nonlinearity of the PA, and interpolation between LUT entries happens naturally as a result of oversampling and subsequent low-pass filtering. Moreover, because the dynamics of the $\Delta\Sigma$ modulator loop are simple in the first-order loop, introducing nonlinearity here is not problematic from a stability standpoint. Overall, the system inversion and LUT interpolation is achieved in a way that is absolutely simple and direct. This attribute is particularly important for handset applications where system complexity adds to cost. Also, because during the training the nonlinearity of the coarse DACs is incorporated into the LUT, the accuracy and therefore the power requirements on these DACs is greatly reduced.

4.2 Principles of the Predistorting $\Delta\Sigma$ Modulator

This architecture uses a Cartesian representation of symbols and consists of a $\Delta\Sigma$ modulated predistorting block, followed by four-bit DACs, analog filters to remove the out of band quantization noise, the upconversion mixer, and a 1-2Watt PA. The downconversion mixer and the attenuator are needed for the LUT training stage. This section describes the LUT training procedure as well as the predistortion operation of the $\Delta\Sigma$ modulator.

4.2.1 Look-Up Table Training

The LUT training process is shown in Fig. 4-2. This training procedure is repeated as often as necessary in order to adapt to changing conditions. First, an RF switch connects the PA output to a 50Ω load to prevent the transmission of training signals. Then, the upconverted training signal directly feeds into the PA, and the output is sampled after the downconversion to capture the compressive nonlinearity characteristic of the PA. The RF switch connects back to the antenna for data transmission after the training completes. Phase alignment is necessary in this system, as phase misalignment will degrade stability margins in the predistorted $\Delta\Sigma$ modulator in much the same way that it will affect a closed-loop Cartesian feedback system [11, 32]. An important advantage to using first-order $\Delta\Sigma$

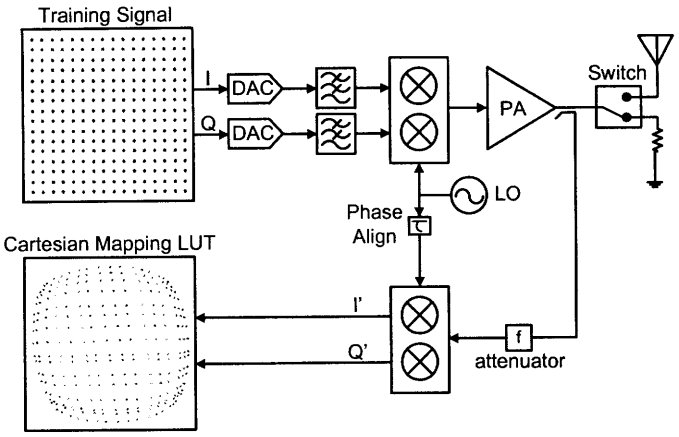

Figure 4-2: The LUT training procedure.

modulators is that its sensitivity to phase misalignment is reduced so as to only be a serious concern if the phase misalignment approaches 90 degrees.

Previously explored LUT training procedures use feedback and an adaptive algorithm to capture the inverse nonlinearity of the PA [13, 14]. This adds complexity to the transmitter system and also suffers from convergence and bandwidth issues. This LUT training, however, only needs to sample the attenuated PA output, which leads to a more straightforward and much faster training with minimum computational overhead. As can be seen from Fig. 4-2, the training symbols are simply all of the available digital address codes for the LUT. For this prototype, this implies a total LUT size of 256 entries. This training procedure is then repeated as often as necessary in order to ensure adaptation to changing conditions.

It is worth noting that this training method results in corrective predistortion only for memoryless nonlinearity. While this would be a serious shortcoming for base station and other high power PAs, memoryless predistortion has been shown to provide substantial improvement at the lower output powers typical of handsets [33].

4.2.2 $\Delta\Sigma$ Modulator

The $\Delta\Sigma$ modulator predistorts the data by using the LUT in the feedback path. The number of quantizer bits is set by the size of the LUT. The 4-bit quantizer allows the use of a 16×16

size LUT. Although a low-order $\Delta\Sigma$ modulator is used in this architecture, a higher order can be considered to further relax the oversampling ratio. Choosing the appropriate order **k**, oversampling ratio **m**, and quantization of **b** bits for the $\Delta\Sigma$ modulator can be decided by using the following equation

$$DR = 3(2k+1)m^{(2k+1)}\frac{(2^b-1)^2}{2\pi^{2k}} \tag{4.1}$$

from [34].

The predistorting $\Delta\Sigma$ modulator block continues to benefit both in terms of speed and power as CMOS technology continues to scale. For example, a pipelined $\Delta\Sigma$ modulator operating at 5.4GHz was validated in [29]. Also, a digital $\Delta\Sigma$ modulator with a multi-bit quantizer in CMOS 90nm for a wireless transmitter presented in [35] shows a sub-mW power consumption running at 468MHz for 7-bit signed data. For the DACs, a 6-bit full Nyquist 3GS/s DAC has been presented that only consumes 29mW [36]. It can be concluded that the fast DACs needed for the oversampled $\Delta\Sigma$ modulator do not add significant power overhead. This is much less burden than the usual DAC performance required in conventional DPs since 12-bit or higher resolution DACs with very high speed are needed in those systems.

Chapter 5

Prototype Design & Validation

A discrete prototype transmitter centered at 900MHz and consisting of an upconversion mixer, phase shifter, attenuator, and downconversion mixer, and a class-A PA (Mini Circuits ZHL-0812-HLN) was formally built by Sungwon Chung. The RF front-end was modeled using Agilent Advanced Design System (ADS) to find the required specifications for each circuit block, which satisfies 41.7dB cascaded gain, 36.0dB output referred third-order intercept point (OIP3), 10dB noise figure, -74dBc noise floor to a sinusoid signal, and 25.0dB output power dynamic range. At the highest output power of 28.7dBm, we allocated 7.27dB margin in the OIP3. The PCB was originally designed to demonstrate WiMAX predistortion and therefore was aimed to meet the WiMAX TX spectral requirement of -25dBr at 2.725MHz offset, -32dBr at 4.875MHz offset, and -50dBr noise floor from 7.375-MHz offset. After investigating permissible nonlinearities in each circuit block while ensuring that the communication standard requirements were met, chips were purchased accordingly that meet all the requirements set in the behavioral model. The PCB was designed using Cadence Allegro with schematics in Capture HDL and layout in PCB Editor and a simple change in jumper location allows easy hardware reconfiguration into either an open-loop transmitter or a closed-loop two-point transmitter.

The LUT was initially implemented in Xilinx Virtex-II PRO FPGA and compiled in FPGA Compiler II. Virtex-II PRO features integrated IBM Power PC processor cores, giving maximum architectural flexibility. Unfortunately, the standard I/O interface did not support the needed bandwidth. Rather than using LVDS I/O interface, instead, the LUT

training signals were captured in the Agilent digital signal analyzer DSA80000B and the predistortion path was implemented in MATLAB. The resulting predistorted signal was loaded into a Tektronix 14-bit AFG3102 arbitrary waveform generator using GPIB programming in 'C' with one PC controlling the measurement setup. The measurement setup is shown in Fig. 5-1 and the implemented PCB Cartesian feedback in shown in Fig. 5-2. Spectrum measurements were taken with Agilent N9020A MXA Signal Analyzer with PA output power of 27dBm.

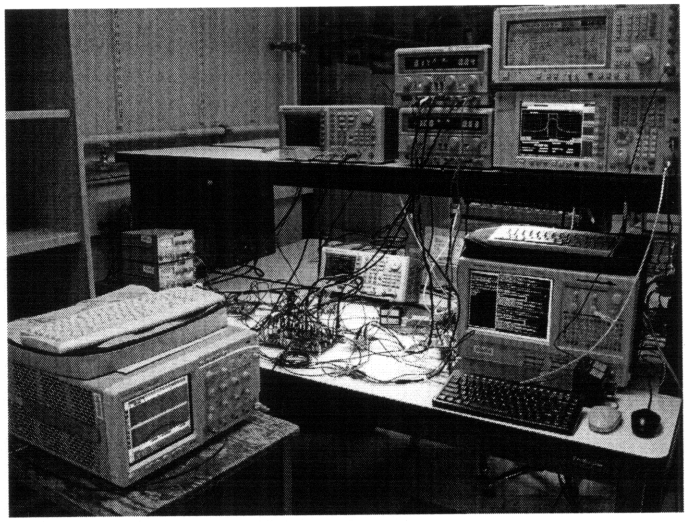

Figure 5-1: Test setup

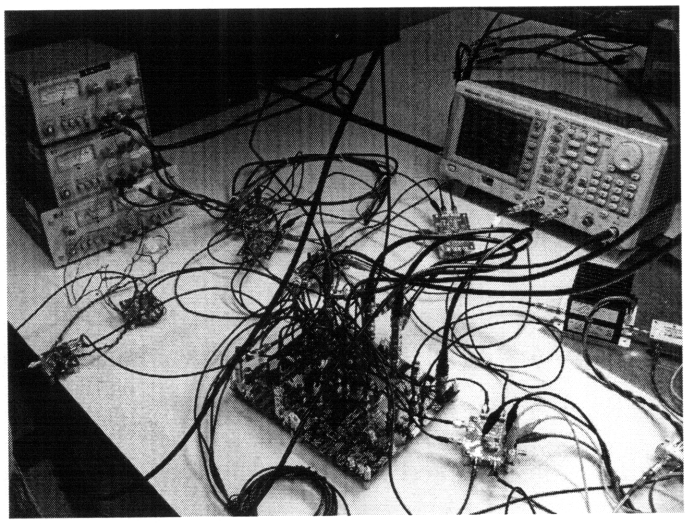

Figure 5-2: PCB of the CFB.

5.1 Two-Point Linearization

5.1.1 Implementation

The two-point architecture demonstration was aimed for signals up to 200KHz, or 100KHz in baseband. This requires f_{unity} to be above 100KHz. The feedback loop was characterized by f_{3dB} = 14kHz, f_{unity} = 250kHz, 38dB feedback attenuation, and 39dB loop gain.

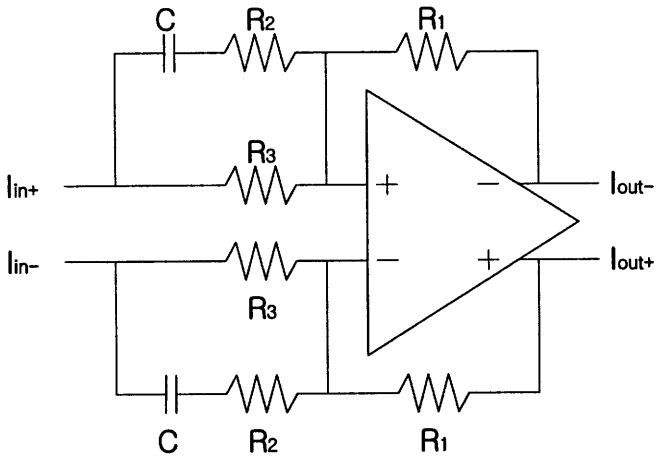

Figure 5-3: Lead compensator.

Lead compensator was implemented as shown in shown in Fig. 5-3 for better phase margin. This transfer function for this circuit is

$$\frac{I_{out+} - I_{out-}}{I_{in+} - I_{in-}}(s) = -\frac{R_1}{R_3}\frac{(R_2 + R_3)Cs + 1}{R_2Cs + 1}. \tag{5.1}$$

The lead zero was placed near the f_{unity} to incease the phase margin by approximately 45 degrees.

Look-Up Table Training

First, the PA output was connected to a 50Ω load instead of the antenna using an RF switch to prevent the transmission of training signals. Then the clock signals for the AD8349 upconversion mixer and the LT5516 downconversion mixer was phase aligned. Phase align-

ment is necessary in this system, as phase misalignment of higher than 90 degrees results in instability [11, 12].

For phase alignment calibration, the clock signal source, a Rhodes&Schwarz SMIQ vector signal generator, was phase shifted using ATM P1213DRE before feeding it into the downconversion mixer. An upconverted sinusoidal input at 1MHz for I channel and a DC signal for the Q channel were fed into the PA. The downconversion mixer clock was phase shifted until the downconverted I channel showed maximum sinusoidal amplitude and Q channel showed a clean DC signal. This was accurate to within $1^o \sim 2^o$ as the I and Q channel coupling in the mixer could not be fixed.

After phase aligning, 1732 LUT training symbols that span the full PA input range were transmitted at 10KSymbol/s. The attenuated PA output was sampled by an Agilent digital signal analyzer DSA80000B after downconversion. 50 samples for each of the 16×16 LUT entries were averaged to reduce the noise floor [12]. Finally, the RF switch was connected back to the antenna for data transmission upon completion of the LUT training.

Combining Cartesian feedback and DPD

The feedforward predistortion path and the Cartesian feedback inputs were synchronized. The clock source from the waveform generator for the Cartesian feedback was used as the reference clock source for all measurement setups. The waveform generator with the loaded predistortion signal was triggered to the Cartesian feedback waveform generator in master-slave fashion.

The summing junction is shown in Fig. 5-4. The opamp outputs $I_{DPD} + I_{in+} - I_{in-}$. Each of the three inputs can be scaled by controlling the values of the input resistors and the feedback resistors. Identical resistance values were used for unity gain in the implementation.

5.1.2 Measurement Results

Cartesian feedback, DPD, and two-point were tested at 26.6dBm output power with 16-QAM input signal with lower than f_{3dB}, higher than f_{3dB} and lower than f_{unity}, and higher

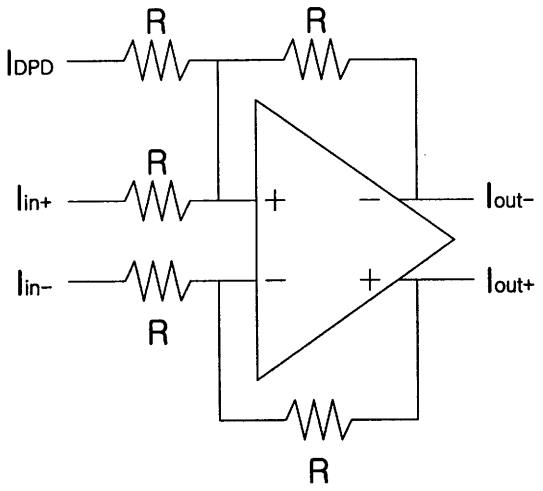

Figure 5-4: Summing junction.

than f_{unity} to give a comprehensive demonstration across various frequency ranges.

Linearization Performance

Fig. 5-5 gives the PA output spectrum at four different frequencies: 20kHz, 160kHz, 320kHz, and 400kHz. In Fig. 5-5(a), two-point linearization and CFB both perform much better compared to DPD. This follows our expectation since the input signal has low bandwidth and therefore it is well within the linearization range of CFB. In Fig. 5-5(b), CFB performs worse than DPD. However, the two-point linearization still gives high linearity. This is also noticeable in Fig. 5-5(c) and Fig. 5-5(d) since the estimated DPD and two-point linearization convergence frequency is 500kHz; DPD takes over the linearization role at baseband frequency of $f_{unity} = 250$kHz, which is 500kHz wide when upconverted.

The resulting sideband suppression is given in Fig. 5-6. A resolution bandwidth of between 1 and 10% of the channel bandwidth was used with frequency offset at half the bandwidth from the carrier. At low frequencies the CFB and two-point linearization give similar sideband suppression. With increasing frequencies, the CFB performance worsens due to loss in loop gain as expected. Although the performance of the two-point linearization worsens with increasing frequencies, the rate of degradation is much slower since DPD starts assisting the linearization. DPD takes over the linearization role at 600kHz, which is

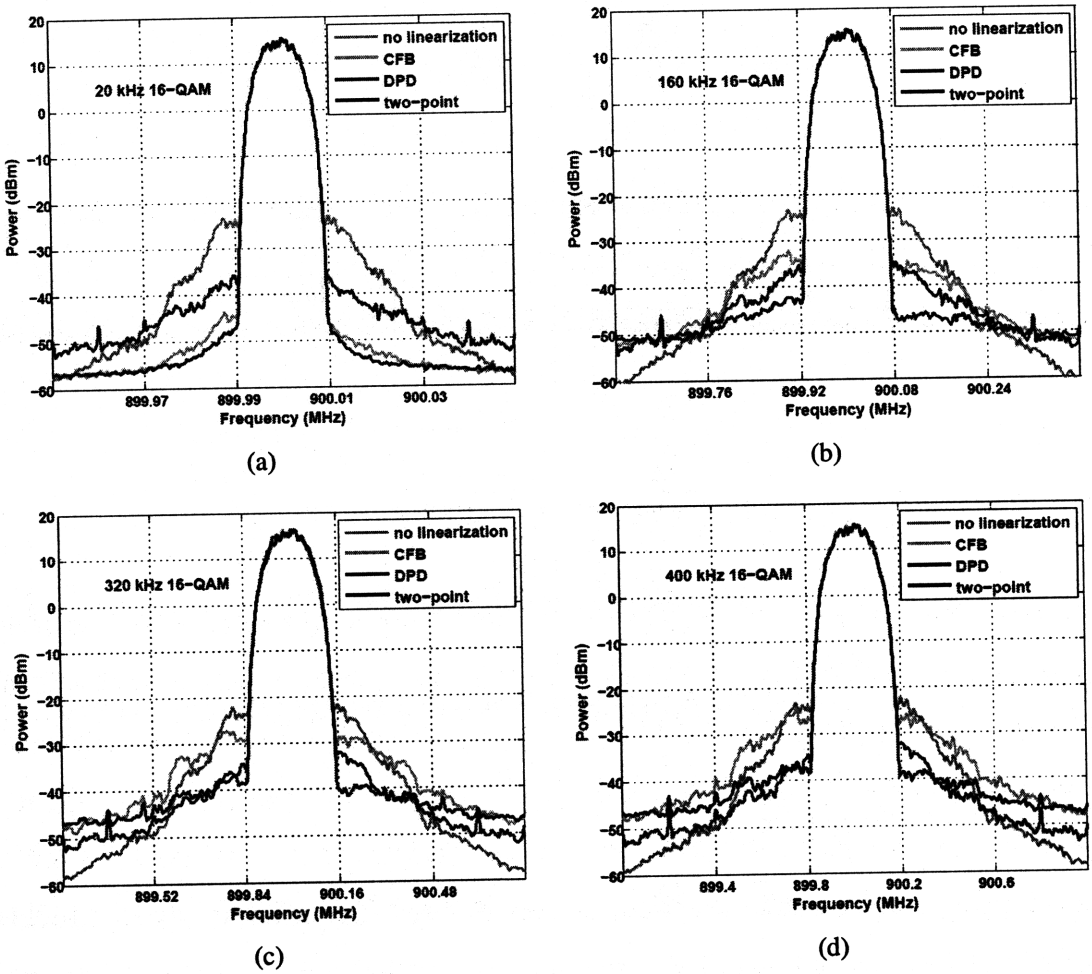

Figure 5-5: The measured linearization spectrum for system with f_{3dB} = 14kHz and f_{unity} = 250kHz with 16-QAM input bandwidths of (a) 20kHz, (b) 160kHz, (c) 320kHz, and (d) 400kHz.

close to the expected 500kHz.

Error vector magnitude (EVM) is also of interest in PA linearization. Fig. 5-12 shows that the EVM for the two-point linearization is just as good as that of DPD across the tested frequency range.

5.1.3 Choosing the Input Bandwidth

Fig. 5-6 shows linearization performance versus input bandwidth. CFB performs worse than DPD for input bandwidths higher than 100kHz. Two-point linearization, on the other hand, can be used for input bandwidths up to 600kHz and still exhibit superior linearity to

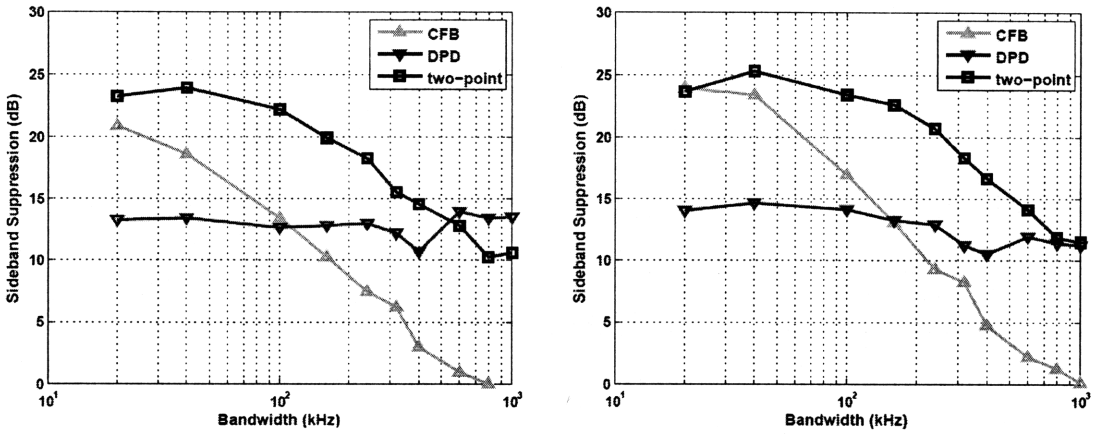

Figure 5-6: The measured sideband distortion suppression for system with $f_{3dB} = 14\text{kHz}$ and $f_{unity} = 250\text{kHz}$ at various baseband bandwidths: (a) left sideband (b) right sideband.

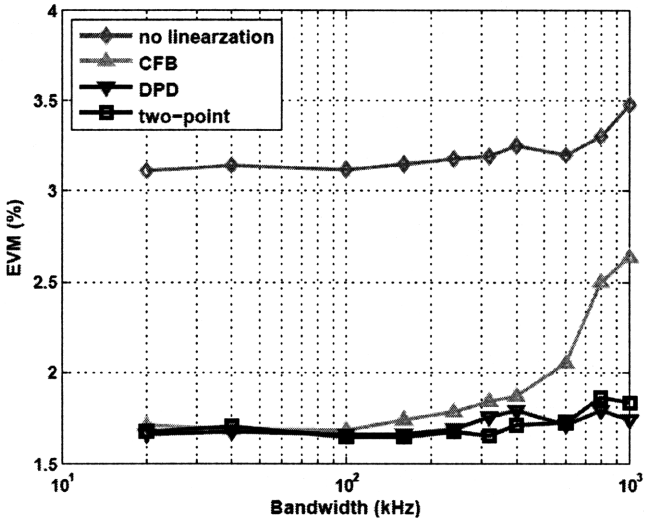

Figure 5-7: The measured EVM for system with $f_{3dB} = 14\text{kHz}$ and $f_{unity} = 250\text{kHz}$ at various baseband bandwidths.

DPD. For higher input bandwidths, the two-point architecture does not retain a performance advantage over DPD.

If seeking to quantitatively evaluate two-point linearization as a bandwidth enhancement for CFB, quantitative performance objectives must first be agreed upon. If, for example, the goal is to achieve 5dB lower distortion products than is possible with static predistortion, then CFB can only deliver this performance for bandwidths up to 70kHz.

Two-point linearization, however, meets this criterion for bandwidths up to 500kHz, and improvement of over 7x. The two-point architecture achieves this with few changes to existing CFB architectures, and effects memory effect suppression without an enormous boost in computation complexity.

5.2 Predistorting $\Delta\Sigma$ Modulator

5.2.1 Implementation

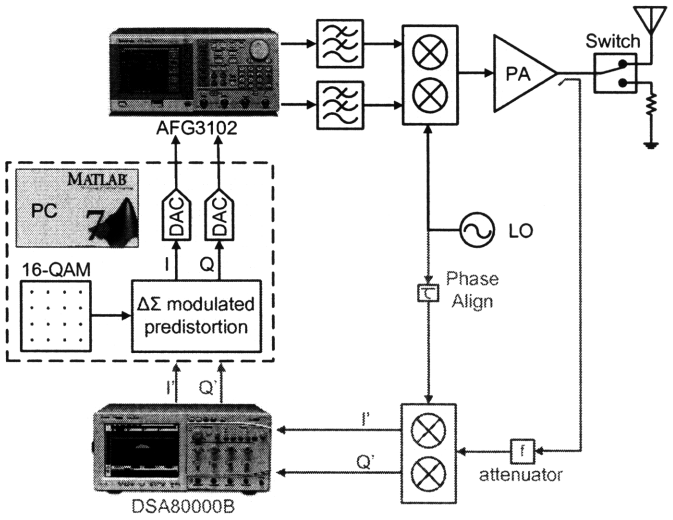

Figure 5-8: The predistortion block was implemented in MATLAB and loaded into a Tektronix waveform generator. The discrete prototype consists of an upconversion mixer, PA, phase shifter, attenuator, and downconversion mixer. The gray signal path is made active during training stage.

The measurement setup is shown in Fig. 5-8. The gray signal path is active only during the training stage. The $\Delta\Sigma$ modulated predistortion block and the DACs were implemented in MATLAB.

16-QAM Signal Generation

First, a 16-QAM signal was generated by pulse shaping using a squared root raised cosine filter (SRRCF) with an upsampling ratio of four and a rolloff ratio of 0.5. The pulse-shaped output was further interpolated to suppress replicas of the signal spectrum occurring

between the baseband and the $\Delta\Sigma$ modulator oversampling frequency. Two hardware-efficient filter structures were considered: half-band FIR and cascaded integrator comb (CIC) filter.

Half-band filters are widely used in multirate signal processing when interpolating or decimating by a factor of two. All of the odd coefficients are zero except for the center one, and all even coefficients are symmetric about the filter center point. Therefore, half-band filter with the length of 2N+1 only requires $\frac{N}{2}$ multiplications per output stage. Since, half-band filter can only have a sample rate change of a factor of two, several of them must be serially connected to realize higher interpolation ratio.

CIC filter, on the other hand, does not require any multiplier or storage for filter coefficients and can accommodate a wide range of rate change factors. Unfortunately, CIC interpolating filter rapidly attenuates frequencies outside a narrow lowpass region and therefore requires a precompensation filter to compensate for the inband attenuation.

Normally, the pulse-shaped signal is interpolated using cascaded half-band filters to raise the sampling rate and then interpolated again using CIC filters to reduce the precompensation filter requirement. Just enough interpolation is needed until spectral replicas get buried in the shaped quantization noise of the following $\Delta\Sigma$ modulator. Three cascaded half-band filters provided sufficient interpolation. The SRRCF uses 41 multipliers, 37 adders with 12-bit coefficient words, and each half-band filters use 10 multipliers and 9 adders with 12-bit coefficient words.

Look-Up Table Training

First, the PA output was connected to a 50Ω load instead of the antenna using an RF switch to prevent the transmission of training signals. Then the clock signals for the AD8349 upconversion mixer and the LT5516 downconversion mixer was phase aligned. Phase alignment is necessary in this system, as phase misalignment of higher than 90 degrees results in instability in the predistorted $\Delta\Sigma$ modulator in much the same way that it will affect a closed-loop Cartesian feedback system [11, 12].

For phase alignment calibration, the clock signal source, a Rhodes&Schwarz SMIQ vector signal generator, was phase shifted using ATM P1213DRE before feeding it into the

downconversion mixer. An upconverted sinusoidal input at 1MHz for I channel and a DC signal for the Q channel were fed into the PA. The downconversion mixer clock was phase shifted until the downconverted I channel showed maximum sinusoidal amplitude and Q channel showed a clean DC signal. This was accurate to within $1^o \sim 2^o$ as the I and Q channel coupling in the mixer could not be fixed.

After phase aligning, a 16×16 constellation LUT training symbols was transmitted at 100KSymbol/s that span the full PA input range. The attenuated PA output was sampled by an Agilent digital signal analyzer DSA80000B after downconversion. 32 samples for each of the 12-bit 16×16 LUT entries were averaged to reduce the noise floor [12]. Finally, the RF switch was connected back to the antenna for data transmission upon completion of the LUT training.

$\Delta\Sigma$ Modulator Specifications

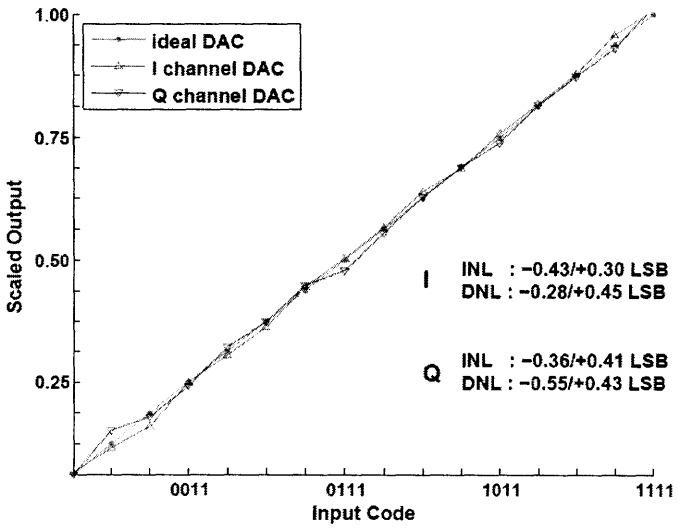

Figure 5-9: The I channel DAC has INL of -.43/+.30 LSB, DNL of -.28/+.45 LSB and the Q channel DAC has INL of -.36/+.41 LSB, DNL of -.55/+.43 LSB

The predistorted signal is $5\times$ wider than the original signal since it carries the inverse nonlinearity of the PA which involve 3rd and 5th order terms. Enough oversampling is needed to ensure that the shaped quantization noise does not mask this predistorted signal. The $\Delta\Sigma$ modulator uses an oversampling ratio of $128\times$ and a 4-bit quantizer. LUT size is

16×16 and each entry has 12-bit resolution. The LUT is bypassed in the $\Delta\Sigma$ modulator when generating signals without predistortion. For the I and Q channel DACs, Gaussian distributed mismatch commensurate with 4-bit performance was added as shown in Fig. 5-9.

5.2.2 Measurement Results

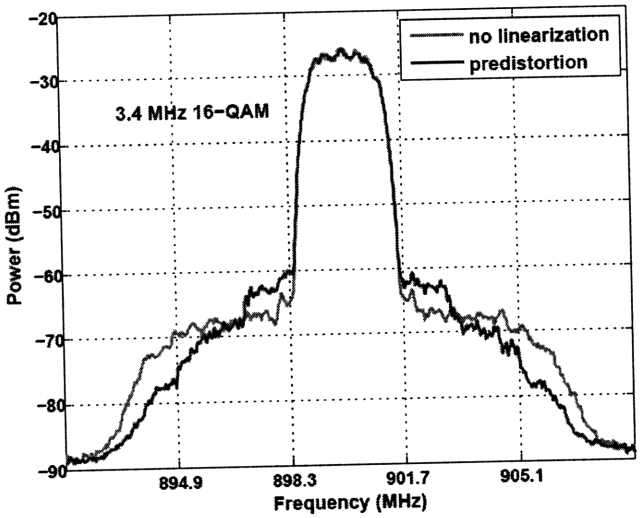

Figure 5-10: The measured specturm of the upconversion mixer output

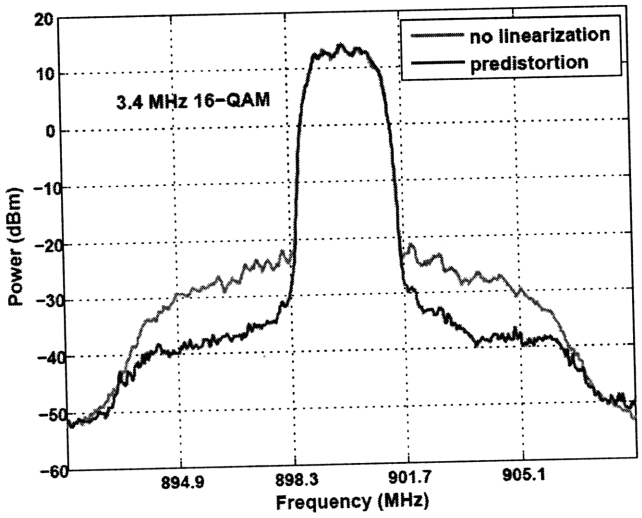

Figure 5-11: The measured output spectrum of the linearized power amplifier with predistortion and without predistortion for 3.4MHz 16-QAM signal.

Fig. 5-10 shows the upconversion mixer output for the signal with predistortion and without predistortion. It can be seen that the predistortion has the effect of actually broadening the spectrum before it passes through the nonlinearity of the PA.

Fig. 5-11 shows the comparison between the unlinearized overall transmitter and the linearized transmitter. We observe approximately a 10dB reduction in distortion products at a total PA output of 26.7dBm. In addition, the measured EVM performance improved from 3.45% to 2.02% as shown in Fig. 5-12. Fig. 5-13 shows the predistorted signal at wider

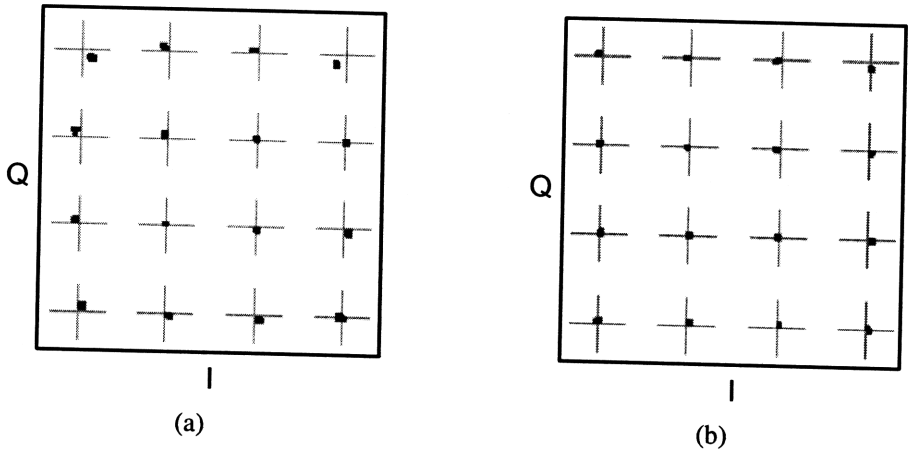

Figure 5-12: The measured EVM shows (a) 3.45% when not linearized and (b) 2.02% after predistortion.

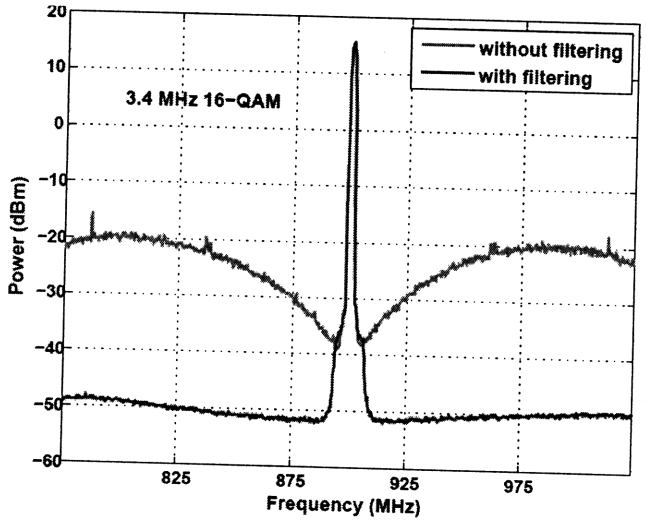

Figure 5-13: A broader band (250MHz) measured spectrum of the linearized power amplifier output with filtering and without filtering.

spectral span. Filtering the $\Delta\Sigma$ modulator output using Mini-Circuit SLP-5 suppresses out-of-band quantization noise. The unfiltered spectrum, however, have quantization noise initially rising by 20dB/dec. The drop in quantization noise starting at 100MHz from the carrier is caused by the AD8349 upconversion mixer's limited modulation bandwidth.

5.3 A Two-Point PA Linearization System Using A Predistorting $\Delta\Sigma$ Modulator

5.3.1 Implementation

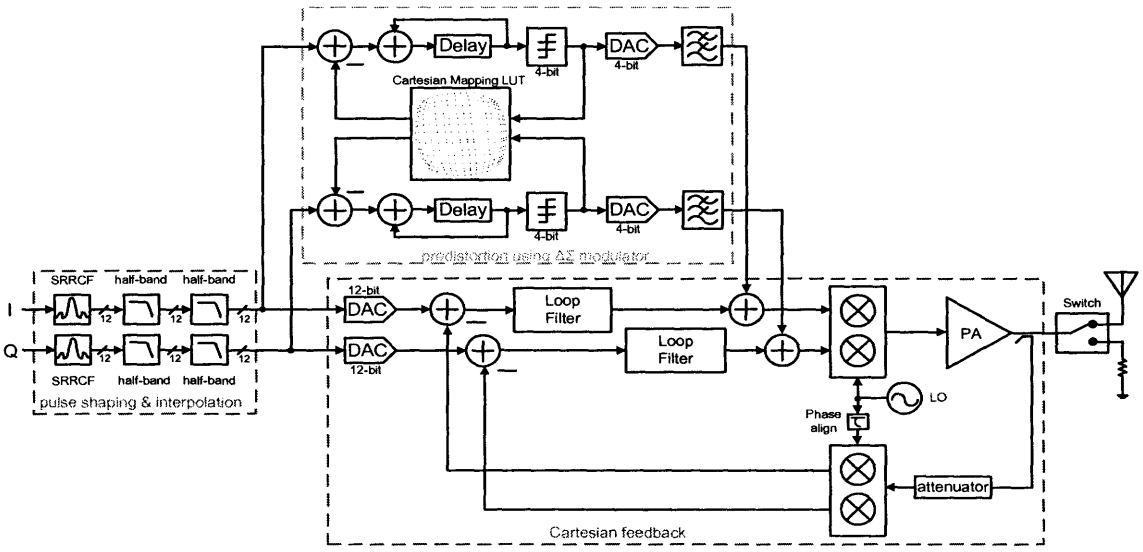

Figure 5-14: A two-point linearization system using a predistorting $\Delta\Sigma$ modulator.

The two-point linearization and predistortiong $\Delta\Sigma$ modulator can be combined as shown in Fig. 5-14. This brings together to benefit of memory effects compensation of two-point linearization and the fast and simple open-loop training of the predistortiong $\Delta\Sigma$ modulator. The design flow of this system is shown in Fig. 5-15.

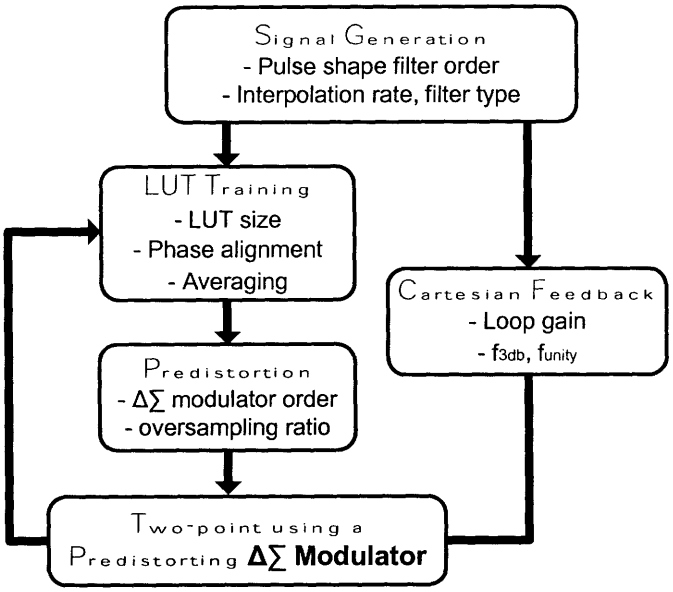

Figure 5-15: The design flow of the two-point system using a predistorting $\Delta\Sigma$ modulator.

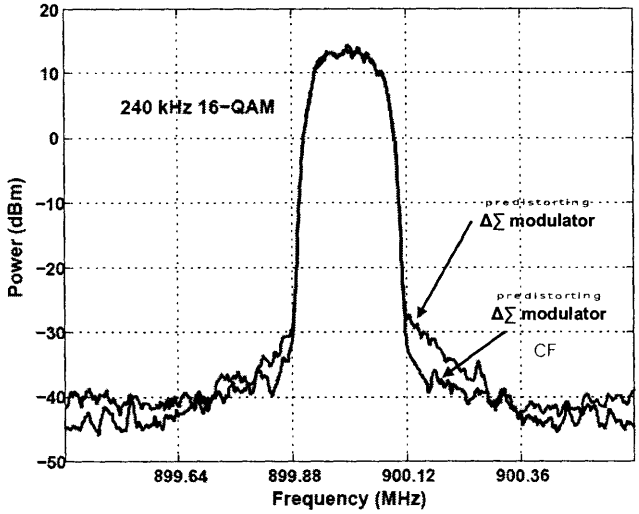

Figure 5-16: Linearization performance of the system compared to predistortion using $\Delta\Sigma$ modulator alone.

5.3.2 Measurement Results

The final system was tested with a 240kHz-wide 16-QAM signal. The linearization performance of the system compared to predistortion using $\Delta\Sigma$ modulator only is shown in Fig. 5-16. Maximum of 5dB better sideband suppression is obtained. This is slightly less than what was measured using the two-point system with conventional predistortion in Fig. 3-1.

This is due to the added nonlinearity of the waveform generator coming from the $128\times$ oversampling ratio of the $\Delta\Sigma$ modulator. We measured 1.41%rms error vector magnitude (EVM) with 1000 symbol points.

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