Micro-Fabrication of 3-D Si/Air and Si/SiO₂/Air PBG Structures

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Abstract

Photonic Band Gap structures (PBGs), or Photonic Crystals, are a novel class of composite materials that present a range of frequencies within which photons can not propagate. In analogy to bandgaps in semiconductors, defects can be introduced and their energy levels are within the optical bandgaps. These features of PBGs provide numerous exciting opportunities for solid state theories as well as new and improved device performance spanning the electromagnetic spectrum from microwave to optical region.

This thesis represents an initial effort at fabricating operational 3-D PBG structures. We focus on the fabrication of the first two layers of a class of 3-D photonic band gap structures at midgap wavelength of 1.53mm, using two material systems Si/air and Si/ SiO₂/air. In the process of building these structures, various fabrication issues were addressed, with special emphasis on planarization, deep submicron pattern transfer and alignment between successive layers.

Two approaches were investigated for the fabrication. The first one features an electron-beam lithography system that is capable of high resolution and fine alignment. The fabrication started with e-beam evaporation of amorphous silicon onto the substrate. The image-reversed pattern was created in the PMMA with electron beam lithography. Then a thick layer of Ni-Cr was evaporated with e-beam, and after lift-off, became the hard mask for reactive ion etching. Special recipes were used to get straight side wall trenches in amorphous silicon. Finally, to finish the first layer, silicon dioxide was deposited with biased high density PECVD tools to conformally fill in the trenches. The wafer was then locally planarized with a combination of physical sputtering and time-controlled wet etch. We also demonstrated the capability of electron beam lithography system at aligning the structures within ±45 nm. These processes are repeatable and with further process control, can lead to the construction of operational 3-D PBG structures. The drawbacks of this approach are long cycle time and low yield.

In the second approach, the first two layers of the 3-D PBG structures were fabricated with a process that is compatible with the existing Integrated Circuits fabrication techniques. Due to the lithography limitations, the center of the bandgap was scaled up to 4.5
μm. Thin layers of polysilicon, silicon nitride, and oxide were sequentially deposited with LPCVD. Poly silicon trenches were then created with Cl₂ based plasma etching, using oxide as a hard mask. The trenches were then filled with BPSG and low temperature oxide, and the wafer was subsequently polished with CMP. With the same procedure, the second layer was built and aligned to the first layer with contact aligner. The alignment was enhanced with specially designed Moire marks and satisfactory alignment between two layers was obtained.

We have also conceived other options for the fabrication of 3-D structures and in the third part of the thesis, some other options are discussed, especially wafer bonding and membrane bonding processes.

Future effort will be concentrated on fabricating operational 3-D PBG structures with defect states incorporated, using e-beam lithography, and this will lead to the author’s Ph.D. thesis.

Thesis Supervisor: Henry I. Smith
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Chapter 1

Introduction

1.1 What are Photonic Bandgap Structures (PBG)?

Photonic Band Gap structures (PBG) [1][2], are a novel class of composite materials that present a range of frequencies within which photons can not propagate. PBG structures are characterized with a periodicity in dielectric constant, just like the periodicity of the potential in crystals, and for that reason, the PBG structures are also called Photonic Crystals. Due to the Bragg scattering of photons at the dielectric interface, photons with certain frequency will be attenuated rapidly and can not propagate in the structure. This forbidden frequency range forms a photonic bandgap (PBG), which is also analogous to an electronic bandgap in a semiconductor crystal.

It should be noted that the building blocks of PBG structures are transparent; and the attenuation of the light is due to the diffraction in the periodic medium, not absorption. Mathematically, the dielectric constants of the media, $\varepsilon(r)$, are purely real numbers.

PBGs are expected to be useful in making high-Q microcavities for single-mode light-emitting diodes and low threshold integrated lasers [3][4]. In the long run, the PBG structures provide an exciting opportunity for photonic information technology. However, the complexity of fabricating the structures has limited the practical applications; most of the implementations have been limited in the one and two dimensions.

1.2 Motivations: Photonic Information Technologies

The research and applications of semiconductors have been continuously fueling the
expanding microelectronic industry that has changed our daily life in almost every aspect. Currently the trends towards smaller devices and higher performance are ever accelerating. Unfortunately, the simple scaling-down results in significant higher power dissipation, more complex processing for interconnects, poor reliability and the devices are having greater sensitivity to signal synchronization [5]. Many scientists are now turning to light instead of electrons as the information carrier. The analogy of the semiconductors in optical domain, the Photonic Bandgap Structures (PBGs) or Photonic Crystals, are expected to play the similar major role in photonic information technology as semiconductors in microelectronics [6].

Using light as information carrier has many advantages over electrons, i.e. much higher speed, high bandwidth, less interaction between carriers, and better reliability. Despite all that, there are serious drawbacks in implementing photonic information technologies. The photons are not as easily controlled as electrons. Light-emitting efficiency is very low and the emission of the light is often omnidirectional. There are no effects that can easily drive photons as electric potential and wires do for electrons. The conventional optical devices like mirrors and lenses are generally bulky.

Photonic Bandgap Structures (PBG), or Photonic Crystals, offer new opportunities for controlling the propagation of photons and miniaturization of photonic devices that can be eventually applicable to all-optical integrated systems or opto-electronic devices.

As in electronics, miniaturization can help to reduce the power consumption and improve the reliability. A good example of miniaturization is the reflecting films in almost all optical lenses and mirrors. Actually those films can be considered one-dimensional PBG structures [7]. The length scales of PBG structures are from one fourth to one half of the wavelengths of photons and offer much higher level of large scale integration.

Conventional optical devices, like optical fibers, rely on the internal reflection, deflection, etc., that require a smooth surface and thus casts significant challenges on the microfabrication. The PBG structures differ from many other optical devices in the way of confining the light propagation. In one dimension, PBG structures become thin layers of alternating dielectrics and can efficiently attenuate the light propagating along the normal
direction in special wavelength regions. In three dimensions the propagation of photons can be better described in analogy with that of electrons in crystals. In a crystal, the atomic lattice presents a three dimensional periodic potential to the electrons propagating within it. And this periodicity leads to attenuation of electrons propagating with certain energies in certain directions, owing to Bragg-like diffractions. In a 3-D dielectric media, this phenomenon also exists and photons with specific wavelength (energy) in some directions can not meet the boundary conditions and therefore can not propagate. This could be easily described with energy bands. For example, a complete bandgap is a range of frequencies within which photons can not propagate in any direction. Band structures could be engineered through proper design of the spatial dielectric function $\varepsilon(r)$.

Another important characteristics of crystals are the impurity states. By introducing some impurities in a specific manner, those impurities have energy levels within the electronic bandgap, therefore changing the electrical properties of the crystal. Semiconductors, having band gaps and impurity levels suited for electronic signals, plays the dominant role in microelectronic circuits. This analogy also holds for PBG structures. A defect state can be introduced in the photonic band gap when the dielectric periodicity of a photonic crystal is broken by the selective removal or addition of dielectric material [8][9]. A point defect results in the spatial localization of the defect mode, yielding a high-Q electromagnetic microcavity for resonators and LEDs. Extended defects could act as waveguides of various shapes, providing high flexibility in guiding photons in PBG structures (“photonic wires”) [10].

These abilities provide a systematic approach in controlling the propagation of electromagnetic waves in materials and open a new and fascinating area for potential applications in optoelectronic devices. For example, a crystal with a complete gap serves as an ideal mirror for lights along all directions, while a partial gap allows light to propagate only along certain directions, and could serve as a substrate for a directional emitter. More specifically, PBGs are expected to be useful in microcavities, low threshold lasers, channel dropping filters, high speed optical switches and extreme high speed interconnections within and between chips. Also it is expected to be helpful in increasing the efficiency of
light-emitting diodes.

1.3 The Challenge: 3-D PBG structures fabrication

The three-dimensional PBG structures offer the best control of photon propagation and least non-ideality of edge effects that are inevitable in one-dimensional and two-dimensional structures. However not all 3-D periodic dielectric structures exhibit the photonic bandgap. The low and high dielectric media must be arranged in a specific manner. The first 3-D PBG structure, called ‘Yablonovite’, was proposed by Yablonovitch [11] in 1991. To date there are several other structures that theoretically exhibit 3-dimensional photonic bandgaps [12][13]. Moreover, a theoretical basis to the analysis of the structures is established where the concepts of reciprocal space, Bloch wave functions, Brillouin zones and dispersion relations become applicable.

Experimentally, while the fabrication of a two-dimensional photonic band gap nanostructure has been reported [14], the fabrication of complete 3-dimensional photonic band gap structures that operate at optical wavelengths is still a major challenge for the PBG applications due to the complicated geometry at sub-micron length scale. The initial effort on fabricating 3-D PBG structure was in microwave region with length scale of centimeters [11]. Since the photonic bandgap is fully scalable with length $r$, this verified the existence of complete 3-D photonic bandgap.

Recently, Feiertag, et al. [15], fabricated the ‘Yablonovite’ structure with silicon-carbon-nitride using deep X-ray lithography. The structure showed a bandgap centered at 125 µm. Another structure proposed by T. Ho, et al. [16], was first fabricated at 600 µm operating wavelength by Ozbay et al. [17]. The process involves a technique of stacking thin micromachined (110) silicon wafers. Then S. Lin et al. fabricated the same structure with a bandgap centered at 10 um using IC compatible processes [18].

To be compatible with the optoelectronics industry and to fully explore the applications of PBG structures, 3-D PBG structures with bandgap centered at 1.53 µm is highly desired. However the sophisticated structures at submicron region do not easily lend themselves to fabrication. State-of-the-art micro-lithography techniques such as electron-beam or X-ray
1.3 THE CHALLENGE: 3-D PBG STRUCTURES FABRICATION

lithography are required to define submicron and non-orthogonal features. Also geometrical errors, alignment error between layers, and material non-ideality all can degrade the bandgap. Practically, band gaps larger than 10% and good attenuation in the bandgap are necessary for PBG applications. This requires careful optimization of processes and the use of materials with large refraction index contrasts. Also, a robust design that can tolerate the fabrication deviations is very important.

C. C. Cheng, et al. fabricated the “Yablonovite” structure with bandgap centered at 1.53 μm on GaAs substrates, however, the attenuation in the bandgap is very weak [19][20]. The process involved electron beam lithography and a 35° angled etch in 3 directions. Nevertheless, the angled etch casts problems on geometrical control over layers. Also the structure suffers from not being able to put defects in, which is critical to fully explore the applications of photonic structures.

This thesis addresses the challenge by focusing on the fabrication of a novel class of 3-D PBG structures proposed by a group led by Professor John D. Joannopoulos at MIT [13]. Among all the 3-D structures, these have the advantage of large complete 3-D bandgaps and are also amenable to planar process technology. Also both point and extended defects can be designed and integrated into the process.

The 3-D PBG structures under investigation are made of two or three materials (Si, SiO₂, and/or air) and consist essentially of a layered structure in which a series of cylindrical air holes are etched at normal incidence through the top surface of the structure. In the structure under fabrication, the photonic band gap is as large as 14% of the midgap frequency using Si, SiO₂ and air; and 23% using Si and air (after the SiO₂ is etched away). The detailed analysis of the structures is given in the next chapter.

This thesis represents the initial effort of fabricating the first two layers of the class of 3-D photonic band gap structures at midgap wavelength of 1.53 μm, using two material systems Si/air and Si/SiO₂/air. In the process of building these structures, various fabrication issues are addressed, with special concentrations on deep submicron lithography: pattern transfer and alignment between layers.

Silicon has been the building block of modern microelectronics and a variety of
technologies have been developed for the fabrication of Si structures at the submicron or even nanometer region. Therefore the Si/SiO₂/Air and Si/Air systems are a good starting point for exploring PBG structures at the submicron regime.

Several difficulties arose during the fabrication of these structures. The fabrication takes advantages of the well-developed VLSI technology. However, the fabrication of Integrated Circuits (IC) usually has different emphasis than that of photonic devices, and the processes optimized for the IC fabrication may not be the suited for making PBG structures. For example, IC etching has tapered side-wall profile for better via filling while straight side walls are desired for trenches in PBG structures. Therefore the processes have to be custom optimized. One of the other major challenges is the lithography, especially the alignment between two subsequent layers. Lithography is usually the driving force and key component of VLSI technology. State-of-the-art optical photolithography in industry can print 0.25 μm lines, with overlayer registration accuracy of 60 nm. However, the rather sophisticated geometry and intricate arrangement of holes and rods in PBGs still cast significant difficulties on delineating the patterns and on geometry control (Critical Dimension) control. As for the alignment, the entire Integrate Circuit (IC) fabrication involves only very few steps that require fine resolution and accurate alignment. This is also because the IC process uses self-alignment and does not require fine alignment of source/drain to gate. In this project, critical alignment is essential for all the layers. Another challenge is the gap filling and planarization processes. The compatibility of equipments prohibits the high temperature process to fill the trenches and the industry standard planarization process CMP does not provide good enough process control for the fine features of PBG structures.

The problems above will be identified and solved in the correspondent chapters. Yet another effort of making the PBG devices using totally IC compatible process was also developed and documented in Chapter 5.

Another difficulty of the fabrication is the exponentially decaying yield. In a research university, the process control is in no way comparable to leading industry manufactures. The long turn-around time and lack of man-power prohibited the massive low-yield fabrication. In another word, each process step has to be well characterized before actual
1.4 OUTLINE OF THE THESIS

fabrication and the fabricated structure has to achieve the designed characteristics in very few iterations.

1.4 Outline of the Thesis

This thesis is composed of two parts. One is for the devices operating at 1.53 μm (i.e. with a bandgap centered at 1.53 μm) and uses special techniques to achieve submicron accuracy. The other is the IC compatible process for higher throughput but lower resolution.

Chapter 2 provides some theoretical backgrounds of the photonic bandgap and the defect states. Also introduces the 3-D structure that is to be fabricated.

Chapter 3 introduces the planar technology and explores the different approaches for the fabrication and explains our implementation strategy.

In Chapter 4 I demonstrated the fabrication of the first two layers of the desired 3-D structure and summarized the procedure for the alignment between layers using electron-beam lithography. The films were deposited using e-beam evaporation and patterned with electron-beam lithography, the trenches were defined with dry plasma etch. Then silicon dioxide was deposited with a high-density plasma deposition tool called PlasmaQuest in TRL. The simultaneous deposition and sputter etching ensured the gap filling and also planarized the oxide. Further planarization was obtained with a sequence of physical sputtering, low power dry etching and slow wet etch. The first layer finished with a controlled etchback of oxide which stops at the top of the silicon veins. The second layer fabrication was the same except the pattern shifted half period. For the successful implementation of e-beam alignment, a supplementary photolithography step is required to open the area where alignment marks lie. Also included in this chapter are process control methods. The PBG structures require sub-micron accuracy and this demands strong process control and calibration. SEM, AFM and ellipsometry are the major characterization techniques.

Chapter 5 covers the fabrication of the first and second layers of the same structure using integrate-circuits (IC) compatible technology in the Microsystems Technology Laboratories (MTL) at MIT. The IC-compatible process has the advantage of high volume
production and availability of various equipments. Due to the limitation of MTL lithogra-
phy systems, the structure is scaled up to have a bandgap centered at around 4.7 µm. One
potential problem is the stress associated with the multi-layer stacking of the poly Si, which
will adversely affect the CMP planarization.

Chapter 6 discusses the future development and other options for fabrication. A
detailed flow for the final fabrication sequence will be presented. Among other options the
bonding of films is a very promising technology and some preliminary work has verified
this.

This thesis work utilizes nearly all the standard IC-fabrication processes, as well as
many non-standard, in-house developed processes. In each process step, the process
equipment and main mechanism will be briefly introduced, and the process parameters
(recipes) provided.
Chapter 2

Backgrounds on PBG theories and 3-D PBG structure design

2.1 Photonic Band Gap (PBG) Theory

A photonic crystal is a 3-D periodic dielectric structure possessing a frequency band or band gap over which all electromagnetic modes, spontaneous emission, and zero point fluctuations are forbidden, irrespective of propagation directions [1].

As an introduction to PBG theory, it is helpful to first review the electronic bandgap. The motions of electrons in a solid can be described by the Schrödinger equation with a set of boundary conditions arising from the periodicity of the potential. The solutions are characterized by a wavevector \( \mathbf{k} \) and a band index \( n \). There are some solutions that have the same energy level and are called \textit{degenerated states}. The density of the solutions within an energy level \( \Delta E \) is called the \textit{density of states}. The region of all allowed wavevectors is called a \textit{Brillouin zone} and the collection of all solutions is termed a \textit{band structure}. The existence of band gaps is most commonly illustrated by the splitting of state energies at Brillouin-zone boundaries.

For electromagnetic-waves, we can consider scatterings with any generalized dielectric and magnetic susceptibilities (dielectrics, metals, etc.), and the solutions are obtained from the four macroscopic Maxwell equations:

\[
\nabla \cdot \mathbf{B} = 0
\]

\[
\nabla \times \mathbf{E} + \frac{1}{c} \frac{\partial \mathbf{B}}{\partial t} = 0
\]
\[ \nabla \cdot \mathbf{D} = 4\pi \rho \]  
(2.3)
\[ \nabla \times \mathbf{H} - \frac{1}{c} \frac{\partial \mathbf{D}}{\partial t} = \frac{4\pi}{c} \mathbf{J} \]  
(2.4)

where \( \mathbf{E} \) and \( \mathbf{H} \) are the macroscopic electric and magnetic fields, respectively, \( \mathbf{D} \) and \( \mathbf{B} \) are the displacement and magnetic induction fields, and \( \rho \) and \( \mathbf{J} \) are the free charges and currents, respectively.

In the absence of external currents and sources, Maxwell's equations can be cast in the following simple Master equation:

\[ \left\{ \nabla \times \frac{1}{\varepsilon(r)} \nabla \times \right\} \mathbf{H}(\mathbf{r}) = \frac{\omega^2}{c^2} \mathbf{H}(\mathbf{r}) \]  
(2.5)

where \( \omega \) is the frequency, \( c \) is the speed of light, and \( \varepsilon(r) \) is the macroscopic dielectric function. The solutions \( \mathbf{H}(\mathbf{r}) \) and \( \omega \) are determined completely by the strength and symmetry properties of \( \varepsilon(r) \).

The photonic bandgap structure refers to a periodic array of dielectric scatterers for which the solution of Maxwell's equations over some frequency range consists of a evanescent propagation vector (wavevector) for all possible directions in space. Two approaches can be used to investigate PBG structures. The first solves Maxwell equations in the frequency domain and the second solves the equations in the time domain. These two methods reveal different information. The frequency-domain method yields the frequency, symmetry, polarization and field distribution of every eigenmode. The time-domain method can be used to determine the coupling efficiency, the scattering, and the quality factor or "Q".

Equation (2.5) indicates that the photonic bandgap is fully scalable with length \( r \) and dielectric constants \( \varepsilon(r) \) [7]. There is no fundamental length scale other than the assumption that the system is macroscopic. Specifically, if the media length is scaled down by a factor of \( s \), the eigenfunctions will scale down by the same factor while the frequency will be multiplied by a factor \( s \). If the dielectric constant \( \varepsilon(r) \) is scaled down by a factor of \( s^2 \), then the harmonic modes will remain the same while the frequency will be scaled up with
a factor of $s$. This feature is in contrast with semiconductors where absolute length scale
dictates the transistor physics due to the inelastic scattering of electrons.

An important impact of PBG structures is the suppression or enhancement of spontane-
ous emission [1]. It is known that the rate of spontaneous radiative decay of an atom scales
with the atom-field coupling and with the density of allowed states at the atomic transition
frequency. By changing either the atom-field coupling or the density of states, the rate of
spontaneous emission can be significantly affected. Since photonic crystals have the ability
of suppressing every mode for a given range of frequencies (in another word, the density
of states in that region is zero), they can be used to control the rate of spontaneous
emission.

### 2.2 Three-dimensional PBG design and basic results

The Design of 3-D PBG structures consists mainly of specifying the dielectric function
$\varepsilon(\mathbf{r})$. A significant simplification is to design composite material systems with distinct
dielectric constants. Geometry and spatial distribution of the component materials are the
main parameters to be specified in a design. Many material systems, i.e. Si/SiO$_2$ and GaAs/
GaAlAs/Air, have large enough contrast in dielectric constants to open a bandgap [7].

Due to the fabrication difficulties discussed in previous chapter, it is very important to
design a structure that is amenable to planar technology and possesses a large, complete
band gap despite inevitable deviations in the micro-fabrication. A novel class of 3-D PBG
structures, designed by Fan et al [13], meet all those criteria and is the target of the
fabrication in this thesis. The structures are composed of two or three materials (Si, SiO$_2$,
and/or air). The complete photonic band gap is as large as 14% of the midgap frequency
using Si, SiO$_2$ and air; and 23% using Si and air (e.g. if SiO$_2$ is etched away).

Figure 2.1 depicts the Si/SiO$_2$/Air structure. It consists essentially of a layered structure
in which a series of cylindrical air holes are etched at normal incidence through the top
surface of the structure. The cylindrical air columns can provide a large index contrast with
the remaining material. This structure appears to be fabricable by conventional planar
technologies.

Since the bandgap can be improved by increasing the dielectric contrast of the components, an improvement can be made on the previous structure by simply etching away the oxide, leaving only a porous Si structure (Fig. 2.1).

Figure 2-1: A 3-D Photonic Band Gap (PBG) structure. It's a layered structure made of Si (black) and SiO2 (light gray) in which a series of air columns are drilled through it (after [13]).

Figure 2-2: The same structure as Figure 2.1 except that all of the SiO2 is etched away. The entire structure is composed only of Si (after [13]).
The parameters of this structure are defined in Fig. 2.3, where \( w \) and \( d \) are the width and depth of the SiO\(_2\) - filled grooves (or Si trenches), respectively. The period \( a \) is chosen to be the unit length scale and every other parameter is defined with respect to it. The size of the structure can be scaled to any wavelength simply by scaling \( a \), provided that the dielectric constants of the components are kept the same. For example, in the case where the gap is centered at 1.53\( \mu \)m (this wavelength is used in optical telecommunications today), \( a \) is equal to 0.79\( \mu \)m. At \( \lambda = 1.53 \mu \text{m} \), the dielectric constant is 12.096 for Si and is 2.084 for SiO\(_2\).

\[ \text{Cross-sectional view of the Si/SiO}_2/\text{Air structure} \]

Device fully scalable: \( w = 0.36a \), \( d = 0.51a \), \( h = 0.35a \)

For device operating at 1.5 \( \mu \text{m} \),
\[ a = 790 \text{ nm}, \quad w = 284 \text{ nm} \]
\[ d = 403 \text{ nm}, \quad h = 276 \text{ nm} \]

Figure 2-3: Definition of the parameters describing the PBG structure

We can achieve the maximum band gap by optimizing the parameters. In the Si/SiO\(_2\)/
air structure (Figure 2.1), a gap as large as 14% of the midgap frequency can be achieved with \( w = 0.40a, d = 0.49a, r = 0.21a, b = 0.71a \) and \( h = 0.35a \). Here \( r \) is the radius of the holes shown in the top surface of Figure 2.1 and \( b \) is the distance between them. In the above example where the gap is centered at 1.53\( \mu \)m \( (f = 196\text{THz}) \), the gap extends from \( \lambda = 1.43\mu \text{m} \) to \( \lambda = 1.64\mu \text{m} \) \( (f = 182\text{THz} \text{ to } f = 210\text{THz}) \).

(a)

![Graph (a)](image)

(b)

![Graph (b)](image)

Figure 2-4: Energy band diagrams of the PBG structures: (a) corresponds to Figure 2.1 (Si/SiO\(_2\)/air structure); (b) corresponds to Figure 2.2 (Si/air structure) (after [13])
2.3 Photon Localization at Defects

In the Si/air structure (Figure 2.2), after all of the oxide is removed, the gap can be further increased by re-optimizing the parameters. With $w = 0.36a$, $d = 0.51a$, $r = 0.24a$, $b = 0.71a$ and $h = 0.35a$, a gap of 23% can be obtained!

The corresponding band diagrams are shown in Figure 2.4. For simplicity, the bands are plotted along various directions of the irreducible Brillouin zone of a simple orthorhombic lattice.

How fabrication-related disorder affects the size of the photonic band gaps can be investigated theoretically [21]. We can choose to study the following deviations from a perfect photonic crystals which may arise during fabrication: variations of layer thickness ($h$), variation of trench depth ($d$), misalignment of the trenches between layers, overall surface roughness, etc. It is shown that the size of the gap is tolerant to significant amounts of deviation from the perfect structure as long as the connectivity of the high dielectric medium in consequent layers is preserved.

2.3 Photon Localization at defects

The introduction of a defect in a perfect PBG crystal can lead to the creation of sharp resonant electromagnetic states in the vicinity of the defect. The properties of these modes can be controlled simply by changing the nature and the size of the defect. A defect can be created by adding extra dielectric material into the structure, or by breaking a rib to remove some dielectric material from the structure. We might call the first a “dielectric defect”, and the second an “air defect”. Either of these defects could be implemented during fabrication (for two examples of air defects, see chapter 4). In the case of removing dielectric material (an “air defect”), the cavity mode evolves from the “dielectric band” (the lower propagation band for photons) and can be swept across the gap by adjusting the amount of dielectric material removed. If the defect involves the addition of extra dielectric material (a “dielectric-defect”), then the cavity mode drops from the “air band” (the upper propagation band for photons). In both cases, the defect state can be tuned to lie anywhere in the gap. This flexibility in tuning the position of the defects makes photonic crystals a very
attractive medium for the design of novel types of filters, couplers, laser microcavities, etc.

Why does a defect localize electromagnetic modes? Actually, the defect is like a cavity with perfectly reflecting walls. If light with a frequency within the band gap somehow winds up near the defect, it cannot leave, because the crystal does not allow extended states at that frequency. So, if the defect allows a mode to be excited with a frequency within the band gap, that mode is forever trapped.

If the size of the defect is properly chosen, a localized state can appear in the gap. An example of such a state is shown in Fig. 2.5. The cross-section of the energy density is shown in the case where a rib is broken in the crystal. The state has a torus shape and is localized in all three dimensions. Its frequency, symmetry and field distribution can be changed by varying the size and the nature of the defect. In this case, the defect involves removing material (a single dielectric rib is broken at the center of the crystal), hence the resonance initially appears at the bottom of the gap, and moves up as the size of the defect is increased.

![Image](image.png)

Figure 2-5: Cross section of the energy density of a defect state in the crystal shown in Fig. 2-2. The defect is made by breaking one of the dielectric ribs. The overlay indicates the edges of the crystal (after [22]).
Chapter 3
Approaches and Outlines of Fabrication

The construction of three-dimensional structures usually employs planar processing. That is, to do processing in each layer to form the 3-D structure. This approach is quite versatile and powerful, though some limitations do apply on what types of structures can be made.

The structures under investigation are better suited for planar processing than other 3-D PBG structures. All the process steps are within the capability of the currently available technologies. Though as described in previous chapters, fine tuning of machines and novel recipes are necessary to achieve the desired device feature characteristics.

It is effective to obtain the necessary parameters and recipes by using monitor wafers and test structures before processing real devices. Various test structures are used to test the feasibility of a process and a number of monitor wafers are used to determine the parameters and recipes for the real fabrication of photonic crystals.

3.1 A brief introduction to VLSI technology

VLSI technology refers to the equipment and processes used for fabrication of microelectronic devices. Recently, many of its components have been extended to the Micro-Electronic Mechanical Systems (MEMS) and opto-electronic systems.

VLSI technology can be classified into five unit processes [23]-[25].

(1) Thin film deposition. This includes physical deposition (evaporation and sputtering), Chemical Vapor Deposition (CVD) and epitaxial growth.

(2) Lithography transfers the design information to a resist material. Methods include
resist technology, optical and non-optical lithography.

(3) Pattern transfer: these processes transfer the resist pattern to the deposited films. Etching, lift-off and plating are the major methods.

(4) Hot processing and ion implantation: these processes are used to change the properties of the layered films. An important application is to introduce the impurities in the semiconductor by diffusion or ion implantation. Some other hot processes include rapid thermal processing (RTP) and thermal oxidation, etc.

(5) Planarization technology: this includes Spin On Glass (SOG), Etchback, and Chemical Mechanical Polishing (CMP). Recently, more and more layers are required to be stacked together. Since the patterning processes usually alter the planarity of the starting surface, planarization is necessary for the successful device fabrication.

In the following sections, we will briefly discuss the processes and equipments that are applicable to the fabrication of PBG structures. Detailed descriptions and discussions can be found in text books (see for example, [25]).

The fabrication of photonic structures shares a lot with the current VLSI processes for microelectronic devices. The only difference is that PBG fabrication does not require hot processing or ion implantation, though the former may improve the robustness of the final structure. This is very important, since every electronic device has certain "thermal budget", i.e. the time and temperature a device can go through a high temperature environment. The fact that the PBG fabrication does not add to the thermal budget is critical to the future integration of PBG structures with electronic devices.

3.1.1 Film deposition

A variety of thin films with different chemical compositions can be deposited.

3.1.1.1 Chemical vapor deposition

Chemical Vapor Deposition (CVD) is the major film deposition method in the IC industry. Many important films, e.g. poly-crystalline silicon, insulating dielectric films, and local interconnects of W, are deposited by CVD.

The mechanism of CVD involves the pyrolysis or surface reactions to form solid films
on the substrate surface. The thermal CVD can be categorized into hot wall and cold wall configurations. Most of the applications now in use are hot wall processes. The advantage is the uniformity but the disadvantage is the waste of reactants and the resulting temperature control problems. Multiple gas feedthroughs are installed inside the tube to improve the wafer-to-wafer uniformity and temperatures are gradually increased along the gas flow to compensate for the reactant depletions. A batch of wafers (up to 150) are processed at the same time. Recently, new trends of small batch process are preferred for larger diameter wafers and for faster ramping up/down. In PBG fabrications, silicon, silicon dioxide and silicon nitride can be deposited by hot-wall thermal CVD. The cold wall process suffers uniformity problems originated from the non-uniform heating. One recent application is single wafer rapid thermal chemical vapor deposition (RTP CVD) which is complementary to the slow batch hot wall processing.

Another type of CVD is the plasma enhanced chemical vapor deposition (PECVD). It is a combination of a glow discharge process and low pressure chemical vapor deposition in which highly reactive chemical species are generated from gaseous reactants by a glow discharge and interact to form a thin solid film product on the substrate and electrode surfaces. The plasma assists or enhances CVD reaction and reduces the temperature required for normal deposition. PECVD tools are usually configured as cold wall processes.

PECVD is highly desired for the back-end-of-line (BEOL) processes where the source and drain of the transistors have been defined, and the high temperature process has to be tightly controlled to minimize the dopant re-distributions.

An important feature of the film deposition is the excellent control of film thickness less than 1 nm.

3.1.1.2 Electron beam evaporation

Some films do not form out of chemical reactions and have to be deposited in a pure form e.g. metals. A high energy electron beam is utilized to heat up the source in a high vacuum chamber and the evaporated molecules/atoms redeposit upon hitting the cold substrate surfaces. Almost all the metals and alloys can be deposited in this way. Silicon and silicon
dioxide can also be evaporated. A special crystal can be used to measure the thickness of deposited films based upon the change of resonant frequency of the crystal.

### 3.1.1.3 Sputtering

Sputtering is a term used to describe the mechanism in which atoms are dislodged from the surface of a material by collision with high energy particles. The sputtering process consists of four steps: 1) ions, i.e. $\text{Ar}^+$, are generated in a glow discharge plasma and directed to a target; 2) the ions sputter target atoms; 3) ejected (sputtered) atoms are transported to the substrate; 4) and condense to form a film. Since the ejected atoms are neutral, they can go toward the substrate against the electric field in the plasma. This method is also useful for materials that do not form from gaseous species. Comparing to e-beam evaporation, sputtering has better film thickness control and uniformity, but may be subject to more particle contamination.

All the above film deposition methods will be applied to the fabrication of PBG structures and the methods selected are based upon the availability of machines, contamination concerns and ease of process control.

There are some other methods of film deposition/growth. One is the epitaxial growth, which is characterized by a single crystalline film grown on the clean and defect free single crystalline substrate [25]. Another way of growing films is the direct oxidation of the substrate. For example, the most critical film in a field effect transistor (FET), the gate oxide is grown by the direct oxidation of single crystalline silicon wafers in dry oxygen or steam. This kind of film has the best film integrity and least particle contamination.

### 3.1.2 Lithography and etching

Pattern transfer involves the exposure of a radiation sensitive material (resist) with a specific radiation (e.g. UV light, X-ray or electron beam), resist development and the subsequent selective removal of the opened region of the resist. The lithography can be categorized into photolithography, X-ray lithography and electron beam lithography (EBL), corresponding to the radiation used. Etching includes wet chemical etching and dry
3.1 A BRIEF INTRODUCTION TO VLSI TECHNOLOGY

plasma etching. Another pattern transfer technique, lift-off is also discussed in this section.

3.1.2.1 Optical lithography

Optical lithography is the most common method for device fabrication and the resist materials are usually called photoresist.

![Diagram of photolithographic pattern transfer]

Figure 3-1: A generic representation of photolithographic pattern transfer

Fig. 3.1 shows a generic process schematic of optical lithography and anisotropic etching. A layer to be patterned is coated with photoresist (a, b) and is then exposed to light through a mask (c) and developed (d). In the case of positive resist (shown here), the exposed parts of the resist layer are removed during development, whereas in the case of negative resist, the unexposed parts are removed. The patterned resist layer then serves as a mask for the etching of the underlying film (e); finally, the resist is removed (f). Note that this procedure is also applicable for other lithography and etching processes.

A set of masks with designed pattern on is necessary for the pattern transfer. The mask itself can be generated with electron beam lithography (EBL) which will be discussed in the next section.

Three types of photolithography techniques have been implemented for pattern transfer: contact, proximity, and projection printing.
Contact photolithography is the first method used for IC fabrication. The frequent contact between the mask and photoresist generates defects in the mask and makes the mask unusable. Interestingly, it still gives the best resolution and most faithful image transfer.

In proximity printing, there is a gap between the mask and the wafer, therefore the mask can be used for much longer printing cycle. However the resolution degrades significantly.

Projection photolithography is the dominant technique in the industry for patterning various types of integrated circuits. The mask is separated from the wafers and the pattern in the mask is imaged and reduced 4x, 5x or 10x to print on the wafer. This considerably relieves the mask-making task, since the mask can be made 5x larger than the minimum feature size to be printed. The whole wafer can be patterned by a step-and-repeat manner and the lithography tool is called a “stepper”.

In this project, contact photolithography is used to transfer PBG pattern to the wafer and to achieve alignment between successive layers.

**3.1.2.2 Electron Beam Lithography (EBL)**

Electron-beam lithography is the process of forming patterns directly on radiation-sensitive materials (resist) using a high-energy focused electron beam. Fig. 3.2 is a schematic of an EBL system. EBL system exposes one pixel at a time and then the beam is moved (and blanked if necessary) to the next pixel. In this manner, a pattern can be generated in the resist after the subsequent development. The EBL can be categorized into **raster scan** and **vector scan** systems [26], [27]. In the raster-scan mode, the beam passes through an X deflector that scans the beam in the X direction as the stage moves in the Y-direction. The pattern is stored in a bitmap and fed to a beam blanker that determines whether the beam can pass or not. In the vector mode, the beam is directed by X-Y deflectors only to the location of each area to be exposed. Patterns are fed into the software that controls the Digital to Analog Converter (DAC) of the X-Y deflection amplifiers. A beam blanker is also necessary to avoid exposing unwanted area when the beam is moving from one location to another non-adjacent location. Since in many cases, the exposed area is much less than 50 percent of the total field, the vector scan improves considerably the through-
put. In order to improve the accuracy of the image addressing, the stage position is constantly monitored by an x-y laser interferometer, and a feedback loop compensates for system drift by feeding a correction signal to the deflector.

Figure 3-2: Schematic of an e-beam pattern generation system (after [31]).

Electron-beam lithography is ideal for device research and advanced prototyping. The direct writing avoids the mask-making step in optical lithography and is ideal for applications where fast cycling time is essential. Compared to optical lithography, EBL has much higher resolution and layer to layer registration. While the optical lithography resolution is limited by the diffraction effect, the wavelengths of electrons in EBL systems are on the
order of 0.1 Å, and diffraction effects can be neglected. Since the electron beam can be focused to very small diameter (to 5 nm), resolution as high as 20 nm can be achieved [28]. The e-beam itself can be used as a probe to detect features on a substrate, and this leads to extremely accurate layer-to-layer registration.

However, the major drawback of EBL is the extremely low throughput. Recently, several versions of projection and proximity electron beam lithography systems have been developed [29]. Nevertheless, these technologies still face with difficulties of mask-making. Other limitations of EBL include the proximity effects, intra-field distortions, and stitching errors [30].

In this project, electron beam lithography is used to pattern the complicated shapes required by the PBG structures. Since the shapes are periodic, proximity effect is compensated through modifying the mask layouts to achieve the designed feature sizes.

Due to electron scattering, the profile of developed PMMA is usually straight or undercut, which is ideal for lift-off process.

3.1.2.3 Lift-off

The lift-off technique is a powerful method for defining metal patterns with extreme high-resolution. It takes advantage of the long mean free path of the evaporated atoms in the electron beam evaporator, where pressures down to $10^{-6}$ torr are typical. With a point source, the shadowing effect can occur during the evaporation. Since the evaporant travels in straight lines without collisions, the vertical or negatively sloped side walls will be shadowed from the straight lines of the evaporant from the point source, and very little or no deposition will occur on the side-wall (Fig. 3.3).

The lift-off process usually applies to a patterned resist or other sacrificial layer (i.e. oxide) with straight or negatively sloped sidewall. After the evaporation, a wet etchant selectively etches away the resist or other sacrificial material and the deposited material on top of it. Therefore the substrate is left with an image-reversed pattern in the evaporated film. This technique is only limited by the lithography and the patterning doesn’t involve the anisotropic dry etching, which may not be available for a variety of metal films.
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Pattern Photoresist

Substrate

Evaporate Metal, (e.g. Ni-Cr)

Substrate

Lift-off Ni-Cr

Substrate

Figure 3-3: Schematics of lift-off. The right side is a more realistic cross sectional view of lift-off.

However, lift-off adds an extra process step. Also point source evaporation needs special care and can not be done in a batch manner. Therefore, it is only popular in the research projects. In industry, since much of the patterning is for the films that can be dry etched, i.e. Si, SiO₂, the more popular way of wafer patterning is the resist patterning and RIE etching.
3.1.2.4 Etching

There are basically two types of etching in micro-fabrication: wet etching and dry etching. For the wet etching process, the wafers are immersed a special type of chemical solution that is called an etchant. The etchant selectively etches the substrate where there is no protection layer (i.e. resist). This is adequate for large feature sizes (several μm), but because the purely chemical etch produces isotropic profiles (see Figure 3.4), accurate feature definition becomes difficult as device dimensions shrink and unacceptable loss of critical dimension control becomes a concern.

Dry etching, in most cases utilizing a glow-discharge plasma, proves to be the answer to anisotropic etching. In this kind of process, the etching gas molecules are dissociated (or activated) in a plasma, ionized and accelerated to the substrate. The ion bombardment helps significantly the reaction between the activated ions and the film to form volatile products. As a result etching is preferred in the direction of the ion bombardment. Since the trajectories of ions generated in a low pressure (~10 mtorr) glow discharge are nearly normal to a substrate surface, the potential for highly directional etching exists. On areas that are covered with a mask material which is not reactive to the ions, the material removal rate is much slower. In this manner, the pattern formed in the resist (or other etch mask) can be “carved” into the film with nearly straight sidewall. An example of an ideal anisotropic profile is shown in Fig. 3.4.

Low pressure, directional plasma-based etching is also called reactive ion etching (RIE). In the process of PBG fabrication, anisotropic reactive-ion etching is key to achieve the designed structure profiles.
3.1.3 Planarization

Every process of pattern transfer introduces non-planarity to the topography. Moreover, the topography differences accumulate when multiple layers are stacked up. Historically, electronic devices contained only a few layers of materials: field oxide, gate dielectric, gate materials and one or two layers of metal for interconnect. The lithography tools used then had fairly long wavelength, low Numerical Aperture (NA), and therefore large depth-of-focus \((DOF=\lambda/2NA^2)\).

When devices are scaled down, more layers of materials are required and the topography differences add up to an extent that adversely affect the integrity of the deposited films, i.e. stingers of metal films over steps, voids in gap filling, etc. Also the depth-of-focus (DOF) becomes smaller since lithography tools using shorter wavelengths are required to print finer feature sizes. This presents difficulties in critical dimension control of features over topographical steps.

Planarization techniques are closely interwoven with conformal deposition of films to fill in topographically recessed regions (e.g. gaps and trenches). Usually, dielectrics are used to fill the gaps, including silicon dioxide, spin on glasses (SOG), and polyimide.
Doped silica glasses can be reflowed at 950–1100 °C to increase step coverage, while SOG and polyimide are liquids at room temperature and after curing, will fill the gaps. Bias-sputtering high-density-plasma-enhanced chemical-vapor deposition is becoming more and more popular for low temperature gap filling for a variety of applications [32].

Etchback and chemical mechanical polishing (CMP) are the major planarization techniques. Etchback refers to the blanket etching of a surface which is already planarized with a spin on dielectric technique (i.e. SOG or polyimide). This technique can achieve local planarization which is related to only short-range variations in the topology. The solution to global planarization, specifically changes which occur over the entire image field of the stepper, is CMP. It polishes wafers using a special soft and flat pad with the help of a special chemical solution, called the “slurry”. The slurry helps in the selective polishing of selected materials, i.e. BPSG or oxide. This approach is conceptually simple but the process requires tight control of both the temperature and the pH of the polishing medium in order to maintain a consistent removal rate during the polishing step, as well as from run to run. With careful control of these parameters, and choice of polishing solution, it is possible to obtain an etch stop action with CMP. Elaborate rinsing procedures are necessary for removal of particulate residues from the slurry and the polishing pads, after the CMP operation is completed. CMP appears to be the only route for achieving truly global planarization over an entire substrate for microcircuits with minimum feature sizes below 0.35μm. CMP has become the dominant technology for planarization, in the semiconductor industry. Recently, more and more attention has been directed to the CMP of other materials, such at W and Cu, for advanced interconnects.

For the project on 3-D photonic crystals, gap-filling and planarization is essential to the fabrication of next layer, and considerable effort in this project was spent on the planarization of silicon dioxides.

### 3.2 Fabrication Strategy

This project is essentially about process development and integration. All the unit processes are available but fine-tuning is necessary to push to the limit of some of the
3.2 FABRICATION STRATEGY

equipment. Also, the sequence and selection of available processes is critical to the success of the project, especially in the view of the long fabrication cycle-time and low yield.

In this section, we focus on the analysis and characterization of the 3-D PBG to be fabricated, evaluate different approaches beforehand, and choose the optimum ones for the actually fabrication.

The straightforward way of fabricating the structure is to deposit films, pattern them, re-fill the gaps, and planarize the surface; then repeat the process. Two approaches are considered. One is to use electron-beam lithography to fabricate the structures on a few small demonstration dies, and the other is to explore an IC compatible process that’s capable of volume production. Some more details are discussed below.

1. Si/SiO₂/Air vs. Si/Air structure.

For e-beam lithography, since the patterns can be altered relatively easily, we can try the Si/SiO₂/Air and Si/Air structures at the same time. For IC compatible processes, due to the expense and long cycle time of the mask making, Si/SiO₂/Air and Si/Air structures are put on the same mask. Although film thickness is different for the two structures, the band gap will not change much for the small differences.

2. When to drill the holes.

The process originally envisioned a hole-drilling process after all the layers were put down. This is a major challenge since the aspect ratio is about 5:1 and we have to etch the Si and SiO₂ at the same time and with similar rates. For e-beam lithography, since the e-beam can expose virtually any shape, the process can be simplified by etching holes on each layer. For the IC compatible process, due to the diffraction limit of the photolithography, the structure is fabricated with gratings first and holes are drilled after all the layers have been deposited.

The alignment challenge for the two approaches are the same because both involve X direction, Y direction and rotation (θ) alignment.

3. Alignment schemes.

Electron beam lithography systems can provide high accuracy layer to layer registration because it is also a scanning electron microscopy(SEM). However, special procedures
are required for alignment mark detection.

For optical lithography, the feature sizes are approaching the limit of the optical microscope and a scheme of Interferometric Broad-Band Imaging (IBBI) is applied to improve the alignment capability of contact aligners for photolithography. The IBBI, which employs grating and grid type alignment marks on mask and substrate, will be discussed in Chapter 5.

4. Planarization techniques

Etchback is used in the e-beam process because the die are small (75–150 μm²). Moreover, etchback provides better process control. The IC compatible process uses CMP for planarization. In our project, a thin layer (300Å) Si₃N₄ is used as an etch stop. The CMP of silica materials such as BPSG requires the use of certain abrasive slurry in a solution with hydroxyl groups. Colloidal silica, in a KOH solution, is commonly used for this purpose, although sodium- and potassium-free slurries are also available. A polishing rate of about 750 Å/min is typical during this operation.

Fig. 3.5 shows the process schematic of the IC-compatible process, and the process using e-beam lithography is similar to it.

A novel approach to fabricate PBG structures is to utilize bonding. It puts structures directly on top of one another either through wafer bonding or membrane bonding. This approach avoids a significant amount of processes for gap filling and planarization. Also the membranes or wafers can be processed in a batch fashion, with bonding required only to assemble the PBG structures. This reduces considerably the cycling time and the yield should also be increased.

Though wafer bonding techniques have been applied to MEMS and other applications, the bonding and alignment at submicron length scales present new challenges, e.g. material properties, membrane handling, and alignment stage construction, which have never been explored before. Special techniques need to be developed for this approach.
3.2 FABRICATION STRATEGY

Outline of the IC Compatible Fabrication Process

Figure 3-5: Schematic of PBG fabrication using IC-compatible processes
Chapter 4

Fabrication of 3-D PBGs with e-beam lithography

4.1 Overview

In this chapter, the fabrication of the first two layers of the Si/Air 3D PBG structure with the bandgap centered at 1.53 μm is demonstrated, and a viable alignment scheme is also provided.

Electron Beam Lithography (EBL) is the ideal choice of the lithography tool for demonstrating PBG device fabrication because of its excellent resolution, accurate layer-to-layer registration and the ability to rapidly pattern small quantities of demonstration dies.

The fabrication of the first layer starts with the sequential deposition of Si₃N₄ and amorphous Si, followed by scanning-electron-beam lithography using PMMA as the resist. Then trenches are etched into the amorphous Si using lifted-off Ni-Cr as a hard mask. Finally, oxide trench-filling and planarization finish the first layer fabrication. A careful alignment is necessary to successfully fabricate the second layer. Fig. 4.1 is a schematic summary accompanied by SEM micrographs of the fabrication of first two layers of the PBG structure.

4.2 Fabrication of the first layer 3-D PBG structures

A schematic of the first layer fabrication is shown in Fig. 4.2.
Summary of 2-Layer 3-D PBG Structure Fabrication

Figure 4-1: A summary of 2 Layer 3-D PBG structure fabrication
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

Figure 4-2: Schematic of the first layer fabrication
4.2.1 Deposit Si₃N₄ and amorphous silicon layers

A thin layer of Si₃N₄ was first deposited to be the etch-stop layer of Si. The thickness was around 20 nm. This can be done with LPCVD or PECVD. Since this was the first step of the process, we could use the IC compatible tool of tube A5 in the Integrated Circuits Laboratory (ICL) of MTL at MIT. The recipe was #461 and the main deposition time was 7 minutes. More detailed description of this process can be found in Chapter 5.

A layer of 420 nm amorphous Si was then evaporated onto the Si₃N₄ layer using electron-beam evaporation in the Nanostructure Laboratory (NSL). The thickness was controlled within 10%.

4.2.2 Lithography

4.2.2.1 PMMA coating

The resist for electron-beam lithography was Poly-Methyl-Methacrylate (PMMA), a type of linear high-molecular-weight polymer. Upon exposure to the high-energy electrons, as well as the lower energy secondary electrons, PMMA undergoes chain scission and can be removed with a special solvent (developer). Thus PMMA is a positive resist. It provides excellent resolution but at the cost of low relative sensitivity. PMMA is a good choice for development of a process.

It is important to know the thickness of coated PMMA, because this will affect the relative dose of the exposure and therefore the critical dimensions of features. A Dektak profilometer was used to measure the resist thickness. Test wafers were coated with 3% 950 K molecular weight PMMA at various spin rates. After a one-hour baking at 180 °C to remove the solvents, the wafers were scratched with a needle and the resulted grooves measured with Dektak. Figure 4.3 is the resulted spin curve. We set the spin rate at 3000 rpm to achieve a PMMA thickness of ~210 nm.
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

4.2.2.2 Electron beam direct writing

The extremely small feature sizes and irregular shapes of the PBG structure necessitate the use of scanning-electron-beam lithography. A Scanning-Electron-Beam Lithography (SEBL) system (VS-PL) was donated from IBM corporation and is located in Room 38-185 at MIT. It is a step-and-repeat vector scan machine with a custom digital-pattern-generator (DPG). Patterns are exposed by moving the substrate (e.g. mask or wafer) under the electron beam column and exposing one small region (called a field) at a time. The stage steps from one field to the next to complete the whole pattern. Within a field, the pattern is composed of primitive shapes such as boxes, lines, etc. which have been programmed into the DPG. A shape is exposed by moving to a starting point with the beam blanked off (by the electrostatic deflection of the beam out of an aperture high up in the column), waiting for the deflection system to settle, and then unblanking the beam, and

Figure 4-3: Spin curve of 3% 950 K PMMA
scanning to fill the interior of the shape. The scanning rate and the beam current dictate the dose each shape receives. In the case of very small shapes, such as single-pass lines, the dose may determine the critical dimension (CD) of the line in resist. The size of a shape in resist may also depend on the dose of the shapes near it (proximity effect). To achieve the desired size in resist, the dimensions of a shape may have to be adjusted before exposure.

(a) Pattern Design and dose optimization
The electron-beam lithography system writes the pattern directly in resist on substrate. This avoids the usually slow and expensive procedure of mask-making, and allow rapid modifications of pattern, something that is essential to the proximity correction of the PBG structures. The disadvantage of slow writing speed is not a concern for pilot processes in research.

The specialized nature of the way in which the SEBL system exposes a pattern dictates the way the pattern is described digitally. Different SEBL systems typically have hardware-specific pattern file formats. The pattern file format of this system is called VSX, which is optimized for electron-beam writing, but is not suitable for pattern layout. Pattern layouts in KIC file format can be converted to VSX using a program called kic2vsx, with a conversion file *.

Figure 4.4 shows the optimized dimensions for the 3-D Si/Air structure to be fabricated. This pattern was entered into the Computer Aided Design (CAD) tool KIC, which uses small primitive shapes of lines, boxes, paths, to compose the shapes to be exposed. A portion of the layout is shown in fig. 4.5, with complicated shapes of PBG structures approximated with small boxes. Since the SEBL uses a Gaussian shaped beam profile, it smooths the sharp edges of the design, resulting in well shaped circles.
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

Figure 4-4: Top view of a 3-D PBG structure with defects (Si-Air structure at 1.53 μm wavelength)

Figure 4-5: KIC layout of the 3-D PBG pattern. The black (exposed) areas are for Si.
The critical dimensions of the exposed PMMA depend on the dose, or the number of electrons per unit area at a given acceleration voltage. The dose is determined by the time interval the beam spot stays at a specific pixel, and is inversely proportional to the frequency at which the beam is stepped along steps (writing frequency). The dose also depends on the spacing of the two consecutive beam steps. The larger the beam step, the smaller the average dose in a given area.

In the VS-PL SEBL system, an e-beam field consists of 16,384 x 16,384 pixels, independent of the field size. Therefore, the smallest beam step or writing resolution is determined by the field size. Smaller field size provides better resolution but larger field sizes are desired for fabrication and measurement concerns. We designed the structure with 75 μm, 100μm, and 150 μm field sizes, respectively. For different field sizes, the dose or the writing frequency had to be adjusted correspondingly. For field size of 75 μm, a writing frequency of 0.37 MHz was found to be the optimum, and for device sizes of 100 μm, and 150 μm, the optimum frequencies were found to be 0.19 MHz, and 0.083 MHz, respectively. Notice that the frequencies are roughly inversely proportional to the total field area.

(b) Writing procedure
The SEBL system can be run in either an SEM mode or an EBL mode. In the SEM mode, we find the registration marks, focus the electron beam, and can map the system with user coordinates.

A drop of gold colloids with 50 nm particle size was put on coated PMMA and dried to serve as a fine artifact for focusing the electron beam. For the best focus, an artifact should be comparable to the beam spot size. In our case, the beam spot size is 60 nm at 35 pÅ emission current. The gold colloids were manually mapped and loaded into the SEBL chamber. Under SEM mode, the gold colloids could be found near the coordinates mapped and interferometer readings of the stage position recorded. Coarse focus was achieved at the visually sharpest colloid image on the monitor. Fine focus could be obtained by single line scanning and maximizing the slopes on the oscillation. Focus was monitored via the current readings in the magnetic objective lens coil and found to be stable during the
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

writing (less than 0.1% drift).

Since the orientation of samples in the SEBL can not be exact, the coordinate system has to be remapped to correct the rotation of mounted samples and system drift. This was done by finding two or more known positions and by inputting the absolute coordinates, and then a linear transformation was applied. This procedure is very important for exposures with alignment.

Stage position is monitored with laser interferometry; a 0.5 nm displacement can be detected. However, the mechanical system can not sustain the stability within ±0.5 nm. Therefore a specific feedback system is employed to continuously correct the vibration. The X-Y position of the stage is monitored constantly by the laser interferometer, and any shift away from the specified position generates an extra deflection field which dynamically "directs" the beam to the desired place.

The automatic exposure process is controlled with a batch file. The batch file specifies a sequence of pattern files at the user mapped x-y coordinates where the patterns are to be written. Before each run, the stage is driven to a desired field position for exposure.

Before each exposure, it is important to carry out a field calibration, which is done through a field calibration routine. The purpose is to account for the non-orthogonality of the mirrors mounting on the stage, used in the HP interferometer relative to the X-Y stage axes. It also accounts for rotation of the scan field, non-orthogonality of the beam scanning directions and non-linearities in the deflection amplifiers. It achieves this by first focusing on some small artifacts (e.g. 60 nm gold colloids), and second moving the stage with a set amount of distance (i.e. 150 μm), which can be read from the HP interferometer. Then it deflects the beam to "look" at the artifact in its new location. Once it finds it, a self correlation [33] against the same image stored in memory enabling adjustment of the beam deflection, rotation, etc., to achieve the maximum correlation (Further correlation algorithm will be discussed in 4.3). If the registration feature is too far away (the field setting is far off), the deviations can be corrected with operator assistance. By running the field calibration routine, information is gathered to correlate the place the beam thinks it has gone with the place it "actually" is. And this equipment setting is saved for the subsequent
exposure.

![Figure 4-6: Field rotation and the displacement after flipping along Y-axis](image)

It is quite important to do the field calibration when writing both on the optical mask and on the substrate for the subsequent optical lithography. Since the optical mask is flipped 180° around the Y-axis when doing optical alignment, a rotation of the e-beam field can spoil the alignment as illustrated in Fig. 4.6.

### 4.2.2.4 Developing the exposed PMMA

The exposed areas in the PMMA have considerably lower molecular weight than unexposed areas and therefore their solubility in a proper solvent developer changes significantly. There is a special dose threshold above which the solubility of exposed PMMA in the developer will increase dramatically (roughly a cubic function of dose). This effect is called the "clipping" effect (Figure 4.7). This is also a reason why we can achieve resolution comparable to beam diameter. The proximity effect correction also takes advantage of this clipping effect.

The developer used were a 2:1 volume ratio of Isopropynol: MIBK. The development rate is very sensitive to temperature and the process was optimized to be at 20~21 °C for 90 seconds. Figure 4.8 is the top view of the developed PMMA.
4.2 Fabrication of the First Layer 3-D PBG Structures

4.2.2.5 Ni-Cr Lift-off

Since PMMA is not a good resist for reactive ion etching, a lift-off process of 60 nm Ni-Cr metal layer was applied after the PMMA development. This step was done with the electron beam evaporator in NSL with a point source of the Ni-Cr alloy.

To account for the image reversal of the lift-off process, the electron exposed areas in PMMA were for the Si veins and the evaporated Ni-Cr would be the hard dry etching mask to protect the these Si veins. Figure 4.9 shows the evaporated Ni-Cr under SEM.
Figure 4-8: Tilted top view of developed PMMA resist. The resist profile could be seen to be nearly vertical.

Figure 4-9: Top view of sample after Ni-Cr lift-off
4.2.2.6 Proximity compensation

Comparing figures 4.5 and 4.9, it was found that the designed pattern and feature sizes were not met. This is due to the proximity effect, i.e. exposure in areas remote from the beam entry point due to the long range backscattered electrons.

When the electron beam strikes a resist-coated surface, the electrons are scattered and the beam is broadened. The exposed resist due to a single beam becomes a strong forward spot surrounded by a broad circle partially exposed by backscattered electrons. Therefore the total exposure dose any one point receives is the sum of the doses from scattered electrons which might origin several microns away.

Figure 4.10 illustrates some consequences of the proximity effect on a developed image.

![Figure 4-10: Proximity effects caused by electron scattering. Square boxes are designed features and gray areas are the exposed pattern.](image)

At point A (the center of a large exposed area), there are doses contributed from surrounding neighbors. At the corners and edges of this large exposed pattern, however, the same total dose is not received, for example at point C, only one fourth of the scattered electron dose is received comparing to point A. On the other hand, adjacent patterns may exhibit cooperative exposure effects if they are closely spaced (as in area B).

If the dose is optimized to obtain the correct features size of pattern A (right side of Fig.
4.10), then the narrow line in the left part of Fig. 4.10 will be underexposed while area around B will be over exposed.

One way to compensate the proximity effect is to write the edges with a higher does (i.e. slower frequency). However this is hard to be implemented in the VS-PL EBL system. Other solutions include using multi-layer resists to absorb back scattered electrons or writing pattern on thin membranes.

My solution to the proximity effects took advantage of the periodicity of the pattern. Since at the edge of a pattern the exposure does is relatively low, some serifs were added to increase the does at the designed feature edges, while the serifs themselves do not have enough exposure dose and therefore are not developed due to the “clipping” effect of the PMMA development curve. This is in analogous to the Optical Proximity correction used extensively in the industry to compensate for the diffraction of light.

A variety of mask design were tested and an optimum mask layout was found to give the right dimensions of the desired structure (Fig. 4.11).
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

4.2.3 Reactive-Ion Etching of the amorphous Si to form the trenches

Once the pattern is defined with Ni-Cr, the wafer is ready for etching, which will transfer the pattern into the deposited a-Si layer. There are generally two types of etching method: isotropic wet etching and anisotropic dry etching. Since in the PBG structure the trench depth is comparable (even larger) than the minimum feature size, anisotropic etching is required. In the dry etch process, the etching gas molecules are dissociated (or activated) in a plasma, ionized and accelerated to the substrate. The ion bombardment helps significantly the reaction of the activated atoms with the substrate to form volatile products, and thus the etching is preferred in the direction of the ion bombardment, which is usually normal to the substrate. On areas that are covered with another material which is not reactive to the ions, the material removal rate is much slower than the exposed substrate. In this manner, the pattern formed in the resist (or other etch mask) can be “carved” into the
substrate with straight sidewalls.

The etching tool used was the PlasmaTherm System IV, 790 Series in NSL. It is a standard RIE etching tool with backside Helium cooling capabilities. Before Si etch, a descum and cleaning process (Table 4.1) was applied to completely remove the organic residues and other contaminants. Without venting the chamber, silicon was etched with CF$_4$ and O$_2$. The recipe is shown in Table 4.2. The gas flow in the main etch step contained 10% of O$_2$ in CF$_4$, which optimized the etch rate [34]. The etch-rate was about 33 nm/min and to achieve a depth of 4200 Å required 12 minutes.

<table>
<thead>
<tr>
<th>Step Number</th>
<th>Hold Time (sec)</th>
<th>Pressure (mtorr)</th>
<th>RF Power (W)</th>
<th>O$_2$ (sccm)</th>
<th>He (sccm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Pumping down</td>
<td>30</td>
<td>0.09</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2. Flow gases</td>
<td>60</td>
<td>40</td>
<td>0</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>3. Spark plasma</td>
<td>5</td>
<td>40</td>
<td>150</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>4. Descum</td>
<td>20</td>
<td>40</td>
<td>150</td>
<td>10</td>
<td>5</td>
</tr>
<tr>
<td>5. Flow gases</td>
<td>60</td>
<td>45</td>
<td>0</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>6. Spark plasma</td>
<td>5</td>
<td>45</td>
<td>50 V DC</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>7. Clean</td>
<td>30</td>
<td>7</td>
<td>50 V DC</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>8. Pumping down</td>
<td>10</td>
<td>0.09</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 4-1: Descum and cleaning process recipe before Si etch

<table>
<thead>
<tr>
<th>Step #</th>
<th>Hold Time (sec)</th>
<th>Pressure (mtorr)</th>
<th>DC Voltage (V)</th>
<th>RF Power (W)</th>
<th>O$_2$ (sccm)</th>
<th>CF$_4$ (sccm)</th>
<th>Backside He Flow (sccm)</th>
<th>Pressure (torr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Pumping down</td>
<td>30</td>
<td>0.09</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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</table>
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

Table 4-2: Process recipe for Si etch using PlasmaTherm.

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</tr>
</thead>
<tbody>
<tr>
<td>2. Flow gases</td>
<td>60</td>
<td>30</td>
<td>0</td>
<td>0</td>
<td>1.5</td>
<td>13.5</td>
<td>4.25</td>
</tr>
<tr>
<td>3. Spark plasma</td>
<td>5</td>
<td>30</td>
<td>400</td>
<td>~170</td>
<td>1.5</td>
<td>13.5</td>
<td>4.25</td>
</tr>
<tr>
<td>4. Etch</td>
<td>720</td>
<td>20</td>
<td>400</td>
<td>~170</td>
<td>1.5</td>
<td>13.5</td>
<td>4.25</td>
</tr>
<tr>
<td>5. Pumping down</td>
<td>30</td>
<td>0.09</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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Figure 4.12 is the cross sectional SEM micrograph of the first layer pattern etched into amorphous Si. Notice the straight side wall and smooth bottom surface. This is because fluorocarbon polymerizes on the sidewalls and prevent the lateral isotropic etching. This anisotropic etch was further enhanced due to the following facts:

(1) The hard mask of Ni-Cr does not erode in the fluorine plasma.
(2) A high plasma-substrate bias ensure a high ratio of vertical/lateral etch rate.
(3) Low chamber pressure (20 mtorr) reduces the ion collision which might result in
oblique ion bombardment and lateral etching.

Further improvement of sidewall profile can be achieved with lower pressure and lower etching temperature. The etch tool is capable of back side Helium cooling to reduce the substrate temperature.

4.2.4 Conformal deposition of oxide with biased HDPECVD

For the next layer Si deposition, the trenches in the first layer Si have to be filled with some materials, and be planarized to the top of the trenches. Materials that can fill the gap and be planarized include silicon dioxide, spin-on glass (SOG), and polyimide. Silicon dioxide was chosen because of its well-known characteristics, various available processes and ease of wet/dry etching.

The manner in which a thin film covers (or conforms to) the underlying features on a substrate is an important characteristic of a deposited film. Conformal coverage means that an equal film thickness exists over all substrate topography regardless of its slope, i.e. vertical and horizontal surfaces are coated with equal film thickness. At high deposition temperatures, most CVD films (e.g. LPCVD poly-Si, Si$_3$N$_4$) are conformal because of the high mobility of reaction intermediates (adatom mobility). At low temperatures, since the reactant surface migration is slow, the geometry of the substrate plays more important roles in the film deposition because it determines the supply of the reactants at a given point. For low pressure deposition, since the mean-free-path is relatively long, the bottom and side wall of a trench usually have less reactant fluxes and less film thickness. Figure 4.13(a) clearly shows that the upper corners of the trench have thicker oxide films deposited.

Usually, SiO$_2$ depositions are done at low pressures and low temperatures, thus are subject to non-conformal deposition. At a certain point during deposition, the overhang of the oxide at upper corners merge together and block the further deposition inside the trenches, thereby forming voids in the film. Figure 4.13 (b) shows the Low Temperature Oxide(LTO) films deposited thermally around 400 C using LPCVD.
Figure 4-13: (a) non-conformal LPCVD Low temperature oxide, (b) voids in LTO films. The pitches in SEM micrographs are 2.5 μm
Obviously, voids in trenches are not acceptable for next layer deposition. The solution can be found through the use of higher mobility intermediates and subsequent high temperature reflow of deposited films. PECVD produces reactants which arrive at the substrate with more energy (obtained in the glow-discharge) resulting in improved step coverage. However, filling high-aspect-ratio trenches is still a challenge for PECVD without bias-sputtering. Tetraethylorthosilane (TEOS) deposition by PECVD at 300 °C gives excellent step coverage due to the highly mobile reaction intermediates. Doped silicate glasses i.e. phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG), are used extensively in industry to achieve the conformal deposition and gap filling. The introduction of Boron and Phosphorus oxide loosen the oxide network and the resulting silicate glasses can be reflowed at temperatures around 900 °C – 1100 °C. However, due to the potential contamination, the equipment for TEOS or BPSG deposition are not available for this process in MTL.

Another solution to achieve conformal deposition at low temperature is to incorporate a sputter etching process during the deposition. Figure 4.14 shows the sputtering efficiency with respect to the incident angle.

![Figure 4-14: Relationships between sputter yield and incident angle (after [35]).](image)

As can be seen, the oblique incidence increases the sputtering efficient considerably. This will compensate for the overhang effects at the upper corners of the steps and thus
achieve gap filling. A schematic of gap filling process using deposition-etch-deposition-etch routines is shown in Fig. 4.15.

![Evolution of the Dep-Etch-Dep Process](image)

**Figure 4-15:** Schematic of gap filling using bias-sputtering deposition (after [32]).

The tool used for the bias-sputtering deposition is a PECVD/RIE machine called "PlasmaQuest", located in TRL. It is a high-density microwave plasma tool. A high frequency microwave (2.45 GHz) is used to excite the plasma through the electron cyclotron resonance (ECR) and the plasma can be directed out of the ECR chamber to the etching/deposition chamber (Fig. 4.16).

The advantage is to separate the plasma density (roughly proportional to Microwave power) and the substrate bias (related to radio frequency power). This improves the controllability of the plasma etching/deposition process (adding another dimension of control). In conventional plasma tools, the plasma density and substrate bias are both related to the power thus limited the process options. The success of bias-sputtering deposition depends on the bias to the substrate during the plasma enhanced CVD of oxide. The pressure of the deposition has to be very low (several mtorr) to enhance the sputtering. Conventional plasma tools can not provide enough plasma density at such low pressures.
and the net deposition rate can be negative. Only high density plasma tools can provide enough plasmas at such low system pressure and control the relative rate of sputter etching and oxide deposition.

Another advantage of the bias-sputtering deposition is that it also planarizes the deposited oxide, as can be seen in figure 4.16.

![Schematic and CVD tool for the ECR bias-sputtering deposition](image)

Figure 4-16: The schematic and CVD tool for the ECR bias-sputtering deposition (after [36]).

The recipes used for deposition are mq_sio3.rcp and mq_sio2p.rcp. The former provides the best gap filling while it erodes the upper part of the gratings and degrades the sidewall profile. Also it has very low deposition rate. However, these are tolerable for our structures at this stage. Figure 4.17 (a) shows the filled trenches with recipe mq_sio3.rcp. Aspect ratios as high as 2:1 can be filled without voids. The other process has faster deposition rate but leaves some voids in special places after etch back. However due to the special characteristics of our process, the voids in the holes do not affect the second layer fabrication because the Si on top of those oxide will be etched off (See figure 1 for reference). Both recipes are still under test to optimize the process. Figure 4.17 (b) shows the cross sectional SEM micrographs of filled first layer structures with a deposition time
similar to that in figure 4.17(a).

Figure 4-17: (a) test grating with trenches filled using recipe mqi_sio3.rcp, (b) first layer PBG structures with trenches filled using recipe mqi_sio2p.rcp. The trench depths are 400 nm.
4.2.5 Planarization by etchback

4.2.5.1 $O_2/N_2$ sputter etch

The first method of planarization is to extend the physical sputter etching in the biased HDPECVD deposition. The sputter etching uses physical momentum transfer to planarize the surface. As pointed out previously (figure 4.14), the material removal rate of sputter etching is strongly dependent on the incident angle. The protrusions on a deposited film will be gradually smoothed out during sputtering etching. The optimal gas for sputter etching is Ar, but it’s not available in the etching tool and $O_2/N_2$ was used instead[37].

Figure 4-18: AFM topography and cross section measurement after 20 min. $O_2/N_2$ sputter etch
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

Figure 4.18 shows the Atomic Force Microscope (AFM) view of the topography and a cross section measurement after 20 min. of O₂/N₂ sputter etching.

4.2.5.2 HF wet etch:
The isotropic wet etch is usually regarded as a drawback for pattern transfer, but is a good candidate for the planarization in this project. As a test, we deposited SiO₂ into the trenches with ECR plasma CVD to completely fill in the trenches. Then the sample was etched in buffered HF (BHF) for 30 seconds. The buffered HF contains about 1:6 volume ratio of concentrated HF (49% weight percentage) and NH₄F. The etch rate of PECVD oxide was around 1500 Å/min. Figure 4.19, 4.20 are the AFM pictures of the topography of as deposited SiO₂ and after 30 seconds BHF etch, respectively. As can be seen, the topography is considerably planarized.

This process also has the advantage of removing the stingers on the side wall of the metal masks. This is helpful to remove the oxide remaining on top of the metal masks when wet etching Ni-Cr masks.
A side effect is that the wet etch preferentially etches oxides along the side-wall. One possible reason for that is the interface stress induces enhancement of etch rate. A small wet etch rate is desired for the process control and dilution of the BHF solution is planned.

### 4.2.5.3 Isotropic dry etching at high pressure

At high pressure and low substrate bias, the directionality of the incident ions is disrupted by the high frequency of particle collisions. Therefore the etching is not as much directional as in low pressure and high biasing. This usually leads to the undercut of the trenches which is not desirable for pattern transfer. However it is good for planarization.

On the same test structure, AFM measurement were carried out before and after the isotropic dry etching (Figure 4.21).
4.2 FABRICATION OF THE FIRST LAYER 3-D PBG STRUCTURES

Figure 4-21: AFM cross section measurement on test gratings before (a) and after (b) 20 minutes of high pressure isotropic dry etching by CF$_4$

### 4.2.5.4 CMP

The semiconductor industry standard for planarization is Chemical Mechanical Polishing (CMP). CMP is good for achieving global planarization. However, process control is hard and the uniformity is not good (5~10% across the wafer). For PBG research, which work with a device area of 50×50 μm, the global planarization is not a concern.

A combination of methods (a)-(c) were applied to achieve the best planarization. The etch back was carefully controlled to stop at the top of the silicon trenches (Fig. 4.22, 4.23)

Figure 4-22: Planarized surface of oxide with a combination of sputter etch, wet etch and isotropic dry etch
4.2.6 Wet etch Ni-Cr to lift off oxide on top of Ni-Cr

The next step is to remove the metal mask on top of the silicon veins. A proprietary chemical solution was used to remove Ni-Cr. The etch rate was 40 Å/sec and a total etch time of 1 minute was applied to make sure the metals are completely removed (Fig. 4.24).
4.2.7 (optional) Selective Si etching to preserve planarity

The recess of SiO₂ after the etch-back is clearly visible in figure 4.24. This could cause some minor problems to the second layer deposition. Moreover, this recess of oxide can be accumulated in subsequent layers. A Si etch based on SF₆ and Cl₂ was developed to selectively dry etch Si. However, the surface of Si after etch became rough (Fig. 4.25).

Figure 4-25: Finished first layer PBG structure

4.3 Pattern alignment

The alignment scheme in the SEBL uses digital image processing and correlation, which was developed by V. Boegli and D. P. Kern at IBM [33]. This process is applicable to a variety of procedures, e.g., deflection field calibration, distortion evaluation, as well as alignment of successive mask levels in direct e-beam writing.

The advantages of the e-beam alignment lie in that its accuracy is proportional to the field size. It is expected that a field of 50 μm × 50 μm is sufficient for verifying the 3-D photonic bandgap. We chose to write the pattern in a larger field of 150 μm × 150 μm. In this way test structures could be put within the e-beam field to verify the alignment before
proceeding to the next layer etching.

### 4.3.1 Alignment mark design

The advantage of the correlation method is its threshold independent mark registration. Therefore the alignment scheme is very much noise tolerant. In order to achieve high immunity to artifacts in the environment of the marks, we used a pattern exhibiting a pseudo-random binary sequences (figure 4.26).

![Alignment Marks](image)

**Figure 4-26:** Layouts and SEM micrograph of alignment marks. (a) is used as the template for the correlation calculation, (b) is the SEM micrograph.

### 4.3.2 Alignment procedure

In the alignment mark registration routine, back-scattered electron signals are collected when the beam is scanned over a feature exhibiting a distinct contrast with respect to the substrate. The contrast can be due to topography or atomic number, since higher atomic number implies larger back scattering coefficients. Between the two methods, atomic number contrast is preferred.

During alignment, the beam scans only certain areas in a field, defined by the template file (usually the four corners of a field) to avoid unwanted exposure of the device area.
4.3 PATTERN ALIGNMENT

After detecting the four alignment marks, the beam scans the marks and calibrates the system in lateral shift, rotation, trapozoid and scaling, thereby remapping the coordinates according to the substrate.

In order to improve the signal-to-noise (S/N) ratio in the detector signal, the scan frequency was slower than the actual writing speed. We used the same current for the alignment and the writing. As a result the areas that contained the alignment marks were totally exposed after the writing. New alignment marks were generated for the next layer alignment.

Special cares, i.e. careful wafer mapping, were taken to avoid accidentally expose the device area when doing alignment or moving the stage.

When aligned, the lateral shifts were normally less than 1 beam step size or least significant bit (LSB). The following table presents a typical alignment setting for the 150 μm field size. The least significant bit (LSB) was 9.31 nm.

<table>
<thead>
<tr>
<th>#</th>
<th>Gain</th>
<th>X shift(LSB)</th>
<th>Y shift(LSB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.6250</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>2</td>
<td>0.6273</td>
<td>-0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>3</td>
<td>0.6316</td>
<td>0.4</td>
<td>0.1</td>
</tr>
<tr>
<td>4</td>
<td>0.6189</td>
<td>0.2</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Table 4-3: Lateral shifts and detector gains for the aligned settings.

Before actual alignment, alignments on test structures is necessary because the contrast and brightness affect the auto-correlation significantly.

4.3.3 Alignment results in test structures

A simple test process was developed to evaluate the e-beam alignment capabilities. Figure 4.27 shows the process schematic and the expected alignment between two layers. Figure 4.28 presents two SEM micrographs showing the variations of alignment shift for different dies. In the best case the structures were fully aligned (Fig. 4.28-a), while the worst case shows a misalignment of 60 nm. In other cases a mean shift of 31.6 nm was achieved, corresponding to 8% for a period of 790 nm for the 3-D PBG structures. This is within the design specification [21].
Figure 4-27: (a) Test mask layout, (b) Outline of the test alignment process
Figure 4-28: Best (a) and worst (b) case of test structure alignment.
4.4 Fabrication of second layer PBG structures

The fabrication of the second layer of 3-D PBG structures started with sputter deposition of amorphous silicon (table 4.4). The tool was located in room 38-161 at MIT. The deposition rate was 117 Å/min, and a deposition time of 23.5 minutes resulted in a 2750 Å a-Si film.

<table>
<thead>
<tr>
<th>Settings</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pressure</td>
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</tr>
<tr>
<td>Ar flow</td>
<td>25 sccm</td>
</tr>
<tr>
<td>RF power</td>
<td>200 W</td>
</tr>
<tr>
<td>RF voltage</td>
<td>1.5 kV</td>
</tr>
<tr>
<td>Presputtering</td>
<td>8 min.</td>
</tr>
<tr>
<td>Sputter time</td>
<td>23.5 min</td>
</tr>
</tbody>
</table>

Table 4-4: Sputter parameters for a-Si deposition

Sputtered a-Si and evaporated a-Si, used in first layer, are both suitable. The sputtered Si may have some type of planarization effect, however sputtered Si may have Ar incorporation and may have some effect on its optical properties. Further characterization of optical properties is planned to help select the better way of doing Si deposition.

After the a-Si deposition, samples were coated with Shipley 1808 photoresist and a photolithography step was applied to open windows for the alignment marks. The detailed description of photolithography steps will be given in Chapter 5.

The photomask was written with the same electron beam writer. It contained a set of 4 large square holes (20 μm × 20 μm) at four corners of each die. Careful field calibration was necessary to minimize the field rotation (figure 4.6). This optical mask was used to open alignment marks buried underneath Si and SiO₂ layers.

A selective Si etch was followed to remove the a-Si on top of the alignment marks and also to create a topography contrast for the alignment marks. The etching gases contained SF₆ and Cl₂.

After dry etching, a 60 nm Gold lift-off was done to replicate the topography steps.
Photoresist was then dissolved in acetone with ultrasonic agitation. This also removed the gold evaporated on top of photoresist.

The fabrication steps after alignment were basically the same as the first layer fabrication. Careful alignment was carried out.

The alignment shift between 2 layers was ∼45 nm for almost all the dies. This could be further improved in view of the extremely low contrast of the topographic alignment mark.

Figure 4.29 shows the final results of two aligned layers of PBG structures. (a) is the schematic and (b) is the SEM micrograph. The alignment shift was around 40 nm and the designed features sizes were well preserved. Notice the overetch of the second layer trenches into first layer Si veins.

![Schematic of PBG structures](image.png)
Figure 4-29: Figure 1-1: Aligned two-layer 3-D Si/Air PBG structures (a) is the schematic and (b) is the SEM cross section view.
Chapter 5

Fabrication of 3D PBGs using Optical Lithography

5.1 Overview

In the previous chapter, we discussed process steps for the fabrication of the PBG structures with bandgap centered at 1.53 μm. Using the electron beam lithography, the small feature size and satisfactory alignment could be achieved. However, this approach suffers severely from the extremely low throughput and long cycle time, which will adversely affect the adoption of PBG for practical applications. In order for the PBG structures to be practically available, the fabrication has to be compatible with the currently overwhelming Integrated Circuit (IC) fabrication. This is also very important in view of the future integration on opto-electronic devices that may contain PBG structures.

The Microsystems Technology Laboratories (MTL) has extended process lines for the IC fabrication at Integrated Circuits Laboratory (ICL) and Technology Research Laboratories (TRL). The goal of the second part of the research is to develop an Integrated Circuit compatible process for the PBG fabrication.

A significant distinction between the IC fabrication and other non-electrical device fabrication is the heavy metal contamination. Heavy metals, e.g., gold, when in semiconductors, have energy levels near the center of the bandgap and act as good recombination centers for the electrons and holes. Therefore, the leakage current is significantly higher to rapidly discharge the capacitor, which is the core of the memory in every kind of silicon chips.

To avoid contamination, all the equipment that potentially see gold should be separated
from other equipment that are used for IC fabrication. In the previous chapter, many of the processes are limited to machines that are available to gold contaminated process, i.e. evaporation of amorphous Si instead of LPCVD. The advantages of IC compatible fabrication process are more equipment options, automated and matured process available, etc.

One severe limitation is the lithography resolution. The ICL steppers can print down to 1\textmu m but is still not sufficient for PBGs at 1.53\textmu m. Fortunately, the device is fully scalable, and we can easily scale the design up to demonstrate the feasibility of fabrication. In this part, the fabrication of the first 2 layers of a PBG structure with a bandgap centered at 4.5 \textmu m was demonstrated with contact aligners for photolithography.

It should be noticed that the state-of-the-art photolithography steppers can print features around 0.25 \textmu m and in the near future, will very much possibly be extended to provide sufficient resolution and alignment precision for PBG structures operating at 1.53 \textmu m.

Beside the lithography, several difficulties arose during the fabrication of the three-dimensional photonic band gap structures. The first difficulty was the creation of the Si trenches with the correct geometry and straight sidewall profile. This problem was solved by using a Low Temperature Oxide (LTO) as a hard mask as opposed to a photoresist mask, which will result sloped side wall due to the photoresist erosion during RIE etching. The second difficulty was the creation of voids in the SiO\textsubscript{2} that was subsequently deposited into the Si trenches using low temperature oxide deposition (LTO). Through a combination of 0.5 \textmu m boron phosphide silicate glass (BPSG) along with 1.5 \textmu m of LTO, the Si trenches were completely filled with SiO\textsubscript{2} after the Chemical Mechanical Polishing (CMP) step. The third difficulty was to reproducibly creating proper alignment between the second layer Si trenches and the first layer suggests. And this can be alleviated using a contact aligner with Moire marks instead of the stepper. Also the non-uniformity of the chemical mechanical polishing leads to the potential application of oxygen ion implantation and wafer bonding. Figure 5.1 is a summary of the fabrication steps and corresponding SEM pictures.
5.1 OVERVIEW

Fabrication of 3-D Photonic Bandgap Structure

Figure 5-1: Major fabrication steps and corresponding SEM micrographs
First, poly-Si, Si\textsubscript{3}N\textsubscript{4}, and SiO\textsubscript{2} are deposited on p-prime Si wafers in consequence. Then photoresist is coated, exposed and developed. SiO\textsubscript{2} serves as a hard mask for the poly-Si etch to get better side-wall profile, while the Si\textsubscript{3}N\textsubscript{4} is used as etch stop for the CMP process and the subsequent poly-Si etch. After the etching, BPSG and LTO are deposited to fill in the trenches. After that, a CMP is applied to planarize the surface and make it ready for the second layer process. The second layer process is basically the same as the first layer but there is a half-period shift of the pattern. Theoretically, it is possible to continue this process and fabricate the whole structure.

5.2 Mask Design

In contrast to the direct writing method of electron beam lithography, the optical lithography requires a set of masks to duplicate the patterns to the photoresist. The masks have a thin layer of Cr deposited on a quartz plate and in certain area, the Cr is etched away so that the light can transmit through the mask to expose the photoresist. Because of the diffraction of the light, the features in the mask can not go down beyond the wavelength of the exposing light. The light source used in contact aligner is the Hg lamp with the emission in UV region ranged from 350 nm to 450 nm. In the contact aligner, the mask is in intimate contact with the photoresist, therefore the diffraction and non-collimation of the light can be minimized and yields the most faithful image transfer and best resolution. By hard vacuum contact, the features down to 0.6 \textmu m can be printed.

In this approach, instead of putting down the trench and holes at the same layer we first define the trenches in each layer, and in the final step, a set of holes will be aligned and drilled throughout all the layers using metal as the hard mask and CF\textsubscript{4}/O\textsubscript{2} as the etching gases.
5.2 MASK DESIGN

Fig. 5.2 shows the dimensions in the cross sectional view of the 3D PBG structure with bandgap centered at 4.5 μm. For 3-D PBG structures, there are two parameters of key importance in mask design: the trench width, \( w \) and the period of trenches, \( a \). Across the whole mask, \( l \) is fixed at 550μm. The three parameters \( w, a, \) and \( l \) are shown in the schematic of the mask (Fig. 5.3).

The macroscopic view of the layout of one unit cell is shown in Figure 5.4. The arrangement of 9 identical unit cells is shown in Figure 5.5. The width of the unit cell is 5.45mm and the length of the unit cell is 12.64mm. The separation between unit cells is 3mm.
Figure 5-4: The macroscopic view of the layout of one unit cell in the optical mask.
The introduction of an air defect in a perfect PBG crystal can lead to the creation of sharp resonant electromagnetic states. If the size of the defect is properly chosen, a localized state can appear in the gap. In this project, the defects are inserted in layer #5. The arrangement of defects is shown in Fig. 5.6. It should be noted that the whole box corresponds to one small box in Fig. 5.4.

In the mask design, three midgap frequencies 4.3µm, 4.5µm and 4.7µm and two material systems Si/air and Si/SiO₂/air are considered. Also, due to the variation of dimensions during fabrication, the size of defects \( r \) and the trench width \( w \) vary in the range of 90% to 110% of design size. All of the parameters that are varied in a unit cell are shown in Table 5.1, where \( w \) is the trench width, \( a \) is the trench period and \( r \) is the radius of defects. The orders of the parameters in table 5.1 are in correspondence with the boxes in Fig. 5.4.

---

**Figure 5-5: The arrangement of 9 unit cells.**
Table 5-1: The corresponding parameters of all the boxes in Figure 5.4
5.2 MASK DESIGN

The design of alignment marks is very important in this project. Three steps of alignment procedures are used:

(1) Using complementary alignment crosses shown in Figure 5.7, alignment to within 1.0 μm can be achieved;

(2) Using the coarse moire marks shown on the right side of Figure 5.8, alignment to within 0.3 μm can be achieved;

(3) The fine moire marks shown on the left side of Figure 5.8 can achieve alignment to within 0.1 μm.

It's worthy to discuss the moire marks. The moire alignment marks consist of gratings with pitches $p_1$ and $p_2$ side by side, but with $p_1$ on the substrate facing $p_2$ on the mask, and $p_2$ on the mask facing $p_1$ on the substrate. In this way, when the mask and substrate marks are imaged, interference fringe patterns (often called a moire pattern, or beat pattern) are formed, having a period $p$, which is given by $p = \frac{p_1 p_2}{|p_1 - p_2|}$. Figure 5.9 is one part of the first layer of moire marks. For the fine moire marks, in the first layer, the period of the left side is $p_1 = 2.0 \mu m$, and that of the right side is $p_2 = 1.9 \mu m$; In the second layer, the periods of the left side and right side are $p_2 = 1.9 \mu m$ and $p_1 = 2.0 \mu m$, respectively. Figure 4.8 is the composite of two layers of moire marks. A beat pattern is formed and the beat period is $p = \frac{p_1 p_2}{|p_1 - p_2|} = 38 \mu m$. Therefore fine moire marks provide a 20× extra magnification and

![Figure 5-6: The arrangement of defects.](image_url)
alignment to within 0.1\(\mu\)m is achievable. When doing alignment, the two beat patterns on both sides should align with each other.

Figure 5-7: Complementary alignment crosses. (a) is the pattern on 1\(^{st}\) layer and (b) is the pattern on 2\(^{nd}\) layer, and (c) is the aligned 1\(^{st}\) and 2\(^{nd}\) layer patterns.
Figure 5-8: Moire alignment marks. The right side is the coarse moire marks and the left side is the fine moire marks.
Figure 5-9: One part of one layer of moire marks. The period of the left side is $p_1=2.0\mu m$ and the period of the right side is $p_2=1.9\mu m$.

Figure 5-10: The composite of two layers of moire marks. The beat period is $38\mu m$. 
5.3 Fabrication Process and Results

We focus on first layer fabrication and alignment between subsequent layers. A process traveler documenting step-by-step process of each wafer set is attached in Appendix.
5.3.1 Define polysilicon trenches

Figure 5.11 is the process schematic of polysilicon trench creation.

5.3.1.1 Deposition of $\text{Si}_3\text{N}_4$, polysilicon and LTO

The fabrication starts with $p$-prime wafers with resistivity of 10-20 $\Omega\cdot\text{cm}$. Although electrical properties of Si wafers do not affect much of their optical properties, the prime wafers have more parallel and smooth surfaces and result in better planarization.

(1) RCA cleaning

Before any high temperature deposition of thin films on Si wafers, an RCA clean is performed in order to remove any ionic or organic contaminants. First the wafers are placed in a 5:1:1 $\text{H}_2\text{O}:\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ solution at 80°C for 10 minutes to remove organic contaminants. Then the wafers are placed in the first rinser to rinse off the organic clean solution (4 cycles automatically) and dipped in a dilute HF solution (50:1 $\text{H}_2\text{O}:\text{HF}$) for 15 seconds to remove the surface oxide. Thereafter, the wafers are rinsed again (4 cycles) and placed in an ionic clean solution of 6:1:1 $\text{H}_2\text{O}:\text{HCL}:\text{H}_2\text{O}_2$ at 80°C for 15 minutes. After that, the wafers are rinsed in the second rinser and finally, the wafers are spun dry in a spin rinser/dryer. The dried wafers will be transferred as soon as possible to high temperature tubes to avoid particle contamination.

(2) Deposition of polysilicon

The polysilicon is deposited by LPCVD in Tube A6 using recipe #150 (Table 5.2). The deposition temperature is 580°C. In this project, there are two material systems Si/air and Si/SiO$_2$/air, which require 1.35µm and 1.16µm of poly-Si, respectively. Since the deposition rate is about 31.6 Å/min, 1.16µm and 1.35µm of poly-Si require 6 hours 7 minutes and 7 hours 7 minutes, respectively. The deposition temperature is 580°C. The deposition reaction is generally given as:

$$\text{SiH}_4 \text{ (vapor)} \rightarrow \text{Si (solid)} + 2\text{H}_2 \text{ (gas)}$$

Some parameters are typical in polysilicon deposition. Silane is fed in three positions: front end, center and back end of the quartz reaction tube to increase the uniformity of deposition. Total gas flow of silane is 122 sccm. Pressure is about 0.250 - 0.260 torr. And
wafer spacing is 0.28 inch.

<table>
<thead>
<tr>
<th>Interval</th>
<th>Description</th>
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</tr>
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<tbody>
<tr>
<td>0</td>
<td>Idle</td>
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</tr>
<tr>
<td>1</td>
<td>Boat in</td>
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</tr>
<tr>
<td>2</td>
<td>Stabilize</td>
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</tr>
<tr>
<td>3-7</td>
<td>Pump and Purge</td>
<td>53</td>
</tr>
<tr>
<td>8</td>
<td>Deposit Poly-Si</td>
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</tr>
<tr>
<td>9-15</td>
<td>Pump and Purge</td>
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</tr>
<tr>
<td>16</td>
<td>Purge to Atmosphere</td>
<td>21</td>
</tr>
<tr>
<td>17</td>
<td>Boat out</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 5-2: LPCVD poly-Si deposition recipe #150.

The structure and properties of poly-Si depend on the deposition temperature. At temperatures below 580°C, the as-deposited film is essentially amorphous. At temperatures above 580°C, the deposited film is poly-crystalline, with a preferred orientation. It was found that as-deposited amorphous films tend to have smoother surfaces than do films grown at 600°C. The 580°C deposition temperature is chosen to achieve the desired results when Si is plasma-etched. Poly-crystalline Si has a larger grain size which would cause severe undercutting during the etching process. Another reason to choose 580°C is that poly-Si deposited at 580°C has better uniformity and lower residual stress. Since the PBG structure is very complicated (10 layers) and eventually, all of the SiO₂ will be etched away, to prohibit the collapse of the entire structure, smaller residual stress is highly desirable. Deposition at 560°C has slower deposition rates and requires too long deposition time which is not good for the equipment.

(3) Deposition of Si₃N₄

A thin layer of 300 Å Si₃N₄ is deposited by low-pressure chemical vapor deposition (LPCVD) in the Integrated Circuit Laboratory (ICL) of the Microsystems Technology Laboratory (MTL) at MIT. A batch of wafers are processed at the same time, and the deposition is performed in an automated furnace (Tube A5). The deposition recipe is #460 (Table 5.3). The deposition rate is about 27Å/min and the main deposition time is
11 minutes. Optical measurements showed a mean thickness of 29 nm and a standard deviation of 0.3 nm for 5 points around the center and 4 edge points on the wafer. This layer of Si₃N₄ is used as an etch stop for the CMP.

<table>
<thead>
<tr>
<th>Interval</th>
<th>Description</th>
<th>Time (min)</th>
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<td>Idle</td>
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</tr>
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<tr>
<td>3-7</td>
<td>Pump and Purge</td>
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</tr>
<tr>
<td>8</td>
<td>Deposit Si₃N₄</td>
<td>11</td>
</tr>
<tr>
<td>9-20</td>
<td>Pump and Purge</td>
<td>24.5</td>
</tr>
<tr>
<td>21</td>
<td>Purge to atmosphere</td>
<td>11</td>
</tr>
<tr>
<td>22</td>
<td>Boat out</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 5-3: LPCVD Si₃N₄ deposition recipe #460.

LPCVD Si₃N₄ is formed by reacting dichlorosilane (SiCl₂H₂) and ammonia (NH₃) at temperatures between 700°C-800°C according to the overall reaction:

\[
3 \text{SiCl}_2\text{H}_2 + 4 \text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6 \text{HCl} + 6 \text{H}_2
\]

Si₃N₄ depositions by LPCVD are controlled by a large number of deposition parameters including temperature, total pressure, reactant ratios, and temperature gradients in the reactor. In general, LPCVD Si₃N₄ films have a density of 2.9-3.1 g/cm³, and a dielectric constant of 6. Process parameters are shown in Table 5.4.

<table>
<thead>
<tr>
<th>ratio</th>
<th>NH₃:SiCl₂H₂ = 3:1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas Flows (typical Gas)</td>
<td>NH₃ = 150 sccm, SiCl₂H₂ = 50sccm</td>
</tr>
<tr>
<td>Pressure</td>
<td>0.380 - 0.420 Torr</td>
</tr>
<tr>
<td>Temperature</td>
<td>center = 780°C</td>
</tr>
</tbody>
</table>

Table 5-4: Process parameters for Si₃N₄ deposition.

(4) LTO deposition and reflow

The low temperature oxide layer acts as the hard mask for the plasma etching of Si. A
5.3 FABRICATION PROCESS AND RESULTS

2500Å layer of LTO is deposited by LPCVD. The deposition is performed in Tube A7 using recipe #462 (Table 5.5). Since the deposition rate is about 52 Å/min, a 2500Å deposition requires 48 minutes. The deposition temperature is 400°C and the gas flow rates are: 30 sccm N₂, 31 sccm O₂ and 38.5 sccm SiH₄.

<table>
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<tr>
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<td>Boat in</td>
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<tr>
<td>2</td>
<td>Stabilize</td>
<td>10</td>
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<td>3-8</td>
<td>Pump and Purge</td>
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<tr>
<td>9</td>
<td>Deposit LTO</td>
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<td>10-17</td>
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<tr>
<td>18</td>
<td>Purge to atmosphere</td>
<td>20</td>
</tr>
<tr>
<td>19</td>
<td>Boat out</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 5-5: LPCVD low temperature oxide (LTO) deposition recipe #462.

The reaction between silane and oxygen forms SiO₂ and hydrogen by a heterogeneous surface reaction. Homogeneous gas-phase nucleation also occurs, leading to small SiO₂ particles that form a white powder on the inner walls of the furnace tube. The deposition rate increases slowly as the temperature is increased between 310 and 450°C. LTO films exhibit lower densities than thermal SiO₂, and have an index of refraction of ~1.44. They also exhibit substantially higher etch rates in buffered hydrofluoric acid (BHF) solutions than thermal SiO₂.

LTO films are then annealed (reflow) in Tube B6 using recipe #280 in ICL. The reflow temperature is 925°C and the main time interval at 925 °C is 15 minutes. Subsequent heating of LTO films after deposition to temperatures between 700-1000°C causes densification. That is, this step causes the density of the material to increase from 2.1 g/cm³ to 2.2 g/cm³, the film thickness to decrease, and the etch rate in HF to decrease.

5.3.1.2 Photolithography

First, HMDS is coated on the samples to improve photoresist adhesion to the LTO
layer. Then Shipley 1808 positive photoresist is coated on the sample, and the coating
parameters are: (1) in coating step, the duration is 6 seconds and the spin speed is 250 rpm,
(2) in spreading step, the duration is 9 sec. and the speed is 750 rpm and (3) in spinning
step, the duration is 30s and the speed is 4500 rpm. The expected thickness of photoresist
is 7700Å. The coated wafers are then prebaked at 90°C for 30 minutes to remove the
solvents.

The pattern transfer is performed with Karl-Suss MA4 Aligner. Standard Operating
Procedures (SOP) can be found in the Technology Research Laboratories (TRL). Hard
vacuum contact and exposing parameters 2s expose-4s wait-15 cycles (at 6.0mW power)
are used. There is one thing should be noted that the number of cycles will change from
time to time, so always use testing wafers to achieve the most suitable cycle number at that
time.

The exposed wafers are placed in MF319 developer for 1 minute development. Then
they are rinsed in cascade rinser and blow-dried with N2 gun. After that, samples are
inspected under microscope to make sure the results are reasonable. A post exposure
baking at 120°C for 20 minutes will improve the resist profile and increase the resistance
of the photoresist to plasma etch.

The best exposure time is determined before the actual process wafers. Special patterns
are included on the mask to facilitate this task. In particular, the desired focus can be
determined by comparing the mask objects which appear as both dark field and bright field
patterns. For instance, the features in Figure 5.12 (a) should all have the same width if the
machine is in focus. To decide if a certain exposure time is satisfactory, one would look at
the array of squares as illustrated in Figure 5.12 (b). The coloration observed within the
squares provides a good indication of whether the photoresist has been exposed to the right
extent. Specifically, a pink coloration due to the photoresist will remain within the square
patterns that have not been sufficiently exposed. In addition, the squares provide a gauge
of the resolution limits in the lithography technique by determining the smallest squares
and square separation with the highest pattern fidelity.
5.3 FABRICATION PROCESS AND RESULTS

5.3.1.3 Dry etching LTO, wet etching Si₃N₄ and dry etching polysilicon

The following techniques are used to achieve desired results using plasma etches.

(1) Etch LTO in AME5000

AME5000 refers to the Applied Materials Precision 5000 etch tool in ICL. It is a load-locked, single wafer process platform and is usually classified as a MERIE (magnetically enhanced reactive ion etcher). The etch recipe is shown in Table 5.6. In the main etch step, the gas flow rates are 15 sccm of CF₄, 10sccm of CHF₃. The system pressure is set at 200mTorr and the RF power at 350Watts. The duration of main etch is 130 seconds and the etch rate is about 19 Å/sec. A moderate oxygen plasma etch is applied before the main etch to clear the residues of photoresist that may remain in the trenches due to the non-uniformity of the development or other unexpected situations.

<table>
<thead>
<tr>
<th>Step</th>
<th>Time (sec)</th>
<th>Pressure (mTorr)</th>
<th>Power (Watt)</th>
<th>Magnet Field (Gauss)</th>
<th>Gas Name and Flows</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Stability</td>
<td>10</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>O₂ (45sccm)</td>
</tr>
<tr>
<td>2. Descum</td>
<td>6</td>
<td>100</td>
<td>150</td>
<td>90</td>
<td>O₂ (45sccm)</td>
</tr>
</tbody>
</table>
### Process Recipe for LTO Etch

<table>
<thead>
<tr>
<th>Step</th>
<th>Temperature</th>
<th>Time</th>
<th>Gas Flow</th>
<th>Remarks</th>
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<tbody>
<tr>
<td>Photoresist</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Removal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wet etch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Si₃N₄</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dry etch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly-Si</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5-6: Process recipe for LTO etch.

(2) **Photoresist removal**

A special solution of 1:3 H₂O₂:H₂SO₄, called “Piranha” is used to strip photoresist. A 10-minute immersion in “Piranha” will oxidize and dissolve the photoresist (basically organic polymers) without etching the Si/SiO₂ structures. After that, the wafers are rinsed in the rinser (4 cycles) and spun dry in a spin rinser/dryer. A dry plasma photoresist remover, called asher, is available in ICL. However, for better removal of photoresist, wet piranha strip is preferred.

If the wafers are not processed for more than several hours, put them back to AME5000 and use the same recipe (5 seconds main etch time) to clear the thin layer of oxide.

(3) **Wet etch of Si₃N₄**

Wet etch the thin layer of Si₃N₄ using Transetch-N solution, which is a special reagent derived from orth-phosphoric acid and can selectively etch Si₃N₄. An etch time of 5 minutes provides reasonable over-etch for complete removal of Si₃N₄.

(4) **Dry etch of Poly-Si**

Poly-Si can be dry etched in chamber B of AME5000 and the etch recipe is shown in Table 5.7. In the main etch step, the gas flow contains Cl₂, HBr, and NF₃. Cl₂ selectively etches Si and does not touch oxide. NF₃ is a much fast etchant for Si than oxide. Moreover both of the etchant only reacts with Si when there is ion bombardment. So this combination provides very good selectivity of Si over SiO₂ as well as directional etching (straight sidewall profile). The etch rate of poly-Si is about 1.1μm/min, 1.16μm of poly-Si requires about 1 min. Adding 10 sec over-etch, the duration of main etch is set at 70 sec. The descum step is not included because the etch mask is oxide instead of photoresist.
5.3 FABRICATION PROCESS AND RESULTS

<table>
<thead>
<tr>
<th>Step</th>
<th>Time (sec)</th>
<th>Pressure (mTorr)</th>
<th>Power (Watt)</th>
<th>Magnet Field (Gauss)</th>
<th>Gas Name and Flows</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Stability</td>
<td>10</td>
<td>30</td>
<td>0</td>
<td>50</td>
<td>Cl₂ (20sccm) HBR(20sccm) NF₃ (10sccm)</td>
</tr>
<tr>
<td>2. Main Etch</td>
<td>70</td>
<td>30</td>
<td>350</td>
<td>50</td>
<td>Cl₂ (20sccm) HBR(20sccm) NF₃ (10sccm)</td>
</tr>
</tbody>
</table>

Table 5-7: Process recipe for poly-Si etch.

(5) BOE wet etch of LTO

Finally, LTO can be selectively removed by Buffered Hydrofluoric acid (BHF), which is also called Buffered Oxide Etchant (BOE). The removal rate is about 1000 Å to 1200 Å/min and 2500Å of LTO requires 2 min 30 sec.

The final result using the above methods is shown in Fig. 5.13. The bottom and sidewall of the trenches are reasonably smooth and within control for the opening a bandgap in PBG structures. The jar shape of the trench is due to the non-directional ion bombardment. Interestingly, this will relieve for some extent for the alignment of the second layer.

Figure 5.13: SEM micrographs of the cross-sectional view of poly-Si trenches
5.3.2 Poly-Si trench-filling and planarization

The schematic of the process in this section is shown in Fig. 5.14.

![Figure 5-13: Schematic of depositing SiO₂ and then using CMP to planarize the surface.](image)

5.3.2.1 Conformal oxide deposition to fill the poly-Si trenches

The conformal deposition for gap/trench filling has been discussed in chapter 4. Among the several ways that enable the gap filling are deposition of LTO, deposition of biased PECVD oxide, and deposition of BoroPhosphoSilicate Glass (BPSG)/low temperature oxide (LTO). The biased PECVD has been discussed and successfully implemented in chapter 4. And in this chapter we turn to another way of gap filling, BPSG deposition/reflow, which is more popular in current IC fabrication.

By adding a phosphorus dopant, typically in the form of phosphine, PH₃, and a boron dopant (e.g. B₂H₆) to the gas flow, the ternary oxide system B₂O₃ - P₂O₅ - SiO₂, borophosphosilicate glass (BPSG) is formed. BPSG is desirable for easy film coverage over abrupt steps in the substrate. Actually, the boron and phosphorus content in the glass composition can be increased within certain constraints to increase the flowability. One
thing should be noted that theoretically, following anisotropic etching, Si trenches have sharp upper corners that are difficult to refill. A second thermal flow (reflow) can round these sharp edges, leading to significantly improved coverage of the SiO$_2$. However, due to the equipment limitations, reflow in ICL generates a large amount of bubbles that completely destroys the structure for thick BPSG films. It has been shown that below $0.5\mu m$, the results are acceptable.

Since the BPSG reflow step requires thickness of less than $0.5\mu m$, BPSG reflow only will not be enough for fabrication of this structure. Instead a hybrid of BPSG and LTO is implemented to fill the trenches.

A $0.5\ \mu m$ borophosphosilicate glass (BPSG) is deposited at ICL in Tube A8 using recipe #780. Followed is the deposition of $1.5\ \mu m$ LTO in Tube A7 using recipe #462 with a 4 hour 48 minutes deposition time. The result is shown in Figure 5.15 (prior to CMP). The void is not a problem in this case, since the small hole is above the Si surface, which will be polished away by CMP.

![SEM micrograph](image)

Figure 5-14: SEM micrograph (cross-sectional view): $0.5\ \mu m$ BPSG/$1.5\mu m$ LTO SiO$_2$ deposited in Si trenches (Photo Courtesy of Xiaofeng Tang).
5.3.2.1 Chemical Mechanical Polishing (CMP) of silicon dioxide

CMP is the main planarization technique for IC industry to achieve planarized dielectric interfaces for multiple-layer interconnects. For a brief description of CMP, please refer to Chapter 3.

The CMP process was first carried out at Lincoln Labs and later was processed in ICL after the acquisition of a Strasbaugh polisher in MTL. Schematic and SEM of a single period 3-D PBG is shown in Figures 5.16 and 5.17, respectively.

Figure 5-15: Schematic of single period of Si/SiO\textsubscript{2}/Air PBG structure

Figure 5-16: Completed first layer of 3-D PBG structure (Photo Courtesy of Xiaofeng Tang)
5.3 FABRICATION PROCESS AND RESULTS

Ideally, CMP would exactly stop at the surface of the thin layer of Si$_3$N$_4$. Therefore, the desired thickness of the remaining LTO on the Si$_3$N$_4$ is 0, and the desired thickness of the LTO in the Si trenches is 9000 Å. However, there is about 5–10% non-uniformity within the wafer. In the last step of this project when all of the oxide is etched away to form the Si/air structure, the fact that LTO is still on top of Si$_3$N$_4$ could result in all of the patterns above the residual LTO layer removed by etching. Also variation of the remaining Si trench depth will affect the properties of photonic crystals.

We can solve these problems in the following ways: (1) Using a thinner layer of nitride to minimize leave less steps in the structure and 300Å Si$_3$N$_4$ is chosen as the etch stop of CMP. (2) A thicker layer of Si$_3$N$_4$ can be used. The thicker Si$_3$N$_4$ would act as a better etch stop of CMP, and cause less over-polishing (dishing effect) of the Si trenches. Then a wet etch of Si$_3$N$_4$ after the CMP will remove the Si$_3$N$_4$ as well as the oxide on top of Si$_3$N$_4$ (lift off effect). (3) The patterning area in the field can be reduced. Since the uniformity across a smaller area is acceptable, the masks for 3-D PBG patterns are created only on the center 1 inch × 2 inches.

5.3.3 Fabrication of layer 2

The schematic of process for fabrication of layer 2 is shown in Figure 5.18.

The second layer fabrication starts with the amorphous silicon deposition. A 0.9 μm thick layer of silicon is deposited with LPCVD in tube A6. Since the thickness is smaller and we can used lower temperature deposition to further reduce the stress without paying too much price on deposition time. Deposition temperature of 560 °C is chosen and the recipe is #705. The main deposition time is 6 hour 50 minutes and the deposition rate is calculated to be 21.5 Å/min. The subsequent deposition of Si$_3$N$_4$ and LTO are basically the same as in 5.3.1.1.

Photolithography is done with Carl Suss MA 6 contact aligners in TRL. A careful alignment procedure is carried out and achieved satisfactory alignment of second layer (Fig. 5.19).
FABRICATION OF 3D PBGS USING OPTICAL LITHOGRAPHY

Figure 5-17: Schematic of process for fabrication of layer 2.
5.3 FABRICATION PROCESS AND RESULTS

Figure 5-18: The successful alignment of complimentary cross, coarse and fine Moire mark alignment. Photograph was taken after the development of photoresist.

All the following process, e.g. dry tech of LTO and polysilicon and wet etch of Si$_3$N$_4$ are the same as in first layer process. The final result is shown in Fig. 5.20.
Figure 5-19: Completion of 2nd layer trenches. (a) is schematic and (b) is the SEM of cross-sectional view.
This process involves a number of complex equipments. To avoid the delay of process when a specific machine goes down, alternative processes are developed wherever possible. For example, PECVD oxide can be used for hard etching masks if LTO deposition tube is down. PECVD PSG or TEOS can be used for gap filling when BPSG tube is down. Also two set of piranha clean can be a substitute for the RCA cleaning.

5.4 Challenges and future developments

There are several limitations for this process. The major challenge is the alignment. The alignment was done very carefully by manually driving wafer chucks. This is very hard to control and not repeatable. Usually for such high alignment precision, automatic stage control by laser interferometers and/or piezo-electric controlled stages are required.

In the contact aligner, the masks and wafers are both rigid and for good resolution, a vacuum contact has to be applied to remove the gap between the mask and wafer. However during the vacuum step, a non-predictable and non-negligible shift between the mask and wafer occurs and ruins the alignment. There is no known method to compensate for the shift. The success of alignment depends on luck.

The Alignment scheme is not repeatable, and different alignment marks have to be printed for each layer. In another word, there is no “absolute” registration available. Moire mark is a good assist for alignment. However, during the alignment process, since the viewing angle is in parallel with the light path of microscope, the interference pattern is blurred due to the strong light from the microscope. In other alignment schemes of moire marks, e.g. IBBI, the moire pattern is viewed in an oblique angle with a CCD camera for better contrast and higher alignment accuracy.

These challenges could be resolved using the optical projection alignment with deep UV light (Deep UV stepper). The Deep UV stepper can provide the required resolution down to 0.4 μm. Actually the industry can print 0.25 μm lines with alignment within ± 50 nm (3 σ). Since the poly-Si is transparent at the wavelength the alignment mark detection is carried out, we can use the same alignment mark to be the absolute registration mark for all the layers, therefore minimize the alignment drift.
FABRICATION OF 3D PBGS USING OPTICAL LITHOGRAPHY
Chapter 6
Future Directions and Other Approaches

In the previous two chapters we demonstrated the successful fabrication of the first two layers of 3-D PBG structures with mid-gap wavelengths at 1.53 μm and 4.5 μm, respectively. Moreover, the first approach, using e-beam lithography and biased PECVD oxide gap filling, can be repeated to fabricate the seven layers that are required to open the complete 3-D bandgap. The IC compatible process, due to the difficulties in lithography and process control, will not be continued until the completion of the first approach.

Nevertheless, there are some other options on fabricating the designed structures. Two novel approaches of wafer bonding and film bonding will be discussed in the second part of this chapter.

6.1 Outlines of future work

6.1.1 Process control

The process control at sub-micro or nanometer length scales is a non-trivial task. It requires sophisticated metrological instruments to measure the structures and characterize the processes.

It is very important to control the critical dimensions of the structures to preserve the bandgap. Because the alignment errors have already decreased a lot on the process window, geometrical deviations have to be tightly controlled. We have been successful in controlling the lateral dimensions of the structures, and for the 3-D fabrication, it's important to extend the control to the third dimension. The vertical process control includes the
film thickness and etch-depth.

The film thickness usually is not a problem for CVD films. However, since we are using the electron beam evaporation for a-Si deposition, we may experience up to 10% process variation on the film thickness. Therefore it is important to set up test structures and monitor the film thickness. We propose to use a piece of Si wafer with 1000 Å oxide as substrate and to measure the evaporated Si film thickness using an ellipsometer. A moderate plasma etch can be used to etchback and get the desired thickness if the film is thicker than desired.

For the etch-depth control, one way is to do a careful timed-etch and the other is to use a layer of etchstop, which is another very thin layer of material that is not etched in the plasma for Si etch. The etching for the Si is slow and the etch-rate does not change much with time. Therefore a timed-etch of 12.5 minutes repetitively results in 420 nm trench depth. Using an etchstop layer will result in better morphology of the trench bottom and also improve the process uniformity. A candidate of etchstop layer for Si is silicon nitride. The etch selectivity of thermally grown silicon nitride: Si is around 1:8 for fluorine-based etching gases. Since thermal Si$_3$N$_4$ is not available, biased HDPECVD nitride will be used instead and the etching characteristics are expected to be similar to the thermal nitride [Singer, 1997 #42]. We can also tune the Si etch to improve the etch selectivity. It should be noted that adding nitride layers might result in stress build-up and adversely affect the optical properties of the structures.

Among the metrological instruments, atomic force microscopy (AFM) is an excellent one to measure the surface topography including the trench depth. However, many artifacts and equipment settings can affect its readings. An easy way to calibrate the AFM reading is ellipsometry. A set of grooves with different aspect ratios will be etched into an oxide layer on top of Si substrate. Care has to be taken to improve the selectivity to avoid overetch into Si. Since the oxide thickness can be precisely determined by the ellipsometer, the readings from AFM can be calibrated. A thickness similar to the device layer thickness will be applied, and the measurements against the aspect ratio will be addressed.
6.1 OUTLINES OF FUTURE WORK

In this section, I present the schematics of the projected fabrication steps for making the complete 7 layer structures. The first module (Fig. 6.1) is to put down the alignment marks for e-beam lithography for all the subsequent layers. As we can see in the following schematic, the alignment marks can be recycled and last for all the layers. The depth of focus of the e-beam is large enough for the topography difference of 2.5 µm for 7 layer of PBG structures. So the registration should be good for all 7 layers provides that there is no high temperature steps. This approach increases one alignment step which will introduces some deviations to the designed structures. However, the absolute registration marks will reduce the alignment drifts.

Figure 6-1: Schematic of the process for layering down alignment marks.

6.1.2 Projected process schematics
Fig. 6.2 is a revised process schematic of first layer fabrication for purpose of better etch depth control and uniformity using etchstop layers. Fig. 6.3 is the corresponding gap-filling and planarization processes. Fig. 6.4 is the schematic of the second layer fabrication
and Fig. 6.5 is the wafer level layout which includes device dies, sacrificial dies and registration features for e-beam alignment and exposure. Schematic of revised gap-filling and planarization processes.

Outline of the Process of Planarization

Figure 6-3: Schematic of the revised gap-filling and planarization processes
Figure 6-4: Schematic of the revised second layer fabrication with alignment.
6.2 PBG fabrication by wafer-bonding and membrane-bonding

The previous processes all involve the gap filling and etchback for planarization, which increase the processing complexity and take a lot of processing time. Moreover, these are sequential processes, and each layer has to go through the same processes one by one. A novel class of approaches, wafer bonding [38] [39], and membrane bonding can eliminate those steps, and the latter can even be applied to fabricate all the layers at one time and just assemble them together.

6.2.1 Wafer bonding

Wafer bonding was first developed for silicon-on-insulator (SOI) applications and recently
it has drawn more attention due to the advantages of SOI in deep sub-micron integrated circuits [40]. The silicon wafer bonding process consists of three basic steps: surface preparation, contacting, and annealing. The surface preparation step involves cleaning the mirror-smooth, flat surfaces of two wafers to form a hydrated surface. Following this preparation, the wafers are contacted in a clean environment by gently processing the two surfaces together at one point. The surfaces come into contact at this point and are bound by a surface attraction of the two hydrated surfaces. A contact wave is initiated at this point and sweeps across the wafer surfaces, bringing them into intimate contact over the entire surface. The exact origin of the attractive force is not universally agreed upon and may involve the bonds formed between –OH groups on the opposing surfaces. The final step in the bounding process is a high temperature anneal of the contacted pair at temperatures between 800-1200 °C, and this increases the bond strength by more than an order of magnitude.

In this project, some test processes were carried out on wafer-bonding technique to fabricate the 3-D PBG structures. The bonding was done with the EV-bonder in the Technology Research Laboratory (TRL) at MTL.

First I carried out the bonding with two prime blank Si wafers. A careful RCA cleaning was done right before the wafer bonding to remove the particle contaminates. The bonded pairs of wafers were imaged using infrared transmission. Figure 6-6(a) is one of the images and the four spots are the Newton rings caused by ~ 1 μm particles in between the bonded wafers.

Then two prime Si wafers with patterns etched into substrates were bonded together almost free of defects (Fig. 6-6 (b)). With a bit of luck, the cross sections (Fig. 6-7) showed that the trenches in two wafers were aligned (There was a slight rotation between two wafers and at some places the trenches happened to be aligned). The etching of trenches was not done with the optimized recipe and the sidewalls were sloped.
6.2 PBG FABRICATION BY WAFER-BONDING AND MEMBRANE-BONDING

Figure 6-6: IR images of bonded wafers, (a) has some particle contaminates, while (b) is almost defect free.

Figure 6-7: Cross section of the bonded prime wafers with satisfactory alignment.

Based on above results, a process schematic was conceived that appeared to be promising on fabricate the 3-D PBG structures using wafer-boding technology.
Proposal of Wafer Bonding for 3-D PBG Fabrication

Single crystal Si
Buried oxide
Substrate

Bonded
SOI wafer

Pattern
1st layer

Bond another
SOI wafer

Bonding
next layer

Align, pattern
2nd layer
alignment
setup in NSL

Fusion
Bonding

Wafer bonder
in TRL

Remove
Oxide

Thinning wafer

Figure 6-8: Schematic of the 3-D PBG fabrication using wafer bonding technology
6.2 PBG FABRICATION BY WAFER-BONDING AND MEMBRANE-BONDING

The advantage of this process is the excellent material properties of single crystal silicon and the smooth surfaces for the strong bonding. However, the SOI wafers are very expensive and cannot be used extensively for process development.

The surface morphology is critical for the success of wafer bonding and a root mean square (RMS) surface roughness of within 0.5 nm is usually required [41]. The prime Si wafers for VLSI fabrication and SOI wafers generally can meet the surface smoothness, while a CMP process is applied before bonding deposited films (e.g., BPSG, poly-Si).

Since the PBG structures do not require single crystal silicon as building blocks, we can take advantage of the amorphous Si because as deposited a-Si film is very smooth.

As a preliminary study for the process feasibility, we deposited 330 nm a-Si and then annealed in N\textsubscript{2} at 1200 °C for 1 hour. No visible crystallites growing from the a-Si layer was seen to degrade the smoothness.

![Image](image.png)

**Figure 6-9:** Amorphous silicon layer after 1200 °C, 1 hour anneal

Bonding between as deposited a-Si films were carried out without CMP and results were satisfactory (Fig. 6-10). A CMP prior to the bonding is planned to improve the bonding strength.
Figure 6-10: Bonding between as-deposited films. (a) is thermal oxide vs. a-Si grown on top of thermal oxide and (b) is bonding between two a-Si layers grown on thermal Si$_3$N$_4$. (Both wafer pairs went through 1200 °C, 1 hour anneal after bonding)

It should be pointed out that the bonding between small structures might be much weaker than between bulk wafers and extreme care must be taken to preserve the alignment
and bonding.

**Membrane Bonding**

![Diagram of membrane bonding process]

Alternative:

Free standing Si membrane

*Figure 6-11: Proposal for 3-D PBG fabrication using membrane bonding.*
6.2.2 Membrane bonding

Another advantage of bonding for PBG structure is that the bonding between layers does not have to be tight. In this point of view, another novel approach of membrane bonding was conceived. In fig. 6.11, first a thin membrane of oxide or nitride can be made by LPCVD deposition and selective KOH etch of the bulk of Si wafer. Then poly or amorphous Si can be e-beam evaporated or sputtered onto the membrane. This silicon layer is then patterned using the processes developed in Chapter 4. Two such kind of membrane are brought face-to-face, aligned and bond together by pressure or heat. The high temperature anneal may improve the bonding strength. Alternatively, free-standing p+ Si membranes can be used to minimize the stress and simplify the process. Since the PBG structures can tolerate the existence of materials that are much thinner than the wavelength of the light, a glue layer can be inserted to enhance the bonding between the membranes, as shown in Fig. 6.12. The glue layer can be Gold or Pb, which form alloys with Si and have low melting temperatures (eutectic bonding). After removing the substrate on one wafer, this process can be repeated to achieve multi-layer structures.

![Diagram](image)

Figure 6-12: Proposal for membrane bonding using glue layers.

A significant advantage of this process is that the membranes can be fabricated in a batch fashion and the fabrication only involves assembling (bonding) of membranes, thus
increase the yield and cycling time considerably.

Despite all the advantages, there are still many remain to be investigated (e.g. stress, particle contamination, and alignment) for the successful implementation of membrane bonding to 3-D PBG fabrication.
Chapter 7
Summary

This thesis deals with the fabrication of a novel class of three-dimensional Si/Air and Si/
SiO_2/Air PBG structures. Two approaches were investigated: one for demonstrating photonic bandgap at wavelength of 1.53 μm using electron-beam lithography and etchback planarization, and the other for high volume IC-compatible fabrication of devices operating at 4.5 μm using standard IC processes. First two layers of the seven layers required for verifying the 3-D photonic bandgap were fabricated for both approaches.

In the first approach, PBG structures were fabricated in small dies ranging from 75 μm^2 to 150 μm^2. Amorphous silicon was evaporated with electron-beam evaporator and patterned with SEBL. Features as small as 100 nm were defined and the proximity effects were corrected to result in correct geometry of the PBG pattern. Using a hard mask of Ni-Cr patterned with lift-off, we achieved straight side wall profile in Si trenches after RIE Si etch. Those trenches were subsequently filled with oxide using a high-density-plasma deposition tool. Planarization was achieved with a combination of physical sputtering, wet etch and isotropic dry etch. Special care was taken to stop the etchback at the top of Si veins. Using self-correlation, alignment between layers was successfully implemented with the average shift of 45 nm, which is sufficient for the PBG structures. This approach can be repeated to fabricate the seven layers that are required to open the complete 3-D bandgap.

The above processes were all carried out at low temperatures, which is highly desirable for the future integration of PBG structures to micro-electronic devices.
In the second approach, various configurations consisting of different trench dimensions have been built on standard 4" (100 cm) silicon wafers. The films were deposited with LPCVD tools and device dimensions approaching the limits of the photolithography have been attained. An LTO hard mask and Cl₂/NF₃/HBr plasma etch were used to obtain Si trenches with straight side walls at the desired dimensions. A combination of BPSG and LTO deposition were applied to conformally fill the trench and the planarization was achieved with CMP. Satisfactory alignment between layers could be obtained with complementary alignment crosses and Moire marks. Theoretically, these steps can be repeated for putting down more layers, but a deep UV stepper is required to overcome the lithography difficulty.

Two novel approaches of wafer bonding and membrane bonding were also discussed and some preliminary results showed the advantages.

Future directions will be concentrated on fabricating the PBG structures with defects incorporated and to verify the 3-D bandgap using the first approach. The success in fabrication two layers of the structure is critical to the completion of the final seven or more layers.

This project has been exciting and will enable a lot more exploration of the fascinating world of PBG structures. Photonic crystals provide various opportunities for the miniaturization of optical devices and will play a central role in the future photonic information technology.
Appendix

Process Traveller for IC-compatible process

Process Traveller
Sidewall etch and trench filling

Created: Feb. 7, 1997

lot: # 3dpbg1
Owner: Minghao Qi
login: mqi@mtl.mit.edu

Starting material: Silicon 4" diameter prime wafers. From MEMC Electronics materials, Inc. single sided polished wafers.

For the diffusion steps, 50 wafers will be processed each time. For other processes, 10 wafers will be a lot.

<table>
<thead>
<tr>
<th>Step #</th>
<th>Step Description</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>RCA clean all wafers</td>
<td># wafers: 48 + 2</td>
</tr>
<tr>
<td></td>
<td>If RCA is down, 2 piranha cleaning will be applied</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>Deposit 300 A Nitride</td>
<td># wafers: Sub lot 20 + 2</td>
</tr>
<tr>
<td></td>
<td>Recipe #460, 27 A/min, 11 min.</td>
<td></td>
</tr>
</tbody>
</table>
Plasma etchstop for poly, stress (~1 GPa)

3. LPCVD 1.3 um Poly
   Recipe #150, Temp: 560 °C (to minimize the stress)
   time=7 hours
   (Deposition rate=31.6 A/min)
   Total time: around 9 hours.

3.5 RCA cleaning in ICL if poly deposited
   in TRL

4. Deposit 300 A Nitride
   Recipe #460, 27 A/min, 11 min.
   Plasma etchstop for poly

5. Deposit 2500 A LTO as hard mask
   Recipe #462, Time=48 min.
   Rate = 52 A/min
   5.1 If LTO is down, PECVD could be used
   Deposited at 300 C.
   5.2 LTO down, projected to use BPSG without #
   doping.

6. Reflow of LTO
   Recipe #280, Temp=925 C

Starting from step 7, the wafers will be processed in 5 sublots each consists of 10 wafers.

The photo step will be processed in TRL using contact aligners.

7. HMDS
   # wafers: 10 + 1
8. Coating
Shipley 1808, manually spreaded with a beaker
Spots of non-uniformity were observed.


10. Align and exposure
Using KS Aligner 2 for multiple exposure
using the chucks of KS Aligner 1

11. Develop and inspect.

12. Postbake, 120 C, 20 min.

Bring wafer back to ICL

13. Dry etch Oxide
Tool: AME5000; Recipe: MING LTO
Rate: 30 A/min, total: 120 seconds.

14. Piranha stripe off the photoresist
The dummy wafer will go back to TRL photo

If the wafers are not processed for more than several hours,
put them back to AME5000 and use MING LTO recipe again (main etch: 5 seconds) to clear the thin layer of oxide

15. Wet Etch Nitride
Transetch -N, 175 C, 6 - 12 min.

16. Plasma Etch Poly
# wafers: 10
Tool: AME5000;
Recipe: MING-POLY
Rate ~120 A/s, time: 80 s

17. BOE etch Oxide # wafers: 10
time: around 1 min, 30 seconds

18. RCA cleaning # wafers: 10 + 1

19. Deposit 2 um BPSG # wafers: 10 + 1

Wafers are taken out of clean room for CMP

20. CMP # wafers: 10 + 1

After proper cleaning, wafers go back to ICL

21. Piranha cleaning # wafers: 10 + 1

22. Stripe off Nitride # wafers: 10 + 1

21. Poly deposition # wafers: 20 + 2
580 C amorphous
Bibliography


BIBLIOGRAPHY


[28] “Specification charts for a JEOL JBX-6000FS/SFE direct write electron beam lithography system,”.


