AN INVESTIGATION OF COMPOUND AMPLIFIER STAGES

by

ROBERT GRADY FULKS

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Certified by

Thesis Supervisor

Accepted by

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ABSTRACT

The use of two or more amplifying devices directly connected together to form a compound amplifier has been very limited even though the few examples in the literature have many outstanding features. An investigation of other compound configurations is made to determine their possible uses, their range of terminal characteristics and how they may be used advantageously in circuit design.

The possible compound amplifier configurations are derived and their characteristics determined from the characteristics of the individual devices in the compound. Using the characteristics of a small-signal transistor, the circuits are tabulated in a form which places in evidence some of their important properties and possible uses in circuit design.

A straightforward method of designing transistor circuits utilizing compound transistors is shown and examples of circuits using compound amplifiers are derived. These include six high impedance transistor circuits with values of input impedance as high as 100 megohms, a d-c regulator circuit using a power transistor, and a low output impedance circuit using a transistor and a vacuum tube. Experimental models of some of these circuits are shown to verify the techniques used.

Thesis Supervisor: Campbell L. Searle
Title: Assistant Professor of Electrical Engineering
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CHAPTER I
INTRODUCTION

One of the fundamental choices in the design of amplifiers is the choice of the configuration in which the available amplifying devices will be utilized. This problem has received widespread attention since the introduction of the transistor since its internal feedback and its easy interstage coupling permit a wide variety of terminal characteristics. Also, the need for properties which are not inherent in the individual devices, has led to new techniques which result in overall terminal characteristics which are vastly different from those of the device used.

One such technique is the application of the compound transistor, which is a combination of two or more transistors coupled together to form a composite device, which is used as a single element in the circuit.

Despite the fact that there are many possible ways in which two transistors may be interconnected, only a small number have been used to any extent. Failure to utilize some of these possible connections quite often results in inefficient use of the devices.

The purpose of this research is to investigate the properties of compound amplifier stages using two amplifying devices. The small signal transistor will be
used as a vehicle by which the many possible circuits can be compared and a number of applications will be given to demonstrate how the developed techniques can be utilized in a practical amplifier.
2.1. Derivation of the Possible Configurations

Vacuum tubes and transistors are fundamentally three terminal devices. Two such devices can be connected together in many ways to form a compound amplifier with three terminals. In the following discussion the transistor will be used as an example of the amplifying element and the resultant terminals of the compound amplifier will be designated correspondingly: base, emitter and collector.

The transistor is normally used singly in one of three basic configurations: the grounded emitter, the grounded base, and the grounded collector. These are shown in Figure 1. It is also possible to use these circuits in the reverse direction although this is not
usually done in circuits where power gain is desired. The interconnection of two such devices which result in a compound amplifier is shown in Figure 2. The terminals of the compound are arbitrarily designated as shown in the figure. Since either transistor (I or II) can be either of six configurations discussed above, there are $6 \times 6 = 36$ possible distinct compound amplifiers. This compound amplifier may be used with any one of its three terminals grounded. The resulting configuration will be designated: grounded emitter, grounded base, and grounded collector, respectively. The reverse of these cases need not be considered separately since they can be generated by the appropriate reversal of the individual transistors. Thus, there exist $36 \times 3 = 108$ possible configurations using two amplifying devices. Some of these are impractical for physical reasons and some are unstable. However a

* A circuit using a reverse stage will be shown.
number of new, useful compound configurations can be found by a systematical investigation of the characteristics of each of these 108 configurations.

2.2. General Analysis of the Compound Circuits

In the following analysis, the individual transistors will be assumed to be operating in a linear portion of their characteristics. The transistor can then be considered as a linear, two terminal pair device and can be described by two linear equations relating its terminal voltages and currents. These equations involve four parameters which are characteristic of the device and completely describe its terminal behavior. The analysis will be further limited to the low frequency operation where the four parameters are constants.

A particularly useful set of parameters for describing the behavior of transistors is the "hybred" set which is defined as follows:

\[
\begin{align*}
\dot{z}_1 &= h_{i1} \dot{x}_1 + h_{i2} z_2 \\
\dot{z}_2 &= h_{x1} \dot{x}_1 + h_{x2} z_2 \\
\Delta h &= h_{n1} h_{n2} - h_{n1} h_{n2} 
\end{align*}
\]

* Superscripts refer to numbered references in the bibliography.
We shall see that the use of these "h" parameters also allows such characteristics as voltage gain, input impedance, and output impedance to be written in a convenient form.

When two such devices are cascaded, as in the grounded emitter form of the compound transistor as defined above, the overall terminal characteristics can also be described by "h" parameters. The equations for the parameters of the compound device in terms of those of the individual devices in cascade are shown in Figure 4. In this

\[
\begin{align*}
\frac{h_{11}}{1 + h_{22} h_{11}'} & = h_{11}' & h_{12} & = h_{12}' \frac{h_{12} h_{12}'}{1 + h_{22} h_{11}'} \\
\frac{h_{21}}{1 + h_{22} h_{11}'} & = h_{21}' & h_{22} & = h_{22}' \frac{h_{22} h_{22}'}{1 + h_{22} h_{11}'}
\end{align*}
\]

Figure 4. Two Stages in Cascade.

way the "h" parameters of a compound transistor in the grounded emitter configuration can be calculated from the parameters of the individual transistors.

The parameters for the grounded emitter case can then be used to determine the parameters for the grounded base and grounded collector configurations. It is also convenient to calculate the determinant of the "h" param-
eter matrix for each of the three orientations. These equations are summarized in Figure 5.

\[
\begin{align*}
\Delta h^a &= h_{11} - h_{12} h_{22}^{-1} \\
\Delta h^b &= h_{11} - h_{13} h_{33}^{-1} \\
\Delta h^c &= h_{11} - h_{12} h_{22}^{-1} + h_{13} h_{33}^{-1}
\end{align*}
\]

Figure 5. Grounded Base and Grounded Collector Parameters in terms of Grounded Emitter Parameters.

Since the 108 circuits contain every possible compound amplifier involving two transistors, half of these
can be derived from the other half by simply interchanging input and output terminals. The "h" parameters for a device reversed in this way can be written in terms of the parameters of the device itself:

\[
\begin{align*}
\text{h}_e^r &= \frac{\text{h}_{11}}{\Delta h} \\
\text{h}_{12}^r &= -\frac{\text{h}_{21}}{\Delta h} \\
\text{h}_2^r &= \frac{-\text{h}_{22}}{\Delta h} \\
\text{h}^r &= \frac{\text{h}_{11} \times \text{h}_{22}}{\Delta h}
\end{align*}
\]

The reverse "h" parameters will also be useful in tabulating other properties of the device.

Using equations 2.2, 2.3 and 2.4 it is now possible to calculate the parameters of the compound transistors in terms of the parameters of the transistors making up the compound.

2.3. **Conditions for Stability**

The criteria which must be satisfied for a compound amplifier to be stable may be derived in terms of "h" parameters from those given in the literature for a general two terminal pair device. Llewellyn has shown that for such an active, linear, two terminal pair device to be stable the following inequalities

* See Appendix III for derivation.
must be satisfied:

\[ R_{11} > 0 \quad \Delta R > 0 \]

\[ R_{22} > 0 \]

where

\[ \Delta = R_{11} x_1 + R_{12} x_2 \quad \Delta R = R_{11} R_{21} - R_{12} R_{21} \]

From these expressions we can derive the corresponding criteria involving "h" parameters.

\[ h_{11} > 0 \quad h_{12} > 0 \quad \Delta h > 0 \]

A number of compound circuits exhibit positive feedback around the interconnecting loop and will not satisfy these criteria.

* See Appendix III for derivation.
3.1. **Properties of the Compound Amplifiers**

Some of the properties of an amplifier stage which are important in circuit design are voltage and current gain, input impedance, and output impedance. These properties are generally functions of the external source and load impedances which are connected to the stage. This can be seen by examining the expressions for these quantities. In the second column of Table I, equations for some of these quantities are given in terms of the "h" parameters of the device and the corresponding external impedance (or admittance). The third column lists the resulting expression if the external impedance (or admittance) is made zero and the fourth column lists...

### Table I

<table>
<thead>
<tr>
<th>Definition</th>
<th>Exact Equation</th>
<th>$Y_L \rightarrow 0$</th>
<th>$Z_1 \rightarrow 0$</th>
<th>$Y_L \rightarrow \infty$</th>
<th>$Z_2 \rightarrow \infty$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Admittance $Y_i$</td>
<td>$\frac{h_{21} + Y_i}{\Delta h + h_\omega Y_i}$</td>
<td>$\frac{h_{21}}{\Delta h}$</td>
<td>$1$</td>
<td>$h_\omega$</td>
<td></td>
</tr>
<tr>
<td>Reverse Current Gain</td>
<td>$\frac{-h_\omega}{\Delta h + h_\omega Z_3}$</td>
<td>$-h_\omega$</td>
<td>$0$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Gain $G_V$</td>
<td>$\frac{-h_{21}}{\Delta h + h_\omega Y_i}$</td>
<td>$-h_{21}$</td>
<td>$0$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Impedance $Z_o$</td>
<td>$\frac{h_{11} + Z_3}{\Delta h + h_{22} Z_2}$</td>
<td>$\frac{h_{11}}{\Delta h}$</td>
<td>$1$</td>
<td>$h_{22}$</td>
<td></td>
</tr>
</tbody>
</table>

$Y_L$ = load admittance

$Z_i$ = source impedance
the expression if the external impedance (or admittance) is allowed to become very large. From the nature of the expressions we can see that for any external impedance (or admittance) between zero and infinity the magnitude of each expression must be between the values given in the third and fourth columns of the table. For example, the magnitude of the voltage gain must be greater than zero but less than $\frac{-h_{11}}{\Delta h}$ for any value of load admittance. The limits in the table express the range of capabilities of the particular device and it is, therefore, desirable to know these limits for each of the compound amplifiers under consideration in any application.

One of the limits is either zero or the reciprocal of one of the "h" parameters. The other limit is the quotient of one of the "h" parameters and the determinant of the "h" matrix of the device. This quotient is, however, also one of the "h" parameters of the device with its terminals reversed, as a re-examination of equation 2.4 will show. In the above example, the maximum voltage gain, $\frac{-h_{11}}{\Delta h}$, is actually the value of "h$_{12}$" of the reversed device. Therefore, if each of the compound stages and its reverse are considered as a pair, the eight parameters for the two devices will give the limits on the possible values of many of the important characteristics of the compound transistor. This fact allows the tabulation of the "h" parameters of the compound transistors in a
form which shows the maximum capabilities of each device when used in circuit application.

3.2 Method of Tabulation

Having established the necessary relations among the "h" parameters of the compound transistor, we may now use these expressions to calculate the parameters of the circuits derived earlier. These parameters have been calculated using a "typical" small signal transistor in both positions of the compound stage. The values used are those used by Hunter and Hermanson and seem average for currently available devices.

TYPICAL SMALL SIGNAL TRANSISTOR "h" PARAMETERS

\[
\begin{align*}
    h_{11} &= 2000 \text{ ohms} \\
    h_{12} &= 600 \times 10^{-6} \\
    h_{21} &= 50 \\
    h_{22} &= 25 \times 10^{-6} \text{ mhos} \\
    h &= .02
\end{align*}
\]

The parameters for the 108 compound transistors are tabulated in Appendix II. They are separated into three main groups. The first group includes those stable compound stages which are derived from using both transistors in the direction of greatest power gain. These circuits, correspondingly, can provide the highest compound power gain and are those which will be used in most cases where amplification is desired.

In Group 3 are the twelve circuits which use a
transistor in its forward direction cascaded, as in the grounded emitter configuration of the compound, with a transistor in the reverse direction. In this case the reversed transistor usually does nothing but provide signal attenuation. The grounded base and grounded collector configurations may, however, have useful characteristics. These circuits are listed separately in Group 2 of the tabulation. While the power gain of this last group is not great, they may find applications in circuits where this is not a determining factor.

Also included in Group 3 are the twelve circuits which have negative "h" matrix determinants, which may be unstable under certain terminations. Bahrs has shown that these circuits may be stabilized by a suitable choice of terminating impedances. Similar circuits have been used by Linville, Larky and others as negative impedance converters in active filter circuits.

Also listed in Group 3 are six circuits which have an "h" matrix determinant of unity. The circuits are symmetrical and are, therefore, the reverse of themselves.

In the tabulation, the a-c circuit of the compound transistor is shown at the top of each column with the value of its "h" matrix determinant and an identification number. The reverse circuit is shown at the bottom of the column. The directions of forward and reverse were chosen to correspond with the physical properties of the
individual transistors where this was possible. The forward direction was defined as the case where the input terminal was the base or emitter of a transistor and the output terminal was the emitter or collector.

The eight parameters of the two devices are shown in the center of the column in the following order:

\[ h_{11} = \text{Input impedance with the output short circuited.} \]
\[ h_{12} = \text{Reverse voltage transfer ratio with the input open circuited.} \]
\[ h_{21} = \text{Forward current gain with output short circuited. This is the maximum current gain.} \]
\[ h_{22} = \text{Output admittance with the input open circuited.} \]
\[ Y_{10} = \text{Input admittance with output open circuited.} \]
\[ G_{rs} = \text{Reverse current gain with input short circuited.} \]
\[ \mu = \text{Voltage gain with output open circuited.} \]
\[ Z_{os} = \text{Output impedance with the input short circuited.} \]

The quantities can be read down the left side for the forward case and up the right side for the reverse case.

Due to the importance of the determinant of the "h" matrix in the formulas listed previously, the circuits in each section have been listed in approximate order of decreasing magnitude of this quantity. It may be noted that the value of this determinant varies over nine orders of magnitude in the circuits listed. We will see that this quantity may be used to indicate some of the
possible uses of these compound amplifiers.

3.3. **The Range of Characteristics Available.**

The approximate limits of the range of characteristics which are available with a single transistor in any of its three configurations are well known and are shown below for our typical transistor:

<table>
<thead>
<tr>
<th></th>
<th>Maximum</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input &amp; output Impedance</td>
<td>2 megohms</td>
<td>.8 Ω</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>Current Gain</td>
<td>50</td>
<td>0</td>
</tr>
</tbody>
</table>

It is also well known that additional gain can be used to extend these limits if appropriate feedback is applied. We would expect that the addition, in some way, of a second transistor with a current gain of 50 could extend the above limits by a factor of 50. This is indeed the case as we can see from an examination of the corresponding limits for two transistor compounds as obtained from the tabulation:

<table>
<thead>
<tr>
<th></th>
<th>Maximum</th>
<th>Minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input &amp; Output Impedance</td>
<td>100 megohms</td>
<td>.8 Ω</td>
</tr>
<tr>
<td>Voltage Gain</td>
<td>50,000</td>
<td>0</td>
</tr>
<tr>
<td>Current Gain</td>
<td>2500</td>
<td>0</td>
</tr>
</tbody>
</table>
With the extension to three or more transistors we would expect further changes by the same factor. It is usually difficult to synthesize a circuit incorporating a second transistor to realize the theoretical limits of possible characteristics, especially when two or more characteristics are desired simultaneously. By tabulating the possible configurations of two transistors the choice of the possible circuits for any particular application is simplified. We will also see that the extension to three or more transistors follows in a straightforward manner.
CHAPTER IV
DEVELOPMENT OF CIRCUITS USING COMPOUND TRANSISTORS

In the following section a number of circuits using compound transistors will be developed. The parameters which were derived in the preceding section will be used to predict the general characteristics of the circuits. In some cases experimental models of these circuits will be constructed and their performance measured. Since the previous analysis has neglected the effect of bias resistors and varying transistor parameters, the measured characteristics will not be expected to agree with the predicted values within more than an order of magnitude. Better accuracy could be obtained from accurate measurements of the devices used but the additional complication is usually not warranted.

4.1. **Derivation of High Impedance Circuits**

As a first example of the use of compound transistors, let us consider a common problem in the use of transistors; that of obtaining a high input impedance. The inherent low input impedance of transistors has led to the development of a number of circuits which result in input impedances much higher than that of the single transistor. Many of these circuits can actually be called compound stages although they are not usually drawn or easily
recognized as such.

From Table I we recall that the input admittance in terms of "h" parameters is given by:

\[ Y_\text{L} = \frac{h_{LL} + Y_L}{\Delta h + h_n Y_L} \]  \hspace{1cm} (4.1)

The limits on the magnitude of this admittance are:

a) \[ \frac{1}{h_{nn}} \quad \text{as} \quad Y_L \to \infty \]  \hspace{1cm} (4.2)

b) \[ \frac{h_{nn}}{\Delta h} \quad \text{as} \quad Y_L \to 0 \]

If \( Y_L > h_{nn} \), equation 4.1 may be written as:

\[ Y_\text{L} = \frac{Y_L}{\Delta h} \]  \hspace{1cm} (4.3)

Re-writing this in terms of input impedance we obtain the following equation:

\[ Z_\text{L} = \Delta h \overline{Z}_L \]  \hspace{1cm} (4.4)

Under these conditions the input impedance is given by the load impedance multiplied by the "h" matrix determinant and the amplifier is an impedance multiplying device. For high input impedance the magnitude of this determinant should be large.

The minimum input admittance is given by equation 4.2-b and should be small. This is listed on the fifth row of the tables. Let us also require that the open circuit voltage gain, should not be much less than one for power gain and reasons that will be explained below. This is listed in the seventh row of the tables. From the tabulation we see that only the first six circuits...
meet these requirements. Let us consider the capabilities of each briefly and then examine experimental realizations of some of these circuits.

The first circuit has a maximum input impedance of \( \frac{1}{Z_{in}} = 2 \) megohms. This can be realized if the load impedance is greater than \( \frac{1}{Z_{out}} = 800 \Omega \). The voltage gain, \( \mu \), is very close to unity, as is common in all these circuits. This circuit was developed by Darlington and has received a great deal of attention in the literature.

The second circuit also has a maximum input impedance of 2 megohms when the load impedance is greater than 800 \( \Omega \) and a very low output impedance (\( Z_{os} \)) when driven from a zero source impedance. This circuit is actually the transistor equivalent of the White Cathode Follower. It has also been used by Waldhauer and in a slightly different form by Middlebrook and Mead.

The third circuit has a maximum input impedance of 100 megohms when the load impedance is greater than 40K\( \Omega \), for lower load impedance the input impedance should be approximately \( \Delta \lambda = 2400 \) times the load impedance. This circuit has been used by Stampfl and Hanel, and Pearlman.

The fourth circuit also has a maximum input impedance of 100 megohms but only when loaded with an impedance greater than 2 megohms. For lower load impedances the
input impedance is 50 times the load impedance. This circuit was also used by Stampfl and Hanel who used a transformer coupled to the load to realize the necessarily high load impedance.

The fifth circuit is unusual in that the input terminal is the emitter of one of the transistors. The input impedance can be as high as 2 megohms if the load is greater than $40 \, \text{k}\Omega$. For lower values of load impedance the input impedance is approximately 50 times the load. The outstanding features of this circuit are its very low output impedance and gain which is extremely close to unity. The circuit may be useful in direct coupled circuits where the emitter input terminal can be used to advantage and in active filter circuits since its extremely stable gain and low output impedance render the resultant filter characteristics independent of transistor parameters.

The sixth circuit is also capable of a 2 megohm input impedance and can have a gain very close to unity. However, since the output impedance is relatively high ($40\, \text{ohm}$) this gain would be difficult to obtain due to the loading effect of any terminating impedance. It has the advantage that the same d-c current flows through both transistors. This usually permits better stabilization of the operating point.

There seems to be no published account of the use
of either of these last two circuits. Their discovery provides two new high impedance circuits which may be useful in many applications.

4.2 Experimental High Impedance Circuits

The primary difficulty in realizing compound circuits physically is that of biasing the transistors in their linear operating region without effecting the a-c equivalent circuit. In the case of high input impedance circuits the input cannot be biased with resistors directly to ground. A technique which has proved very useful is that of "bootstrapping". This is the procedure of connecting the bias resistors, $R_b$, between the point to be biased and a low impedance point of approximately the same a-c potential, as in Figure 6 below:

Since the a-c current, $i_b$, in the bias resistor $R_b$ is equal to the voltage across it $(v_2 - (1 - \delta)v_1)$ divided by its
resistance,
\[ I_b = \frac{\delta I_i}{R_b} \]  
(4.5)
the input current is:
\[ I_i = \frac{\alpha_i}{R} + \frac{\delta I_i}{R_b} \]  
(4.6)
and the input impedance is, therefore:
\[ Z_i = \frac{\alpha_i}{\lambda_i} = \frac{1}{\frac{1}{R_i} + \frac{\delta}{R_b}} \]  
(4.7)
If \( \delta \) is very small, the bias resistor has no effect on
the input impedance. In each of these six circuits
considered above, the gain is very close to unity and the
input bias resistors can be "bootstrapped" to the output.
This is usually done with large capacitors although
zener diodes or batteries could be used in some cases
if high d-c impedance is required. Figure 7 shows
circuit diagrams for utilizing compound transistors
2, 3, and 5, respectively. The values of input imped-
ance, output impedance, and voltage gain agree reason-
ably well with the predicted values.

* The physical area, such as shields, near this high
impedance circuit can be also connected to this point.
The stray capacitance to these areas is then multiplied
by \( \delta \). This procedure, sometimes called "guarding" or
"double shielding" can reduce the effective input
capacitance to a very small value even when long
shielded cables are used.

** See Appendix III for method of measurement of
these values.
\[ R_\mu = 12.2 \text{ MEG.} \]
\[ R_o = 2.6 \ \Omega \]
\[ G_v = 1 - \frac{1}{1860} \]

(2)

\[ R_i = 42.7 \text{ MEG.} \]
\[ R_o = 90.5 \ \Omega \]
\[ G_v = 1 - \frac{1}{108} \]

(3)

\[ R_\kappa = 1.38 \text{ MEG.} \]
\[ R_o = 11.4 \ \Omega \]
\[ G_v = 1 - \frac{1}{10^{10}} \]

(5)
4.3. **Extension to Three Transistors**

Any compound amplifier can be extended to include three amplifying devices if the requirements for the circuit cannot be met with two such devices. This fact is perhaps most easily shown by an example. Consider the problem of designing a transistor amplifier with a very low output impedance. The lowest impedance available with two transistors was 0.8 ohms, (circuits 2 and 5). To achieve a still lower value we must use a third transistor. This can be added by replacing one of the transistors in the previous compound transistor with a new compound. The compound circuit number 2 is shown in Figure 8a. If the lower transistor is replaced by a general "h" parameter box the resulting circuit is that shown in Figure 8b. We can now make a number of approximations to simplify the analysis. Since \( h_{22} \) is shunting the very low output impedance it can be neglected.

![Figure 8](image-url)

**Figure 8.** Replacing one Transistor with a compound.
h₁₂ can also be neglected since its effect is to partially "bootstrap" the impedance from the collector to base of the upper transistor, raising the overall input impedance. A straightforward circuit analysis of this simplified circuit leads to the following expression for the overall output impedance.

\[ Z_o \approx \frac{(Z_s + h_{21a})(1 + h_{21b}h_{12b})}{h_{11a}h_{21b}} \] (4.8)

Where "a" refers to the upper transistor and "b" to the lower compound. Z_s is the source impedance.

For a low output impedance, h₁₁b should be less than \( \frac{1}{h_{21b}} = 4\Omega \) and h₂₁b should be positive and very large. The only compound transistor which satisfies these requirements is circuit 8 with values:

- \( h_{11b} = 2000 \) ohms
- \( h_{21b} = 2400 \) ohms

Evaluating the above expression using these values results in an expected output impedance of approximately 0.017 ohms with zero source impedance. An experimental circuit using this three transistor compound is shown in Figure 9. The measured output impedance was 0.065 ohms.
Figure 9. Low Output Impedance
Three Transistor Compound Amplifier.

The procedure of replacing one transistor by a compound is limited in two respects; first, since the single transistor in the grounded emitter configuration has a positive current gain the replacing compound must also have a positive current gain. However, the other transistor must contribute a negative current gain so that the total loop gain will remain negative. Therefore, this limitation can be removed by attempting to replace the second transistor by a compound instead of the first. In this way both possibilities may be explored.

The second limitation is that of instability. In
the preceding example the overall loop gain for three transistors was approximately $50^3 = 125000$. Phase shift at high and low frequencies becomes a serious problem. The direct coupling of transistors is very helpful in keeping the circuit stable. It is usually necessary to use high frequency transistors and control the phase shift with auxiliary networks. In the circuit of Figure 9, oscillations at 5 megacycles were stopped by the use of the 1000 $\mu$F capacitor across the load resistor of the second stage.

These examples would indicate that three transistors is the practical limit of this procedure without using special coupling networks. The possibility exists of using two separate feedback loops; one, for example, to raise the input impedance, and one to lower the output impedance. This would require a more thorough investigation than could be undertaken here.

4.4. **A Direct-Current Regulator Circuit**

As a second example let us consider the design of a d-c transistor voltage regulator circuit, which will show one of the uses of "reverse" compound transistors.

In most regulator circuits, at least one transistor is a power transistor with very different characteristics than those used in our calculations. However, the relative merit of each configuration using a power transistor
will be related to that of the same configuration using small signal transistors, because each compound configuration utilizes the available loop gain to change one or more of the overall characteristics of the device. The general characteristics are more a property of the configuration than of the individual devices. We may derive circuits which provide the necessary general characteristics using small signal transistors and then substitute other amplifying devices with a reasonable assurance that they will function as planned. Experimental models can then be used to choose the best circuit for a particular requirement. This procedure especially useful with the compound transistors with large power gain such as the circuit of Group 1 of the tabulation.

The basic circuit of the d-c regulator is shown in Figure 10. The input is direct current plus some a-c ripple in most cases. The load generally can vary somewhat. The object is to filter out the a-c signal and
render the output d-c voltage independent of load changes. Therefore, the a-c gain and output impedance should be as low as possible. There are no other a-c restrictions. The source impedance is usually small and the load much greater than the output impedance so the circuits to be considered are those with low $\beta$ and $Z_{os}$. Circuits (89) and (91) are the only two which have these properties. These are shown in Figure 11.

![Figure 11](attachment:figure11.png)

Figure 11. Possible d-c Regulator Circuits

Both of these circuits are suitable for the d-c requirements since the load current can flow as the collector or emitter current of one of the transistors.

Circuit (89) has a very low a-c voltage gain but would be difficult to bias properly. Circuit (91) is correctly biased as shown and the reference voltage may be placed in the base of the lower transistor since the d-c voltage drop from its base to emitter is very small. An experimental circuit using a power transistor is shown in Figure 12 using circuit (91). The measured gain was
approximately \(1.8 \times 10^{-3}\) at 10 volts input and no change in output voltage was noticed over the ranges of input and load conditions shown in the figure.

![Experimental d-c Regulator Circuit](image)

**Figure 12. Experimental d-c Regulator Circuit**

In this circuit transistor "I" could be replaced by a compound as in the previous case, if more stringent requirements must be met.

4.5 **A Vacuum Tube-Transistor Compound Amplifier**

Vacuum tubes and transistors are not usually used together since their physical requirements are quite different. However, the addition of a single transistor to an existing vacuum tube circuit is very simple and may result in a desirable change in characteristics.

As an example, let us consider the addition of a transistor to a standard vacuum tube cathode follower for the purpose of reducing the overall output impedance. The cathode follower using a triode is shown in Figure 13. To avoid the necessity of any physical change in wiring
we must choose a compound stage in which the cathode follower may be used directly. Circuits 1, 3, 5, and 6 satisfy this requirement. Of these circuits, 5 has the lowest output impedance so it will be chosen for the compound. Circuit 5 and an experimental transistor-triode realization are shown in Figure 14.

The characteristics of the circuit are listed below:

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<td>Voltage Gain</td>
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The simple addition of one transistor and one resistor has reduced the output impedance by a factor of 250. The grid to cathode voltage of the triode is of such a magnitude to operate the transistor satisfactorily.

We see that the physical problems encountered are not as bad as they may seem and that the transistor may be used advantageously in conjunction with vacuum tube circuitry.

4.6. Other Properties of Compound Amplifiers

Although we have only considered the low frequency, linear operation of compound amplifiers there are many other properties which may be of interest. Some of the circuits have been found to have low distortion characteristics and low noise properties. For example, Boxall has shown that base current feedback, as in circuit (17), can greatly reduce non-linear distortion in power transistors. Shea has shown similar results using the Darlington compound transistor circuit (15). The noise figure of this compound transistor is also said to be quite low.

Two dissimilar devices are compounded, the combination quite often retains some of the desirable characteristics of each. Faran has used circuit (8), see Figure 15, with NPN small-signal transistor in position "I" and PNP power transistor in position "II". The compound has the physical characteristics of a high gain, NPN power transistor.
This is useful since there are currently more PNP power transistors available at a lower cost than NPN type.

As another example, consider the frequency response of circuit (12), shown in Figure 16, in the case where transistor "I" is a small-signal transistor and "II" is a power transistor. If the alpha cut-off frequency of "I" is much greater than that of "II", as it easily can be, then the compound transistor will have a current gain of approximately 50 up to the alpha cut-off frequency of the power transistor. This frequency is 50 times higher than that of the power transistor alone when used in a
configuration of the same gain. Similar relations may also exist for other compound circuits. These circuits would be very useful since poor high frequency response is one of the limitations of most current power transistors.

4.7. Conclusions

The preceding analysis has disclosed many new compound amplifier configurations with a wide range of terminal characteristics. The circuits have been tabulated in a manner which facilitates their use in circuit design. Although the characteristics have been calculated only for small-signal transistors, the tabulation may be used in more general cases by seeing how the available loop gain of the devices is used to change the overall terminal characteristics. The examples shown indicate that this extension is valid and that many useful properties can be obtained by combining the individual characteristics of different devices.

The method of designing circuits using compound amplifiers which is presented here has an important advantage. Every circuit which has the desired properties can easily be considered with very few calculations and the most efficient use of the available device characteristics can be obtained.
BIBLIOGRAPHY


19. The circuit shown was developed by other methods by H. P. Hall, General Radio Company, June 1958, and reported to the author by private communication.


APPENDIX I
SUMMARY OF FORMULAS

A.) Definition of "h" parameters of linear network

\[ a_1 = h_{11} a_1 + h_{12} a_2 \]
\[ a_2 = h_{21} a_1 + h_{22} a_2 \]

B.) Useful terminal characteristics in terms of values listed in tabulation of circuits.

- **Input Impedance**
  \[ Z_i = \frac{a_1}{a_2} = \frac{\Delta h + h_{11} Y_L}{h_{22} + Y_L} \]
  \[ Y_L \rightarrow \infty \]
  \[ Z_{2 \rightarrow} \infty \]

- **Output Admittance**
  \[ Y_o = \frac{a_1}{a_2} = \frac{\Delta h + h_{22} Z_i}{h_{11} + Z_L} \]
  \[ \frac{1}{Y_L} \]
  \[ h_{22} \]

- **Current Gain**
  \[ G_i = \frac{a_1}{a_2} = \frac{-h_{21} Y_L}{h_{22} + Y_L} \]
  \[ 0 \]
  \[ h_{21} \]

- **Voltage Gain**
  \[ G_v = \frac{a_1}{a_2} = \frac{-h_{21}}{\Delta h + h_{11} Y_L} \]
  \[ \mu \]
  \[ 0 \]

- **Transfer Impedance**
  \[ Z_m = \frac{a_1}{a_2} = \frac{-h_{21}}{h_{22} + Y_L} \]
  \[ -h_{21} \]
  \[ h_{22} \]

Matched Power Gain
\[ G_p = \frac{h_{21}}{(\sqrt{h_{11} h_{22}} + \sqrt{\Delta h})^2} \]
C.) Transistor Parameters used in Tabulation

\[ h_{11} = 2000 \text{ ohms} \quad h_{12} = 600 \times 10^{-6} \]
\[ h_{21} = 50 \quad h_{22} = 25 \times 10^{-6} \text{ mhos} \]

D.) Explanation of Tabulations

The circuits are tabulated in three groups:

- **Group 1:** High power gain circuits
  (used for most applications when power gain is desired)
- **Group 2:** Low power gain circuits
- **Group 3:**
  - a) Cascade circuits using one reversed transistor
  - b) Conditionally unstable circuits
  - c) Symmetrical circuits

For each circuit the following information is listed:

- \( \Delta h \): Determinant of "h" matrix of the device.
- \( \text{No.} \): Identification number.
- a-c circuit

- \( h_{11} \): Input impedance with the output short circuited.
- \( h_{12} \): Reverse voltage transfer ratio with the input open circuited.
- \( h_{21} \): Forward current gain with output short circuited
  This is the maximum current gain.
- \( h_{22} \): Output admittance with the input open circuited.
- \( Y_{10} \): Input admittance with output open circuited.
- \( G_{\text{rs}} \): Reverse current gain with input short circuited.
- \( \mu \): Voltage gain with output open circuited.
- \( Z_{os} \): Output impedance with the input short circuited.
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**GROUP 1**

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<td>Z_{os}</td>
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GROUP 2
LOW POWER GAIN CIRCUITS
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<td>33</td>
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</table>

**a-c Circuit**

|---|-----------------|-----------------|-----------------|-----------------|-----------------|

<table>
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<tr>
<th>h₁₁</th>
<th>2000</th>
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<th>40</th>
<th>41</th>
<th>39</th>
<th>50,000</th>
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</thead>
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<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
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<td>.5</td>
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<tr>
<td>h₂₁</td>
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<td>-2.0</td>
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<td>-1.02</td>
<td>-.983</td>
<td>-.982</td>
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<tr>
<td>h₂₂</td>
<td>.98 x 10⁻⁶</td>
<td>25 x 10⁻⁶</td>
<td>.51 x 10⁻⁶</td>
<td>.90 x 10⁻⁶</td>
<td>630 x 10⁻⁶</td>
<td>.48 x 10⁻⁶</td>
</tr>
</tbody>
</table>

| Y₁₀   | .50 x 10⁻⁶ | 13 x 10⁻⁶| .50 x 10⁻⁶| .49 x 10⁻⁶| 1200 x 10⁻⁶| .93 x 10⁻⁶ |
| G₉θ   | -.50 | -.50| -.981| -.981| -.972| -.972 |
| μ    | 1.0  | 1.0| 1.0| 1.0| 1.9 | 1.9 |
| Z₉θ   | 1000 | 40 | 39 | 40 | 75 | 97,000 |

**a-c Circuit**

|---|-----------------|-----------------|-----------------|-----------------|-----------------|

<table>
<thead>
<tr>
<th>Δh</th>
<th>.50</th>
<th>.50</th>
<th>.98</th>
<th>.98</th>
<th>1.9</th>
<th>1.9</th>
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**GROUP 2**

LOW POWER GAIN CIRCUITS
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<th>$0.35$</th>
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<th>$3900 \times 10^{-6}$</th>
<th>$690 \times 10^{-6}$</th>
<th>$27 \times 10^{-6}$</th>
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<tr>
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<td><img src="image1" alt="Circuit" /></td>
<td>$h_{11}$</td>
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<td>50,000</td>
<td>4000</td>
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<td><img src="image2" alt="Circuit" /></td>
<td>$h_{12}$</td>
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<td>$2000 \times 10^{-6}$</td>
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<td><img src="image3" alt="Circuit" /></td>
<td>$h_{21}$</td>
<td>$-0.50$</td>
<td>$-0.19$</td>
<td>$-2000 \times 10^{-6}$</td>
<td>$-2000 \times 10^{-6}$</td>
<td>$-0.50$</td>
<td>$0.020$</td>
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<tr>
<td>37</td>
<td><img src="image4" alt="Circuit" /></td>
<td>$h_{22}$</td>
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<td>$48 \times 10^{-6}$</td>
<td>$981 \times 10^{-6}$</td>
<td>$50 \times 10^{-6}$</td>
<td>$13 \times 10^{-6}$</td>
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<tr>
<td>38</td>
<td><img src="image5" alt="Circuit" /></td>
<td>$Y_{10}$</td>
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<td>$14 \times 10^{-6}$</td>
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<tr>
<td>39</td>
<td><img src="image6" alt="Circuit" /></td>
<td>$Z_{0S}$</td>
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<td>$1.5 \times 10^{-6}$</td>
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<td>$1.5 \times 10^{-6}$</td>
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**GROUP 2**

LOW POWER GAIN CIRCUITS
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<tr>
<th>( \Delta h )</th>
<th>No.</th>
<th>Circuit</th>
<th>( h_{11} )</th>
<th>( h_{12} )</th>
<th>( h_{21} )</th>
<th>( h_{22} )</th>
<th>( Y_{10} )</th>
<th>( G_{es} )</th>
<th>( \mu )</th>
<th>( Z_{os} )</th>
<th>( \Delta h )</th>
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</thead>
<tbody>
<tr>
<td>37,000</td>
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<td></td>
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<td>710</td>
<td>-14</td>
<td>0.019</td>
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<td>-0.019</td>
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<tr>
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<td></td>
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<td>0.98</td>
<td>-0.028</td>
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<td>67</td>
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<td>.066</td>
<td>43</td>
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<td>14</td>
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<tr>
<td>1400 ( \times ) 10^{-6}</td>
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<td>-0.028</td>
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<td>75</td>
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<td>27 ( \times ) 10^{-6}</td>
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GROUP 3-a
LOW POWER GAIN CASCADE CIRCUITS
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<th>Δh</th>
<th>a-c Circuit</th>
<th>h11</th>
<th>h12</th>
<th>h21</th>
<th>h22</th>
<th>Y₁₀</th>
<th>Z₁₀</th>
<th>Gcs</th>
<th>μ</th>
<th>Zo</th>
<th>Δh</th>
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<tbody>
<tr>
<td>46</td>
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<tr>
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<td>-420 x 10⁻⁶</td>
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<td>-0.01 x 10⁻⁶</td>
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GROUP 3-a
CONDITIONALLY UNSTABLE CIRCUITS
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<td><img src="image" alt="Circuit Diagram" /></td>
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</tr>
<tr>
<td>h_{11}</td>
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<td>40000</td>
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<td>190,000</td>
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<td>.43</td>
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<td>h_{21}</td>
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<td>$2400 \times 10^{-6}$</td>
<td>$980 \times 10^{-6}$</td>
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<td>$50 \times 10^{-6}$</td>
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<td>$G_{cs}$</td>
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<td>-1.0</td>
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**GROUP 3-c**

**SYMMETRICAL CIRCUITS**
APPENDIX III

DERIVATION OF EQUATIONS

A.) Derivation of Equation 2.4, page 8

The "h" parameters of a reversed device can be derived as follows:

\[
\begin{align*}
\lambda_{n}^2 &= \frac{x_i}{x_i} \bigg|_{x_i = 0} \\
\lambda_{22} &= \frac{x_2}{x_2} \bigg|_{x_2 = 0}
\end{align*}
\]

\[
\begin{align*}
\lambda_{n}^2 &= \frac{x_i}{x_i} = \frac{1}{h_{22}} \frac{1}{1 - h_{11}h_{11} / h_{11}h_{11}} = \frac{h_{11}}{h_{11}h_{22} - h_{12}h_{21}} = \frac{h_{11}}{\Delta h} \\
\lambda_{22} &= \frac{x_2}{x_2} \bigg|_{x_2 = 0}
\end{align*}
\]

\[
\begin{align*}
\lambda_{n}^2 &= \frac{x_i}{x_i} = \frac{-h_{12}}{h_{11}h_{22} - h_{12}h_{21}} = \frac{-h_{12}}{\Delta h} \\
\lambda_{22} &= \frac{x_2}{x_2} \bigg|_{x_2 = 0}
\end{align*}
\]

\[
\begin{align*}
\lambda_{n}^2 &= \frac{x_i}{x_i} = \frac{-h_{21}}{h_{11}h_{22} - h_{12}h_{21}} = \frac{-h_{21}}{\Delta h} \\
\lambda_{22} &= \frac{x_2}{x_2} \bigg|_{x_2 = 0}
\end{align*}
\]

\[
\begin{align*}
\lambda_{n}^2 &= \frac{x_i}{x_i} = \frac{1}{h_{22}} \frac{1}{1 - h_{11}h_{11} / h_{11}h_{11}} = \frac{h_{11}}{h_{11}h_{22} - h_{12}h_{21}} = \frac{h_{22}}{\Delta h} \\
\lambda_{22} &= \frac{x_2}{x_2} \bigg|_{x_2 = 0}
\end{align*}
\]

From equation 2.5,

\[ R_{11} > 0 \quad ; \quad R_{22} > 0 \quad ; \quad \Delta R > 0 \]

The "h" parameters can be written in terms of "R" parameters.

\[ h_{11} = \frac{\Delta R}{R_{22}} \quad ; \quad h_{12} = \frac{R_{12}}{R_{22}} \]

\[ h_{21} = -\frac{R_{11}}{R_{22}} \quad ; \quad h_{22} = \frac{1}{R_{22}} \]

\[ \Delta k = \frac{R_{11}}{R_{22}} \]

from which

\[ h_{11} > 0 \quad ; \quad h_{22} > 0 \quad ; \quad \Delta k > 0 \]

follows directly.

C.) Method of measuring values given in Figure 7.

The measurements on the high impedance circuits can be made using the following procedure. References are made to the figure below:

\[ G = 1 - \delta \]

\[ \delta \ll 1 \]

\[ I_{E} : \quad R_{4} = \infty \quad R_{L} = \infty \]

\[ \text{Then:} \quad \frac{a_{4}}{a_{6}} = N \approx \frac{R_{2}}{R_{2} + R_{4}} \]

\[ \text{or:} \quad R_{x} = \left[ \frac{N}{1-N} \right] R_{4} \]

The input impedance can then easily be measured. \( R_{s} \) should be of the same order of magnitude as \( R_{4} \).
C.) Continued

To measure \( R_e \) and the gain \((1-\delta)\) two other measurements must be made

if \( R_L = \infty \), \( R_t \neq \infty \), \( R \gg \frac{R_f}{\delta} \)

then
\[
\frac{\Delta I}{\Delta V} = k \approx \frac{1 + \frac{R_e}{R_f}}{1 + \frac{R_e}{R_f} + \frac{\delta R_t}{R_f}}
\]

and if \( R_L \neq \infty \), \( R_t \neq \infty \), \( R \gg \frac{R_f}{\delta} \)

then
\[
\frac{\Delta I}{\Delta V} = m \approx \frac{1 + \frac{R_e}{R_f}}{1 + \frac{R_e}{R_f} + \frac{\delta R_t}{R_f} + \frac{R_e R_t}{R_f}}
\]

These two equations may then be solved for the two unknowns \(\delta\) and \(R_e\).

\[
\frac{1}{\delta} = \frac{R_e}{R_f} \left[ \frac{K}{1 - K} \right] \left[ \frac{R_f}{R_e} - \left( \frac{1}{m} - \frac{1}{K} \right) \right]
\]

where \(C = 1 - \delta\)

\[
R_e = \frac{\left( \frac{1}{m} - \frac{1}{K} \right)}{\frac{R_f}{R_e} - \left( \frac{1}{m} - \frac{1}{K} \right)} R_f
\]

The following values of resistors were used in the measurements listed

\[
R_f = 100 \ \Omega
\]
\[
R_e = 50 \ \text{K}\Omega
\]
\[
R_L = 10 \ \text{K}\Omega
\]

Blocking capacitors must be used so that the d-c bias conditions will not be disturbed. Small value of signal, \(\Delta_i\), should be used to avoid clipping in the output waveform.