Enhanced Hole Transport in Short-Channel Strained-SiGe p-MOSFETs

Citation: Gomez, L., P. Hashemi, and J.L. Hoyt. "Enhanced Hole Transport in Short-Channel Strained-SiGe p-MOSFETs." Electron Devices, IEEE Transactions on 56.11 (2009): 2644-2651. © 2009 Institute of Electrical and Electronics Engineers

As Published: http://dx.doi.org/10.1109/ted.2009.2031043

Publisher: Institute of Electrical and Electronics Engineers

Persistent URL: http://hdl.handle.net/1721.1/52379

Version: Final published version: final published article, as it appeared in a journal, conference proceedings, or other formally published context

Enhanced Hole Transport in Short-Channel Strained-SiGe p-MOSFETs

Leonardo Gomez, Pouya Hashemi, *Student Member, IEEE*, and Judy L. Hoyt, *Fellow, IEEE*

***Abstract*—Hole mobility and velocity are extracted from scaled strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs on insulator. Devices have been fabricated with sub-100-nm gate lengths, demonstrating hole mobility and velocity enhancements in strained-$Si_{0.45}Ge_{0.55}$ channel devices relative to Si. The effective hole mobility is extracted utilizing the dR/dL method. A hole mobility enhancement is observed relative to Si hole universal mobility for short-channel devices with gate lengths ranging from 65 to 150 nm. Hole velocities extracted using several different methods are compared. The hole velocity of strained-SiGe p-MOSFETs is enhanced over comparable Si control devices. The hole velocity enhancements extracted are on the order of 30%. Ballistic velocity simulations suggest that the addition of $\langle 110 \rangle$ uniaxial compressive strain to $Si_{0.45}Ge_{0.55}$ can result in a more substantial increase in velocity relative to relaxed Si.**

***Index Terms*—Hole mobility, hole velocity, p-MOSFET, silicon germanium, uniaxial stress.**

I. Introduction

SCALING of device dimensions alone can no longer provide the necessary current drive enhancements required to continue historic performance gains. Novel channel materials are being explored as a means to supplement the performance gains provided by geometric scaling. Starting at the 90-nm CMOS technology node, embedded SiGe source/drains (S/Ds) were used to introduce uniaxial compressive strain into the channel as a means to increase the p-MOSFET drive current [1]. The uniaxial strain imparted by the embedded SiGe S/D regions alters the intrinsic electrical properties of the channel, making it favorable for hole transport [2], [3]. The hole velocity in state-of-the-art strained-Si p-MOSFETs has been extracted, and a velocity enhancement is observed over comparable relaxed-Si devices [4]. The transport benefits provided by uniaxial strain are expected to saturate in Si, requiring the introduction of other high-mobility/low-carrier effective mass channel materials [2], [5].

SiGe and Ge are under investigation as Si channel replacement technologies. Substantial hole mobility enhancements have been reported for long-channel biaxial compressive strained-Ge p-MOSFETs [6], [7]. Sub-100-nm strained-Ge p-MOSFETs have also been fabricated, which demonstrate enhanced drive current over comparable Si control devices [8]–[11]. The intrinsic transport properties of bulk Ge make it an attractive material for n- and p-MOSFETs, but process integration issues and degradation of transistor performance characteristics (e.g., formation of a high-quality gate dielectric and increased OFF-state leakage due to bandgap narrowing) are making Ge CMOS a challenging endeavor. SiGe can provide transport performance gain for the p-MOSFET without the same magnitude of challenges. Long-channel bulk strained-SiGe p-MOSFETs have been fabricated, which exhibit substantial hole mobility enhancements relative to relaxed-Si controls [7], [12]. Enhanced drive currents have also been reported in sub-100-nm strained-SiGe channel p-MOSFETs [13]–[15]. These studies have focused most of their efforts in examining the transistor performance characteristics, while the fundamental hole transport metrics (e.g., carrier velocity) for a strained-SiGe channel have yet to be studied as extensively.

In this paper, the merits of a biaxial compressive strained-SiGe channel are explored experimentally from the perspective of carrier transport. The hole mobility and velocity are measured in sub-100-nm strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs on insulator. The goal is to assess the scalability of these transport metrics. An ultrathin-body architecture is utilized to improve electrostatics at shorter gate lengths without the requirement of halo or body implants, which may impact the channel strain or degrade carrier mobility by introducing coulombic scattering centers [16]. Process steps, which might disrupt the channel strain, were modified or eliminated in an attempt to examine the intrinsic transport performance gains independent of process conditions. Band structure and ballistic velocity simulations are also presented to explore the benefits of introducing uniaxial compressive stress to an already biaxial compressive strained-SiGe channel. This paper is organized as follows. The device fabrication sequence is discussed in Section II. Then, the electrical measurements, as well as the mobility and velocity extraction methods, are described in Section III. Finally, the extracted transport metrics, as well as simulated velocity results, are discussed in Section IV.

II. Device Fabrication

Device fabrication began by growing a 7-nm-thick strained-$Si_{0.45}Ge_{0.55}$ film on a 15-nm-thick (100) SOI film. After $Si_{0.45}Ge_{0.55}$ growth, the structure was capped with 5 nm of Si. This structure was grown in an Applied Materials Epi Centura LPCVD reactor. The $Si_{0.45}Ge_{0.55}$ layer in this structure is under biaxial compressive strain due to the lattice mismatch

Manuscript received February 26, 2009; revised May 27, 2009. First published September 29, 2009; current version published October 21, 2009. The review of this paper was arranged by Editor D. Esseni.

The authors are with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA, and also with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: leog@mit.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2009.2031043

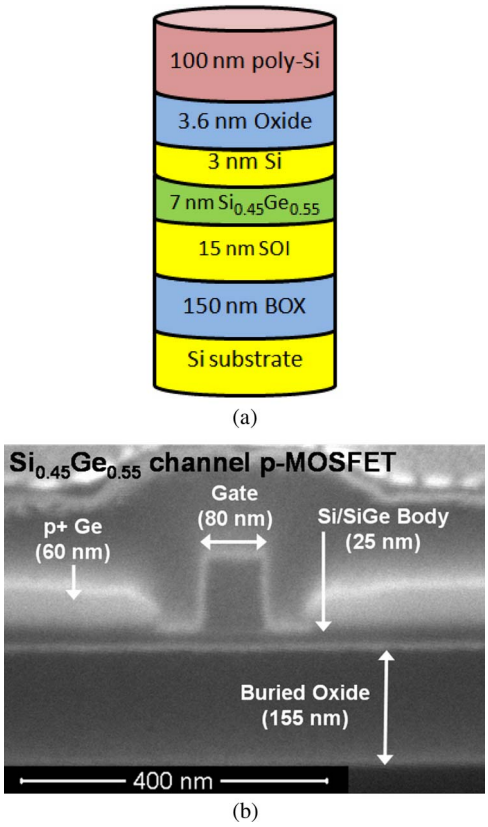


Fig. 1. (a) Schematic view of the device structure. The channel consists of a 7-nm-thick biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ layer pseudomorphic to a 15-nm-thick relaxed SOI. The structure is capped with 3 nm of Si. (b) Cross-sectional SEM micrograph of an 80-nm-long strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET. The total channel thickness is 25 nm. Heavily boron doped Ge of 60 nm was selectively grown in the S/D region.

that is present between the $Si_{0.45}Ge_{0.55}$ and the underlying relaxed SOI film. A mesa isolation scheme oriented in the $\langle 110 \rangle$ direction was used to electrically isolate devices from one another. The gate stack was subsequently formed by thermally oxidizing the Si cap at 600 °C to form a 3.6-nm gate oxide and depositing 100 nm of heavily n-doped polycrystalline silicon. Hybrid e^--beam and photolithography were used to pattern a nitride hard mask on the gate. Gate lengths down to 65 nm were patterned using XR-1541 (Dow Corning) e^--beam resist. The extension region was then formed by implanting boron into the substrate (boron, 6 keV, 2×10^{14} cm^{-2}). A medium-dose extension implant was utilized to minimize strain relaxation in the $Si_{0.45}Ge_{0.55}$ channel. Retaining the strain along the $\langle 110 \rangle$ transport direction is critical to observe enhanced hole transport characteristics. LTO of 120 nm was then deposited, and spacers were formed. The deep S/D implant was omitted from this process to avoid strain relaxation. Boron-doped germanium was selectively grown in the S/D region to reduce the parasitic series resistance. Dopants were activated with a rapid thermal anneal consisting of 30 s at 650 °C followed by 5 s at 700 °C. A conservative thermal budget was maintained to minimize Ge outdiffusion from the strained-$Si_{0.45}Ge_{0.55}$ layer. Silicon control devices were also fabricated in parallel for comparison. Fig. 1(a) shows a depiction of the channel structure, and Fig. 1(b) shows a cross-sectional scanning electron micrograph of a completed MOSFET with an 80-nm polysilicon gate length.

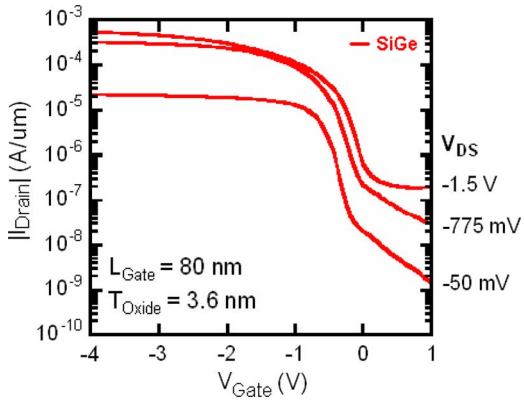


Fig. 2. Transfer characteristics for 80-nm strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET. The measured subthreshold swing is 170 mV/dec.

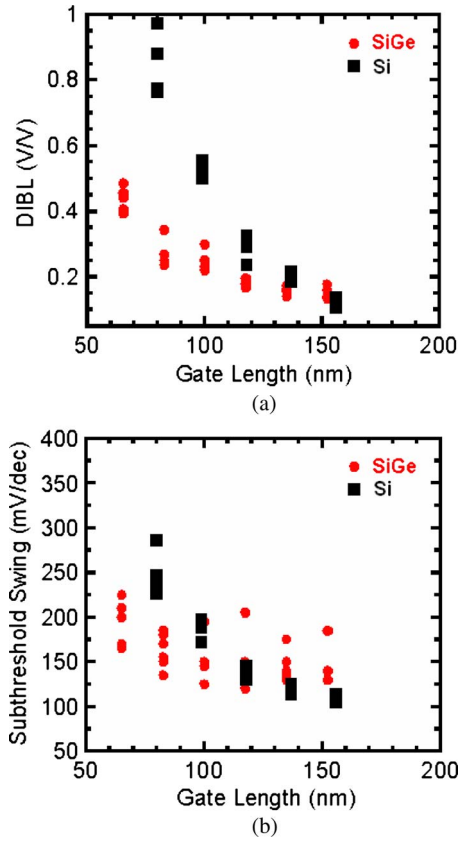


Fig. 3. (a) DIBL versus L_{Gate} comparison between strained-$Si_{0.45}Ge_{0.55}$ and Si control p-MOSFETs. (b) Subthreshold swing versus L_{Gate} comparison between strained-$Si_{0.45}Ge_{0.55}$ and Si control devices. The strained-$Si_{0.45}Ge_{0.55}$ channel devices exhibit improved electrostatic behavior at shorter gate lengths due to a thinner body. DIBL was measured using the constant current method in the subthreshold regime. The subthreshold swing was measured at $V_{\mathrm{DS}} = -50$ mV.

III. Electrical Measurements and Analysis

A. Electrical Measurements

Standard I_{DS}–V_{GS} curves are shown in Fig. 2 for an 80-nm gate-length strained-$Si_{0.45}Ge_{0.55}$ p-MOSFET. The DIBL and subthreshold swing characteristics versus gate length (L_{Gate}) are shown in Fig. 3. Reasonable electrostatic behavior is observed down to a gate length of 100 nm for strained-$Si_{0.45}Ge_{0.55}$ devices and 120 nm for the Si control. The

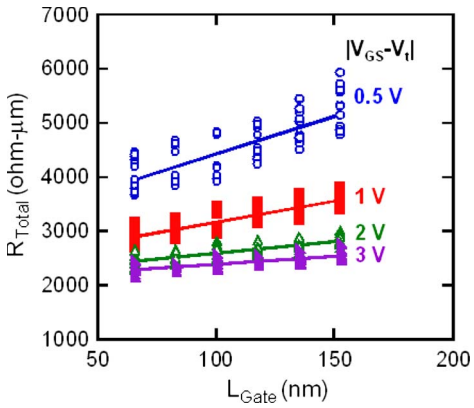


Fig. 4. Total device resistance R_{Total} versus gate length at various gate overdrives. The slope of each line is utilized to determine the extrinsic series resistance and hole effective mobility.

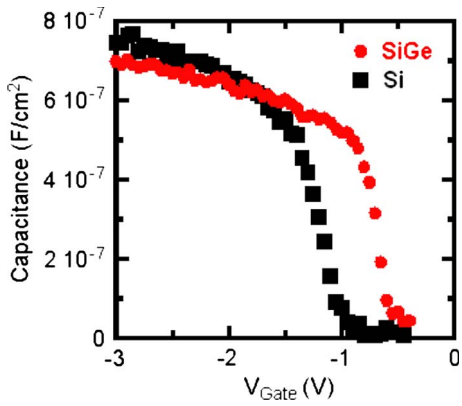


Fig. 5. Measured gate C–V curves for long-channel (4 μm long $\times$ 50 μm wide) Si control and strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs. The measurement frequency was 5 kHz.

difference in electrostatic behavior can be attributed to the difference in body thickness between these devices. The strained-$Si_{0.45}Ge_{0.55}$ devices have a total body thickness of 25 nm, which includes a 3-nm Si cap, 7-nm buried $Si_{0.45}Ge_{0.55}$ channel, and 15-nm underlying SOI film. The Si control devices have a body thickness of 40 nm.

Series resistance extraction was performed using the L-array method [17]. Fig. 4 shows the total device resistance plotted for a variety of gate lengths and gate overdrive values. The series resistance is the value at which the various lines converge. Cross-sectional SEM imaging at $L_{\mathrm{Gate}} = 135$ nm and $L_{\mathrm{Gate}} = 80$ nm was utilized to determine the offset between the target and physical gate length. This offset was used to determine the physical gate length of the devices in this paper. The extracted S/D extrinsic series resistances (R_{SD}'s) for strained-SiGe and Si control devices are 2000 and 2500 $\Omega \cdot \mu$m, respectively. The high series resistance is due to the large distance between the gate edge and S/D contact plugs (2 μm) and the absence of a silicide or germanide process. In addition, some contribution to R_{SD} may be expected from the S/D extension process (moderate-dose and low-temperature activation) which largely preserved the channel strain, as shown in the next sections. For incorporation of SiGe in state-of-the-art p-MOSFETs, processes must be developed which preserve the channel strain while minimizing the impact on series resistance.

The measured gate capacitance–voltage (C–V) curves for long-channel Si and strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs are shown in Fig. 5 and were used in the mobility and velocity extractions discussed in the following section. The measurement frequency was 5 kHz. The large series resistance of these devices prevented the measurement at higher frequencies.

B. Hole Effective Mobility Extraction

Hole effective mobility was measured in short-channel strained-SiGe and Si control devices using the dR/dL method [18]. The dR/dL mobility is calculated using the slope of the total device resistance versus gate length as shown in Fig. 4. This extraction method is a measure of the mobility over a range of gate lengths and assumes that the mobility, as well as the

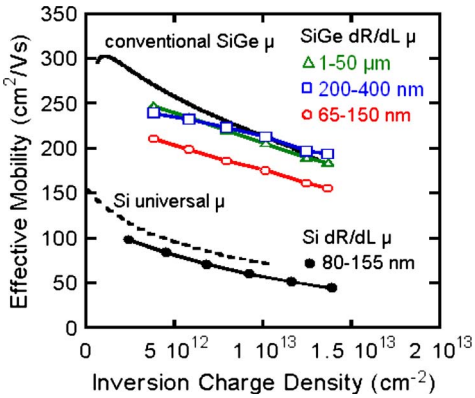


Fig. 6. Comparison between the long-channel (g_D/Q_{inv}) and short-channel dR/dL extracted mobilities for Si and strained-SiGe p-MOSFETs. A 3$\times$ enhancement over the Si hole universal mobility is observed for strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs with L_{Gate} ranging from 0.2 to 50 μm. Devices with gate lengths ranging from 65 to 150 nm show a 2.4$\times$ enhancement. The dR/dL mobility curve for Si p-MOSFETs with gate lengths ranging from 80 to 155 nm is also plotted for comparison.

series resistance, is constant for devices in a given range. The dR/dL hole effective mobility was calculated as follows:

$$\mu_{\mathrm{eff}} = \frac{1}{WQ_{\mathrm{inv}}\frac{dR_{\mathrm{Total}}}{dL}} \tag{1}$$

where W is the device width, Q_{inv} is the inversion charge density, and dR_{Total}/dL is the slope of the linear fit to the data in Fig. 4. The inversion charge density is estimated from the C–V curves measured on large-area MOSFETs with a gate length of 4 μm and a device width of 50 μm (Fig. 6). The long-channel hole effective mobility was extracted using both the dR_{Total}/dL and the more conventional (g_D/Q_{inv}) approach

$$\mu_{\mathrm{eff}} = \frac{g_D L}{Q_{\mathrm{inv}} W} \tag{2}$$

where g_D is the output conductance measured at low V_{DS}, L is the gate length, W is the device width, and Q_{inv} is the inversion charge density [17]. The dR/dL mobility was calculated for strained-$Si_{0.45}Ge_{0.55}$ devices with gate lengths

ranging from 65 to 150 nm, 200 to 400 nm, and 1 to 50 μm. The conventional $g_D/Q_{\rm inv}$ effective mobility was extracted from a 100-μm-long strained-$Si_{0.45}Ge_{0.55}$ channel mobility extraction MOSFET [19]. The extracted effective hole mobility curves are shown in Fig. 6. The Si hole universal mobility and dR/dL mobility for Si p-MOSFETs with gate lengths ranging from 80 to 155 nm are also plotted for comparison. The reported mobilities for both long- and short-channel strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs are higher than the Si control and hole universal mobility curves. These results are discussed in more detail in Section IV.

C. Hole Velocity Calculation

Hole velocity has been extracted utilizing various methods on both strained-$Si_{0.45}Ge_{0.55}$ and Si channel p-MOSFETs. The velocities examined in this paper are defined as follows:

$$\upsilon_{\rm id} = \frac{I_D}{W\int\limits_0^{V_{\rm GS}-\Delta V_t} C_{\rm GSD}\,dV_{\rm GS}} \tag{3}$$

$$\upsilon_{\rm gmi} = \frac{g_{\rm mi}}{WC_{\rm inv}} \tag{4}$$

$$\upsilon_{\rm xo} = \frac{\upsilon}{1 - WC_{\rm inv}R_S(1+2\delta)\upsilon} \tag{5}$$

where I_D is the drive current, $V_{\rm GS}$ is the gate-to-source voltage, W is the device width, ΔV_t is the threshold voltage difference due to roll-off and DIBL at a given gate length, $C_{\rm GSD}$ is the gate-to-S/D capacitance, $g_{\rm mi}$ is the intrinsic transconductance correcting for the source resistance [20], υ is the average velocity of carriers ($\upsilon = I_D/WQ_{\rm inv}$), $C_{\rm inv}$ is the gate capacitance at inversion, R_S is the source resistance which is assumed to be half of $R_{\rm SD}$, and δ is the DIBL coefficient [4], [21]. Energy balance simulations performed by Lochtefeld and Antoniadis indicate that the $\upsilon_{\rm id}$ and $\upsilon_{\rm gmi}$ extraction methods estimate the carrier velocity at different points along the channel [21]. The virtual source velocity ($\upsilon_{\rm xo}$) as defined by (5) has been utilized by Khakifirooz *et al.* to extract the carrier velocity near the source injection point [4]. Both $\upsilon_{\rm xo}$ and $\upsilon_{\rm id}$ estimate the carrier velocity near the source injection point, while $\upsilon_{\rm gmi}$ tends to estimate the velocity deeper into the channel.

The bias conditions at which $\upsilon_{\rm id}$, $\upsilon_{\rm gmi}$, and $\upsilon_{\rm xo}$ were calculated correspond to the peak transconductance (g_m), where $V_{\rm DS} = -1.5$ V. The inversion charge density was estimated by integrating the C–V characteristics of large-area MOSFETs. The inversion capacitance was also estimated from large-area C–V characteristics. Corrections were made for V_t roll-off and DIBL in estimating the inversion charge density and capacitance. The average gate overdrive at which $\upsilon_{\rm id}$, $\upsilon_{\rm gmi}$, and $\upsilon_{\rm xo}$ were calculated is -1.4 V. This corresponds to an inversion charge density of $\sim 6 \times 10^{12}$ cm^{-2}.

The calculated hole velocities are shown in Fig. 7(a) and (b) versus gate length and in Fig. 7(c) and (d) versus DIBL. The reported velocities are higher in the strained-$Si_{0.45}Ge_{0.55}$ channel p-MOSFETs relative to the Si control. This will be discussed further in the following section.

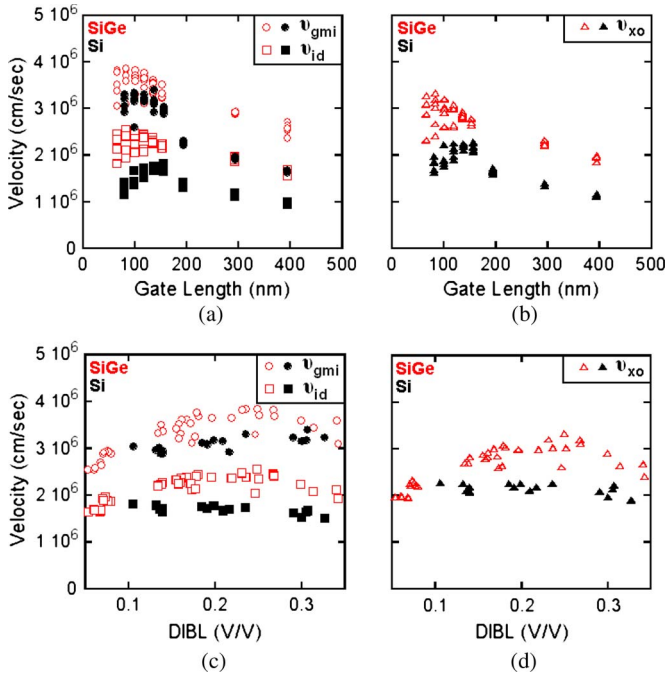


Fig. 7. Comparison of (a) $\upsilon_{\rm gmi}$ and $\upsilon_{\rm id}$ versus $L_{\rm Gate}$, (b) $\upsilon_{\rm xo}$ versus $L_{\rm Gate}$, (c) $\upsilon_{\rm gmi}$ and $\upsilon_{\rm id}$ versus DIBL, and (d) $\upsilon_{\rm xo}$ versus DIBL between strained-$Si_{0.45}Ge_{0.55}$ and Si control devices. The open symbols represent strained-SiGe channel devices, while the closed symbols represent the Si control devices.

IV. Discussion

A. Hole Mobility in Scaled Strained-SiGe p-MOSFETs

Hole mobility is dependent upon the scattering rate of carriers and their effective mass. The hole mobility benefits derived from adding biaxial compressive strain to $Si_{1-x}Ge_x$ result from a reduction in phonon scattering and a reduction in the hole effective mass [2], [22]. For $\langle 110\rangle$-oriented devices, a reduction in carrier effective mass stems from both the presence of Ge in the channel and the biaxial compressive strain present in the material. The biaxial compressive strain also works to lift the degeneracy between the light and heavy hole valence bands, reducing the phonon scattering rate. If significant strain loss occurs during processing, then the transport benefits derived from a strained-SiGe channel can be lost. Preserving the channel strain can be difficult as gate lengths are scaled. While process steps like extension and halo implants are critical for ensuring electrostatic integrity at shorter gate lengths, they can alter or reduce the strain in the channel.

The extracted effective hole mobilities for long- and short-channel strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs are shown in Fig. 6. For devices with gate lengths larger than 200 nm, the conventional $g_D/Q_{\rm inv}$ and dR/dL extraction methods are in good agreement, particularly at higher inversion charge densities. A 3× mobility enhancement over the Si hole universal mobility curve is observed for this device set. The dR/dL mobility extracted from devices with gate lengths ranging from 65 to 150 nm is also shown in Fig. 6 along with the dR/dL hole mobility for Si control devices with gate lengths ranging from 80 to 155 nm. A 2.5× hole mobility enhancement is observed relative to the Si control mobility for strained-SiGe channel p-MOSFET with gate lengths ranging from 65 to 150 nm. A

slight reduction in mobility is seen as the gate length is reduced, but the enhancement provided over the Si control mobility is still substantial. The observed mobility drop may result from partial relaxation of the longitudinal strain in the channel. While attempts were made to minimize strain relaxation in the channel, some strain loss may have occurred through the course of fabricating these devices.

B. Hole Velocity in Scaled Strained-SiGe p-MOSFETs

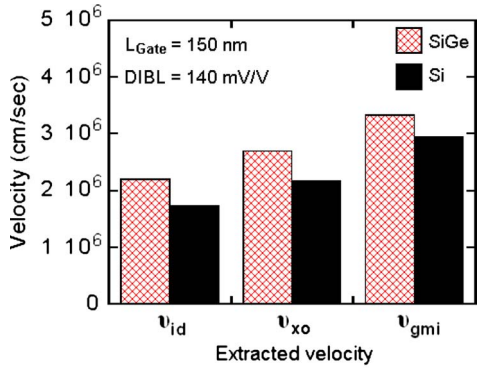
Carrier velocity increases for smaller carrier effective mass [2], [4]. Theoretical calculations indicate that the hole effective mass in relaxed $Si_{1-x}Ge_x$ is lower than that in relaxed Si [22]. With the introduction of biaxial compressive strain, the effective mass is reduced further. The lower hole effective mass of strained SiGe should translate to improved velocity characteristics relative to relaxed Si.

Fig. 7(a) and (b) shows the gate-length dependence of $\upsilon_{\rm id}$, $\upsilon_{\rm gmi}$, and $\upsilon_{\rm xo}$ extracted for the devices in this paper. An increase in velocity is observed as the gate length decreases. The velocity's dependence on DIBL shown in Fig. 7(c) and (d) is less dramatic for values greater than 0.1 V/V. A slight increase in velocity is observed as DIBL increases. This relation is a result of the drain's influence on the channel potential. As DIBL increases, the channel potential drops more abruptly from source to drain, which increases carrier velocity. There is also evidence to suggest that device design influences the velocity–DIBL relation [23]. In Fig. 8(a), a comparison of the extracted velocities is made between strained-SiGe and Si p-MOSFETs with similar DIBL and gate-length values, i.e., 140 mV/V and 150 nm, respectively. This provides the best basis for comparison since velocity is dependent on DIBL, gate length, and other device design parameters [23].

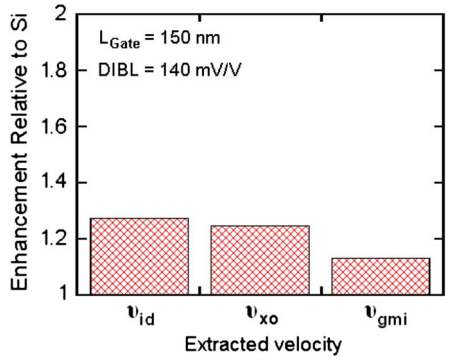
As mentioned previously, the velocity extraction methods employed estimate the carrier velocity at different points in the channel. In Fig. 8(a), the extracted velocities are arranged in order of increasing distance from the source, where $\upsilon_{\rm id}$ is closest to the source injection point and $\upsilon_{\rm gmi}$ estimates the velocity furthest into the channel. We observe the expected trend of increasing velocity at points further from the source (i.e., further into the channel). The velocity enhancement is also observed to be largest near the source. The hole velocity enhancement shown in Fig. 8(b) for various extraction methods ranges from 1.1× to 1.3×. The velocity gains reported for a biaxial compressive strained-SiGe channel are modest due to the limited effective mass reduction resulting from biaxial compressive strain. A more substantial increase in velocity is expected with the addition of uniaxial compressive strain along the ⟨110⟩ direction of transport.

C. Uniaxial Strain in SiGe Channel p-MOSFETs

As mentioned previously, hole velocity is correlated to the carrier effective mass. Velocity calculations performed by Uchida *et al.* [2] and Antoniadis and Khakifirooz [5] indicate that uniaxial compressive stress when applied to (100) Si or Ge along the ⟨110⟩ direction is more effective than biaxial compressive strain in reducing the hole effective mass and



(a)



(b)

Fig. 8. (a) Comparison of the average $\upsilon_{\rm id}$, $\upsilon_{\rm gmi}$, and $\upsilon_{\rm xo}$ extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ and Si control devices examined here have an average $L_{\rm Gate} = 150$ nm and DIBL = 140 mV/V. (b) Enhancement relative to the Si control for the average $\upsilon_{\rm id}$, $\upsilon_{\rm gmi}$, and $\upsilon_{\rm xo}$ extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs exhibit an enhancement over Si control devices ranging from 1.13× to 1.27×. All devices have an average $L_{\rm Gate} = 150$ nm and DIBL = 140 mV/V.

thus increasing the hole velocity. Fig. 9 shows simulated $k \bullet p$ dispersion calculations performed in this paper in the ⟨110⟩ direction for relaxed Si, biaxial compressive strained $Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed Si, relaxed Ge, and biaxial compressive strained Ge pseudomorphic to relaxed $Si_{0.6}Ge_{0.4}$, all with uniaxial stress ranging from 0 to −3 GPa added along the ⟨110⟩ direction. These $k \bullet p$ band calculations were performed using $nextnano^3$ [24]. For the material systems examined in Fig. 9, carriers preferentially occupy the HH band due to a lifting of the degeneracy between the LH and HH valence bands. The applied uniaxial stress increases the curvature associated with the HH band and thus reduces the effective mass. This type of HH band deformation is favorable toward increasing the carrier velocity [2], [5], [25].

The $E-k$ dispersion relations for relaxed Si and biaxial compressive strained $Si_{0.45}Ge_{0.55}$, in Fig. 9(a) and (b), respectively, show that, with 3 GPa of applied compressive uniaxial stress, the strained-$Si_{0.45}Ge_{0.55}$ HH band has a higher degree of curvature. Improved velocity characteristics are expected for strained $Si_{0.45}Ge_{0.55}$ over Si as a result. Examining the dispersion relations for relaxed Ge and biaxial compressive strained Ge, in Fig. 9(c) and (d), respectively, we notice that the initial shapes of the HH bands are dissimilar, but as uniaxial stress is applied to these systems, the HH bands begin to follow the same trajectory. As a result, similar hole velocity characteristics would be expected with added uniaxial stress,

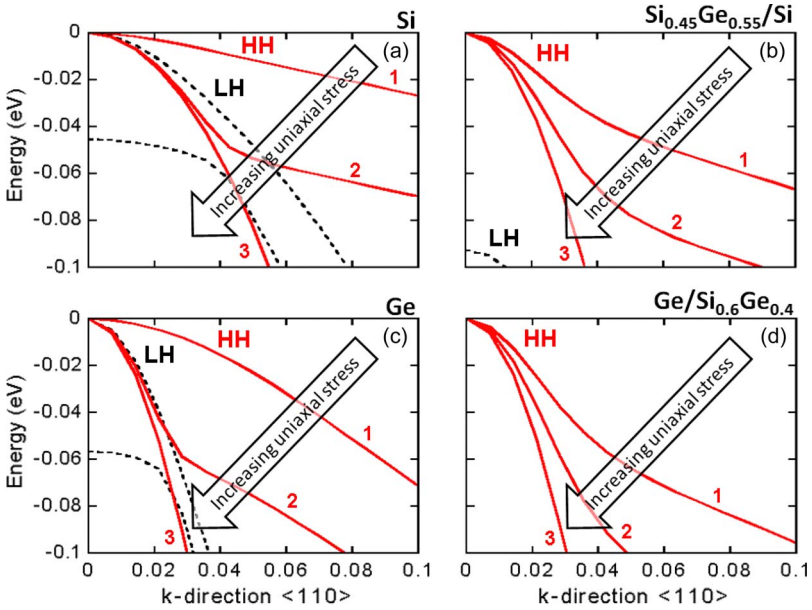


Fig. 9. $\langle 110 \rangle$ $E-k$ dispersion relation for (a) Si, (b) strained $Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed Si ($Si_{0.45}Ge_{0.55}/Si$), (c) Ge, and (d) strained Ge pseudomorphic to relaxed $Si_{0.6}Ge_{0.4}$ ($Ge/Si_{0.6}Ge_{0.4}$) with 0, -1, and -3 GPa of uniaxial stress applied in the $\langle 110 \rangle$ direction. The curves, which correspond to these stress levels, are marked 1, 2, and 3, respectively. The solid lines represent the HH band, and the dashed lines represent the LH band. The arrows point in the direction of increasing uniaxial stress going from 0 to -3 GPa. The addition of uniaxial stress increases the curvature of HH band. An increase in curvature is strongly correlated to a reduction in effective mass, which results in an increase in velocity. Simulations were performed using $nextnano^3$ [24].

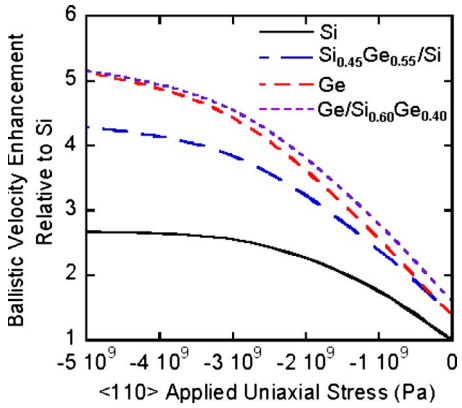


Fig. 10. Simulated ballistic velocity enhancement relative to relaxed Si with applied compressive uniaxial stress for Si, biaxial compressive strained $Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed Si ($Si_{0.45}Ge_{0.55}/Si$), Ge, and biaxial compressive strained Ge pseudomorphic to relaxed $Si_{0.6}Ge_{0.4}$ ($Ge/Si_{0.6}Ge_{0.4}$). Simulations were performed using $nextnano^3$ and FETtoy [24], [26].

irrespective of whether one begins with relaxed or biaxially strained Ge.

In Fig. 10, the simulated ballistic velocity enhancement relative to relaxed Si is provided for Si, biaxial compressive strained $Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed Si, Ge, and biaxial compressive strained Ge pseudomorphic to relaxed $Si_{0.45}Ge_{0.55}$, all with added uniaxial strain. Simulations were performed by calculating the 2-D $E-k$ dispersion relation using $nextnano^3$. The simulated band structure was used as an input to FETtoy which calculates the ballistic current [26]. The calculated ballistic current and $Q_{\rm inv}$ were used to determine the ballistic velocity (v_θ) according to $v_\theta = I_{\rm ballistic}/WQ_{\rm inv}$.

The virtual source velocity $(v_{\rm xo})$ is related to the ballistic velocity (v_θ) according to $v_{\rm xo} = Bv_\theta$, where B is the ballistic efficiency [4]. A comparison of the relative velocity enhancement can be made between $v_{\rm id}$, $v_{\rm xo}$, and v_θ due to this linear relation. Examining the ballistic velocity simulations in Fig. 10, we see that a biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ channel with no applied uniaxial stress provides a $1.4\times$ ballistic velocity enhancement over unstrained Si. This is of the same order as the measured velocity enhancement for biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ in Fig. 8(b) for $v_{\rm id}$ and $v_{\rm xo}$, i.e., $1.3\times$ and $1.2\times$, respectively. This indicates that biaxial compressive strain is not as beneficial for hole velocity as it is for hole mobility. In the context of hole velocity, the simulated result in Fig. 10 predicts that uniaxial stress in SiGe is required to significantly outperform relaxed Si.

Enhanced hole velocity characteristics have been reported for Si channel p-MOSFETs with applied uniaxial compressive stress [4]. The simulation results in Fig. 10 predict that the ballistic velocity enhancement for Si will saturate around $2.7\times$. A substantial increase in the ballistic velocity is predicted with the incorporation of Ge into the channel and the application of compressive uniaxial stress in the $\langle 110 \rangle$ direction. From Fig. 10, a strained-$Si_{0.45}Ge_{0.55}$ channel is expected to provide a $4.3\times$ velocity enhancement over relaxed Si with the application of -5 GPa of uniaxial stress. A pure Ge channel is predicted to outperform relaxed Si by $5.2\times$. This result indicates that, with appropriate strain, even a moderate concentration of Ge in the channel (50 at. %), which could ease integration issues relative to pure Ge, may provide substantial velocity improvement relative to a Si channel p-MOSFET.

V. Conclusion

Biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs with gate lengths down to 65 nm have been fabricated to explore

the merits of a strained-$Si_{0.45}Ge_{0.55}$ channel. Care was taken to avoid process steps that might alter or eliminate the strain in the channel. Hole mobility and velocity have been extracted and are benchmarked against a comparable Si control device. Devices with gate lengths in the range of 65–150 nm are observed to exhibit a 2.5× hole effective mobility enhancement over the Si control mobility. While a slight drop in mobility is observed as the gate length is reduced, the observed mobility enhancement is still substantial. Three velocity extraction methods were employed, and the velocity characteristics of scaled strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs have been documented. A modest 1.3× velocity enhancement is observed in biaxial compressive stained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs over control devices with a similar gate length and DIBL. While biaxial compressive strain in SiGe is very beneficial in providing a substantial mobility enhancement, it does not prove to be as beneficial to the carrier velocity. Band structure and ballistic velocity calculations indicate that a substantial enhancement in velocity can be expected with the incorporation of Ge into the channel and the addition of uniaxial stress. While the velocity enhancement provided by uniaxial compressive stress in Si is expected to saturate at 2.7× relative to relaxed Si, simulations predict that a strained-$Si_{0.45}Ge_{0.55}$ channel will outperform relaxed Si by 4.3×. Moving to a pure Ge channel is predicted to provide a slightly higher performance gain at 5.2×. This suggests that even moderate amounts of Ge incorporated into the channel and combined with uniaxial compressive stress can provide a significant velocity enhancement over relaxed-Si channel p-MOSFETs.

ACKNOWLEDGMENT

The authors would like to thank G. Riggott, A. Khakifirooz, and J.-K. Lee for their assistance in completing this paper. The authors would also like to thank the Microsystems Technology Laboratory at MIT, Lemelson foundation, NSF, and FCRP MSD.

REFERENCES

[1] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layer Cu interconnects, low k ILD, and 1 μm^2 SRAM cell," in *IEDM Tech. Dig.*, 2002, pp. 61–64.

[2] M. Uchida, Y. Kamakura, and K. Taniguchi, "Performance enhancement of pMOSFETs depending on strain, channel direction, and material," in *Proc. Int. Conf. Simul. Semicond. Process. Devices*, 2005, pp. 315–318.

[3] H. M. Nayfeh, S. Jeng, S. Narasimha, S. Butt, R. Pal, A. Waite, K. Tabakman, J. B. Johnson, J. Liu, J. Holt, T. Adam, A. Madan, and A. Domenicucci, "Hole transport in nanoscale p-type MOSFET SOI devices with high strain," in *Proc. Device Res. Conf.*, 2007, pp. 51–52.

[4] A. Khakifirooz and D. A. Antoniadis, "Transistor performance scaling: The role of virtual source velocity and its mobility dependence," in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[5] D. A. Antoniadis and A. Khakifirooz, "MOSFET performance scaling: Limitations and future options," in *IEDM Tech. Dig.*, 2008, pp. 253–256.

[6] T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nishi, and K. Saraswat, "Low defect ultra-thin fully strained-Ge MOSFET on relaxed Si with high mobility and low band-to-band-tunneling," in *VLSI Symp. Tech. Dig.*, 2005, pp. 82–83.

[7] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 97, no. 1, pp. 1–27, Dec. 2005.

[8] G. Nicholas, B. De Jaeger, D. P. Brunco, P. Zimmerman, G. Eneman, K. Martens, M. Meuris, and M. M. Heyns, "High-performance deep submicron Ge pMOSFETs with halo implants," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2503–2511, Sep. 2007.

[9] O. Weber, Y. Bogumilowicz, T. Ernst, J.-M. Hartmann, F. Ducroquet, F. Andrieu, C. Dupre, L. Clavelier, C. Le Royer, N. Cherkashin, M. Hytch, D. Rouchon, H. Dansas, A.-M. Papon, V. Carron, C. Tabone, and S. Deleonibus, "Strained Si and Ge with high-k/metal gate stack for high mobility dual channel CMOS," in *IEDM Tech. Dig.*, 2005, pp. 137–140.

[10] T. Yamamoto, Y. Yamashita, M. Harada, N. Taoka, K. Ikeda, K. Suzuki, O. Kiso, N. Sugiyama, and S. Takagi, "High-performance 60 nm gate length germanium p-MOSFETs with Ni germanide metal source/drain," in *IEDM Tech. Dig.*, 2007, pp. 1041–1043.

[11] S. W. Bedell, A. Majumdar, J. A. Ott, J. Arnold, K. Fogel, S. J. Koester, and D. K. Sadana, "Mobility scaling in short-channel length strained Ge-on-insulator P-MOSFETs," *IEEE Electron Device Lett.*, vol. 29, no. 7, pp. 811–813, Jul. 2008.

[12] C. Ni Chleirigh, X. Wang, G. Rimple, Y. Wang, N. D. Theodore, M. Canonico, and J. L. Hoyt, "Super critical channel thickness SiGe-channel heterostructure p-type metal-oxide-semiconductor field-effect transistors using laser spike annealing," *J. Appl. Phys.*, vol. 103, no. 10, pp. 4501–4503, May 2008.

[13] Y. C. Yeo, Q. Lu, T. J. King, C. Hu, T. Kawashima, M. Oishi, S. Mashiro, and J. Sakai, "Enhanced performance in sub-100 nm CMOSFETs using strained epitaxial silicon-germanium," in *IEDM Tech. Dig.*, 2000, pp. 753–756.

[14] Z. Shi, D. Onsongo, R. Rai, S. B. Samavedam, and S. K. Banerjee, "Hole mobility enhancement and Si cap optimization in nanoscale strained $Si_{1-x}Ge_x$ PMOSFETs," *Solid State Electron.*, vol. 48, no. 12, pp. 2299–2306, Dec. 2004.

[15] F. Andrieu, T. Ernst, O. Faynor, Y. Bogumilowicz, J.-M. Hartmann, J. Eymery, D. Lafond, Y.-M. Levaillant, C. Dupre, R. Powers, F. Fournel, C. Fenouillet-Beranger, A. Vandooren, B. Ghyselen, C. Mazure, N. Kernevez, G. Ghibaudo, and S. Dleonibus, "Co-integrated dual strained channels on fully depleted sSDOI CMOSFETs with HfO_2/TiN gate stack down to 15 nm gate length," in *Proc. IEEE Int. SOI Conf.*, 2005, pp. 223–225.

[16] F. Andrieu, T. Ernst, F. Lime, F. Rochette, K. Romanjek, S. Barraud, C. Ravit, F. Boeuf, M. Jurczak, M. Casse, O. Weber, L. Brevard, G. Reimbold, G. Ghibaudo, and S. Deleonibus, "Experimental and comparative investigation of low and high field transport in substrate- and process-induced strained nanoscaled MOSFETs," in *VLSI Symp. Tech. Dig.*, 2005, pp. 176–177.

[17] G. Hu, C. Chang, and Y.-C. Chia, "Gate-voltage-dependent effective channel length and series resistance of LDD MOSFETs," *IEEE Trans. Electron Devices*, vol. ED-34, no. 12, pp. 2469–2475, Dec. 1987.

[18] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 43–46.

[19] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selma, and E. Sangiorgi, "Low field electron and hole mobility of SOI transistors fabricated on ultrathin silicon films for deep sub-micrometer technology applications," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2842–2850, Dec. 2001.

[20] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductance of FETs," *IEEE Trans. Electron Devices*, vol. ED-34, no. 2, pp. 448–450, Feb. 1987.

[21] A. Lochtefeld and D. A. Antoniadis, "On experimental determination of carrier velocity in deeply scaled NMOS: How close to the thermal limit?," *IEEE Electron Device Lett.*, vol. 22, no. 2, pp. 95–97, Feb. 2001.

[22] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," *J. Appl. Phys.*, vol. 80, no. 4, pp. 2234–2253, Aug. 1996.

[23] H. Hu, J. B. Jacobs, L. T. Su, and D. A. Antoniadis, "A study of deep-submicron MOSFET scaling based on experiment and simulation," *IEEE Trans. Electron Devices*, vol. 42, no. 4, pp. 669–677, Apr. 1995.

[24] $nextnano^3$, Munich, Germany: NEXTNANO, 2007. [Online]. Available: http://www.nextnano.de/

[25] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 361–363, Jul. 1997.

[26] Purdue Univ., FETtoy 2.0, nanoHUB, West Lafayette, IN, 2008. [Online]. Available: https://nanohub.org/tools/fettoy/wiki

Leonardo Gomez received the B.S. degree in electrical engineering from the University of South Florida, Tampa, in 2004. He has been working toward the Ph.D. degree in the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (MIT), Cambridge, since 2004.

He has been a Graduate Research Fellow with the National Science Foundation and a Presidential Fellow with MIT. He is currently with the Microsystems Technology Laboratories, MIT. His primary research interests are in the areas of carrier transport in Si/Ge-based MOSFETs, Si/Ge epitaxy, and advanced CMOS processing techniques.

Pouya Hashemi (S'05) received the B.Sc. and M.Sc. degrees in electrical engineering (both with highest honors) from the University of Tehran, Tehran, Iran, in 2003 and 2005, respectively. He is currently working toward the Ph.D. degree in electrical engineering and computer science at the Massachusetts Institute of Technology (MIT), Cambridge.

From 2002 to 2005, he was with the Thin-Film Research Laboratories, University of Tehran, working on electrical and optical properties of nanocrystalline silicon and fabrication of low-temperature silicon and germanium thin-film transistors on flexible substrates. In 2005, he joined the MIT Microsystems Technology Laboratories, where his current research focuses on fabrication and investigation of carrier transport in nanoscale strained SOI, silicon germanium, and germanium channel CMOS devices with planar and nanowire architectures. In summer 2009, he was with the IBM T. J. Watson Research Center, Yorktown Heights, NY, working on multicrystalline silicon-based photovoltaics.

Mr. Hashemi is a Student Member of the IEEE Electron Devices Society and the Material Research Society. He was the recipient of the IBM Ph.D. Fellowship award in 2008.

Judy L. Hoyt (M'83–SM'06–F'08) received the B.S. degree in physics and applied mathematics from the University of California, Berkeley, in 1981 and the Ph.D. degree in applied physics from Stanford University, Stanford, CA, in December 1987.

From 1988 to 1999, she was a member of the Research Staff with the Department of Electrical Engineering, Stanford University. Since January 2000, she has been with the faculty of the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology (MIT), Cambridge. She is also currently with the Microsystems Technology Laboratories, MIT. Her primary research interests are in the areas of silicon-based heterostructure devices and technology, Si epitaxy, and CMOS front-end processing. She has authored or coauthored over 130 publications in these areas and is the holder of six patents.

Dr. Hoyt is a member of the American Physical Society and the Materials Research Society. She has served as the General Chair of the IEEE International Electron Devices Meeting in 2001.