# *A 32-mu W 1.83-kS/s Carbon Nanotube Chemical Sensor System*

# A 32-$\mu$W 1.83-kS/s Carbon Nanotube Chemical Sensor System

Taeg Sang Cho, *Student Member, IEEE*, Kyeong-Jae Lee, *Student Member, IEEE*, Jing Kong, and Anantha P. Chandrakasan, *Fellow, IEEE*

***Abstract*—This paper presents an energy-efficient chemical sensor system that uses carbon nanotubes (CNT) as the sensing medium. The room-temperature operation of CNT sensors eliminates the need for micro hot-plate arrays, which enables the low energy operation of the system. An array of redundant CNT sensors overcomes the reliability issues incurred by the CNT process variation. The sensor interface chip is designed to accomodate a 16-bit dynamic range by adaptively controlling an 8-bit DAC and a 10-bit ADC. A discrete optimization methodology determines the dynamic range of the DAC and the ADC to minimize the energy consumption of the system. A simple calibration technique using off-chip reference resistors reduces the DAC non-linearity. The sensor interface chip is designed in a 0.18-$\mu$m CMOS process and consumes, at maximum, 32 $\mu$W at 1.83 kS/s conversion rate. The designed interface achieves 1.34% measurement accuracy across the 10 k$\Omega$–9 M$\Omega$ range. The functionality of the full system, including CNT sensors, has been successfully demonstrated.**

***Index Terms*—Carbon nanotube (CNT), chemical sensor system, low power, sensor interface.**

## I. Introduction

THE advancement in wireless microsensor networks facilitates a real-time monitoring of environment in both natural and industrial settings [1]. Both industry and government have shown interests towards monitoring air for hazardous chemical detections and bio-chemical attack preventions in particular. To design a reliable chemical sensor system suited for wireless microsensor applications, three requirements should be met: the designed system should be stable, cheap and ultra-low power.

Recently, a number of sensing methods based on nano-materials have emerged [2]–[6]. Interestingly, many of these sensors change resistance when exposed to the chemical of interest. To reflect this trend, many low-power CMOS platforms are introduced to read the resistance of sensors, from which the chemical concentration can be estimated [7]–[11]. The CMOS interface should exhibit a good linearity in the resistance measurement to reliably estimate the chemical concentration. A number of published work in literature integrated both the sensor and CMOS interface on a single chip [8]–[10], aimed at low-cost portable sensor applications.

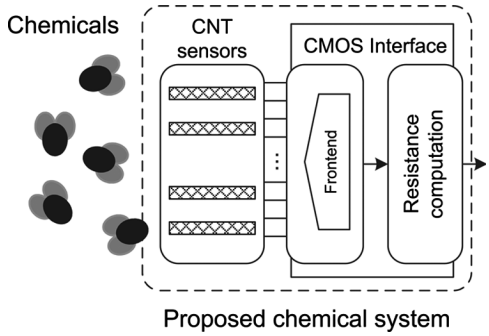



Fig. 1. The proposed chemical sensor system.

Current approaches, which rely on micro-hotplate, consume milli-watts of power. To make circuits compatible with $\mu$-power sensor networks, the power consumption must be significantly reduced. The primary source of power consumption is the micro-hotplate. New sensing mediums exhibit high sensitivity and selectivity typically only at elevated temperatures ($\sim$300 °C), and several milliwatts are required for the CMOS platforms to stably provide the heat. Another source of power consumption has been the use of operational amplifiers (op-amps). Due to the process variation, the static resistance of sensors typically varies $2 \sim 3$ orders of magnitudes [7]. The interfaces should accomodate such a large dynamic range in addition to sensing small resistance changes due to chemical exposures. While op-amps increase the accuracy of the resistance measurement and the dynamic range, the high gain in op-amps results in a relatively high power consumption.

This paper extends upon the state-of-the-art by presenting an ultra-low power chemical sensor system consuming 32 $\mu$W using carbon nanotubes (CNTs) as the chemical sensing medium [12]. The main contribution of this work can be summarized as the following:

- the development of a low-power chemical sensor system.
- the characterization of the carbon nanotube impedance variation.
- the design of the CMOS interface chip that accomodates a 16-bit dynamic range.

The prototype system comprises of a CMOS interface chip and a CNT sensor chip (Fig. 1). An array of redundant CNT sensors is used to stably sense the chemical in the presence of CNT process variation. Section II briefly discusses the performance

Manuscript received February 14, 2008; revised September 08, 2008. Current version published January 27, 2009. This work was supported by the Interconnect Focus Center, one of five research centers funded under the Focus Center Research Program, a Semiconductor Research Corporate Program. The work of T. S. Cho was partially funded by Samsung Scholarship. The work of K.-J. Lee was partially funded by Intel.

The authors are with the Microsystems Technology Laboratories, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: taegsang@mit.edu).

Digital Object Identifier 10.1109/JSSC.2008.2010805

and fabrication of CNT sensors. Section III presents the architecture employed in this work, along with detailed description of energy optimization methodologies. Section IV describes the circuit techniques and system control strategies. The paper concludes with measurement results and discussions.

## II. Carbon Nanotube Chemical Sensors

Chemical sensors based on single-walled CNTs were first demonstrated independently by Kong and Collins [6], [13], and since then CNTs have gathered tremendous interest for use in chemical and biological sensing applications. CNT sensors are typically fabricated using either isolated CNT or thin films. While most studies achieve high sensitivity through resistive sensing, capacitance sensing of CNT thin films has proven to be effective for vapors at low pressures [14], [15]. In this study, the resistance change of CNT FETs is monitored as the sensors are exposed to $NO_2$, a toxic gas released in industrial processes and automotive emissions. $NO_2$ was used since CNT's characteristics under $NO_2$ are well established [6].

### A. Sensor Response

Unlike other conventional sensing methods, CNTs are highly sensitive even at room temperature, which eliminates the need for a micro-hotplate. Also, all the atoms of a CNT are exposed on the surface, which allows miniaturization and means for chemical coating to achieve high selectivity to specific chemical agents. However, current fabrication methods generally yield CNTs with large resistance variations. Furthermore, CNT sensors exhibit fast response but slow recovery time to gases. While active heat or UV treatment can accelerate the long recovery time, such schemes cannot be implemented to maintain low power.

Two different sensing mechanisms have been proposed in literature for CNT FETs. The first mechanism suggests that charge transfer occurs between the CNT and the gas molecules that adsorb on the CNT surface [16], which then gives rise to a change in carrier density and thus affects the CNT channel resistance. The second mechanism resorts to the modification of the Schottky barrier (SB) at the metal-CNT contacts due to the adsorption of molecules on both the metal and the CNT. Experimental work shows that gas adsorption on the metal contacts can alter the work function of the metal, thus affecting the energy alignments at the junction leading to the change in SB height [17], [18].

The relative strengths of the surface interaction between the gas molecule and the metal/CNT will determine which effect dominates the sensor response. In particular, the CNT sensor response to $NO_2$ has been widely studied but experimental results suggest conflicting conclusions [6], [19]–[21]. $NO_2$ is widely regarded to withdraw electrons when adsorbed on the CNT surface. Since chemically intrinsic CNT FETs are dominated by hole transport, the $CNT - NO_2$ interaction effectively increases the CNT channel conductance (or decreases resistance). While such charge transfer doping has been clearly indicated [6], the $NO_2$ sensing response appears to be dominated by the SB change at the metal contact [22].

Depending on the electron withdrawing nature of the analyte, a number of gases may show sensing responses similar to that of $NO_2$. For example, while CO molecules show no sensing response, $NO_2$ and $SO_2$ molecules show similar responses. Thus, simple devices such as those presented here have limited selectivity and further means of chemical modification are required. Poly-ethyleneimine coating of single-walled CNT sensors has been shown to impart selectivity to $NO_2$ and block other molecules [19]. Other polymer coatings, such as chlorosufonated poly-ethylene and hydroxypropyl cellulose have been used to implement sensing for $Cl_2$ and HCl species [23]. Characterizing such methods is beyond the scope of this paper. In this work, a controlled study of $NO_2$ sensing is used as a benchmark for testing the overal system performance in the presence of CNT device variations.

### B. Device Characterization

In this work, an array of 24 single-walled CNT FETs is fabricated on a p-type silicon wafer with a thin layer of thermal oxide on top. First, a metal layer (Ti/Pt) is deposited to provide large pads for probing and to align CNT growth in subsequent steps. After patterning and depositing islands of Fe/Mo-based catalyst, CNTs are grown via chemical vapor deposition (CVD), using a $CH_4$ gas source at 900 °C [24]. Finally, a second metal layer (Cr/Au) is deposited to achieve good electrical contact to the nanotubes. Fig. 2 shows the CNT FET structure (4-$\mu$m channel, Cr/Au contacts) and the distribution of resistance, exhibiting a spread across 6 orders of magnitude. This distribution results from one of the most critical and challenging aspects of CNT fabrication: the number of CNTs between the electrodes of each device can vary, the CNTs can be either metallic or semiconducting, where semiconducting CNT FETs have a diameter-dependent band gap, and lastly, the contact resistance between each CNT and metal vary as well.

The CNT array is used as grown (i.e., without any additional treatment.) While the large dynamic range poses circuit challenges, using an array of sensors as opposed to single devices can effectively increase the reliability of gas detection and identification. Fig. 3 shows the linear relation between the resistance change and the initial baseline resistance. This linearity can be parameterized for gas concentration estimation. Furthermore, the as-grown array allows systematic studies of the resistive properties of CNT FETs over a wide range, and highlights the need for variation-tolerant circuit interfaces. Further details of the CNT sensor device can be found in [22].

Fig. 4 shows the transient response of a CNT device in response to $NO_2$ under different gate voltages. A decrease in resistance is clearly visible. The response time for a device under zero gate voltage is rather slow and generally observed to be above 10 minutes for concentrations between 10–100 ppm. Conducting sensor experiments while applying a positive gate voltage significantly improved the response time to within several minutes, which is consistent and comparable to CNT sensors reported in [6] and [20]. Kong *et al.* used single semiconducting CNTs with a positive gate voltage that showed very fast response times on the order of a minute. However, devices with many CNTs showed longer response times to $NO_2$. Furthermore, the concentration of $NO_2$ may gradually

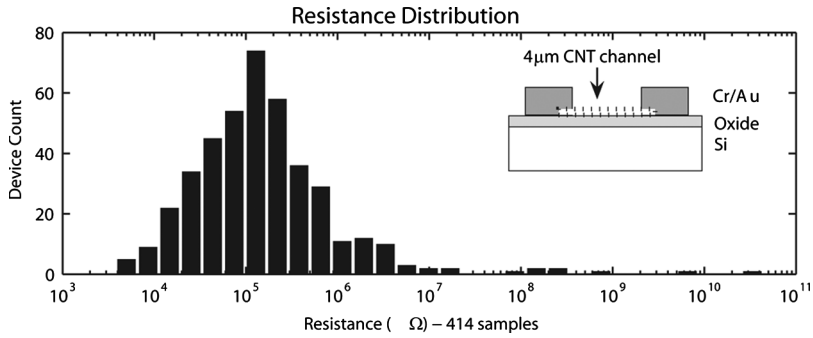



Fig. 2. Measured data on the distribution of CNT resistance from 414 devices. inset: CNT-FET sensor diagram.

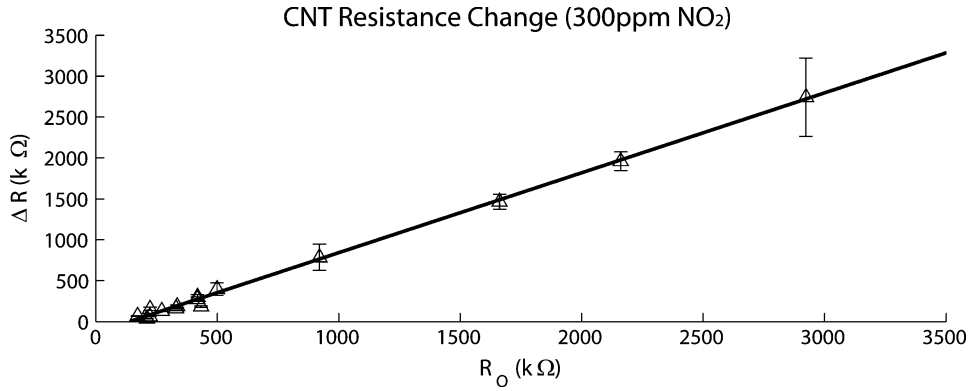



Fig. 3. Experimental data on the linear dependence on $\Delta \mathrm{R} - \mathrm{R}_0$.

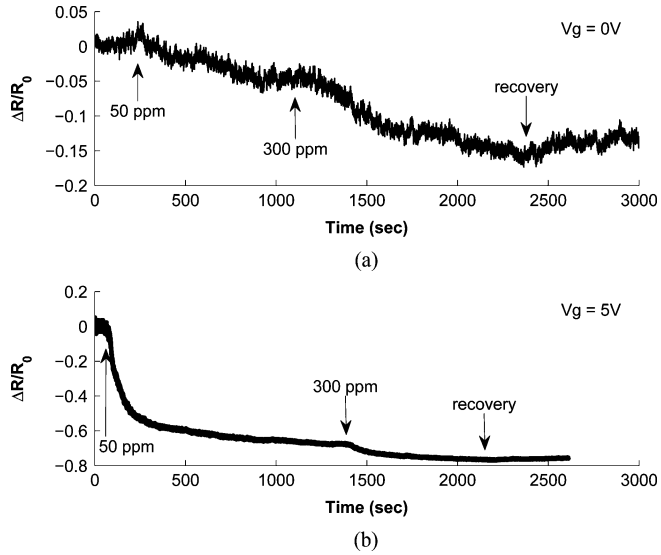



Fig. 4. Transient response of a CNT device in response to 50 ppm and 300 ppm $NO_2$ with (a) zero gate voltage and (b) a positive gate voltage (5 V) applied. CNT conductance measurements were made with custom-built equipment.

change within a large chamber, which can also increase the sensor repsonse time [21].

To interface to the CNT sensor array, the front-end circuit needs to address a wide resistance range, effectively defined as 10 k$\Omega$–9 M$\Omega$. In addition, the CNT resistance should be measured with a precision near 2% to detect $NO_2$ in the sub-ppm range, which results in a 16-bit dynamic range ($R_{LSB} = 182\ \Omega$).

## III. CMOS Interface Architecture

The limited power budget and the required large dynamic range renders the design of the CMOS interface a non-trivial task. Previous designs [7], [11] have resorted to using op-amps to increase the dynamic range of the interface, but can result in higher power consumption. Therefore, we introduce an architecture that does not require an op-amp. The proposed architecture meets these goals by delegating the large dynamic range requirement to two simpler analog blocks of lower dynamic range and lower power. We also extensively clock-gate the entire chip in order to further reduce the power consumption through duty-cycling.

### *A. Architecture*

The basic idea of the architecture is to source a predetermined known current to the CNT sensors, and read the resulting voltage. This concept is attractive because the interface can change the resistance measurement resolution by changing the input current as the following:

$$R_{LSB} = \frac{V_{LSB}}{I_{INPUT}}. \tag{1}$$

Also, the current source can easily be time-multiplexed to access multiple sensor channels (Fig. 5): while the effective read-out rate for each sensor is reduced by a factor of the number of sensors connected to the chip, we show that the read-out rate of the system is fast enough to accomodate the minimum required read-out rate per sensor.

Equation (1) signifies that in order to increase the resistance measurement accuracy (i.e., low $R_{LSB}$), the interface should

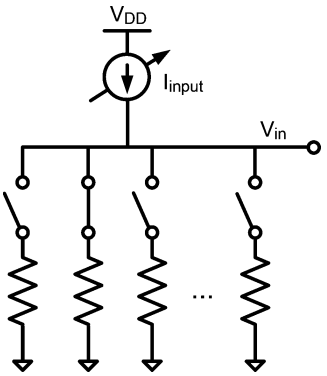



Fig. 5. The basic concept of the developed system. By applying a known amount of current to an unknown resistor, and measuring the voltage across the resistor, the resistance can be calculated with Ohm's law.

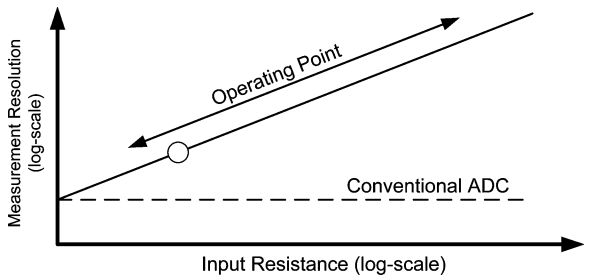



Fig. 6. The current control, in effect, modifies the minimum resolvable resistance to expand the dynamic range.

increase the input current ($I_{INPUT}$). However, we cannot indefinitely increase ($I_{INPUT}$) for three reasons: large input current signifies that the power consumption of the system is large; the maximum current through a single CNT should be less than 30 $\mu$A; a certain voltage headroom should be kept across the current source to guarantee the linearity. This suggests that the interface requires an adaptive input current control scheme.

To balance the resistance measurement resolution and the design constraints, the following control strategy is employed: if $V_{in}$ is large, reduce the input current, whereas if $V_{in}$ is small, increase the input current. Section IV-B studies the implementation details. The current control, in effect, is changing the minimum resolvable resistance for each resistance level of interest to expand the dynamic range, as illustrated in Fig. 6. This can be contrasted with the conventional ADC with a fixed current source, where the minimum resolvable resistance is fixed.

Fig. 7 shows the architecture employed in the current design, comprised of an ADC, a variable current source and a digital controller. Note that if the dynamic range of the ADC and the DAC is $N$ bits and $M$ bits, respectively, the dynamic range of the whole system is $N+M$ bits. For this chip, two extra bits are added to the required 16-bit dynamic range to enable a digital DAC calibration.

A successive approximation register (SAR) ADC is chosen for this work because the only circuit blocks that draw static current are the preamplifiers in the comparator. The preamplifiers are gated when the ADC is turned off to further save power [25]. Also, a sub-DAC configuration is used for the capacitor DAC in order to save die area [25].

The variable current source ($I_{INPUT}$) is implemented using a current steering DAC: The current source can be controlled with digital words rather than an analog voltage. A thermometer—code configuration of a current steering DAC is used to better match the DAC cells in the presence of process variations. The minimum current from the current source ($I_{LSB}$) is determined by the largest resistance to measure and the required voltage headroom for the DAC linearity (in this implementation, 0.3 V headroom is guaranteed across the DAC.) To measure 9 M$\Omega$ with 0.9 V voltage swing available at the ADC input node, 100 nA is chosen as the minimum current.

The digital controller block (Fig. 8) serves three purposes: calibrating the non-linearity of the DAC, adaptively controlling the DAC current as the resistance changes, and controlling the ADC operation. The designed chip interfaces to 24 CNT sensors, which are sequentially time-multiplexed through a 32:1 CNT multiplexer. Extra ports in the 32:1 multiplexer are used for off-chip reference resistors (Section IV-C.) Unlike Grassi *et al.* [7], this chip does not dedicate a full readout system per channel by time-multiplexing the readout system.

There are two operational modes in this chip: the DAC calibration mode and the resistance measurement mode. In the calibration mode, the reference resistors are accessed, instead of CNT sensors, to calibrate any current error present in the DAC. In the resistance measurement mode, the analog blocks are duty-cycled to reduce the power consumption: When the DAC is sourcing current to a CNT sensor, the ADC is turned off until the voltage across the sensor becomes stable; when the ADC is converting, the DAC is turned off since the analog voltage across the CNT sensor no longer needs to be sustained.

The operation of the system can be summarized:

- The DAC sources current to the CNT of interest.
- Once the voltage at the input of the ADC settles, the ADC samples the voltage onto the capacitor DAC and computes the voltage.
- The resistance computation block uses the measured voltage, DAC current setting, and the calibration word to compute the resistance.

### *B. Architecture Optimization*

For circuit blocks that do not require high analog gains and high computing performance, voltage scaling can be an effective solution to reduce the power consumption of the chip [26]. Therefore, the supply voltages in analog and digital domains are scaled to 1.2 V and 0.5 V, respectively. While low supply voltage in the analog domain severely limits the available dynamic range and poses sheer constraints on the required precision of the analog circuit blocks, on-chip calibration, as well as careful design, alleviates problems associate with it.

Given an 18-bit dynamic range requirement, allocating the dynamic range to two analog sub-blocks is underconstrained. This can be understood by the fact that the 5-bit ADC/13-bit DAC pair and the 10-bit ADC/8-bit DAC pair both attain 18 bits of dynamic range. This work constrains the problem by designing the interface to attain optimum energy performance. Energy consumed per resistance conversion can be represented as

$$E_{OP} = P_{ADC} \times T_{ADC} + P_{DAC} \times T_{DAC} + E_{DIGITAL} \quad (2)$$

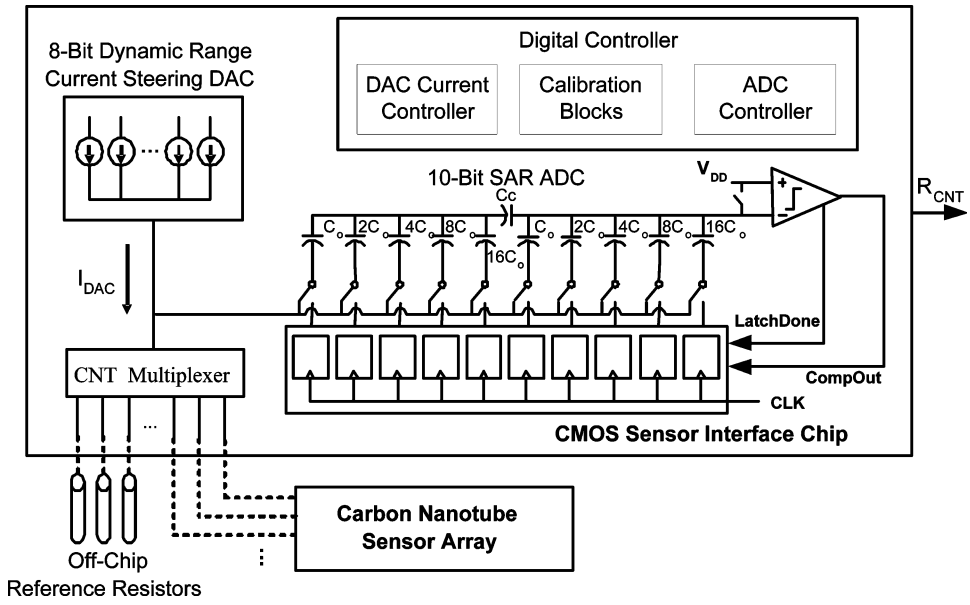



Fig. 7. The interface architecture with an on-chip calibration functionality.

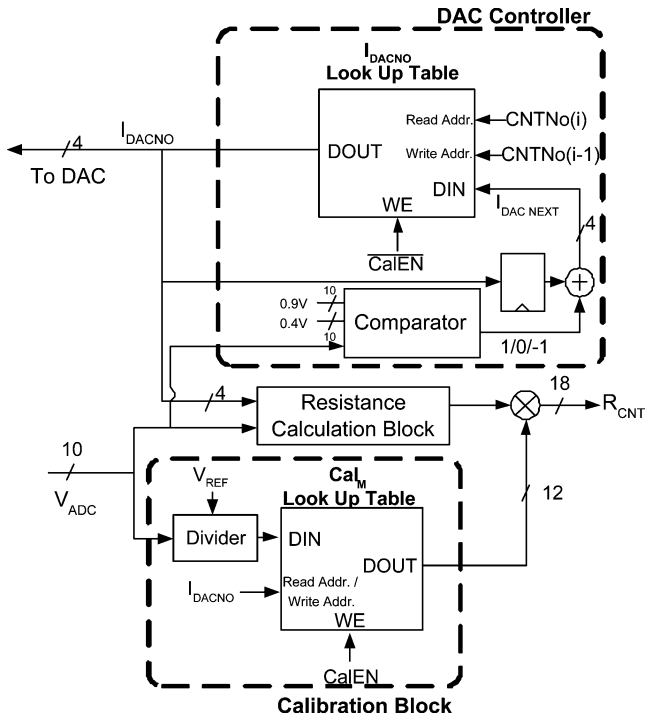



Fig. 8. A block diagram illustrating the critical dataflow in the digital controller.

where $P_{ADC}$ and $P_{DAC}$ are the power consumed by ADC and DAC respectively, and $T_{ADC}$ and $T_{DAC}$ are the on-period of ADC and DAC, respectively. The objective of the optimization is to minimize $E_{OP}$ as $N$ varies, where $N$ is the number of bits allocated to the ADC.

In the case of the SAR ADC, $T_{ADC}$ can simply be modeled as $N \times T_{CLK}$, the amount of time needed for one voltage conversion operation. Modeling $T_{DAC}$ is not as straightforward because it is in general a function of $N$ and parasitic capacitances at the ADC input node. When the ADC is $N$ bits, the signal present at the ADC input node should also have at least $N$-bit precision. Thus,

$$T_{DAC} \geq R_{INPUT} \times C_{INPUT} \times \ln(2^N) \tag{3}$$

where $R_{INPUT}$ and $C_{INPUT}$ are the effective resistance and capacitance looking into the ADC input node from the current steering DAC. $R_{INPUT}$ is roughly the CNT resistance, while $C_{INPUT}$ can be approximated by the sum of capacitances from the capacitor DAC in the ADC and the parasitic capacitance at the input signal node. The sub-DAC implementation is assumed for the capacitor DAC in the ADC. The parasitic capacitance $(C_{par})$ at the input signal node is assumed to be 3 pF (derived from on a simple model of the testing setup.)

$P_{ADC}$ is extrapolated from the figure-of-merit (FOM) of typical low speed ADCs. Assuming 20 kS/s operation with an FOM of 250 fJ/conversion step, $P_{ADC} = 5 \times 10^{-9} \times 2^{N+1}$. Since $I_{LSB}$ is 100 nA, the DAC power $P_{DAC} = 100\,\mathrm{nA} \times 2^{(18-N)} \times 1.2\ \mathrm{V}$.

The algorithm sweeps $N$ from 4 to 15 based on these models to determine the optimal $N$. The energy plot is shown in Fig. 9(a): the energy per conversion achieves a broad optimum around $N = 11$. However, designing a single-ended 11-bit ADC is not a trivial task, and the penalty paid by using a 10-bit ADC instead is only 17%. Thus, a 10-bit ADC is used in this work.

To examine how the parasitic capacitance at the ADC input node affects the optimal $N$, we swept the $C_{par}$ from 0.3 pF to 4.7 pF for $N = 10,\ 11,\ 12$. The energy plot is shown in Fig. 9(b). Note that assigning 10 bits to the ADC can actually be the optimum design choice when the parasitic capacitance is small.

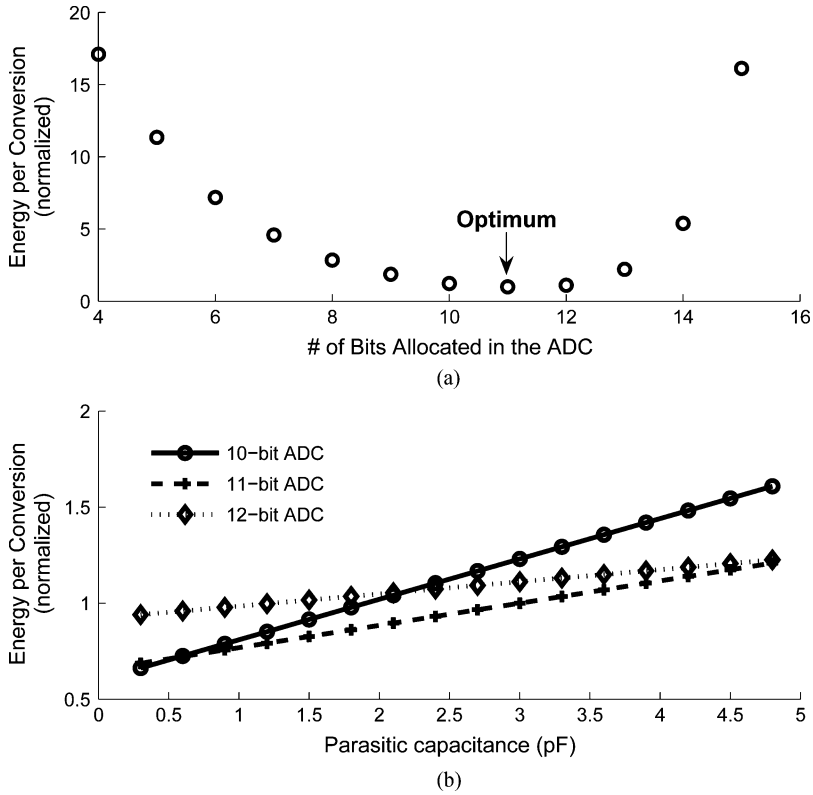



Fig. 9. (a) The energy consumed per resistance conversion as the ADC resolution changes. (b) The energy consumed per resistance conversion as a function of the parasitic capacitance at the ADC input node.

## IV. Circuit Design and Optimization

### A. DAC Cell Design

When designing a DAC cell, several things should be carefully evaluated. First of all, the trade-off between the small die area and the matching among the DAC cells has been considered one of the most important metrics in the DAC design [27]. While matching among the cells can be improved with common-centroid layout techniques [28], the intrinsic matching characteristics is limited by the area of the DAC cells [29]. Secondly, even when the DAC current is small, the total leakage current from the DAC cells should be negligible compared to the output current. Therefore, leakage reduction techniques, similar to the techniques applied to digital circuits [26], should be employed. We propose special DAC cells tailored to the employed current control scheme.

The DAC cells are shown in Fig. 10. Two types of DAC cells are used: the unit DAC cell sources 100 nA and the double DAC cell sources 200 nA. Consider the unit DAC cell. When the cell is on, $M_1$ and $M_2$ are biased with $V_c$ and $V_b$, respectively. While $M_2$ increases the output impedance of the DAC cell, it also performs as a switch (multiplexer). When the DAC cell is turned off, $V_c$ and $V_b$ are pulled up to $V_{DD}$, and this causes the internal node—connected to $M_2$ and $M_3$—to float. The leakage current through $M_2$ will, in turn, be $V_{INADC}$ dependent, degrading the linearity of the DAC. Thus, $M_3$ is added to hold the internal node to an internally biased voltage when the DAC cell is turned off. $M_3$ also reduces the leakage current through $M_2$ by reverse-biasing $M_2$. In a double DAC cell, the switch $(M_2)$ and the reverse biasing transistor $(M_4)$ are shared by two unit transistors ($M_1$ and $M_3$) to reduce the die area.

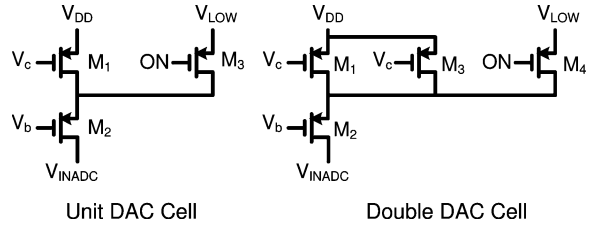



Fig. 10. Two types of DAC cells used in this work.

### B. DAC Control Schemes

While the DAC current control has to balance the resistance measurement resolution and other design criteria, the DAC current control is further complicated by the fact that several combinations of current and voltage can result in the same resistance value. In other words, many different input current levels can be used to read a certain resistance.

A possible method to circumvent such ambiguities is to source maximum input current while meeting the voltage headroom constraint. This allows the interface to attain the maximum measurement resolution as well. The maximum input current is only 25.6 $\mu$A, therefore the power consumption is not a severe issue. The current control scheme is further simplified by allowing only binary-weighted current from the DAC, making the current source a logarithmic DAC. In other words, the DAC output current can be one of nine levels

(100 nA, 200 nA, ..., 25.6 $\mu$A). The input current is denoted with 4-bit $I_{DACNO}$, which takes on the values 0–8 as current increases. Allowing the current levels to only binary multiples of minimum current has an additional benefit in that the chip can compute the resistance with simple register shift operations.

The DAC control scheme also has to handle resistance variations due to the chemicals: the current controller automatically adjusts the DAC output current for the next measurement based on the present resistance measurement (Fig. 8). If the voltage from the $ith$ sensor is greater than 0.9 V or less than 0.4 V, the comparator outputs $-1$ and 1, respectively. The output of the comparator is added to the $I_{DACNO}$ to update the look-up table for that particular $(ith)$ CNT's next measurement.

### C. DAC Current Calibration

The chip relies heavily on the ideal characteristics of the DAC and ADC to measure the exact resistance. However, process variations can deteriorate the linearity of the current-steering DAC and ADC. While a capacitor-based SAR ADC can be designed to exhibit a high linearity with careful layout techniques [25], the linearity of the current steering DAC may not be guaranteed in an analogous way since the DAC cells are biased in a subthreshold regime. Thus, a DAC current calibration technique is proposed to upperbound the DAC linearity error to 1% across the 100 nA–25.6 $\mu$A current range.

The current calibration scheme measures the exact current at each desired current levels by sourcing the current to known off-chip reference resistors and measuring the voltage across them. Then the chip stores the ratio of the desired current to the measured current—$I_{IDEAL}/I_{MEAS}$—in a look-up table, shown at the bottom of Fig. 8. This ratio is then multiplied by the resistance computed without calibration to obtain the calibrated resistance. The overhead (in terms of power, die area, and calibration time) of measuring the current is not significant since there are only nine current levels. The calibration is performed when the system is on, and whenever the operating environment changes (signalled externally with CalEN in Fig. 8).

The current calibration scheme can give rise to resistance non-linearity if the offset voltage in the ADC is significant [30]. Therefore, the ADC employs two preamplifiers in front of the latch to reduce the offset voltage. [30] further proves that the gain error of the ADC does not degrade the current calibration performance as long as the offset voltage is small.

### D. CNT Multiplexer Design

For small resistances near 10 k$\Omega$, the non-linear resistance of pass transistors in 32:1 multiplexer can cause linearity errors. To reduce the resistance of pass gates, the width of pass transistors can be increased. However, the width cannot be increased indefinitely due to possible leakage current through the pass gates when turned off. Thus, a special pass gate structure is introduced, which is shown in Fig. 11. The width of pass transistors are moderately large, and the gate of the pass transistors are voltage boosted with low leakage boosting circuit to reduce on-resistance. When the pass gate is turned off, the access transistor $M_2$ is reverse-$V_{GS}$ biased with $V_{DDL}$ to minimize the voltage-dependent leakage current through the pass transistors.

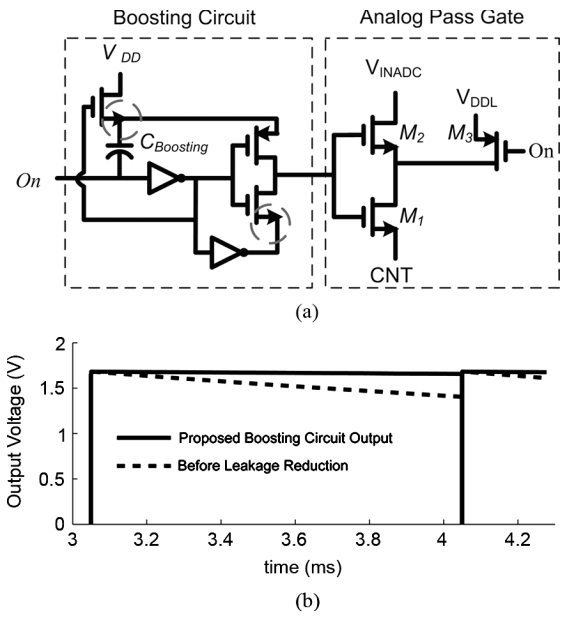



Fig. 11. (a) Proposed analog pass-gate structure (b) Boosting circuit simulation result.

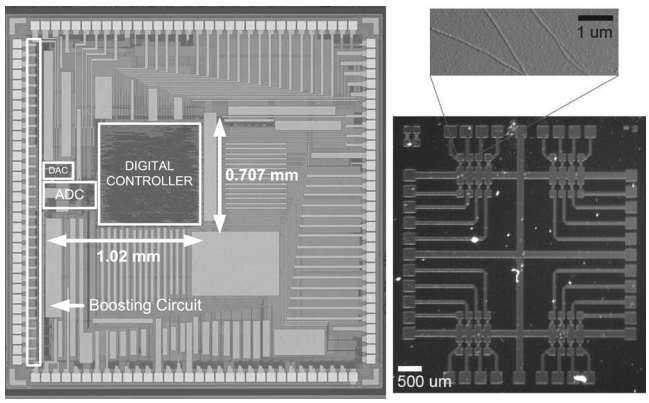



Fig. 12. Die photo of (a) the developed CMOS interface circuit, and (b) the CNT chemical sensor chip.

Note from Section III-B that DAC should be turned on for a long period to settle the voltage at the input of the ADC. This requires that the boosting circuit be able to sustained the boosted voltage for a long time. In this work, the boosting circuit is designed to sustain the high voltage for 1 ms (Fig. 11(b)) by blocking possible leakage paths (shown with dotted circles) with a reverse $V_{GS}$ bias. The boosted voltage is controlled to be less than the process limit of the technology (1.8 V) by choosing an appropriate $C_{Boosting}$[31].

## V. Chip Measurement Result

The CMOS interface chip was fabricated in a 0.18 $\mu$m CMOS process (Fig. 12(a)). $T_{DAC}$ of 512 $\mu$s was sufficient to provide 10-bit signal resolution at the input of the ADC, and was kept at 512 $\mu$s throughout testing. Table I summarizes the details of the chip.

Fig. 13 shows the effectiveness of the DAC calibration scheme. The testing setup fixes the bias voltage for the DAC cells, which may induce large current errors. However, DAC current error up to 8% can be calibrated down to less than 1.2%

TABLE I
STATISTICS OF THE CHIP

| Chip Specifications | |
|---|---|
| Process Technology | 180 nm |
| Active Area | $\sim$ 1.02 mm $\times$ 0.707 mm |
| Number of Pins | 128 Pins |
| Supply Voltage | 0.5 V (Digital) 1.2V (Analog) |

TABLE II
COMPARISON OF PUBLISHED SENSOR INTERFACE CIRCUITS

| | Meas. Error | Resistance Range | Readout Rate | Power Consumption |
|---|---|---|---|---|
| Malfatti *et al.*[8] | 0.5% > | $500K\Omega \sim 1G\Omega$ | Not Available | $3.1mW$ |
| Grassi *et al.*[7] | 0.14% > | $100\Omega \sim 20M\Omega$ | $100Hz$ | $6mW$ |
| Flammini *et al.*[11] | 0.5% > | $10K\Omega \sim 10G\Omega$ | Depends on Res. | $600mW$ |
| Frey *et al.*[35] | 0.2% > | $3K\Omega \sim 12M\Omega$ | $3kHz$ | $\sim 130mW$ |
| **This work** | **1.32% >** | **10KΩ ~ 9MΩ** | **1.83kHz** | **32$\mu$W** |

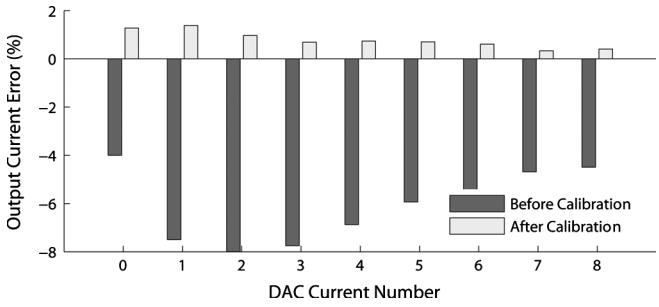



Fig. 13. The performance of the calibration scheme.

for every current level. The residual current error is suspected to be due to the mismatch among the reference resistors.

The resistance measurement error is less than 1.34% across the whole dynamic range (Fig. 14(a).) The primary sources of error are the DAC nonlinearity and the ADC nonlinearity. While the DAC nonlinearity appears as a piece-wise vertical shift of the resistance error curve, the nonlinearity of the ADC appears as the measurement error within the piece-wise shifted portion of the curve. The ADC error thus appears as the repeated spikes in Fig. 14(a). The INL and DNL of the designed ADC is $+1.34$LSB/$-1.2$LSB and $+0.46$LSB/$-0.22$LSB, respectively [30]. The ADC linearity error resulted primarily from capacitor mismatches and can be improved through a more careful layout.

Fig. 14(b) shows that the power dissipation of the designed interface scales linearly as the sampling rate reduces. Thus, the conversion operation can be gated when the measurement does not require a fine time resolution. A static power dissipation of 7.5 $\mu$W exists for the designed interface, which is mostly due to subthreshold leakage. The measurement in Fig. 14(b) was taken with random resistor samples, and is subjected to an increase based on the value of sensed resistances. In the worst case, when resistors all lie close to 10 k$\Omega$, the DAC is fully on for all CNTs, and 32 $\mu$W is consumed in total at 1.83 kS/s sampling rate.

Table II compares the performance of several chemical sensor interfaces and excludes the micro-hotplate power when applicable. Notice that the specification of the published interfaces varies greatly, thus a fair comparison of these interfaces remains a difficult task. Nonetheless, the power consumption of this work compares favorably with the state-of-the-art sensor interfaces.

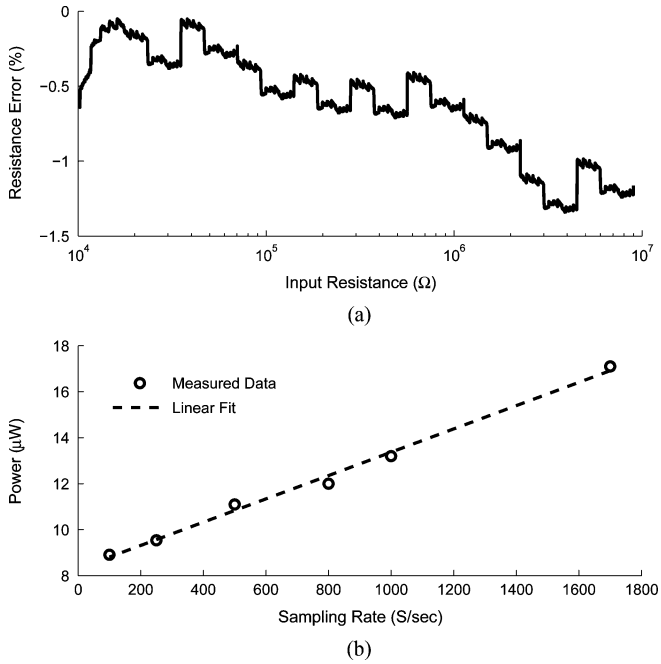



Fig. 14. (a) Measurement error across the entire dynamic range. (b) Power consumption as the conversion rate varies.

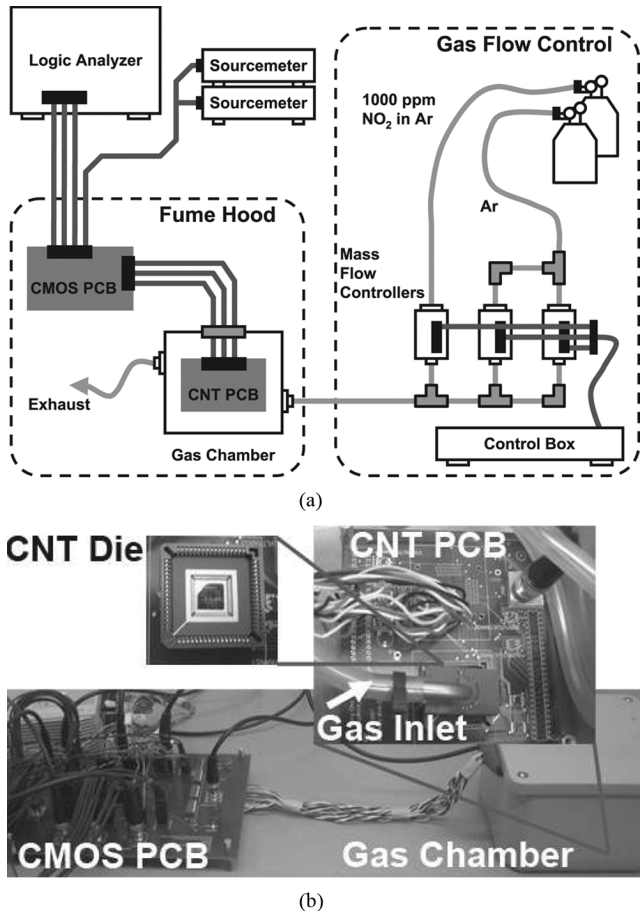



Fig. 15. (a) The equipment setup for the system demonstration. (b) A photo of the testing setup.

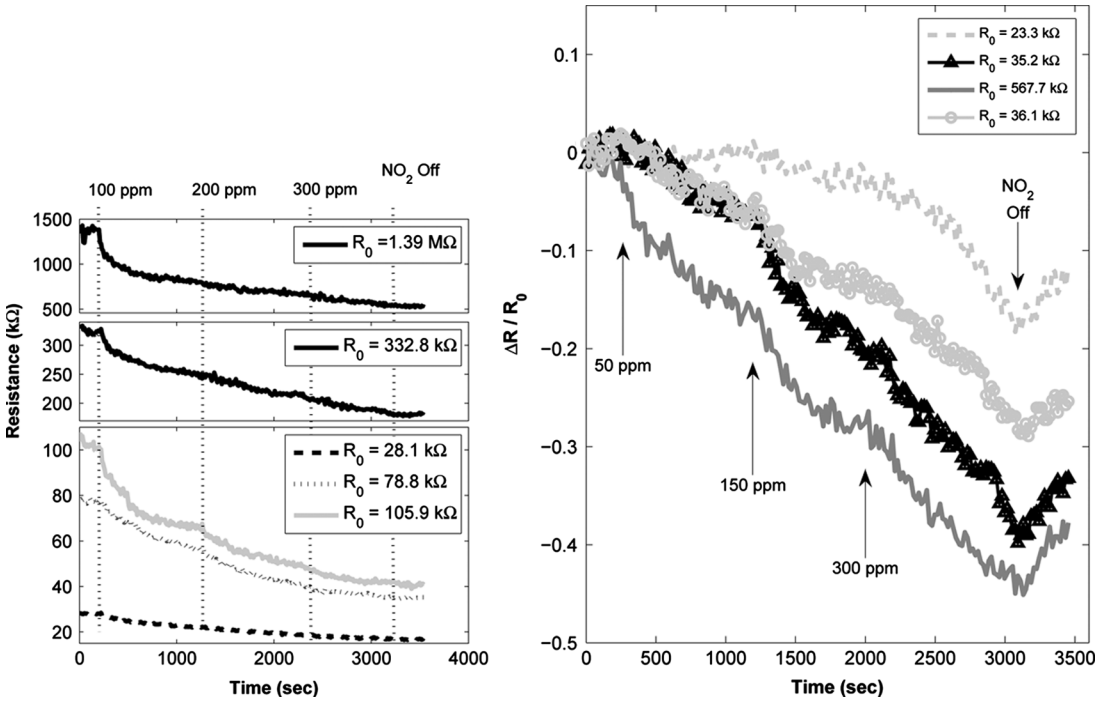



Fig. 16. The CNT resistance change detected with the interface circuitry. Experimental conditions (gas exposure time, chamber size, and device geometry) differ from that in Figs. 3 and 4. Two independent experiments with exposure to (a) 100 ppm, 200 ppm and 300 ppm $NO_2$ and (b) 50 ppm, 150 ppm, and 300 ppm $NO_2$.

## VI. Sensor System Result

### A. Test Setup

CNT chemical sensors and the interface chip is connected with a printed circuit board, and the functionality of the full system is tested by exposing the CNT sensors to varying concentrations of $NO_2$ in Ar. Fig. 15(a) shows a diagram of the equipment setup. The gas is introduced to the CNT sensors that sit in a gas chamber, and the measurement taken by the fabricated chip is acquired by a logic analyzer. A gas-flow control system is constructed to serve as a test vehicle for characterizing the CNT sensors with the CMOS interface chip. Each mass flow controller (MFC) has an independent control knob, and a total of three MFCs were used: two for the carrier gas (Ar) and one for the sensing gas ($NO_2$). The concentration of $NO_2$ is modulated by adjusting the flow rates of each gas. The maximum flow rate for the two MFCs for Ar differ by an order of magnitude to produce a broader range of gas concentrations. In addition, a pre-diluted mix of 1000 ppm $NO_2$ in Ar is used to achieve ppm-range concentrations. Due to practical limits of maximum flow rate and MFC control resolution, the effective concentration range is 600 ppb–1000 ppm. A varying mixture of $NO_2$ and Ar eventually flows into the sealed gas chamber, out through an outlet, and is dispersed in the chemical fume hood. The chamber is sealed and additional tubing is employed inside to ensure reliable delivery of the gas analytes to the CNT sensor chip (Fig. 15(b)). To accommodate the printed circuit board, a much larger gas chamber was used for system testing than that used for device characterization in Section II-B. All system measurements were taken with zero gate voltage.

### B. Measurement Results

Since the CNT sensors do not consume any active power, the total power consumption of the designed chemical sensor system is at maximum 32 $\mu$W, enabling deployment of the developed system in a sensor network environment. Fig. 16 shows the measured resistance values from the CMOS interface for two independent sensing experiments and thus verifies the real-time sensing operation of the entire system. The response time of the devices are well above 10 minutes. As discussed in Section II-B, the slow response time can be attributed to several factors. A large gas chamber is used here, which limits the response time of $NO_2$ to achieving the desired concentration in the chamber. In addition, zero gate voltage was applied to the devices, and the sensors fabricated here have varying mixtures of several semiconducting and metallic CNTs within each sensor device.

Fig. 16(a) shows a few sample devices using their absolute resistance values. The CMOS interface is able to read resistance values across the entire dynamic range (10 k$\Omega$–9 M$\Omega$). Fig. 16(b) compares the relative resistance change normalized by the initial base resistance. It is important to note that the characteristic of CNT sensors varies significantly from tube to tube. From Fig. 3, the $\Delta \mathrm{R} - \mathrm{R}_0$ curve is linear but does not pass through the origin due to a non-zero minimum value of the baseline resistance $R_0$. Hence, the magnitude of $\Delta R/R_0$ tends to be larger for larger values of $R_0$, which is reflected in Fig. 16(b). However larger deviations seem to exist from this trend for smaller values of $R_0$ because such devices are likely composed of multiple CNTs. Since the $NO_2$—CNT binding energy is known to vary depending on the type of CNT [32], devices with multiple CNTs tend to exhibit larger variations from the general trend. This justifies the use of multiple CNT sensor devices, which span across a wide dynamic range, to sense the

chemicals in the frontend. Standard pattern recognition and machine learning techniques can be used to estimate the chemical concentration from the resistance measurement data [33], [34].

## VII. Conclusion

This paper presents a low power chemical sensor system using carbon nanotubes as the sensing medium. Carbon nanotubes are passive sensing devices that attain high sensitivities even at room temperature, which enable aggressive power savings at the system level. The carbon nanotube sensors are interfaced by an energy efficient interface chip that attains a large dynamic range through automatic current control, along with on-chip digital calibration of analog components. The system overcomes the CNT sensor process variations by deploying multiple sensors to sense the chemical.

Future research should focus on developing a single-chip solution of the CNT chemical sensor system by including reference resistors on-chip and packaging carbon nanotubes on-die. Packaging carbon nanotubes on-die can be done by transferring grown carbon nanotubes to pads that are otherwise wire-bonded. The single chip solution will decrease the cost of the developed system, which will facilitate mass deployments.

## Acknowledgment

The authors would like to thank National Semiconductor for fabricating the chip, and D. Nezich for providing part of the CNT resistance data. This work was carried out in part through the use of MIT's Microsystems Technology Laboratories.

## References

[1] B. Calhoun, D. Daly, N. Verma, D. Finchelstein, D. Wentzloff, A. Wang, S.-H. Cho, and A. Chandrakasan, "Design considerations for ultra-low energy wireless microsensor nodes," *IEEE Trans. Computers*, vol. 54, p. 6, 2005.

[2] A. Sadek, S. Choopun, W. Wlodarski, S. Ippolito, and K. Kalantarzadeh, "Characterization of ZnO nanobelt-based gas sensor for $H_2$, $No_2$, and hydrocarbon sensing," *IEEE Sensors J.*, vol. 7, pp. 919–924, Jun. 2007.

[3] D. Q. Li, X. Wei Huang, S. L. Bai, G. J. Zhou, R. X. Luo, and A. F. Chen, "$CH_4$ sensor of Sn, In, and Ti nanosized oxides," *IEEE Sensors J.*, vol. 7, pp. 293–294, Feb. 2007.

[4] V. Filippov, A. Vasiliev, W. Moritz, and J. Szeponik, "Room-temperature hydrogen sensitivity of a MIS-structure based on the $Pt/LaF_3$ interface," *IEEE Sensors J.*, vol. 6, pp. 1250–1255, Oct. 2006.

[5] I. Sayago, M. D. C. Horrillo, S. Baluk, M. Aleixandre, M. J. Fernandez, L. Ares, M. Garcia, J. P. Santos, and J. Gutierrez, "Detection of toxic gases by a tin oxide multisensor," *IEEE Sensors J.*, vol. 2, pp. 387–393, Oct. 2002.

[6] J. Kong, N. Franklin, C. Shou, M. Chapline, S. Peng, K. Cho, and H. Dai, "Nanotube molecular wires as chemical sensors," *Science*, pp. 622–625, Jan. 2000.

[7] M. Grassi, P. Malcovati, and A. Baschirotto, "A 160 dB equivalent dynamic range auto-scaling interface for resistive gas sensor arrays," *IEEE J. Solid-State Circuits*, vol. 42, pp. 518–528, Mar. 2007.

[8] M. Malfatti, D. Stoppa, A. Simoni, L. Lorenzelli, A. Adami, and A. Baschirotto, "A CMOS nterface for a gas-sensor array with a 0.5% linearity over the 500 k$\Omega$-to-1 G$\Omega$ Range and $\pm 2.5\,^{\circ}$C temperature control accuracy," in *IEEE ISSCC Dig. Tech. Papers*, 2006.

[9] D. Barrettino, M. Graf, S. Taschini, S. Hafizovic, C. Hagleitner, and A. Hierlemann, "CMOS monolithic metal-oxide gas sensor microsystems," *IEEE Sensors J.*, vol. 6, pp. 276–286, Apr. 2006.

[10] D. Barrettino, M. Graf, W. H. Song, K. U. Kirstein, A. Hierlemann, and H. Baltes, "Hotplate-based monolithic CMOS microsystems for gas detection and material characterization for operating temperatures up to 500 C," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1202–1207, Jul. 2004.

[11] A. Flammini, D. Marioli, and A. Taroni, "A low-cost interface to high-value resistive sensors varying over a wide range," *IEEE Trans. Instrum. Meas.*, vol. 53, pp. 1052–1056, Aug. 2004.

[12] T. S. Cho, K.-J. Lee, J. Kong, and A. Chandrakasan, "A low power carbon nanotube chemical sensor system," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2007.

[13] P. Collins, K. Bradley, M. Ishigami, and A. Zettl, "Extreme oxygen sensitivity of electronic properties of carbon nanotubes," *Science*, vol. 287, no. 5459, pp. 1801–1804, 2000.

[14] E. Snow and F. Perkins, "Capacitance and conductance of single-walled carbon nanotubes in the presence of chemical vapors," *Nano Lett.*, vol. 5, no. 12, pp. 2414–2417, 2005.

[15] E. Snow, F. Perkins, E. Houser, S. Badescu, and T. Reinecke, "Chemical detection with a single-walled carbon nanotube capacitor," *Science*, vol. 307, no. 5717, pp. 1942–1945.

[16] S. Peng and K. Cho, "Chemical control of nanotube electronics," *Nanotechnology*, vol. 11, no. 2, pp. 57–60, 2000.

[17] X. Cui, M. Freitag, R. Martel, L. Brus, and P. Avouris, "Controlling energy-level alignments at carbon nanotube/Au contacts," *Nano Lett.*, vol. 3, no. 6, pp. 783–787, 2003.

[18] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors," *Nature*, vol. 424, no. 6949, pp. 654–657, 2003.

[19] P. Qi, O. Vermesh, M. Grecu, A. Javey, Q. Wang, H. Dai, S. Peng, and K. Cho, "Toward large arrays of multiplex functionalized carbon nanotube sensors for highly sensitive and selective molecular detection," *Nano Lett.*, vol. 3, no. 3, pp. 347–351, 2003.

[20] J. Suehiro, H. Imakiire, S. Hidaka, W. Ding, G. Zhou, K. Imasaka, and M. Hara, "Schottky-type response of carbon nanotube $NO_2$ gas sensor fabricated onto aluminum electrodes by dielectrophoresis," *Sensors Actuators B (Chemical)*, vol. 114, no. 2, pp. 943–9, 2006.

[21] J. Zhang, A. Boyd, A. Tselev, M. Paranjape, and P. Barbara, "Mechanism of $NO_2$ detection in carbon nanotube field effect transistor chemical sensors," *Appl. Phys. Lett.*, vol. 88, no. 12, pp. 123112–1, 2006.

[22] K. J. Lee and J. Kong, "Chemical Sensing with SWNT FETs," in *Carbon Nanotube Electronics*, A. Javey and J. Kong, Eds. New York: Springer, 2009, pp. 192–209.

[23] Y. Lu, C. Partridge, M. Meyyappan, and J. Li, "A carbon nanotube sensor array for sensitive gas discrimination using principal component analysis," *J. Electroanalyt. Chem.*, vol. 593, no. 1-2, pp. 105–110, 2006.

[24] J. Kong, H. Soh, A. Cassell, C. Quate, and H. Dai, "Synthesis of individual single-walled carbon nanotubes on patterned silicon wafers," *Nature*, vol. 395, no. 6705, pp. 878–881, 1998.

[25] N. Verma and A. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1196–1205, Jun. 2007.

[26] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2002.

[27] M. Tiilikainen, "A 14-bit 1.8-V 20-mW 1-$mm^2$ CMOS DAC," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1144–1147, Jul. 2001.

[28] A. Hastings, *The Art of Analog Layout*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 2005.

[29] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, Oct. 1989.

[30] T. S. Cho, "An energy efficient CMOS interface to carbon nanotube chemical sensors," Master's thesis, Massachusetts Inst. Technol., Cambridge, MA, 2007.

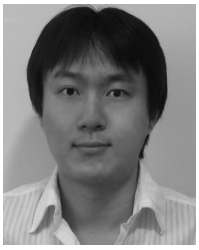
[31] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, pp. 374–378, Jun. 1976.

[32] J. Zhao, A. Buldum, J. Han, and J. Lu, "Gas molecule adsorption in carbon nanotubes and nanotube bundles," *Nanotechnology*, vol. 13, no. 2, pp. 195–200, 2002.

[33] F. Zee and J. Judy, "Micromachined polymer-based chemical gas sensor array," *Sensors Actuators B: Chemical*, vol. 72, no. 2, pp. 120–128, Jan. 2001.

[34] R. Shaffer and S. Rose-Pehrsson, "Improved probabilistic neural network algorithm for chemical sensor array pattern recognition," *Analyt. Chem.*, vol. 71, no. 19, pp. 4263–4271, Oct. 1999.

[35] U. Frey, M. Graf, S. Taschini, K. U. Kirstein, and A. Hierlemann, "A digital CMOS architecture for a micro-hotplate array," *IEEE J. Solid-State Circuits*, vol. 42, pp. 441–450, Feb. 2007.



**Taeg Sang Cho** (S'05) received the B.S. degree in electrical engineering and computer science from Korea Advanced Institute of Science and Technology, Seoul, Korea, in 2005, and the S.M. degree in electrical engineering and computer science from Massachusetts Institute of Technology, Cambridge, MA, in 2007, where he is currently working toward the Ph.D. degree in the field of computer vision and computer graphics.

His current research focuses on developing algorithms for image editing applications, and developing computational imaging methodologies for subject motion deblurring.

Mr. Cho was the recipient of 2007 AMD/CICC Student Scholarship Award, 2008 DAC/ISSCC Student Design Contest Award, and 2008 IEEE CVPR Best Poster Paper Award. He is a recipient of the Samsung scholarship.

**Kyeong-Jae Lee** (S'05) received the B.S. degree in computer engineering from the University of Virginia, Charlottesville, VA, in 2005, and the S.M. degree in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, in 2007, where he is currently working toward the Ph.D. degree.

His research focuses on hybrid system design and integration of CMOS and carbon nanotube/graphene devices.

**Jing Kong** received the B.S degree in chemistry from Peking University, Beijing, China, in 1997 and Ph.D. degree in chemistry from Stanford University, Stanford, CA, in 2002.

In 2004, she joined the Massachusetts Institute of Technology, Cambridge, MA, where she is currently an Assistant Professor in the Electrical Engineering and Computer Science Department. She has worked in the field of carbon nanotubes for over ten years and has published numerous papers on this subject. She and her colleagues at Stanford were among the first to develop the CVD method for synthesizing individual single-walled carbon nanotubes, and they also initiated the research on carbon nanotube chemical sensors. The research activity in her current group involves controlled synthesis of carbon nanotubes and graphene, investigation of their electronic and optical properties and integration with the CMOS circuits.

**Anantha P. Chandrakasan** (F'04) received the B.S, M.S., and Ph.D. degrees in electrical engineering and computer science from the University of California, Berkeley, in 1989, 1990, and 1994, respectively.

Since September 1994, he has been with the Massachusetts Institute of Technology, Cambridge, MA, where he is currently the Joseph F. and Nancy P. Keithley Professor of Electrical Engineering. He is the Director of the MIT Microsystems Technology Laboratories. His research interests include low-power digital integrated circuit design, wireless microsensors, ultra-wideband radios, and emerging technologies. He is a co-author of *Low Power Digital CMOS Design* (Kluwer Academic, 1995), *Digital Integrated Circuits* (Pearson Prentice-Hall, 2003, 2nd edition), and *Sub-threshold Design for Ultra-Low Power Systems* (Springer, 2006). He is also a co-editor of *Low Power CMOS Design* (IEEE Press, 1998), *Design of High-Performance Microprocessor Circuits* (IEEE Press, 2000), and *Leakage in Nanometer CMOS Technologies* (Springer, 2005).

Dr. Chandrakasan was a co-recipient of several awards including the 1993 IEEE Communications Society's Best Tutorial Paper Award, the IEEE Electron Devices Society's 1997 Paul Rappaport Award for the Best Paper in an EDS publication during 1997, the 1999 DAC Design Contest Award, the 2004 DAC/ISSCC Student Design Contest Award, the 2007 ISSCC Beatrice Winner Award for Editorial Excellence and the 2007 ISSCC Jack Kilby Award for Outstanding Student Paper. He has served as a technical program co-chair for the 1997 International Symposium on Low Power Electronics and Design (ISLPED), VLSI Design '98, and the 1998 IEEE Workshop on Signal Processing Systems. He was the Signal Processing Sub-committee Chair for ISSCC 1999–2001, the Program Vice-Chair for ISSCC 2002, the Program Chair for ISSCC 2003, and the Technology Directions Sub-committee Chair for ISSCC 2004–2008. He was an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1998 to 2001. He served on SSCS AdCom from 2000 to 2007 and he was the meetings committee chair from 2004 to 2007. He is the Technology Directions Chair for ISSCC 2009.