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# Wafer-Scale 3D Integration of InGaAs Image Sensors with Si Readout Circuits

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**Abstract**

*In this work, we modified our wafer-scale 3D integration technique, originally developed for Si, to hybridize InP-based image sensor arrays with Si readout circuits. InGaAs image arrays based on the InGaAs layer grown on InP substrates were fabricated in the same processing line as silicon-on-insulator (SOI) readout circuits. The finished 150-mm-diameter InP wafer was then directly bonded to the SOI wafer and interconnected to the Si readout circuits by 3D vias. A 1024 x 1024 diode array with 8-μm pixel size is demonstrated. This work shows the wafer-scale 3D integration of a compound semiconductor with Si.*

## I. Introduction

Compound semiconductors, such as InP and GaAs, offer certain properties that are superior or unique in comparison to Si. For instance, circuits based on III-V transistors can achieve higher speed because of higher electron mobility. III-V materials also have different optical properties from Si because of their different band gap. The functionality of a microelectronic system can be significantly enhanced if Si and III-V circuits can be integrated on a single chip. A variety of technologies have been explored for such integration. For instance, chiplets of III-V circuits were bonded to Si wafers for heterogeneous integration [1]. InP-based material has also been selectively grown on engineered SOI wafers for circuit integration [2].

Another approach uses wafer-scale three-dimensional (3D) integration, which has drawn growing interest recently for complex Si microelectronic systems to enhance performance and functionality. Three dimensional integrated circuits (3DIC) shorten the interconnect length, resulting in reduced time delay and power consumption. The advantage of using 3D integration for III-V and Si circuits is that it does not require processing of Si and III-V circuits on a the same wafer, which requires compromises because of material incompatibility. Wafer-scale integration also provides better alignment accuracy and interconnect size than chip stacking, allowing denser interconnects between Si and III-V circuits. In this work, 3D integration of InP-based sensor arrays and Si readout circuits is demonstrated to expand the technology to heterogeneous materials.

## II. Wafer fabrication

In order to apply the same 3D integration technology we developed for 150-mm silicon-on-insulator (SOI) wafers [3], InP wafers of the same diameter were used. The OMCVD-grown epitaxial layers for PIN detector diodes consisted of, starting from a semi-insulating InP substrate, a 3-μm thick $n^+$ InP layer, a 1.5-μm thick InGaAs undoped absorption layer, and a 0.6-μm thick undoped InP top layer. Planar-diode structure was chosen to simplify the wafer bonding process, illustrated in Fig. 1. The PIN diodes were defined by implanting the p-region with Be and annealing at 725ºC for 5 min in a phosphorus ambient. Then a silicon nitride layer was deposited as the passivation layer. The contact to the diode was defined and nitride etched to expose the InP layer. The Ti/Al metal was then deposited and patterned to complete diode fabrication. Because the InP diodes were processed in the same Si fabrication facility, the non-gold based contact metal was used. Next, a nitride and a thick oxide layer were deposited and planarized by chemical mechanical polishing (CMP) for bonding. Any step height after CMP was less than 20 nm, and the surface roughness was less than 0.5 nm. Since all equipment used is designed for Si, processing parameters were adjusted to handle InP wafers which are much more fragile. Special attention was given to handling InP wafers and minimizing the impact of thermal shock.

The Si circuits were fabricated on 150-mm-diameter wafers using 180-nm fully depleted silicon-on-insulator (FDSOI) process [4]. This technology has



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an unloaded inverter delay of 30 ps/stage and $f_T$ of 60 GHz at 1.5 V bias.

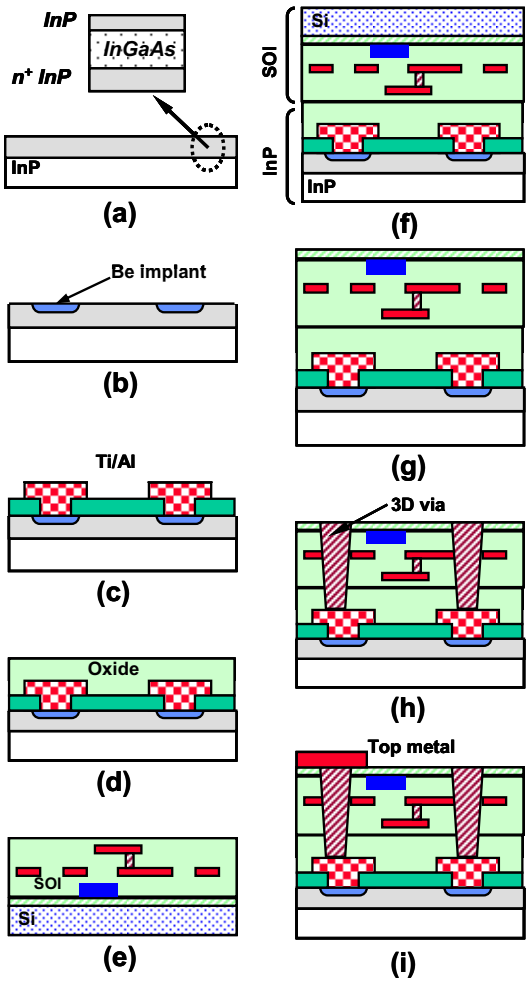


Fig. 1 3D integration process. (a) InP substrate with epitaxial layers. (b) Be implant to define p-region of the diode. (c) Nitride passivation and metal contacts formed through etched contact area for diodes. (d) Oxide deposition and planarization by CMP. (e) Planarization of finished SOI wafers with oxide deposition and CMP. (f) Bonding the SOI wafer to the InP wafer with circuits facing each other using low-temperature oxide bond. (g) Removal of Si handle wafer by grinding and wet etch which stops at buried oxide layer of SOI wafer. (h) Back contacts and 3D vias are etched and filled with W. (i) Deposit and pattern top metal for interconnects

The Si readout wafers were also prepared with oxide deposition and CMP to planarize the surface. The backside of both Si and InP wafers may need additional oxide deposition to compensate for stress induced bowing, which was kept below 40 µm over the 150-mm wafers. Using low-temperature oxide-to-oxide wafer-bonding technique, the SOI wafer with readout circuits was bonded face-to-face to the InP wafer containing diode arrays. The alignment accuracy was better than 1 µm, and the highest temperature in this bonding process was 175ºC. No adhesive was used in this process.

The SOI wafer was then thinned by grinding and selective wet etch to completely remove the Si handle substrate. The 3D vias were defined and etched through the oxide layers of the Si circuits to the metal on the InP wafer. The vias were filled with tungsten by chemical vapor deposition, followed by CMP to form the 3D plugs connecting Si circuits with InP diodes. As the last step, top metal was deposited and patterned on the wafer stack as the final interconnect. In this design, the size of the 3D vias was 2 µm; and it has been reduced to 1.25 µm in our current process [5].

The detailed layer structure after 3D integration is shown in Fig.2. The Si circuit on top of the InP substrate is mostly oxide and metal layers with scattered SOI islands for FETs. The complete removal of Si handle wafer can alleviate stress issues created by the thermal mismatch between InP and Si. There are three metal layers for SOI circuits and only one on InP PIN diodes. The top metal (BM1) is defined after wafer bonding and thinning. Each InP diode is connected to the SOI circuit by a single 3D via.

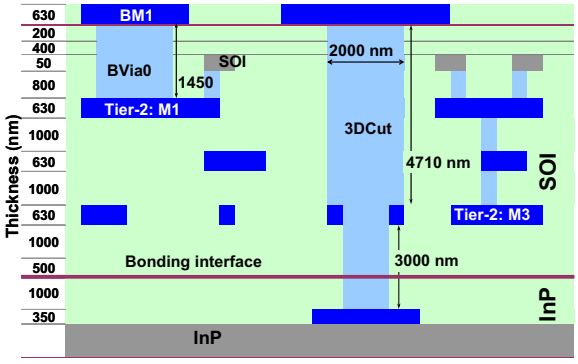


Fig. 2 Cross section of 3D integrated InP and SOI wafers

The readout circuit at each pixel consists of three MOSFETs as shown in Fig. 3. Photo current from the InGaAs PIN diode is integrated on the gate capacitor of transistor T1. When the readout transistor is on, the output node between the source of T1 and the current source follows the gate voltage of T1. The PIN diode is connected to this circuit by a single 3D via. The image array uses a modular design with four identical panels, which reduces the speed requirement for the off-chip analog-to-digital converters (ADC) [4].

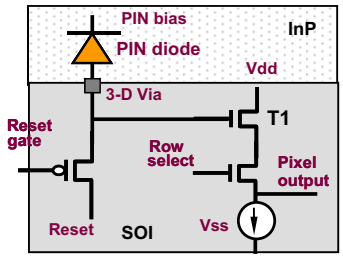


Fig. 3 Si readout circuit for each PIN pixel

Because our bonding method involves only deposited oxide, the type of the underlying wafer is not relevant. Therefore, this wafer bonding technique can be readily applied to InP or any other materials. Stress is monitored during fabrication and compensation dielectric layers are deposited when required to keep wafer bow within specifications. The low-temperature process alleviates the issues associated with different thermal-expansion coefficients of dissimilar substrates.

## III. Test Results

Figure 4(a) is the photo of a bonded InP/SOI wafer which has SOI circuits on top of the InP wafer. The individual pixels in the array are shown in the close-up of Fig. 4(b). The corresponding layout of the Si readout circuit, which is the same as that used for CMOS imagers [4], is also shown as a reference. Each PIN diode is connected to its Si readout circuit by one 3D via. The pitch of the pixel and the diameter of the 3D via are 8 and 2 µm, respectively.

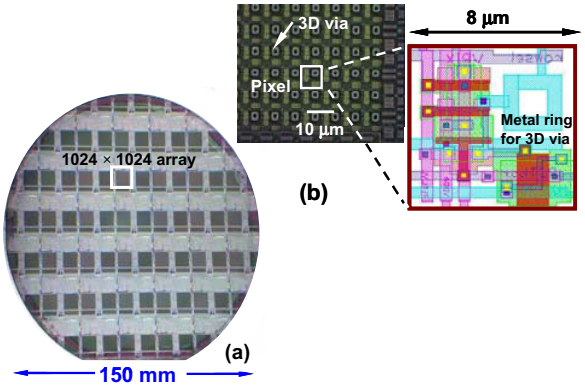


Fig. 4 Bonded InP and SOI wafers. (a) Wafer photo. The substrate is InP. (b) Pixel and corresponding readout circuit. Each pixel has one 3D via.

The cross sectional SEM micrograph of the 3D integrated sensor array is shown in Fig. 5. As in the 3D bonding process for SOI wafers [3], the diameter of the 3D via at the top is approximately 2 µm. The size of this via landing on InP diode is reduced to approximately 1.3 µm, which is determined by the opening of the metal ring in the SOI layer for interconnect. There are more than 1 million parallel 3D vias in this sensor array. The close-up of Fig. 5(b) shows seamless oxide bonding interface and landing of 3D via on the diode contact metal. The I-V characteristic of 2100 parallel test PIN diodes, same as those in the sensor array, after 3D integration is shown in Fig. 6. The dark current at 1 V reverse bias is approximately 1 mA/cm$^2$. This relatively high dark current of our first implanted planar diodes can be lowered by optimizing the diode processing.

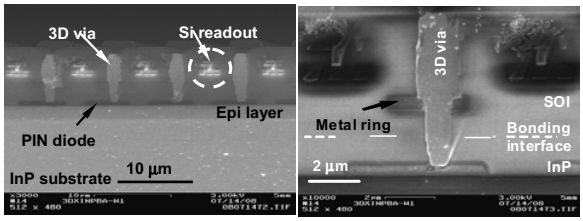


Fig. 5 SEM cross section. (a) Photo shows 3D vias in the array with Si readout circuit for each pixel. (b) Close up of the 3D via landing on PIN metal contact. A line is added to identify the bonding interface which is not visible in the SEM micrograph.

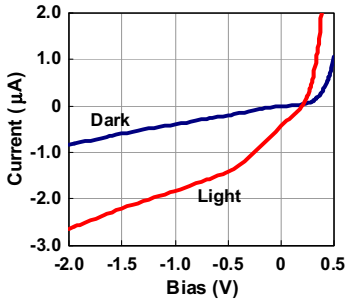


Fig. 6 Measured current of 2100 parallel PIN diodes on bonded wafers. Uncalibrated white light is focused on the diodes through the microscope.

A preliminary test result of the sensor array is shown in Fig. 7. All tests were done at room temperature on a probe station using a probe card for contact. A pulsed laser at 1.55-µm wavelength was used to illuminate the entire array with a pulse width of 125 µs. The purpose of the test was to verify the optical response of the diodes and the laser power was not calibrated. Comparison of the signals shows approximately 110 mV of output signal from each pixel generated by the laser pulses. Obviously, the high dark current of these diodes limits the resolution in this first wafer.

To capture images, external circuits consisting of operational amplifiers and ADCs were designed and

attached to the probe card. A different CW laser at 1.55 μm wavelength illuminated part of the diode array, and Fig. 7 shows the detected laser spot, which measures approximately 0.8 × 0.8 mm. The laser power was 16 mW and estimated power at each pixel was 1.6 μW. Note that with front illumination, the PIN diode was partially blocked by the readout circuit and the actual optical power was difficult to calculate. To obtain meaningful images, the image array has to be packaged and illuminated from the backside. However, the initial result is encouraging and shows a working InP-based image array 3D integrated with Si readout circuits.

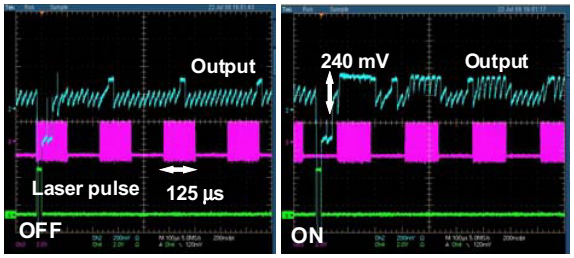


Fig. 7 Scope captures of output waveforms of 13 contiguous columns of the array in the same row. The laser diode was always on with 125-μS pulses. The light is blocked from the array for OFF-state measurement. The PIN diode was reverse biased at 1 V with 2 μS integration time. The illumination generates approximately 110 mV signal at the output of each pixel.

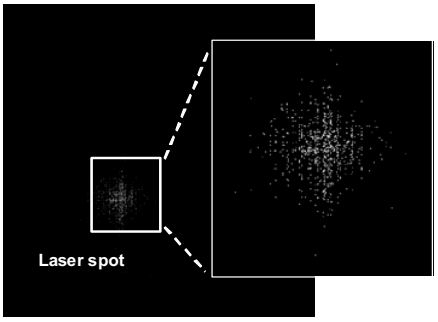


Fig. 8 Detected laser spot, which measures approximately 0.8 × 0.8 mm. The laser beam passed through the readout circuit to reach the photo detectors.

## IV. Conclusions

We have demonstrated 3D integration of InP to SOI wafers using the low-temperature oxide bonding technique developed for SOI wafer bonding. Once the bonding oxide is deposited and planarized, the bonding becomes independent of the substrate material. The same bonding process can potentially be applied to any substrates. However, stress induced by dissimilar materials has to be monitored carefully during bonding. Because the Si substrate is completely removed after bonding, the thermal mismatch between the SOI and the other substrate type is less severe.

The Si readout circuits used in this successful demonstration were designed and used for CMOS imagers. This work shows that the same Si readout circuit can be used for imagers made of any other materials to reduce the cost and development time for imagers covering different spectra. To prepare PIN diodes, we also developed InP processing that is fully compatible with Si processing and 150-mm-diameter InP wafers, the largest available.

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