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Low-Dark-Current, Back-Illuminated Charge-Coupled-Devices*

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Abstract:

Dark current for back-illuminated (BI) charge-coupled-device (CCD) imagers at Lincoln Laboratory has historically been higher than for front-illuminated (FI) detectors. This is presumably due to high concentrations of unpassivated dangling bonds at or near the thinned back surface caused by wafer thinning, inadequate passivation and low quality native oxide growth. The high dark current has meant that the CCDs must be substantially cooled to be comparable to FI devices. The dark current comprises three components: frontside surface-state, bulk, and back surface. We have developed a backside passivation process that significantly reduces the dark current of BI CCDs. The BI imagers are passivated using molecular beam epitaxy (MBE) to grow a thin heavily boron-doped layer, followed by an annealing step in hydrogen. The frontside surface state component can be suppressed using surface inversion, where clock dithering reduces the frontside dark current below the bulk. This work uses surface inversion, clock dithering and comparison between FI and BI imagers as tools to determine the dark current from each of the components. MBE passivated devices, when used with clock dithering, have dark current reduced by a factor of one hundred relative to ion-implant/laser annealed devices, with measured values as low as $10\text{-}14\text{ pA/cm}^2$ at 20°C .

KEYWORDS:

Charge coupled device, CCD, dark current, back-illumination, quantum efficiency, molecular beam epitaxy, MBE.

1. Introduction:

High quantum efficiency (QE) imagers are important for low-light-level imaging applications. One of the best techniques for achieving high QE CCDs and CMOS active pixel sensors, particularly at ultraviolet and soft x-ray wavelengths, is to back-illuminate the devices. Low-dark-current is important for resource-limited platforms such as satellites, aircraft, unmanned air vehicles, and unattended ground sensors. Such imagers can deliver highly-sensitive images without the requirements of cooling to below ambient temperatures. Unfortunately, the processes to fabricate the detectors for back-illumination can substantially increase the dark current. In addition, for x-ray or long wavelength optical (up to $1\text{ }\mu\text{m}$) sensitivity, thick detector layers ($45\text{-}75\text{ }\mu\text{m}$ or greater) are required to increase absorption, requiring the use of high resistivity silicon to enable depletion of the layers. This can lead to an increase in dark current as will be described later.

To develop a low dark current BI CCDs it is important to understand the dark current contributions from the different regions of the device. By doing this the dark current from the back side treatment can be estimated. Dark current in a BI CCD comprises four components, illustrated schematically in Figure 1: frontside surface-state, bulk (depleted and undepleted), and back surface. The frontside surface-state component, which originates from dangling bonds at the oxide/silicon interface (hereafter referred to as "frontside"), can be suppressed using surface inversion, which occurs when the clock voltage of the blocking phases drops below the inversion level. However, the integrating phase will not necessarily be inverted, so it will still contribute frontside dark current, unless that phase is also inverted. Typically this is done by inserting an additional implant into the integrating phase that enables inverting or "pinning" all the phases of the CCD during the integration. This is referred to as multi-phase pinned¹ (MPP) or all-gates pinned², (AGP) device. An alternative method of fully suppressing the frontside dark current from the integrating phase is to use two or more integrating phases, and dynamically invert them during the integration, essentially shifting charge between them³. This technique, referred to as "charge shifting" or "clock

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dithering” can suppress frontside dark current because the surface generation rate remains low for some time after inversion, and can be kept low by periodically inverting the surface during the integration. This technique, while not requiring a specially fabricated device structure, has the drawback that it requires faster clock dithering at higher operating temperatures.

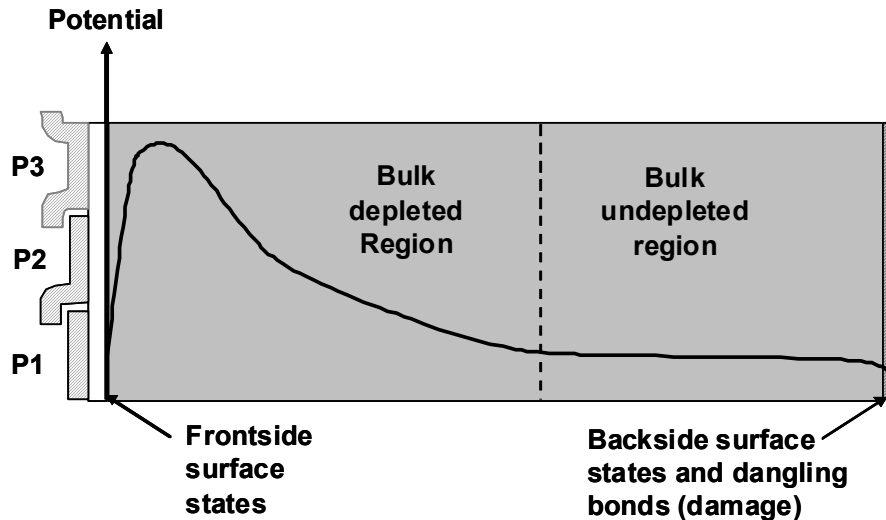


Figure 1. Schematic illustration of a CCD cross section, with potential superimposed on the device structure, illustrating the regions in which the sources of dark current occur

With frontside dark current suppressed, the remaining sources of dark current are the bulk and the backside components. These originate from the depleted and undepleted bulk silicon of the device and from the back-surface, which can have dangling bonds (both surface-state and from silicon damage) that act as generation centers. Since the detectors require high QE in the near infrared, and thus thick silicon layers, and because bulk dark current increases with detector thickness, the high QE requirement tends to increase the bulk dark current.

At Lincoln Laboratory, the dark current in BI CCD imagers has typically been higher than for FI imagers. The sources for the increased dark current can include:

- a. Unpassivated, damaged silicon bonds on or near the back surface,
- b. loss of the hydrogen that passivates dangling silicon bonds at the gate oxide-silicon interface during deposition of the low-temperature-oxide cover glass,
- c. low quality back oxide growth, or
- d. damage resulting from plasma exposure during etching steps that are needed to expose the bond pads.

Various techniques have been used to form surface layers on BI CCDs to create an electric field to accelerate the photoelectrons to the CCD detection channel for high QE. Dark current levels vary depending on the back-surface treatment. For many processes, the back-surface is the dominant dark current source. In this paper, four processes have been compared for dark current, namely ion implant-furnace anneal (IIFA), ion-implant-laser anneal (IILA), charge chemisorption (CC) and molecular beam epitaxy (MBE). Comparison of the passivation techniques and dark current testing supports the postulate that the increased dark current originates from unpassivated dangling bonds at or near the thinned back surface. They arise from wafer thinning, backside damage (ion implantation, laser annealing) and low quality native oxide growth.

Dynamic clock dithering and static surface inversion techniques were used to separate the frontside, backside and bulk dark current for FI and BI devices, for two back-surface processes, namely IILA and MBE. As part of a program to reduce the dark current in BI CCDs, the relative dark current produced by different backside passivation techniques has been explored, and a superior MBE process with hydrogen sinter step has been established.

2. Backside illumination – Passivation Processes

We have explored four backside passivation techniques namely: IIFA, IILA, MBE and CC, the latter in collaboration with Michael Lesser at the University of Arizona⁵. Figure 2 illustrates the cross-sections for these back-surface treatments and the processes are described below.

Ion Implant-Furnace Anneal (IIFA)

Most passivation methods are based on introducing a very shallow doped region in the backside surface of the thinned imager. This can be done using an ion implantation followed by a low-thermal budget furnace anneal, sometimes termed the refractory process. This process was used on the BI CCDs for the Chandra X-ray Observatory. The process consists of a thermal oxidation (35 nm dry oxidation) followed by a 25 keV BF_2 implantation and an 850°C furnace anneal to activate the dopant. This process was performed on CCDs using narrow (~1 mm wide) rim-thinned wafers⁴.

Ion Implant-Laser Anneal (IILA)

An alternative to the furnace anneal for activating the implanted dopant is pulsed laser annealing to melt and recrystallize the implanted surface. The laser beam is expanded to an area of about 6 mm x 7 mm, and this beam is then step-scanned to anneal large devices. The laser pulse is a few tens of ns in duration, and thus the heating is highly localized to the back-thinned surface. This is essential because the CCD wafer is mounted to a handle wafer using epoxy for back thinning. This enables ease of handling after the device wafers are thinned, but limits all remaining steps to temperatures that are compatible with the epoxy. For this reason, the mounted wafers may not undergo an anneal step in hydrogen to repassivate dangling bonds after the back-illumination. Ease of processing with IILA has made it useful, but lack of hydrogen annealing after backside processing has also caused it to produce higher dark current.

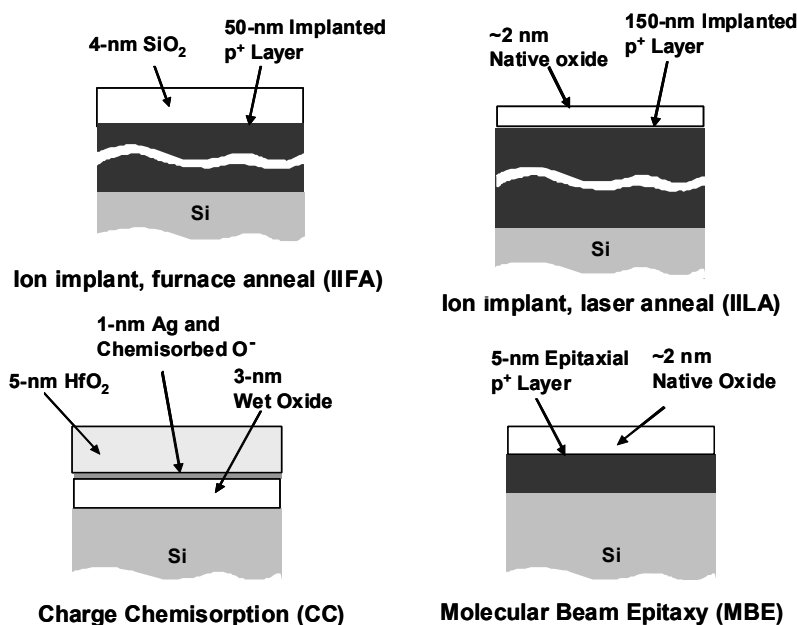


Figure 2. Illustration of backside structures for CCD device passivation

Charge Chemisorption (CC)

For the CC process, as practiced at the University of Arizona⁵, the back surface is oxidized and a thin silver layer is deposited on the SiO_2 layer. The silver catalyzes oxygen dissociation, which produces a negative charge in the back-surface oxide creating an electric field that drives photoelectrons produced near the back surface towards the

front surface, where they can be collected in the buried channel. The silver layer is capped with a hafnium oxide layer as a sealant⁶. In limited testing, however, the dark current in CC processed imagers has been nearly as high as for the IILA devices.

Molecular Beam Epitaxy (MBE)

Backside passivation has been performed using an MBE process to grow an ultra thin boron-doped silicon layer on the imager back-surface. The MBE process, similar to one published by JPL⁷, was developed at LL⁸, and has recently been improved⁹. Two important differences between the MBE processes in references 8, 9 and this work were the reduction of the growth rate by a factor of 10 due to doping limitations, and the inclusion of a 400°C, hydrogen annealing step after the MBE for surface passivation.

Dark Current Preliminary Results

As a baseline for comparing the dark current of different backside treatments, historical data was used to compare imagers prepared with each of the above alternatives. In these tests, the imagers were typically operated in inverted mode, but clock dithering was not done to further reduce the frontside dark current. The typical dark current ranges at -50 °C are presented in Table I for an imager with a 24- μm pixel. The FI dark current is given for reference. These data, available from typical testing conditions provided an overview of the backside dark currents and how they compare to the FI case. Generally, the two backside treatments with the lowest dark current appeared to be the IIFA and MBE processes. More recently, results on MBE passivated CCDs (Ref. 9) indicated the potential to obtain lower dark current than in the table, suggesting the backside dark current could be reduced further. Based on these preliminary results, the MBE process was targeted for a more complete comparison with the FI imagers and those passivated using IILA.

Imager structure	Dark current range (e ⁻ /pixel/sec)	Dark current range (pA/cm ²)
FI (unthinned)	0.6-2.4	0.017-0.065
IIFA	5.7-12.6	0.157-0.349
IILA	10.5-23	0.293-0.654
CC	12-16	0.336-0.448
MBE (Ref. 8)	6.7-19.5	0.188-0.544

Table I. Dark current data for 24 μm pixel CCD imagers front-illuminated and back-illuminated with different backside treatments. All data were taken at -50°C.

3. Device Characterization

All measured results in this section were made on a Lincoln Laboratory imager, CCID-41, which has been described elsewhere¹⁰. The architecture is a three-phase (P1, P2, P3), three-layer polysilicon CCD imager with n-type buried-channel and 24- μm pixels in the image array. The CCD imagers were fabricated on high resistivity float-zone (FZ) wafers, > 4000 $\Omega\text{-cm}$. The CCD imager has a frame-transfer architecture with 1024 \times 1024 imaging array with 4 readout ports (A,B,C,D).

Onset of Surface Inversion

The frontside component from the two blocking phases can be suppressed using surface inversion. Surface inversion occurs when the gate voltage bias is reduced to the point where the oxide-silicon interface is just below zero potential, thus enabling the formation of an inversion layer. The onset of inversion for the devices used in the measurements is expected to occur at about -5 V, as calculated using a one-dimensional simulation presented in Figure 3. The figure also shows the accumulation of holes near the oxide-silicon interface as the voltage is decreased. In these devices, fabricated on high-resistivity float-zone wafers, the depletion depths can range from 25 to 60 μm , depending on the gate voltage. The inversion voltage was determined experimentally by measuring dark current versus gate voltage. With a fixed clock swing of 10 V, the dark current was measured as the gate clock offset voltage was lowered. Figure 4 shows the measured imaging-array dark current from a MBE processed device at

10°C versus the low rail of the clock voltages for all four ports. From this data we can confirm that the onset of surface inversion starts at a gate voltages of -4 to -5 V and is fully suppressing dark current at around -7 V. For subsequent measurements we select low rails above -4 V or below -7 V in order to turn the frontside dark current on or off.

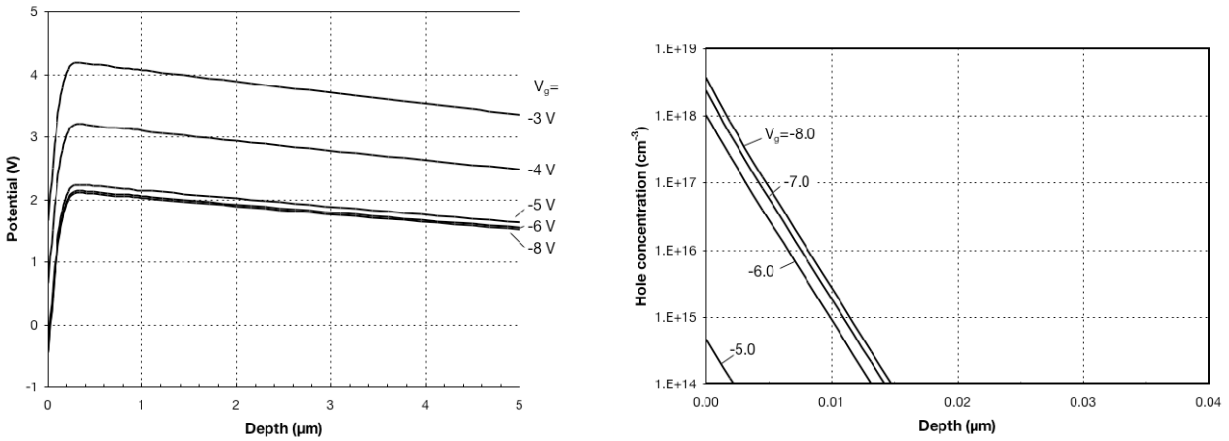


Figure 3. Voltage potential and hole concentration in CCD buried layer calculated from a one-dimensional simulation.

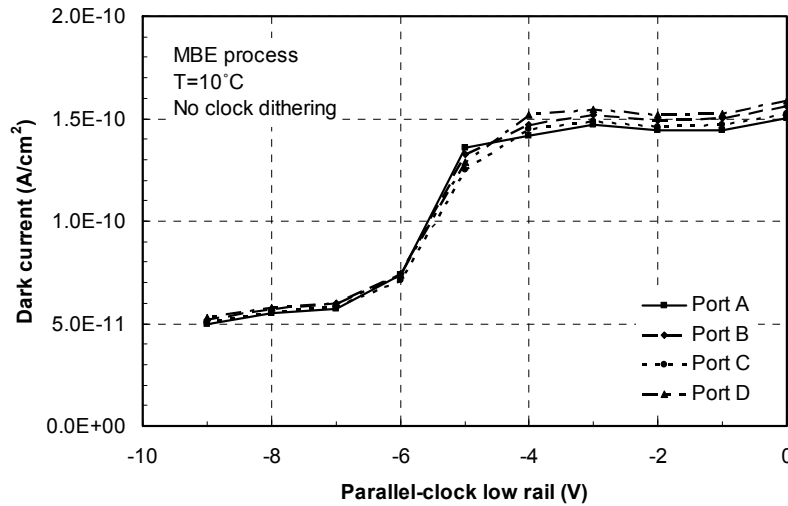


Figure 4. Dark current of a MBE backside passivated CCD versus the parallel-low clock rail at 10°C. Clock swing is 10 V.

Dark Current versus Temperature

The dark current versus temperature for low rails of -1.0 and -8.0 is plotted in Figure 5. Included on the graph is a fit to the data for an equation that describes the temperature dependence of the dark current J_D in silicon for mid-gap states:

$$J_D = k_0 T^{3/2} \exp(-0.603 / kT) \quad (1)$$

where k is Boltzman's constant, k_0 is a pre-exponential factor, 0.603 eV is the activation energy for mid-gap states, and T is the temperature in Kelvin. The data illustrate the reduction of dark current versus temperature due to inverting the blocking phases. In these measurements, P2 was at the high clock voltage setting (VH) above inversion to collect the dark current charge, while the remaining two phases were held at a low clock voltage (VL). Thus, the data in Figure 5 does not represent suppression of the surface-state dark current under P2.

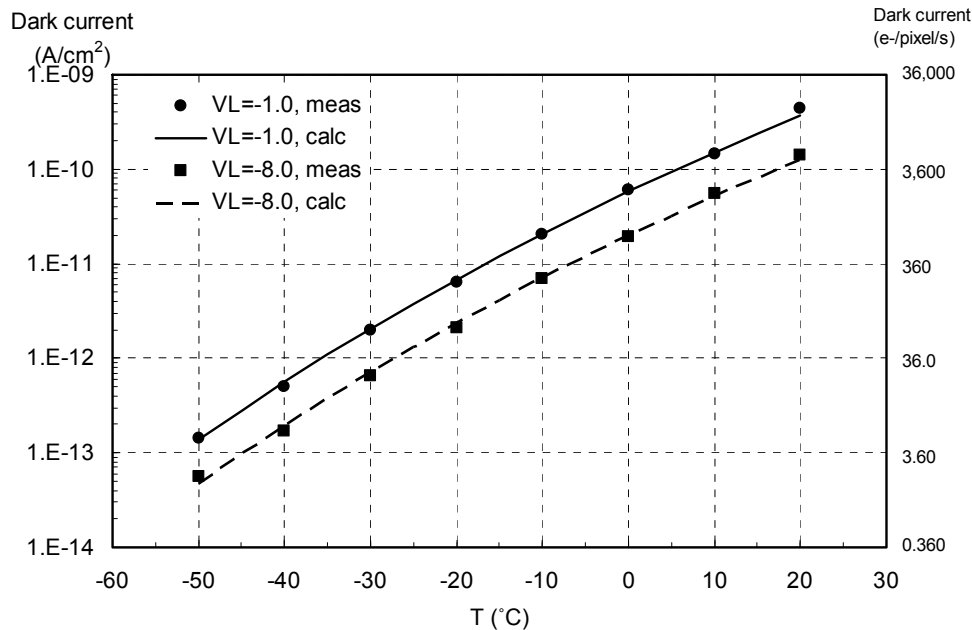


Figure 5. Measured and calculated dark current of a MBE backside passivated CCD versus temperature for two settings of the parallel-low clock rail. No clock dithering.

Dark Current with Dithering

Dynamic clock dithering was used to further reduce frontside dark current. This involves shifting the charge between phases within a pixel at a rate that is faster than the recovery time of carrier generation via surface-states. When a gate is switched from VL to VH, the dark current does not increase to its non-inverted steady-state value immediately but rather recovers over a period of time³. At room temperature the dark current begins to measurably increase at about 100 μ s after the switching, but this recovery time increases rapidly as the temperature is lowered. We have applied the following recipe for clock-dithering measurements:

1. Integrate under P2 (P2=VH, P1, P3=VL) for T_0 seconds
2. Transfer the charge to P1, then back to P2 (2-1-2 dithering)
3. Repeat step 1 and 2 for the entire integration time.

The total transfer time from P2 to P1 and back to P2 took 180 μ s. $T_0 = 820 \mu$ s was used for the data described in Figure 6. This is not quite sufficient to fully suppress frontside dark current at room temperature, but it is adequate at temperatures below -10°C .

Figure 6 shows dark current versus VL at -10°C for both dithered and non-dithered conditions for the MBE passivated CCDs. The most striking result is the dark current reduction under inverted clock conditions, indicating how low the bulk and backside dark current are relative to the frontside component. The dark current at VL = -9 V with dithering is 22 e-/pixel/s, a reduction of 11 \times below the non-dithered case at VL = -9, and a reduction of 35 \times below the non-dithered, non-inverted case (VL=0). The figure also illustrates that about 6-6.5 pA/cm² of frontside dark current is eliminated per phase as it is inverted. Moving from -1 V to -8 V eliminates \sim 13 pA from 2 blocking

phases, while dithering eliminates another ~ 6 pA from the integrating phase. The remaining dark current from the bulk and the MBE back surface is quite low, 0.76 pA/cm^2 .

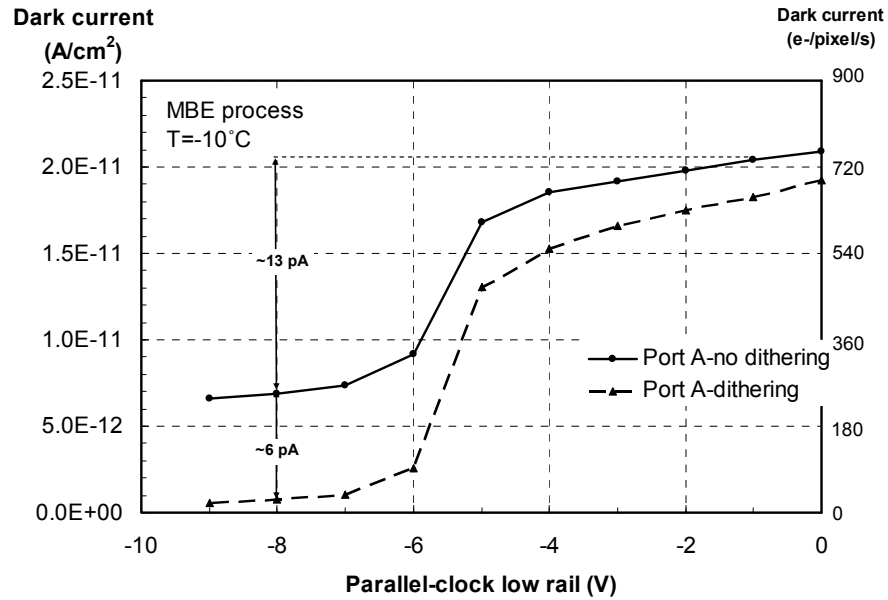


Figure 6. Dark current of a MBE backside passivated CCD for dithered and non-dithered conditions as a function of clock voltage.

Another interesting feature of this data is that dithering reduces the dark current even under non-inverted clocking conditions. This effect has not been fully explained at this point; it may have to do with the flow of hole dark current along the channel surface to the channel stops. A further curious feature is the voltage dependence of the dark current under non-inverted conditions (as opposed to voltage independence in Figure 4). This may be related to changes in depletion extent in the channel stop regions as the gate voltage increases.

Comparison Between IILA and MBE Passivation

To better understand the differences in dark current sources between the MBE and IILA backside treatments, CCD imagers were operated in the inverted mode, with and without dithering. The dithering rate was increased in these measurements to completely suppress frontside dark current at 20°C . The total charge transfer time from P1 to P2 and back to P1 was decreased to $24 \mu\text{s}$, and $T_0 = 56 \mu\text{s}$ was used for all the data described below.

Figure 7 shows the results of these experiments, and several items are apparent from the comparison. The frontside dark current from a single phase of the MBE-treated device at -10°C is about 5 pA , consistent with that observed in Figure 6. The dark current from the backside of the IILA device, dithered to eliminate the frontside component, is approximately the same as the frontside dark current from a single phase of the MBE device non-dithered. This indicates that the IILA backside has an areal density of active defects that are equivalent to approximately one-third of those present at the gate oxide interface. The frontside dark current from a single phase of the IILA device is significantly higher than this, adding $\sim 60 \text{ pA}$ to the dark current per phase, an order of magnitude higher than the MBE device. At 20°C , the dark current for the non-dithered IILA device is high enough to saturate the device during the integration, so that data point is not plotted. One possible reason for this difference is the loss of hydrogen from the gate oxide during the low temperature oxide deposition of the cover glass (item b in section 1). For the MBE devices, hydrogen anneal is repeated after the MBE back-surface treatment and is the last high temperature process.

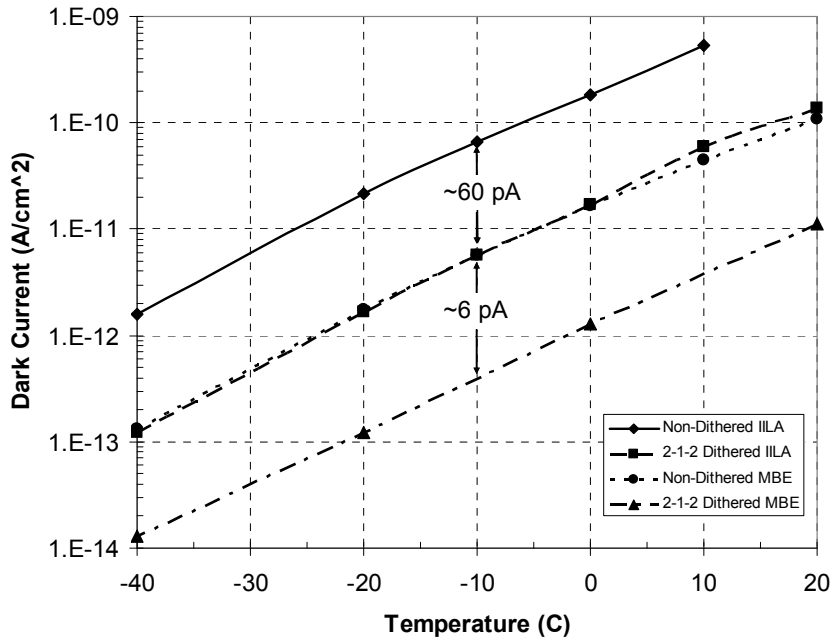


Figure 7. Dark current versus temperature for CCD imagers with ILLA and MBE backside treatments.

Comparison Between Front and Back Illuminated Devices

To compare backside dark current with that from FI (un-thinned) devices, we operated the CCD in inverted mode, with and without dithering, again to determine the frontside dark current from a single phase. The FI CCD has a phosphorus-doped gettering layer on the back side, so it is metallized and operated with a back gate voltage of +5 V. This essentially depletes a region $\sim 75\text{-}\mu\text{m}$ thick near the back surface, removing nearly all of the thermal electrons generated through the back contact. Consistent with the MBE treated device, the frontside (single phase) dark current is $\sim 5\text{ pA}$ at -10°C , indicating that the hydrogen passivation is equivalent for the two imagers. In the dithered FI case, the only dark current source should be from the silicon bulk. The collection region includes a $\sim 50\text{ }\mu\text{m}$ thick depleted layer extending from the front side of the device, and half of the remaining undepleted silicon layer, which is $550\text{ }\mu\text{m}$ thick. If we take a simple approach and scale the total bulk dark current proportionally from $325\text{ }\mu\text{m}$ to $45\text{ }\mu\text{m}$, we obtain the estimate in Figure 8 for the bulk dark current component in the $45\text{ }\mu\text{m}$ thick (MBE treated) device, labeled "FI scaled to $45\text{ }\mu\text{m}$ ". This is equivalent to assuming that the bulk dark current can be modeled with the depleted and undepleted generation rates the same. This assumption will be evaluated in the discussion section below. This dark current curve falls below the actual MBE-treated curve, indicating that it also contains a component due to the backside that can be estimated from the difference. These calculated data are labeled as "MBE backside only" in Figure 8. Using this approximation, the estimated MBE backside dark current is about 0.005 pA/cm^2 at -40°C (greater than the bulk dark current), 0.2 pA/cm^2 at -10°C (nearly equals the bulk), and about 2 pA/cm^2 at 20°C (less than the bulk).

4. Discussion

Comparison with Other Investigations

Comparison with other investigations provides some additional insight into the relative contributions to dark current from back side, bulk and surface states.

For example, Widenhorn, et al¹¹, published dark current data for a 3-phase/3-poly, n-buried channel BI CCD with a $24\text{ }\mu\text{m}$ pixel that was operated in MPP mode to eliminate frontside dark current. At 18°C , the average dark current in the CCD they studied was plotted to be about 33 pA/cm^2 , which is 2-3 times higher than the results obtained here. The depletion depth of the CCD in that study is reported to be $8.6\text{ }\mu\text{m}$, with an additional undepleted region of $\sim 10\text{ }\mu\text{m}$ or less. Using Figure 8, and scaling the bulk dark current to $\sim 20\text{ }\mu\text{m}$ produces an estimate of $\sim 4\text{ pA/cm}^2$, so

that it appears that the backside dark current of the MBE treated device is significantly lower than the device measured by Widenhorn, et al. In addition, they present data that can be used to evaluate the assumption used in scaling the bulk dark current contribution to make Figure 8. They measure the activation energy of the dark current to be lower (0.57 eV) at lower temperature and higher (1.14 eV) at higher temperature due to the difference between the generation rate in the depleted versus undepleted region. In our measurements, we measure similar activation energies at lower and higher temperature, with the data over the full temperature range fitting reasonably well using a 0.828 eV activation energy, plotted as “2-1-2 Dithered FI fit” in Figure 8. Since the depleted and undepleted bulk dark current generation rates are not very different in this study, the assumption provides a reasonable estimate of the bulk dark current in the thinned CCD.

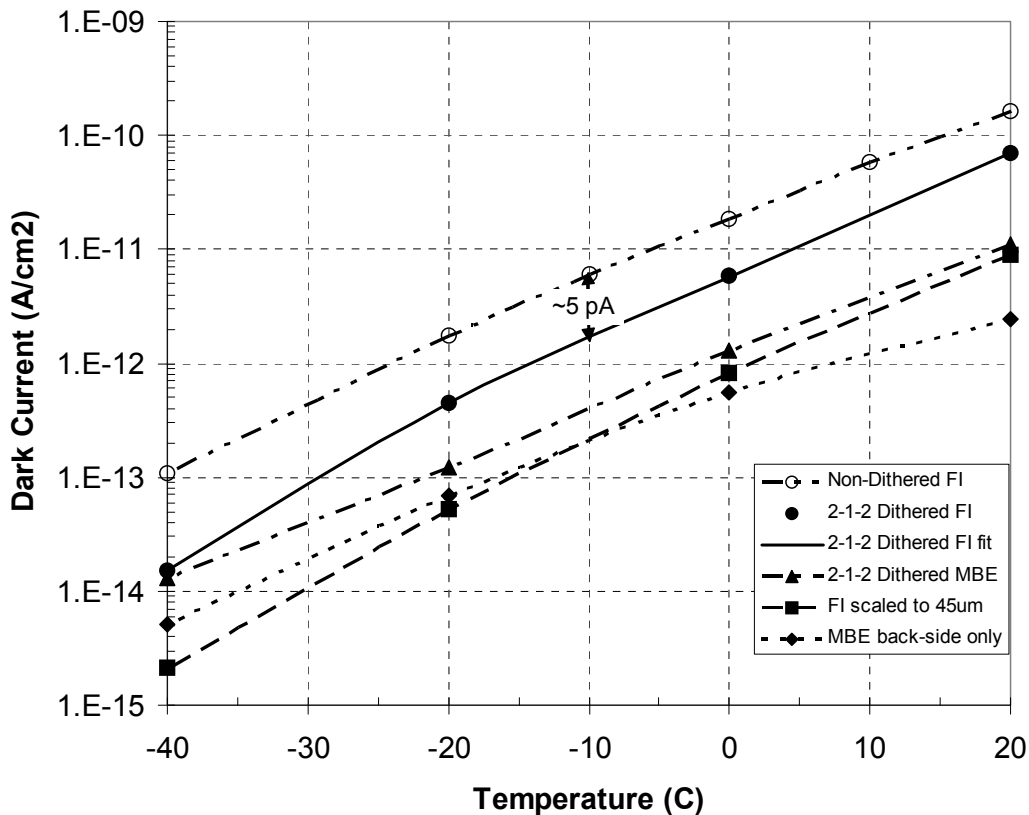


Figure 8. Dark current versus temperature for a FI CCD and a BI CCD with MBE backside treatment.

Operating Temperature versus Dark Current

Since in many previous applications^{4,6,9} it has been acceptable to reduce dark current by cooling to the temperature range of -60 to -100°C, many of the CCDs from Lincoln have not required the improvements implemented in this paper, namely MBE backside treatment or dithered clocking. In these lower temperature ranges the readout noise is larger than the dark current. However, for higher operating temperatures, e.g. conditions where power or weight are constrained, or reliability is critical, a thermoelectric cooler is undesirable. In that case a passive radiator may be preferred, and the dark current needs to be reduced by these other methods. Compared with non-dithered-IILA devices the operating temperature for the dithered-MBE-treated devices can be more than 40°C warmer, with equivalent dark current. Compared to dithered-IILA devices, the dithered-MBE-treated devices can be operated 25°C warmer with equivalent dark current.

To Dither or Not to Dither

The need to make a low-dark current CCD at higher temperature has highlighted the need for reducing frontside dark current through trap filling. While this has been done in this work by clock dithering, it has been done for many commercial CCDs using the MPP structure. It should be useful to determine what sort of application requirements can be met with clock dithering and what requirements call for the MPP structure. It is apparent that for the benefits of reduced power, weight, and improved reliability (thermoelectric coolers tend to be mechanically fragile and pose a higher risk of failing), that elevated operating temperatures will be preferred if possible. Also, in some applications in which charge is naturally shifted between phases/pixels during integration, e.g. time delay and integration (TDI), or jitter correction in an orthogonal transfer CCD, that clock dithering is being done intrinsically by the application. In these cases, a CCD with MPP may not be necessary. Note that clock dithering must be fast enough to prevent surface states from re-filling between clock pulses³, e.g. about 100 $\mu\text{sec}/\text{transfer}$ at 20°C. Further, fast clock dithering can also consume power, though a large CCD with a total capacitance of 1 μF , should require only about 1 W dithering at 100 $\mu\text{sec}/\text{transfer}$; this is less than a cooler typically would use. At higher temperatures, e.g. 45°C, the faster required dithering rate, e.g. 10 $\mu\text{sec}/\text{transfer}$ could consume about 10 W, which is comparable to that of a cooler.

In cases where a staring array is needed, there is essentially no advantage to clock dithering over the MPP structure, with the possible exception of full well capacity. The MPP structure can then be advantageous.

5. Conclusion

We have developed a back-illumination passivation process that provides significantly lower dark current than has previously been obtained using the IILA passivation process. The MBE-treatment has lowered dark current to below the level of bulk dark current in these 45 μm thick devices. This lower dark current has opened up an array of possible applications for which low dark current CCDs operating at near room temperature present an advantage. Using these techniques, we have been able to operate these devices at room temperature with many seconds of integration time. Figure 9 shows two images taken with a BI MBE-treated imager operated at 20°C, using non-dithered and dithered conditions with integration times of 15 and 60 seconds respectively. A time-equivalent dark frame is subtracted from each to reduce the noise in the images. Even the brightest pixels in the raw images, however, were only about half of the full well charge of 120,000 electrons. On average, the dark current accounted for about 90% and 60% of the charge in the raw images for the non-dithered and dithered cases, respectively. In both cases the images have excellent spatial resolution and contrast (e.g., the shadows of tree branches are visible on the walls of the house).



(a) non-dithered conditions, 15 second integration (b) dithered conditions, 60 second integration
Figure 9. Images taken with the MBE-processed BI imager operated at +20°C, using conditions shown.

The comparison of non-dithered and dithered clocking, along with comparisons to similar FI devices, enables separating out the various dark current components, indicating their relative magnitudes. The dynamic dithering and MBE passivation process has reduced the dark current (at any temperature) by a factor of one hundred relative to ion-implant/laser annealed devices, enabling operating temperatures to be increased by approximately 30°C with equivalent dark current. The MBE BI CCDs with the dynamic clock dithering have given measured dark current as low as 10 to 14 pA/cm² at 20°C. Along with describing the MBE process and presenting the dark current characterization measurements, a comparison has been made between the trade-off in power required for dithering and cooler requirement versus operating temperature.

REFERENCES:

1. J. Janesick, T. Elliot, G. Fraschetti, and S. Collins, "Charge-coupled device pinning technologies," Proc. SPIE, Los Angeles, CA, 1989, Vol. 1071-15.
2. I.M. Peters, A. Kleinmann, F. Polderdijk, W. Klaassens, R. Frost, J.T. Bosiers, "Dark-current reduction in very-large area CCD imagers for professional DSC applications," IEDM 2004, 04-993.
3. B.E. Burke and S.A. Gajar, "Dynamic suppression of interface-state dark current in buried channel CCDs," IEEE Trans. Electron Devices, Vol. 38, No.2, pp. 285-290, 1991.
4. B. Burke, J. Gregory, M. Bautz, G. Prigozhin, S. Kissel, B. Kosicki, A. Loomis, and D. Young, "Soft-X-Ray Imagers for AXAF," IEEE Trans. Electron Dev., Vol. 44, pp. 1633-1642, 1997.
5. M. Lesser and V. Iyer, "Enhancing the back illuminated performance of astronomical CCDs," Proc. SPIE, vol. 3355, pp. 446-456, 1998.
6. B. Burke, J.A. Gregory, A.H. Loomis, M. Lesser, M.W. Bautz, S.E. Kissel, D.D. Rathman, R.M. Osgood III, M.J. Cooper, T.A. Lind, and G.R. Ricker, "CCD Soft-X-Ray Detectors With Improved High- and Low-Energy Performance", IEEE Trans. Nucl. Sci. Vol. 51, No. 5, pp. 355-359, 2004.
7. M.E. Hoenk, P.J. Grunthaler, F.J. Grunthaler, and R.W. Terhune, M. Fattahi and H. Tseng, "Growth of a delta-doped silicon layer by molecular beam epitaxy on a charge-coupled device for reflection-limited ultraviolet quantum efficiency", Appl. Phys. Lett. Vol. 61, No. 9, pp.1084-1086, 1992.
8. S.D. Calawa, B.E. Burke, P.M. Nitishin, A.H. Loomis, J.A. Gregory, and T.A. Lind, "Substrate preparation and low-temperature boron-doped silicon growth on wafer-scale charge-coupled devices by molecular beam epitaxy", J. Vac. Sci. Technol. B, Vol. 20, No. 3, pp. 1170-1173, 2002.
9. R.C. Westhoff, M.K. Rose, J.A. Gregory, G.D. Berthiaume, J.F. Seely, T.N. Woods, G. Ucker, "Radiation-hard charge-coupled devices for the extreme ultraviolet variability experiment", Proceeding of SPIE, Vol. 6686, pp. 668604(1-9), 2007.
10. K. Koyama and the XIS Team, "The X-ray imaging spectrometer (XIS) on board Suzaku," Publications of the Astronomical Society of Japan, 59, pp. S23-S33, 2007.
11. R. Widenhorn, M.M. Blouke, A. Weber, A. Rest and E. Bodegum, "Temperature dependence of dark current in a CCD", Proc. SPIE, Vol. 4669, pp. 193-201, 2002.