YOUR NAME _____

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology

6.012 Electronic Devices and Circuits

FINAL EXAMINATION

Open book.

Notes:

1. Unless otherwise indicated, assume room temperature and that kT/q is 0.025 V, kT/q ln 10 = 60 mV, and $n_i = 10^{10}$ cm^{-3} for Si.

2. This test is designed so that most parts can be worked independently of the others.

3. All of your answers and any relevant work must appear on these pages. Any additional paper you hand in will not be graded.

4. Make reasonable approximations and assumptions. State and justify any such assumptions and approximations.

5. Be certain that you have all twelve (12) pages of this exam booklet and make certain that you write your name at the top of this page as indicated.

6. You may see your final exam in Room 13-3058 beginning June 5, 2000.

Grader Use Only	**PROBLEM 1**	_____	(out of 20 possible)
	PROBLEM 2	_____	(out of 25 possible)
	PROBLEM 3	_____	(out of 28 possible)
	PROBLEM 4	_____	(out of 27 possible)
	TOTAL		

Problem 1 - (20 points)

Warm-up questions:

a) A sample of silicon is known to contain 10^{17} cm^{-3} arsenic atoms (column V) and 5 x 10^{16} cm^{-3} boron atoms (column III). What are the thermal equilibrium hole and electron concentrations in this sample at room temperature where $n_i = 10^{10}$ cm^{-3}?

$n_o =$ _____ cm^{-3}

$p_o =$ _____ cm^{-3}

b) A high quality long base silicon p-n diode is inadvertently irradiated in a nuclear reactor with the consequence that the minority carrier lifetimes on the n- and p-sides decrease from 10^{-4} s to 10^{-8} s (no other materials parameters change). How much, if at all, does the diode saturation current change?

$$\frac{I_{ES}(\text{after})}{I_{ES}(\text{before})} \approx \text{\_\_\_\_\_}$$

c) i) Rank order the common-emitter (CE), common-base (CB), emitter follower (EF) bipolar linear amplifier configurations in order of increasing input resistance, assuming comparable bias levels, I_C:

_____	_____	_____
Lowest	Middle	Highest

Explanations:

ii) Rank order the common-source (CS), common-gate (CG), source follower (SF) MOSFET linear amplifier configurations in order of increasing output resistance, assuming comparable bias levels, I_D:

_____	_____	_____
Lowest	Middle	Highest

Explanations:

Problem 1 continues on the next page.

Problem 1 continued

d) Answer in five words or less:

i) CMOS is one of the fastest MOSFET logic families and it is used in the highest speed microprocessors. At the same time, one of the most important applications for CMOS is in low speed circuitry. What is CMOS's advantage for low speed applications?

ii) What major structural change was made to enable the 486 to run faster than the 386 (and again to make the Pentium faster than the 486)?

iii) Why is CMOS attractive for linear amplifier applications? Give one reason (there are several).

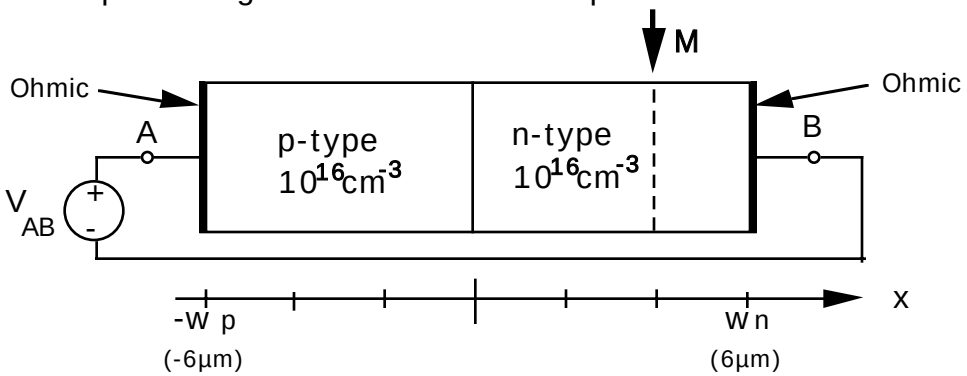
e) A certain common-emitter bipolar transistor amplifier is fabricated using resistors whose resistance is insensitive to temperature and with transistors whose forward current gain, β_F, Early voltage, V_A, and base-emitter knee voltage, $V_{BE,ON}$, are essentially unchanged between room temperature (25°C) and 100°C. None the less, when this amplifier is heated to 100°C its voltage gain, A_v, drops noticably. Give an explanation as to why the voltage gain might change and use your explanation to estimate $A_V(100°C) / A_V(25°C)$.

$A_V(100°C) / A_V(25°C) \approx$ _____

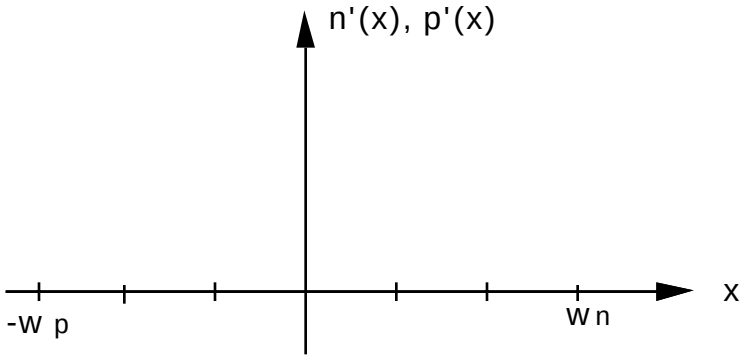
End of Problem 1

Problem 2 - (25 points)

The symmetric p-n diode shown below, with $N_{Ap} = N_{Nn} = 10^{16}$ cm^{-3}, is illuminated by steady state light that generates M hole-electron pairs/cm^2-s uniformly over the plane at $x = 2\,w_n/3$. The p- and n- region widths, w_n and w_p, are both 6 µm, and both minority carrier diffusion lengths are much larger than this, i.e., L_e, L_h >> 6 µm. The electron mobility, μ_e, is 1600 cm^2/V-s, and the hole mobility, μ_h, is 600 cm^2/V-s. Neglect the depletion region widths relative to 6 µm.



a) On the axes below plot the excess minority carrier concentrations throughout the diode when $V_{AB} = 0.54$ V and M = 0.



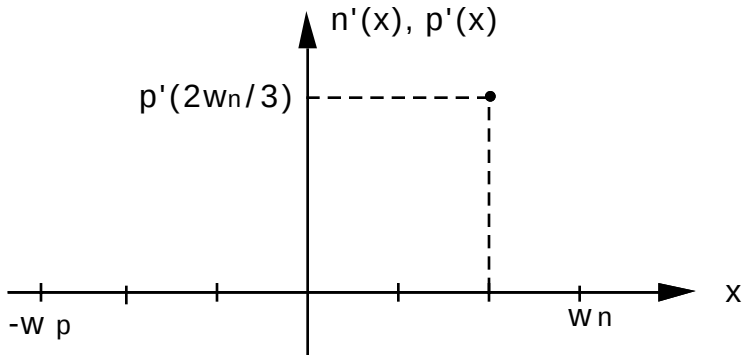
b) If we take as the criterion for low level injection (LLI) that the excess minority carrier concentration must not exceed 10% of the equilibrium majority carrier concentration, how large can V_{AB} be before LLI is violated when M = 0?

$V_{AB} \leq$ _____

c) Now consider setting $V_{AB} = 0$, i.e., short circuiting the diode, and applying illumination, $M = 3.75 \times 10^{13}$ cm^{-2}s^{-1}. On the axes provided at the top of the next page plot the excess minority carrier concentrations throughout the diode now. Assume p' has the value indicated on the axes at $x = 2w_n/3$.

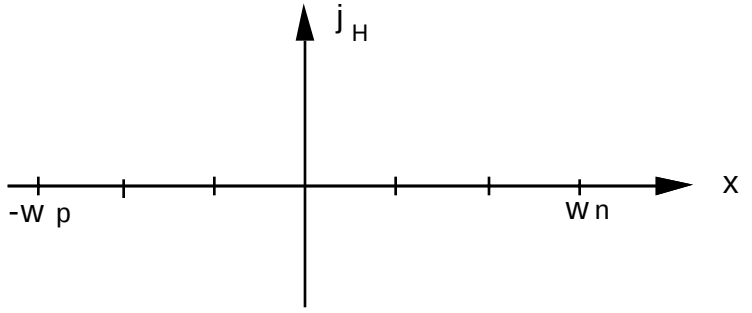
Problem 2 continues on the next page.

Problem 2 continued

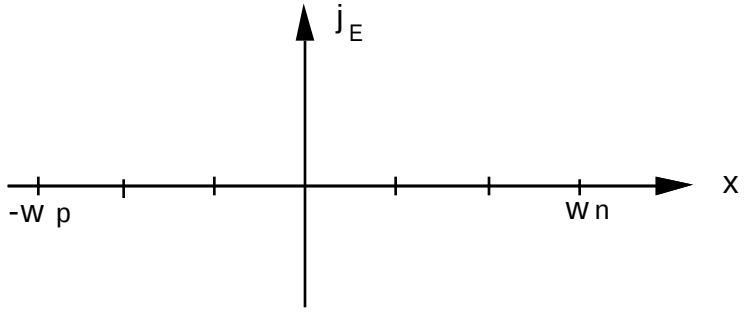


d) On the axes below make labeled plots of the hole current density, j_H; the electron current density, j_E; and the total current density, j_{TOTAL}; throughout the short-circuited, illuminated device.

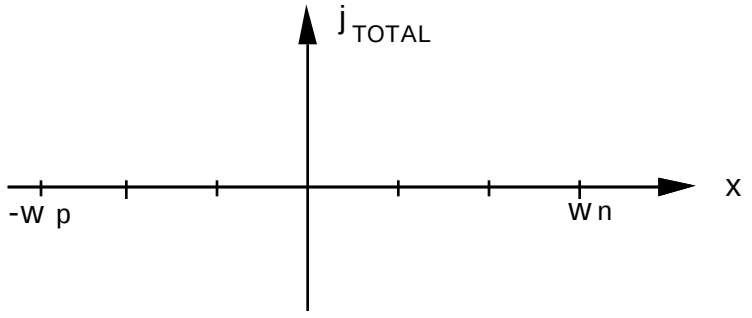
i) Hole current density:



ii) Electron current density:



iii) Total current density:



Problem 2 continues on the next page.

Problem 2 continued

e) i) What is $p'(2w_n/3)$?

$p'(2w_n/3)$ = _____

ii) How large can M be before LLI is violated when $V_{AB} = 0$?

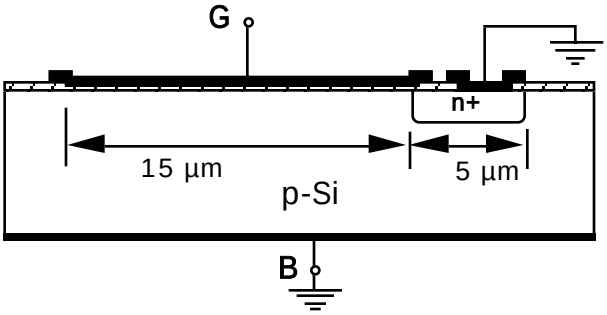
M ≤ _____

End of Problem 2

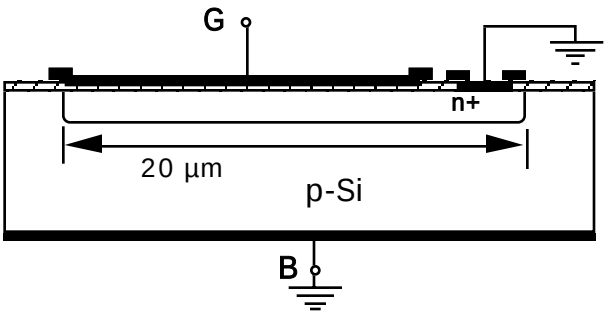
Problem 3 - (28 points)

Consider the two silicon device structures shown in cross-section below:

Device A:



Device B:



Both of these devices are made on p-type silicon with a net doping level of 10^{17} cm^{-3}, and are 20 µm wide normal to the page. The n^+ regions are doped to 10^{18} cm^{-3}, and the n^+-p junction is 1 µm from the top surface. The thin oxide is a high quality thermal oxide 16 nm thick, and covers an area 20 µm wide by 15 µm long. In Device A the n^+ region is 20 µm wide by 5 µm long and extends just up to the edge of the thin oxide, while in Device B it is 20 µm wide by 20 µm long and extends all the way under the thin oxide, as shown in the figure.

You may assume that throughout the silicon the electron mobility, μ_e, is 1600 $cm^2/V\text{-}s$ and the hole mobility, μ_h, is 600 $cm^2/V\text{-}s$ (except in an inversion layer in which case μ_e = 600 $cm^2/V\text{-}s$ and μ_h = 400 $cm^2/V\text{-}s$); that the intrinsic carrier concentration, n_i, is 10^{10} cm^{-3} at room temperature; and that the dielectric constant, ε_{Si}, is 10^{-12} F/cm. The dielectric constant of the oxide, ε_{ox}, is 3 x 10^{-13} F/cm, and the electrostatic potential of the gate metal relative to intrinsic Si is 0.3 V.

a) i) What is the electrostatic potential of the p-type silicon, relative to intrinisic silicon, in thermal equilibrium at room temperature?

Electrostatic potential = _____

ii) What is the built-in potential of the unbiased n+-p junction at room temperature?

Built-in potential = _____

Problem 3 contines on the next page.

Problem 3 continued

b) What are the flat band voltages, V_{FB}, of the MOS capacitor structures in Devices A and B, respectively?

V_{FB} (Device A) = _____

V_{FB} (Device B) = _____

c) The magnitude of the threshold voltage, $|V_T|$, for the MOS structure is 1 V in one of these devices, and 4 V in the other. Use this information and your knowledge of MOS capacitors to deduce the magnitude and sign of V_T for each of these MOS capacitors, i.e., the one made on p-Si and the made on n+-Si.

V_T (Device A) = _____

V_T (Device B) = _____

d) What is the condition (accumulated, depleted, or inverted) of the semiconductor surface under the thin oxide in each of these devices with a gate voltage, V_{GB}, of 2 Volts? Also give the identity and sheet density of any mobile holes or electrons induced at the oxide-silicon interface.

Device A:

Surface condition: _____

Carrier type and sheet concentration: _____

Device B:

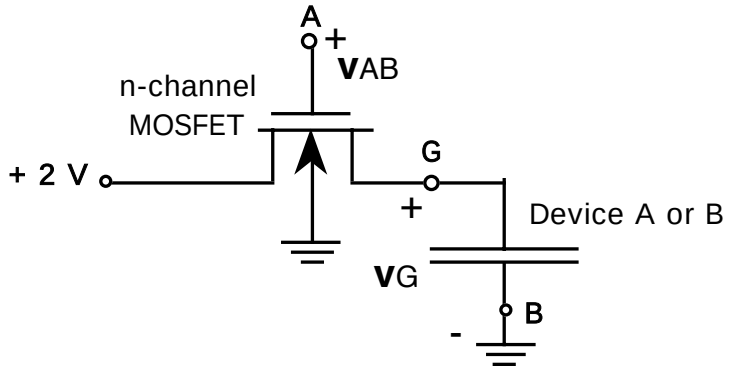
Surface condition: _____

Carrier type and concentration: _____

Problem 3 continues on the next page

Problem 3 continued

Next consider using these devices as the storage capacitor in the dynamic memory cell illustrated below. The MOSFET is an n-channel device with a threshold voltage, V_T, of 0.75 V (ignor any variation with v_{BS}) and a drain current in saturation of 0.1 $(v_{GS} - V_T)^2$ mA.



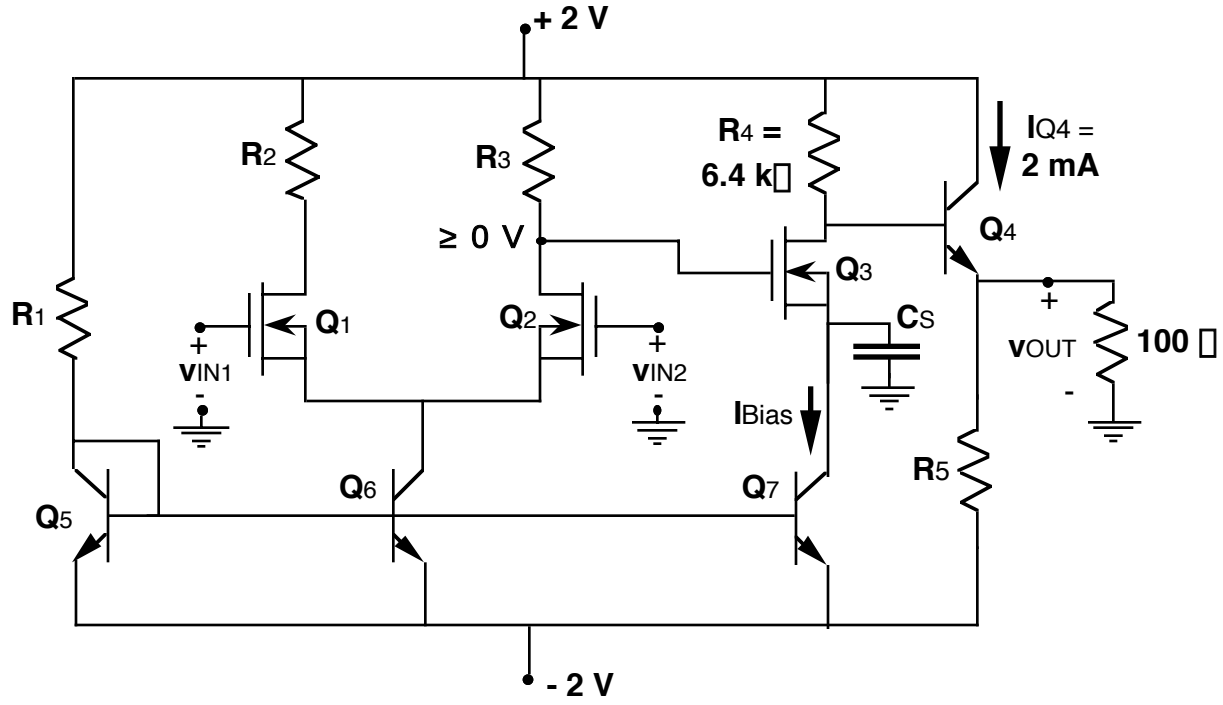
e) If V_{GB} is initially 0 V and V_{AB} is increased from 0 V to 2 V, what will the new value of V_{GB} be?

f) After having been 2 V for a long period of time, V_{AB} is switched to 0 V at t = 0. How will V_{GB} vary with time for t > 0? Give its initial value and describe how it changes with time, if at all.

End of Problem 3

Problem 4 - (27 points)

Consider the differential amplifier circuit illustrated below:



In this circuit the three n-channel MOSFETs are identical; they have a threshold voltage, V_T, of 1 V, a drain current in saturation of $2.5(v_{GS} - V_T)^2$ mA, and an Early voltage of 10 V. The MOSFETS do not operate properly if $(v_{GS} - V_T)$ is less than 0.2 V. The npn bipolar junction transistors (BJTs) all have forward betas, β_F, of 100, reverse betas, β_R, of 5, and an Early voltage of 50 V. The BJT sizes have been adjusted to that to a good approximation you may use $|V_{BE,ON}| = 0.6$ V; $|V_{CE,SAT}| = 0.2$ V. Assume C_S is a short at mid-band frequencies, and R_2 and R_3 are identical.

Note that value of the resistor R_4, the quiescent collector current on Q_4, and minimum quiescent voltage on the gate of Q_3 are indicated on the schematic, as are the supply voltages.

a) What must the bias level (I_{Bias}) on Q_3 be to have a quiescent output voltage of approximately 0 V? (Assume that the quiescent collector current of Q_4 is 2 mA, as indicated, and do not forget its base current.)

I_{Bias} = _____ mA

Problem 4 continues on the next page

Problem 4 continued

b) Select R_5 be to be consistent with a quiescent collector current in Q_4 of 2 mA, and a quiescent output voltage of approximately 0 V.

R_5 = _____ Ω

c) Select R_1 to give a bias current through Q_5 of 1 mA. You may ignor the base currents of Q_5, Q_6, and Q_7.

R_1 = _____ Ω

d) i) In the space below sketch a small signal linear equivalent <u>half</u> circuit one could use to calculate the signal voltage on the gate of Q_3 due to the difference-mode input signal, v_{in1} - v_{in2}. Find an expression for this voltage in terms of incremental linear equivalent circuit model parameters.

ii) Write an expression for the differential-mode voltage gain of the differential stage (Q_1, Q_2) in terms of the resistors, the MOSFET K-factors, and the quiescent bias levels of Q_1 and Q_2. Select R_2 (= R_3) and the drain current of Q_1 and Q_2 to maximize this voltage gain (magnitude).

I_D = _____ mA, R_2 (= R_3) = _____ Ω, $|A_{vd,max}|$ = _____

Problem 4 continues on the next page

Problem 4 continued

e) Suppose you can replace R_2 and R_3 with a current mirror made with p-channel MOSFETs with $|V_T| = 1$ V and $|V_A| = 20$ V. In the space below draw the schematic of such a current mirror, and discuss what inpact this would have on the voltage gain.

f) Looking at the output stage, what are the most positive and negative values of v_{out} possible? Explain your answers.

_____ < v_{out} < _____

End of Problem 4 and the Exam.