6.012 Electronic Devices and Circuits

Answers to Exam No. 2 -

(Average grade: 64.2%, St. dev. = 16.1%)

Problem 1 (Average grade: 21.5 / 30 = 72%, St. dev. = 5 / 30 = 27%)

(a) r is $1/g$, and $g = g_m / \beta_F = qI_C / kT \beta_F$, so we can relate I_C to r as follows

$$r = kT \beta_F / qI_C,$$

or, since we know r and want I_C, we can write this as

$$I_C = kT \beta_F / qr$$

Substituting $kT/q = 0.025$ V, $\beta_F = 200$, and $r = 5000$ Ohms, we get $I_C = 1$ mA.

(b) Having a large reverse beta is <u>not consistent</u> with having a small Early effect because the former requires that the collector be more heavily doped than the base, whereas the latter requires the opposite.

(c) The npn has lower defects because the electron diffusion coefficient is larger than that of holes (this ratio appears in expression for the emitter defect), and because the minority carrier diffusion length is longer for electrons than for holes for the same reason (this appears in expression for the base defect).

(d) All else being equal, the transconductance of the n-channel device is higher because the transconductance depends on K, which is proportional to the mobility, which is higher for electrons, the carriers in n-channel devices.

(e) The carriers in the channel of a MOSFET come from the source and drain regions (just the source in saturation).

(f) (i) The source can be used as the emitter (or collector), the drain as the collector (or emitter), and the substrate as the base. (The gate is not used, and should be shorted to the emitter.)

(ii) This transistor will have a large Early effect and the gain will be low because many of the minority carriers injected into the base from the emitter are not directed toward the collector (i.e., see a large base width).

Problem 2 (Average grade: 20.7 / 30 = 69%, St. dev. = 5.4 / 30 = 18%)

(a) The interface is depleted because the applied voltage, 0 V, is between the flatband voltage, - 0.5 V, and the threshold voltage, 1.0 V.

(b) (i) The current is just the reverse saturation current of the diode, 10^{-9} A.

(ii) The inversion layer charge, Q_N, is $-(V_{GS} - V_T) C_{ox}$, or -0.4×10^{-12} Coul.

(c) The answer is "no" because now any charge that formed in an inversion layer would be attracted to the n^+ region and an inversion layer can not be maintained. Looking at the structure as the source and gate of a MOSFET, we see immediately that $V_{GS} = 0$, and we need $V_{GS} > V_T$ to have a channel (i.e., inversion).

(d) (i) With the interface in accumulation, the diode's reverse characteristics are not changed and I_B is 10^{-9} A.

(ii) With the interface inverted the n+ region is made larger by the additional

"induced" n-region. The diode area is increased and thus the saturation current is increased proportionally (by a factor of 6 in this case so I_B is 6 x 10^{-9} A).

Problem 3 (Average grade: 22 / 40 = 55%, St. dev. = 9.6 / 40 = 24%)

(a) Assume the MOSFET is in saturation, as it must be for this to function well as an amplifier. Thus $I_D = K (V_{GS} - V_T)^2 / 2$, so $V_{GS} = V_T + \sqrt{2I_D / K}$. We find V_{GS} = 2.5 V.

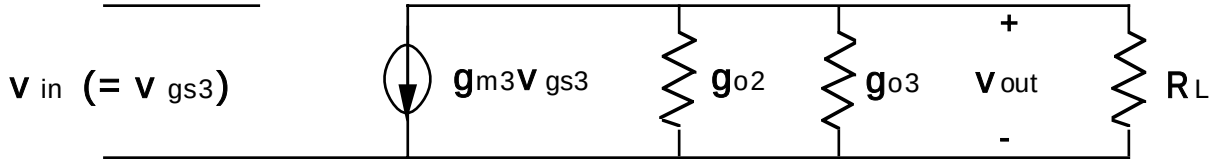
(b) The voltage drop across R is 6 V less two diode junction forward voltage drops of 0.6 V each, or 4.8 V, and the current we want to have through it is 1 mA. Thus R must be 4,800 Ohms, or 4.8 kOhms.

(c) (i) If V_{IN} is too positive the transistor Q_2 will go saturate and the transistor Q_3 will go out of it saturation region into its linear or triode region. The former occurs when V_{EC3} = 0.2 V, or when the drain of Q_3 is at 2.8 V, and the latter when V_{DG2} = - 0.5 V, or thus when the gate of Q_3 is at 2.8 - (-0.5) = 3.3 V. This (i.e., 3.3 V) is the maximum value V_{IN} can have.

(ii) If V_{IN} is too negative the transistor Q_5 will saturate. This occurs when V_{CE5} = 0.2 V, or when the source of Q_3 is at - 2.8 V. V_{GS3} is 2.5 V, as we found in part (a) when the circuit is function properly, so the gate of Q_3 must be at - 0.3 V, when its source is at - 2.8 V. This (i.e., - 0.3 V) is the minimum value V_{IN} can have.

(d) The DC power is found by either adding up the power dissipated in each element, or by finding the power supplied by the voltage sources. The later is easier because we have i mA flowing through Q_1 and Q_2, and 1 mA flowing through Q_2, Q_3, and Q_5. That is, the sources are supplying 2 mA, so the power is 6 V times 2 mA, or 12 mW (1.2 x 10^{-2} W).

(e) (i)



where $g_{m3} = \sqrt{2K_3 I_D}$ = 10^{-3} mS, $g_{o3} = \frac{I_D}{V_{A3}}$ = 10^{-4} mS, $g_{o2} = \frac{I_D}{V_{A2}}$ = 5 x 10^{-5} mS,

(ii) $A_v = - \frac{g_{m3}}{(g_{o3} + g_{o2} + G_L)}$ = - 6.25

(iii) We can write $A_v = - \frac{\sqrt{2K_3 I_D}}{\frac{I_D}{V_{A3}} + \frac{I_D}{V_{A2}} + \frac{1}{R_L}}$ and maximize this with respect to I_D, or we can note that the denominator is dominated by the V_{A3} term, and thus the entire expression varies as $1/\sqrt{I_D}$ and can be increased by decreasing I_D.